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(54) Title: METHODS AND CIRCUITS FOR ADAPTIVE EQUALIZATION AND CHANNEL CHARACTERIZATION USING LIVE DATA

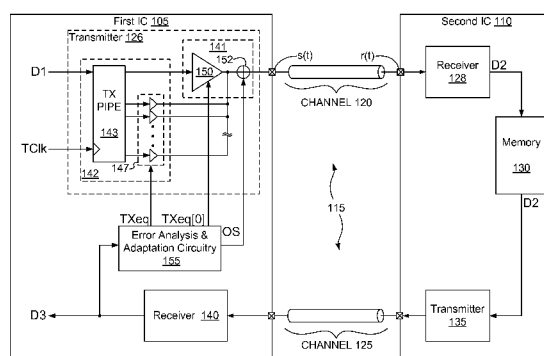


FIG. 1

(57) Abstract: A communication system supports high-speed communication over a signal lane that extends between respective transmitting and receiving integrated circuit (IC) devices. One or both of the IC devices includes an equalizer to offset channel characteristics that otherwise impair speed performance. A margining circuit on the receiving IC measures a timing margin of the received signal and adjusts the equalization settings for one or both transmitters to maximize the timing margin. Another embodiment compensates for performance asymmetry between ICs communicating over a bidirectional lane by instantiating relatively complex error analysis and adaptation circuitry on the higher-performance side of the lane. The error analysis and adaptation circuitry reduces the error margin of the transmitted signal to introduce bit errors at the receiver, analyzes the bit errors to measure ISI imposed by the channel, and adjusts voltage offsets of the continuous-time signal to compensate for the ISI. In some embodiments the receiver calculates the system response for diagnostics and for computing equalization settings.

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**METHODS AND CIRCUITS FOR ADAPTIVE EQUALIZATION
AND CHANNEL CHARACTERIZATION USING LIVE DATA**

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TECHNICAL FIELD

[0001] The present disclosure relates generally to the field of communications, and more particularly to high speed electronic signaling within and between integrated circuit devices.

BACKGROUND

[0002] The performance of many digital systems is limited by the interconnection bandwidth within and between integrated circuit devices (ICs). High performance communication channels between ICs suffer from many effects that degrade signals. Primary among them are frequency-dependent channel loss (dispersion) and reflections from impedance discontinuities, both of which lead to temporal spreading and consequent overlapping of individual signal pulses, or “symbols.” The resulting overlapping symbols interfere with one another, and thus adversely impact channel performance. This problem is known to those of skill in the art as “intersymbol interference” (ISI).

The quality of high-speed signals is largely dependent upon characteristics of the communication channel. In extreme cases, ISI imposed by the channel renders the received data unintelligible by a simple receiver. In these cases, transmitters and receivers

are equipped with various forms of equalizers designed to offset channel-induced distortion. These equalizers are often adjustable to account for differences between channels. Ideally, transmit and receive equalization work together to mitigate the degradation imposed by the channel, and thus allow increased data rates, reduced probability of communication errors, or both.

[0003] In some systems, memory systems for example, the communicating ICs have an asymmetry to them that complicates optimization of the transmit and receive equalization schemes applied to counter the effects of the corresponding channel. For example, a memory controller that communicates with one or more memory devices may benefit from a fabrication technology that is different from that best suited for manufacturing the memory devices. It is therefore often the case that a memory controller can employ circuitry that exhibits significantly better speed and power performance than the associated memory device or devices. This process and performance asymmetry between the communicating ICs complicates the task of optimizing equalization between the two devices.

[0004] Transmit and receive equalizers are adjusted for improved signal quality. To this end, receivers in high-speed communication systems sometimes include control circuitry that monitors various characteristics of incoming signals and adapts the associated equalization circuitry accordingly. Such equalization adjustments may be done once, to accommodate unique channel characteristics and process variations, or may be carried out continuously or periodically to adjust for time-variant parameters, such as supply-voltage and temperature.

[0005] Some methods for adapting equalization settings require a fixed, periodic training signal. Such methods require communication between the transmitter and receiver to coordinate equalization training, and cannot be used to derive appropriate equalization settings from normal traffic data ("live data"). Other methods for adapting

equalization settings do not require coordinated training, and are capable of operating on live data. For example, some adaptive equalizers rely upon a derivation of a least-mean-squared (LMS) algorithm called “sign-sign LMS” to establish and maintain appropriate filter coefficients on live data, but only if the received data sequence has approximately zero autocorrelation between successive symbols.

[0006] Adaptation methods that employ sign-sign LMS algorithms attempt to zero ISI components associated with data symbols of particular latencies. The final values of the equalizer settings provide some measure of the ISI components. However, this approach does not provide accurate measures of ISI for components within the temporal range of the equalizer if they cannot be forced to zero, and cannot provide measures of ISI components outside the temporal range of the equalizer. Such measures would be useful in both diagnostic and operational modes. Furthermore, the approximately zero autocorrelation requirement can affect the correctness of the sign-sign LMS algorithm when arbitrary data is being communicated. In light of these and other deficiencies, there is a need for improved methods and systems for measuring the system response (e.g., the single-bit or step response) of a channel during arbitrary data communication, both to diagnose signaling difficulties and to provide bases for establishing and maintaining equalization settings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The subject matter disclosed is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

[0008] Figure 1 illustrates a signaling system 100 in accordance with one embodiment.

[0009] Figure 2 is a flowchart 200 depicting a method of tuning transmitter 126 of Figure 1 in accordance with one embodiment.

[0010] Figure 3 depicts a high-speed communication system 300 in accordance with another embodiment.

[0011] Figure 4A depicts equalization control circuitry 400 that may be used as control circuitry 340 of Figure 3.

[0012] Figure 4B details an embodiment of a tap-value generator 425 of Figure 4A that generates a tap value using a sign-sign, least-mean-squared (SS-LMS) algorithm.

[0013] Figure 5A depicts error analysis and adaptation circuitry 500 that may be used to implement circuitry 360 of Figure 3.

[0014] Figure 5B details an embodiment of tap value generators 515 of Figure 5A that generates a tap value using a sign-sign, least-mean-squared (SS-LMS) algorithm.

[0015] Figure 6 is a flowchart 600 illustrating the operation of error analysis and adaptation circuitry 500 of Figures 5A and 5B as it would operate in a system similar to system 300 of Figure 3.

[0016] Figures 7A-7I are waveform diagrams illustrating the calibration sequence of flowchart 600 as it applies to e.g. system 300 of Figure 3.

[0017] Figure 8 is a flowchart 800 depicting the operation of error analysis and adaptation circuitry 360 of Figure 3 in accordance with another embodiment.

[0018] Figures 9A-9F are waveform diagrams illustrating the calibration sequence of flowchart 800 as it applies to e.g. system 300 of Figure 3.

[0019] Figure 10 depicts a communication system 1000 in accordance with another embodiment.

[0020] Figure 11 is a flowchart 1100 depicting a method of tuning transmitter 1025 and receiver 1030 of Figure 10 in accordance with one embodiment.

[0021] Figures 12A-12D are waveform diagrams illustrating the calibration sequence of flowchart 1100.

[0022] Figures 13A-13C are eye diagrams illustrating a calibration sequence in accordance with another embodiment.

[0023] Figure 14 is a flowchart 1400 depicting a method of tuning transmitter 1025 of Figure 10 in accordance with an embodiment in which adaptation circuitry 1050 serves as a margining circuit that measures a timing margin TM of signal $r(t)$ and adjusts the equalization settings of transmitter 1025 to maximize the timing margin.

[0024] Figure 15 depicts a communication system 1500 in accordance with another embodiment.

[0025] Figure 16 depicts an integrated circuit (IC) 1600 upon which a receiver 1605 is instantiated in accordance with one embodiment.

[0026] Figure 17A is a flowchart 1700 illustrating the operation of the system-response measurement circuit 1635 in IC 1600 of Figure 16 in accordance with one embodiment.

[0027] Figure 17B depicts a matrix equation 1750 that may be used to calculate SBR signals $SBR[3:0]$ in an embodiment of Figure 16 in which sampler 1620 and buffer 1630 provide four consecutive data samples D_i through D_{i-3} to system-response measurement circuitry 1635.

[0028] Figure 18 depicts a receiver 1800 in accordance with an embodiment that operates in much the same manner as receiver 1605 of Figure 16.

[0029] Figure 19A is a waveform diagram 1900 depicting the signal behavior at various nodes of receiver 1800 of Figure 18.

[0030] Figure 19B is a flowchart 1902 depicting the operation of one embodiment of receiver 1800 of Figure 18.

[0031] Figure 20 is a matrix equation 2000 that might be the product of flowchart

1902 of Figure 19B for the particular set of data patterns expressed in matrix 1903.

[0032] Figure 21 depicts a receiver 2100 in accordance with another embodiment.

[0033] Figure 22 is a flowchart 2200 depicting the operation of receiver 2100 of Figure 21 in accordance with one embodiment.

[0034] Figure 23 depicts a portion of a receiver 2300 that is in some ways like receiver 2100 of Figure 21, like-numbered elements being the same or similar.

[0035] Figure 24 is a flowchart 2400 depicting the operation of receiver 2300 of Figure 23 in accordance with one embodiment.

[0036] Figure 26 depicts an error sampler 2600 and a phase mixer 2605 for use in yet another embodiment.

[0037] Figure 26A depicts a matrix equation 2600 that may be used to calculate rising and falling edge responses RE[3:0] and FE[3:0] in an embodiment of Figure 16 in which sampler 1620 and buffer 1630 provide five consecutive data samples $Data_i$ through $Data_{i+4}$ to system-response measurement circuitry 1635.

[0038] Figure 26B depicts a matrix equation 2605 that is a simplified form of equation 2600 of Figure 26A.

DETAILED DESCRIPTION

[0039] Figure 1 illustrates a signaling system 100 in accordance with one embodiment. System 100 includes a first integrated circuit (IC) device 105 coupled to a second IC device 110 via a high-speed signal lane 115. In this example, lane 115 includes a write channel 120 and a read channel 125, which may comprise circuit-board traces. The write and read channels may be implemented over the same conductor or set of conductors in other embodiments.

[0040] Device 105 may be fabricated using a process that affords considerably higher transmit and receive circuit density and speed performance than the process

employed in fabricating device 110. In one embodiment, for example, the minimum feature size for input/output transistors on device 105 is less than 50% of the minimum feature size for input/output transistors on device 110. In other embodiments, device 105 has at least twice the number of interconnect layers as device 110, allowing more compact implementation of complex circuits. Communication system 100 accommodates the resulting performance asymmetry between devices 105 and 110 by instantiating the majority of the complex equalization circuitry on device 105. Transmit and receive channels 120 and 125 can thus support the same relatively high symbol rate without burdening the second IC device 110 with the area and power required to support complex equalization circuits.

[0041] Performance asymmetry between communicating devices might be desirable for reasons other than or in addition to process differences. For example, market demands may weigh more heavily on one of a pair of communicating devices, making it economically advantageous to minimize the complexity of that device. Also, total system cost can be reduced if the performance-enhanced circuitry can be instantiated on one or a relative few devices that communicate with a greater number of devices that employ less sophisticated equalization circuitry.

[0042] Device 105 includes an equalizing transmitter 126 that transmits a first bit sequence D1 over channel 120 as a continuous-time signal $s(t)$. A receiver 128 on second IC device 110 receives a signal $r(t)$ that is a version of signal $s(t)$ degraded by channel 120. Receiver 128 converts signal $r(t)$ into a second bit stream D2 that, in the absence of errors, matches bit sequence D1. Receiver 128 may be or include a decision circuit, such as a sampler or multi-bit analog-to-digital converter (ADC), that interprets received signal $r(t)$. Receiver 128 may additionally include e.g. an amplifier or equalizer disposed between channel 120 and the decision circuit, in which case the received signal $r(t)$ is considered to be at the input to the decision circuit.

[0043] Second IC device 110 includes memory 130, in this embodiment, to store second bit sequence D2. IC device 110 communicates bit stream D2 from memory 130 back to IC device 105 via channel 125, a second transmitter 135, and a second receiver 140, where it is received as bit sequence D3. Channel 125 may be implemented over the same physical conductor or conductors as channel 120 in other embodiments.

[0044] Transmitter 126 includes an output driver 141 and a multi-tap transmit equalizer 142. Transmit equalizer 142, in turn, includes a transmit pipe 143 and one or more sub-drivers 147. Output driver 141 and sub-drivers 147 function collectively to convert bit sequence D1 into continuous-time signal $s(t)$. The particular transmit equalizer in this embodiment may also be referred to as a finite-impulse-response (FIR) equalizer.

[0045] Equalizers on the transmit-side of a communication channel are sometimes referred to as “pre-emphasis equalizers” or “de-emphasis equalizers” because they emphasize or de-emphasize signal components prior to transmission over the channel to mitigate the effects of channel-induced ISI. For example, transmit equalization, often used to flatten the total amplitude response of a communication channel over a frequency band of interest, can be accomplished by (1) amplifying (emphasizing) the signal frequency components most sensitive to channel loss, (2) attenuating (deemphasizing) signal components that are less sensitive to channel loss, or (3) using a combination of frequency-dependent amplification and attenuation. The goal of equalization is typically to reduce or minimize the effects of ISI observed at the receive side of a channel (e.g. at signal $r(t)$ to receiver 128). Equalization is typically accomplished by adjusting one or more signal characteristics to mitigate the effects of ISI.

[0046] Channels 120 and 125 are assumed to act as simple low-pass filters in this example. For each transmitted symbol, equalization signals from sub-drivers 147 combine with the main signal from driver 141 to selectively deemphasize low-frequency signal components relative to high-frequency signal components, and thus to compensate in

advance for the low-pass nature of channel 120. When we refer to the ISI of channels 120 and 125, or similar channels in other embodiments, we also implicitly refer to non-idealities of the associated transmit and receive circuits, such as filtering or additive offsets that may exist in these circuits and the auxiliary circuits associated with them such as ESD structures. The transmitted and received versions $s(t)$ and $r(t)$ of a communicated continuous-time signal may be a binary, differential, AC-coupled voltage signal. Other embodiments may employ signals that are e.g. single-ended, multilevel, DC-coupled, or current driven. Moreover, the frequency response of a given channel may differ considerably from a simple low-pass filter. In the case of AC-coupled channels, continuous-time signals should have approximately zero DC content for proper operation, both during data transmission and during calibration operations described below. These and other variations will be evident to those skilled in the art.

[0047] Each of sub-drivers 147 is either a pre-tap sub-driver or post-tap sub-driver. If driver 141 has already transmitted the symbol value at the input to a given sub-driver, that sub-driver is a post-tap sub-driver; if driver 141 has yet to transmit the symbol value at the input to the sub-driver, that sub-driver is a pre-tap driver. Transmit pipe 143 might select, for example, N post-tap drivers and one pre-tap driver. In an alternate embodiment equalizer 142 and driver 141 can be realized as a high-speed digital-to-analog converter (DAC) structure that can drive arbitrarily complex waveforms (to the DAC resolution), and the transmit equalization may be computed in the digital domain on signals that are provided to the DAC inputs.

[0048] Different numbers of post-tap and pre-tap drivers may be provided in alternative embodiments, thereby allowing for transmit equalization based on values having different symbol latencies with respect to the main tap. Filter taps may also be timed to non-integer symbol latencies. The respective filter coefficients, or tap weights, of the sub-drivers can be controlled by application of transmit coefficients to the

corresponding control inputs. Alternatively, in the case of a DAC transmit equalizer, the filter coefficients can be applied by appropriate changes to DAC parameters. Further, each of the transmit coefficients may be adjusted over a range of values to tailor transmitter 126 to a particular channel and noise environment. Such adjustments can be applied once, e.g. at power-up, or can be adapted periodically during system operation to account for changes in the system environment that may impact performance. Methods and circuits for setting transmit coefficients in accordance with some embodiments are discussed below.

[0049] Driver 141 includes a main-tap driver 150 and an adder 152. The signal swing provided by main-tap driver 150 can be controlled by application of a transmit filter coefficient $TXeq[0]$, while the DC offset of signal $s(t)$ can be controlled by application of an offset-control signal OS to adder 152. Filter coefficients and DC offset signals may be referred to collectively as “transmit control signals.” In some instances, adder 152 may consist only of a wired connection to sum the outputs of multiple current sources. Driver 141 and equalizer 142 may be referred to separately and collectively as “signal-offset circuitry” because they all determine the extent to which signal $s(t)$ is offset from a reference level when expressing a given data bit or bit pattern. In the depicted embodiment the signal offsets induced by sub-drivers 147 and driver 141 are data dependent, which is to say that the offsets vary with patterns expressed in first bit sequence D1. In contrast, the offset induced by adder 152 is not data dependent. Note that DC offset OS is primarily useful when channel 120 is DC-coupled, as an AC-coupled channel will block any DC signal content.

[0050] ISI induced by channel 120 can produce errors in bit sequence D2. The error patterns in bit sequence D2 may depend, to a considerable extent, upon the ISI imposed by channel 120. Bit sequence D2 is conveyed back to first IC device 105 as a received bit sequence D3. IC device 105 is equipped with error analysis and adaptation

circuitry 155 that analyzes errors in bit sequence D3 to develop measures of ISI for channel 120 and to derive offset-control signals (filter coefficients TXeq, TXeq[0], and DC-offset signal OS in this embodiment) to compensate for ISI associated with channel 120. In the depicted embodiment, circuitry 155 obtains the second bit sequence D2 by reading the contents of memory 130, as delivered to IC device 105 as bit sequence D3. One or both of transmitter 135 and receiver 140 may be tuned to minimize errors associated with channel 125 so that bit sequence D3 accurately represents bit sequence D2. For example, receiver 140 may include equalization hardware that was previously adapted to compensate for the ISI of channel 125. This is also accomplished by altering the operation of transmitter 126 to margin communication on channel 120 so as to substantially increase the error rate in sequence D2, in a way that depends on the ISI of channel 125. For example, after such margining by transmitter 126, communication over channel 120 may have an error rate of 1E-3, while communication of channel 125 may have an error rate of 1E-6. While neither of these error rates may be sufficiently low for final operation in a given application, approximately 99.9% of errors observed in D3 are due to errors encountered in D2, allowing error analysis and adaptation circuitry 155 to use sequence D3 to observe the impact of ISI in channel 120. Alternatively, bit sequence D2 may be conveyed from memory 130 to first IC device 105 by means of a low speed signal channel, not shown. These or other steps may be taken to minimize errors in bit sequence D3 that are not attributable to channel 120.

[0051] Error analysis and adaptation circuitry 155 adjusts the offsets imposed by signals TXeq, TXeq[0], and OS to minimize the effects of ISI on signal $r(t)$ at the far end of channel 120. In other words, error analysis and adaptation circuitry 155 adjusts transmitter 126 such that the offsets collectively applied to signal $s(t)$ compensate for the undesired ISI imposed by channel 120, and therefore minimize the impact of channel-induced ISI on signal $r(t)$ and errors in bit sequence D2. Adjusting transmitter 126 by

observing errors in bit sequence D3 at first IC device 105, and thereby errors in bit sequence D2, as measures of transmit-channel characteristics reduces or eliminates the need for evaluating signal quality at receiver 128, which in turn reduces the requisite complexity of second IC device 110.

[0052] Receiver 128 and transmitter 135 may each be part of a transceiver that communicates with some core logic, such as or including memory 130. Receiver 128 may support timing and offset voltage adjustments, in which case the sample voltage and timing of receiver 128 may be centered within received data eyes of signal $r(t)$. Though not shown, receiver 128 can additionally include some simple receive-equalization circuitry. Such receive equalization circuitry may either have fixed equalization settings, or may be adaptively set by error analysis and adaptation circuitry 155, much like transmitter 126. Transmitter 135 can likewise provide some transmit equalization, but the circuitry employed for this purpose may be less complex than the circuitry transmitter 126 employs for this purpose. For example, transmitter 135 can have fewer filter taps than transmitter 126, or can have fixed tap settings that are known to provide a minimal baseline of equalization.

[0053] Figure 2 is a flowchart 200 depicting a method of tuning transmitter 126 of Figure 1 in accordance with one embodiment. First, at step 205, circuitry 155 reduces the error margin for channel 120 by changing one or more of the offset adjustments to transmitter 126. For example, the swing at signals $s(t)$ and $r(t)$ can be reduced by changing signals TX_{eq} and $TX_{eq}[0]$, or the DC offset can be adjusted up or down by changing signal OS, or both. The timing of transmitted data might also be modified to reduce the error margin, as detailed below in connection with another embodiment. Whatever the adjustment mechanism, the margin may be reduced such that ISI imposed by channel 120 introduces significant sampling errors at receiver 128. In this context,

“significant” means that the sampling errors have statistical significance sufficient to derive useful information about the ISI imposed by channel 120.

[0054] Next, at step 210, transmitter 126 transmits known data patterns in bit sequence D1, which receiver 128 interprets as second bit sequence D2, and stores in memory 130. Though not shown in Figure 1, system 100 may include for this purpose a separate “request” channel for conveying read and write commands and their associated addresses. Further, channel 120 may be one of multiple parallel channels, and the transmitter or transmitters associated with one or a subset of the channels can be tuned using e.g. the method of Figure 2 while another channel or channels can be used as a request channel.

[0055] Due to the margin reduction in step 205, bit sequence D2 should exhibit errors, which is to say that the patterns in bit sequence D2 should differ from the write patterns D1 of step 210, and the errors induced should depend on the ISI and offsets of channel 120. Circuitry 155 reads the erroneous patterns D2 from memory 130 (step 215). Transmitter 135, channel 125, and receiver 140 convey bit sequence D2 to first IC device 105, where it is received as bit sequence D3 free or substantially free of additional errors, so errors expressed in bit sequence D3 are measures of ISI induced errors for channel 120 and the associated circuitry. Circuitry 155 uses these measures of ISI induced errors--the erroneous data patterns in bit sequence D3--to calculate properties of the ISI induced in signal $s(t)$ by channel 120 (step 220). The resulting ISI calculations are then used to adjust the signal offsets introduced by one or more of signals TXeq, TXeq[0], or OS so as to counteract the effects of ISI (step 225). Steps 205 through 225 may be repeated a number of times to derive optimal signal offsets. Finally, the margin reduction of step 205 is reversed (step 230) to allow relatively error-free communication over channel 120. For example, if the output swing at $s(t)$ was reduced in step 205, then the output swing might be restored to its original value in step 230. In other embodiments receiver 128 may

convey bit sequence D2 to receiver 140 without first storing bit sequence D2 in a memory.

[0056] Figure 3 depicts a high-speed communication system 300 in accordance with another embodiment. System 300 includes first and second IC devices 305 and 310 separated by a signal lane 315. First device 305 includes a transmitter 320 that supports transmit equalization, e.g. of the type discussed above in connection with Figure 1. Device 305 also includes a receiver 322, which in turn includes a receive equalizer 327, a data sampler 330, a signal monitor 335, and equalization control circuitry 340. Second device 310 is similar to second device 110 of Figure 1, like-named elements being the same or similar.

[0057] Transmitter 320 includes a five-tap transmit equalizer, which in turn includes a FIFO buffer 323 and five coefficient multipliers 324. The transmit equalizer is a finite impulse response (FIR) equalizer in this example, though other types of equalizers may be used instead of or in addition to an FIR. Buffer 323 presents pre-tap data D_{i+2} and D_{i+1} , current (main) data D_i , and post-tap data D_{i-1} and D_{i-2} to respective coefficient multipliers 324. Multipliers 324 multiply the outputs of buffer 323 by respective transmit filter coefficients $TX\alpha[2:-2]$. An adder 325 sums the resulting products to obtain continuous-time signal $s(t)$ on channel 120. The products from multipliers 324 that correspond to pre- and post-cursor filter tap provide voltage offsets for signal $s(t)$ that correct for ISI; the product from the main tap ($D_i * TX\alpha[0]$) provides a voltage offset that largely determines the amplitude of signal $s(t)$ and that is adjusted such that the sum of the products of multipliers 324 has some desired peak transmitter output power; the signal OS provides a DC offset voltage for signal $s(t)$.

[0058] Receive equalizer 327 supports two post-cursor filter taps in this embodiment. Equalizer 327 is a decision-feedback equalizer (DFE) in this example,

though other types of equalizers may be used instead of or in addition to a DFE. For example, equalizer 327 may include one or more partial-response DFE (PrDFE) taps, e.g. of the type described in published U.S. Patent App. No. 2005111585 to Stojanovic et al. entitled "Partial Response Receiver." A FIFO buffer 345 presents first post-tap data $D3_{i-1}$ (first post cursor) and second post-tap data $D3_{i-2}$ to respective coefficient multipliers 346. Multipliers 346 multiply the outputs of a buffer 345 by respective tap coefficients $RX\alpha[2:1]$, and the sum of the outputs of multipliers 346 is subtracted from the incoming signal from channel 125 to produce an equalized signal V_{eq} . Alternatively, receive equalizer 327 could be implemented as a direct continuous-time, linear equalizer with tunable coefficients. In general, an equalizer can adjust the signal-to-ISI ratio (SIR) at a particular node in the receiver to achieve some desired characteristic, e.g. a low bit-error rate or, as in the case of a PrDFE, can speculatively apply multiple ISI offset corrections and later select the appropriate correction to achieve the desired characteristic.

[0059] An amplifier 350 within signal monitor 335 compares signal V_{eq} with a selected data level D_{lev} , outputting a signal indicative of a logic one (zero) if V_{eq} is greater than (less than) level D_{lev} . A sampler 355 periodically captures the output from amplifier 350 on rising edges of a receive clock signal $RClk$ to produce a series of error samples Err_i . Error samples Err_i are conveyed to equalizer control circuitry 340.

[0060] An amplifier 356 within data sampler 330 compares signal V_{eq} with reference voltage V_r (e.g. zero volts), outputting a signal indicative of a logic one (zero) if V_{eq} is greater than (less than) level V_r . A sampler 357 periodically captures the output from amplifier 356 on rising edges of receive clock signal $RClk$ to produce a series of data samples $D3_i$. Data samples $D3_i$ are conveyed to equalizer control circuitry 340 and to any other circuitry (not shown) to which the received data is directed. In accordance with the depicted embodiment, control circuitry 340 employs the data and error samples

to derive data level D_{lev} and receive equalization coefficients $RX\alpha[2:1]$ for receive equalizer 327.

[0061] IC device 305 additionally includes error analysis and adaptation circuitry 360 that controls the DC offset of signal $s(t)$ and the data-dependent signal offsets provided by each filter tap and the main cursor of transmitter 320. This control is obtained via tap-coefficient signals $TX\alpha[2:-2]$ and the DC offset-signal OS, which circuitry 360 derives from data patterns received in bit sequence $D3_i$. IC device 305 may additionally include a test-pattern generator 365 and a multiplexer 370. Error analysis and adaptation circuitry 360 can use these elements to select either a desired test pattern TP or write data WRITE for application to transmitter 320.

[0062] Because circuitry 360 uses bit sequence $D3_i$ as a measure of ISI for channel 120, errors associated with channel 125 can reduce the quality of measurement. The read path associated with channel 125 is therefore calibrated to reduce or eliminate errors associated with channel 125 while or before circuitry 360 calibrates transmitter 320. Other embodiments may include other ways of ensuring reliable read data from memory 130. For example, a more robust, relatively low-speed sideband return channel may be included for this purpose. Such a channel can be implemented over the same or different signal paths as the main data channel.

[0063] Figure 4A depicts equalization control circuitry 400 that may be used as control circuitry 340 of Figure 3. Control circuitry 400 includes a series of synchronous storage elements 420, tap-value generators 425, and a digital-to-analog converter (DAC) 430. Storage elements 420 and tap-value generators 425 together generate, from data and error samples $D3_i$ and Err_i , tap coefficients $RX\alpha[2,1,0]$. Tap value $RX\alpha[0]$ is a digital measure of the average amplitude of the received data symbols $D3_i$, which DAC 430

converts into voltage D_{lev} . The remaining tap values $RX\alpha[2,1]$ are the receive coefficients, e.g. for equalizer 327 of Figure 3.

[0064] The error comparisons that produce error signals Err_i are based upon the upper signal level defined by voltage D_{lev} and applied via amplifier 350. Control circuitry 400 thus only updates the tap values $RX\alpha[2,1,0]$ based upon measurements that take place when data sample $D3_i$ is a logic one. The data and error samples to tap-value generators 425 are delayed by one clock cycle, so error comparisons for sample $D3_i$ are delayed by one clock cycle. The enable terminals of tap-value generators 425 are therefore coupled to output terminal $D3_{i-1}$ to prevent updates to control circuitry 400 when the sample $D3_{i-1}$ is a logic zero. Other embodiments can include a second comparator/sampler pair to generate error samples when $D3_{i-1}$ is a logic zero, such as by comparing the incoming signal V_{eq} with the lower data level $-D_{lev}$, or the reference voltage to amplifier 350 can be varied over a number of values or ranges of values to facilitate additional testing and error-correction methods.

[0065] Figure 4B details an embodiment of a tap-value generator 425 of Figure 4A that generates a tap value using a sign-sign, least-mean-squared (SS-LMS) algorithm. Other algorithms, such as linear or gradient-descent LMS, can be used in other embodiments. Generator 425 includes an XNOR gate 431, a multiplier 435 that multiplies the output of XNOR gate 431 by a constant μ , an adder 440, and a register 445. XNOR gate 431 compares the corresponding data and error samples and presents its output to multiplier 435. The output of XNOR gate 431 represents a logic one for true and a logic negative one for false. The data and error samples represent the signs of the sampled values, so XNOR gate 431 has the effect of multiplying the signs and presenting the resulting product to multiplier 435. Multiplier 435 multiplies the product from XNOR gate 431 by a selected step size μ , which may be tailored for the selected filter tap. Adder 440 adds the output from multiplier 435 to the current contents of register 445, which is

then updated with the new count. Register 445 thus accumulates a count representative of the alpha value for the filter tap associated with the data samples of a particular latency.

[0066] Figure 5A depicts error analysis and adaptation circuitry 500 that may be used as circuitry 360 of Figure 3. Error analysis and adaptation circuitry 500 includes margin control circuitry 505, a deserializer 510, and four tap-value generators 515. Deserializer 510 reads five bits of bit sequence $D3i$ into a set of sequential storage elements 520. The data output from the center one of sequential storage elements 520 is treated as the main data for purposes of computing filter coefficients, and is coupled to the data inputs of each of tap-value generators 515. The data outputs of the remaining storage elements 520 are coupled to the error inputs E of respective tap-value generators 515. Note that these connections are specific to a particular adaptation method and data test pattern, described below. Margin control circuitry 505 issues an update signal UD to each tap-value generator 515 each time deserializer 510 contains an appropriately shifted/deserialized pattern for consideration. Margin control circuitry 505 also derives DC-offset signal OS and main-cursor coefficient $TX\alpha[0]$ as described below in connection with Figure 6.

[0067] Figure 5B details an embodiment of tap value generators 515 of Figure 5A that generates a tap value using a sign-sign, least-mean-squared (SS-LMS) algorithm. As in the example of Figure 4B, other algorithms, such as linear or gradient-descent LMS, can be used in other embodiments. Generator 515 includes an XOR gate 550, a multiplier 555 that multiplies the output of XOR gate 550 by a constant μ , an adder 560, and a register 565. XOR gate 550 compares the corresponding data and error samples on input terminals D and E and presents its output to multiplier 555. The output of XOR gate 550 represents a logic one for true and a logic negative one for false. The data and error samples represent the signs of the sampled values, so XOR gate 431 has the effect of

multiplying the signs and presenting the resulting product to multiplier 555. Multiplier 555 multiplies the product from XOR gate 550 by a selected step size μ , which may be tailored for the selected filter tap. Adder 560 adds the output from multiplier 555 to the current contents of register 565, which is then updated with the new count. Register 565 thus accumulates a count representative of the alpha value for the filter tap associated with the data samples of a particular latency. Update signal UD is asserted by control circuitry 505 (Figure 5A) when deserializer contains a data pattern D3 appropriately shifted for consideration.

[0068] Figure 6 is a flowchart 600 illustrating the operation of error analysis and adaptation circuitry 500 of Figures 5A and 5B as it would operate in a system similar to system 300 of Figure 3. Beginning with step 610, first IC 305 writes data patterns into memory 130, e.g. via a separate channel that may operate at a lower bit rate. Alternatively, the transmitter on the memory side might have a built in test sequence generator. As yet another alternative, it may be acceptable for step 610 to operate over channel 120 with some bit errors so long as the adaptation of step 620 is able to complete successfully. Some receive equalization algorithms, including the sign-sign LMS algorithm referenced previously, can operate on nearly arbitrary data. If such algorithms are used, step 620 may be able to adapt so that data D3 matches data D2 without regard to whether data D2 matches data D1.

[0069] Next, receiver 322 reads the patterns in memory 130 (step 615). Signal monitor 335 and data sampler 330 respectively derive error and data samples Err_i and $D3_i$ from the resulting incoming signal from second IC device 310. Equalization control circuitry 340 then derives data level D_{lev} and receive filter coefficients $RX\alpha[2,1]$ from the data and error samples to calibrate DFE 327 (step 620).

[0070] Once receiver 322 is properly calibrated, bit sequence $D3_i$ may be assumed to be identical or substantially identical to bit sequence $D2_i$. The adapted receive filter coefficients $RX\alpha[2:1]$ are held (step 625) or may continue to operate in an adaptive mode during the subsequent training of error analysis and adaptation circuitry 360.

[0071] Figures 7A-7I are waveform diagrams illustrating the calibration sequence of flowchart 600 as it applies to e.g. system 300 of Figure 3. Referring first to the diagram of Figure 7A, the waveform presented is an idealized transmission of a bit sequence 000100000 from transmitter 320. The waveform expresses logic ones and zeros as voltage levels normalized to plus one (+1) and minus one (-1), respectively, with respect to a transmit reference voltage V_{refT} . Figure 7B depicts the degraded response, a second continuous-time signal $r(t)$, of the waveform of Figure 7A at the input node of receiver 128. Though degraded, the signal of Figure 7B would likely be properly interpreted at each sample instant when compared to a reference voltage V_{refR} that receiver 128 uses to interpret incoming symbols. The received bit sequence $D2$ would thus be nearly identical to transmitted bit sequence $D1$, and would consequently not contain a statistically sufficient amount of information about the ISI imposed by channel 120 to adapt an equalizer. However, the ISI imposed by channel 120 may degrade the signal sufficiently that the bit sequence $D2$ still has more bit errors than are desirable for normal communication.

[0072] Returning to Figure 6, at step 627 error analysis and adaptation circuitry 360 sets offset signal OS to zero, transmit coefficient $TX\alpha[0]$ to 0.5, and filter coefficients $TX\alpha[2,1,-1,-2]$ to zero. An idealized depiction of the resulting waveform, when expressing the same bit sequence as Figure 7A, is depicted in Figure 7C. In step 630, error analysis and adaptation circuitry 360 directs transmitter 320 to write a steady stream of logic zeros to receiver 128: Figure 7D depicts an idealized version of the

transmitted waveform. The resulting bit sequence D2 is then read from memory 130 (step 635) to determine the ratio of ones to zeros.

[0073] Writing a sequence of zeros to memory 130 should result in a sequence of logic zeros stored in memory 130. As such, when the data is read back by first IC device 305 decision 640 should initially produce a “no” response: that is, the probability of a bit being interpreted as a logic one should not be observed to be 50%. The adaptation process would then move to step 645, in which case margin control circuitry within error analysis and adaptation circuitry 360 (e.g., margin control circuitry 505 of Figure 5) would increment offset signal OS and return to step 630. The margin control circuitry would continue to increment offset signal OS with each successive data pattern until the voltage VTL transmitted by transmitter 320 to express a logic zero matched the reference voltage Vrefr at receiver 128, a condition depicted in Figure 7E when $V_{TL} = V_{TLmar}$. As the voltage VTL that transmitter 320 employs to express a logic zero rises along the y-axis, the probability that receiver 128 will interpret that signal as a logic zero decreases. Voltage VTL is at its margin level V_{TLmar} when transmitted voltage VTL is equally likely to be interpreted as a one or a zero at receiver 128. In this example, the input to transmitter 320 that receives signal OS serves as a voltage-margin control port, and it is by controlling signal OS that error analysis and adaptation circuitry 360 sets the voltage level of signal $s(t)$ to a margin level V_{TLmar} that results in a received signal $r(t)$ equal to reference voltage Vrefr.

[0074] With the margin of channel 120 thus reduced, receiver 128 is extremely sensitive to channel ISI. In step 650, error analysis and adaptation circuitry 360 induces transmitter 320 to transmit two sequences of zeros separated by a single logic one. Given the low margin, the signal from transmitter 320 is likely to introduce errors at receiver 128 to be stored in memory 130. Figures 7F and 7G respectively depict an idealized waveform transmitted in step 650 and an exemplary resulting degraded waveform at

receiver 128. The degraded waveform of Figure 7G can be an average taken from a plurality of received data patterns to reduce the effects of noise. In Figure 7G an “X” denotes a bit that is equally likely to be received as a 1 or a 0 by receiver 128, a “1” indicates a bit that has a greater than 50% chance of being received as a logic one, and a “0” indicates a bit that has a greater than 50% chance of being received as a logic zero. The objective in this example is to compensate for ISI in the channel so that all bits, other than the one at time 0, are equally likely to be received as a one or a zero. In this example, the waveform of Figure 7G exhibits signal levels at times -2, -1, 1, 2, and 3, which would not be received as 50% ones and 50% zeros at receiver 128. Error analysis and adaptation circuitry 360 can use these biases toward logic one or logic zero to infer and correct for some of the channel ISI by adjusting the voltage offset coefficients $TX\alpha[-2, -1, 1, 2]$ provided to transmitter 320, as described below.

[0075] In step 655 the bit sequence D2 in memory 130 is read back to error analysis and adaptation circuitry 360 via transmitter 135, channel 125, and receiver 322. Circuitry 360 then analyzes the bit patterns to provide appropriate tap coefficient settings. Considering Figure 7G, the voltage level at time zero should strongly express a logic one, while the levels at the other sample instants should be at or near reference voltage V_{refr} . Circuitry 360 adjusts (step 660) the offset voltages applied to the pre- and post-cursor taps of transmitter 320 to bring the voltage levels at the sample instants other than that of the main cursor closer to voltage level V_{refr} . For example, applying the most likely sampled pattern 011101 in the example of Figure 7G to error analysis and adaptation circuitry 500 of Figure 5A would reduce $TX\alpha[-1]$ and $TX\alpha[1]$ to compensate for positive ISI at these bit positions, and increase $TX\alpha[-2]$ and $TX\alpha[2]$ to compensate for negative ISI at these bit positions. These changes act to reduce the differences between voltage V_{refr} and the voltage levels at that sample instants other than that of the main cursor, a result depicted

in Figure 7H. This process can be repeated until transmitter 320 is tuned appropriately, for example by counting through a predetermined number of calibration iterations until the offset signals $TX\alpha[2,1,-1,-2]$ to approach or dither about asymptotic levels. When finished, as determined by decision 665, offset signals $TX\alpha[2,1,-1,-2]$ are stored (step 670) and offset signal OS is returned to zero (step 675).

[0076] Transmitter 320 exhibits a maximum output power that can be divided among its five taps. For illustrative purposes, that output power may be normalized to a value of one. Error analysis and adaptation circuitry 500 therefore renormalizes offset signals $TX\alpha[2:-2]$ such that the sum of the absolute values of these five offset signals, which represents the total peak power output of transmitter 320, is equal to one (step 680). In this renormalization process, all of the offset signals $TX\alpha[-2:2]$ are scaled by the same constant, so that their relative weights remain the same. The resulting equalized waveform at receiver 128 may look something like the response of Figure 7I, which exhibits less ISI than the original similar waveform shown in Figure 7B.

[0077] System 300 of Figure 3 can also be used to directly measure the single bit response of channel 120 with a method similar to that shown in Figure 6. Again, we refer to the waveform of Figure 7B as indicative of an initial continuous-time signal at receiver 128 of second IC device 310, when offset signal OS is set to zero and first IC device 305 sends a single “1” bit surrounded by sequences of “0” bits on either side. Now, if offset signal OS is set to a sufficient negative value $-X$, it is possible to shift the entire waveform of Figure 7B below the reference voltage V_{refr} . In this condition, receiver 128 would sample the signal with $P_1=0$ at every bit position, indicating that the initial waveform of Figure 7B never exceeded V_{refr} by more than X . Then, first IC device 305 gradually increases offset signal OS while retransmitting the waveform, possibly multiple times, at each of a number of offset-signal settings. At some OS setting, second IC device 310 will

receive the waveform with $P_1[0]=50\%$. At this point, the (negative) value of OS indicates the amount by which the original waveform $r(t)$ in Figure 7B exceeded V_{refr} at RxC_{clk} time 0. As the process continues, first IC device 305 similarly records the values of OS at which each of the sample probabilities $P_1[i]$ crosses 50%. These values of signal OS represent measures of the amplitude of waveform 7B, relative to V_{refr} , at each of the sample times i . In the embodiment of Figure 10, discussed below, this procedure could be extended to include sweeping of the transmit or receive phase, allowing the shape of the waveform shown in Figure 7B to be effectively observed at times between the integer sample clock times.

[0078] Figure 8 is a flowchart 800 depicting the operation of error analysis and adaptation circuitry 360 of Figure 3 in accordance with another embodiment. Beginning at step 805, error analysis and adaptation circuitry 360 sets transmit coefficients $TX\alpha[2,1,-1,-2]$ to zero and $TX\alpha[0]$ to one. Next, in step 810, transmitter 320 writes data patterns into memory 130 via channel 120. Receiver 322 then, at the direction of error analysis and adaptation circuitry 360 or some other control mechanism, reads (step 815) the resulting data patterns from memory 130 via channel 125 and calibrates DFE 327 in the manner discussed above (step 820). Once the appropriate receive coefficients are established, equalization control circuitry 340 either holds the values of the receive coefficients (step 825) or continues to adapt these values during subsequent system operation.

[0079] Transmitter calibration begins at step 830, at which time error analysis and adaptation circuitry 360 causes transmitter 320 to transmit a step function as a sequence of zeros followed by a sequence of ones. An idealized form of the transmit waveform is depicted in Figure 9A, in which the low and high transmit voltage levels are depicted as levels V_{TL} and V_{TH} , respectively. Data D1 expressed by the waveform is bitwise

associated with the timing of the transmit clock TXCLK. With reference to Figure 9B, the received waveform associated with the transmit step function of Figure 9A will include some effects of ISI. This is depicted as dotted lines and shadings illustrative of an average of the received signals associated with some number of transmitted steps from transmitter 320. The decimal values along the waveform of Figure 9B refer to the probabilities of the depicted waveform being interpreted by receiver 128 as a logic one on an associated rising edge of receive clock RxClk. For each receive clock cycle -4 through -1 the probability of receiver 128 interpreting the signal as a logic one is very nearly 0.0, whereas the probabilities at clock cycles 0 through 4 is very nearly 1.0. These probabilities indicate that receiver 128 accurately reproduces the pattern of Figure 9A. Even though this particular pattern may be received nearly error free by receiver 128, the effects of ISI may lead to more likely bit error occurrences when different data patterns are transmitted.

[0080] Returning to Figure 8, data read in step 835 is analyzed by error analysis and adaptation circuitry 360 to determine whether the probability of a logic one at clock cycle -2 of the receive clock is greater than or equal to 0.2 and the probability of a logic one at clock cycle 3 of the receive clock is less than or equal to 0.8. If not, then the error analysis and adaptation circuitry decrements filter coefficient $TX\alpha[0]$ (step 845) and the process returns to step 830. Step 845 decreases the output swing of transmitter 320, and these reductions continue until the received data D2 begins to exhibit bit errors. Averaging the results from received patterns over time will eventually cause decision 840 to exhibit a “yes” condition. Error analysis and adaptation circuitry 360 will thus alter filter coefficient $TX\alpha[0]$ to reduce the swing-voltage margin until bit sequence D2 exhibits statistically significant errors. In this example, the input to transmitter 320 that receives filter coefficient $TX\alpha[0]$ serves as the voltage-margin control port, and it is by

controlling coefficient $TX\alpha[0]$ that error analysis and adaptation circuitry 360 sets the swing voltage of signal $s(t)$ to a marginal level.

[0081] Figures 9C and 9D respectively show the reduced-amplitude transmit pattern and the resulting reduced-amplitude received signal. Decision 840 may be based upon errors counted over numerous received data patterns and statistically analyzed to determine the probabilities of the data exhibiting a logic one value for each of the clock cycles of interest. In Figure 9D, for example, clock cycle -2, should always exhibit a zero given the transmitted waveform of Figure 9C; clock cycle -2 nevertheless exhibits a 0.3 probability of being a logic one due to the low margin of error. Likewise, clock cycle 2 should always be a logic one but exhibits only a 0.8 probability of being a logic one. The probabilities expressed for the various clock cycles, when related to the received data pattern, provide measures of the ISI imposed by channel 120, and can thus be used by error analysis and adaptation circuitry 360 to adjust equalizing transmitter 320.

[0082] Returning to Figure 8, error analysis and adaptation circuitry 360 writes data patterns 00001111 Y times into Y respective memory addresses (step 850). Error analysis and adaptation circuitry 360 then reads back that data patterns and calculates the ones probability for each bit or a subset of the bits (step 860). In this example, error analysis and adaptation circuitry 360 calculates ones probabilities $P1[3:-3]$.

[0083] Next, in a for-loop 865A-B, error analysis and adaptation circuitry 360 adjusts transmit parameters $TX\alpha[-2,-1]$ as needed to close the differences between the ones probabilities of bits -2 and -1 of the data patterns with that of bit -3. If the ones probability $P1[k]$ is greater than $P1[-3]$, then transmit parameter $TX\alpha[k]$ is decremented (decision 867 and step 869). If the ones probability $P1[k]$ is less than $P1[-3]$, then transmit parameter $TX\alpha[k]$ is incremented (decision 871 and step 873).

[0084] In a second for-loop 875A-B, error analysis and adaptation circuitry 360 adjusts transmit parameters $TX\alpha[2,1]$ as needed to close the differences between the ones probabilities of bits 2 and 1 of the data patterns with that of bit 3. If the ones probability $P1[k]$ is greater than $P1[3]$, then transmit parameter $TX\alpha[k]$ is decremented (decision 877 and step 879). If the ones probability $P1[k]$ is less than $P1[3]$, then transmit parameter $TX\alpha[k]$ is incremented (decision 881 and step 883).

[0085] The process returns to step 850 after both for-loops complete. Over time, repeated application of the for loops to sets of data patterns will produce an optimal or near-optimal set of transmit parameters $TX\alpha[2,1,-1,-2]$. Figure 9E depicts a hypothetical example of a resulting equalized signal. As in the example of Figure 6, the offset signals may then be renormalized to reverse the initial margin reduction and restore the signal, in which case the equalized waveform may look something like the response of Figure 9F.

[0086] Because the method shown in Figure 8 does not rely on a DC offset signal, it may be better suited for use in AC-coupled links than the procedure shown in Figure 6. In an AC-coupled link, the particular test patterns indicated in Figure 8 may be segments of larger repeating test patterns that maintain overall DC balance.

[0087] As noted above, transmitters 320 exhibits a maximum output power that is divided among its five taps, and this power may be normalized to a value of one. Error analysis and adaptation circuitry 500 may therefore renormalize offset signals $TX\alpha[2:-2]$ such that the sum of the absolute values of the five offset signals is equal to one.

[0088] Figure 10 depicts a communication system 1000 in accordance with another embodiment. System 1000 includes a first IC device 1005 coupled to a second IC device 1010 via a high-speed signal lane or channel 1015. As in prior embodiments, device 1005 may be fabricated using a process that affords considerably higher transmit and receive circuit density and speed performance than the process employed in

fabricating device 1010. Communication system 1000 accommodates the resulting performance asymmetry by instantiating the majority of the complex equalization circuitry on device 1005. In particular, margin reduction and error analysis and adaptation circuitry are located on device 1005.

[0089] Device 1005 includes an equalizing transmitter 1025 that transmits a first bit sequence D1 over channel 1015 as a continuous-time signal $s(t)$. A receiver 1030 on second IC device 1010 receives a signal $r(t)$ that is a degraded version of signal $s(t)$. Receiver 1030 converts signal $r(t)$ into a second bit stream D2 that, in the absence of errors, matches bit sequence D1. Second IC device 1010 supports some form of signal path 1035 for conveying bit sequence D2 back to transmitter 1025. Bit sequence D2 can be stored in the receiving device, as in the foregoing examples, or may be stored in IC device 1005 or elsewhere. Many suitable methods of storing bit sequences and conveying them between IC devices are known to those of skill in the art.

[0090] Transmitter 1025 includes a two-tap transmit equalizer, which in turn includes a FIFO buffer 1037 and two coefficient multipliers 1040. Buffer 1037 presents current (main) data $D1_i$ and post-tap data $D1_{i-1}$ to respective coefficient multipliers 1040. Multipliers 1040 multiply the outputs of buffer 1037 by respective tap coefficients $TX\alpha[1:0]$. An adder 1045 adds the resulting products to obtain continuous-time signal $s(t)$. The product of $TX\alpha[0]$ and $D1_i$ establishes the voltage offset used to convey the main data, whereas the product of $TX\alpha[1]$ and $D1_{i-1}$ establishes the voltage offset to be added to the main signal to compensate for first-post-cursor ISI. Different numbers of post-tap and pre-tap drivers may be provided in alternative embodiments.

[0091] IC device 1005 is equipped with error analysis and adaptation circuitry 1050 that analyzes errors in bit sequence D2 to develop measures of ISI for channel 1015

and to derive the offset-control signals for transmitter 1025—filter coefficients $TX\alpha[1:0]$ in this embodiment—and a DC-offset control signal OS for receiver 1030.

[0092] As in prior embodiments, error analysis and adaptation circuitry 1050 adjusts the transmit filter coefficients to minimize the effects of ISI on signal $r(t)$ at the receiver. However, instead of adjusting the DC offset at transmitter 1025 to correct for DC channel offset errors, error analysis and adaptation circuitry 1005 remotely controls the DC offset of received signal $r(t)\#$, or controls a reference voltage that receiver 1030 uses to interpret signal $r(t)\#$. Sampler 1060 thus samples an offset corrected received signal $r(t)$. Error analysis and adaptation circuitry 1050 thus adjusts both the transmitter and the receiver such that the offsets collectively employed to equalize signal $s(t)$ and interpret signal $r(t)$ closely compensate for the undesired ISI imposed by channel 1015, and therefore minimize the impact of channel-induced ISI on signal $r(t)$. As in prior embodiments, we consider non-idealities of transmitter 1025 and receiver 1030, such as filtering characteristics or random offsets, to be part of the ISI imposed by channel 1015.

[0093] Error analysis and adaptation circuitry 1050 derives a transmit clock $TClk$ from a reference clock $Clkref$, and is capable of varying the phase of the transmit clock to alter the error margin of signal $r(t)$ for reasons discussed below. Though receiver 1030 includes some of the requisite correction circuitry, the majority of the complex circuitry required to measure and adapt for ISI is located on first IC device 1005. Specifically, IC device 1005 controls the margining of the transmitted waveform $s(t)$ to induce statistically significant errors in D2. It also updates the various correction coefficients based on observation of bit sequence D2.

[0094] Turning now to second IC device 1010, receiver 1030 includes a sampler 1060, an adder 1065, and an offset register 1070. Adder 1065, responsive to offset signal OS from register 1070, adjusts the DC offset receiver 1030 uses to interpret the received

signal. In this example, the applied offset OS adjusts received signal $r(t)$ to signal $r(t)$ at the input of sampler 1060. Error analysis and adaptation circuitry 1050 is coupled to register 1070, via lane 1015 or some other means, and can write offset-control signal OSc to register 1070. Error analysis and adaptation circuitry 1050 can therefore remotely control the DC offset used to interpret signal $r(t)$. In other embodiments circuitry 1050 can issue other types of receiver control signals to adjust offset or equalization parameters with which receiver 1030 can interpret signal $r(t)$. Sampler 1060, a single-bit decision circuit, may be extended to multiple bits in other embodiments.

[0095] Figure 11 is a flowchart 1100 depicting a method of tuning transmitter 1025 and receiver 1030 of Figure 10 in accordance with one embodiment. First, at step 1102, receiver 1030 synchronizes receive clock signal RClk with that data input to sampler 1060. Such synchronization can be carried out using a number of conventional circuits and methods that are well known to those of skill in the art. In some embodiments, for example, receiver 1030 may include clock and data recovery circuitry (not shown) that automatically recovers reference clock signal RClk from incoming signal $r(t)$. Other embodiments may establish appropriate relative timing for clock signal RClk and received signal $r(t)$ by sweeping one or both signals to vary their relative phase over a bit time while monitoring the bit error rate (BER). A relative phase adjustment that results in a relatively low BER indicates proper phase alignment between signals RClk and $r(t)$. Some embodiments may identify a signal eye as a range of phase offsets over which the BER remains below a threshold value and adjust the relative phases of signals RClk and $r(t)$ to center the sample instants within the signal eye.

[0096] Next, at step 1105, error analysis and adaptation circuitry 1050 presets a number of variables. Among them, coefficient $TX\alpha[1]$ is set to zero, a direction bit Dir is set to 1b, a phase-offset variable ΔPH is set to some maximum phase offset PH_{max} , and

first and second phase variables PH1 and PH2 are each set to an initial value Φ_{init} that corresponds to the phase setting of step 1102.. The purposes of these variables will become clear in the following description.

[0097] Next, first IC device 1005 transmits a first data pattern to second IC device 1010 some number of times (step 1110). In this example, the first data pattern is a sequence of zeros followed by a sequence of ones such that signal $s(t)$ exhibits a step function. Figure 12A is a waveform diagram 1200 showing an exemplary step function 1205 timed to transmit clock TClk with a rising edge at transmit time zero. Figure 12A also shows the averaged response $r(t)$ to a number of step functions. The response is shaded to illustrate ranges for the averaged data.

[0098] Returning to Figure 11, receiver 1030 interprets the received signals $r(t)$ and conveys the resulting patterns back to error analysis and adaptation circuitry 1050 via signal path 1035 (step 1115). Error analysis and adaptation circuitry 1050 then considers the probability that the sampled data at time zero of receive clock RClk is interpreted as a logic one (decision 1120). If the probability is not 50%, then error analysis and adaptation circuitry 1050 delays or advances the phase of transmit clock TClk if the probability is greater than or less than 50%, respectively (step 1125), and stores the resulting TClk phase as PH1 (step 1130). In the example of Figure 12A, the probability $P_0[1]$ that the sampled data at time zero is interpreted as a logic one is greater than 50%, so error analysis and adaptation circuitry 1050 will induce some delay in transmit clock TClk.

[0099] The process of transmitting, receiving, and interpreting data patterns repeats until the probability $P_0[1]$ that the sampled data at time zero of the receive clock is interpreted as a logic one is 50%. Figure 12B is a waveform diagram 1215 illustrating this condition. Error analysis and adaptation circuitry 1050 then holds phase offset PH1 and begins transmitting a second data pattern (step 1140).

[00100] In this example, transmitter 1025 includes a timing-margin control port that allows error analysis and adaptation circuitry 1050 to control the timing margin of the continuous-time signal in response to a timing-margin control signal corresponding to the phase of TClk.

[00101] Figure 12C is a waveform diagram 1230 showing an exemplary second pattern—a sequence of logic one values interrupted by a single logic zero—timed to transmit clock TClk and adjusted to phase PH1 in the manner detailed above. Figure 12C also shows the averaged response $r(t)$ to a number of the transmitted patterns. The zero-to-one transition of this second pattern crosses voltage V_{refr} earlier than the step function of Figure 12B, so the probability $P_0[1]$ that the sampled data at time zero of receive clock RClk is interpreted as a logic one is no longer 50%. In other words, there is now a different phase offset at which the data would have to be sampled at to produce a 50% probability of being interpreted as a logic one. This phase difference results from channel ISI, and it is an object of error analysis and adaptation circuitry 1050 to adjust the filter coefficients of transmitter 1025 to minimize this difference.

[00102] Returning to Figure 11, receiver 1030 interprets the received signals $r(t)$ and conveys the resulting patterns back to error analysis and adaptation circuitry 1050 via signal path 1035 (step 1145). Error analysis and adaptation circuitry 1050 then considers the probability that the sampled data at time zero of receive clock RClk has been interpreted as a logic one (decision 1150). If the probability is less than or greater than 50%, then error analysis and adaptation circuitry 1050 advances or delays the phase of transmit clock TClk, respectively (step 1155), and stores the resulting TClk phase as PH2 (step 1160). In the example of Figure 12C, the probability $P_0[1]$ that the sampled data at time zero is interpreted as a logic one is greater than 50%, so error analysis and adaptation circuitry 1050 induces some delay in transmit clock TClk.

[00103] The process of transmitting, receiving, and interpreting the second data patterns repeats until the probability $P_0[1]$ that the sampled data from the rising edge of the received waveform at time zero is interpreted as a logic one is again 50%. Figure 12D is a waveform diagram 1245 illustrating this condition. Error analysis and adaptation circuitry 1050 then holds phase offset PH2 and the process continues to step 1165.

[00104] At step 1165, error analysis and adaptation circuitry subtracts phase PH1 from phase PH2; the absolute value of the resulting phase difference is stored as a new phase difference ΔPH_n . Because an object of error analysis and adaptation circuitry is to minimize this phase difference, when the new phase difference ΔPH_n is less than the prior phase difference ΔPH (or the initial value of ΔPH in the case of the first iteration), the current setting for $TX\alpha[1]$ is considered an improvement over the previous setting. Consequently, per decision 1170, if the new phase difference ΔPH_n is less than the prior phase difference ΔPH , then phase difference ΔPH is updated to the new phase difference ΔPH_n (step 1175) and filter coefficient $TX\alpha[1]$ is further adjusted in the current search direction, Dir (step 1180).

[00105] Step 1175 reflects a reduction in the phase difference from the prior value, which is interpreted as an improvement. The following step 1180 updates the filter coefficient before returning to step 1110 to determine whether better results might be obtained with a different coefficient. Should decision 1170 determine that the phase difference has increased, then direction variable Dir is negated in step 1185 to reverse the direction of the filter-coefficient change of step 1180.

[00106] If left to operate over a sufficient time period, error analysis and adaptation circuitry 1050 will eventually settle upon and dither about a setting for coefficient $TX\alpha[1]$ that minimizes or nearly minimizes the phase difference between the zero-to-one transitions exhibited by the first and second data patterns. Error analysis and adaptation

circuitry 1050 can then employ the optimized coefficient for data transmission. Such optimization techniques are commonly referred to as “descent” based searches. Because descent searches operate to continually reduce an observation that is to be minimized, regardless of knowledge of the underlying connection between the adjustment and the observation, they are often well suited to a wide variety of equalizers that may not have a simple mapping between adjustment ports and observed ISI components, or in cases where manufacturing variations may prevent sufficient knowledge of the mapping.

[00107] Embodiments of the communication system detailed on connection with the foregoing figures can comprise a communication channel; an equalizing transmitter transmitting a continuous-time signal over the communication channel; a receiver coupled to the communication channel and sampling the continuous-time signal to obtain a bit sequence, wherein the continuous-time signal exhibits an error margin at the receiver; and wherein the equalizing transmitter includes adaptation means for reducing the error margin to induce errors in the bit sequence and for deriving, from the errors, signal offsets for the continuous-time signal. The signal offsets may control the equalizing of the transmitter.

[00108] Integrated-circuit devices in accordance with some embodiments may comprise: a transmitter having a transmitter input port to receive a first bit sequence, an output driver to convert the first bit sequence into a continuous-time signal, and an offset-adjustment port to adjust a voltage offset of the continuous-time signal; an input port to receive an erroneous second bit sequence derived from the continuous-time signal and including errors, wherein the errors are differences between the first and second bit sequences; and error analysis and adaptation circuitry coupled to the input port and the offset-adjustment port, the error analysis and adaptation circuitry to derive a control signal from the errors and apply the control signal to at least one of an equalizer and a DC offset control port to adjust the continuous-time signal. In such devices, adjusting the

voltage offset of the continuous-time signal may adjust a DC component of the continuous-time signal, the voltage offset of the continuous-time signal may vary with bit patterns expressed in the first bit sequence, the transmitter may be an equalizing transmitter that includes a filter-coefficient input port, and wherein the offset signal is applied to the filter-coefficient input port, and the at least one equalizer and DC offset control port may be instantiated on the integrated circuit device.

[00109] Communication systems in accordance with some embodiments of the above-described circuits and method may comprise: (a) a transmitter instantiated on a first integrated circuit device and having: a transmitter input port to receive a first bit sequence; a transmitter output port; transmit circuitry coupled between the transmitter input port and the transmitter output port to convert the first bit sequence into a first continuous-time signal on the transmitter output port; and margin control circuitry coupled to the transmit circuitry, the margin control circuitry to adjust a signal offset of the first continuous-time signal; (b) a communication channel coupled to the transmitter output port, the communication channel to convey the first continuous-time signal as a second continuous-time signal degraded by intersymbol interference; (c) a receiver instantiated on a second integrated circuit device and coupled to the transmitter output port via the first communication channel, the first receiver to convert the second continuous-time signal into a second bit sequence; (d) error analysis circuitry coupled to the receiver, the error analysis circuitry to derive, from the second bit sequence, a measure of the intersymbol interference; and (e) adaptation circuitry coupled between the error analysis circuitry and the transmit circuitry, the adaptation circuitry to adjust the transmit circuitry responsive to the measure of intersymbol interference. In such systems, the signal offset may be a timing offset or a DC offset, and may be data-dependent. Also, the adaptation circuitry may adjust a filter coefficient of the transmit circuitry responsive

to the measure, or adjust a DC offset of the transmit circuitry responsive to the measure.

The error analysis circuitry may be instantiated on the first integrated circuit device.

[00110] Figures 13A-13C are hypothetical eye diagrams illustrating a calibration sequence, in accordance with another embodiment, that can be implemented using e.g. system 1000 of Figure 10. Sampling an incoming signal using a reference voltage and sample instant within an eye opening may be expected to result in a properly received signal. Thus, the opening (vertical dimension) of a given signal eye is a measure of the voltage margin for a repeatedly sampled signal and the width (horizontal dimension) is a measure of the timing margin TM.

[00111] In each of Figures 13A-C, offset signal OS to receiver 1030 is adjusted such that the reference voltage V_r against which receiver 1030 interprets incoming signal $r(t)$ is vertically centered within the eye. In Figure 13A, the phase of transmit clock signal TCclk, and therefore the timing of signal $r(t)$, is adjusted such that signal $r(t)$ is aligned to clock signal RClk and the sample instants are centered horizontally within the data eye. This initial phase adjustment is labeled ϕ_{init} in Figure 13A. Given these settings, the probability P_{err} of a sampling error should be low, but possibly higher than is desired in a particular application.

[00112] Referring now to Figure 13B, the transmit clock signal TCclk is delayed to a phase offset ϕ_1 , such that the received eye at $r(t)$ is delayed relative to the sample instants. At this new TCclk phase, the probability P_{err} of a sample error exceeds some threshold, 0.02 in this example. The timing at which errors exceed a threshold may be interpreted as one timing boundary for the eye. Figure 13C depicts the case in which TCclk is advanced to a new phase offset ϕ_2 , such that the received eye at $r(t)$ is advanced relative to the sample instants. At this new TCclk phase the probability P_{err} of a sample error again exceeds the same threshold used in the example of Figure 13B. Phase offset ϕ_2 demarks

the second edge of the signal eye, and can be used with phase offset ϕ_1 to find with eye width and eye center. A procedure similar to the one detailed in Figure 11 and described above could be used to maximize the eye width, $|\phi_1 - \phi_2|$. In such a procedure, error analysis and adaptation circuitry 1050 reduces the timing margin in the manner shown in Figures 13B and 13C by alternating the phase of transmit clock signal TC1k to measure the eye width at a given adaptation setting for TX α [1]. By adjusting the adaptation setting, and remeasuring the eye width, circuitry 1050 determines whether the adjustment of TX α [1] increased or decreased the eye width, and continues or reverses the adjustment appropriately.

[00113] Returning to Figure 10, error analysis and adaptation circuitry 1050 can reduce the timing margin in the manner shown in Figures 13B and 13C by adjusting the phase of transmit clock signal TC1k. First IC device 1005 can reduce the error margins sufficiently to introduce errors in signal D2 that can be used as detailed above to optimize equalization and offset settings in one or both of transmitter 1025 and receiver 1030. After this optimization, IC device 1005 can return TC1k to the original phase to reverse the margin reduction.

[00114] Figure 14 is a flowchart 1400 depicting a method of tuning transmitter 1025 of Figure 10 in accordance with an embodiment in which adaptation circuitry 1050 serves as a margining circuit that measures a timing margin TM of signal r(t) and adjusts the equalization settings of transmitter 1025 to maximize the timing margin. This embodiment is discussed in connection with the eye diagrams of Figures 13A-C.

[00115] First, at step 1402, receiver 1030 synchronizes receive clock signal RC1k with that data input to sampler 1060. As noted previously in connection with flowchart 1100 of Figure 11, such synchronization can be carried out using a number of well known circuits and methods. Next, at step 1405, error analysis and adaptation circuitry 1050

presets a number of variables: among them, coefficient $TX\alpha[1]$ is set to zero, a direction bit Dir is set to one, first and second phase variables $PH1$ and $PH2$ are each set to an initial value Φ_{init} that corresponds to the phase setting of step 1402, and a timing-margin variable TM is set to zero. The purposes of these variables will become clear in the following description.

[00116] Next, first IC device 1005 transmits a first data pattern to second IC device 1010 (step 1410). In this example, the first data pattern is a pseudo-random sequence such that signal $s(t)$ approximates live data. Receiver 1030 interprets the received signals $r(t)$ and conveys the received data pattern back to error analysis and adaptation circuitry 1050 via signal path 1035 (step 1415). Error analysis and adaptation circuitry 1050 then compares the transmitted and received data $D1$ and $D2$ to detect errors. Alternatively, errors can be detected at device 1010 and reported back to IC 1005.

[00117] Error analysis and adaptation circuitry 1050 then considers the error rate of data $D2$ (decision 1420). If the error probability P_{err} is not more than e.g. 0.02, then error analysis and adaptation circuitry 1050 retards the phase of transmit clock $TClk$ (step 1425). With reference to Figure 13A, retarding the transmit clock has the same effect as advancing receive clock $RClk$; namely, the sample instant moves to the left with respect to each signal eye. Other embodiments advance receive clock $RClk$ in step 1425, or can adjust both the transmit and receive clocks. Once adjusted, the new clock phase is recorded in step 1430 as phase $PH1$ and the process returns to step 1410. Steps 1410, 1415, 1425, and 1430 are repeated until the sample instant of receive clock $RClk$ is so far advanced relative to the signal eye that the error rate goes above the threshold value of 0.02, a condition that is illustrated in Figure 13B. Value $PH1$ then represents one edge of the signal eye that represents signal $r(t)$ in Figures 13A-C. Error analysis and adaptation circuitry 1050 stores phase offset $PH1$, advances the phase of $TClk$ by the value $PH1$ to

re-center the sample instant (step 1435), and begins transmitting a second data pattern (step 1440).

[00118] The loop formed by decision 1450 and steps 1440, 1445, 1455, and 1460 functions just as the preceding loop that involved decision 1420 to find the opposite edge of the signal eyes. That is, adaptation circuitry 1050 advances transmit clock TClk until the error rate P_{err} again surpasses 0.02. This phase offset PH2 corresponds to the right-most edge of the signal eye, as shown in Figure 13C.

[00119] Having recorded the left and right extremes of the signal eye, adaptation circuitry 1050 calculates a new timing margin TM_n as the difference between phase offsets PH2 and PH1 (step 1465). Per decision 1470, if the new timing margin is greater than the previously stored timing margin TM , that timing margin TM is updated with the new value TM_n (step 1475) and coefficient $TX\alpha[1]$ is either incremented or decremented, depending upon the polarity of direction variable Dir (step 1480). The process then returns to step 1410 so that adaptation circuitry 1050 can see whether the new transmit coefficient improves or reduces the timing margin. In decision 1470, if the new timing margin is no greater than the old, then step 1483 returns variable $TX\alpha[1]$ to its previous best value by subtracting direction variable Dir from the current $TX\alpha[1]$. Then, direction variable Dir is negated (step 1485) and the process moves to step 1480. The negation of variable Dir causes adaptation circuitry 1050 to move coefficient $TX\alpha[1]$ in the opposite direction before returning to step 1410 to try another transmit-equalization setting.

[00120] If left to operate over a sufficient time period, error analysis and adaptation circuitry 1050 will eventually settle upon and dither about a setting for coefficient $TX\alpha[1]$ that maximizes or nearly maximizes the timing margin TM for receives signal $r(t)$. Error analysis and adaptation circuitry 1050 can then employ the optimized coefficient for data transmission.

[00121] Figure 15 depicts a communication system 1500 in accordance with another embodiment. System 1500 includes a transmitter 1505 that transmits a differential data signal V_{in} (V_{in_p}/V_{in_n}) to a receiver 1510 via a differential channel 1515. A conventional transmitter may be employed as transmitter 1505, so a detailed treatment is omitted here for brevity. Transmitter 1505 optionally includes transmit pre-emphasis circuitry to dynamically adjust the data signal V_{in} to reduce signal distortion caused by the effects of channel 1515. Such transmit pre-emphasis circuitry may include, for example, a multi-tap transmit amplifier 1520 adapted to cause the voltage amplitudes of the data symbols of signal V_{in} to be selectively increased or decreased based on the data values of pre and/or post cursor data symbols.

[00122] Receiver 1510 includes an equalizer 1525 that equalizes data signal V_{in} to produce an equalized signal V_{eq} (V_{eq_p}/V_{eq_n}). Equalizer 1525 adjusts the magnitude (e.g., voltage and/or current) of at least some data symbols in data signal V_{in} . In one embodiment, equalizer 1525 receives signal V_{in} , via a differential input port, and amplifies signal V_{in} using a range of amplification factors, with higher frequencies components of V_{in} being treated to higher amplification factors. Such an equalizer may be used to, for example, compensate for the low-pass nature of channel 1515. In that case, the degree to which equalizer 1525 amplifies higher frequency signals relative to lower frequency signals can be adjusted via an equalizer input port Eq .

[00123] A pair of decision circuits, samplers 1530 and 1535, sample the received and equalized continuous-time signal V_{eq} in synchronization with respective receive clock signals $ClkA$ and $ClkB$ to produce sampled signals D_{inA} and D_{inB} . Clock signals $ClkA$ and $ClkB$ may be derived from a common receive clock $RClk$. Receive clock $RClk$ may, in turn, be derived from a number of sources, including from a PLL with a stable reference, such as a crystal clock part. A pair of phase adjusters 1540 and 1545 allows a

finite state machine 1550 to independently control the phases of clock signals ClkA and ClkB by application of appropriate control signals PHA and PHB.

[00124] State machine 1550 may work much as adaptation circuitry 1050 as described above in connection with flowchart 1400 of Figure 14 to optimize the equalization settings of equalizer 1525 to achieve the widest timing margin TM. That is, state machine 1550, in combination with other circuitry, can function as a margining circuit to measure the timing margin TM of signal Veq and adjust the equalization settings of receiver 1510 to maximize the timing margin. The inclusion of two independently controlled samplers 1530 and 1535 in this embodiment facilitates equalizer adaptation based upon live data.

[00125] In operation, sampler 1530 samples incoming symbols and provides the resulting data DinA to some core logic (not shown) and an error detector 1553, an XOR gate in this embodiment. Should data DinA and DinB fail to match, error detector 1553 asserts an error signal Err to an error counter 1555. Error counter counts the number of errors per some predetermined number of bit times and asserts a signal $Perr > Merr$ if the error probability exceeds a selected maximum error value (e.g., 0.02). State machine 1550 uses signal $Perr > Merr$ to identify the edges of signal eyes in signal Veq in the manner detailed above in connection with Figure 14. In finding those edges, state machine 1550 advances and retards clock ClkB with respect to clock ClkA by varying a phase-offset signal ΔPH to an adder 1560 such that control signal PHA differs from control signal PHB by a positive or negative offset ΔPH .

[00126] State machine 1550 advances and retards the phase of clock signal ClkB until error counter asserts signal $Perr > Merr$ to find the two extreme signal-eye edges and calculates the timing margin as the difference between the two. State machine 1550 then adjusts an equalization signal Eq to equalizer 1525 and again measures the timing margin.

If a change to the equalization signal improves the timing margin, state machine 1550 continues to attempt changes in the same direction. If the change worsens or fails to improve the timing margin, then state machine 1550 attempts to change the equalization setting in the opposite direction. Eventually, state machine 1550 settles on an optimal or near optimal equalization setting. The calibration sequence can be performed once or can be repeated periodically or continuously, as on live data, to accommodate changes in e.g. temperature or supply voltage.

[00127] State machine 1550 controls equalizer 1525 in this example, but can control additional or different receive equalizers in other embodiments. State machine 1550 might also issue transmit-equalizer control signals TXeq, via a suitable backchannel 1570, instead of or in addition to controlling receive-equalization settings. State machine 1550 may also control other aspects of the receive circuitry, such as the reference voltage (not shown) against which single-ended signals are compared. Of interest, the above-described method may provide optimal or near optimal equalization settings even if such a reference voltage is not ideally positioned at the widest point within a signal eye. In that case the measured timing margin may not represent the full width of an eye, but the resulting equalization settings would nevertheless provide for maximum eye width. Thus, “timing margin” as used herein may refer to a signal-eye width for a sample voltage at any of a range of voltages along the vertical dimension of a signal eye.

[00128] In still other embodiments the margining circuitry may be used to determine the optimal reference voltage against which to measure incoming signals. The timing margin can be optimized as detailed above for a range of reference voltages. Incoming signals can then be sampled using the reference voltage associated with the largest timing margin.

[00129] Figures 14 and 15 collectively illustrate a method for calibrating a communication system in which a transmitter on a first integrated circuit device transmits

to a receiver on a second integrated circuit device via a communication channel, the method comprising: converting, at the transmitter, a first bit sequence into a transmitted version of a continuous-time signal; transmitting the transmitted version of the continuous-time signal over the communication channel, wherein the communication channel degrades the transmitted version of the continuous-time signal to produce a received version of the continuous-time signal; equalizing at least one of the transmitted or received versions of the continuous-time signal by application of a filter coefficient; measuring a timing margin of the received version of the continuous-time signal; and changing the filter coefficient based upon the timing margin.

[00130] In various embodiments of the method illustrated in connection with Figures 14 and 15:

- the second integrated circuit device measures the timing margin of the received version of the continuous-time signal. In this embodiment, it may be that the first integrated circuit device equalizes the transmitted version of the continuous-time signal in response to the filter coefficient.
- the method may include sampling, at the receiver, the received version of the continuous-time signal to create a second bit sequence, in which case measuring the timing margin may comprise comparing the first and second bit sequences, and measuring the timing margin may comprise comparing the first and second bit sequences at the transmitter.
- the method may include sampling, at the receiver, a received version of the continuous-time signal to create a third bit sequence. In that case, measuring the timing margin may comprise comparing the second and third bit sequences, and measuring the timing margin may comprise sampling the received version of the continuous-time signal at a first sample instant for each bit of the first bit

sequence and sampling the received version of the continuous-time signal at a second sample instant for each bit of the first bit sequence, and wherein the first and second sample instants are offset from one another and are timed to sample the same symbol in the received version of the continuous-time signal.

[00131] Integrated circuits of the type illustrated in Figure 15 may include at least one pad to communicate a continuous-time signal; an equalizer coupled to the pad and including an equalizer control port; and a margining circuit to measure a timing margin of the continuous-time signal and to issue a timing-margin signal representative of the timing margin; wherein the equalizer equalizes the continuous-time signal in response to the timing-margin signal. Such integrated circuits can transmit the continuous-time signal on the pad, and may further comprise: a transmitter to convert a transmit bit stream into the continuous-time signal, wherein the margining circuit measures the timing margin using a process that includes comparing the transmit bit stream with a received bit stream derived from the continuous-time signal; and/or first and second decision circuits to sample the continuous-time signal at first and second clock phases. The margining circuit may adjust one of the first and second clock phases relative to the other in deriving the timing-margin signal.

Channel Characterization

[00132] Figure 16 depicts an integrated circuit (IC) 1600 upon which a receiver 1605 is instantiated in accordance with one embodiment. IC 1600 includes a pad 1610 that receives a continuous-time data input signal V_{in} from an external signal source (not shown) by way of a communication channel 1611. Pad 1610 conveys signal V_{in} to receiver 1605, which includes an equalizer 1615, a data sampler 1620, a level detector 1625, a data buffer 1630, system-response measurement circuitry 1635, and a tap-coefficient generator 1640. Equalizer 1615 equalizes the incoming signal V_{in} by applying

tap coefficients $RX\alpha[P:1]$ to provide an equalized input signal Ve_q . Data sampler 1620 periodically samples signal Ve_q on edges (rising, falling, or both) of a data clock $DClk$ to recover a bit sequence, data signal $Data_i$, from signal Ve_q . The bit expressed as data signal $Data_i$ propagates through a buffer 1630, which presents prior data samples $Data_{i-1}$ to $Data_{i-M}$ to response measurement circuitry 1635.

[00133] Level detector 1625 periodically or continuously measures the voltage level of signal Ve_q and presents the resulting data-level measurement $Dlev$ to response measurement circuitry 1635. Response measurement circuitry 1635 then employs data patterns from buffer 1630 and voltage levels from detector 1625 to calculate the single-bit response (SBR) of the combination of channel 1611 and equalizer 1615. The level detector can detect current or a combination of voltage and current in other embodiments.

[00134] Generally, an SBR is the waveform observed at a receiver after transmission of a signal-bit-wide logic-high pulse preceded and succeeded by null transmissions. For a transmitter that sends a sequence of data pulses, the linear time-invariant (LTI) system response at the receiver will be a superposition of scaled and time-shifted copies of the SBR. For example, if a transmitter sends 2-PAM binary data with logical values 1 and 0 represented by transmission levels of +1 and -1, then the response at the receiver is the superposition of time-shifted copies of the positive and negative SBR.

[00135] An SBR can provide measures of various forms of signal degradation, including those caused by attenuation, reflections, and dispersion. Such measures can be very helpful for diagnostics and for computing equalization settings. It is often desirable to measure the SBR of a channel without actually transmitting a single bit pulse preceded and succeeded by null transmissions. For example, a 2-PAM transceiver system may not be equipped to transmit an SBR test pattern because it can only transmit logic-high and

logic-low levels, but not a null level, or it might be preferable to measure the SBR during live data transmission, in which case an isolated single bit transmission might never occur. In these cases, the receiver can only observe the superposition of several SBRs corresponding to a specific received bit pattern at a given instant. For purposes of the present disclosure, such a superposition of SBRs can be used to characterize a communication channel and derive appropriate equalization coefficients by considering the specific data patterns that generate the observed superpositions.

[00136] In receiver 1605, response measurement circuitry 1635 associates specific bit patterns from data buffer 1630 with their corresponding data levels (Dlevs) from level detector 1625, formed by the corresponding superposed SBRs, and employs this information to derive the SBR at receiver signal V_{eq} . In this example, response measurement circuit 1635 stores patterns and associated data levels in respective registers 1645 and 1650, and distinguishes between pattern/level pairs by addressing registers 1645 and 1650 using a common counter 1655.

[00137] Response measurement circuit 1635 represents the SBR as a set of signals $SBR[M:0]$. As noted above, the SBR can be used for diagnostics; in this embodiment, however, tap-coefficient generator 1640 uses some or all of signals $SBR[M:0]$ to derive tap coefficients $RXa[P:1]$ for equalizer 1615. Embodiments that do not include an equalizer may omit tap-coefficient generator 1640. Furthermore, level detector 1625 can be fed from the input of equalizer 1615 (e.g., after pad 1610) to facilitate response measurements at that node instead of or in addition to the input of sampler 1620.

[00138] Figure 17A is a flowchart 1700 illustrating the operation of response measurement circuit 1635 in IC 1600 of Figure 16 in accordance with one embodiment. First, counter 1655 is set to zero to prepare for receipt of the first data pattern of interest (step 1705). In response, pattern register 1645 selects a first pattern $Pattern[0]$ and level register 1650 prepares to receive a data-level value at address zero (step 1710). Next, data

sampler 1620 periodically samples signal V_{eq} to produce a series of data samples on nodes $Data_i$ - $Data_{i-M}$. For each sample so received, response measurement circuit 1635 determines whether the selected pattern $Pattern[Cnt]$ from register 1645 matches the bit stream in buffer 1630 (decision 1720). Absent a match, response measurement circuit 1635 merely awaits the next data sample $Data_i$, and thus the next pattern (step 1715). If there is a match, however, register 1650 stores data level D_{lev} as level $Lev[0]$. The count is then incremented (step 1730).

[00139] Moving to decision 1735, if the count is less than or equal to some preordained target count, the process returns to step 1710 so that response measurement circuitry 1635 can relate another pattern to a corresponding voltage level. This loop will continue until the number of obtained measurements surpasses the target count, at which time a sufficient number of pattern/level pairs are available to calculate the combined SBR for channel 1611 and equalizer 1615. Then, in step 1740, response measurement circuitry 1635 uses the collected levels and associated patterns to calculate signals $SBR[M:0]$. Finally, tap-coefficient generator 1640 derives tap coefficients $RX\alpha[P:1]$ from signals $SBR[M:0]$ to establish appropriate equalization settings for equalizer 1615 (step 1745). The derivation of the tap coefficients may be done in an iterative manner, where after each response measurement the coefficients are adjusted from their previous settings based on the response measurement.

[00140] Figure 17B depicts a matrix equation 1750 that may be used to calculate SBR signals $SBR[3:0]$ in an embodiment of Figure 16 in which sampler 1620 and buffer 1630 provide four consecutive data samples $Data_i$ through $Data_{i-3}$ to response measurement circuitry 1635. The matrix equation 1750 can be solved if matrix D is square and of full rank. In the instant example, signal V_{in} is a 2-PAM signal in which logic ones and zeros are expressed as voltage levels that are equal and opposite with respect to a reference voltage, and adjacent bits need not be separated by a null

transmission. Sampled data Data_i - Data_{i-M} can therefore be expressed as patterns of +1 and -1 data bits, where +1 represents a logic one and -1 represents a logic zero (e.g., 1010b is expressed as +1,-1,+1,-1). Matrix D is populated with patterns expressed as positive and negative ones in this embodiment, as these values represent the transmission that resulted in the observed levels at node Veq . Other values expressing the same or other levels may be used in other embodiments.

[00141] Populating register 1650 with levels $\text{Lev}[0]$ through $\text{Lev}[3]$ for the corresponding patterns allows response measurement circuitry 1635 to solve for vector SBR, which represents the SBR for channel 1611 and equalizer 1615. This method does not depend on statistical properties of the received data sequence. Instead, the method only requires that the desired data patterns and associated signal levels can be observed. This is important because it allows the response measurement to be made with very little requirements on the nature of the transmitted data, allowing the method to be used during live data transmission in a wide variety of systems, specifically those that may have data with non-zero autocorrelation. However, if the overall link has a non-zero SBR at times outside the range of the SBR vector and the data pattern has significant autocorrelation, then the response measurement may be biased by the statistics of the received data. It may therefore be desirable to use an SBR vector that covers the full time range where any non-zero response may be expected. This key benefit and the possibility of biased results if the SBR vector does not span the overall SBR of the link and at the same time the data has non-zero autocorrelation are common to the various embodiments and methods described below.

[00142] Matrix equation 1750 is easily solved if the patterns are carefully chosen. Since some communication protocols preclude the use of certain data patterns, response measurement circuitry 1635 may be capable of solving more general matrices. Response measurement circuitry 1635 may support Gaussian Elimination, a well known method, to

solve more general matrix equations. Note that pattern register 1645 may support more than a minimum set of M patterns, so that if a certain pattern match is not found after a predetermined period of time, a different pattern match can be attempted. However, the final set of M patterns should result in a square and full rank D matrix. To remove the effects of noise on the data levels from the SBR calculation, it is possible to repeat this measurement and matrix computation several times, and average the results, so that random (uncorrelated) noise effects will tend to be filtered from the final result.

Alternatively, if noise is present in the measurements, it is possible to construct a matrix equation where D has more than M rows. Noise on Lev may cause such an equation to not have a single unique solution. However, common regression techniques such as MLSE can be used to derive an estimated solution of SBR that filters out some of the noise influence.

[00143] The SBR matrix SBR provides a measure of the SBR at node Ve_q in receiver 1605 at the data sample times, and therefore of the ISI observed at sampler 1620. The matrix SBR can therefore be used to update filter coefficients for equalizer 1615 using well-understood techniques. Some types of equalizers, such as decision-feedback equalizers (DFEs), may use coefficients that are directly derived from SBR values, in which case tap-coefficient generator 1640 can be simplified. In other embodiments tap coefficient generator 1640 can support whatever interpretation of the SBR is required to update appropriate equalizer coefficients.

[00144] Figure 18 depicts a receiver 1800 in accordance with an embodiment that operates in much the same manner as receiver 1605 of Figure 16. An equalizer 1805 equalizes an incoming signal V_{in} that arrives over a channel 1806. A data sampler 1810 periodically samples the resulting equalized signal Ve_q on edges of a data clock $DClk$ and conveys the resulting samples $Data_i$ to a data buffer 1815. Buffer 1815 stores the four most recent previous data samples $Data_{i-1}$ to $Data_{i-4}$ and presents the series to a response

measurement circuitry 1825. A level detector 1830 periodically measures the voltage level of signal V_{eq} and presents the resulting data-level measurement D_{lev} to response measurement circuitry 1825. Response measurement circuitry 1825 then employs data patterns from sampler 1810 and buffer 1815 and the voltage levels from detector 1830 to calculate the SBR at node V_{eq} , including the combined effects of equalizer 1805, channel 1806, and any other filtering or equalization present at the transmitter (not shown).

[00145] The SBR is represented as a set of signals $SBR[3:-1]$ in this example. Of these, signal $SBR[0]$ represents the strength of the main cursor (the contribution to voltage V_{eq} by the current data symbol); signals $SBR[3:1]$ represent post-cursor ISI imposed upon the voltage V_{eq} by the three immediately preceding data symbols; and $SBR[-1]$ represents pre-cursor ISI imposed upon the voltage V_{eq} by the immediately subsequent symbol. An equalizer 1805, a decision-feedback equalizer (DFE) in this example, compensates for post-cursor ISI using filter coefficients $RXa[3:1]$. A tap-coefficient generator 1835 derives or updates these filter coefficients based on signals $SBR[3:1]$. Signal $SBR[-1]$ may be used to tune another equalization component, e.g. an equalizing transmitter (not shown) that is the source of input signal V_{in} .

[00146] Level detector 1830 includes a sample-and-hold (S/H) circuit 1840 and an analog-to-digital converter (ADC) 1845. S/H circuit 1840 samples input signal V_{eq} on edges of data clock $DClk$ and holds the resulting sample voltage V_{sam} on an input of ADC 1845. ADC 1845 derives digital data level D_{lev} from sample voltage V_{sam} . Receiver 1800 includes a clock divider 1850 to divide data clock signal $DClk$, by five in this example, such that ADC 1845 produces one D_{lev} measurement for every fifth data sample. This reduction in clock frequency to ADC 1845 relaxes power versus performance tradeoffs or constraints in the ADC design.

[00147] Data sampler 1810 includes an S/H circuit 1855 and a data slicer 1860. S/H circuit 1855 works like S/H circuit 1840 and slicer 1860 samples the resulting held

data on edges of clock signal DCIk to produce data samples $Data_i$. The data samples are conveyed to data buffer 1815 and away from receiver 1800 to whatever other circuitry (not shown) that is the intended recipient of the received data. In a typical example, the other circuitry might include memory to store the received data.

[00148] Response measurement circuitry 1825 includes a pattern-matching circuit 1865, a state machine 1870, and a delay element 1874. State machine 1870 issues selected patterns $Pat[4:0]$ to pattern-matching circuit 1865 and receives in response a signal Ma that is asserted when sampled data $Data_i$ through $Data_{i-4}$ match pattern $Pat[4:0]$. Delay element 1874 delays state-machine clock $SMClk$ by two periods of data clock $DCIk$ as compared with clock signal $DCIk/5$. This delay aligns selected patterns with corresponding detected levels, as detailed below. Delay element 1874 can be adjustable in other embodiments to provide response measurement circuit 1825 the ability to associate sampled levels with different bit positions in sampled data patterns.

[00149] Equalizer 1805 is optional, and may be omitted. Other embodiments may include other types of equalizers instead of or in addition to a DFE; for example, equalizer 1825 may include one or more partial-response DFE (PrDFE) taps of the type described in published U.S. Patent App. No. 2005111585 to Stojanović et al. entitled “Partial Response Receiver.” A series of synchronous storage elements 1875-1877 respectively present first, second, and third post-tap, or post-cursor, data to respective coefficient multipliers 1880. Multipliers 1880 multiply the outputs of the storage elements by respective tap coefficients $RX\alpha[3,2,1]$, and DFE 1805 subtracts the sum of the outputs of multipliers 1880 from incoming signal V_{in} to produce equalized signal V_{eq} . Alternatively, equalizer 1805 could be implemented as a direct, continuous-time linear equalizer with tunable coefficients. In general, an equalizer can adjust the SBR at a particular node to achieve some desired characteristic, e.g. a low bit-error rate or, as in

the case of a PrDFE, can speculatively apply multiple ISI corrections and later select the appropriate correction to achieve the desired characteristic.

[00150] Figure 19A is a waveform diagram 1900 depicting the signal behavior at various nodes of receiver 1800 of Figure 18. The signals of interest are identified along the Y axis: the X axis is time measured in periods of data clock DCIk. Data symbols captured at time X on a rising edge of data clock DCIk at node Data_i are labeled DX. The same convention is used for other signals. Thus, data captured at node Data_i at time 0 is labeled D0. Diagram 1900 illustrates the receipt of a bit pattern D-9 through D4 as it is conveyed through data buffer 1815 and presented to pattern matching circuitry 1865.

[00151] Figure 19B is a flowchart 1902 depicting the operation of one embodiment of receiver 1800 of Figure 18. First, at step 1905, five test patterns Pattern[0]-Pattern[4] are selected for the calibration process. These test patterns, each expressed as bits Pat_{i+1} to Pat_{i-3}, form a matrix 1903. The patterns need not be selected at once, but selecting patterns in advance simplifies this illustration. Other embodiments can use any received pattern for the first data pattern and later accept subsequent received patterns such that a resulting collection of patterns provides enough information for state machine 1870 to derive the SBR. In the case of binary data, one way to ensure that a collection of patterns provides sufficient information is to accept unique patterns that all have the same value for a particular bit position.

[00152] At step 1910 a count Cnt is set to zero, after which state machine 1870 sets pattern bits Pat[4:0] to pattern Pattern[0], bit sequence 10000b in this example (step 1915). As noted previously, logic ones and zeros may be expressed as +1 and -1 values, respectively; pattern 1903 employs the latter notation. Data sampler 1810 then samples each data symbol expressed on input Veq on an edge of clock signal DCIk to produce the next data sample Data_i (step 1920). Pattern match circuitry 1865 compares each pattern that results from newly sampled data bits Data_i through Data_{i-4} against Pat[4:0].

Assuming the patterns do not match, the process returns to step 1920 at which time the next data bit $Data_i$ is sampled. (Step 1920 is not strictly part of the process: data bit $Data_i$ is periodically sampled irrespective of decision 1925 or the steps of flowchart 1902.)

Turning to waveform 1900 (Figure 19A), sequences of data bits $Data_i$ through $Data_{i-4}$ thus propagate through receiver 1800. A matching pattern that occurs without a corresponding rising edge of state-machine clock signal $SMClk$ is evident at time -4, and a non-matching pattern that occurs with a rising edge of state-machine clock $SMClk$ is evident at time -3. Neither of these patterns meets both of the requirements of decision 1925, so in each case the process awaits receipt of the next data sample.

[00153] Eventually, decision 1925 detects a matching pattern on the rising edge of clock signal $SMClk$, as is evident at time 2 in Figure 19B. The value of $Dlev$ at that time is the voltage level of signal Ve_q that level detector 1830 captured upon the last rising edge of clock signal $DClk/5$ at time zero. Also at time 2, signals $Data_{i-4}$ through $Data_i$ have values $D-3$ through $D1$ that respectively represent the data bits received from the third sample time before time zero through the first sample time after time zero. State machine 1870 captures this value of $Dlev$ as $Lev[Cnt-1]$, or $Lev[-1]$ in this example (step 1930). The saved value is denoted with index “-1” because this is the measured signal level for a logic zero that corresponds to the data pattern entered into the matrix equation of Figure 20 on the same row as $SBR[-1]$. Note that this offset between signals $DClk/5$ and $SMClk$ allows the pattern match to include the data bit $D1$ received just after the observed $Dlev$ value sampled at time zero. Therefore, the offset between signals $DClk/5$ and $SMClk$ allows response measurement circuit 1825 to measure pre-cursor ISI contributions.

[00154] Figure 20 is a matrix equation 2000 that might be the product of flowchart 1902 of Figure 19B for the particular set of data patterns expressed in matrix 1903. A dotted rectangle around the values for the top row of matrices $Dlev$ and D show the

information obtained thus far in the flow of Figure 19B, and as depicted at time 2 in Figure 19A. That is, state machine 1870 has associated a data-level value $Lev[-1]$ with the first data pattern $Pattern[0]$.

[00155] Returning to flowchart 1902 of Figure 19B, once the first pattern association is made, the process moves to step 1935 in which the count is incremented. Per decision 1940, if the count is less than five there are more patterns to consider so the flow returns to step 1910. Each of the data levels corresponding to the remaining patterns is thus measured and stored. When the count reaches five, vector D_{lev} and matrix D of equation 2000 (Figure 20) is fully populated, at which time state machine 1870 has sufficient information to solve for vector SBR . In some embodiments, this process may be repeated several times, and the results averaged, so that a better estimate of SBR can be made if there is any unrelated noise in the system.

[00156] Figure 21 depicts a receiver 2100 in accordance with another embodiment. An equalizer 2105 equalizes an incoming signal V_{in} by applying tap coefficients $RX\alpha[3,2,1]$. A data sampler 2110 periodically samples the resulting equalized signal V_{eq} on edges of a data clock $DClk$ and conveys the resulting samples $Data_i$ to a data buffer 2115. Buffer 2115 stores the three previous data samples $Data_{i-1}$ to $Data_{i-3}$ and presents the series to a response measurement circuit 2125. A level detector 2130 periodically measures the voltage level of signal V_{eq} and presents the resulting data-level measurement D_{lev} to response measurement circuit 2125. Response measurement circuit 2125 then employs data patterns from buffer 2115 and voltage levels from detector 2130 to calculate the SBR at node V_{eq} for receiver 2100. A tap-coefficient generator 2131 is included in this embodiment to derive or update tap coefficients $RX\alpha[3:1]$ for DFE 2105 from the SBR from circuit 2125.

[00157] Data sampler 2110 includes a comparator 2133 and a data slicer 2135. Comparator 2133 compares equalized signal V_{eq} with a reference voltage V_r and

provides the result to slicer 2135. Slicer 2135 samples the output from comparator 2133 on edges of clock signal DClk to produce data samples $Data_i$, which indicate whether voltage V_{eq} is above or below reference voltage V_r at sample time i .

[00158] Level detector 2130 includes an error sampler 2140, which in turn includes a comparator 2145 and an error slicer 2150. Comparator 2145 compares signal V_{eq} with an analog data-level signal $D_{lev\#}$ and provides the result to slicer 2150. Slicer 2150 samples the resulting error signals on edges of clock signal DClk to produce error samples Err_i . The error samples Err_i are conveyed to an XNOR gate 2155, which serves as an error detector.

[00159] XNOR gate 2155 compares the corresponding data and error samples and presents its output to a multiplier 2160. The output of XNOR gate 2155 represents a logic one for true and a logic negative one for false. The data and error samples represent the signs of the sampled values, so XNOR gate 2155 has the effect of multiplying the signs of the data and error values and presenting the resulting product to multiplier 2160. Multiplier 2160 multiplies the product from XNOR gate 2155 by a selected step size μ , which may be tailored to provide appropriate feedback granularity.

[00160] An accumulator 2165 accumulates a data-level value D_{lev} by adding the product from multiplier 2160 to the accumulator contents each time a match signal Ma is asserted by pattern match circuit 2175. The digital value D_{lev} is conveyed to a digital-to-analog converter 2170 and to response measurement circuitry 2125. DAC 2170 converts value D_{lev} into analog reference voltage $D_{lev\#}$ for comparator 2145.

[00161] Response measurement circuitry 2125 includes a pattern-match circuit 2175 and a state machine 2180. State machine 2180 issues patterns $Pat[3:0]$ to pattern-match circuit 2175 and receives in response a match signal Ma that pattern-match circuit 2175 asserts when D_i through D_{i-3} match pattern $Pat[3:0]$. Response measurement

circuitry correlates data level Dlev with specific data patterns to measure the combined SBR for the channel (not shown) and DFE 2105.

[00162] Figure 22 is a flowchart 2200 depicting the operation of receiver 2100 of Figure 21 in accordance with one embodiment. At step 2205 state machine 2180 issues a reset signal Rst to set a count register (not shown) to zero. State machine 2180 then selects a first pattern Pat[3:0] using any of a number of criteria. Here, for example, the first pattern is 1111b, but some communication protocols do not support a stream of four ones. In that case, another data pattern would be chosen. The patterns might be pre-selected to work with a given protocol, or state machine 1870 can identify useful patterns from the incoming data.

[00163] Next, a for-loop 2215A/B is executed for each data sample Data_i. If the sampled data pattern matches pattern Pat[3:0], then match circuitry 1865 asserts match signal Ma (decision 2220). Accumulator 2165 then subtracts from its contents the product from multiplier 2160 (step 2225) to adjust data levels Dlev and Dlev#. The counter is incremented (step 2230). If the count equals some pre-selected maximum, for-loop 2215A/B ends and a high value HRX_α[3] is set equal to level Dlev (step 2240). At this point level Dlev represents the average incoming signal level present at node Veq at the time when the last bit in a data pattern 1111b is received. The maximum count is set to a value that ensures level Dlev will have time to settle upon an adequate measure of the signal level for the selected pattern.

[00164] Next, the count is zeroed (step 2245) and the second pattern is selected to be 1110b, which differs from the first pattern by the value of data sample D_{i-3}. For-loop 2215A/B is then repeated again such that level Dlev settles upon a new level associated with the new data pattern. A low value LRX_α[3] is then set equal to that new level Dlev (step 2280). State machine 2180 then calculates an SBR component SBR[3] as one half of the difference between the high and low values HRX_α[3] and LRX_α[3] (step 2285).

The process of Figure 22 can be repeated, using appropriately selected data patterns, to derive other tap coefficients.

[00165] The process of Figure 22 works for non-random data patterns by masking uncorrected ISI associated with data samples not under consideration, so that they do not bias the observation, even if they have some correlation to the data samples under consideration. E.g., in flowchart 2200, ISI associated with the first and second post-cursor bit positions is masked by keeping Pat[2:1] to be the same value during both iterations of for-loop 2215A/B. This ensures that the ISI from these two bit positions is the same during both measurements, and the only difference between the two is the ISI contributed due to the differing value of the last bit position. The mask can be of any length, but will typically be limited to consideration and masking of symbols that may contribute considerable ISI. Furthermore, if the incoming data stream may have non-trivial autocorrelation (the data is not random), the mask should span all bit positions around the position under measurement that contribute considerable ISI, as mentioned previously. The ability to measure the SBR and calculate tap coefficients based upon arbitrary, possibly non-random, data is important, as receiver 2100 is capable of measuring the SBR and calculating tap coefficients while receiving live data.

[00166] Figure 23 depicts a portion of a receiver 2300 that is in some ways like receiver 2100 of Figure 21, like-numbered elements being the same or similar. The point at which data and error samples are compared is modified, however, to facilitate measures of pre-cursor ISI in accordance with another embodiment. Receiver 2300 includes response measurement circuitry 2305, which in turn includes a state machine 2310 and a pattern-matching circuit 2315.

[00167] Figure 24 is a flowchart 2400 depicting the operation of receiver 2300 of Figure 23 in accordance with one embodiment. Beginning with step 2410, state machine 2310 selects a first data pattern by asserting the pattern on lines Pat[5:0]. In this example,

the bits marked 'X' can be assigned to any value that is desired, but the one corresponding to data $Data_{i-1}$ is set to 1. The data pattern $Pat[5:0]$ is read left to right, from newest to oldest sample instant. The goal of the example of flowchart 2400 is to provide a measure of first pre-cursor ISI, which is the ISI contribution from an adjacent, subsequent bit. To achieve this result, the process measures the impact of the data bit at signal $Data_{i-1}$ on the average voltage level $Dlev\#$ that was present when the data bit at signal $Data_{i-2}$ was received.

[00168] Per decision 2415, if error sample Err_{i-2} matches corresponding data sample $Data_{i-2}$ about half the time for the selected pattern, then level $Dlev\#$ and digital value $Dlev$ may be considered to represent the average upper data level for the selected pattern. In that case, the upper level $HSBR[-1]$ is set to $Dlev$ (step 2435). As long as the error level is not 5020, however, the next sample is considered (step 2420) and the value $Dlev$ in accumulator 2165 is updated if the new pattern is a match (decision 2425 and step 2430). As in prior examples, a 5020 error rate may be assumed based upon a number of pattern matches and associated adjustments, though other methods might also be used.

[00169] Once the upper data level for the first pattern is found, the process moves to step 2440 in which SBR circuitry 2305 considers a second data pattern. This second pattern is identical to the first except for the bit associated with the ISI contributor of interest. In this case the ISI contributor of interest is associated with the first precursor value, and the corresponding bit is stored at $Data_{i-1}$. In the bit pattern $Pat[5:0]$, the bit of interest is the second one, which corresponds to data sample at $Data_{i-1}$, so the second pattern can be found by performing an exclusive OR of the first pattern and the pattern 010000b. If, for example, the first pattern is 111111b, then the second pattern is the exclusive OR of 111111b and 010000b, or 101111b.

[00170] Level $Dlev$ once again settles at the 5020 error rate for the new pattern using decisions 2415 and 2425 and steps 2420 and 2430. This new level $Dlev$ represents

the average upper boundary of incoming signal V_{eq} for the second pattern, and is stored as lower level $LSBR[-1]$ (step 2445). The difference between values $HSBR[-1]$ and $LSBR[-1]$ is due to the difference between the data patterns of steps 2410 and 2440, and the difference between the data patterns is limited to the bit of interest, data $Data_{i-1}$. The ISI contributed by the bit preceding the error, $SBR[-1]$, can thus be calculated as half of the difference between the high and low levels $HSBR[-1]$ and $LSBR[-1]$ (step 2450).

[00171] Figure 24 illustrates how one pre-cursor ISI value can be calculated using receiver 2300. The process can be repeated for other pre- and post-cursor ISI values by considering different data patterns. In addition, different data patterns can be used to refine the measure of $ISI[-1]$, or the process can be modified to fill in a matrix in a manner similar to what is detailed above. In some embodiments, the patterns are not pre-selected, but are chosen from patterns initially observed in the incoming data sequence. The resulting ISI values collectively describe a channel SBR for receiver 2300, and may be used for diagnostics or to provide filter tap coefficients to transmit or receiver equalizers.

[00172] Figure 26 depicts an error sampler 2600 and a phase mixer 2605 for use in yet another embodiment. Error sampler 2600 includes a comparator 2615, a slicer 2620, and a second phase mixer 2625. These components can be used in e.g. receiver 2100 of Figure 2100 to allow response measurements that take into account intersymbol interference measurements at times other than the data sample times.

[00173] Phase mixer 2605 derives data clock $DClk$ by mixing four clock phases $P[3:0]$ as directed by a control signal (not shown). Such phase mixers are commonly used in clock and data recovery circuits, which may be included in some embodiments, so a detailed discussion of phase mixer 2605 is omitted for brevity. Phase mixer 2625 is similarly controlled, but allows an error clock $EClk$ to be adjusted relative to data clock $DClk$ using a phase-adjust signal P_{adj} . The error samples Err_i may thus be taken at times

between edges of data clock DCIk to measure ISI effects that occur between data sample times.

[00174] A single SBR cannot be superposed to describe data pattern waveforms in all systems. Examples include systems with non-complementary rising and falling edges, such as some single-ended signaling systems. In the foregoing embodiments, a single-ended signal swings between $-DC/2$ to $+DC/2$. However, other embodiments can employ signals that vary from e.g., 0 to $+DC$. Furthermore, DC represents the DC swing in response to a stream of 0's followed by a stream of 1's. Rather than decomposing data pattern waveforms into the sum of scaled and shifted copies of a single SBR, we can decompose these waveforms into the sum of shifted copies of rising and falling edge responses. Both rising and falling edge responses may be DC shifted such that they each start from 0 for mathematical convenience. The methods described above can be extended to derive rising and falling-edge responses.

[00175] Figure 26A depicts a matrix equation 2600 that may be used to calculate step responses, both rising and falling edge responses RE[3:0] and FE[3:0], in an embodiment of Figure 16 in which sampler 1620 and buffer 1630 provide five consecutive data samples $Data_i$ through $Data_{i+4}$ to response measurement circuitry 1635. In this case, the response measurement circuitry is used to measure edge responses. The matrices **RD** and **FD** are derived from the data patterns as follows.

$$\begin{aligned} \mathbf{RD}(j,i) &= \begin{cases} 1 & \text{if } Data_i < Data_{i+1} \text{ in pattern } j, \\ 0 & \text{otherwise} \end{cases} \\ \mathbf{FD}(j,i) &= \begin{cases} 1 & \text{if } Data_i > Data_{i+1} \text{ in pattern } j, \\ 0 & \text{otherwise} \end{cases} \end{aligned}$$

The left matrix **Lev** is derived from the sample levels as follows.

$$\mathbf{Lev}(j) = \begin{cases} \text{sample}(j) - DC/2 & \text{if pattern } j \text{ starts with 1,} \\ \text{sample}(j) + DC/2 & \text{otherwise} \end{cases}$$

where $\text{sample}(j)$ is the actual sample level seen by sampler 1620 and DC is the DC swing in response to a stream of 0's followed by a stream of 1's. Both rising and falling edge

responses are assumed to be DC shifted to start from 0 for the matrix equation 2600 to hold.

[00176] Figure 26B rewrites the matrix equation 2600 of Figure 26A in a more compact form, equation 2605. Similar to matrix equation 1750, equation 2600 can be solved if matrix **ED** is square and of full rank.

[00177] The DC swing can be measured beforehand with a constant input stream of 0s followed by a stream of 1s. In the case of live data, this requirement can be eliminated by constructing two sets of equation 2605, for patterns starting with 1 and 0 respectively. The sum of the left matrices **Lev** is no longer dependent on DC. The edge responses can be obtained by solving the composite equation which is the sum of the two equations constructed.

[00178] Embodiments of the methods detailed above can comprise: receiving an input signal via the channel; sampling the input signal to obtain data samples; measuring the input signal to obtain a first signal level; correlating the first signal level with a first pattern of data samples from the data samples; measuring the input signal to obtain a second signal level; correlating the second signal level with a second pattern of data samples from the data samples; and calculating the response of the channel at the receiver from the first and second signal levels and the first and second data patterns. In these methods, calculating the response may comprise populating a matrix with the first and second data patterns. The first and second signal levels form a second matrix that is a product of the first-mentioned matrix and the response of the channel. Calculating the response may comprise solving for at least one of a single-bit response or a step response using the first and second matrices, and the calculated response may comprise a plurality of measures of intersymbol interference, possibly a measure of pre-cursor intersymbol interference. Measuring the input signal to obtain a first signal level may comprise repeatedly sampling the input signal relative to a range of reference levels. Correlating

the first signal level with the first pattern of data samples may comprise filtering the data samples for the first pattern of data samples. The method may additionally include monitoring an error rate over the range of reference levels.

[00179] Embodiments of the above-described receivers may comprise an input node to receive an input signal via a channel; a data sampler coupled to the input node, the data sampler for sampling the input signal to obtain data samples; means for measuring the input signal to obtain a first signal level and correlating the first signal level with a first pattern of data samples from the data samples; means for measuring the input signal to obtain a second signal level and correlating the second signal level with a second pattern of data samples from the data samples; and means for calculating the system response of the channel from the first and second signal levels and the first and second data patterns. Such receivers might additionally comprise an equalizer coupled to the input node, wherein the means for calculating the system response of the channel produces tap coefficients for the equalizer.

[00180] In the foregoing description and in the accompanying drawings, specific terminology and drawing symbols are set forth to provide a thorough understanding of the present disclosure. In some instances, the terminology and symbols may imply specific details that are not required to practice embodiments of the invention. For example, the interconnection between circuit elements or circuit blocks may be shown or described as multi-conductor or single conductor signal lines. Each of the multi-conductor signal lines may alternatively be single-conductor signal lines, and each of the single-conductor signal lines may alternatively be multi-conductor signal lines. Signals and signaling paths shown or described may be single-ended or differential, and embodiments of the invention may be adapted for use with binary or multilevel-pulse-amplitude-modulated (multi-PAM) signals.

[00181] An output of a process for designing an integrated circuit, or a portion of an integrated circuit, comprising one or more of the circuits described herein may be a computer-readable medium such as, for example, a magnetic tape or an optical or magnetic disk. The computer-readable medium may be encoded with data structures or other information describing circuitry that may be physically instantiated as an integrated circuit or portion of an integrated circuit. Although various formats may be used for such encoding, these data structures are commonly written in Caltech Intermediate Format (CIF), Calma GDS II Stream Format (GDSII), or Electronic Design Interchange Format (EDIF). Those of skill in the art of integrated circuit design can develop such data structures from schematic diagrams of the type detailed above and the corresponding descriptions and encode the data structures on computer readable medium. Those of skill in the art of integrated circuit fabrication can use such encoded data to fabricate integrated circuits comprising one or more of the circuits described herein.

Pseudo-Claims to Embodiments Implemented Using Computer-Readable Storage Media

[00182] In one embodiment implemented as a computer-readable storage medium having stored thereon a data structure defining a receiver to receive a continuous-time signal expressed as a sequence of data symbols, the data structure comprises: first data representing an equalizer to equalize the continuous-time signal and having a coefficient input node; and second data representing a margining circuit coupled to the coefficient input node of the equalizer, the margining circuit to measure a timing margin of the continuous-time signal and to issue to the coefficient input node a timing-margin signal representative of the timing margin; wherein the equalizer equalizes the continuous-time signal in response to the timing-margin signal.

[00183] In another embodiment implemented as a computer-readable storage medium having stored thereon a data structure defining a transmitter adapted to transmit a continuous-time signal expressed as a sequence of data symbols, the data structure

comprises: first data representing a transmitter having a transmitter input port to receive a first bit sequence, an output driver to convert the first bit sequence into the continuous-time signal, and an offset-adjustment port to adjust a voltage offset of the continuous-time signal; second data representing an input port to receive an erroneous second bit sequence derived from the continuous-time signal and including errors, wherein the errors are differences between the first and second bit sequences; and third data representing error analysis and adaptation circuitry coupled to the input port and the offset-adjustment port, the error analysis and adaptation circuitry to derive a control signal from the errors and apply the control signal to at least one of an equalizer and a DC offset control port to adjust the continuous-time signal.

[00184] In yet another embodiment implemented as a computer-readable storage medium having stored thereon a data structure defining a receiver adapted to receive an input signal expressed as a sequence of data symbols, the data structure comprises: first data representing an input node to receive the input signal via a channel; second data representing a level detector, coupled to the input node, to measure levels of the signal; third data representing a data sampler having a sampler input terminal, coupled to the input node, and a sampler output terminal, the sampler to produce data samples on the sampler output terminal; fourth data representing a data buffer coupled to the sampler output terminal to store the data samples; and fifth data representing a system-response measurement circuit coupled to the data buffer to receive the data samples and to the level detector to receive the levels, the system-response measurement circuit to calculate the system response of the channel using the data samples and the levels of the signal.

[00185] The present invention is not limited to the embodiments detailed above. For example,

1. Receivers in accordance with some embodiments can incorporate a variable-gain amplifier to provide DC-offset or automatic-gain control.

Such amplifiers can be configurable or can be controlled e.g. using Dlev to establish and maintain desired DC signal levels.

2. Transmitters in accordance with some embodiments can likewise incorporate a pre-distorted offset to provide compensation for any receiver DC-offset or automatic-gain control. Such transmitter pre-distortion can be configurable or can be controlled e.g. using Dlev mapped and scaled as appropriate for the transmitter.
3. Transmitters and receivers could use test or training patterns in lieu of live data to calibrate transmit and receive coefficients.
4. Other types of equalizers, such as passive or active continuous time analog filters or transversal filters, could be used instead of or in addition to the above-described equalizers.
5. It may be the case that other circumstances drive the desire to put equalization on one device. Cost, complexity, experience, and desire to use standard devices on one end could each be reasons to asymmetrically distribute the equalization burden.
6. Other types of equalizers, such as passive or active continuous time analog filters or transversal filters, could be used instead of or in addition to the above-described equalizers.
7. Coding schemes may be developed to minimize the effects of ISI at particular instants relative to a symbol of interest.
8. More efficient sampling instants may be selected for ISI minimization.
9. Response measurement circuits in accordance with some embodiments rely upon different basis data patterns. For example, a multi-bit response, such as a di-bit response, can be used in lieu of a step response or an SBR.

Moreover, some components are shown directly connected to one another while others are shown connected via intermediate components. In each instance the method of interconnection, or “coupling,” establishes some desired electrical communication between two or more circuit nodes, or terminals. Such coupling may often be accomplished using a number of circuit configurations, as will be understood by those of skill in the art. Still other embodiments will be obvious to those of ordinary skill in the art. Therefore, the spirit and scope of the appended claims should not be limited to the foregoing description. Only those claims specifically reciting “means for” or “step for” should be construed in the manner required under the sixth paragraph of 35 U.S.C. §112.

CLAIMS

What is claimed is:

1. A communication system comprising:
 - a. a communication channel;
 - b. a transmitter coupled to the communication channel, the transmitter to transmit a transmitted version of a continuous-time signal over the communication channel;
 - c. a receiver coupled to the transmitter via the communication channel, the receiver including a decision circuit to sample a received version of the continuous-time signal; and
 - d. a margining circuit to measure a timing margin of the received version of the continuous-time signal and to issue a timing-margin signal representative of the timing margin;
 - e. wherein at least one of the transmitter or the receiver includes an equalizer coupled to the margining circuit, the equalizer to equalize the received version of the continuous-time signal in response to the timing-margin signal.
2. The communication system of claim 1, wherein the transmitter and the receiver are instantiated on respective first and second integrated-circuit devices.
3. The communication system of claim 2, wherein the margining circuit and the equalizer are instantiated on the first integrated-circuit device.
4. The communication system of claim 1, further comprising a second equalizer coupled to the margining circuit, wherein the first-mentioned equalizer is to adjust the transmitted version of the continuous-time signal and the second equalizer is to

adjust the received version of the continuous-time signal.

5. The communication system of claim 1, wherein the margining circuit comprises a state machine.
6. The communication system of claim 1, wherein at least one of the transmitter or the receiver comprises an error detector.
7. The communication system of claim 6, wherein the transmitter derives the transmitted version of the continuous-time signal from a first data series and the decision circuit samples the received version of the continuous-time signal to obtain a second data series, and wherein the error detector compares the first and second data series.
8. The communication system of claim 7, wherein the transmitter includes the error detector.
9. The communication system of claim 6, wherein the transmitter derives the transmitted version of the continuous-time signal from a first data series and the decision circuit samples the received version of the continuous-time signal to obtain a second data series and a third data series, and wherein the error detector compares the second and third data series.
10. A communication system comprising:
 - a transmitter instantiated on a first integrated circuit device and having:
 - a transmitter input port to receive a first bit sequence;
 - a transmitter output port; and
 - an output driver coupled between the transmitter input port and the transmitter output port, the output driver to convert the first bit sequence into a

first continuous-time signal on the transmitter output port;

a first communication channel coupled to the transmitter output port, the first communication channel to convey the first continuous-time signal as a second continuous-time signal degraded by intersymbol interference;

a receiver instantiated on a second integrated circuit device and coupled to the first communication channel, the first receiver to convert the second continuous-time signal into a second bit sequence;

a second communication channel coupled to the receiver to convey the second bit sequence to the first integrated circuit device; and

error analysis circuitry instantiated on the first integrated circuit device and coupled to the second communication channel to receive the second bit sequence, the error analysis circuitry to derive, from the second bit sequence, a measure of the intersymbol interference.

11. The communication system of claim 10, wherein the error analysis circuitry derives a transmit control signal from the second bit sequence.
12. The communication system of claim 11, the transmitter further comprising signal-offset circuitry coupled to the first communication channel and the error analysis circuitry, the signal-offset circuitry to apply a DC voltage offset to the first continuous-time signal responsive to the transmit control signal.
13. The communication system of claim 11, the transmitter further comprising a transmit equalizer coupled to the first communication channel and the error analysis circuitry, the transmit equalizer to equalize the first continuous-time signal responsive to the transmit control signal.
14. The communication system of claim 10, wherein the error analysis circuitry derives a receive control signal from the second bit sequence, the receiver further comprising signal-offset circuitry coupled to the first communication channel.

15. The communication system of claim 10, wherein the output driver includes a voltage-margin control port coupled to the error analysis circuitry, the voltage-margin control port to control a voltage margin of the continuous-time signal responsive to a voltage-margin control signal.
16. The communication system of claim 15, wherein the error analysis circuitry derives the voltage-margin control signal from the second bit sequence.
17. The communication system of claim 16, wherein the voltage-margin control signal adjusts a voltage swing of the continuous-time signal.
18. The communication system of claim 16, wherein the voltage-margin control signal adjusts a voltage offset of the first continuous-time signal relative to a reference voltage.
19. The communication system of claim 10, further comprising a timing-margin control port coupled to the error analysis and adaptation circuitry, the timing-margin control port to control a timing margin of the first continuous-time signal responsive to a timing-margin control signal.
20. The communication system of claim 19, wherein the timing-margin control port adjusts the phase of the first continuous-time signal.
21. The communication system of claim 10, further comprising a memory, wherein the memory stores the second bit sequence.
22. The communication system of claim 21, wherein the second communication channel is coupled to the receiver via the memory.

23. The communication system of claim 10, wherein the first and second communication channels are separate unidirectional channels.
24. The communication system of claim 10, wherein the first and second communication channels are implemented over at least one common conductor.
25. The communication system of claim 10, wherein the receiver comprises a receive equalizer, and wherein the error analysis circuitry instantiated on the first integrated circuit device adjusts the receive equalizer based upon the measure of the intersymbol interference.
26. A method for calibrating a communication system in which a transmitter on a first integrated circuit device transmits to a receiver on a second integrated circuit device via a communication channel, the method comprising:
- converting, at the transmitter, a first bit sequence into a first continuous-time signal;
 - transmitting the first continuous-time signal over the communication channel, wherein the communication channel degrades the first continuous-time signal to produce a second continuous-time signal;
 - converting, at the receiver, the second continuous-time signal into a second bit sequence;
 - controlling the transmitter to alter the first continuous-time signal and reduce an error margin of the second continuous-time signal to induce errors in the second bit sequence; and
 - analyzing the second bit sequence to derive a measure of intersymbol interference for the communication channel.

27. The method of claim 26, wherein analyzing the second bit sequence takes place on the first integrated circuit device.
28. The method of claim 27, wherein reducing the error margin comprises altering at least one of an offset voltage, a swing voltage, and a phase of the first continuous-time signal.
29. The method of claim 26, further comprising applying a DC signal offset to at least one of the first and second continuous-time signals responsive to the measure of intersymbol interference.
30. The method of claim 26, further comprising equalizing the first continuous-time signal and adjusting the equalization of the first continuous-time signal responsive to the measure of intersymbol interference.
31. The method of claim 30, further comprising increasing the error margin of the second continuous-time signal after deriving the measure of intersymbol interference.
32. The method of claim 26, wherein reducing the error margin comprises adjusting an offset of the first continuous-time signal.
33. The method of claim 32, wherein the offset is a voltage offset that varies with patterns expressed in the first bit sequence.
34. The method of claim 32, wherein the offset is a timing offset of the first continuous-time signal with respect to a timing reference.

35. The method of claim 26, further comprising transmitting multiple instances of a first data pattern in the first bit sequence and, for each instance, storing a corresponding second pattern of the second bit sequence on the second integrated circuit device.
37. The method of claim 35, wherein analyzing the second bit sequence comprises averaging a plurality of the second patterns.
38. The method of claim 26, wherein reducing the error margin comprises observing, on the first integrated circuit device, the second bit sequence over a range of margin settings.
39. A receiver comprising:
- an input node coupled to a channel to receive an input signal;
 - a level detector, coupled to the input node, to measure levels of the input signal;
 - a data sampler having a sampler input terminal, coupled to the input node, and a sampler output terminal, the sampler to produce data samples of the input signal on the sampler output terminal;
 - a data buffer coupled to the sampler output terminal to store the data samples as sample patterns; and
 - a system-response measurement circuit coupled to the data buffer to receive the sample patterns and to the level detector to receive the levels, the system-response measurement circuit to calculate the system response of the channel using the patterns and the levels of the input signal.
40. The receiver of claim 39, wherein the system response includes a single-bit response

of the channel.

41. The receiver of claim 39, wherein the system response includes a step response of the channel.
42. The receiver of claim 39, further comprising an equalizer coupled to the system-response measurement circuit and the input node, the equalizer to equalize a data signal to produce the input signal.
43. The receiver of claim 42, wherein the equalizer includes a plurality of filter taps, and wherein the filter taps receive tap coefficients from the system-response measurement circuit.
44. The receiver of claim 42, further comprising a tap-coefficient generator disposed between the measurement circuit and the equalizer.
45. The receiver of claim 39, wherein the level detector includes an analog-to-digital converter.
46. The receiver of claim 39, wherein the measurement circuit includes a pattern matching circuit coupled to the data buffer.
47. The receiver of claim 39, wherein the measurement circuit performs matrix computations to calculate the system response of the channel.
48. The receiver of claim 47, wherein the matrix computations relate ones of the measures of the levels of the input signal with corresponding ones of the patterns of the data samples.

49. The receiver of claim 48, wherein the patterns are linearly independent.
50. The receiver of claim 39, wherein the level detector includes an error sampler coupled to the input node to receive the input signal.
51. The receiver of claim 50, wherein the level detector includes an error detector having a first error-detector input coupled to an output of the error sampler and a second error-detector input coupled to an output of the data sampler to receive the data samples.
52. The receiver of claim 51, wherein the second error-detector input is coupled to the output of the data sampler via at least one sequential storage element.
53. The receiver of claim 39, wherein the measurement circuit is a means for deriving the single-bit response of the channel at the receiver from the data samples and the levels.
54. The receiver of claim 39, wherein the measurement circuit is a means for deriving at least one of a single-bit response or a step response from the data samples and the levels.

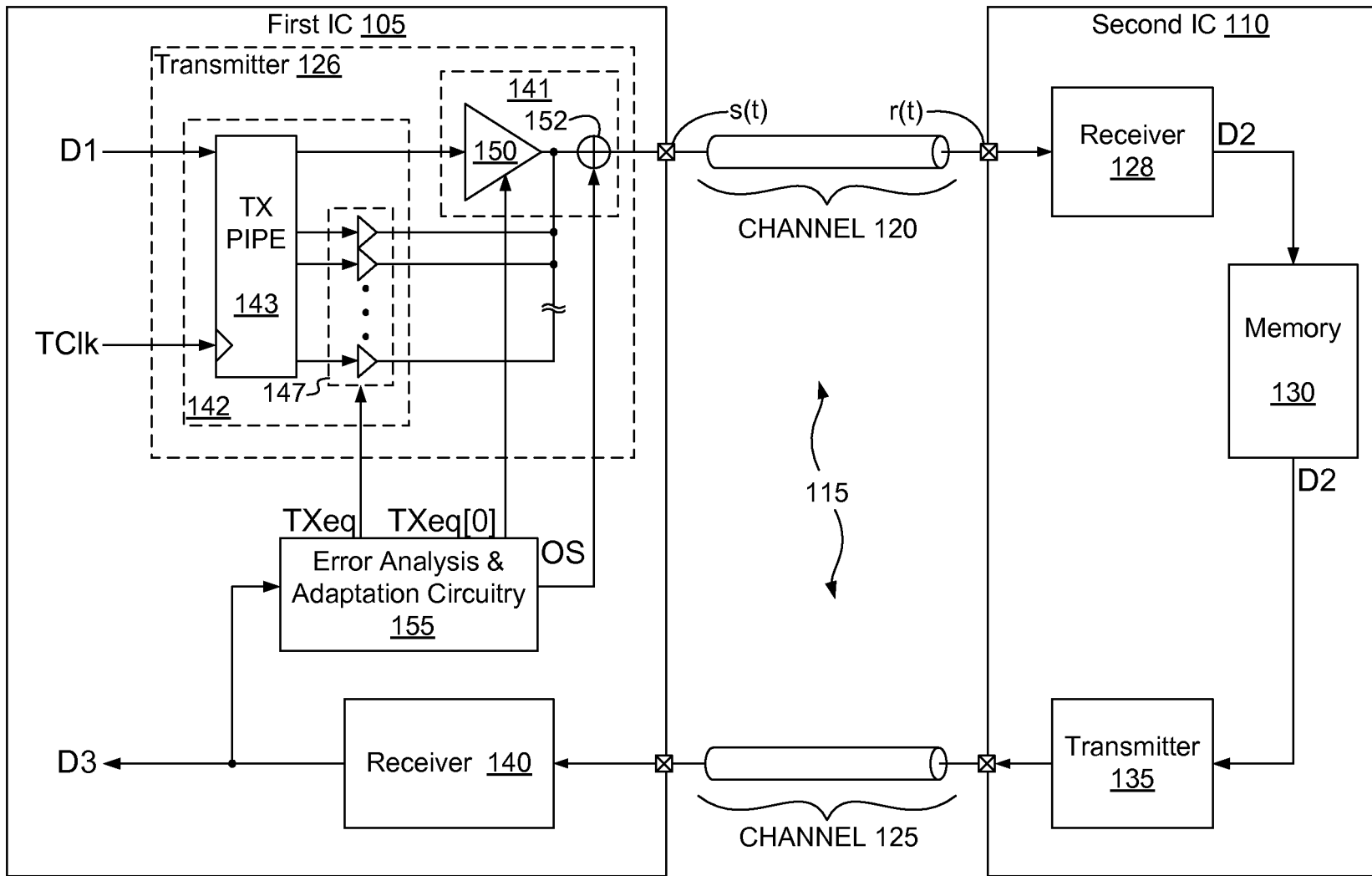


FIG. 1

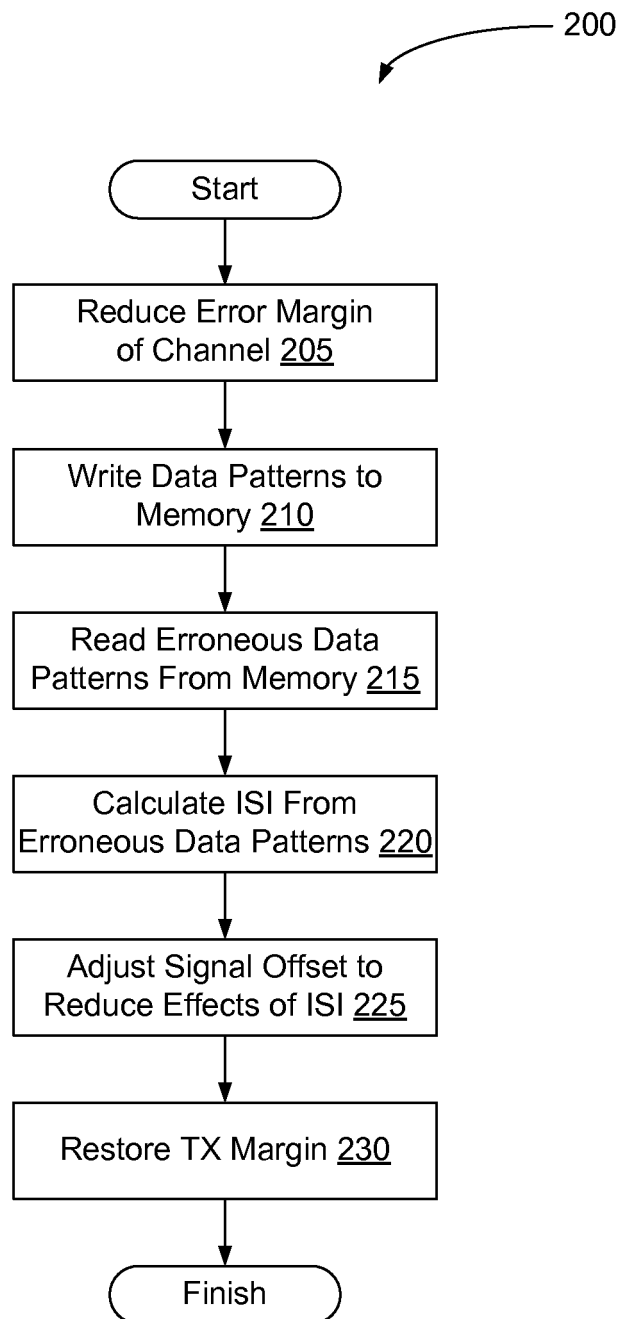


FIG. 2

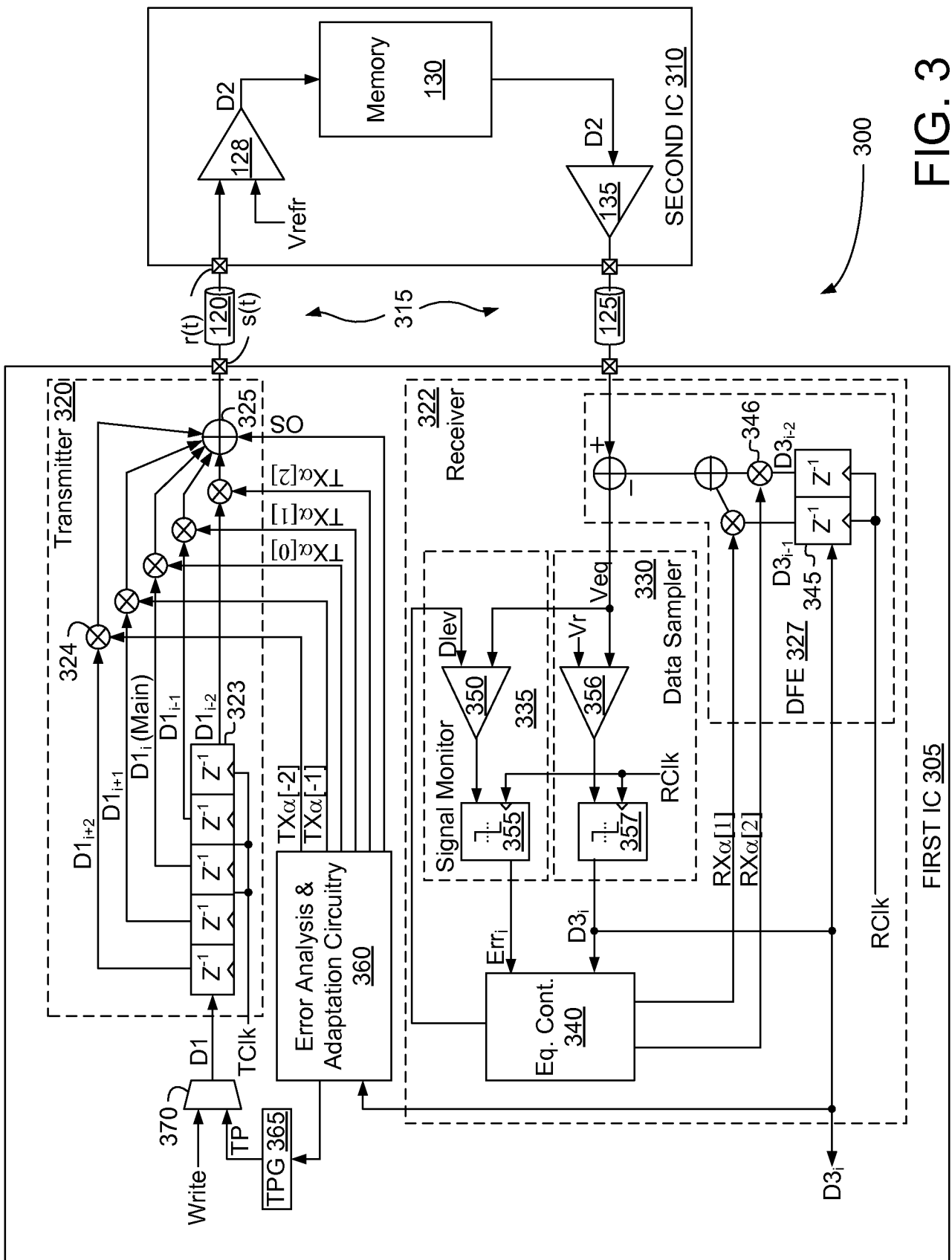


Fig. 3

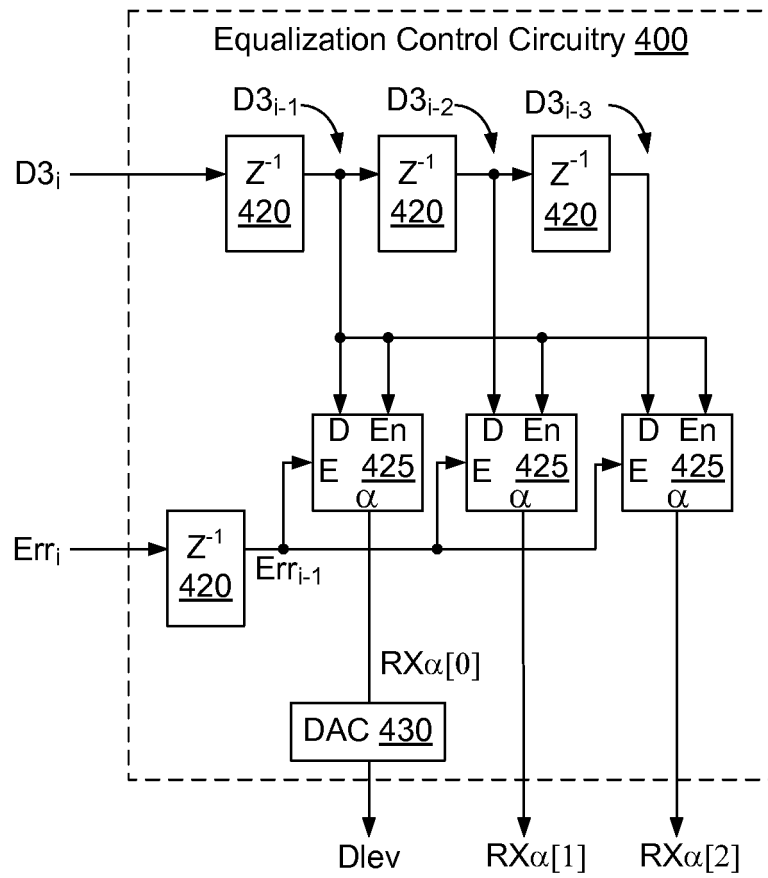


FIG. 4A

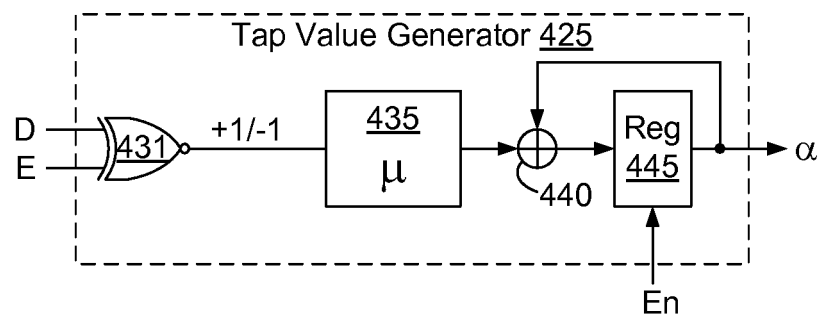


FIG. 4B

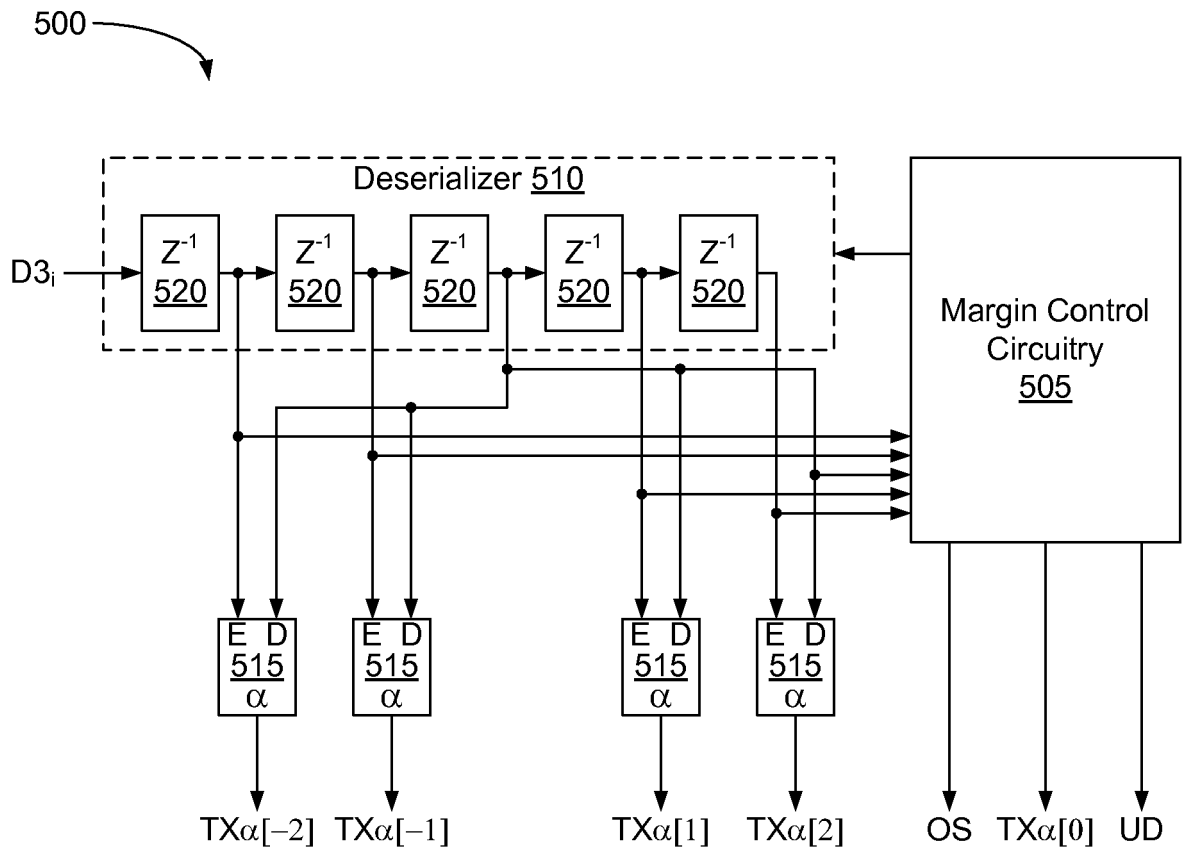


FIG. 5A

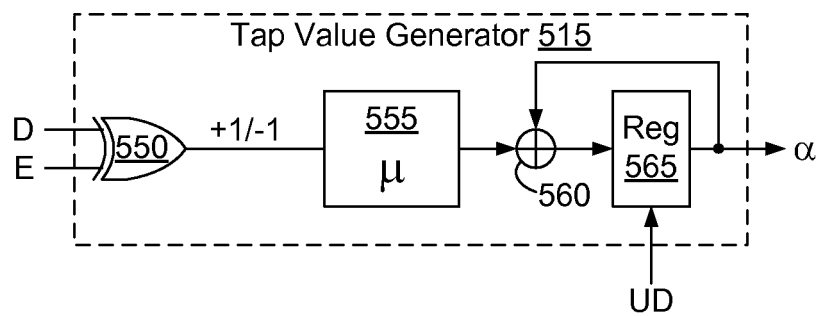


FIG. 5B

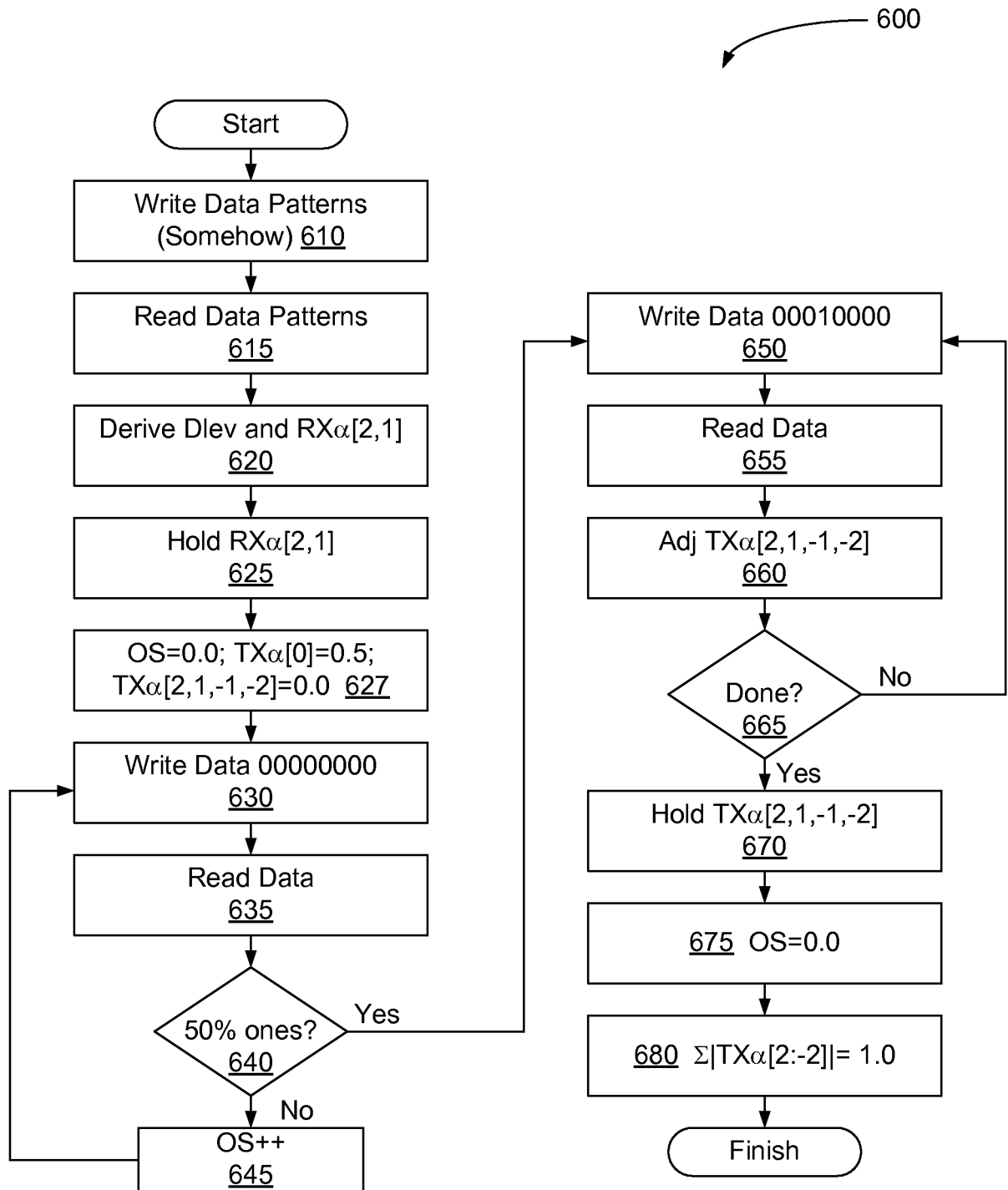


FIG. 6

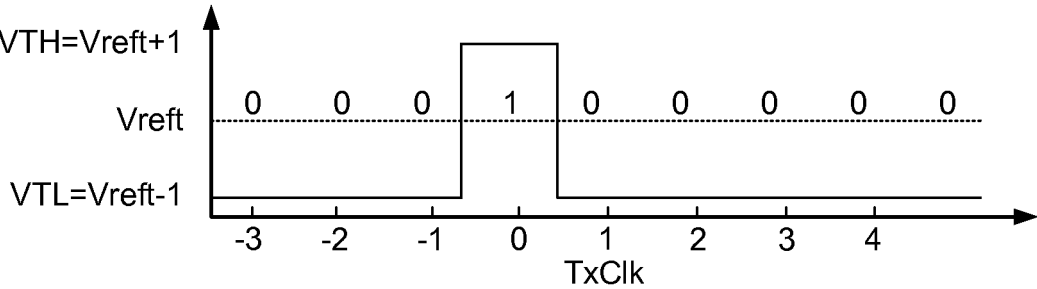


FIG. 7A

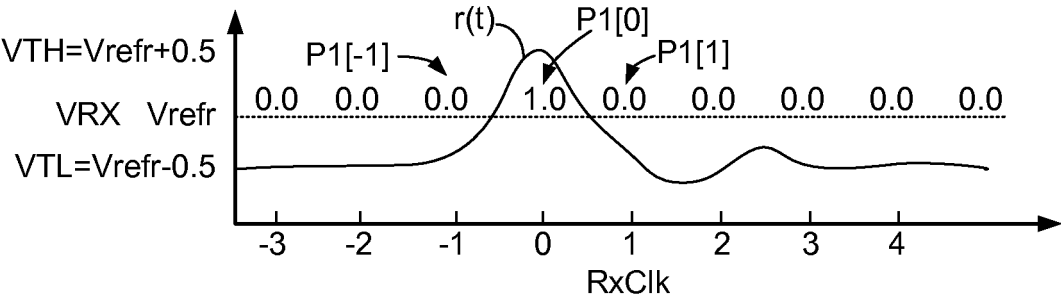


FIG. 7B

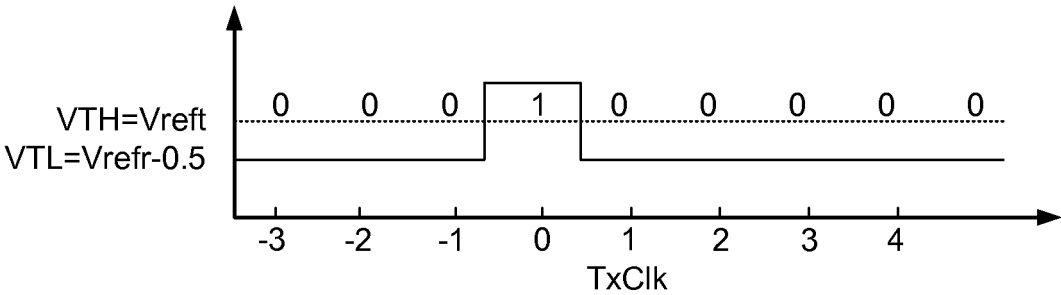


FIG. 7C

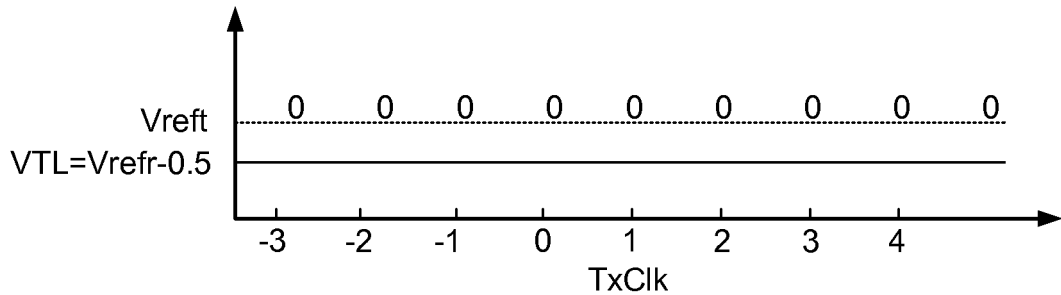


FIG. 7D

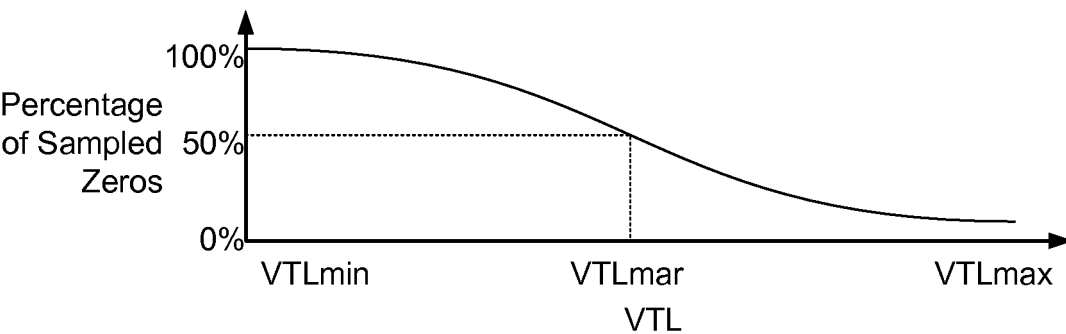


FIG. 7E

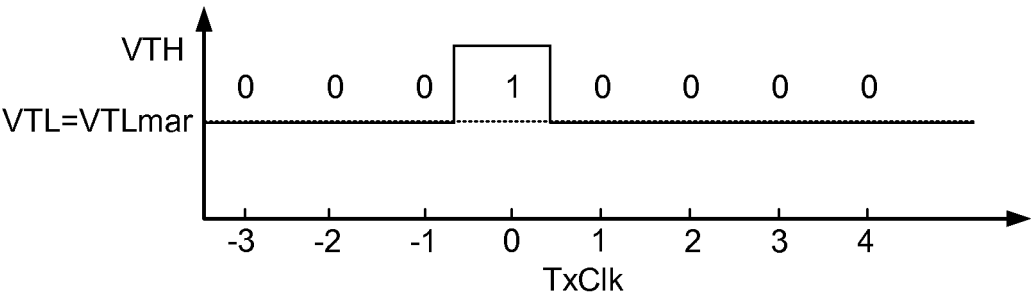


FIG. 7F

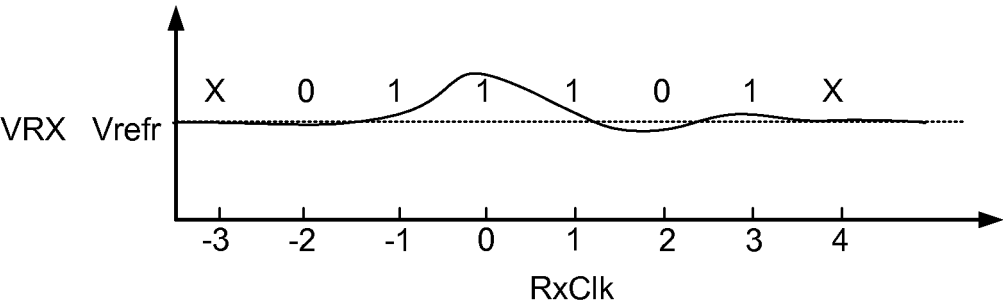


FIG. 7G

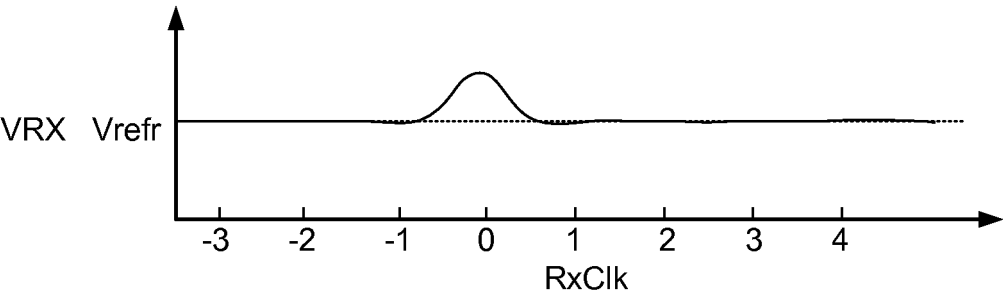


FIG. 7H

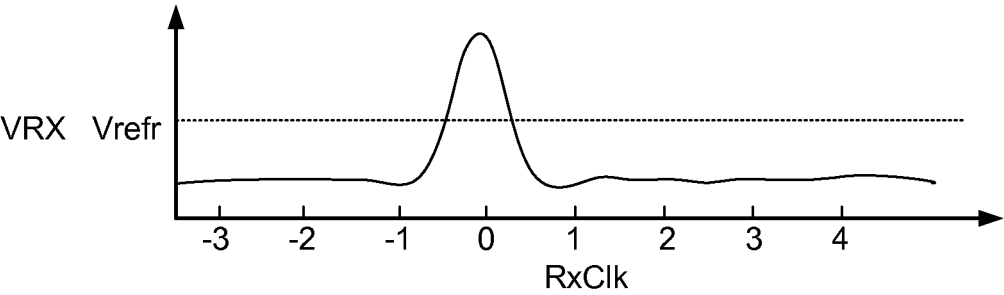


FIG. 7I

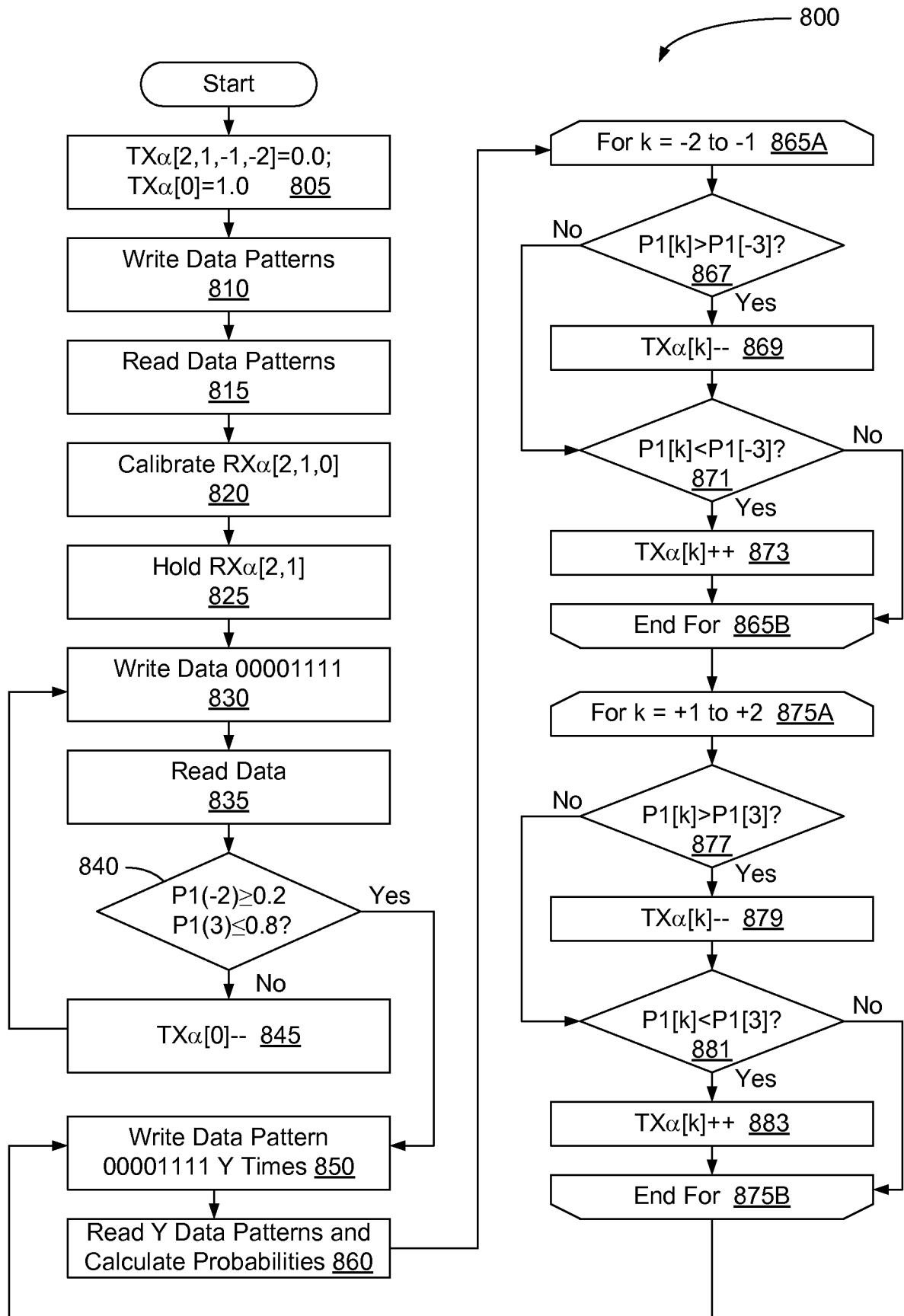


FIG. 8

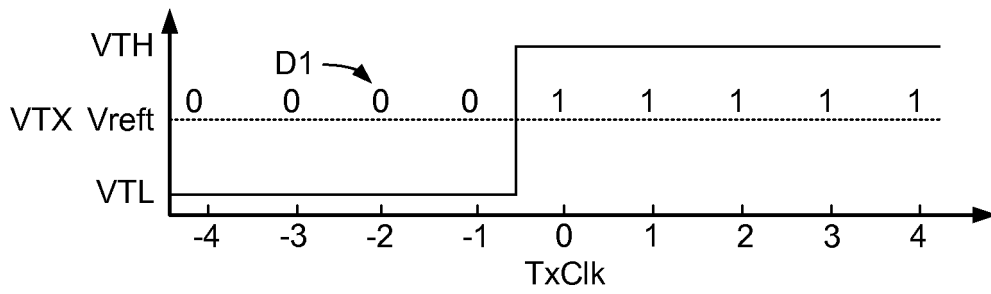


FIG. 9A

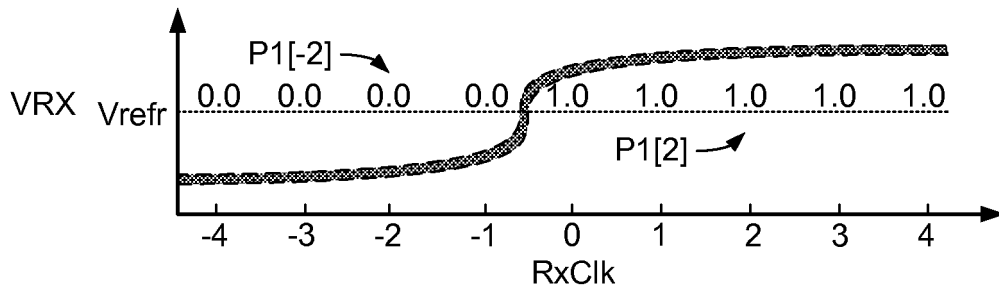


FIG. 9B

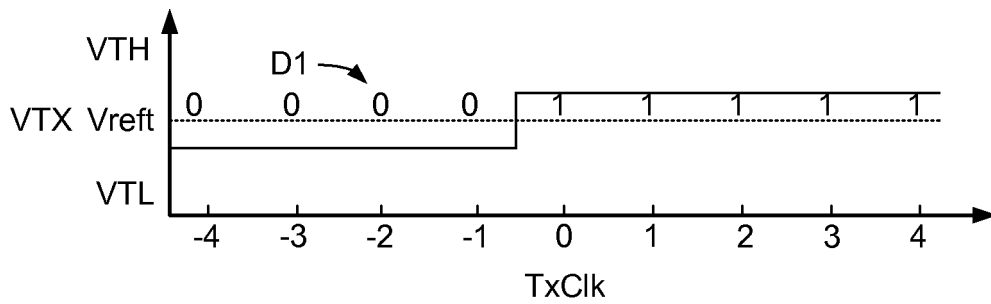


FIG. 9C

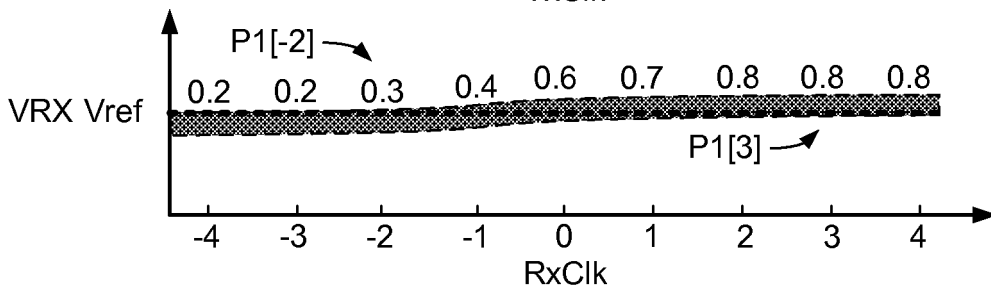


FIG. 9D

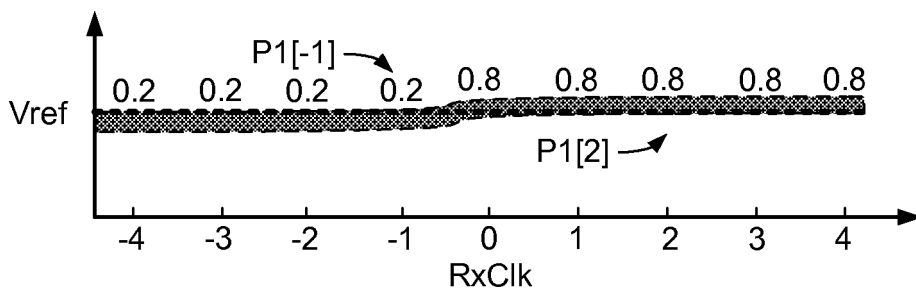


FIG. 9E

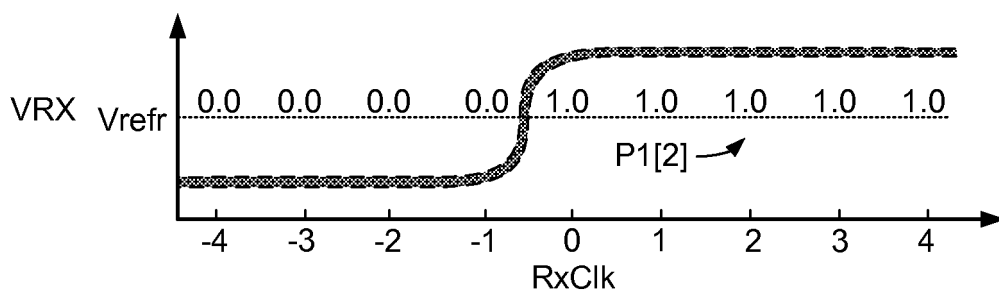


FIG. 9F

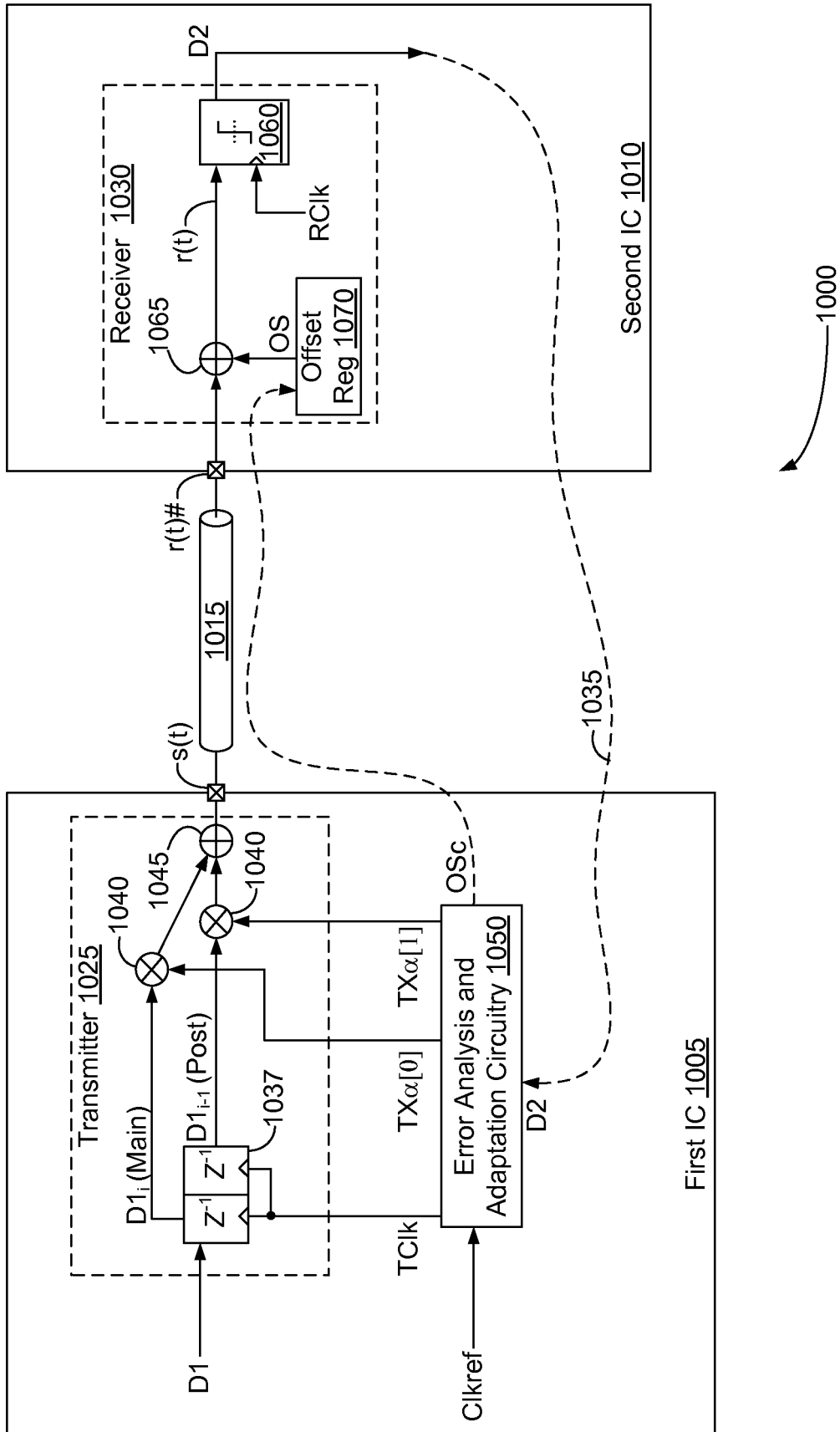


FIG. 10

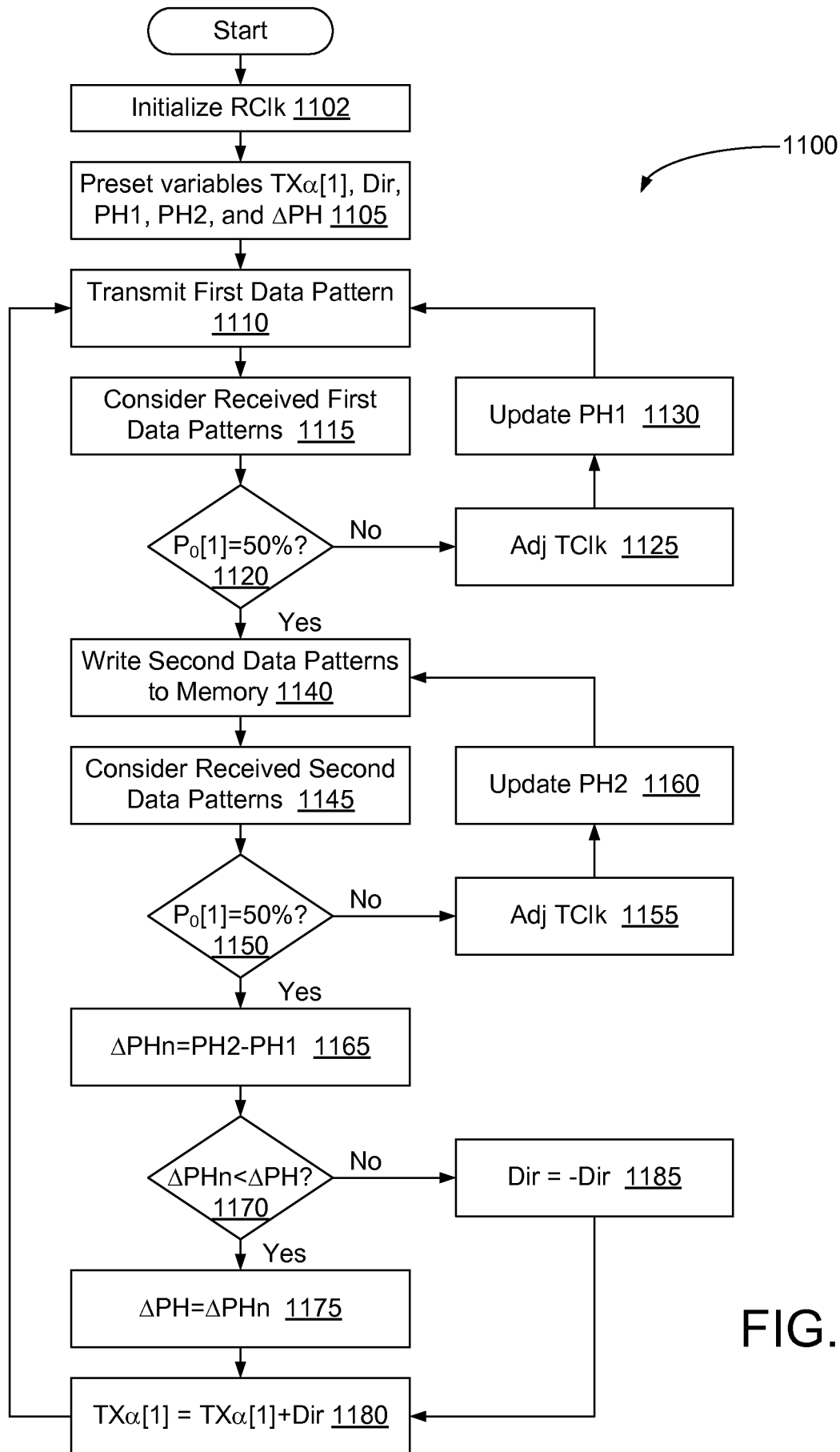


FIG. 11

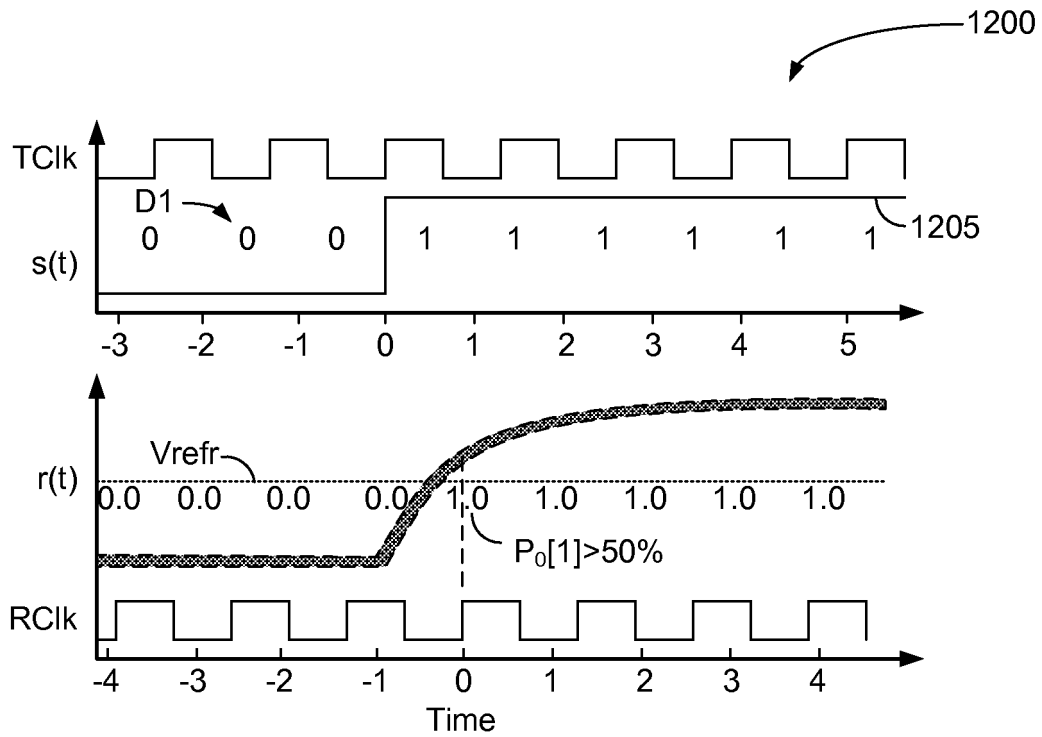


FIG. 12A

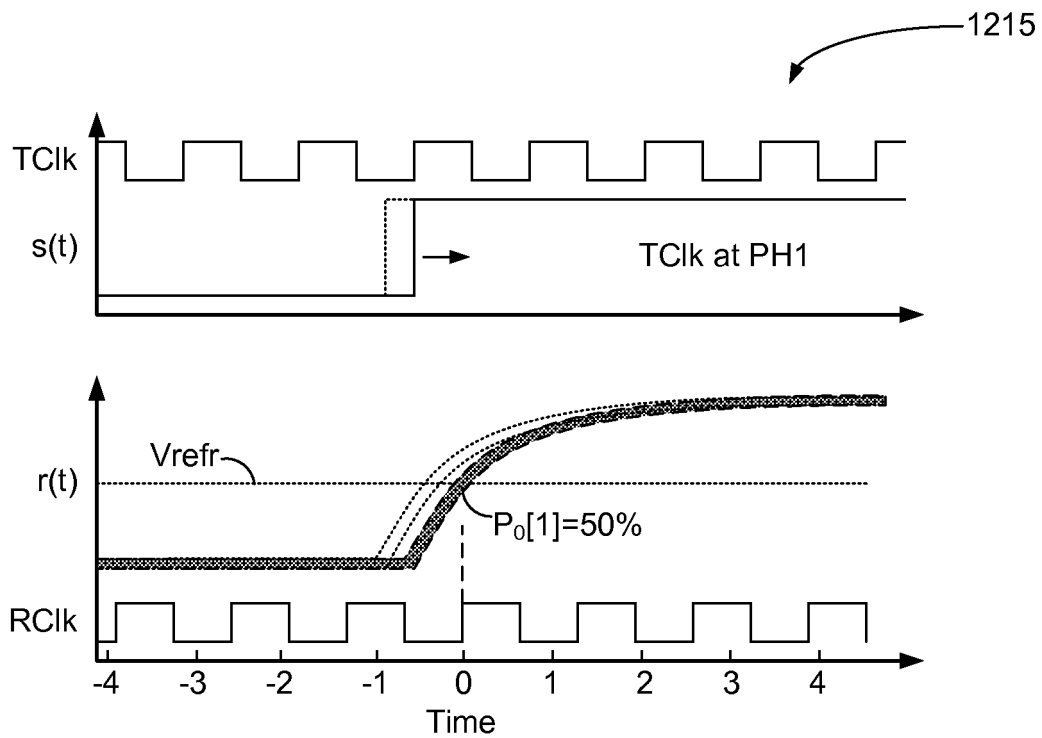


FIG. 12B

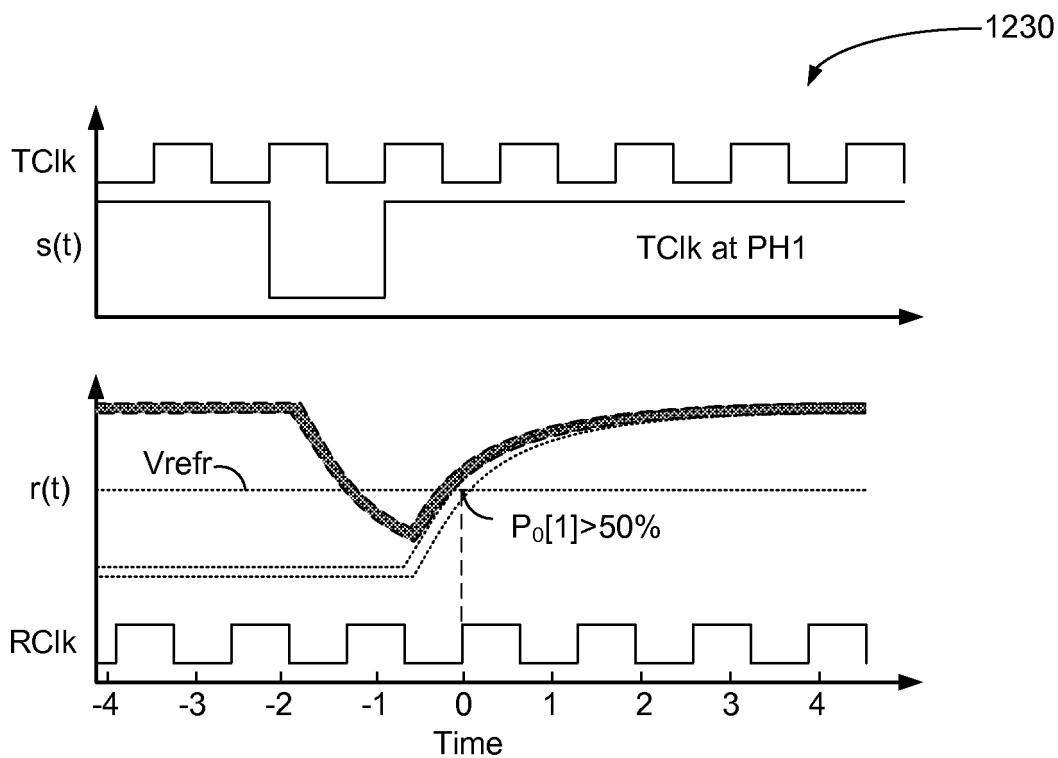


FIG. 12C

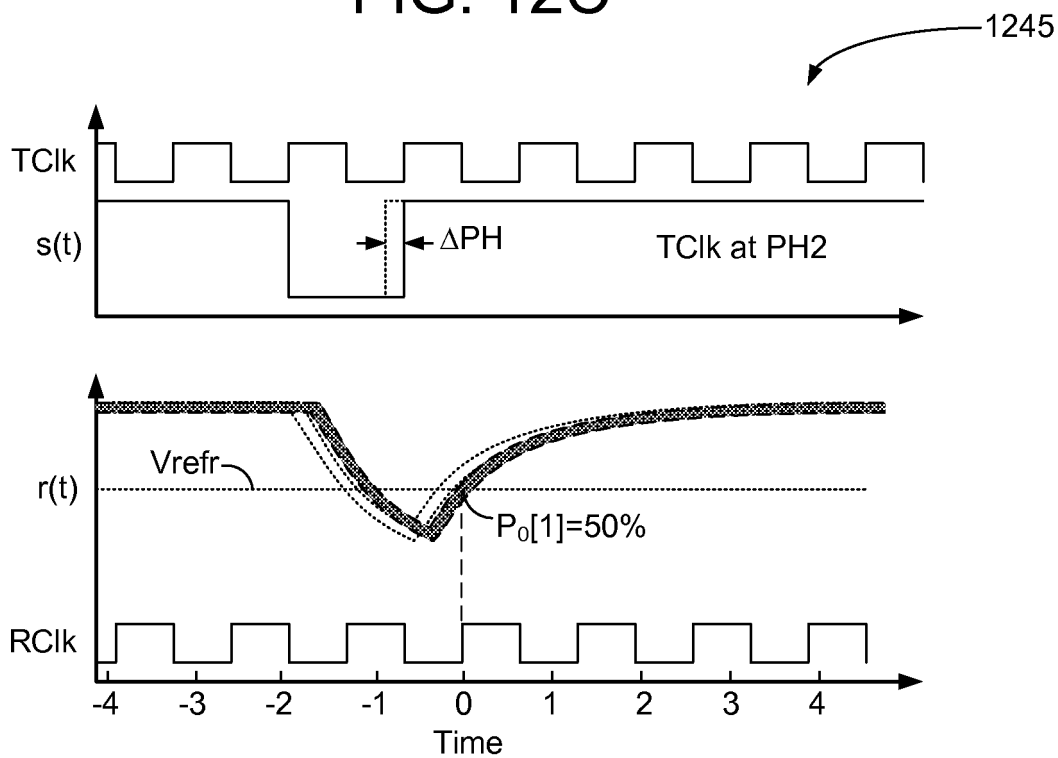


FIG. 12D

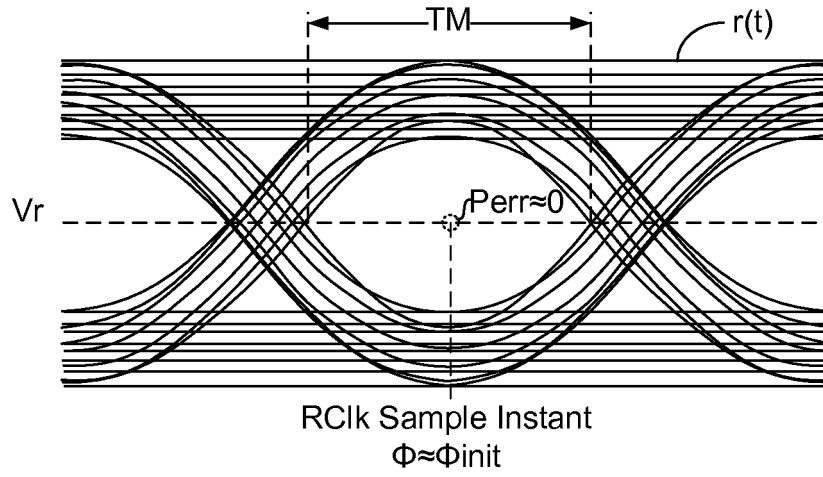


FIG. 13A

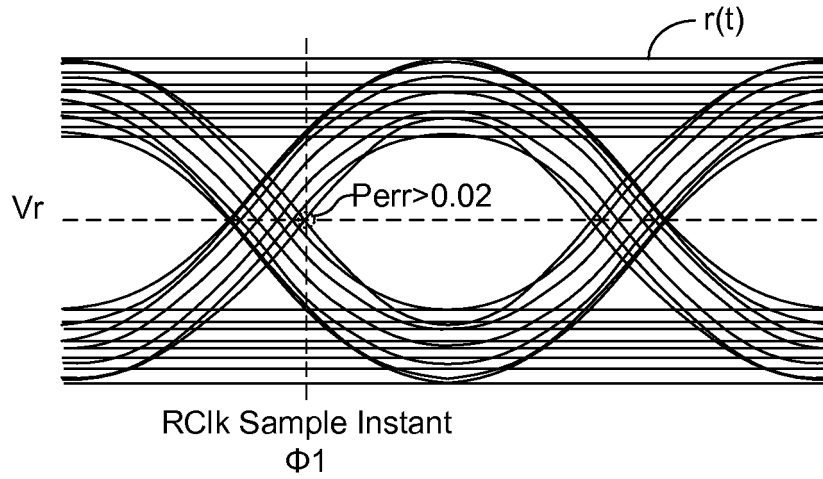


FIG. 13B

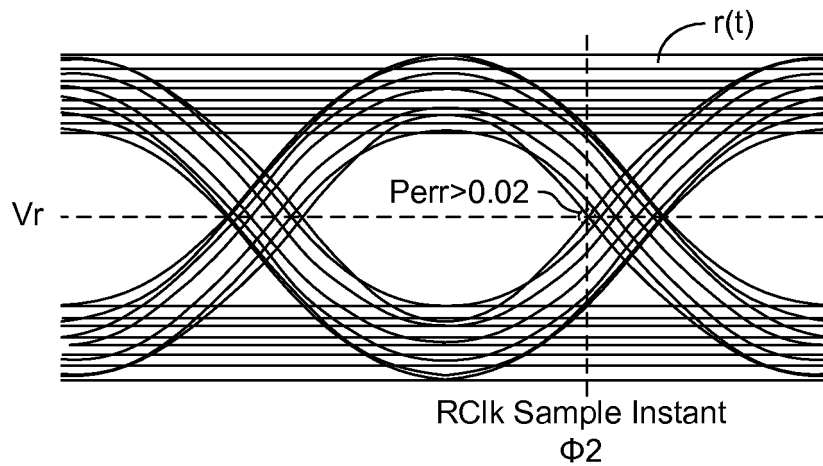


FIG. 13C

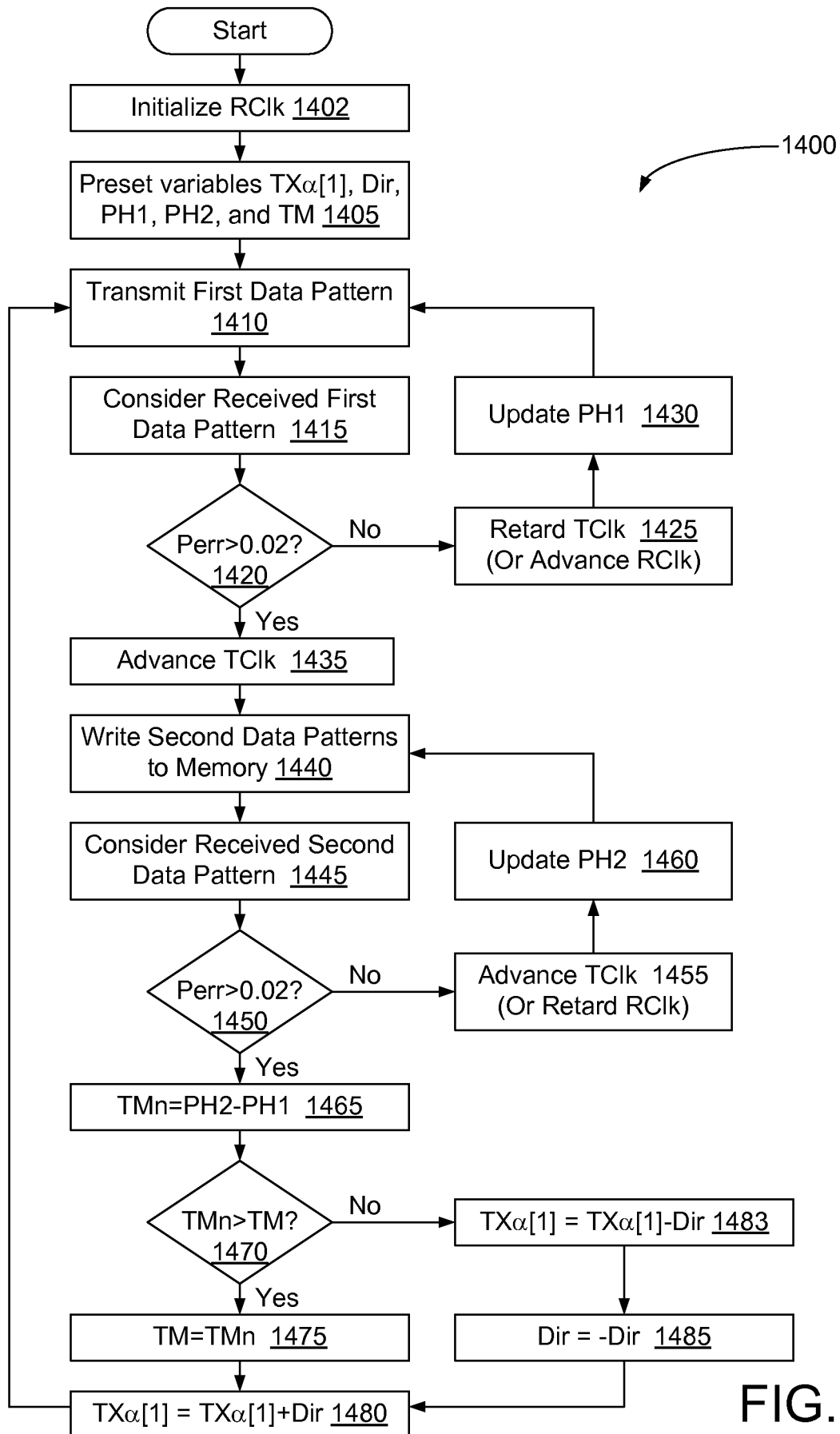


FIG. 14

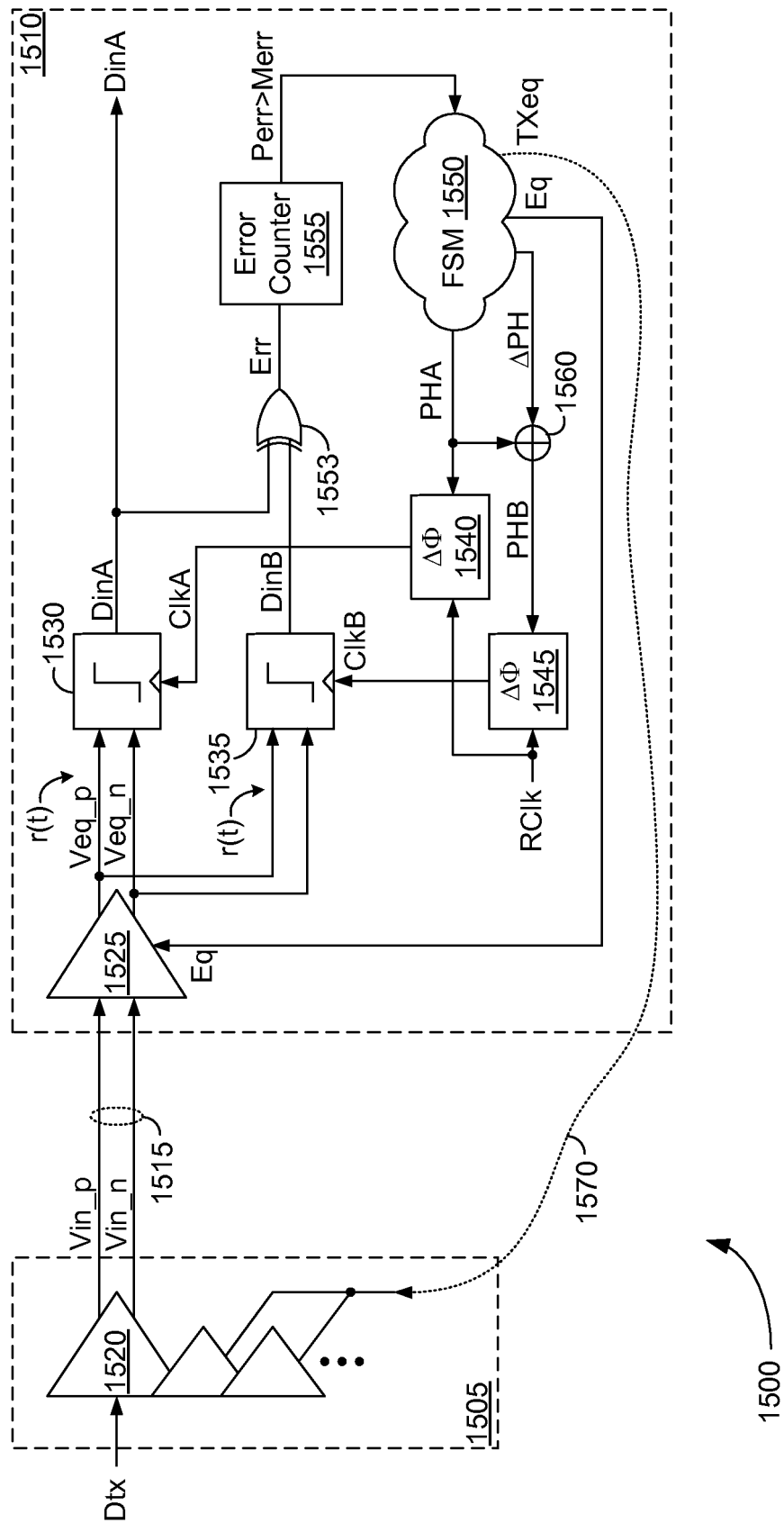


FIG. 15

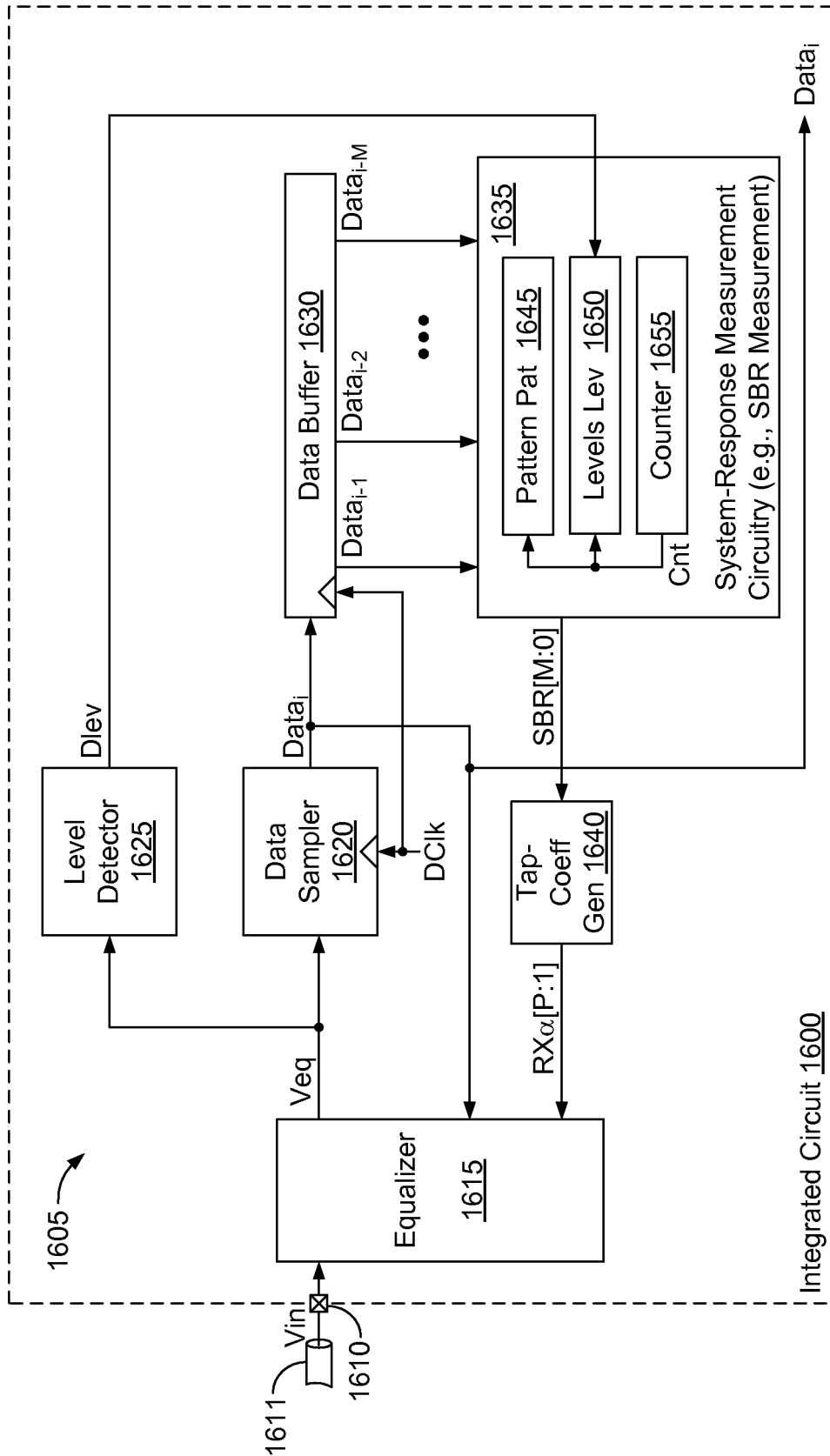


FIG. 16

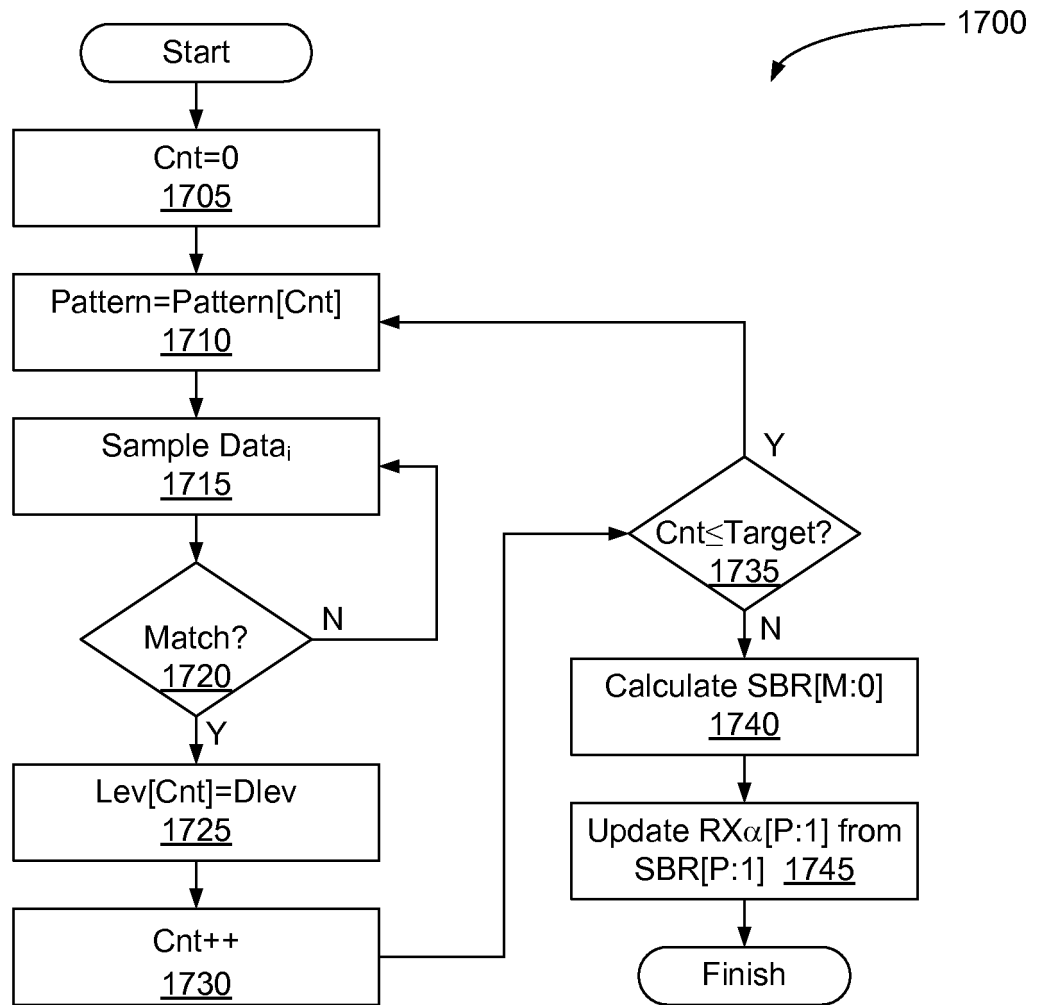


FIG. 17A

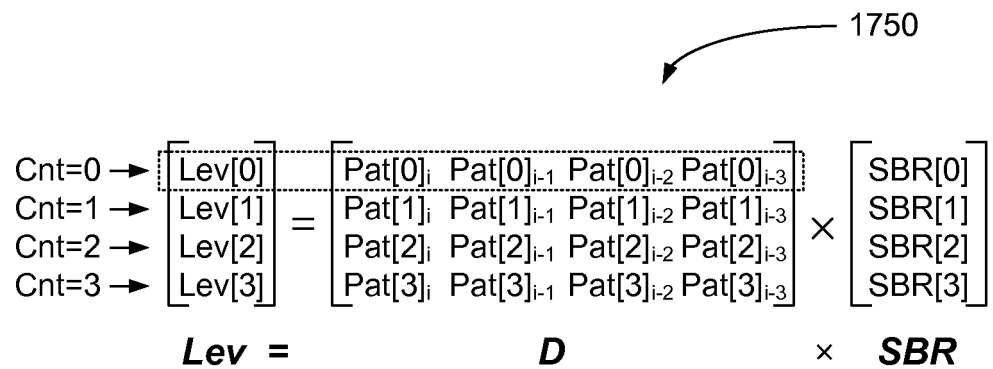


FIG. 17B

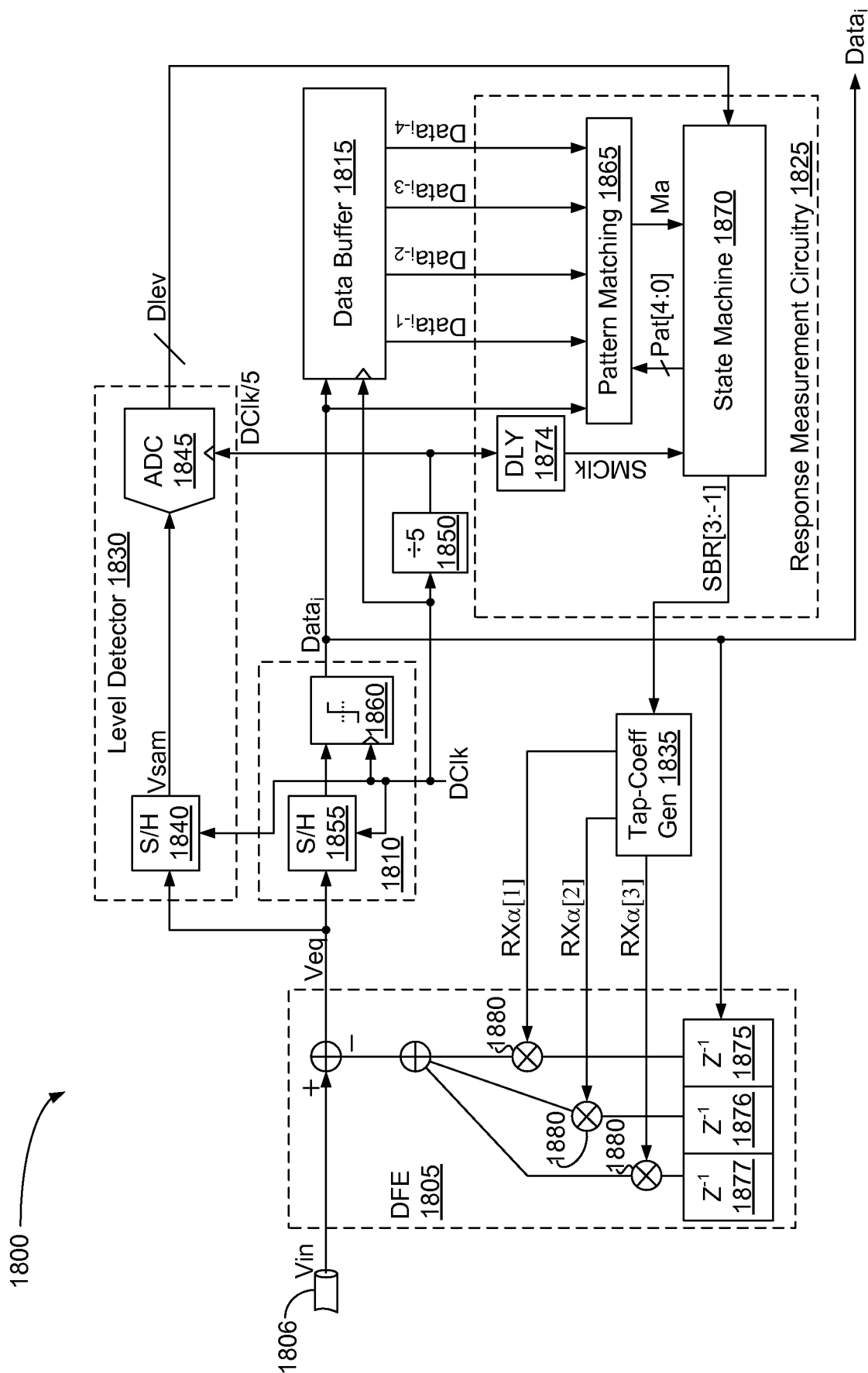


FIG. 18

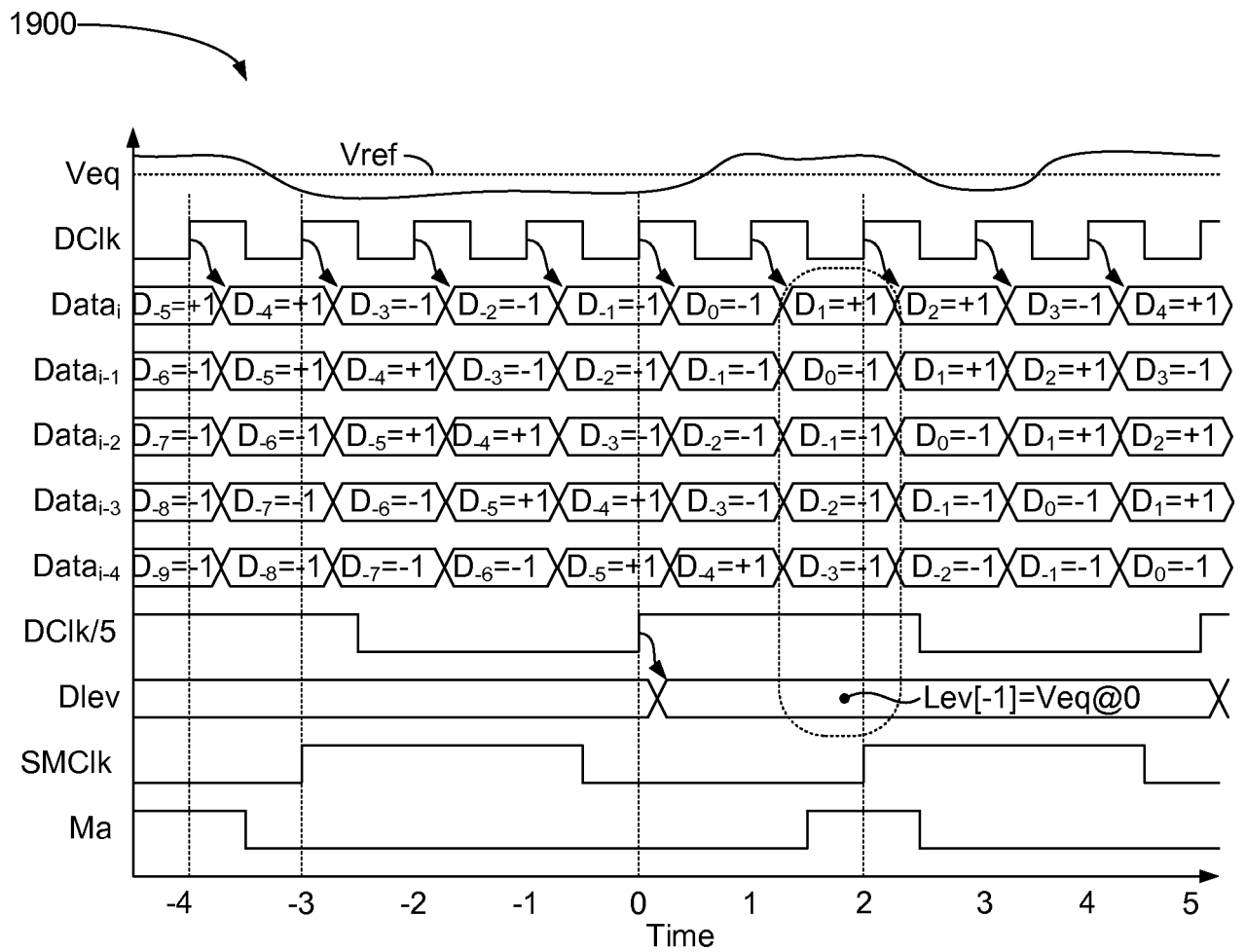


FIG. 19A

2000

$$\begin{array}{l}
 \text{Pattern}[0] \\
 \text{Pattern}[1] \\
 \text{Pattern}[2] \\
 \text{Pattern}[3] \\
 \text{Pattern}[4]
 \end{array}
 \begin{array}{c}
 V_{eq_i} \\
 \left[\begin{array}{c} Lev[-1] \\ Lev[0] \\ Lev[1] \\ Lev[2] \\ Lev[3] \end{array} \right]
 \end{array}
 =
 \begin{array}{c}
 D_{i+1} \quad D_i \quad D_{i-1} \quad D_{i-2} \quad D_{i-3} \\
 \left[\begin{array}{ccccc} +1 & -1 & -1 & -1 & -1 \\ -1 & +1 & +1 & -1 & +1 \\ -1 & -1 & +1 & -1 & +1 \\ -1 & +1 & -1 & +1 & +1 \\ -1 & -1 & -1 & -1 & +1 \end{array} \right]
 \end{array}
 \times
 \begin{array}{c}
 \left[\begin{array}{c} SBR[-1] \\ SBR[0] \\ SBR[1] \\ SBR[2] \\ SBR[3] \end{array} \right]
 \end{array}$$

$Lev = D \times SBR$

FIG. 20

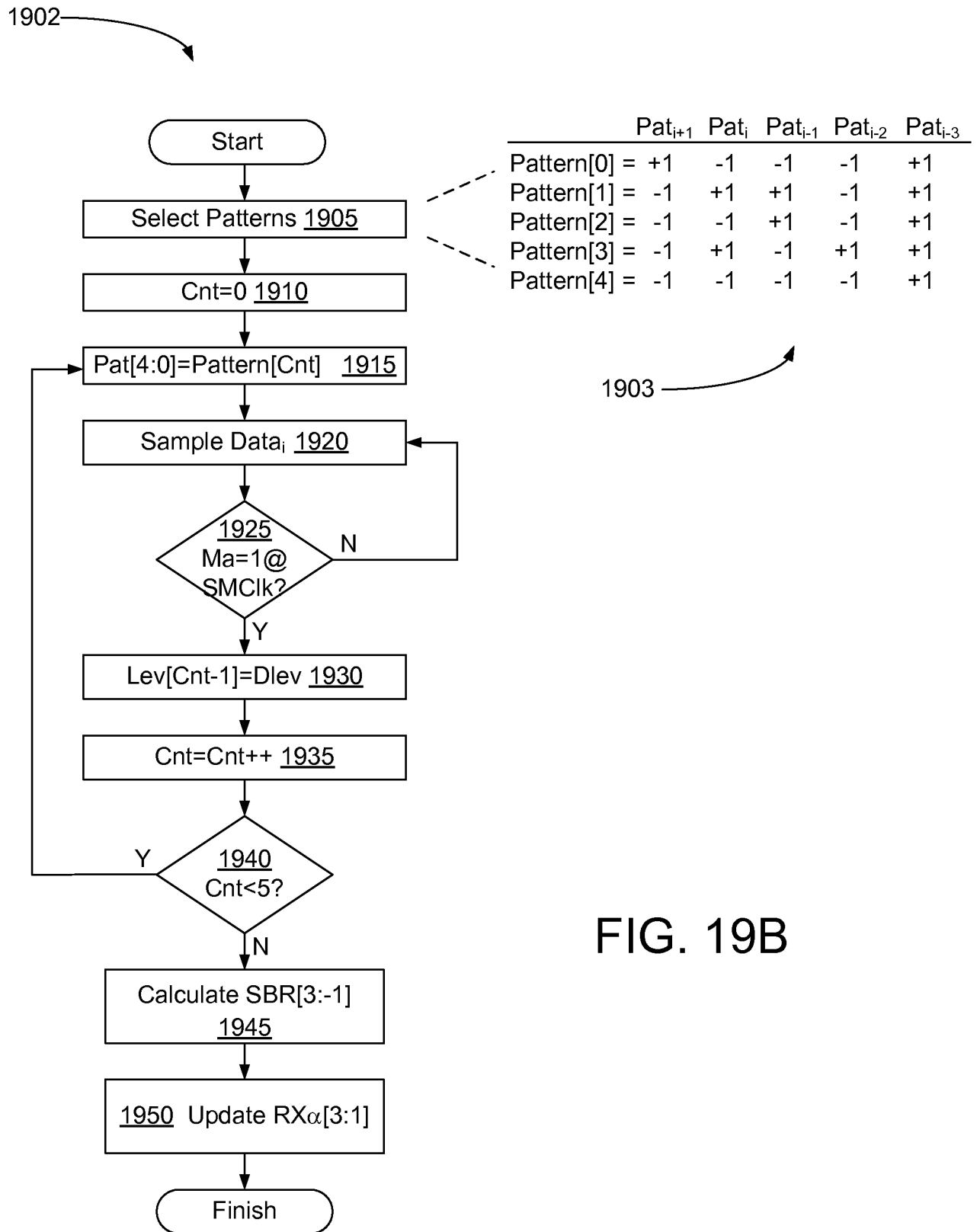


FIG. 19B

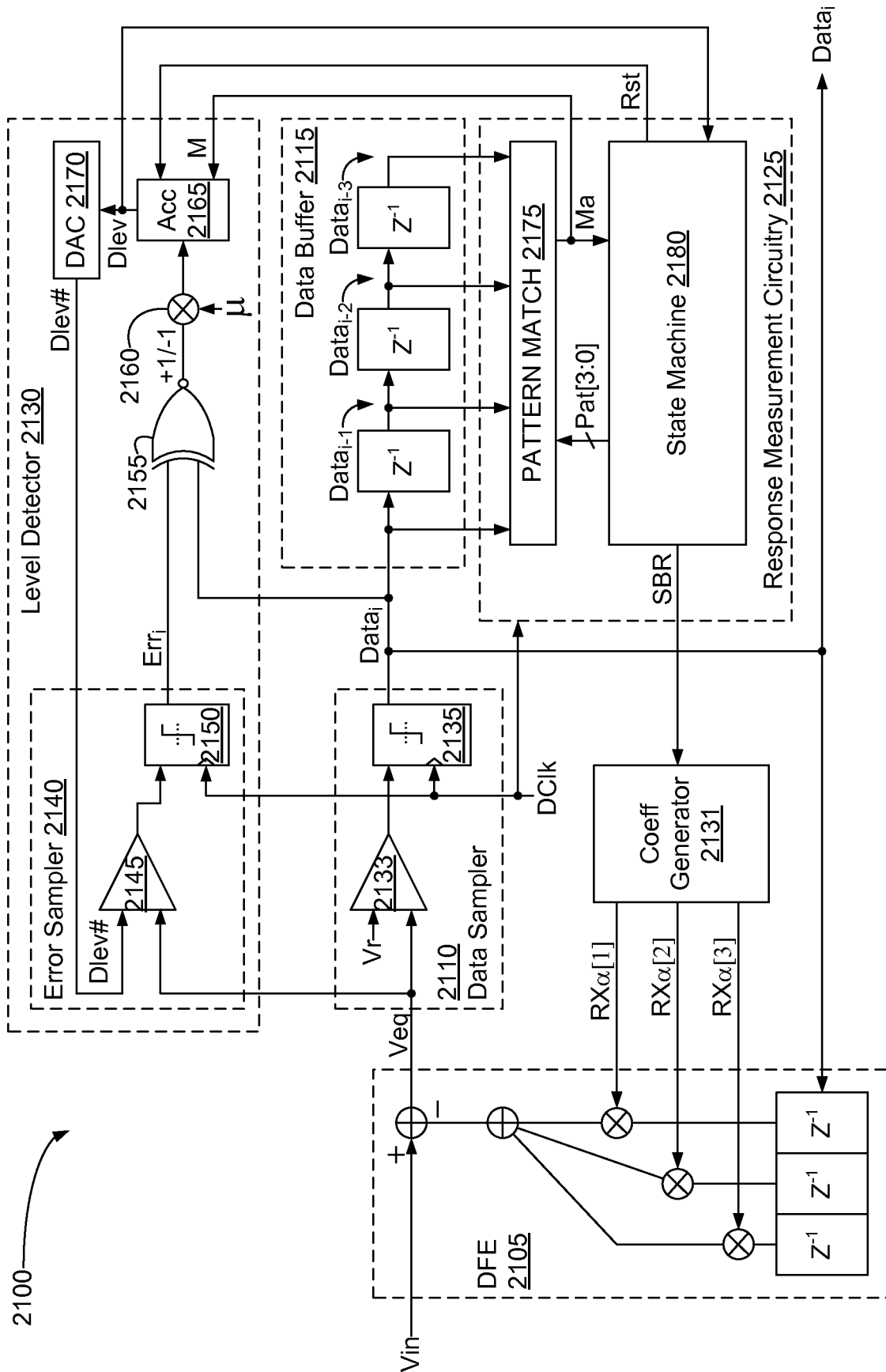


FIG. 21

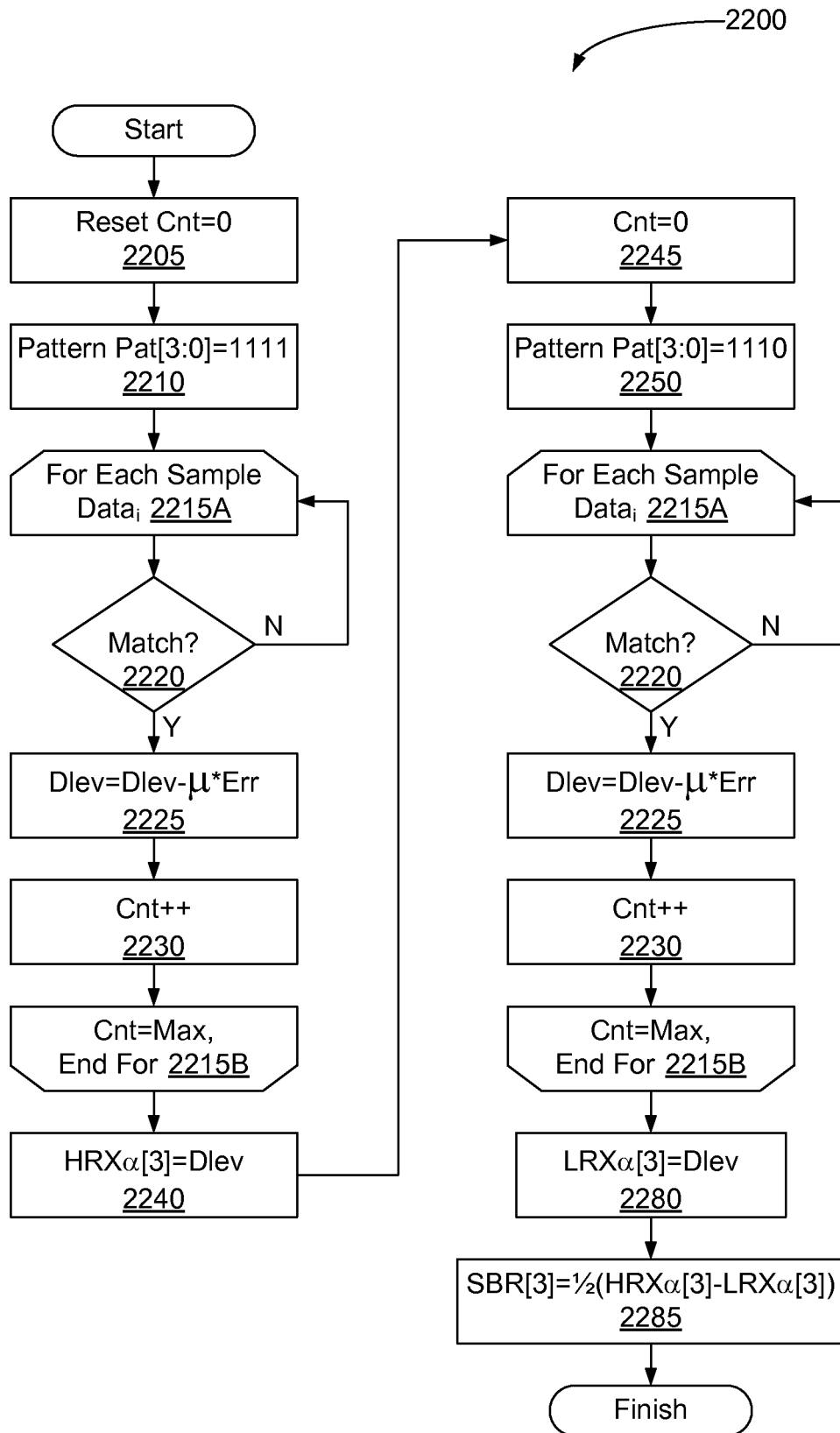


FIG. 22

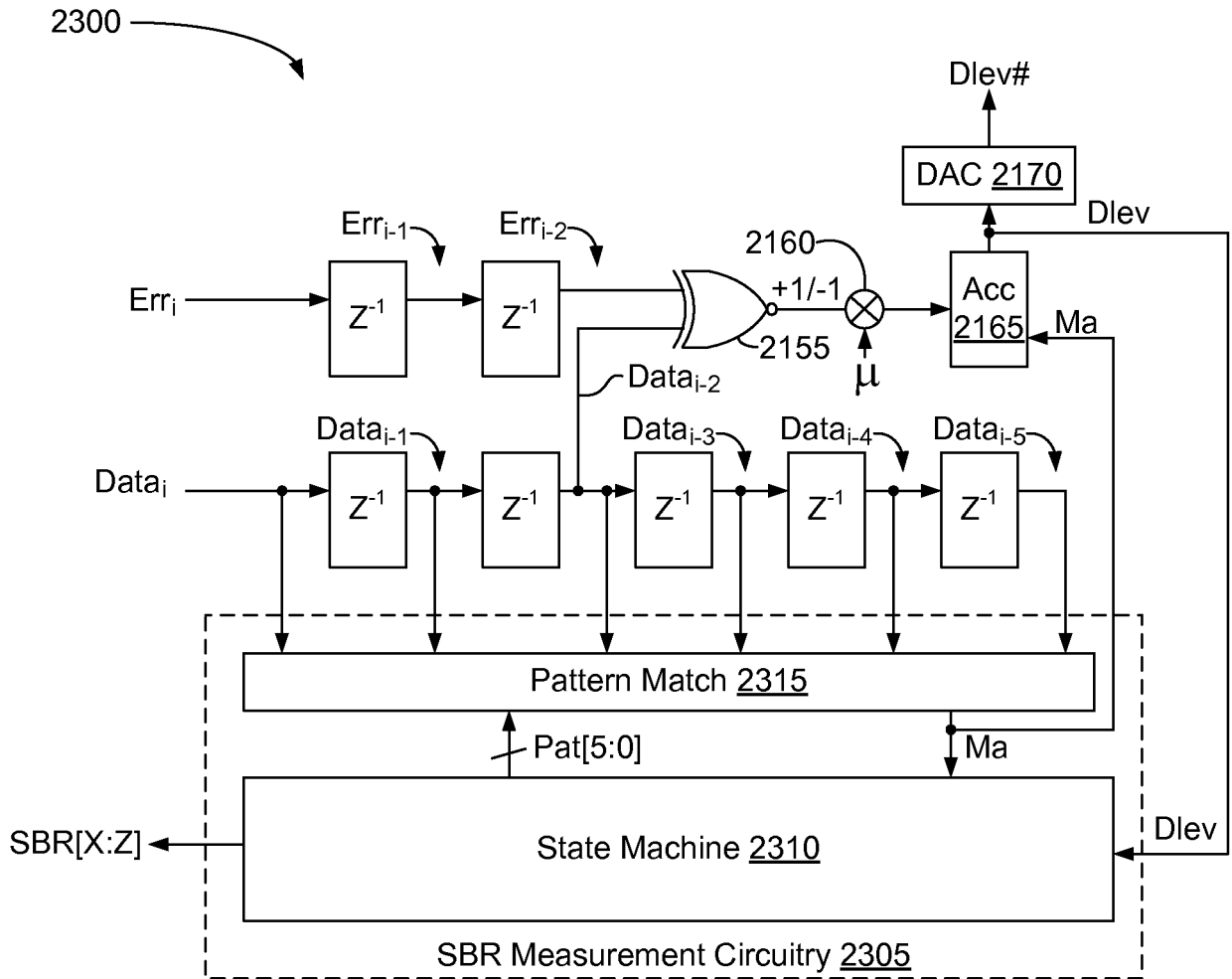


FIG. 23

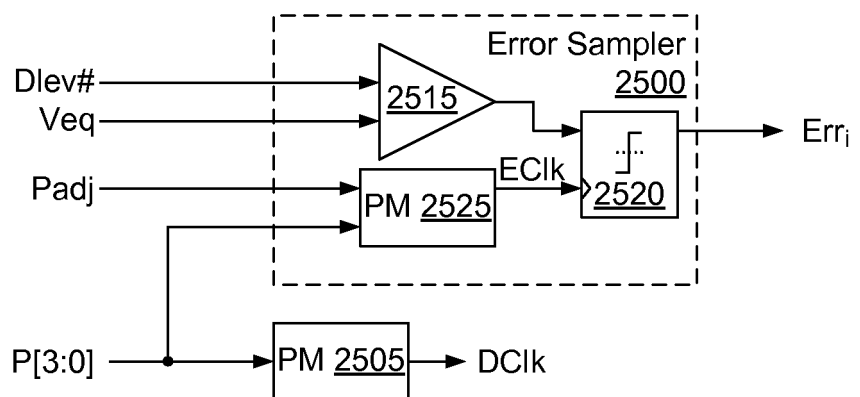


FIG. 25

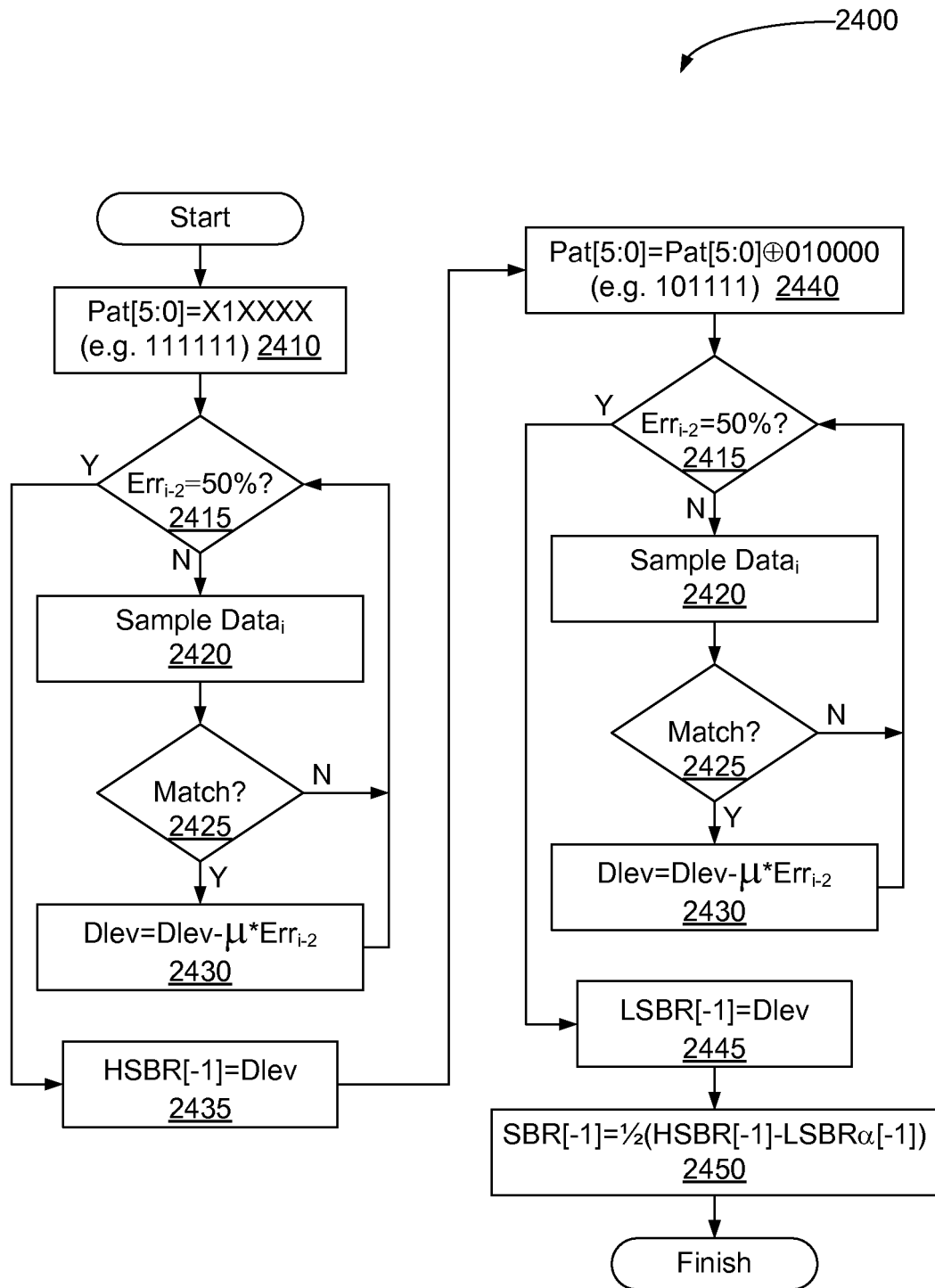


FIG. 24

2600

Cnt=0 →

Cnt=1 →

Cnt=2 →

Cnt=3 →

Cnt=4 →

Cnt=5 →

Cnt=6 →

Cnt=7 →

Lev[0]

Lev[1]

Lev[2]

Lev[3]

Lev[4]

Lev[5]

Lev[6]

Lev[7]

=

R1_N

R2_N

R3_N

R4_N

R5_N

R6_N

R7_N

R8_N

R1_{N-1}

R2_{N-1}

R3_{N-1}

R4_{N-1}

R5_{N-1}

R6_{N-1}

R7_{N-1}

R8_{N-1}

R1_{N-2}

R2_{N-2}

R3_{N-2}

R4_{N-2}

R5_{N-2}

R6_{N-2}

R7_{N-2}

R8_{N-2}

R1_{N-3}

R2_{N-3}

R3_{N-3}

R4_{N-3}

R5_{N-3}

R6_{N-3}

R7_{N-3}

R8_{N-3}

×

RE[0]

RE[1]

RE[2]

RE[3]

+

F1_N

F2_N

F3_N

F4_N

F5_N

F6_N

F7_N

F8_N

F1_{N-1}

F2_{N-1}

F3_{N-1}

F4_{N-1}

F5_{N-1}

F6_{N-1}

F7_{N-1}

F8_{N-1}

F1_{N-2}

F2_{N-2}

F3_{N-2}

F4_{N-2}

F5_{N-2}

F6_{N-2}

F7_{N-2}

F8_{N-2}

F1_{N-3}

F2_{N-3}

F3_{N-3}

F4_{N-3}

F5_{N-3}

F6_{N-3}

F7_{N-3}

F8_{N-3}

×

FE[0]

FE[1]

FE[2]

FE[3]

Lev =

RD

×

RE

+

FD

×

FE

FIG. 26A

2605

Cnt=0 →

Cnt=1 →

Cnt=2 →

Cnt=3 →

Cnt=4 →

Cnt=5 →

Cnt=6 →

Cnt=7 →

Lev[0]

Lev[1]

Lev[2]

Lev[3]

Lev[4]

Lev[5]

Lev[6]

Lev[7]

=

RD

×

FD

×

RE[0]

RE[1]

RE[2]

RE[3]

FE[0]

FE[1]

FE[2]

FE[3]

Lev =

ED

×

EDGEResp

FIG. 26B