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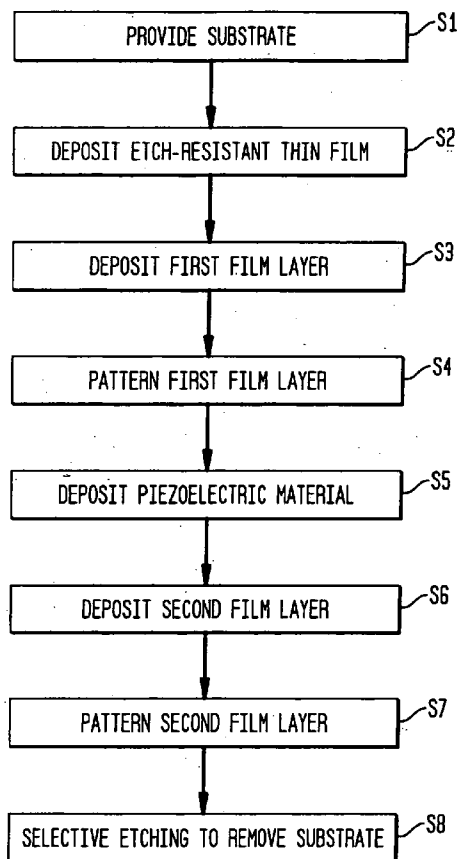
(19) **United States**(12) **Patent Application Publication****Fetter et al.**(10) **Pub. No.: US 2004/0163244 A1**(43) **Pub. Date: Aug. 26, 2004**(54) **METHOD OF MANUFACTURING AND MOUNTING ELECTRONIC DEVICES TO LIMIT THE EFFECTS OF PARASITICS**(52) **U.S. Cl. 29/840**(75) Inventors: **Linus Albert Fetter**, Morganville, NJ (US); **Yin-Huen Wong**, Summit, NJ (US); **Michael George Zierdt**, Belle Mead, NJ (US)(57) **ABSTRACT**

A method of producing and mounting electronic devices to negate the effects of parasitics on device performance. In one aspect, the substrate surface of the device is coated with a thin, etch-resistant film during fabrication that acts as a barrier to allow removal of substrate material beneath the film, creating a suspended structure upon which the remaining layers of circuitry rest. Alternatively the device is made with a film that is integral to the device, and that acts as the supporting membrane. To mount the device on a carrier or package, solder bumps are applied near the ends of the conductors of the device, and the die is then secured to a carrier or package, and positioned so that leads extending from the conductors mate up with bonding strips on the carrier or package. The solder bumps are then reflowed or melted to establish electrical connection between leads of the device and corresponding bonding strips of the carrier. The resultant electronic device is essentially immune to the effects of parasitic capacitances and parasitic inductances, with the device as mounted being further configured so as to tune out any residual parasitics which may still exist after fabrication.

Correspondence Address:

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 8910
RESTON, VA 20195 (US)(73) Assignee: **Agere Systems Inc.**(21) Appl. No.: **10/742,916**(22) Filed: **Dec. 23, 2003****Related U.S. Application Data**

(62) Division of application No. 09/698,175, filed on Oct. 30, 2000, now Pat. No. 6,675,450.

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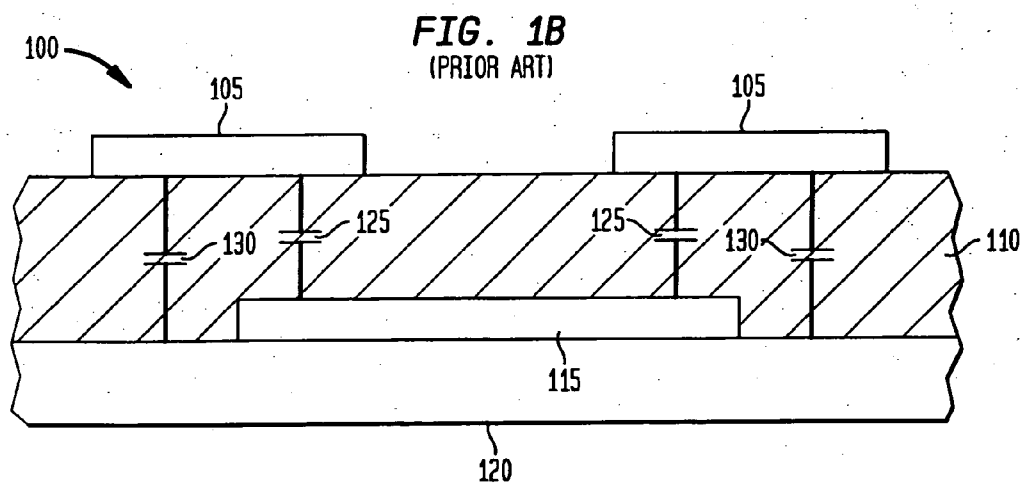
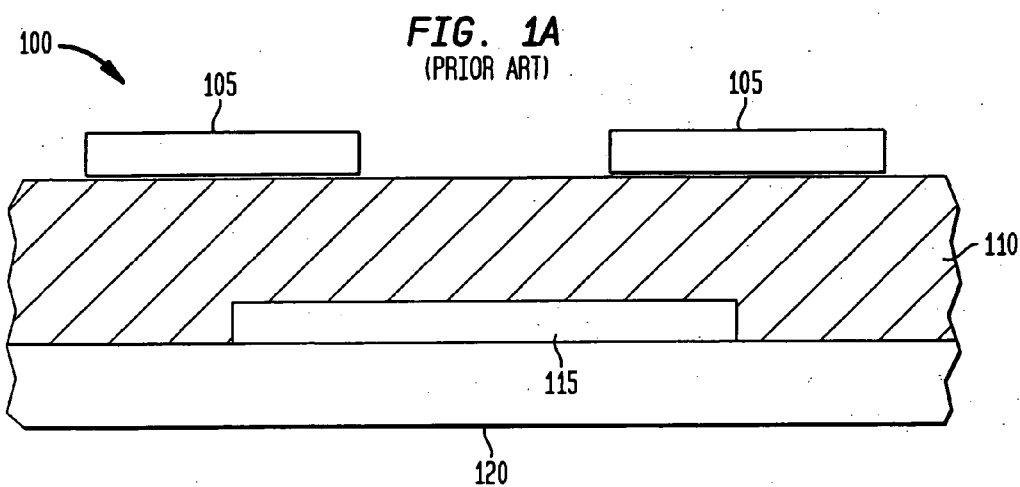


FIG. 2
(PRIOR ART)

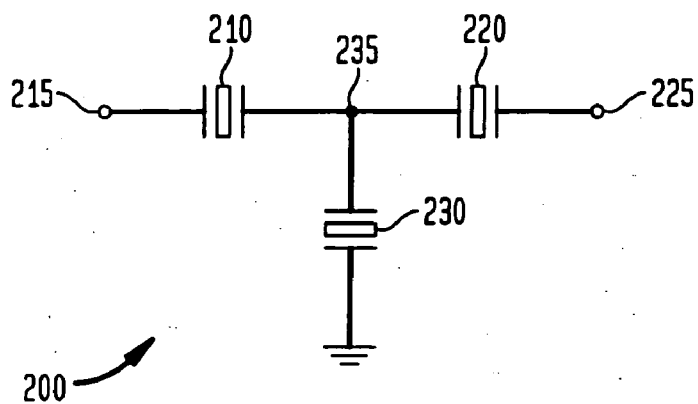


FIG. 4

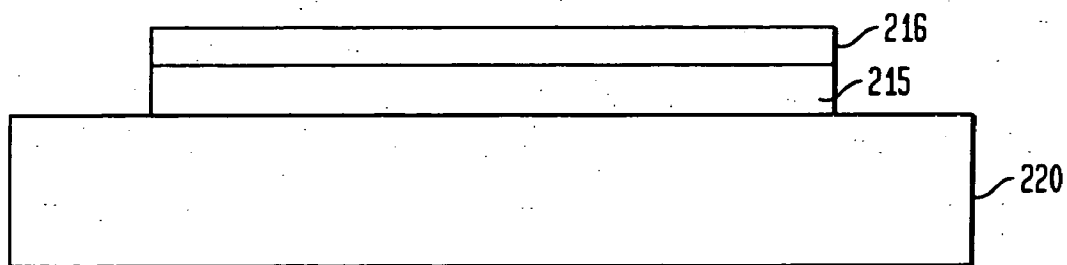


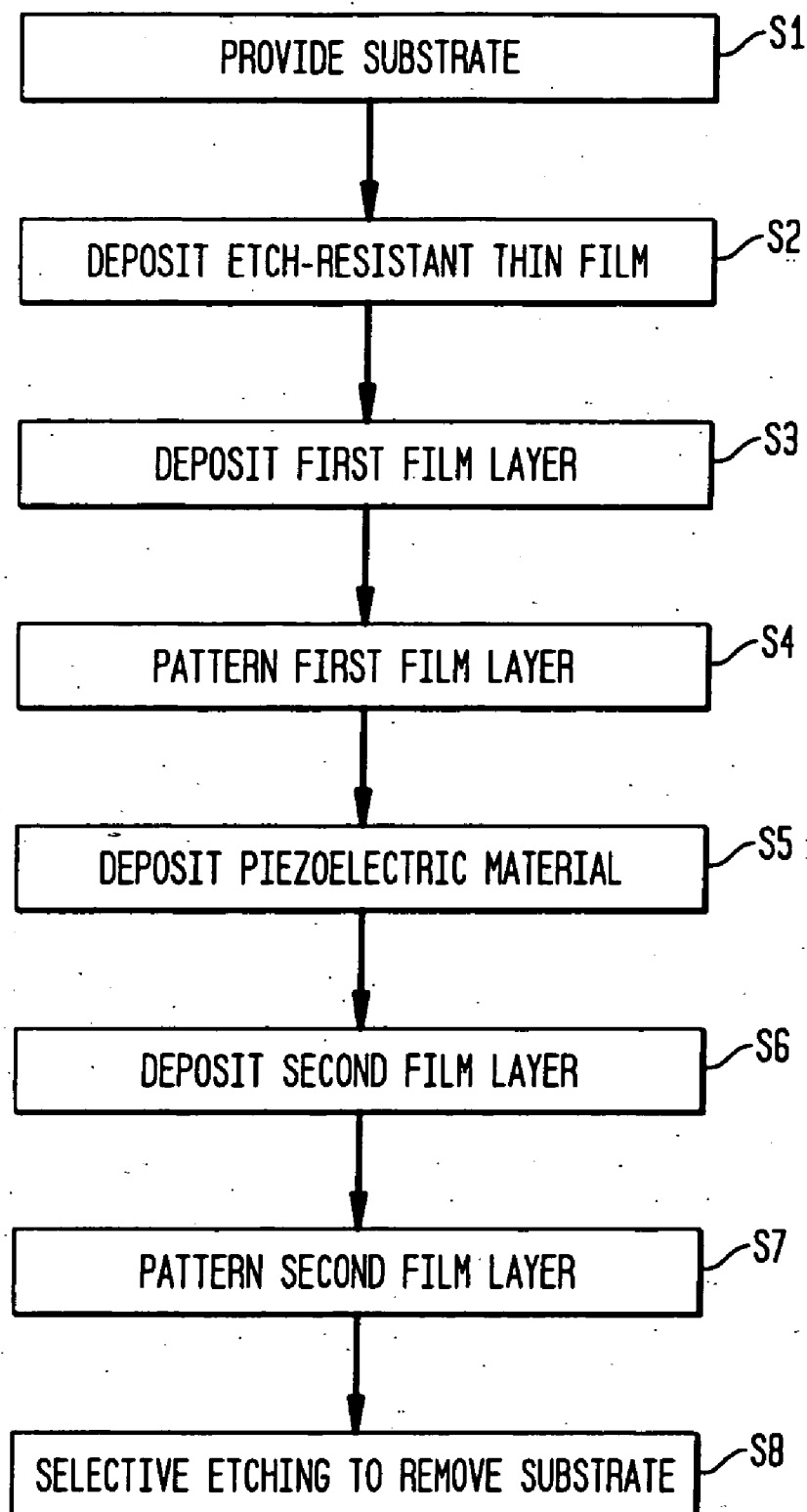
FIG. 3

FIG. 5A

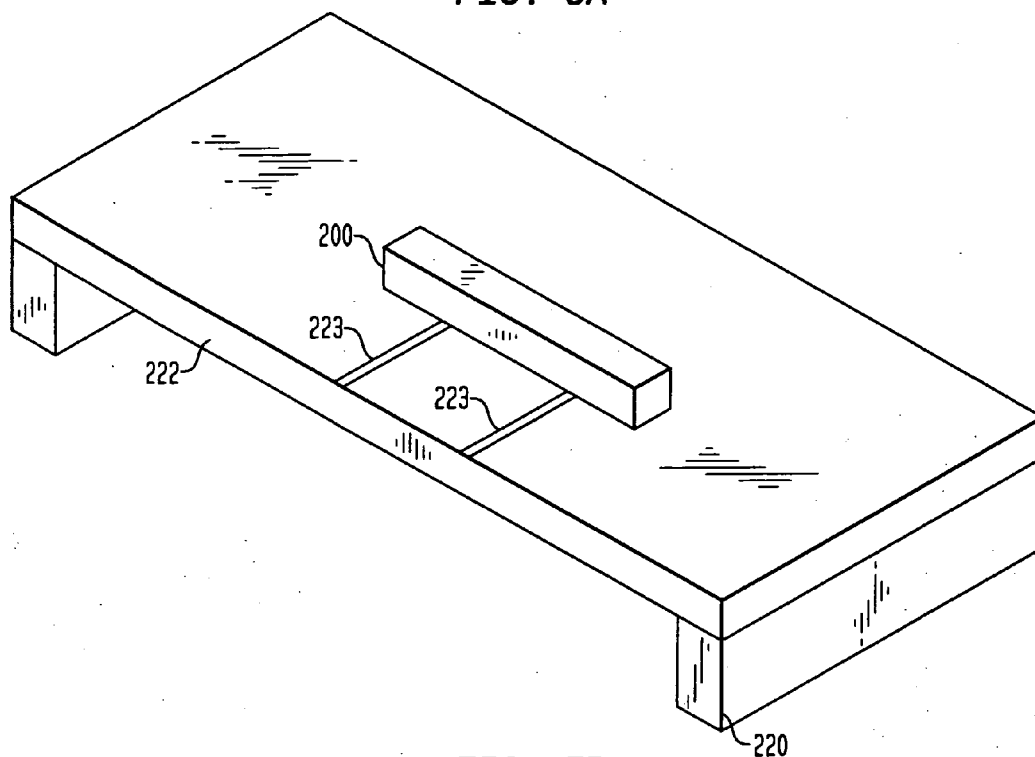


FIG. 5B

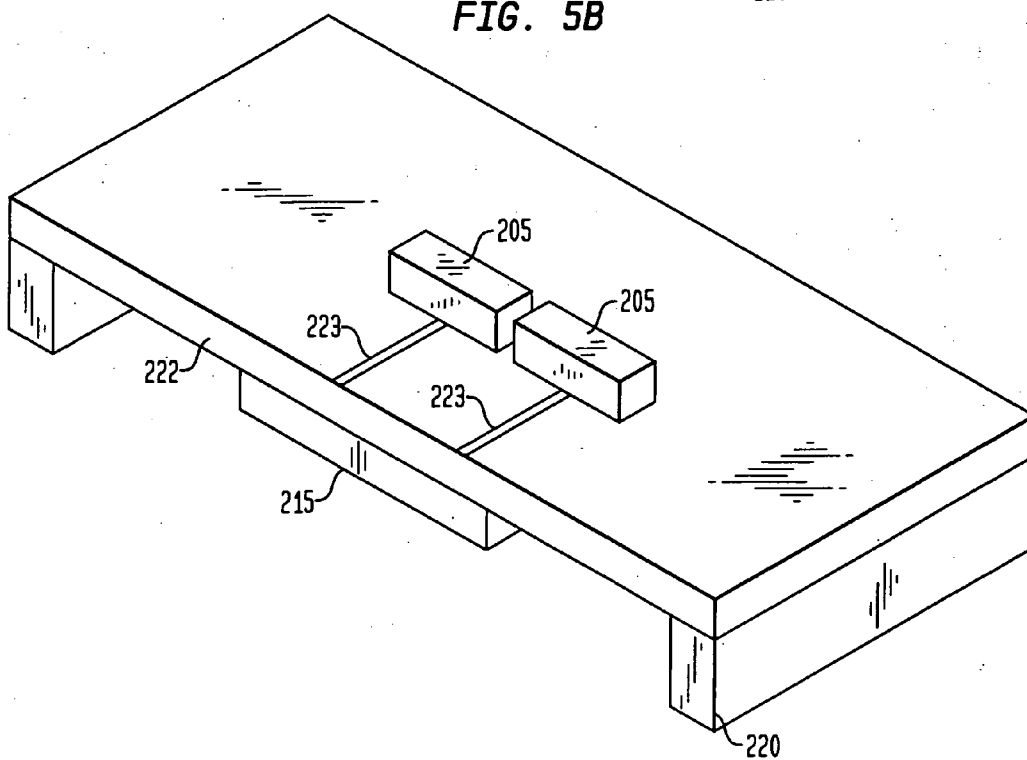


FIG. 6

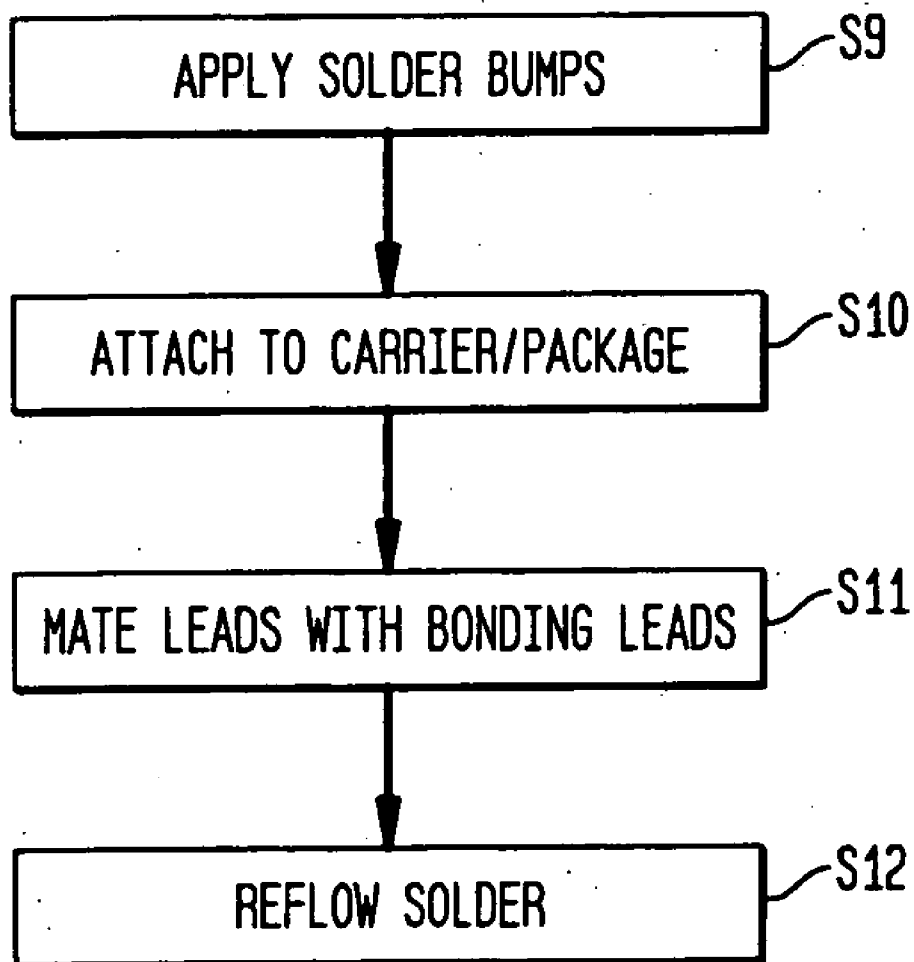
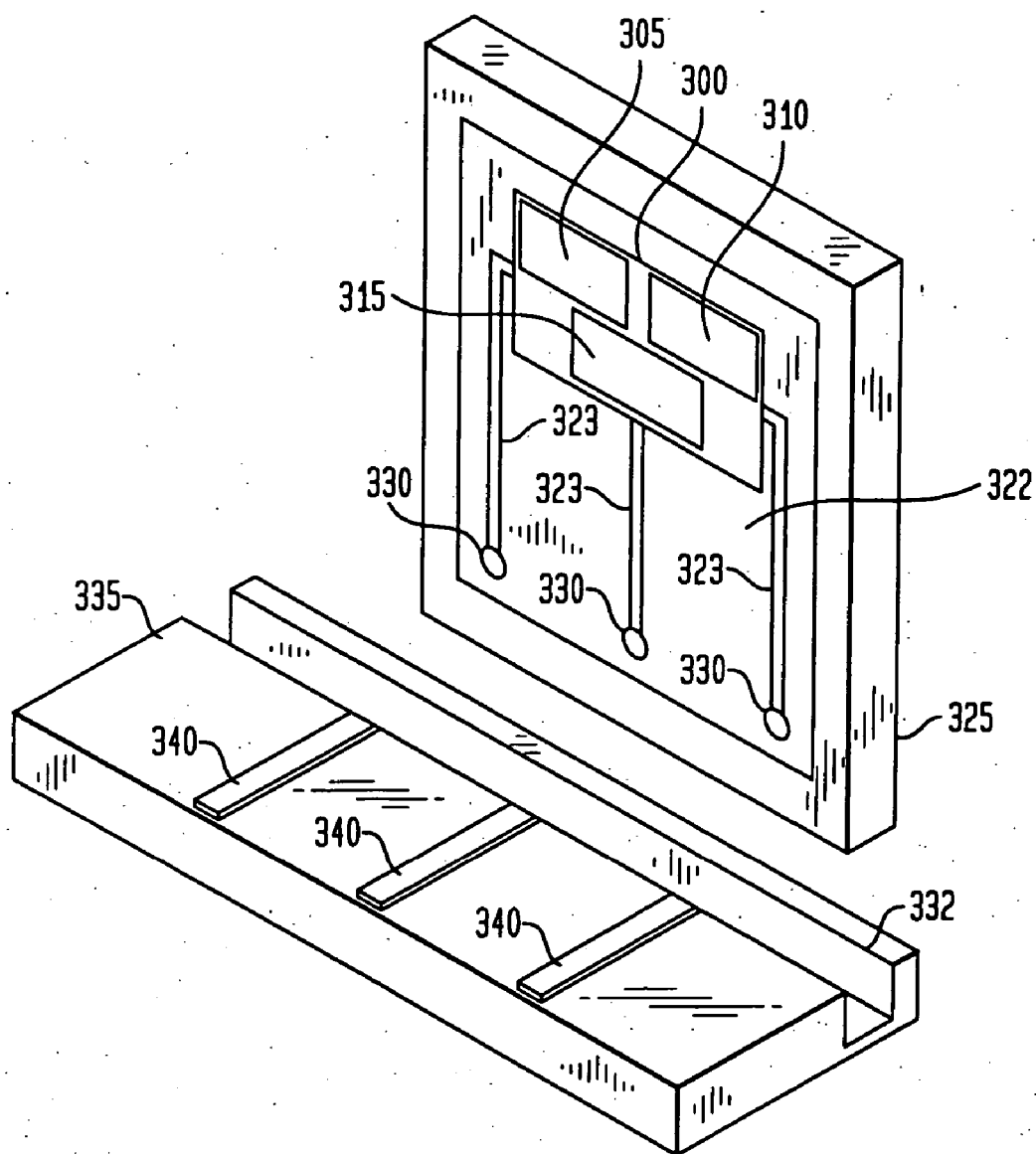


FIG. 7



METHOD OF MANUFACTURING AND MOUNTING ELECTRONIC DEVICES TO LIMIT THE EFFECTS OF PARASITICS

CONTINUATION INFORMATION

[0001] This application is a divisional of co-pending application Ser. No. 09/698,175, filed on Oct. 30, 2000, the entire contents of which are hereby incorporated by reference herein, and for which priority is claimed under 35 U.S.C. § 120.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to electronic devices, more particularly to methods for manufacturing and mounting electronic devices such as thin film resonators (TFRs) to limit parasitic effects.

[0004] 2. Description of the Related Art

[0005] Electronic devices such as thin film resonators (hereinafter "TFR") are typically used in high-frequency, high-power environments ranging from several hundred megahertz (MHz) to several gigahertz (GHz). FIG. 1 illustrates a side view or cross-section of a typical TFR component 100. In FIG. 1, TFR component 100 includes a piezoelectric material 110 interposed between two conductive electrode layers 105 and 115, with electrode layer 115 formed on a support structure 120. The support structure 120 may be a membrane, or may be a plurality of alternating reflecting layers on a solid semiconductor substrate which may be made of silicon or quartz, for example. The piezoelectric material is preferably one selected from the group comprising at least ZnO, CdS and AlN. Electrode layers 105 and 115 are formed from a conductive material, preferably of Al, but may be formed from other conductors as well.

[0006] TFRs are often used in electronic signal filters, more particularly in TFR filter circuits applicable to a myriad of communication and microelectronic technologies. For example, TFR filter circuits may be employed in cellular, wireless and fiber-optic communications, as well as in computer or computer-related information-exchange or information-sharing systems.

[0007] The piezoelectric material in TFR resonators converts electrical to mechanical energy and vice versa, such that at its mechanical resonance frequency, the electrical behavior of the device abruptly changes. Electrical signals of particular frequencies easily pass through the resonators, while others will not be transmitted. These particular frequencies can typically be dictated by choosing resonator size and design. Resonators of certain sizes and design frequencies can be networked in appropriate combinations, such that they will impose desired filtering functions on signals passing through the network.

[0008] A standard approach to designing filters out of resonators is to arrange them out of simple building blocks such as in a ladder configuration, that is, in an alternating series-shunt relationship. A series element in this sense carries signal from an input toward an output, whereas a shunt element provides an alternative path for the signal to ground. The transmission or blocking characteristics of both series and shunt elements affect the final signal reaching

output from input, somewhat analogous to how branching of water pipes can affect the flow through the main water line.

[0009] FIG. 2 illustrates schematically this simple building block, commonly known as a T-Cell. Referring specifically to FIG. 2, a schematic of a T-Cell building block 200 includes three TFR components 210, 220 and 230. TFR components 210 and 220 comprise the "series arm" portion of the T-Cell block, being connected in series between an input port 215 and an output port 225 of T-Cell 200. TFR component 230 comprises the "shunt leg" portion of T-Cell 200, being connected in shunt between node 235 and ground. A TFR T-Cell itself may define a filter; although a TFR ladder filter typically has a plurality of these T-cells concatenated together.

[0010] As can be seen from FIG. 1, many electronic devices fabricated today using planar technologies are built on silicon wafers. In some of these devices, only the first few microns of the wafer's bulk or thickness are involved in the device's performance. In other devices, this wafer serves only as a mechanical support.

[0011] As will be described in further detail below, the manufacturing process for many electronic devices, a TFR being just one exemplary device, often entails the deposition and patterning of several metallic layers that in a final form serve as integral parts of the device, and/or as interconnects between these integral parts.

[0012] One of the most serious and persistent problems regarding the above device is the effects of parasitic capacitances and inductances on device performance. These parasitics are typically created by interactions between the substrate and the layers forming the device; and/or these parasitic capacitances and inductances are already present in the connecting layers within the device. In general, any pair of conducting or semi-conducting plates separated by a dielectric material may act as a capacitor, and any strip of conducting material may act as an inductor. Such structures are often included as part of a circuit's design. However, these structures may also occur incidentally as part of a circuit's physical layout.

[0013] FIG. 1(b) illustrates parasitic capacitors which could be present within the TFR device of FIG. 1(a). FIG. 1(b) is essentially the TFR of FIG. 1(a), but illustrates capacitors which may be intended in its design (see at 125); and those capacitors which may be incidental to the TFR's layout (see at 130). These incidental (i.e., parasitic) capacitors, resulting from interactions between the device structure and the substrate, tend to degrade device performance and should be accounted for and limited. Accordingly, what is needed is a method of manufacturing electronic devices such as TFRs that do not suffer from the detrimental effects that parasitics currently have on device efficiency and performance.

SUMMARY OF THE INVENTION

[0014] The present invention provides a method of manufacturing electronic devices that have at least a portion of their supporting substrate removed to eliminate parasitic capacitance. In another aspect of the invention, a mounting technique for mounting the aforementioned electronic device is described for tuning out any residual parasitics.

[0015] In one embodiment, after providing the substrate, the substrate surface is coated with a thin, etch-resistant film.

The film acts as a barrier to allow removal of at least some of the substrate material during subsequent manufacturing steps, creating a suspended structure upon which the remaining layers of circuitry rest. In another embodiment, a film which is an integral part of the device acts as the supporting membrane.

[0016] Regarding the mounting method, solder bumps are applied near the ends of conductors or electrodes of the manufactured device. The completed die (surface on which the substrate/membrane and device circuitry rest) is then inserted vertically and/or edge-on into a carrier or package that is to include the device, and the solder bumps are reflowed (i.e., melted with a conventionally used heat source) to establish contact with corresponding bonding strips on the carrier. Both the manufacturing and mounting techniques may reduce and/or eliminate the adverse effects of parasitics, since these membrane-supported devices suffer from essentially no parasitic capacitance, and little if any parasitic inductance.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The present invention will become fully understood from the detailed description given hereinbelow and the accompanying drawings, wherein like elements represent like reference numerals, which are given by way of illustration only and thus are not limitative of the invention and wherein:

[0018] FIG. 1(a) illustrates a cross-section of a typical electronic device such as a thin film resonator (TFR) device.

[0019] FIG. 1(b) illustrates the parasitic capacitors present in the TFR of FIG. 1(a).

[0020] FIG. 2 illustrates a T-cell building block.

[0021] FIG. 3 describes a manufacturing method in accordance with the present application.

[0022] FIG. 4 illustrates a partially fabricated TFR device.

[0023] FIG. 5(a) illustrates an electronic device supported by a non-integral membrane structure.

[0024] FIG. 5(b) illustrates an electronic device in which the supporting membrane is an integral part of the circuit.

[0025] FIG. 6 describes a mounting method in accordance with the present application.

[0026] FIG. 7 illustrates the manufactured device and a carrier in accordance with a mounting method of FIG. 6.

DETAILED DESCRIPTION

[0027] The present invention provides a method of producing and a method of mounting electronic devices that are supported by a thin membrane rather than a bulk substrate. Each method contributes to the reduction and/or elimination of electronic parasitics such as parasitic inductances and parasitic capacitances. In one aspect of fabrication, the substrate surface of the device is coated with a thin, etch-resistant film which acts as a barrier to allow removal of at least some of the substrate material during subsequent manufacturing steps, creating a suspended membrane upon which the remaining layers of circuitry rest. In another aspect, a thin film that is integral with the device may support the device, so that no additional etch-resistant film

is required during fabrication. In either case, substantial elimination of substrate parasitics is accomplished when, as a final production step, some or substantially all of the substrate material is removed in an etchant.

[0028] To mount the device, solder bumps (i.e., small balls of conducting metal material having a low melting point) are applied near the ends of the conductors or electrodes of the device. The completed die on which the membrane-mounted device rests is secured into a carrier or package that is to contain the device. The solder bumps are then reflowed to establish contact between leads of the electrodes and corresponding bonding strips on the carrier.

[0029] The resultant membrane mounted electronic device has a substantially reduced presence of parasitics and/or parasitic effects than current electronic devices, since these parasitics are induced by the very presence of the bulk supporting substrate on which conventional electronic devices rest. Since a substantial portion of the substrate is removed, any parasitics which could have been induced therein are effectively eliminated with the removal of substrate material. Further, any residual parasitics that might still be present in the membrane are further eliminated when the device is mounted in a "tuning" carrier or package, i.e., these parasitics can be electronically eliminated or tuned out.

[0030] Accordingly, these membrane-supported devices suffer from essentially no parasitic capacitance, and from little parasitic inductance. As will be described below, capacitors and inductors arranged on the carrier's surface may also be implemented in order to tune out any remaining parasitics. In other words, the resultant electronic device is essentially immune to the effects or parasitic capacitances and parasitic inductances, with the mounted device being configurable so as to tune out any residual parasitics that may still exist after fabrication.

[0031] Although the below discussion focuses on the fabrication of a thin film resonator (TFR) device, the method of manufacturing and method of mounting in accordance with the present application is not limited to such a device. As may be recognized by those having ordinary skill in the art, the present application is applicable to any electronic device which has a wafer-like substrate or membrane, and/or which is manufactured using a series of deposition and patterning steps to form integral layers of the device.

[0032] FIG. 3 illustrates the method of manufacturing an electronic device such as a TFR in accordance with the present application. Though there can be a variety of thin film process steps involved in the batch fabrication of a TFR device (as there is in fabricating any modern integrated circuit or electronic device), the vast majority of these processes involve repeated applications of three primary operations: deposition, lithography, and etching.

[0033] Referring to FIG. 3, initially a base support structure such as a substrate is provided (Step S1). In conventional devices, the base structure is often not integral to device operation; it provides only mechanical support. The base structure in the present embodiment, hereinafter "substrate" is preferably a silicon wafer substrate. Alternatively, the substrate may include a plurality of alternating reflecting layers of acoustically mismatched materials such as SiO₂ and AlN that are deposited on a wafer substrate of silicon, quartz, or glass wafer. This process is now described in more

detail below, and illustrates one aspect as to how the detrimental effects of parasitics may be eliminated.

[0034] After providing the substrate, a thin, etch resistant film or membrane is applied to the substrate (Step S2). This film may be a thin layer of AlN or SiN, for example, and may act as the supporting membrane. This film is preferably applied by chemical vapor deposition (CVD), but may also be applied with techniques such as physical vapor deposition (PVD), evaporation, etc., or application techniques familiar to one practiced in the art. Alternatively, and as noted above, a thin film that is integral to the device may ultimately serve as the substrate (membrane). For example, in fabricating a TFR, the piezoelectric material (AlN) may serve a dual role as the supporting membrane, sandwiched by conductor or electrode layers attached thereto.

[0035] Next, a thin metal film layer (approximately 100 nanometers or 100×10^{-9} meters thick) is deposited on the substrate surface (Step S3). This deposition may preferably be performed in a vacuum chamber using one of the above-described plurality of thin-film deposition techniques. In the present embodiment, this metal film acts as a bottom surface electrode for the TFR and is preferably composed of Al, but other conductors may be used as well. This deposition may preferably be performed in a vacuum chamber using one of a variety of thin-film deposition techniques, as described above.

[0036] Once the metal film has been deposited, it undergoes a patterning process (Step S4). A lithographic process is employed in which a thin layer of a photo-sensitive, chemically-resistant polymer, or "photo resist", is applied to completely coat the metal film. Exposure to light through a "photo mask", a material or masking layer that has holes or openings at certain locations for light to pass, sensitizes the photo resist such that subsequent immersion in a developer removes only that resist material that was subject to the light. At this point, the sample surface consists of regions where the protective resist layer remains, and regions of un-protected metal. This extent or nature of this patterning process may be based on the desired application; i.e., in TFR applications, this patterning is determined by the design of the desired or required filter.

[0037] The base or bottom electrode patterning process continues with the transfer of this lithographically-defined pattern into the metal layer via an etching process. A number of etching techniques are routinely practiced in the art, including wet chemical etching (KOH), dry or reactive ion etching (RIE), and sputter etching. Such processes, through either chemical or physical action, remove any metal which is unprotected by the photo resist, while leaving the resist-coated metal intact, thereby "sculpting" the metallic surface into the desired electrode pattern.

[0038] An electrode defined by such a process is illustrated in FIG. 4. Resist 216 has protected metal layer 215 during the removal of all unprotected material on substrate 220. When the remaining photo resist material 216 is removed by a solvent or polymer etching process, a metallic layer 215 defined by the desired pattern remains. The semi-completed device is then returned to the vacuum chamber for the deposition of some type of intermediate film (Step S5). In the present embodiment, this is an active piezoelectric material film.

[0039] Similar to the metal deposition alternatives listed above, the piezoelectric layer can be deposited in different

ways, such as through RF sputtering of an insulating target, pulsed DC reactive sputtering of a metallic target, chemical vapor deposition (CVD) and molecular beam epitaxy (MBE) for example. This piezoelectric material is preferably Aluminum Nitride (AlN) as in the presently described embodiment, but may be composed of ZnO or CdS for example. Similar to the metal film, the AlN film is deposited entirely over the substrate, but unlike the metal film it is not patterned in this embodiment.

[0040] The intermediate film is subsequently coated with a second thin metal film layer of Al or other suitable conductor, so as to form the top electrode of the device (Step S6). This second metal film is patterned and etched (Step S7) with the lithographic process as described above in Step S4. Once the photo resist is removed, the structure of the device is almost complete.

[0041] The final step in the device's fabrication consists of masking the substrate for selective removal of at least some, or even all of the substrate material underlying the device. After masking, the exposed Si may be etched with either wet (KOH, for example) or dry (RIE) chemistry (Step S8). This Si etch terminates on the initially-deposited etch-resistant film or a film which is integral to device operation (i.e., AlN, SiN or ZnO for example), as is appropriate for the desired device or application.

[0042] FIGS. 5(a) and 5(b) illustrate two exemplary embodiments of a membrane-supported electronic device. FIG. 5(a) illustrates a device supported by a non-integral membrane; the membrane acts only as a mechanical support structure. Referring to FIG. 5(a), the membrane 222 is in fact the etch-resistant film of Step S2 in FIG. 3. Film 222 results from the removal of substrate 220, and spans the un-etched remnants of the Si substrate 220 to support a device 200, but does not form an integral part of that device 200. It is noted that some residual Si may remain, hence "remnants", even after material is removed by selective etching. Wires or leads 223 patterned as part of the device fabrication process carry electronic signals to and from the device 200.

[0043] FIG. 5(b) illustrates a device in which the supporting membrane is an integral part of the device. Note that, in the latter figure, no membrane film deposition (as described in step S2 of FIG. 3) would be required. Referring to FIG. 5(b), a membrane 222 spanning the un-etched remnants of the Si substrate 220 supports material on both its faces (top electrodes 205 and bottom electrode 215) and, as in the case of a TFR 200, communication between the top and bottom mounted electrodes is accomplished through the membrane 222. The membrane, in this case, is an integral part of the device and may be made of piezoelectric material such as AlN and SiN, for example, or any other known materials which have piezoelectric properties. The electrodes 205 and 220 remain supportably attached to film 222 due to inherently strong bonding properties occurring between the layers, as is known to those skilled in the art. Wires or leads 223, which may be patterned as part of the device fabrication process, carry the electronic signal to and from the device, such as via top electrodes 205 as shown in FIG. 5(b).

[0044] FIG. 6 describes steps of the mounting technique of the present application: FIG. 7 illustrates the membrane-mounted device attached to a carrier in accordance with a mounting technique described in FIG. 6. In general, a

completed device such as shown in FIGS. 5(a) and/or 5(b) would be inserted into a carrier or package assembly, or even another integrated circuit, for example. Solder bumps that had been previously applied to the electrodes of the device would then be reflowed (melted) to create an electrical connection to the carrier. A surface of the carrier on which the device is attached or connected may then be configured with, or contain circuitry thereon to tune out any residual parasitics (capacitances or inductances) that may still be present in the device.

[0045] In the exemplary arrangement as shown in FIG. 7, after fabrication of the TFR device 300, solder bumps are applied to the electrodes (step S9 in FIG. 6). In FIG. 7, there is illustrated a TFR device 300 in a T-Cell configuration on top of membrane 322 that rests on die 325. Leads 323 (i.e., leads from the metal electrodes of the device) extend from series resonators 305 and 310 and shunt resonator 315 respectively to the edge of the membrane 322.

[0046] At the ends of these leads 323, corresponding solder bumps (small balls of conductive material) 330 may be provided or applied by conventionally known soldering techniques, or those currently being used in the art. The die 325 may then be attached to a carrier or package (step S10), inserted in an edge-on fashion into a recess 332 that may be provided on a package or carrier 335, as shown in FIG. 7 for example. The die 325 is positioned (step S11) such that the solder bumps 330 contact corresponding bonding leads 340, and then the solder is reflowed (i.e., melted by conventionally known or used heat sources) (step S12) in order to solidify the electrical connections between device 300 and carrier 335. Mounted in this configuration, residual parasitics are substantially negated since, with minimal or no substrate, any possible capacitor or inductor configuration which could be a source of such parasitics (i.e., parallel plates separated by a dielectric) no longer exists, or is minimized to the extent that it does not interfere with device performance.

[0047] If required, circuitry for tuning out any residual parasitics can be built or provided on the carrier mounting surface 335. For example, and with the understanding that capacitor reactance is typically a negative reactance and inductor reactance typically a positive reactance, capacitor and/or inductor elements could be added on the surface of the carrier 335 where necessary, between at least one of the bonding leads and ground. Thus, in an exemplary case where there might be residual inductive parasitics present, capacitors may be employed to offset or cancel the positive inductor reactance with a negative capacitor reactance, and vice versa.

[0048] The invention being thus described, it will be obvious that the same may be varied in many ways. For example, each of the deposition and patterning steps illustrated in FIG. 3 (steps S3-S7) may be repeated several times in order to build up a device for whatever application is desired. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and also to modifications as would be obvious to one skilled in the art or intended to be included within the scope of the following claims.

What is claimed is:

1. An thin film resonator (TFR) device, comprising:

a substrate having an etch-resistant thin film thereon; and

a piezoelectric material layer formed between first and second conductors, said first conductor contacting said etch-resistant thin film, the etch-resistant thin film and substrate configured as a suspended membrane supporting said first and second conductors and said piezoelectric layer.

2. The TFR device of claim 1, wherein the etch resistant film acts as a barrier to allow removal of substantially all of said substrate to form a membrane that supports said piezoelectric layer and said first and second conductors.

3. The TFR device of claim 1, wherein said piezoelectric material is a material selected from a group consisting of AlN, SiN and ZnO.

4. The TFR device of claim 1, wherein said first and second conductors are Al metal electrodes or other conductors.

5. The TFR device of claim 1, wherein said substrate is formed of silicon, quartz, or glass.

6. The TFR device of claim 1, wherein said substrate is essentially immune to effects of parasitic capacitance and inductance.

7. The TFR device of claim 1, further comprising a plurality of solder bumps that are applied to ends of leads extending from said first and second conductors, wherein said leads are formed on a die that supports the TFR device.

8. The TFR device of claim 7,

wherein the die is attached to a carrier or package intended for the device so that said solder bumps contact corresponding bonding leads on said carrier or package; and

wherein the solder bumps are reflowed to effect electrical connection to the carrier or package.

9. The TFR device of claim 8, wherein the carrier or package connected device is configured so that the effects of any residual parasitic capacitances and parasitic inductances are negated or limited.

10. An electronic device, comprising:

a substrate having an etch-resistant thin film thereon; and

a piezoelectric layer formed between first and second conductor layers, the etch-resistant thin film forming a suspended membrane for supporting the electronic device.

11. The device of claim 10, wherein the etch resistant film thereon acts as a barrier to allow removal of substantially all of said substrate to form the suspended membrane supporting said piezoelectric layer and conductor layers of the electronic device.

12. The device of claim 10, wherein

said piezoelectric material is selected from a group consisting of AlN, SiN and ZnO;

said conductive films are Al metal electrodes or other conductors; and

said substrate is formed of silicon, quartz, or glass and is essentially immune to the effects of parasitic capacitance and parasitic inductance.

13. The device of claim 10, further comprising a plurality of solder bumps applied to ends of leads extending from said conductors, wherein said leads are formed on a die that supports the device.

14. The device of claim 13, wherein the die is attached to a package intended for the device so that said solder bumps contact corresponding bonding leads on said package; and the solder bumps are reflowed to effect electrical connection to the package.

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