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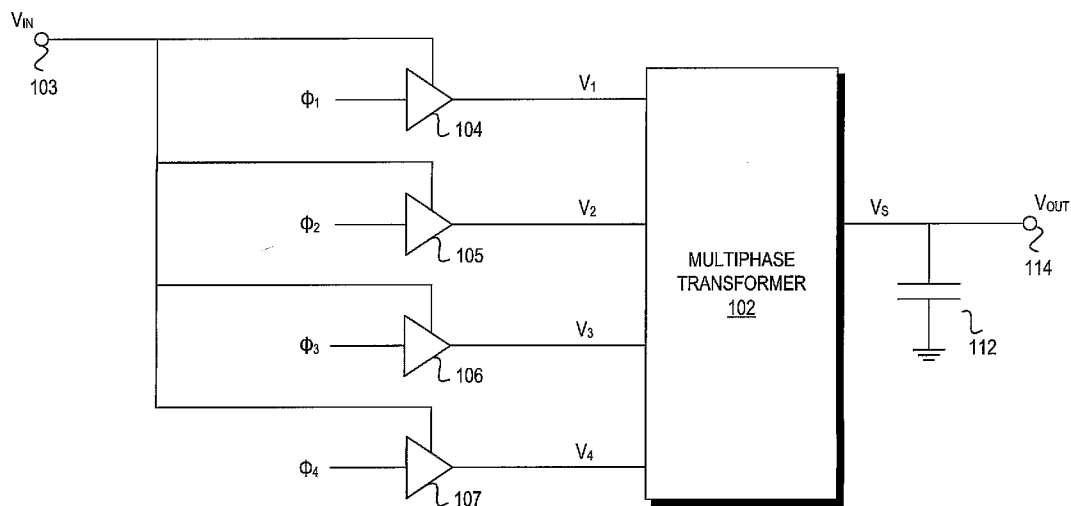
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(54) Title: MULTIPHASE TRANSFORMER FOR A MULTIPHASE DC-DC CONVERTER



MULTIPHASE DC-DC
CONVERTER
100

(57) Abstract: A multiphase DC-DC converter is provided that includes a multiphase transformer, the multiphase transformer including a plurality of input voltage terminals and an transformer output voltage terminal, each input voltage terminal associated with a corresponding phase. Each phase is assigned to an input voltage terminal of the plurality of input voltage terminals to minimize a ripple current at the input voltage terminals of the multiphase transformer.

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MULTIPHASE TRANSFORMER FOR A MULTIPHASE DC-DC
CONVERTER

BACKGROUND

5 Field

Embodiments of the invention relate to the field of power converters and more specifically, but not exclusively, to a multiphase transformer for a multiphase DC-DC converter.

10 Background Information

Direct Current to Direct Current (DC-DC) converters are able to convert energy from a power supply from one voltage and current level to another voltage and current level. DC-DC converters are utilized in conjunction with various computing systems such as desktop, servers, and
15 home electronics. DC-DC converters may also be found in mobile computer systems such as laptops, mobile phones, personal digital assistants, and gaming systems.

Today's microprocessors may consume 100-200 Watts of power. A DC-DC converter may be used to provide power to a processor that requires
20 low voltages, such as 0.5 to 2.0 volts (V), and high currents, such as 100 amperes (A) or more. Further, the current demands of processors may change over a relatively wide range with a relatively high slew rate.

Multiphase DC-DC converters may be used to provide the high-current low-voltage demands of computing systems. Today's multiphase

DC-DC converters may use discrete-inductor topologies, which require large filter capacitances and may not be suitable for monolithic integration. Other multiphase DC-DC converters may include multiphase transformer topologies that fail to maximize the efficiency of the DC-DC converter. Also, 5 such multiphase DC-DC converters fail to take into account the order that phases are assigned to the multiphase transformer.

BRIEF DESCRIPTION OF THE DRAWINGS

Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following figures, wherein like reference numerals refer to like parts throughout the various views unless
5 otherwise specified.

Figure 1A is a block diagram illustrating a multiphase DC-DC converter in accordance with one embodiment of the present invention.

Figure 1B is a diagram illustrating voltage waveforms of a multiphase DC-DC converter in accordance with one embodiment of the present
10 invention.

Figure 2 is a circuit diagram illustrating a cyclic cascade multiphase transformer in accordance with one embodiment of the present invention.

Figure 3 is a circuit diagram illustrating a DC-DC converter floorplan using a cyclic cascade multiphase transformer in accordance with one
15 embodiment of the present invention.

Figure 4 is a circuit diagram illustrating a modified cyclic cascade multiphase transformer in accordance with one embodiment of the present invention.

Figure 5 is a circuit diagram illustrating a DC-DC converter floorplan using a modified cyclic cascade multiphase transformer in accordance with
20 one embodiment of the present invention.

Figure 6A is a circuit diagram illustrating a mixed cyclic cascade multiphase transformer in accordance with one embodiment of the present invention.

Figure 6B is a circuit diagram illustrating a mixed cyclic cascade multiphase transformer in accordance with one embodiment of the present invention.

Figure 7 is a circuit diagram illustrating a DC-DC converter floorplan using a mixed cyclic cascade multiphase transformer in accordance with one embodiment of the present invention.

Figure 8 is a flowchart illustrating the logic and operations to assign phases to a multiphase transformer in accordance with one embodiment of the present invention.

Figure 9A is a diagram illustrating the assignment of phases to a multiphase transformer in accordance with one embodiment of the present invention.

Figure 9B is a diagram illustrating the assignment of phases to a multiphase transformer in accordance with one embodiment of the present invention.

Figure 9C is a graph illustrating the efficiency trend with different numbers of phases in accordance with embodiments of the present invention.

Figure 10 is a block diagram illustrating a multiphase DC-DC converter in accordance with one embodiment of the present invention.

Figure 11A is a block diagram illustrating a system having a multiphase DC-DC converter in accordance with one embodiment of the present invention.

Figure 11B is a block diagram illustrating a computer system in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

In the following description, numerous specific details are set forth to provide a thorough understanding of embodiments of the invention. One skilled in the relevant art will recognize, however, that embodiments of the invention can be practiced without one or more of the specific details, or with other methods, components, materials, etc. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring understanding of this description.

Reference throughout this specification to “one embodiment” or “an embodiment” means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearances of the phrases “in one embodiment” or “in an embodiment” in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

In the following description and claims, the term “coupled” and its derivatives may be used. “Coupled” may mean that two or more elements are in direct contact (physically, electrically, magnetically, optically, etc.). “Coupled” may also mean two or more elements are not in direct contact with each other, but still cooperate or interact with each other.

Turning to Figure 1A, an embodiment of a multiphase DC-DC converter 100 is shown. Multiphase DC-DC converter 100 may also be referred to as a Multiphase Voltage Regulator Module (VRM) in the relevant

art. In one embodiment, multiphase DC-DC converter 100 is an integrated on-die device. Multiphase DC-DC converter 100 includes a multiphase transformer 102 in accordance with embodiments described herein. Various embodiments of multiphase transformer 102 will be described below.

5 Multiphase DC-DC converter 100 receives an input voltage V_{IN} at terminal 103. The input voltage is applied to bridge 104, 105, 106, and 107. Each bridge also receives a corresponding control signal ($\Phi_1 - \Phi_4$). In one embodiment, switch control of the bridges 104-107 uses pulse-width modulation (PWM). While Figure 1A shows a multiphase DC-DC converter
10 with four phases, it will be understood that embodiments of the invention are not limited to a multiphase transformer having four phases.

In general, the phases are shifted by a multiple of $360/N$ degrees, where N is the number of phases. For example, in Figure 1B, the four phases N of multiphase DC-DC converter 100 are shifted by multiples of 90
15 degrees, e.g., 90, 180, and 270 degrees. Transformer output voltage V_S has a residual ripple voltage (and corresponding ripple current) due to the switching of the bridges. In one embodiment, a capacitor is used to minimize this ripple voltage.

Each bridge 104-107 outputs a voltage V_1-V_4 , respectively, that is
20 applied to corresponding terminals of multiphase transformer 102. Voltages V_1-V_4 are the switching PWM waveforms according to the control signals ($\Phi_1 - \Phi_4$). The assignment of phases to the bridge inputs for the control signals corresponds to the assignment of phases to the input terminals of the

multiphase transformer 102. The assignment of phases determines the phase shift for each transformer input terminal.

Multiphase transformer 102 produces a transformer output voltage V_S . Voltage V_S is filtered by capacitor 112 to provide output voltage V_{OUT} of
5 multiphase DC-DC converter 100 at terminal 114. Furthermore, capacitor 112 stabilizes output voltage V_{OUT} in the event of a sudden change of the load current. The required size of capacitor 112 may be reduced by increasing the number of phases and by increasing the coupling factor of the multiphase transformer.

10 In accordance with embodiments herein, phases are assigned to multiphase transformer 102 in an order to increase DC-DC converter efficiency. Converter efficiency is a ratio of the power output to the power input of the converter. Some loss occurs as the DC-DC converter converts electrical power from the input voltage level to the desired output voltage
15 level.

The assignment of phases sequentially to multiphase transformer 102, as shown in the example of Figure 1B, leads to lower converter efficiency due to high ripple currents at the transformer input voltage terminals. The efficiency degradation can be several percentage points
20 below 90%. The assignment of phases as described herein leads to DC-DC converter efficiencies of 90% or higher.

Embodiments of multiphase transformer 102 will now be discussed. It will be understood that embodiments of the invention are not limited to these multiphase transformer embodiments. Also, the multiphase

transformers are not limited to the number of phases as described. The multiphase transformers may be scaled to the number of phases as appropriate for the implementation.

Referring to Figure 2, an embodiment of a multiphase transformer 5 200 is shown. Multiphase transformer 200 uses a cyclic cascade topology. Multiphase transformer 200 includes four 2-phase transformers. In the embodiment of Figure 2, the four 2-phase transformers are implemented as coupled inductors, L1-L4.

In one embodiment, the coupled inductors include two inductors 10 magnetically coupled. The windings of the two inductors are made about the same core. As shown by the dot notation, the two inductors are wound with the same polarity and are directly coupled (as opposed to indirectly coupled). The number of windings of each inductor are the same (1:1 ratio). The dotted bar over coupled inductors L1-L4 indicates a magnetic core. In 15 one embodiment, the inductors are integrated inductors on a semiconductor die.

Voltages V_1 - V_4 are inputted to input voltage terminals 202-205, respectively. Transformer output voltage V_s at output terminal 206 is approximately $V_s = (V_1+V_2+V_3+V_4)/4 = (V_1+\dots+V_N)/N$, even in the presence of 20 large currents at any of the transformer terminals.

Input voltage terminal 202 is coupled to terminal 210 of inductor 242 of coupled inductors L1. Terminal 212 of inductor 242 is coupled to terminal 240 of inductor 256 of coupled inductor L4. Terminal 214 of inductor 244 of coupled inductors L1 is coupled to transformer output voltage V_s terminal

206. Terminal 216 of inductor 244 of coupled inductors L1 is coupled to terminal 220 of inductor 246 of coupled inductors L2.

Input voltage terminal 203 is coupled to terminal 218 of inductor 246 of coupled inductors L2. Terminal 222 of inductor 248 of coupled inductors L2 is coupled to transformer output voltage V_S terminal 206. Terminal 224 of inductor 248 of coupled inductors L2 is coupled to terminal 228 of inductor 250 of coupled inductors L3.

Input voltage terminal 204 is coupled to terminal 226 of inductor 250 of coupled inductors L3. Terminal 230 of inductor 252 of coupled inductors L3 is coupled to transformer output voltage V_S terminal 206. Terminal 232 of inductor 252 of coupled inductors L3 is coupled to terminal 236 of inductor 254 of coupled inductors L4.

Input voltage terminal 205 is coupled to terminal 234 of inductor 254 of coupled inductors L4. Terminal 238 of inductor 256 of coupled inductors L4 is coupled to transformer output voltage V_S terminal 206. And as described earlier, terminal 240 of inductor 256 of coupled inductors L4 is coupled to terminal 212 of inductor 242 of coupled inductors L1.

Turning to Figure 3, an embodiment of a floorplan of an on-die or monolithic 12-phase DC-DC converter 300 using a multiphase transformer having cyclic cascade topology is shown. DC-DC converter 300 includes two-phase transformers, such as two-phase transformer 306. The two-phase transformers are arranged in two columns so as to minimize the parasitic resistance of the connections between the transformers. The bridges, such as bridge 304, are arranged in two columns on either side of

the DC-DC converter 300. The transformers deliver the output current to the V_{CC} bumps, such as V_{CC} bump 308. The V_{CC} bumps are shown by "+" symbols in Figure 3. The V_{CC} bumps may be connected to a consumer circuit, such as a processor.

5 Referring to Figure 4, an embodiment of a multiphase transformer 400 is shown. Multiphase transformer 400 uses a modified cyclic cascade topology. Voltages V_1 - V_4 are inputted to input voltage terminals 402-405, respectively. Transformer output voltage V_S at output terminal 406 is approximately $V_S = (V_1+V_2+V_3+V_4)/4 = (V_1+\dots V_N)/N$, even in the presence of
10 large currents at any of the transformer terminals.

Input voltage terminal 402 is coupled to terminal 410 of inductor 442 of coupled inductors L1. Terminal 412 of inductor 442 is coupled to terminal 440 of inductor 456 of coupled inductors L4. Terminal 416 of inductor 444 of coupled inductors L1 is coupled to input voltage terminal 403. Terminal 414
15 of inductor 444 is coupled to terminal 418 of inductor 446 of coupled inductors L2.

Terminal 420 of inductor 446 of coupled inductors L2 is coupled to transformer output voltage V_S terminal 406. Terminal 422 of inductor 448 of coupled inductors L2 is coupled to transformer output voltage V_S terminal
20 406. Terminal 424 of inductor 448 is coupled to terminal 428 of inductor 450 of coupled inductors L3.

Input voltage terminal 404 is coupled to terminal 426 of inductor 450 of coupled inductors L3. Terminal 430 of inductor 452 of coupled inductors

L3 is coupled to terminal 434 of inductor 454 of coupled inductors L4.

Terminal 432 of inductor 452 is coupled to input voltage terminal 405.

Terminal 436 of inductor 454 is coupled to transformer output voltage V_S terminal 406. Terminal 438 of inductor 456 of coupled inductors L4 is
5 coupled to transformer output voltage V_S terminal 406. And as described above, terminal 440 of inductor 456 is coupled to terminal 412 of inductor 442 of coupled inductors L1.

Turning to Figure 5, an embodiment of a floorplan of an on-die or monolithic 12-phase DC-DC converter 500 using a multiphase transformer
10 having modified cyclic cascade topology is shown. DC-DC converter 500 includes 12 two-phase transformers, such as two-phase transformer 506. The two-phase transformers are arranged in two columns so as to minimize the parasitic resistance of the connections between the transformers. The bridges, such as bridge 504, are spread out between the transformer
15 columns. The transformers deliver the output current to the V_{CC} bumps, such as V_{CC} bump 508, shown by the "+" symbols in Figure 5. The V_{CC} bumps may be connected to a consumer circuit, such as a processor.

In the 12-phase DC-DC converter 500, the output current is delivered to the V_{CC} bumps more evenly as compared to the floorplan in Figure 3. In
20 Figure 3, the output current is delivered predominately to the V_{CC} bumps on the left and right edges of the converter block, which could overstress these bumps and leaves the bumps in the center with higher parasitic resistance. This higher parasitic resistance leads to lower efficiency and worse transient voltage droop performance.

Further, in converter 500, transformer outputs and bridges don't compete for as much metal density since they are not in the same area, as compared to converter 300. This also leads to lower parasitic resistance in converter 500.

5 Thus, converter 500 has lower parasitic resistance, and hence higher efficiency, as compared to converter 300. Converter 500 also has better transient voltage droop performance and lower thermal stress.

Referring to Figure 6A, an embodiment of a multiphase transformer 600 is shown. Multiphase transformer 600 has a mixed cyclic cascade
 10 topology. Multiphase transformer 600 includes four 2-phase transformers. In the embodiment of Figure 6A, the four 2-phase transformers are implemented as coupled inductors, L1-L4. Voltages V_1 - V_4 are inputted to input voltage terminals 602-605, respectively. Transformer output voltage V_S at output terminal 606 is approximately $V_S = (V_1+V_2+V_3+V_4)/4 =$
 15 $(V_1+\dots V_N)/N$, even in the presence of large currents at any of the transformer terminals.

Input voltage terminal 602 is coupled to terminal 610 of inductor 642 of coupled inductors L1. Terminal 612 of inductor 642 is coupled to terminal 640 of inductor 656 of coupled inductors L4. Terminal 616 of inductor 644 is
 20 coupled to terminal 620 of inductor 646 of coupled inductors L2. Terminal 614 of coupled inductors L1 is coupled to transformer output voltage V_S terminal 606.

Input voltage terminal 603 is coupled to terminal 618 of inductor 646 of coupled inductors L2. Terminal 622 of inductor 648 of coupled inductors

L2 is coupled to transformer output voltage V_S terminal 606. Terminal 624 of inductor 648 is coupled to terminal 628 of inductor 650 of coupled inductors L3.

Input voltage terminal 604 is coupled to terminal 626 of inductor 650 of coupled inductors L3. Input voltage terminal 605 is coupled to terminal 632 of inductor 652 of coupled inductors L3. Terminal 630 of inductor 652 of coupled inductors L3 is coupled to terminal 634 of inductor 654 of coupled inductors L4.

Terminal 636 of inductor 654 is coupled to transformer output voltage V_S terminal 606. Terminal 638 of inductor 656 of coupled inductors L4 is coupled to transformer output voltage V_S terminal 606. And as described above, terminal 640 of inductor 656 is coupled to terminal 612 of inductor 642 of coupled inductors L1.

In the mixed cyclic cascade 600, coupled inductors L1 and L2 are arranged as part of a cyclic cascade (as shown in Figure 2), whereas coupled inductors L3 and L4 are arranged as part of a modified cyclic cascade (as shown in Figure 4). In one embodiment of a mixed cyclic cascade topology, one or more parts may be in a cyclic cascade arrangement, while the majority may be in a modified cyclic cascade arrangement.

In one embodiment, the mixed cyclic cascade topology may have an odd number of phases, which may result in higher efficiency. In general, a modified cyclic cascade is used with an even number of phases, and usually not an odd number of phases. A modified cyclic cascade with an even

number of phases may have better efficiency than a (regular) cyclic cascade with an odd number of phases. This is due to the routing congestion incurred by the (regular) cyclic cascade. The mixed cyclic cascade may provide both: an odd number of phases and no routing congestion.

5 Turning to Figure 6B, an embodiment of a multiphase transformer 650 using a mixed cyclic topology having an odd number of phases is shown. Multiphase transformer 650 includes five 2-phase transformers. Each 2-phase transformer is implemented as coupled inductors, shown as L1-L5. In a mixed cyclic cascade topology with an odd number of phases:
10 coupled inductors L1-L4 are arranged as part of a modified cyclic cascade, whereas coupled inductors L5 are arranged as part of a (regular) cyclic cascade.

 Turning to Figure 7, an embodiment of a floorplan for an on-die or monolithic 11-phase DC-DC converter 700 using a multiphase transformer
15 having a mixed cyclic cascade topology is shown. DC-DC converter 700 includes 11 two-phase transformers, such as two-phase transformer 706. The two-phase transformers are arranged in two columns so as to minimize the parasitic resistance of the connections between the transformers. The bridges, such as bridge 704, are spread out between the transformer
20 columns. The transformers deliver the output current to the V_{CC} bumps, such as V_{CC} bump 708, shown by the "+" symbols in Figure 7. The V_{CC} bumps may be connected to a consumer circuit, such as a processor.

 Turning to Figures 8, 9A and 9B, the assignment of phases to a multiphase transformer in accordance with embodiments of the present

invention are shown. While embodiments of a multiphase transformer topology, as discussed above, provide the advantages of a multiphase transformer, that is, small output inductance and large input inductance, the actual value of the input inductance, and therefore the ripple current at the input terminals, depends on the order in which the phases are assigned to the input terminals of the multiphase transformer.

In an ideal multiphase transformer, the ripple current of individual windings will be a perfectly symmetrical triangular waveform, and thus, the order in which the phases are assigned the input terminals of the multiphase transformer would not matter. However, such an ideal multiphase transformer is not practically feasible. In one embodiment, an ideal multiphase transformer is approximated with combinations of two-phase transformers as described above in conjunction with Figures 2-7.

In one embodiment, the phases are assigned to the multiphase transformer to minimize the ripple current at the input of the multiphase transformer. The assignment of phases to the voltage input terminals of the multiphase transformer impacts the shape and effective amplitude of the ripple current that passes through the windings, and consequently, the efficiency of the multiphase DC-DC converter. The assignment of phases described below closely approximates an ideal situation keeping the input ripple current small. The phase assignment affects the input ripple current, part of which comes from the magnetization change of the core. The output ripple current is essentially independent of the phase assignment.

An embodiment for assignment of phases is as follows. Let $N =$
number of phases, $\Phi_T =$ the phase assigned to terminal T , with an angle $A =$
 $360 \cdot (\Phi_T - 1) / N$. Assign phase $\Phi_1 = 1$ to the first terminal, T_1 . Assign phases
 Φ_T to the other terminals $T = 2 \dots N$ such that the phases are equally spaced
5 and the phase differences $360 \cdot (\Phi_{T+1} - \Phi_T) / N$ are as close as possible to 180
 $+ n \cdot 360$, where n is an arbitrary integer. This can be achieved by finding the
closest integer $m = (\Phi_{T+1} - \Phi_T) < (N/2)$ such that N is not a multiple of m .
Note that if m is a solution, then so is $N - m$.

An embodiment of the above algorithm, shown by flowchart 800 in
10 Figure 8, is as follows:

$$\Phi_1 = 1;$$

$\Phi_{T+1} = (\Phi_T - 1 + (N/2 - \frac{1}{2})) \bmod N + 1$, where N is odd number of
phases

$$= (\Phi_T - 1 + (N/2 - 1)) \bmod N + 1, \text{ where } N \text{ is even number of}$$

15 phases and

$$N \bmod (N/2 - 1) \neq 0$$

Two phase assignments $(\Phi_{a,1}, \dots, \Phi_{a,N})$ and $(\Phi_{b,1}, \dots, \Phi_{b,N})$ are
equivalent

20 if $\Phi_{a,i} = (\Phi_{b,i} - 1 + p) \bmod N + 1$ for $i=1 \dots N$ and p is an arbitrary integer.

Examples of the above embodiment will be discussed in conjunction
with Figures 9A and 9B, where $N =$ the number of phases. The numbers
inside the circles denote the input terminals (terminal number) of the

multiphase transformer and the numbers outside the circles denote the assigned phases (phase number). Four examples are described below.

In Figure 9A, $N = 5$ phases. Phase 1 is assigned terminal 1.

The phase assigned to terminal 2 = $(1 - 1 + (5/2 - 1/2)) \bmod 5 + 1$

$$5 \quad = (2) \bmod 5 + 1$$

$$= 2 + 1$$

$$= 3$$

Thus, phase 3 is assigned to

terminal 2.

10

The phase assigned to terminal 3 = $(3 - 1 + (5/2 - 1/2)) \bmod 5 + 1$

$$= (4) \bmod 5 + 1$$

$$= 4 + 1$$

$$= 5$$

15 , Thus, phase 5 is assigned to

terminal 3.

In Figure 9B, $N = 12$ phases. Phase 1 is assigned to terminal 1.

The phase assigned to terminal 2 = $(1 - 1 + (12/2 - 1)) \bmod 12 + 1$

$$20 \quad = (5) \bmod 12 + 1$$

$$= 5 + 1$$

$$= 6$$

Thus, phase 6 is assigned to

terminal 2.

$$\begin{aligned} \text{The phase assigned to terminal 3} &= (6 - 1 + (12/2 - 1)) \bmod 12 + 1 \\ &= (10) \bmod 12 + 1 \\ &= 10 + 1 \\ 5 \quad &= 11 \end{aligned}$$

Thus, phase 11 is assigned to
terminal 3.

One skilled in the art having the benefit of this description will
10 appreciate how the embodiment above may be applied to the remaining
input terminals of Figures 9A and 9B. Also, from the above examples, it will
be appreciated how embodiments of the method may be applied to
multiphase transformers having various numbers of phases.

In one embodiment, the number of phases assigned to the
15 multiphase transformer in accordance with the above method is 16.

Analysis shows that the use of 16 phases in a multiphase transformer
having the cyclic cascade or modified cyclic cascade topology results in a
converter efficiency of approximately 90%.

Referring to Figure 9C, graph 950 illustrating the efficiency trend with
20 different numbers of phases in accordance with embodiments of the present
invention is shown. In graph 950, the vertical axis shows the efficiency of
the DC-DC converter and the horizontal axis shows the number of phases
N.

As shown in graph 950, the efficiency may increase with the number of phases N and may approach a maximum value of approximately 90% for N=16. An odd number of phases may provide a higher efficiency compared to embodiments with an even number of phases. Some even numbers of phases, such as, for example, 4, 6, 10, 14, and other numbers which may be a prime number multiplied by two, may conflict with the optimal phase assignment and may therefore result in lower efficiency.

It will be noted that DC-DC converters as described herein may be arrayed to deliver a higher total power to a larger load. In one embodiment, multiple DC-DC converters 500 designed for an output current of 5A each may have their voltage outputs coupled in parallel. For example, in a dual-core processor each core may require a supply current of 20A, and the cache memory and I/O (input/output) may consume a current of 5A each. To supply this processor with current, ten DC-DC converters 500 may be used: four converters connected in parallel to supply the first core, another four converters connected in parallel to supply the second core, one converter to supply the cache memory, and one converter to supply I/O.

In one embodiment, the converters may be arranged in regular arrays (e.g., 2x5). The output voltages delivered to the two cores, the cache, and the I/O may be all different so as to operate each of these components under optimal conditions and to conserve power. For example, an idling core may be supplied with a lower voltage to reduce the leakage power loss.

Furthermore, two or three of the four converters supplying an idling core may be turned off in order to improve the efficiency at light load. The

phase assignments between such converters may be optimized to minimize the input ripple current of each of the multiphase DC-DC converters and to minimize the residual output voltage ripple.

Referring to Figure 10, a multiphase DC-DC converter 1000 having a programmable capability is shown. Multiphase DC-DC converter 1000 includes a shuffle circuit 1002 coupled to multiphase transformer 102. Input voltage V_{IN} and phase assignments ($\Phi_1 - \Phi_4$) are applied to shuffle circuit 1002. A control input 1004 is also applied to shuffle circuit 1002.

In one embodiment, shuffle circuit 1002 is used during fabrication of multiphase DC-DC converter 1000 to appoint the phases as desired to multiphase transformer 102. In one embodiment, control input 1004 is used to blow fuses within shuffle circuit 1002 so that phase assignments ($\Phi_1 - \Phi_4$) are assigned to the voltage input terminals of the multiphase transformer as desired. In this particular embodiment, the phases are permanently assigned. Control input 1004 may be managed by a computer system, such as shown in Figure 11B.

In another embodiment, control input 1004 may be used to change phase assignments to multiphase transformer 102 using hardware logic in shuffle circuit 1002. Thus, the assignment of phases may be changed in a deployed system. In one embodiment, the control input may be changed using a Basic Input/Output System (BIOS) setup utility of a computer system, such as shown in Figure 11B.

Referring to Figure 11A, a system 1100 including multiphase DC-DC converter 100 is shown. In system 1100, the output voltage V_{OUT} of

multiphase DC-DC converter 100 is coupled to a consumer circuit 1104.

Consumer circuit 1104 may also be referred to as a load. In one embodiment, consumer circuit 1104 includes a processor.

In one embodiment of system 1100, multiphase DC-DC converter
5 100 is an integrated on-die device in a package, and consumer circuit 1104 is separately packaged. In one embodiment, converter 100 and consumer 1104 are mounted to the same printed circuit board and electrically coupled together.

In another embodiment of system 1100, multiphase DC-DC converter
10 100 and consumer circuit 1104 are packaged in the same chip package. In one embodiment, converter 100 and circuit 1104 are integrated on the same die. In another embodiment, converter 100 and circuit 1104 are integrated on separate dies. In this particular embodiment, converter 100 and circuit 1104 may be positioned side-by-side or stacked as in a multi-chip module.

15 Figure 11B is an illustration of a computer system 1150 on which embodiments of the present invention may be implemented. Computer system 1150 includes a processor 1152 and a memory 1154 coupled to a chipset 1158. Storage 1158, Non-Volatile Storage (NVS) 1156, network interface (I/F) 1162, and Input/Output (I/O) device 1164 may also be coupled
20 to chipset 1158. Embodiments of computer system 1150 include, but are not limited to, a desktop computer, a notebook computer, a server, a personal digital assistant, a network workstation, or the like. In one embodiment, computer system 1150 includes a multiphase DC-DC

converter as described herein to supply power to a consumer circuit of computer system 1150, such as processor 1152.

Processor 1152 may include, but is not limited to, an Intel Corporation x86, Pentium®, Xeon®, or Itanium® family processor, or the like. In one
5 embodiment, computer system 1150 may include multiple processors. In another embodiment, processor 1152 may include two or more processor cores.

Memory 1154 may include, but is not limited to, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM),
10 Synchronized Dynamic Random Access Memory (SDRAM), Rambus Dynamic Random Access Memory (RDRAM), or the like. In one embodiment, memory 1154 may include one or more memory units that do not have to be refreshed.

Chipset 1158 may include a memory controller, such as a Memory
15 Controller Hub (MCH), an input/output controller, such as an Input/Output Controller Hub (ICH), or the like. In an alternative embodiment, a memory controller for memory 1154 may reside in the same chip as processor 1152. Chipset 1158 may also include system clock support, power management support, audio support, graphics support, or the like. In one embodiment,
20 chipset 1158 is coupled to a board that includes sockets for processor 1152 and memory 1154.

Components of computer system 1150 may be connected by various interconnects. In one embodiment, an interconnect may be point-to-point between two components, while in other embodiments, an interconnect may

connect more than two components. Such interconnects may include a Peripheral Component Interconnect (PCI), such as PCI Express, a System Management bus (SMBUS), a Low Pin Count (LPC) bus, a Serial Peripheral Interface (SPI) bus, an Accelerated Graphics Port (AGP) interface, or the like. I/O device 1164 may include a keyboard, a mouse, a display, a printer, a scanner, or the like.

Computer system 1150 may interface to external systems through network interface 1162. Network interface 1162 may include, but is not limited to, a modem, a Network Interface Card (NIC), or other interfaces for coupling a computer system to other computer systems. A carrier wave signal 1168 may be received/transmitted by network interface 1162. In the embodiment illustrated in Figure 11B, carrier wave signal 1168 is used to interface computer system 1150 with a network 1166, such as a Local Area Network (LAN), a Wide Area Network (WAN), the Internet, or any combination thereof. In one embodiment, network 1166 is further coupled to a computer system 1172 by carrier wave signal 1170 such that computer system 1150 and computer system 1172 may communicate over network 1166.

Computer system 1150 also includes non-volatile storage 1156 on which firmware and/or data may be stored. Non-volatile storage devices include, but are not limited to, Read-Only Memory (ROM), Flash memory, Erasable Programmable Read Only Memory (EPROM), Electronically Erasable Programmable Read Only Memory (EEPROM), Non-Volatile Random Access Memory (NVRAM), or the like. Storage 1160 includes, but

is not limited to, a magnetic disk drive, a magnetic tape drive, an optical disk drive, or the like. It is appreciated that instructions executable by processor 1152 may reside in storage 1160, memory 1154, non-volatile storage 1156, or may be transmitted or received via network interface 1162.

5 It will be appreciated that in one embodiment, computer system 1150 may execute Operating System (OS) software. For example, one embodiment of the present invention utilizes Microsoft Windows® as the operating system for computer system 1150. Other operating systems that may also be used with computer system 1150 include, but are not limited to,
10 the Apple Macintosh operating system, the Linux operating system, the Unix operating system, or the like.

 For the purposes of the specification, a machine-accessible medium includes any mechanism that provides (i.e., stores and/or transmits) information in a form readable or accessible by a machine (e.g., a computer,
15 network device, personal digital assistant, manufacturing tool, any device with a set of one or more processors, etc.). For example, a machine-accessible medium includes, but is not limited to, recordable/non-recordable media (e.g., Read-Only Memory (ROM), Random Access Memory (RAM), magnetic disk storage media, optical storage media, a flash memory device,
20 etc.). In addition, a machine-accessible medium may include propagated signals such as electrical, optical, acoustical or other forms of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.).

 Various operations of embodiments of the present invention are described herein. These operations may be implemented by a machine

using a processor, an Application Specific Integrated Circuit (ASIC), a Field Programmable Gate Array (FPGA), or the like. The order in which some or all of the operations are described should not be construed as to imply that these operations are necessarily order dependent. Alternative ordering will
5 be appreciated by one skilled in the art having the benefit of this description. Further, it will be understood that not all operations are necessarily present in each embodiment of the invention.

The above description of illustrated embodiments of the invention, including what is described in the Abstract, is not intended to be exhaustive
10 or to limit the embodiments to the precise forms disclosed. While specific embodiments of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible, as those skilled in the relevant art will recognize. These modifications can be made to embodiments of the invention in light of the above detailed description.
15 The terms used in the following claims should not be construed to limit the invention to the specific embodiments disclosed in the specification. Rather, the following claims are to be construed in accordance with established doctrines of claim interpretation.

CLAIMS

What is claimed is:

1. A method, comprising:
 - providing a multiphase DC-DC converter including a multiphase transformer, the multiphase transformer including a plurality of input voltage terminals and transformer output voltage terminal, each input voltage terminal associated with a corresponding phase; and
 - assigning each phase to an input voltage terminal of the plurality of input voltage terminals to minimize a ripple current at the input voltage terminals of the multiphase transformer.

2. The method of claim 1 wherein assigning the phases includes assigning the phases non-sequentially to the plurality of input voltage terminals.

3. The method of claim 1 wherein the phases are assigned in accordance with the following:
 - a first phase Φ_1 is assigned to a first terminal T1 of the plurality of input voltage terminals;
 - if the number of phases N is odd, then

$$\Phi_{T+1} = (\Phi_T - 1 + (N/2 - \frac{1}{2})) \bmod N + 1,$$
 where T is the terminal number; and

if the number of phases N is even, then

$\Phi_{T+1} = (\Phi_T - 1 + (N/2 - 1)) \bmod N + 1$, where T is the terminal number.

4. The method of claim 1 wherein the multiphase transformer includes a two-phase transformer for each phase of the multiphase transformer, the two-phase transformers arranged in a cyclic cascade topology.

5. The method of claim 4 wherein each two-phase transformer includes coupled-inductors.

6. The method of claim 1 wherein the multiphase transformer includes a two-phase transformer for each phase of the multiphase transformer, the two-phase transformers arranged in a modified cyclic cascade topology.

7. The method of claim 6 wherein each two-phase transformer includes coupled-inductors.

8. The method of claim 1 wherein the multiphase transformer includes a two-phase transformer for each phase of the multiphase transformer, the two-phase transformers arranged in a mixed cyclic cascade topology.

9. The method of claim 8 wherein each two-phase transformer includes coupled-inductors.

10. A multiphase DC-DC converter, comprising:
a multiphase transformer;
a transformer output voltage terminal coupled to the multiphase transformer; and
a plurality of input voltage terminals coupled to the multiphase transformer, wherein a plurality of phases corresponding to a plurality of input voltages are assigned to the plurality of input voltage terminals, respectively, to minimize a ripple current at the input voltage terminals of the multiphase transformer.
11. The multiphase DC-DC converter of claim 10 wherein the multiphase transformer includes a two-phase transformer for each phase of the multiphase transformer, the two-phase transformers arranged in a cyclic cascade topology.
12. The multiphase DC-DC converter of claim 10 wherein the multiphase transformer includes a two-phase transformer for each phase of the multiphase transformer, the two-phase transformers arranged in a modified cyclic cascade topology.
13. The multiphase DC-DC converter of claim 10 wherein the multiphase transformer includes a two-phase transformer for each phase of the

multiphase transformer, the two-phase transformers arranged in a mixed cyclic cascade topology.

14. The multiphase DC-DC converter of claim 10, further comprising a shuffle circuit coupled between the plurality of input voltage terminals and corresponding bridges of the multiphase transformer to enable programmability of the assignment of phases to the multiphase transformer.

15. The multiphase DC-DC converter of claim 10 wherein an output voltage terminal of the multiphase DC-DC converter is coupled to a second output voltage terminal of a second multiphase DC-DC converter in parallel.

16. The multiphase DC-DC converter of claim 10 wherein the DC-DC converter is integrated on a semiconductor die.

17. A system, comprising:

a processor;

a multiphase DC-DC converter integrated on a semiconductor die to provide a supply voltage to the processor, the DC-DC converter including:

a multiphase transformer;

an transformer output voltage terminal coupled to the multiphase transformer; and

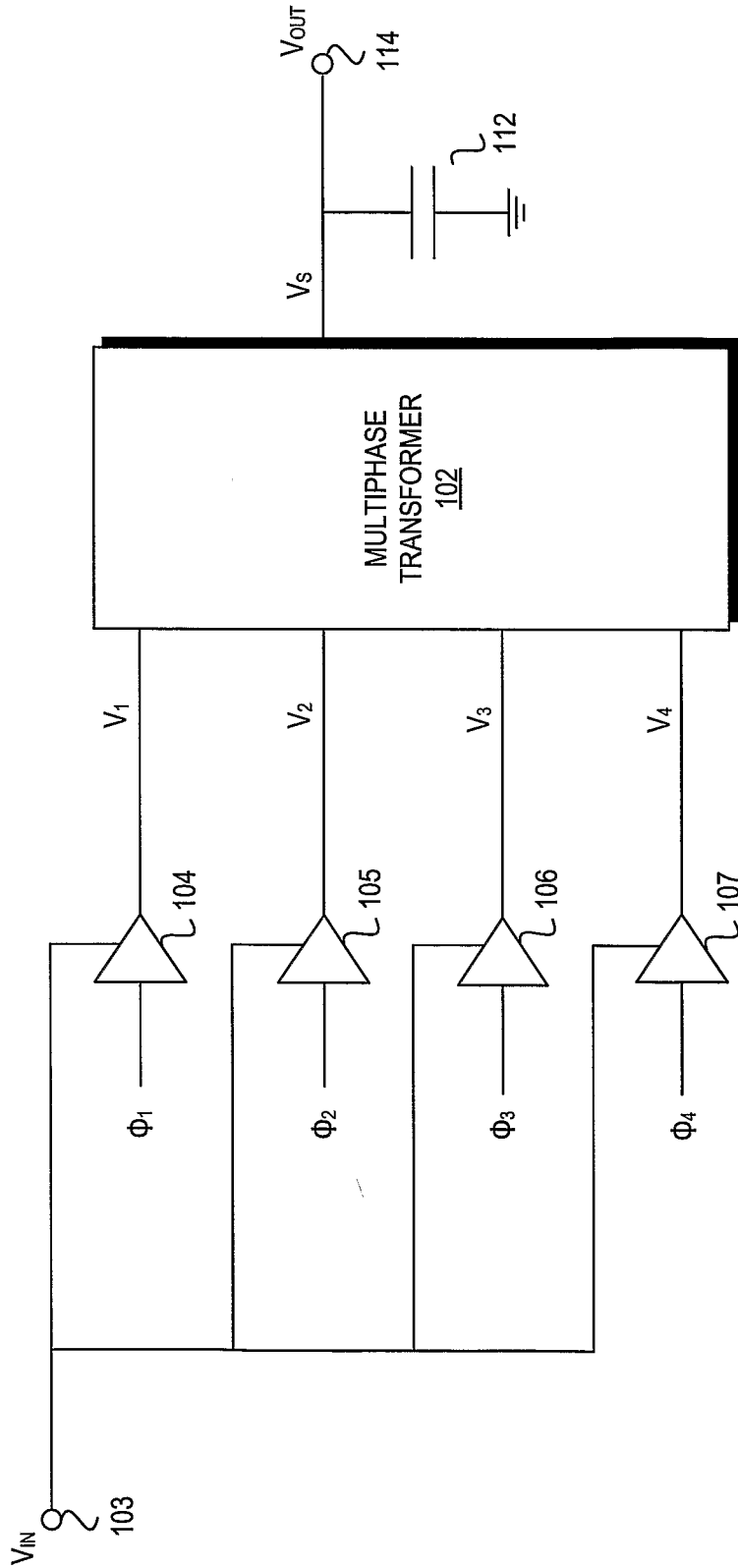
a plurality of input voltage terminals coupled to the multiphase transformer, wherein a plurality of phases corresponding to a plurality

of input voltages are applied to the plurality of input voltage terminals, respectively, to minimize a ripple current at the input voltage terminals of the multiphase transformer.

18. The system of claim 17 wherein the multiphase transformer includes a two-phase transformer for each phase of the multiphase transformer, the two-phase transformers arranged in one of a cyclic cascade topology, a modified cyclic cascade topology, or a mixed cyclic cascade topology.

19. The system of claim 17 wherein the processor and the multiphase DC-DC converter are packaged in the same package.

20. The system of claim 19 wherein the processor and the multiphase DC-DC converter are integrated on the same semiconductor die.



MULTIPHASE DC-DC
CONVERTER
100

FIG. 1A

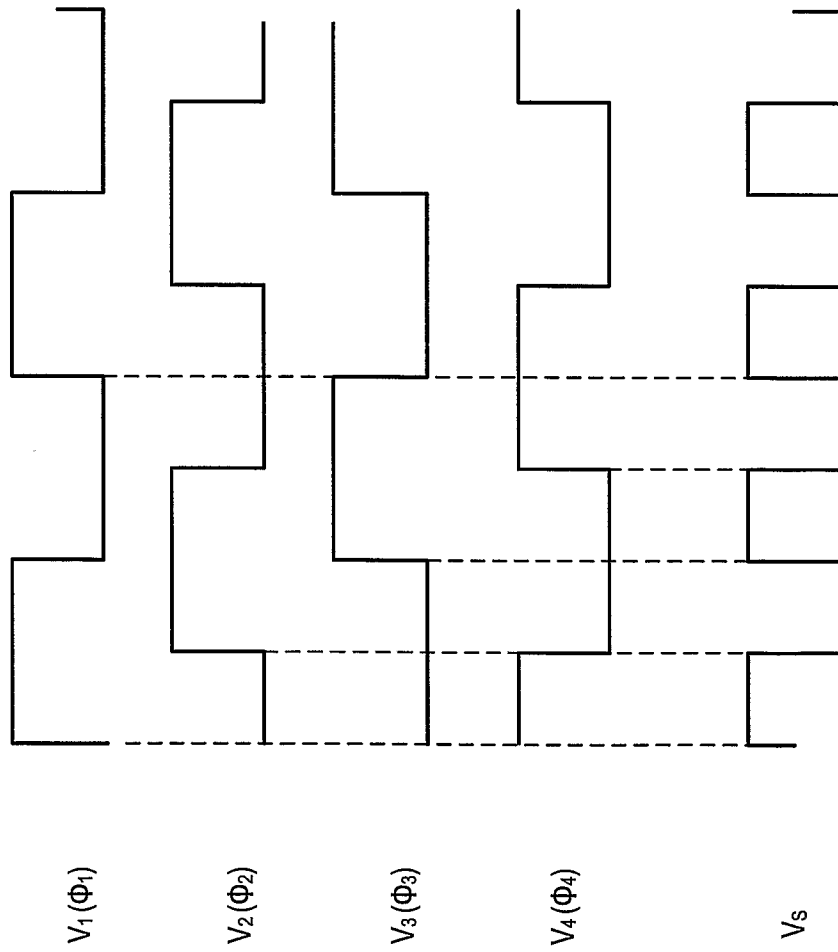
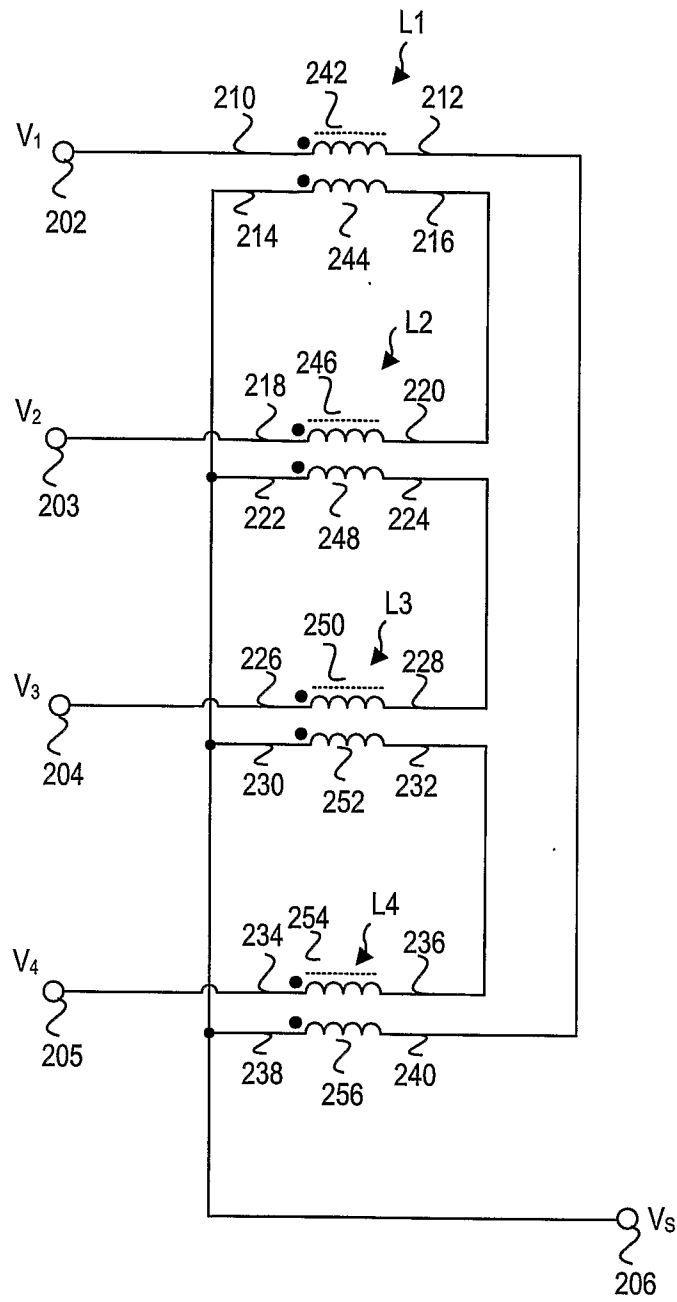
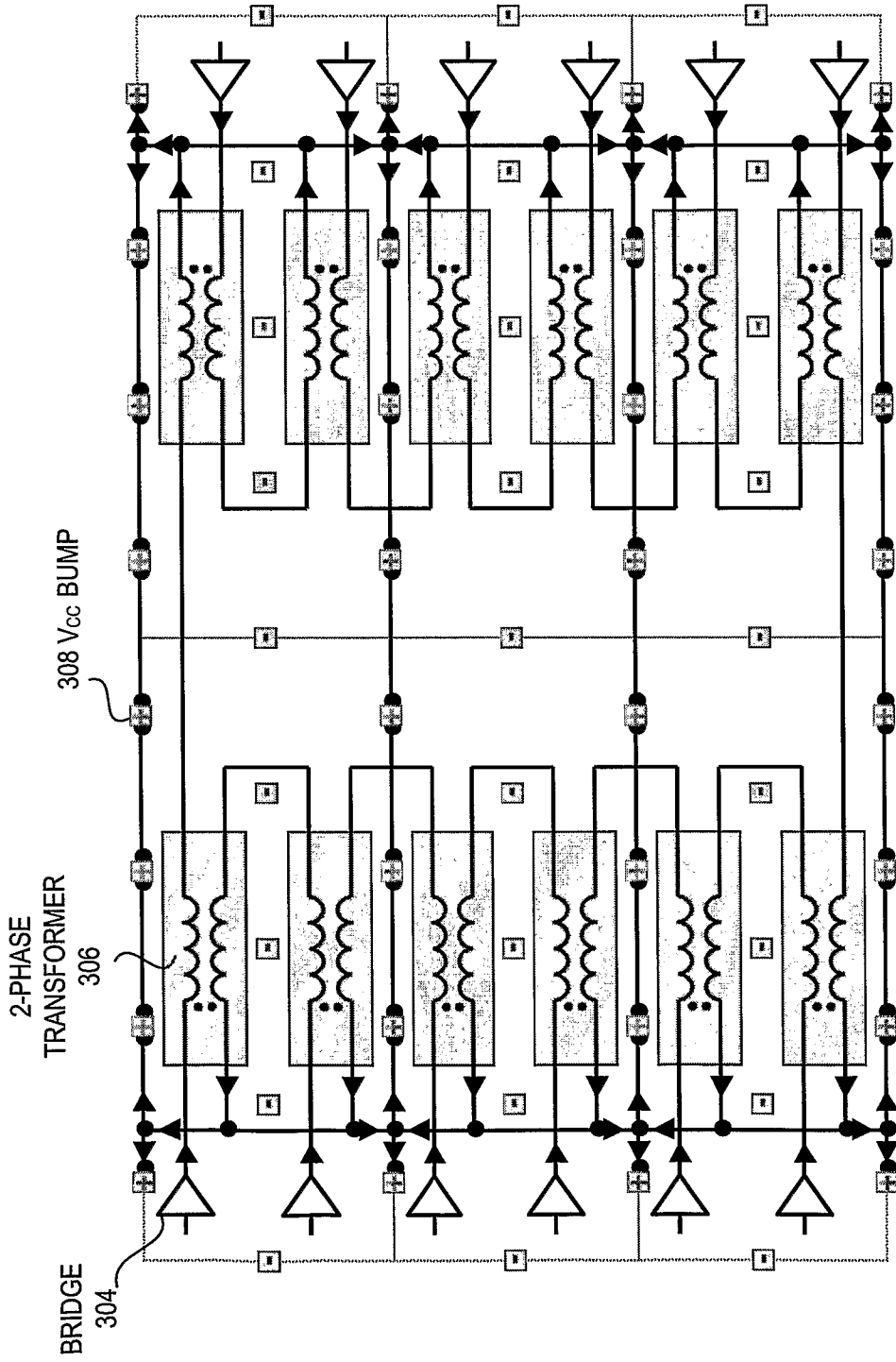


FIG. 1B



CYCLIC CASCADE
200

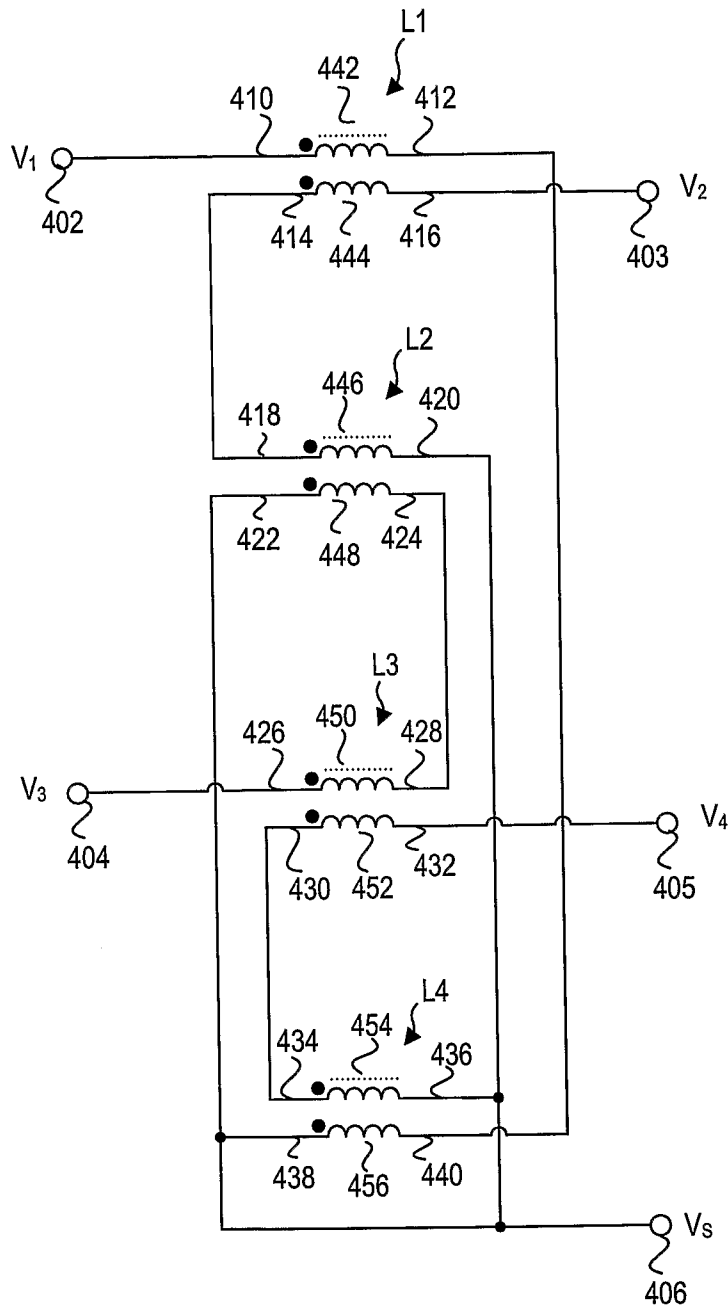
FIG. 2



CYCLIC CASCADE
300

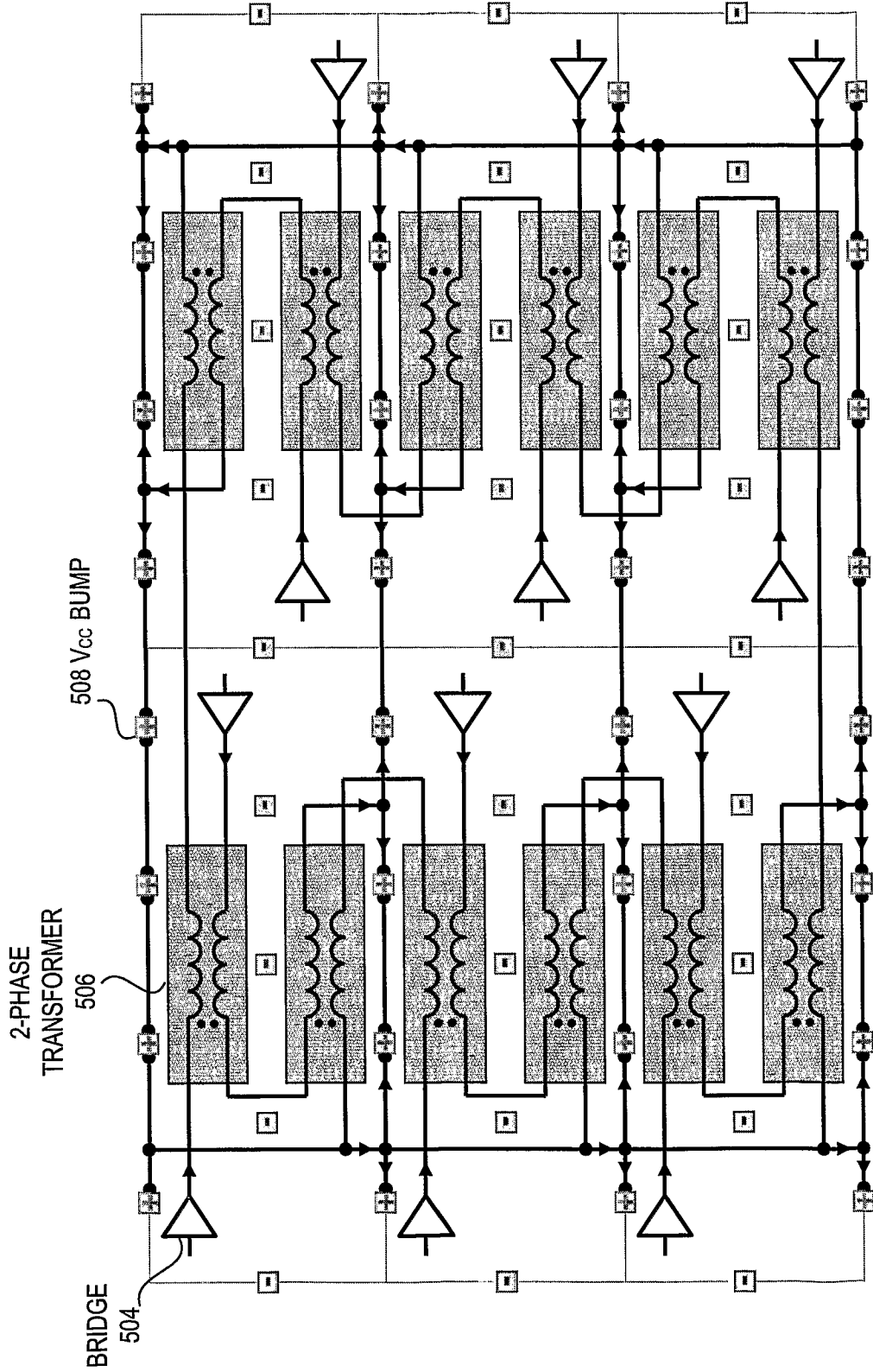
FIG. 3

5/14

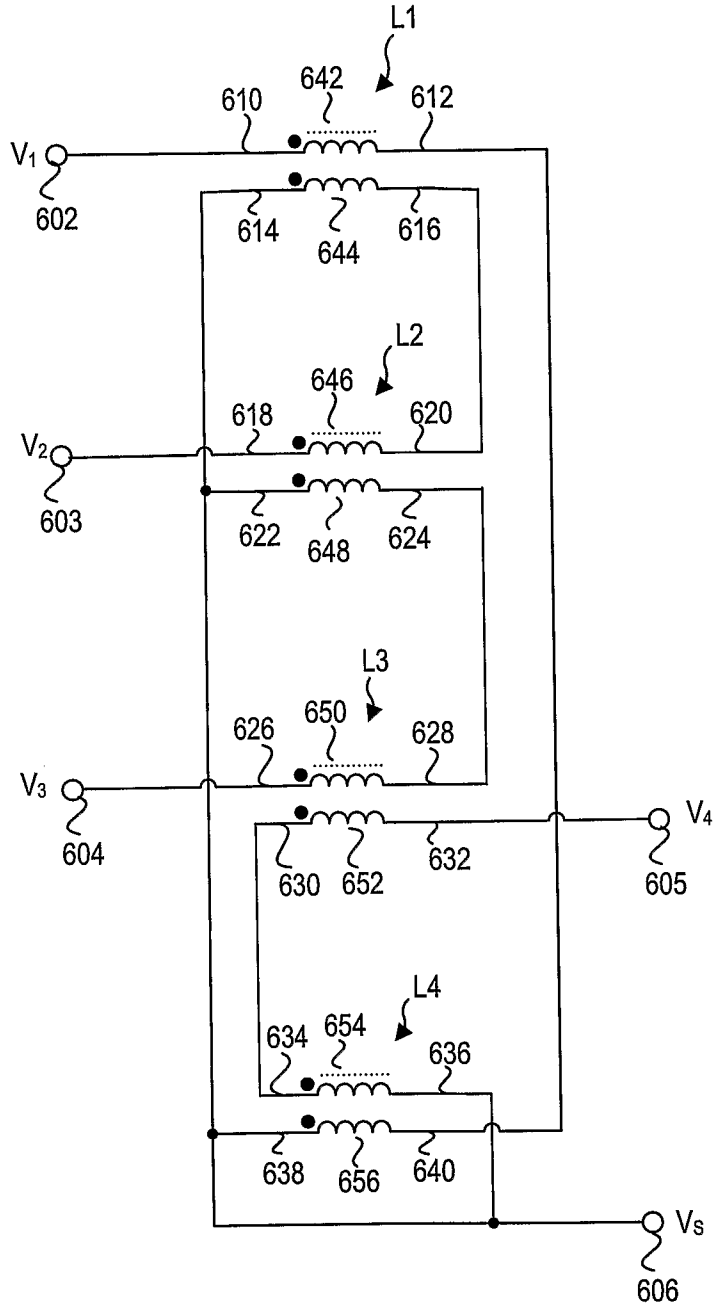


MODIFIED CYCLIC
CASCADE
400

FIG. 4

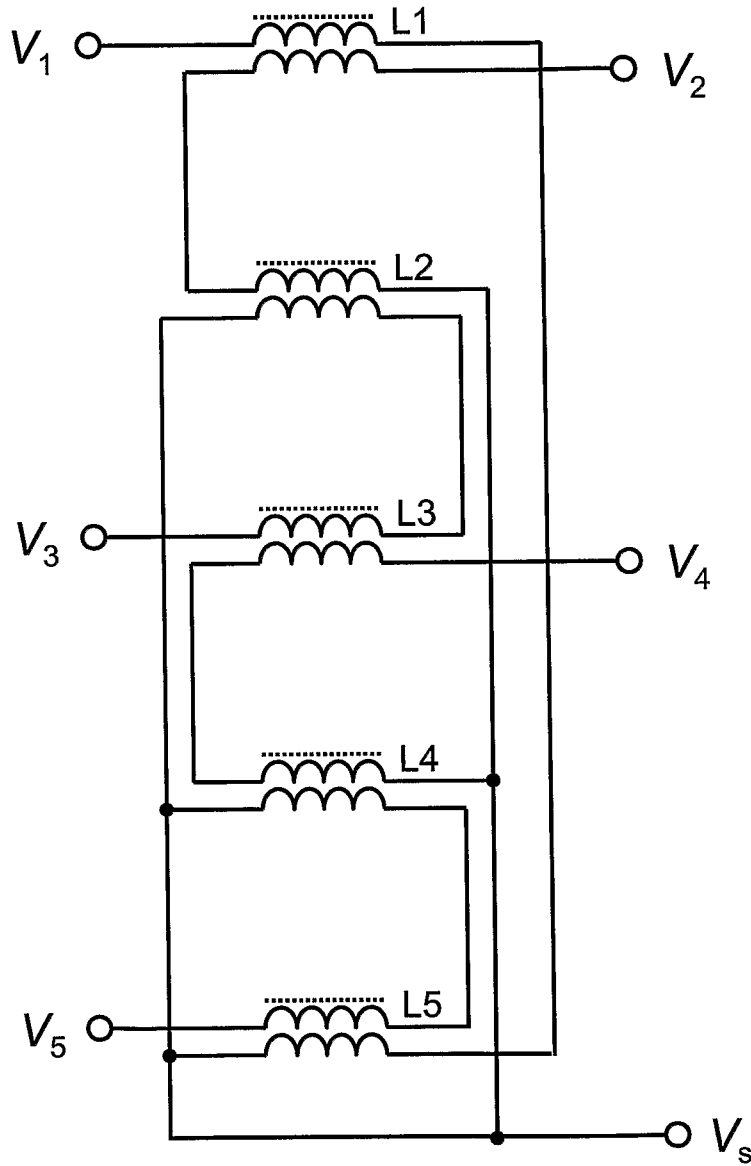


MODIFIED CYCLIC CASCADE
500
FIG. 5



MIXED CYCLIC
CASCADE
600

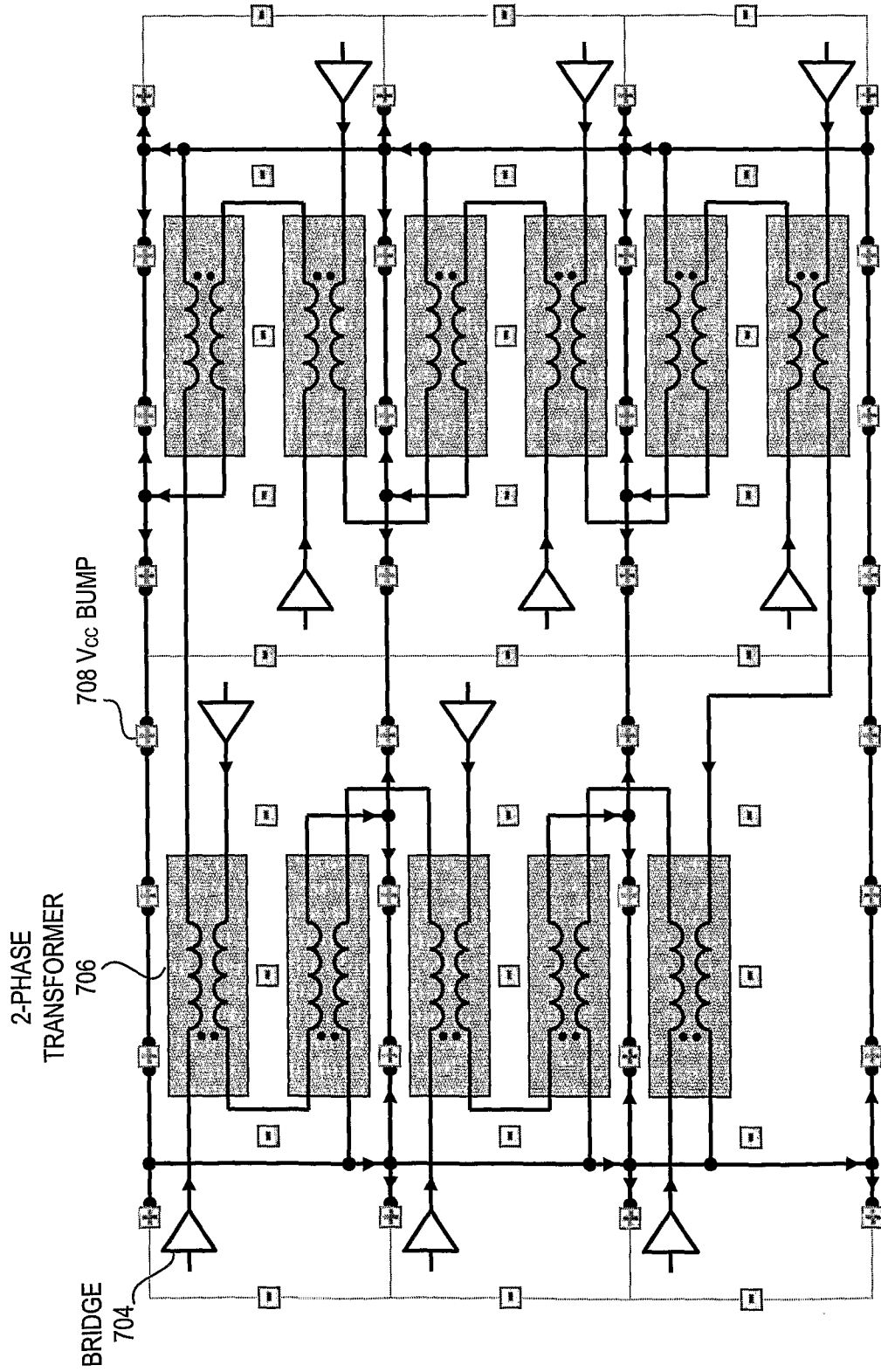
FIG. 6A



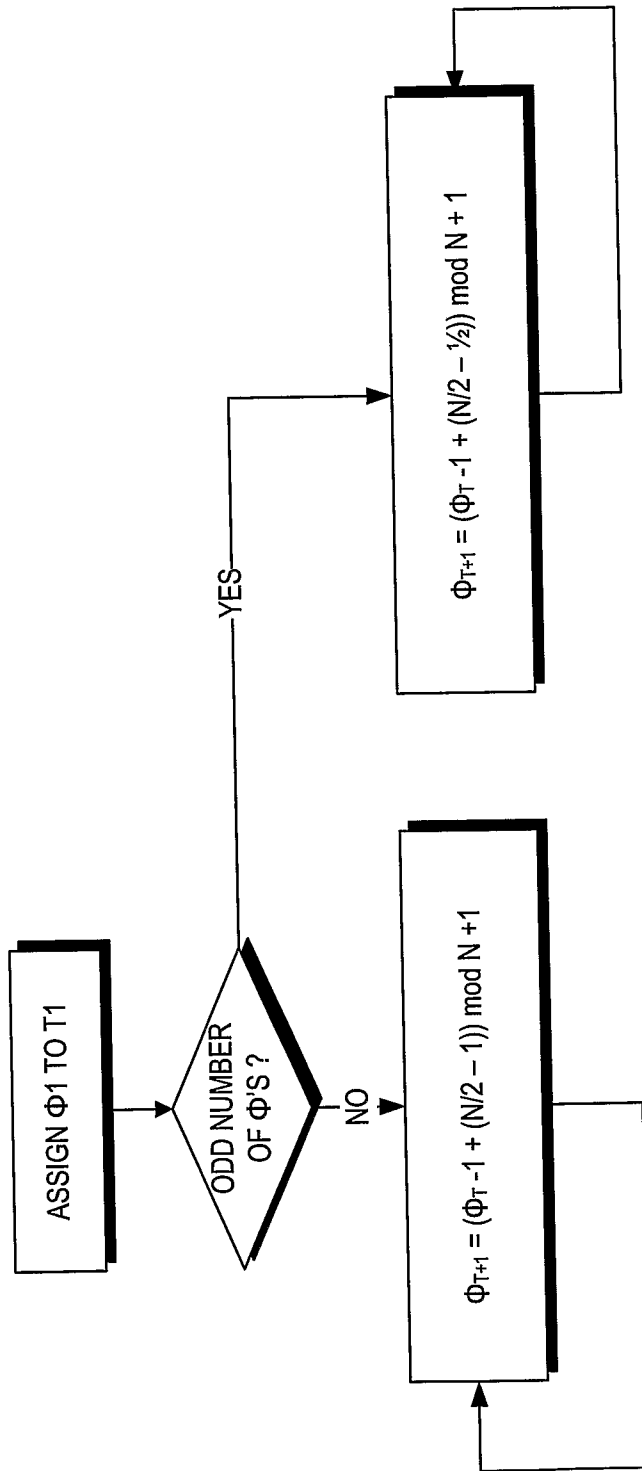
MIXED CYCLIC CASCADE
(5 PHASES)

650

FIG. 6B

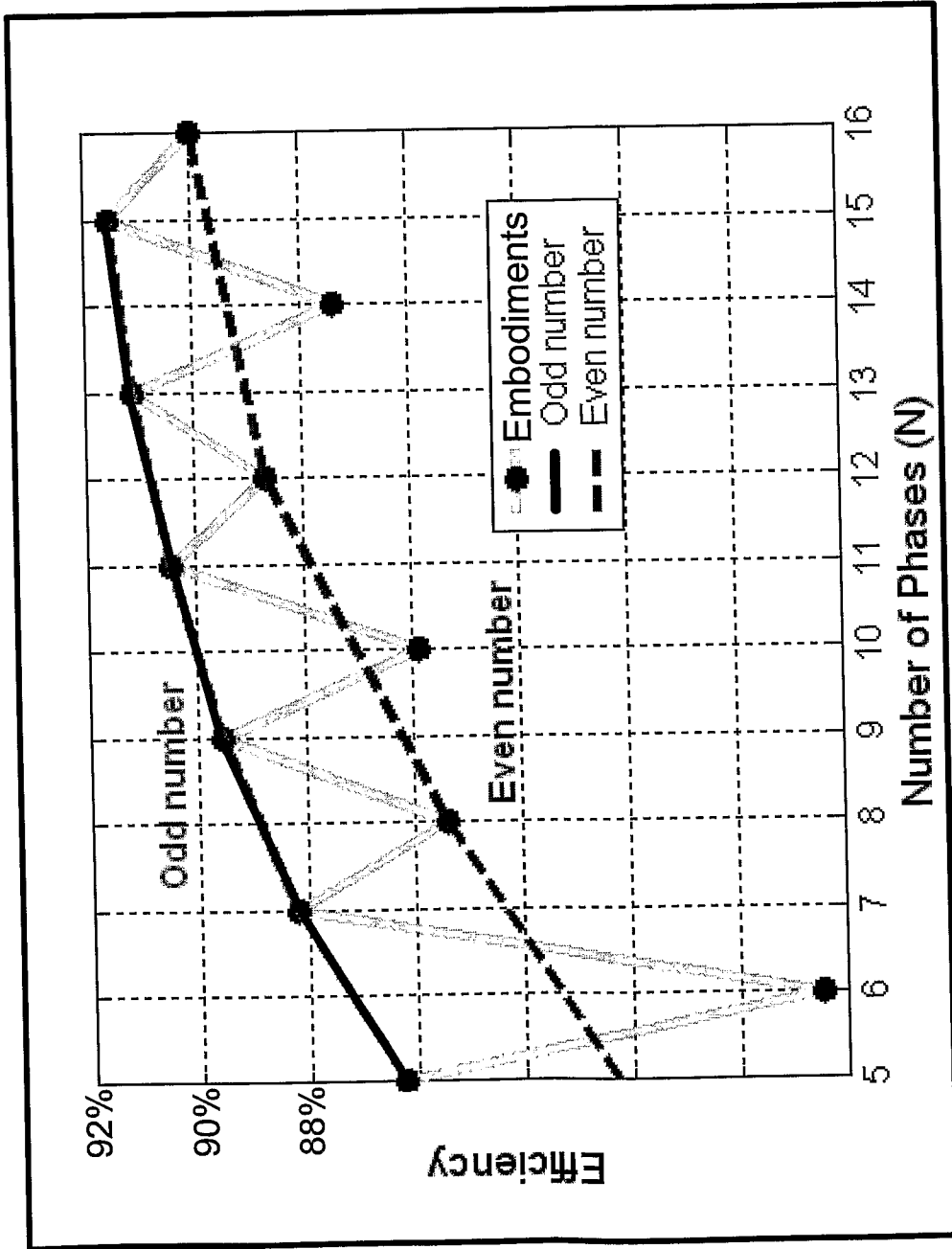


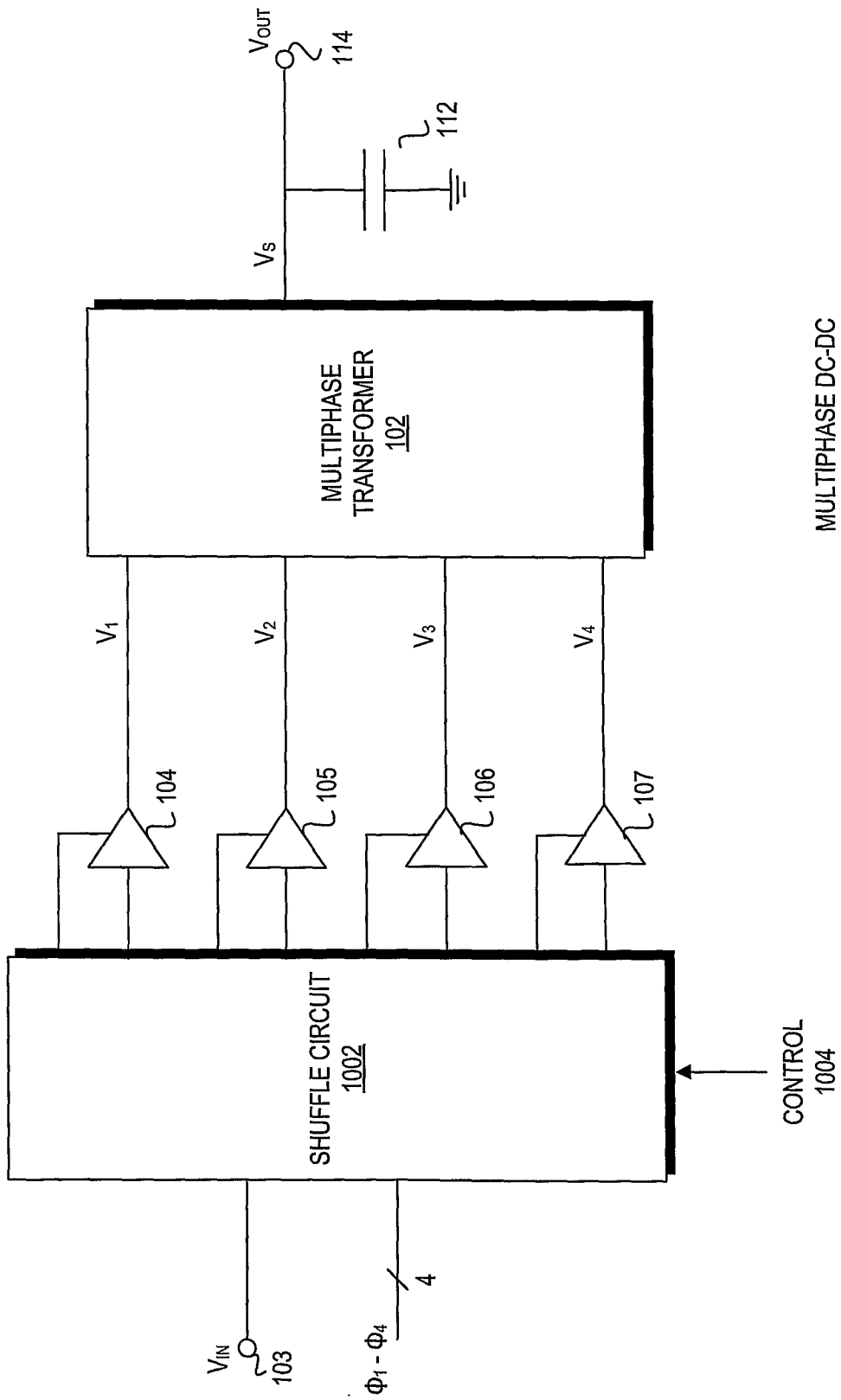
MIXED CYCLIC CASCADE
700
FIG. 7



800

FIG. 8





MULTIPHASE DC-DC
CONVERTER
1000
FIG. 10

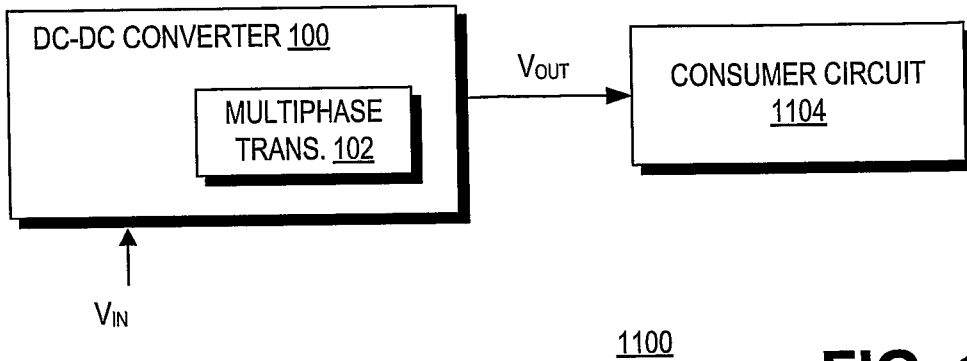


FIG. 11A

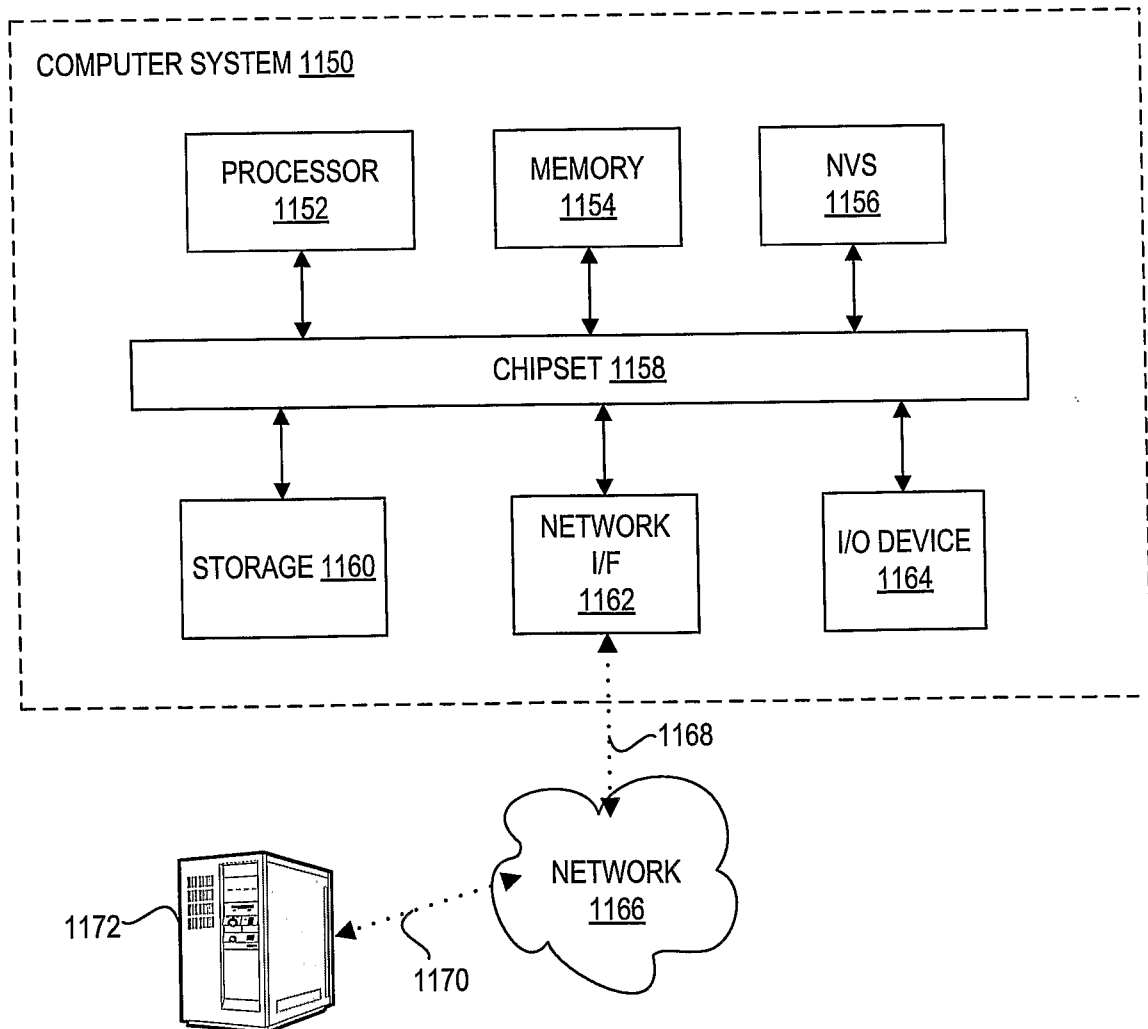


FIG. 11B

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/025712A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M3/22

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ZUMEL P ET AL: "Magnetic integration for interleaved converters" APEC 2003. 18TH. ANNUAL IEEE APPLIED POWER ELECTRONICS CONFERENCE AND EXPOSITION. MIAMI BEACH, FL, FEB. 9 - 13, 2003, ANNUAL APPLIED POWER ELECTRONICS CONFERENCE, NEW YORK, NY : IEEE, US, vol. VOL. 1 OF 2. CONF. 18, 9 February 2003 (2003-02-09), pages 1143-1149, XP010631656 ISBN: 0-7803-7768-0	1,5,7,9, 10,17
A	abstract page 1144, left-hand column figure 3 ----- -/--	3,14-16, 19,20

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents :

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- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- *Z* document member of the same patent family

Date of the actual completion of the international search

23 October 2006

Date of mailing of the international search report

03/11/2006

Name and mailing address of the ISA/

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Roider, Anton

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2006/025712

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 931 919 A (NGUYEN VIETSON M [US] ET AL) 5 June 1990 (1990-06-05)	1,2,4,6, 8,10-13, 17,18
A	column 2, lines 3-19 column 4, line 35 - column 6, line 12 figures 2-4	3,14-16, 19,20
X	----- US 5 070 440 A (WALKER LOREN H [US]) 3 December 1991 (1991-12-03) abstract column 3, lines 3-48 figure 1 -----	1,10,17

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No PCT/US2006/025712

Patent document cited in search report	Publication date	Publication date	Patent family member(s)	Publication date
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US 5070440	A	03-12-1991	DE 69116957 D1	21-03-1996
			DE 69116957 T2	26-09-1996
			EP 0473257 A2	04-03-1992
			JP 3238721 B2	17-12-2001
			JP 4229025 A	18-08-1992