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(54) Title: A MOST SIGNIFICANT BITS ANALOG TO DIGITAL CONVERTER, AND AN ANALOG TO DIGITAL CONVERTER INCLUDING A MOST SIGNIFICANT BITS ANALOG TO DIGITAL CONVERTER

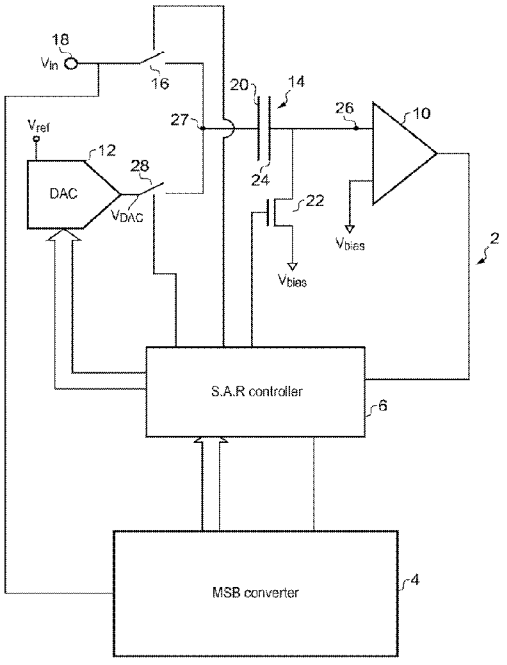


FIG. 1

(57) Abstract: A most significant bits analog to digital converter for determining a first P bits of an N bit analog to digital conversion, the most significant bits analog to digital converter comprising: a digital to analog converter a capacitive attenuator, and a switching arrangement for inhibiting action of the attenuator during sampling and enabling the attenuator during conversion.

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A MOST SIGNIFICANT BITS ANALOG TO DIGITAL CONVERTER, AND AN ANALOG TO DIGITAL CONVERTER INCLUDING A MOST SIGNIFICANT BITS ANALOG TO DIGITAL CONVERTER

FIELD OF THE INVENTION

[001] The present invention relates to analog to digital converters.

BACKGROUND OF THE INVENTION

[002] Analog to digital converters typically compare a voltage that has been sampled onto a sampling capacitor with a plurality of voltages to see which voltage best represents the sampled voltage. The plurality of voltages are often provided by a digital to analog converter, DAC. Various analog to digital converter technologies exist. In simplistic designs the voltage on the sampling capacitor is provided to one input of a comparator and the output of the digital to analog converter is provided to the other input of a comparator. The comparator output is supplied to a controller which determines which DAC voltage best approximates the input voltage.

[003] Low power devices are of increasing significance due to battery life and heat dissipation concerns. Generally power dissipation can be reduced by lowering supply voltage. Within an analog to digital converter different components may run at different supply voltages and the voltage at the comparator may be relatively low, say around 2 volts or so.

[004] Using low comparator voltages brings its own problems. The transistors formed within the comparator have parasitic components associated with them, and in particular the formation of switches connected to the input transistors gives rise to parasitic diodes at the comparator input, and if the input to the comparator falls outside the power supply range for the comparator then these parasitic diodes can switch on thereby allowing charge to be lost from the sampling capacitor. If this happens then the result of the analog to digital conversion process is unreliable. Also, voltage excursions outside of the supply rails may damage a device.

SUMMARY OF THE INVENTION

[005] According to a first aspect of the present invention there is provided a most significant bits analog to digital converter for determining a first P bits of an N bit analog to digital conversion, the most significant bits analog to digital converter comprising: a digital to analog converter, a capacitive attenuator, and a switching arrangement for inhibiting action of the attenuator during sampling and enabling the attenuator during conversion.

[006] It is thus possible to compensate for discrepancies between performance of the most significant bits (MSBs) analog to digital converter and a main analog to digital converter.

[007] As used herein the term "main analog to digital converter" will be used to refer to an analog to digital converter which is used to convert the majority of the bits in an analog to digital conversion.

[008] According to a second aspect of the present invention there is provided a method of performing an analog to digital conversion using a converter comprising a main analog to digital converter and a most significant bits analog to digital converter, and where the most significant bits analog to digital converter comprises a sampling capacitor, a digital to analog converter, a capacitive attenuator and a comparator, the capacitive attenuator acting to attenuate a signal received by the comparator, wherein a switching arrangement is provided in combination with the capacitive attenuator for inhibiting the action of the attenuator during sampling of a signal onto the sampling capacitor.

[009] Advantageously the sampling capacitor may be provided by capacitors within a switched capacitor array of the digital to analog converter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The present invention will further be described, by way of example only, with reference to the accompanying drawings, in which:

[0011] Figure 1 schematically illustrates an analog to digital converter constituting an embodiment of the present invention;

[0012] Figure 2 schematically illustrates the internal configuration of a prior art most significant bits analog to digital converter;

[0013] Figure 3 schematically illustrates the internal configuration of a most significant bits analog to digital converter constituting an embodiment of the present invention;

[0014] Figure 4 illustrates a switched capacitor dual ended most significant bit converter constituting a further embodiment of the present invention;

[0015] Figure 5 shows an alternative configuration of switches and a load or attenuation capacitor: and

[0016] Figure 6 shows a further embodiment of the invention

DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

[0017] Figure 1 schematically illustrates an analog to digital converter constituting an embodiment of the present invention. The analog to digital converter comprises a main analog to digital converter generally designated 2, a most significant bits, MSB, converter 4, and a successive approximation routine, SAR, controller 6. Advantageously the main analog to digital converter includes redundancy so to be able to recover from an incorrectly kept bit, if for example, there is a slight difference between the decision thresholds for the main and MSB converters. The use of redundant bits is discussed in greater detail in US 6 828 927 , which is incorporated by reference, and more particularly to column 6 lines 30 to 41 and column 7 line 20 to column 9 line 38.

[0018] An input 18 is connected to the MSB converter 4 and is selectively connectable to an intermediate node 27 of the main converter 2 via an electronically controlled switch 16. Similarly a digital to analog converter, DAC, 12 can be connected to the intermediate node via a switch 28. A sampling capacitor 14 has a first plate 20 connected to the intermediate node 27 and a second plate 24 connected to an output

node 26. A first input of a comparator 10 is connected to the output node 26, and a second input is connected to a bias voltage, Vbias, provided by a suitable voltage generator or a ground connection if Vbias is zero volts. A second electronically controlled switch 22 extends between the second plate 24 of the capacitor 14 and the bias voltage, Vbias. As will be discussed later the sampling capacitor 14 may comprise a plurality of capacitors within the DAC.

[0019] The SAR controller 6 is responsive to the comparator 10 within the main converter 2.

[0020] The SAR controller 6 controls the digital to analog converter, DAC, 12. In use the SAR controller selectively sets the bits (or bit weights) within the DAC to trial the contribution of the bits in sequence in conjunction with the combination of any previously kept bits, as is known to the person skilled in the art. The output of the DAC 12 is compared with a voltage sampled onto the sampling capacitor 14. This comparison is done, in this example, by summing the output of the DAC 12 with the voltage on the capacitor 14, and comparing the result with the voltage Vbias.

[0021] It is worthwhile considering the voltage sampling and comparison processes in detail at this time. At the start of sampling, switch 16 is closed, thereby allowing the voltage at an input terminal 18 to be applied to the first plate 20 of the sampling capacitor 14. The switch 16 is formed by a field effect transistor. At or about the same time the second switch, formed by transistor 22, is closed such that a second plate 24 of the capacitor 14 is connected to Vbias.

[0022] During sampling the sampling capacitor 14 is in series with switches 16 and 22. In practice switch 16 typically has a significantly lower resistance than switch 22 and so for this discussion its impedence is ignored. The impedance of the sampling capacitor 14 is frequency dependent whilst that of switch 22 is frequency independent (assuming no parasitic capacitance). For a sinusoidal input the magnitude of the impedance Zc of the sampling capacitor 14 is given by

[0023] $Zc = 1/(2.\pi.F.C)$

[0024] Where

F is the input frequency in Hertz, and

C is the capacitance of the sampling capacitor

[0025] As the frequency term F is in the denominator, Zc decreases with input frequency while the impedance of switch 22 remains fixed. As a result, more of the input signal appears across switch 22 at higher input frequencies.

[0026] The magnitude of the voltage, Ve, across the switch 22 for a sinusoidal input is given by

$$Ve = 1/(1 + 1/(2.\pi.F.R.C)^2)^{0.5}$$

[0027] Where

R is the resistance of switch 22, and

C is the capacitance of the sampling capacitor 14

[0028] Thus the voltage across the sampling capacitor at any instant is reduced from Vin to Vin-Ve.

[0029] We will come back to this later, but at the moment we will assume that a direct current signal is being sampled and that the sampling period is sufficiently long for Ve to be zero.

[0030] At the end of the sampling period switch 22 is made high impedance, and shortly after that switch 16 is also made high impedance. The voltage Vin-Vbias has been stored on the sampling capacitor 14.

[0031] At this point we have no idea what the value of Vin is. It is however worth noting that the voltage at plate 24 of the capacitor 14 is Vin-Vbias less than the voltage at plate 20. Consequently, if plate 20 was connected to ground then the voltage at a

first input 26 of the comparator 10 would be -(Vin-Vbias) which would be -Vin if Vbias = 0.

[0032] In converters not having an MSB converter 4, the SAR controller 6 uses the DAC 12 of the main converter to test all of the bits required to complete the analog to digital conversion.

[0033] This would mean setting the most significant bit of the DAC 12 whilst leaving all other bits unset. Thus, if the reference voltage to the DAC 12 is Vref, then the output is set to Vref/2.

[0034] Consequently the voltage of the input 26 to the comparator 10 is

$$(Vref/2)-Vin+Vbias$$

[0035] If, for simplicity, we set Vbias=0, then we can identify an input voltage, Vmsb, that equals the threshold voltage for the first bit trial,

$$Vmsb = Vref/2$$

[0036] The comparator 10 then compares the voltage with Vbias, in effect working out whether Vref/2 is greater than Vin or less than Vin. If Vin is greater than Vref/2 then the first bit is kept, otherwise it is discarded. The SAR controller then asserts the next bit so that next word being tested is 11000... if the first bit was kept or 01000... if the first bit was discarded.

[0037] This process is repeated for each bit from the most significant bit ,MSB, to the least significant bit, LSB, in sequence thereby achieving the analog to digital conversion.

[0038] The voltage at the input of the comparator 10 during a bit trial is Vbias-Vin+Vdac, where Vdac is the output voltage of the digital to analog converter 12. During a successive approximation conversion Vdac converges with Vin, so by the end of the trial the voltage at the input to the comparator 10 is very close to Vbias.

[0039] If, for the purposes of discussion we allow Ve to be non-zero then we see that the value for Vmsb changes to

$$Vmsb = (Vref/2) + Ve$$

[0040] Returning to considering the operation of the ADC, it can be seen that large voltage excursions at the output node 26, and consequently at the input of the comparator 10, only exist for the first one or two bit trials.

[0041] If the first few bits could be determined then the comparator 10 could be designed to work at a lower supply voltage resulting in lower power consumption. The lower supply voltage also allows the use of faster, lower geometry devices giving further power and speed benefits.

[0042] One way to achieve these objectives is to provide a MSB converter 4. Figure 2 shows the structure of an MSB converter constituting an embodiment of the invention in greater detail.

[0043] The topology is similar to that of the main converter, and like parts are indicated by numerals 100 greater than used in Figure 1. The DAC 112 is much simplified and is configured to only test the first P bits (P typically =1, 2 or 3) of the N bit conversion. N is typically 14, 16 or 18.

[0044] The sampling capacitor 114, which can be regarded as a first capacitor, is associated with a second capacitor 150 so as to form a capacitor voltage divider, i.e. a capacitive attenuator. The second capacitor 150 has one plate connected to the plate 124 of the first capacitor 114. In some prior art MSB converters the bottom plate 152 of the second capacitor 150 is directly connected to Vbias, in others the second capacitor is provided as a parasitic component.

[0045] The bandwidths of the main and MSB analog to digital converters are matched. This is assumed in prior art designs to be sufficient to ensure proper operation.

[0046] However the inventor has realised that contrary to accepted wisdom the operation of the MSB converter 4 is subject to error as the input bandwidth increases.

[0047] Although the signal sampled on to the sampling capacitors 14 and 114 is acceptably similar in both the MSB converter 4 and the main converter 2, the effect of the capacitor attenuator is to introduce an error between these two converters such that the MSB decisions determined by the MSB converter when applied to the main converter can result in unacceptable errors.

[0048] As noted before. the affect of a high input frequency signal during acquisition is to impose a signal Ve on node 126 (representing the output of the attenuator and input to the comparator) which is proportional to the derivative of the input signal. Directly after sampling, plate 120 of the first capacitor 114 (sampling capacitor) is at Vin whilst it other terminal 124 is at Ve.

[0049] To test, for example, the MSB decision the DAC output would be set to Vref/2 and switch 128 would be closed. The voltage on the comparator input Vcomp is , assuming Vbias=0, given by

$$Vcomp = Ve + [(Vref/2 - Vin)*C1/(C1+C2)]$$

[0050] That is, the comparator input voltage is equal to Ve plus the change in the voltage on node 27 between sampling and when set to Vref/2, that is [(Vref/2) - Vin] attenuated by the capacitor attenuator formed by first capacitor 114 having a capacitance C1 and the second capacitor 150 having capacitance C2. The transfer function between nodes 127 and 126 for this capacitive divider can be expressed as [C1/(C1+C2)].

[0051] Rearranging this equation and setting the voltage at the input to the comparator to zero (assuming Vbias=0) we can see what input voltage Vin corresponds to the MSB threshold voltage Vmsb:

$$Vmsb = Vref/2+(Ve*(C1+C2)/C1)$$

[0052] This equation also applies to the main converter. However, in the main converter C2 is not present and hence its value in the above equation is zero. Clearly since in one case C2 has a significant value, it can be as large as or greater than C1, and in the main converter it is zero, Vmsb can be significantly different for the two converters. Note that in the case of a DC or a slowly moving input signal Ve is zero or close to zero in which case Vmsb will be the same (or very nearly the same) for both the main DAC and MSB DAC. It is therefore the existence of a significant Ve, due to a moving input voltage, plus the fixed attenuating capacitor C2, that gives rise to the error.

[0053] In an embodiment of the invention, shown in Figure 3, the prior art arrangement of Figure 2 is modified by the inclusion of a first additional switch 160 interposed between terminal 152 of the second capacitor 150 and Vbias, and a second additional switch 162 across the second capacitor 150.

[0054] The switches are controlled by the SAR controller 6 (or some other controller) such that during acquisition switch 162 is closed (low impedance) and switch 160 is open. The second capacitor 150 does not therefore present a load to the MSB converter's input sampling network during the sampling phase. With a time varying input signal there will be a voltage Ve on node 126 and the same voltage on the equivalent node 26 in the main converter.

[0055] Directly after sampling both switches 122 and 116 are turned off. Consequently both terminals of the second capacitor 150 are at Ve. Switch 162 is then opened and switch 160 is closed. Node 127 is floating. The affect of closing switch 160 is to pull nodes 126 and the bottom plate 152 of the second capacitor 150 to Vbias, which may be zero Volts (Vbias =0) and node 127 is pulled to Vin – Ve.

[0056] On closing switch 128 the output of the DAC 112 is provided to the circuit and this gives rise to a comparator input voltage Vcomp for the MSB bit decision given by

$$Vcomp = (Vref/2 - (Vin - Ve)) * C1/(C1 + C2)$$

[0057] Again, by setting Vcomp to zero (assuming Vbias=0) allows us to determine what input voltage corresponds to the MSB voltage (Vin=Vmsb):

$$0 = (Vref/2 - (Vmsb - Ve)) * C1/(C1 + C2)$$

[0058] By multiplying both sides by (C1+C2)/C1 we get

$$0 = Vref/2-(Vmsb-Ve)$$

[0059] Then making Vmsb the subject, we see that

$$Vmsb = Vref/2 + Ve$$

[0060] So with this circuit the input voltage corresponding to the MSB threshold is independent of both C1 and C2 and so the MSB converter and main converter can be expected to have the same decision threshold Vmsb.

[0061] Thus the errors in the MSB converter due to high frequency components in a signal can be made to scale more closely with the main DAC, even though the MSB converter includes a capacitor based attenuator so as to avoid the risk of driving an input signal to the comparator out of range.

[0062] The DACs 12 and 112 can be single ended or dual ended. The converters can be fabricated as switched capacitor devices, in which case the capacitors of the DACs 12, 112 can also function as the sampling capacitors. In such an arrangement the attenuation circuit amounts to selectively connecting and disconnecting a load capacitor to the signal path extending from the DAC to the associated comparator.

[0063] Furthermore, as the MSB DAC is only required to provide output signals for the first one, two or three bit trials it can be formed from capacitors of the same size as one another, and hence can be formed of a "unit" sized capacitor, thereby allowing the MSB DAC to be physically small.

[0064] Figure 4 shows a MSB converter comprising two channels so as to act as a differential converter. For simplicity only the "negative" channel will be described in detail.

[0065] Given the DAC 200 is only required, in this example, to output 4 voltage levels corresponding to 0, 0.25, 0.5, 0.75 Vmax then it can be fabricated from four equal sized capacitors C1' to C4'. Each has a "top plate" connected to an output 210 of DAC 200. Each bottom plate is selectively connectable via associated switches to Vin- to sample the signal, or Vref+ or Vref- during conversion. As the switches are implemented as three transistors we also have a "not connected" condition available.

[0066] The capacitors in the positive channel DAC 202 are similarly associated with switches to connect them to Vin +, Vref+ and Vref-. The outputs 210 and 212 of the DACs are connected to respective inputs of a comparator 214.

[0067] Attenuation or load capacitors for use in the capacitive attenuator are provided as capacitors 220 and 222 in series connection between lines 210 and 212 with a series switch 224 provided to isolate them from one another. Each capacitor 220 and 222 has a respective shorting switch.

[0068] Thus as before each attenuation capacitor can effectively be disconnected or removed during sampling and inserted or connected during conversion.

[0069] For completeness, the operation of the "negative" channel will be briefly considered. To sample the input C1' to C4' are connected to Vin- and the switch 122' is closed. After sampling has been completed (122' now open) the first bit trial may be set up by connecting C1' and C2' to Vref+ ; and C3' and C4' to Vref-. The second bit trial will have 3 out of 4 of capacitors C1' to C4' connected to Vref+ or Vref- (as appropriate and determined by the MSB trial) and the other capacitor connected to the other one of Vref+ and Vref-.

[0070] In use, the MSB converter can identify the correct status for the first one, two (in this example) or even three bits of the conversion whilst the main converter is idle. The values of the most significant bits can then be passed via the controller 6 to the

main converter 2 such that the voltage swings at the input to the comparator 10 are always modest or small for the main converter. This means that the comparator 10 can be optimised for use over a small and known voltage input range (typically centred around the middle of the supply voltage).

[0071] In testing , this arrangement has enabled the input frequency of an analog to digital converter to be extended from 5MHz to 30MHz for the same accuracy and resolution.

[0072] Other topologies are available. Thus Figure 5 shows the load capacitor 150 and the series switch 160 reversed in order.

[0073] Figure 6 shows an alternative configuration for the dual ended arrangement of Figure 4 where a single load capacitor is placed between series connected switches. Capacitors 114 and 114' may be instantiated by C1-C4 and C1'- C4' (or similar) as shown in Figure 4.

[0074] It is thus possible to provide an improved analog to digital converter.

CLAIMS

1. A most significant bits analog to digital converter for determining a first P bits of an N bit analog to digital conversion, the most significant bits analog to digital converter comprising:

a digital to analog converter

a capacitive attenuator, and a switching arrangement for inhibiting action of the attenuator during sampling and enabling the attenuator during conversion.

2. A most significant bits analog to digital converter as claimed in claim 1, in which the capacitive attenuator comprises a load capacitor in series with a switch for selectively enabling charge flow via the capacitor during conversion.

3. A most significant bits analog to digital converter as claimed in claim 2, in which the load capacitor is connected between an output node and a bias voltage.

4. A most significant bits analog to digital converter as claimed in claim 2 in which the analog to digital converter is a dual ended converter comprising first and second digital to analog converters having respective capacitive attenuators, and the load capacitors are placed in series connection or each connected to a bias voltage during conversion, or a load capacitor may be shared between the first and second digital to analog converters

5. A most significant bits analog to digital as claimed in claim 2, further comprising a shorting switch in parallel with the load capacitor for providing a low impedance path to discharge the load capacitor during sampling.

6. A most significant bits analog to digital converter as claimed in claim 5, in which the shorting switch is placed in a high impedance states during conversion.

7. A most significant bits analog to digital converter as claimed in claim 1, in which the capacitive attenuator comprises first and second capacitors, with a first capacitor extending between an input of the attenuator and an output of the attenuator, and a second capacitor selectively connectable between the output of the

attenuator and a further node, the second capacitor being disconnected from one of the output and the further node during sampling of a signal to be converted, and reconnected while the signal is being converted.

8. A most significant bits analog to digital converter as claimed in claim 7, in which the first capacitor acts as a sampling capacitor.

9. A most significant bits analog to digital converter as claimed in claim 2, in which the digital to analog converter comprises a switched capacitor array, and the capacitors of the array cooperate with the load capacitor to form the capacitive attenuator.

10. An analog to digital converter comprising a combination of a main converter and a most significant bits converter as claimed in claim 1, wherein, is use, the most significant bits converter is used to trial the first P bits, and the result is then passed to the main converter which has its first P bits set in accordance with the values determined by the most significant bits converter.

11. An analog to digital converter as claimed in claim 10, where the main converter has redundancy

12. A method of performing an analog to digital conversion using a converter comprising a main analog to digital converter and a most significant bits analog to digital converter, and where the most significant bits analog to digital converter comprises a sampling capacitor, a digital to analog converter, a capacitive attenuator and a comparator, the capacitive attenuator acting to attenuate a signal received by the comparator, wherein a switching arrangement is provided in combination with the capacitive attenuator for inhibiting the action of the attenuator during sampling of a signal onto the sampling capacitor.

13. A method as claimed in claim 12, in which the first P bits of the analog to digital conversion are performed by the most significant bits analog to digital converter, and the result passed to the main converter.

14. A method as claimed in claim 12, in which during conversion a load capacitor is selectively coupled to the input of the comparator so as to cooperate with the sampling capacitor to form a capacitive voltage divider.

15. A method as claimed in claim 14, in which the digital to analog converter comprises a plurality of capacitors having switches associated therewith such the respective first terminals of the capacitors can be selectively connected to a first reference voltage or a second reference voltage, and second terminals of the capacitors are connected to an output node of the digital to analog converter, and wherein a signal to be converted can also be sampled onto at least one of the capacitors.

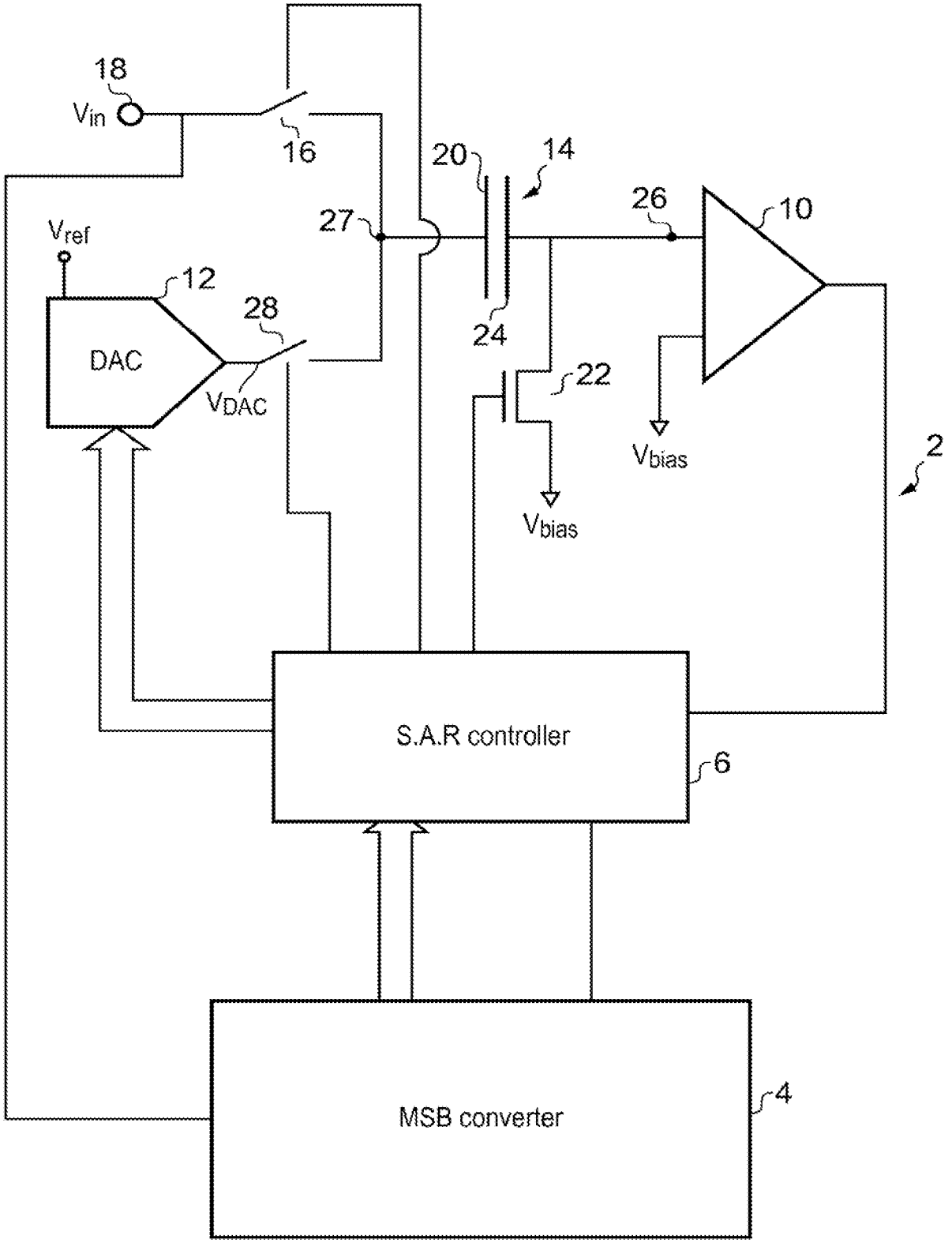

18
Vin
16
20
14
27
26
10
Vref
12
28
DAC
VDAC
24
22
Vbias
Vbias
2
S.A.R controller
6
MSB converter
4

FIG. 1

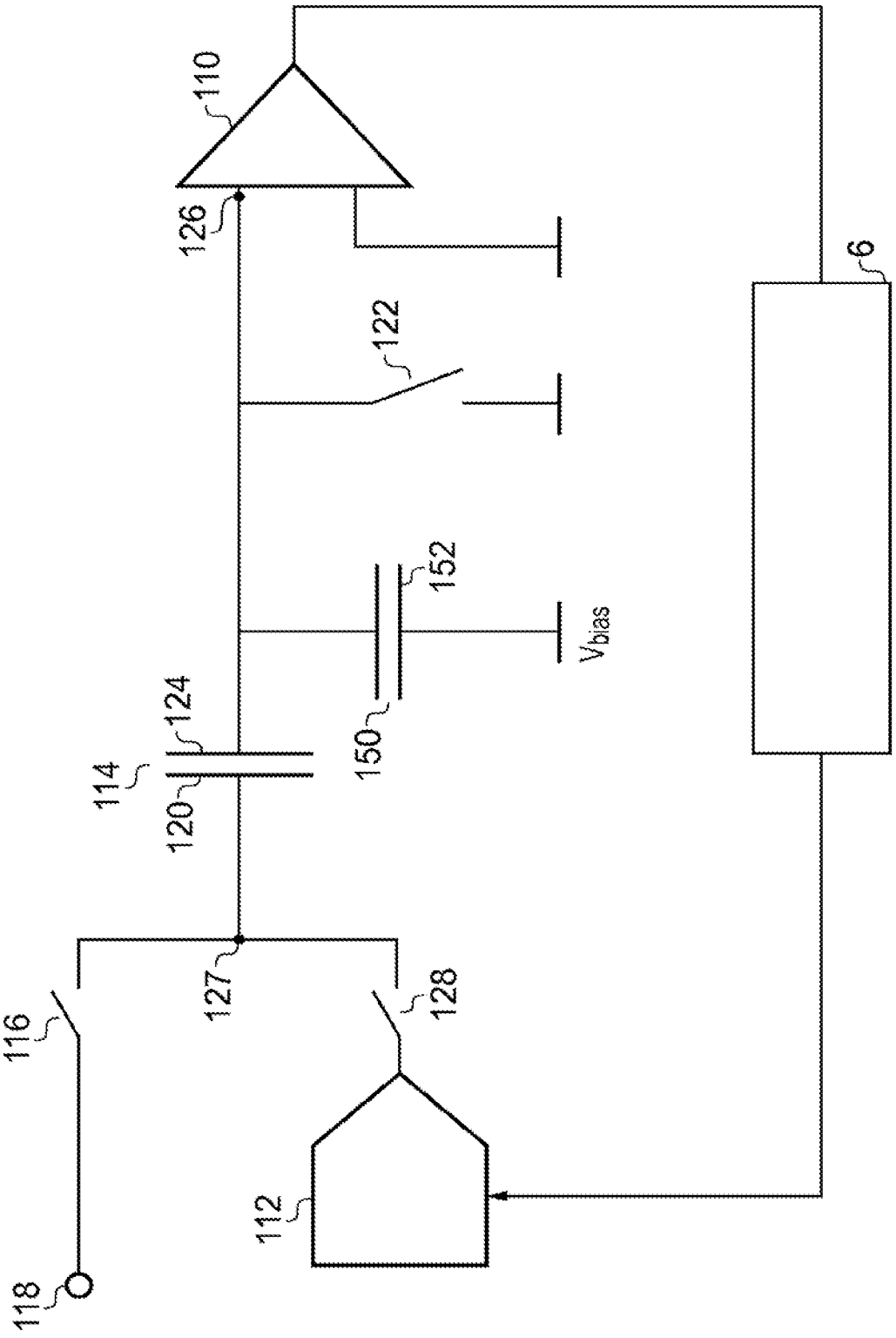


FIG. 2

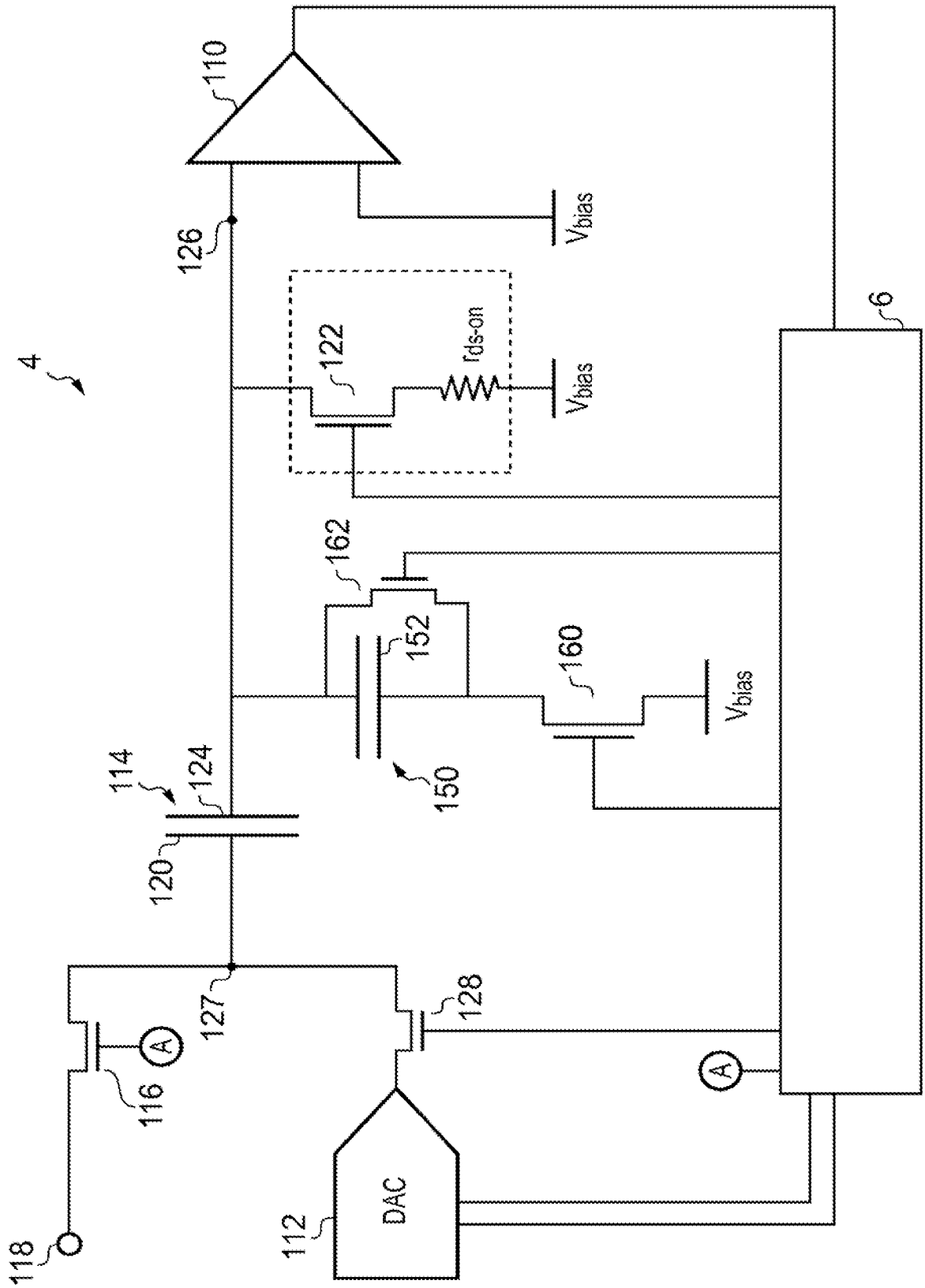

4
110
126
V_{bias}
122
r_{ds-on}
V_{bias}
6
162
152
160
V_{bias}
114
124
150
120
127
128
116
A
A
118
112
DAC

FIG. 3

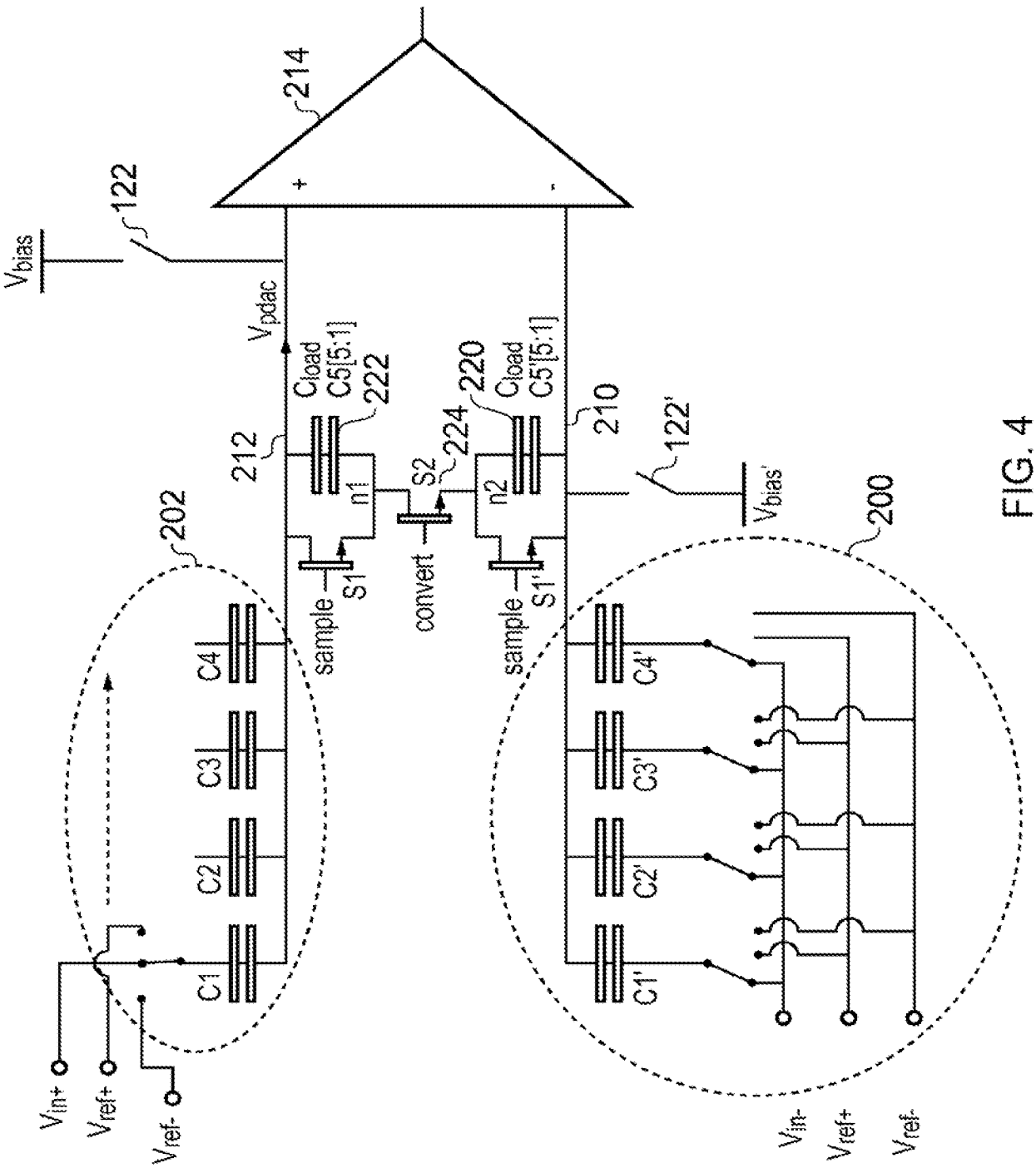

214
122
Vbias
Vpdac
Cload
C5[5:1]
222
220
224
S2
n1
n2
212
210
122'
Vbias'
202
200
C4
C3
C2
C1
C4'
C3'
C2'
C1'
sample
S1
convert
S1'
Vin+
Vref+
Vref-
Vin-
Vref+
Vref-

FIG. 4

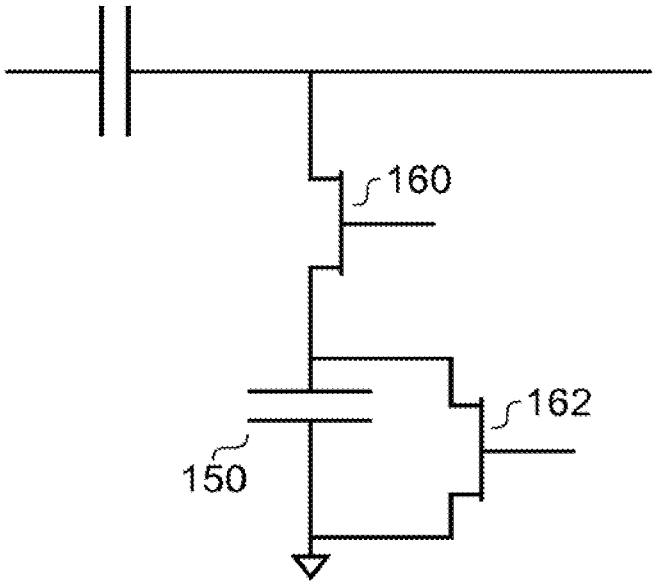


FIG. 5

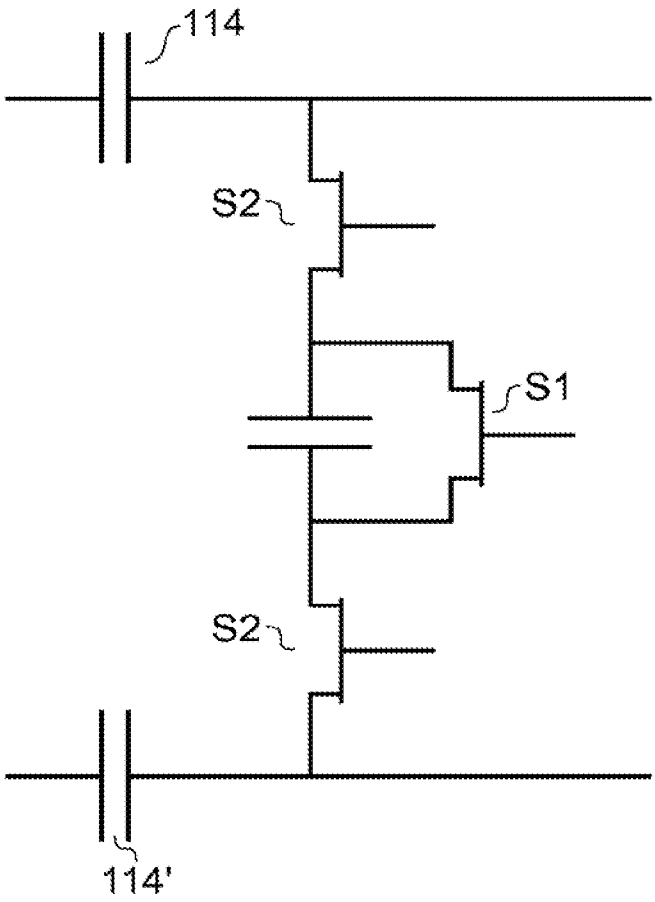


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/036348

A. CLASSIFICATION OF SUBJECT MATTER

INV. A61K31/137 A61K31/337 A61K31/343 A61K31/395 A61K31/401
A61K31/4025 A61K31/4045 A61K31/4184 A61K31/427 A61K31/435
A61K31/4422 A61K31/4453 A61K31/4525 A61K31/517 A61K31/5375

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
A61K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, EMBASE, BIOSIS, CHEM ABS Data, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	HEFFETER ET AL: "Multidrug-resistant cancer cells are preferential targets of the new antineoplastic lanthanum compound KP772 (FFC24)" BIOCHEMICAL PHARMACOLOGY, PERGAMON, OXFORD, GB LNKD- DOI:10.1016/J.BCP.2007.03.002, vol. 73, no. 12, 5 May 2007 (2007-05-05), pages 1873-1886, XP022062511 ISSN: 0006-2952	2,4-7,9, 11
Y	abstract; first of "results"	8,10, 12-16

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 September 2010	05/10/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Dahse, Thomas

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/036348

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	WO 2006/009765 A2 (US HEALTH [US]; SZAKACS GERGELY [US]; ANNEREAU JEAN-PHILLIPE [FR]; LAB) 26 January 2006 (2006-01-26) p. 1, l. 11; p. 2, l. 9-16; claim 12; p. 11, l. 30 to p. 12, l. 6, in particular compound NSC10580	1,3,5-16 2,7-16
A	LIN A J ET AL: "Catecholamine analogs as potential antitumor agents. II" JOURNAL OF PHARMACEUTICAL SCIENCES 1981 US, vol. 70, no. 7, 1981, pages 806-808, XP002592579 ISSN: 0022-3549 abstract, compounds I, VI, X	1,3,5-16
A,P	ORINA J N ET AL: "Evaluation of current methods used to analyze the expression profiles of ATP-binding cassette transporters yields an improved drug-discovery database" MOLECULAR CANCER THERAPEUTICS 20090701 AMERICAN ASSOCIATION FOR CANCER RESEARCH INC. USA LNKD- DOI:10.1158/1535-7163.MCT-09-0256, vol. 8, no. 7, 1 July 2009 (2009-07-01), pages 2057-2066, XP002592580 ISSN: 1535-7163 Fig. 4B; p. 2065, col. 1, penultimate	1,3,5-16
X,P	TURK D ET AL: "Identification of compounds selectively killing multidrug-resistant cancer cells" CANCER RESEARCH 20091101 AMERICAN ASSOCIATION FOR CANCER RESEARCH INC. USA LNKD- DOI:10.1158/0008-5472.CAN-09-2422, vol. 69, no. 21, 1 November 2009 (2009-11-01), pages 8293-8301, XP002592581 ISSN: 0008-5472 abstract; table 4	1-16
Y	WO 02/102805 A1 (KAROLINSKA INNOVATIONS AB [SE]; LARSSON OLLE [SE]; AXELSON MAGNUS [SE]) 27 December 2002 (2002-12-27) table 5; fig. 2A/2B; claim 14	2,7, 9-13,16

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/036348

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 03/014128 A2 (FAUSTUS FORSCHUNGS CIE [DE]; KEPPLER BERNHARD [DE]) 20 February 2003 (2003-02-20) p. 12, example 2	2,4-16
A	DE 101 38 538 A1 (FAUSTUS FORSCHUNGS CIE [DE]) 27 February 2003 (2003-02-27) example 2; claim 6	2,4-16
A	US 4 699 978 A (BARTON JACQUELINE K [US]) 13 October 1987 (1987-10-13) col. 6, l. 19-20 and table 1; col. 2, l. 12-46	2,4-16

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/036348

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☒ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

2(completely); 4-16(partially)

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☒ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1, 3(completely); 5-16(partially)

   directed to compounds of formula I for use as growth inhibitors of drug resistant cells.

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2. claims: 2, 4-16(all partially)

   directed to compound NSC43320 for use as growth inhibitors of drug resistant cells.

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3. claims: 2, 4-16(all partially)

   directed to compounds NSC672027, NSC672036 for use as growth inhibitors of drug resistant cells.

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4. claims: 2, 4-16(all partially)

   directed to compounds NSC632736, NSC632733, NSC632738, NSC654724, NSC632591, NSC162800, NSC165697, NSC619179, NSC619181, NSC619183, NSC619184, NSC619188, NSC630123, NSC632591, NSC632734, NSC632735, NSC632737, NSC632738 for use as growth inhibitors of drug resistant cells.

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5. claims: 2, 4-16(all partially)

   directed to compound NSC632955 for use as growth inhibitors of drug resistant cells.

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6. claims: 2, 4-16(all partially)

   directed to compound NSC633657 for use as growth inhibitors of drug resistant cells.

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7. claims: 2, 4-16(all partially)

   directed to compound NSC710857 for use as growth inhibitors of drug resistant cells.

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8. claims: 2, 4-16(all partially)

   directed to compounds NSC651859, NSC653864, NSC403148 for use as growth inhibitors of drug resistant cells.

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9. claims: 2, 4-16(all partially)

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

directed to compound NSC693046 for use as growth inhibitors of drug resistant cells.

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10. claims: 2, 4-16(all partially)

directed to compounds NSC705305, NSC705301 for use as growth inhibitors of drug resistant cells.

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11. claims: 2, 4-16(all partially)

directed to compound NSC639743 for use as growth inhibitors of drug resistant cells.

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12. claims: 2, 4-16(all partially)

directed to compound NSC635977 for use as growth inhibitors of drug resistant cells.

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13. claims: 2, 4-16(all partially)

directed to compound NSC636097 for use as growth inhibitors of drug resistant cells.

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14. claims: 2, 4-16(all partially)

directed to compound NSC624967 for use as growth inhibitors of drug resistant cells.

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15. claims: 2, 4-16(all partially)

directed to compound NSC669341 for use as growth inhibitors of drug resistant cells.

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16. claims: 2, 4-16(all partially)

directed to compound NSC697920 for use as growth inhibitors of drug resistant cells.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2010/036348

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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