A method of fabricating an integrated circuit comprising providing a substrate, forming a first layer on the substrate by electrochemical deposition using an electrolyte solution, and converting at least a portion of the first layer into a second layer by electrochemical oxidation using an electrolyte solution, the second layer being an oxide layer.
METHOD OF FABRICATING AN INTEGRATED CIRCUIT

BACKGROUND

[0001] The fabrication of highly integrated electrical circuits (also referred to as simply Integrated Circuits or ICs) with small structural dimensions is carried out by subjecting a semiconductor substrate disk, also referred to as a wafer, to a complex series of different processes. The processes include deposition steps in order to form layers of different materials on the wafer. Further process steps during which electrical structures of integrated circuits are gradually formed on the wafer include removal, patterning and modification steps.

[0002] An electrical structure of an integrated circuit may for example comprise a stack of layers, the stack including two layers which are separated from each other by an insulating or dielectric layer. Examples of such a layer stack include MIM—(Metal-Insulator-Metal), SIS—(Semiconductor-Insulator-Semiconductor), MIS—(Metal-Insulator-Semiconductor), RIR—(Ruthenium-Insulator-Ruthenium) and RIM—(Ruthenium-Insulator-Metal) structures.

[0003] Conventional processes carried out to deposit layers on a semiconductor wafer for electrical structures of an integrated circuit include deposition techniques, for example, CVD (Chemical Vapor Deposition), ALD (Atomic Layer deposition) and PVD (Physical Vapor Deposition). In these processes, the deposition is typically performed in a vacuum or low-pressure atmosphere, which may be associated with a relatively high complexity. Moreover, the formation of layers in structures with a high aspect ratio of depth to width may be challenging using the conventional deposition techniques.

SUMMARY

[0004] The embodiments described herein relate to methods of fabricating an integrated circuit.

[0005] One embodiment provides a method of fabricating an integrated circuit. In the method, a substrate is provided. A first layer is formed on the substrate by electrochemical deposition using an electrolyte solution. At least a portion of the first layer is converted into a second layer by electrochemical oxidation using an electrolyte solution, the second layer being an oxide layer.

[0006] Another embodiment provides a method of fabricating an integrated circuit in the method, a substrate is provided. A first layer is formed on the substrate by electrochemical deposition using an electrolyte solution. A portion of the first layer is converted into a second layer by electrochemical oxidation using an electrolyte solution to provide a second layer, the second layer being an oxide layer and being located on the first layer. A third layer is formed on the second layer being separated from the first layer by the second layer.

[0007] Yet another embodiment provides another method of fabricating an integrated circuit. In the method, a substrate is provided. A first layer is formed on the substrate by electrochemical deposition using an electrolyte solution. A second layer is formed on the first layer by electrochemical deposition using an electrolyte solution. The second layer is converted into an oxide layer by electrochemical oxidation using an electrolyte solution.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] So that the manner in which the above recited features of the present invention can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0009] FIGS. 1 to 6 illustrate schematic sectional views of a substrate for illustrating steps of a method for fabricating a structural element of an integrated circuit, according to an embodiment of the invention.

[0010] FIG. 7 illustrates a schematic view of a device for carrying out an electrochemical process using an electrolyte solution, according to an embodiment of the invention.

[0011] FIG. 8 illustrates a Pourbaix diagram of aluminium, according to an embodiment of the invention.

[0012] FIG. 9 illustrates a schematic view of another device for carrying out an electrochemical process using an electrolyte solution, according to an embodiment of the invention.

[0013] FIGS. 10 to 11 illustrate schematic sectional views of a substrate for illustrating steps of a further method for fabricating a structure element of an integrated circuit, according to an embodiment of the invention.

[0014] FIGS. 12 to 16 illustrate schematic sectional views of a substrate for illustrating steps of a further method for fabricating a structure element of an integrated circuit, according to an embodiment of the invention.

[0015] FIGS. 17 to 18 illustrate schematic sectional views of a substrate for illustrating steps of a further method for fabricating a structure element of an integrated circuit, according to an embodiment of the invention.

[0016] FIGS. 19 to 23 illustrate schematic sectional views of a substrate for illustrating steps of a further method for fabricating a transistor, according to an embodiment of the invention.

[0017] FIGS. 24 to 28 illustrate schematic sectional views of a substrate for illustrating steps of another method for fabricating a transistor, according to an embodiment of the invention.

[0018] FIG. 29 illustrates a schematic sectional view of a substrate comprising recesses, according to an embodiment of the invention.

[0019] FIGS. 30 and 31 illustrate the substrate of FIG. 29, wherein layer stacks are formed in the recesses, according to an embodiment of the invention.

[0020] FIG. 32 illustrates a schematic sectional view of a substrate comprising recesses, the recesses having an undercut geometry, according to an embodiment of the invention.

[0021] FIGS. 33 and 34 illustrate the substrate of FIG. 32, wherein layer stacked are formed in the recesses, according to an embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0022] In the following, reference is made to embodiments of the invention. However, it should be understood that the invention is not limited to specific described embodiments. Instead, any combination of the following features and elements, whether related to different embodiments or not, is contemplated to implement and practice the invention. Furthermore, in various embodiments the invention provides numerous advantages over the prior art. However, although embodiments of the invention may achieve advantages over other possible solutions and/or over the prior art, whether or not a particular advantage is achieved by a given embodiment...
is not limiting of the invention. Thus, the following aspects, features, embodiments and advantages are merely illustrative and are not considered elements or limitations of the appended claims except where explicitly recited in a claim(s). Likewise, reference to “the invention” shall not be construed as a generalization of any inventive subject matter disclosed herein and shall not be considered to be an element or limitation of the appended claims except where explicitly recited in a claim(s).

[0023] Embodiments described herein relate to the fabrication of a structure element of an integrated circuit device. The integrated circuit device may for example be a control circuit or a memory circuit. Examples for the latter are DRAM (Dynamic Random Access Memory), PCRAM (Phase Change RAM), CBRAM (Conductive Bridging RAM), MRAM (Magneto-resistive RAM) and flash memory devices. The methods generally comprise the formation of layers and conversion of the same by means of electrochemical processes using an electrolyte solution. In this connection, the applied electrochemical processes may be carried out using an external current source, or may be performed in an electroless manner. The electrochemical processes may further be carried out at normal pressure, so that layer formation and conversion may be performed with a relatively low complexity.

[0024] FIGS. 1 to 6 illustrate schematic sectional views of a substrate 100 for illustrating steps of a method for fabricating a structure element 140 of an integrated circuit, according to an embodiment of the invention. The substrate 100, which may include a semiconductor material such as e.g. silicon, may for example be a semiconductor wafer.

[0025] As illustrated in FIG. 1, a first layer 110 may be formed on the surface of the provided substrate 100. Formation of the layer 110 may be carried out by electrochemical deposition using a liquid electrolyte solution. For example, in one embodiment, the substrate 100 may be immersed in the electrolyte solution as described further below. The electrolyte solution may include charged particles or ions, respectively, of the layer material to be deposited, which may be discharged when deposited at the substrate surface. The particles or ions may for example be positively charged, and may be reduced in the deposition process by gain of electrons.

[0026] As an example, the layer 110 may be a metal layer comprising for example Al, in one embodiment. In this case, Al$^{3+}$ ions may be dissolved in the electrolyte solution and deposited according to the following chemical reaction

$$\text{Al}^{3+} + 3e^- \rightarrow \text{Al} \quad (1).$$

[0027] After deposition of the layer 110 on the substrate 100, an upper portion of the layer 110 may be converted into a second layer 120 as depicted in FIG. 2, the second layer 120 being an oxide layer in one embodiment. In this context, the term “upper” portion of a layer used herein and in the following relates to a portion of the respective layer adjoining to the exposed or uncovered layer surface. In one embodiment, partially oxidizing the layer 110 may be carried out by electrochemical oxidation using an electrolyte solution. The oxidation process includes the loss of electrons by atoms or molecules of the respective layer material.

[0028] In case the layer 110 is an aluminum layer (as described in the above-mentioned example), the partial oxidation of the layer 110 to provide the layer 120 may e.g. take place according to the following chemical reactions

$$\text{Al} \rightarrow \text{Al}^{3+} + 3e^- \quad (2)$$

and

$$2\text{Al}^{3+} + 3\text{H}_2\text{O} \rightarrow \text{Al}_2\text{O}_3 + 6\text{H}^+ + 6e^- \quad (3).$$

[0029] In one embodiment, an upper portion of the oxide layer 120 may be converted into a third layer 130, as illustrated in FIG. 3. The third layer 130 is separated from the first layer 110 by the second layer 120. Partially converting the layer 120 to provide the third layer 130 may be carried out by electrochemical reduction using an electrolyte solution. In one embodiment, the third layer 130 may include the same material as the first layer 110. This may be because the third layer 130 may originate from the initially deposited layer 110, in one embodiment. The reduction process includes the gain of electrons by the atoms or molecules of the respective layer material.

[0030] In the example where the layer 120 is an aluminum oxide layer (as described in the above-mentioned example), the partial reduction of the layer 120 to form the layer 130 may e.g. take place according to the following chemical reaction

$$\text{Al}_2\text{O}_3 + 6\text{e}^- + 3\text{H}_2\text{O} \rightarrow 2\text{Al} + 6\text{OH}^- \quad (4).$$

[0031] The layer stack including the three layers 110, 120, 130 located one upon another on the substrate 100 may subsequently be structured to provide the structure element 140 as shown in FIG. 4. In one embodiment, a dry etching process may for example be carried out. An example of dry etching is reactive ion etching (RIE). In order to define the lateral structure of the structure element 140 to be formed, a corresponding area on the layer 130 may be covered by means of one or more suitable masking layers (not shown) previous to performing the etching process. The masking layer may for example include a structured photoresist layer or a structured hard mask layer.

[0032] Alternatively, as illustrated in FIG. 5, the substrate 100 may be provided with a structured masking layer 150 before carrying out the electrochemical deposition of the layer 110. The structured masking layer 150 may be a photoresist layer or a hard mask layer. By means of the structured masking layer 150, a selective region of the surface of the substrate 100 may be exposed. Therefore, by carrying out the electrochemical processes described above with reference to FIGS. 1 to 3, it is possible to selectively deposit the layer 110, and thus to fabricate the structure element 140 only on the surface region of the substrate 100 not being covered by the masking layer 150 as shown in FIG. 6.

[0033] In one embodiment, the fabricated structure element 140 comprises two metal layers 110, 130 being separated from each other by an oxide layer 120. Such a layer stack, which represents a RIR- or MIM-structure, may for example be used as a capacitor in an integrated circuit device. Apart from the above specified metal aluminum, other metals like e.g. Cu, Ag, Au, Pd, Pt, Ru, Ni, Cr, Fe, Ti, Ta, Hf, Zr may be considered.

[0034] In one embodiment, a semiconductor material like e.g. Si or Ge may be electrochemically deposited on the substrate 100. In this case, the layer stack and thus the structure element 140 represents a SIS-structure comprising two semiconductor layers 110, 130 being separated from each other by an oxide layer 120.

[0035] Apart from deposition of a single material, it is further possible to electrochemically deposit different materials or metals simultaneously. In this way, the layer 110 (and thus the layer 130) may comprise a mixture of different materials or an alloy.
Potential electrolyte solutions which may be used to carry out the electrochemical deposition and conversion (oxidation, reduction) processes include aqueous electrolyte solutions, organic electrolyte solutions and ionic liquids. An example for an organic electrolyte solution is alcohol. Examples for ionic liquids, which may substantially comprise ions, are 1-butyl-1-methylpyridinium-bis(trifluoromethylsulfonyl)amide and 1-ethyl-3-methylimidazolium-bis(trifluoromethylsulfonyl)amide.

The type of electrolyte solution to be applied may depend on the respective electrochemical process to be carried out, for example, with respect to a deposition process, the material to be deposited may govern the selection of the electrolyte solution. As an example, an aqueous electrolyte solution may be used for the electrochemical deposition of Cu, Ag, Au, Pd, Pt, Ru, Ni, Cr and Fe. Materials like for example Ti, Ta, Al, Si, Ge, Hf and Zr may be electrochemically deposited by means of an organic electrolyte solution or an ionic liquid. In one embodiment, the materials to be deposited may for example be dissolved in the respective electrolyte solutions in the form of salts. Apart from these materials, an electrolyte solution may comprise further dissolved substances or agents e.g. originating from salts, by means of which an electrochemical process may be influenced or controlled, respectively. This may, for example, be the case when carrying out a process in an electroless manner, as described further below.

The electrochemical deposition and conversion processes, e.g. the sequence of deposition, oxidation and reduction to fabricate the stack of layers 110, 120, 130 depicted in FIG. 3, may each be performed using a different electrolyte solution. In other words, for each process, the substrate 100 may be immersed in a different electrolyte solution. In one embodiment, the substrate 100 may for example be rinsed (e.g. by means of water) in between two immersion steps. Alternatively, it is possible to perform different electrochemical processes by means of the same electrolyte solution, i.e. the substrate 100 is immersed in one electrolyte solution throughout a number or all electrochemical processes to be carried out in the fabrication of a layer sequence. This variant, which makes it possible to carry out layer deposition and conversion with relatively little time and effort, may be performed by means of an external current source. In one embodiment, the different electrochemical processes may be controlled, inter alia, by the magnitude and polarity of the applied voltage and current.

FIG. 7 shows a schematic view of a device 160 which may be used to carry out an electrochemical process by applying an external current/voltage, according to an embodiment of the invention. The device 160 may include a tank 162 which is filled with a liquid electrolyte solution 170. The electrolyte solution 170 may be an aqueous electrolyte solution, an organic electrolyte solution, or an ionic liquid. A substrate holder 163 is provided in order to hold a substrate 100. By means of the substrate holder 163, the substrate 100 may be held in an upside-down manner, and may be partially immersed in the electrolyte solution 170, so that the surface of the substrate 100 (or a layer arranged on the substrate 100) may be subjected to the electrochemical process where the surface contacts the electrolyte solution 170 as illustrated in FIG. 7.

The device 160 furthermore comprises a counter-electrode 164 being arranged in the tank 162, and a current source or power supply 165. Wirings 166, 167 connect the substrate 100 and the counter-electrode 164 to the power supply 165. As indicated in FIG. 7, the wiring 166 may contact the backside of the substrate 100. By means of the power supply 165 and the wirings 166, 167, an external voltage or current may be applied between the substrate 100 and the counter-electrode 164. In this way an electrical current is generated between the substrate 100 and the counter-electrode 164, thereby providing or drawing off electrons to evoke the respective electrochemical deposition and/or conversion reactions at the substrate 100 and the layer(s) formed thereon, respectively. Similarly, respective chemical oxidation and reduction reactions may take place at the counter-electrode 164. Deposition of a layer by means of an external power supply 165 is also referred to as electroplating or electrodeposition.

In order to allow for transfer of electrons through the substrate 100 from and to the substrate backside, the substrate 100 may comprise a doped semiconductor material. Alternatively, it is possible to provide the surface of the substrate 100 with a conducting seed layer, wherein the seed layer is connected to the wiring 166 (not shown). When a hardly conducting, insulating or oxide layer is present on the surface of the substrate, for example the oxide layer 120 depicted in FIGS. 2 and 3, electron transfer may take place through the respective layer by for example electron tunneling processes.

Parameters like magnitude, polarity and time period of the applied current and voltage may be used to control and to cause the electrochemical deposition and conversion processes. As an example, the thicknesses of the individual layers to be formed may be set by means of the time period of the applied current/voltage. In one embodiment, the current and voltage may be applied with a constant magnitude. Alternatively, it is possible to apply the current and voltage in a periodic manner, which in the case of layer deposition is also referred to as pulse plating. Further parameters by means of which the electrochemical processes may be influenced relate to the composition of the electrolyte solution 170, i.e. for example to concentrations of dissolved substances and, when the electrolyte solution 170 is an aqueous electrolyte solution, to the pH-value.

In case of an aqueous electrolyte solution, process parameters for the control of an electrochemical process (e.g. the magnitude of an external current/voltage to be applied in order to cause a specific process) may be determined with the aid of so-called Pourbaix diagrams. These diagrams, which may be constructed through the use of thermodynamic theory (the Nernst equation) map out possible stable states of a material in an aqueous medium or water, respectively.

FIG. 8 illustrates a Pourbaix diagram 900 for the electrolyte system aluminium/water, according to an embodiment of the invention. The diagram 900 indicates the stability regions of pure Al (region 901), Al\(^{3+}\) ions (region 902), Al\(_2\)O\(_3\) (region 903) and AlO\(_2\)\(^{-}\) ions (region 904) as a function of pH-value and electrochemical potential (reduction potential with respect to the standard hydrogen electrode) U. The regions 902 and 904 for the Al\(^{3+}\) and AlO\(_2\)\(^{-}\) ions are further illustrated depending on concentrations of the respective ions, wherein the specifications 0, -2, -4, -6 represent the logarithm of the concentration by mol/l. The diagram 900 furthermore illustrates a diagonal dashed line 910 which represents the lower limit of the stability of water. In the region below the dashed line 910, hydrogen gas is evolved from hydronium contained in water. In one embodiment, for a pH-value of 7, an oxidation reaction of Al to form Al\(_2\)O\(_3\) may
be caused at a potential \( U \) of greater than approximately \(-2V\). In a potential region above \(-2V\), however, additionally formation of hydrogen gas occurs. Consequently, a potential \( U \) of greater than approximately \(-0.5V\) (i.e. above the dashed line\(910\)) may be applied in order to only perform oxidation of AI without formation of hydrogen gas. In case of a relatively low pH-value of for example 1, formation of \( \text{AI}_2\text{O}_3 \) from AI does not occur since AI atoms may only be converted into \( \text{AI}^3+ \) ions which are dissolved in the aqueous electrolyte solution. For relatively high pH-values, AI atoms may convert into \( \text{AI}O_2^- \) ions instead of being oxidized. Similarly, conclusions regarding applicable pH-values and electrochemical potentials \( U \) may be derived with respect to electrochemical deposition of AI and reduction of \( \text{AI}_2\text{O}_3 \).

[0045] In one embodiment, instead of carrying out an electrolytic process like e.g. a layer deposition process by means of an external current source, an electrochemical process may also be performed in an electroless manner. In case of layer deposition, this process is also referred to as electroless plating. In addition to deposition, reduction and oxidation processes may also be performed in an electroless manner. In case a sequence of different electrochemical processes is to be carried out in an electroless manner, each of the processes may be performed using a different electrolyte solution.

[0046] As an illustration, FIG. 9 shows a schematic view of a device 161 which may be used to carry out an electrochemical process in an electroless manner. The device 161 may include a tank 162 which is filled with an electrolyte solution 171. The electrolyte solution 171 may be an aqueous electrolyte solution, an organic electrolyte solution, or an ionic liquid. The device 161 further comprises a substrate holder 163 by means of which a substrate 100 may be partially immersed in the electrolyte solution 171, thereby establishing contact of the surface of the substrate 100 (or a layer arranged on the substrate 100) to be subjected to the electrochemical process with the electrolyte solution 171.

[0047] In one embodiment, the electrolyte solution 171 may include reactants which may provide (reducing agent) or draw off electrons (oxidizing agent) to evoke a respective electrochemical process. The tendency for a respective chemical reaction in an electrolyte solution 171 is given by the reduction potential of the reactants in the electrolyte solution 171. According to the Nerst equation, the reduction potential is dependent on the concentrations of the reactants in the electrolyte solution 171 and, when the electrolyte solution 171 is an aqueous electrolyte solution, on the pH-value. In other words, an electroless process may be controlled by means of the concentrations of reactants in the electrolyte solution 171 and, in some cases, the pH value of the solution 171. A further parameter that controls an electroless process is the time period during which the substrate 100 is subjected to the electrolyte solution 171.

[0048] Examples for a reducing agent (electron donor) include \( \text{H}_3\text{PO}_4 \), \( \text{H}_3\text{PO}_3 \), \( \text{H}_2\text{CO} \) and Mn\(^{2+}\). With respect to these substances, donation of electrons may for example take place according to the following chemical reactions

\[
\text{H}_3\text{PO}_4 + 2\text{H}_2\text{O} \rightarrow \text{H}_2\text{PO}_4^- + 4\text{H}^- + \text{H}_3\text{O}^+ \quad (5)
\]

\[
\text{H}_3\text{PO}_4 + \text{H}_2\text{O} \rightarrow \text{H}_3\text{PO}_4 + 2\text{H}^+ + 2\text{e}^- \quad (6)
\]

\[
\text{H}_2\text{CO} + \text{H}_2\text{O} \rightarrow \text{HCOOH} + 2\text{H}^+ + 2\text{e}^- \quad (7)
\]

and

\[
\text{Mn}^{2+} + 2\text{H}_2\text{O} \rightarrow \text{MnO}_2 + 4\text{e}^- + 4\text{H}^+ \quad (8)
\]

[0049] An example for an oxidizing agent (electron acceptor) is Mn\(^{2+}\). The respective oxidation reaction may e.g. take place according to the following chemical reaction:

\[
\text{MnO}_2 + 8\text{H}^+ + 5\text{e}^- \rightarrow \text{Mn}^{2+} + 4\text{H}_2\text{O} \quad (9)
\]

[0050] The chemical reactions (5) to (9) may also take place when carrying out an electrochemical process using an external current source, provided that the respective reducing or oxidizing agents are dissolved in the applied electrolyte solution.

[0051] With respect to carrying out a deposition process in an electroless manner, for example deposition of the layer 110 on the surface of the substrate 100 as illustrated in FIG. 1, the surface to be deposited may be subjected to a surface preparation or treatment before carrying out the deposition process. In this way it is possible to catalytically promote the subsequent layer deposition. An example of a surface treatment process is the deposition of an organic layer or seed layer on the surface to be deposited.

[0052] A whole sequence of electrochemical processes—e.g. the sequence of deposition, oxidation and reduction to fabricate the stack of layers 110, 120, 130 depicted in FIG. 3—may be performed both in an electroless manner and by means of providing external current. Moreover, it is also possible to perform a sequence of processes in a manner that one or several processes are performed using external current, whereas another process or other processes are performed in an electroless manner. As an example, deposition of the layer 110 may be carried out in an electroless manner using a respective electrolyte solution, and the subsequent oxidation and reduction processes to form the layers 120, 130 may be performed by means of an external current source using (a) further electrolyte solution(s).

[0053] In the following figures, further methods including electrochemical deposition and conversion processes according to embodiments of the invention are illustrated. For these methods, the above description relating to details of electrochemical processes, e.g. to materials to be deposited, possible electrolyte solutions, carrying out processes by means of an external current source or in an electroless manner etc. may be applied as well.

[0054] FIGS. 10 and 11 show schematic sectional views of a substrate 100 for illustrating steps of an alternative method for fabricating a structure element 141 of an integrated circuit, according to an embodiment of the invention. This method includes steps similar to the method described with reference to FIGS. 1 to 6, i.e. a first layer 110 is formed on the provided substrate 100 (e.g. a semiconductor wafer) by electrochemical deposition using an electrolyte solution, and an upper portion of the first layer 110 (e.g. a semiconductor wafer) by electrochemical deposition using an electrolyte solution, the second layer 120 being an oxide layer (see FIGS. 1 and 2). Thereafter, instead of electrochemically reducing a portion of the oxide layer 120, a third layer 131 is formed on the second layer 120 by electrochemical deposition using an electrolyte solution (FIG. 10).

[0055] For example, in one embodiment, the deposition of the first layer 110 and formation of the layer 120 may be performed with the same electrolyte solution (e.g. by application of a different external current/voltage), and deposition of the layer 131 may be carried out using a different electrolyte solution (in an electroless manner or using an external
The layer 131 may for example be a metal layer, which is deposited on the oxide layer 120 according to the following chemical reaction:

\[ \text{Me}^{z+} + ze^{-} \rightarrow \text{Me} \]  

(10),

wherein Me denotes the metal species, and z the charge of the Me ions and the number of gained electrons, respectively. In alternative embodiments, the deposited layer 131 may also be a semiconductor layer.

The stack including the three layers 110, 120, 131 located one upon another on the substrate 100 may subsequently be structured to provide the structure element 141 as shown in FIG. 11. Depending on the materials deposited to form the layer 110 and the layer 131, the structure element 141 may represent a MIM-, RIR-, SIS-, MIS-, or RIM-structure.

Patterning the layers 110, 120, 131 to provide the structure element 141 may for example be performed by means of a dry etching process using one or several masking layers (not shown). Alternatively, the substrate 100 may be provided with a structured masking layer 150 before carrying out the electrochemical deposition of the layer 110, so that fabrication of the structure element 141 may selectively take place on the surface region of the substrate 100 not being covered by the masking layer 150.

The following FIGS. 12 to 16 show schematic sectional views of a substrate 100 for illustrating steps of a further method for fabricating a structure element 240 of an integrated circuit, according to an embodiment of the invention. The substrate 100 may for example be a semiconductor wafer. As illustrated in FIG. 12, a first layer 210 is formed on the surface of the provided substrate 100 by electrochemical deposition using an electrolyte solution. The layer 210 may for example be a metal layer or a semiconductor layer.

In one embodiment, the layer 210 may be a titanium layer which is deposited on the substrate 100 according to the following chemical reaction

\[ \text{Ti}^{2+} + 2e^{-} \rightarrow \text{Ti} \]  

(11).

Thereafter, a second layer 220 may be formed on the first layer 210 by electrochemical deposition using an electrolyte solution (FIG. 13). The second layer 220 may e.g. be a metal layer or a semiconductor layer, as well. In one embodiment, the layer 220 may be an aluminum layer which is deposited on the layer 210 according to the above specified chemical reaction (1). In one embodiment, formation of the layers 210, 220 may be carried out using different electrolyte solutions.

Subsequently, as shown in FIG. 14, the second layer 220 may be totally converted into an oxide layer 221 by electrochemical oxidation using an electrolyte solution. Conversion of the layer 220 may for example be performed with the same electrolyte solution used for deposition of the same (e.g. by application of a different external current/voltage), or alternatively with a different electrolyte solution. In case the layer 220 is an aluminum layer (see the above-mentioned example), the oxidation of the layer 220 to provide the (aluminum) oxide layer 221 may take place according to the above specified chemical reactions (2) and (3).

Subsequently, as shown in FIG. 15, a third layer 230 may be formed on the oxide layer 221 by electrochemical deposition using an electrolyte solution. The third layer 230 may for example be a metal layer or a semiconductor layer. With respect to a metal layer, the electrochemical deposition may take place according to the above specified chemical reaction (10). In one embodiment, formation of the layer 230 may be performed using another electrolyte solution which differs from the electrolyte solution used to convert the layer 220 into the oxide layer 221.

The stack including the three layers 210, 221, 230 located one upon another on the substrate 100 may subsequently be structured to provide the structure element 240 as shown in FIG. 16. The structure element 240 may represent a MIM-, RIR-, SIS-, MIS-, or RIM-structure, depending on the materials deposited to form the layer 210 and the layer 230.

Structuring the stack of layers 210, 221, 230 to provide the structure element 240 may for example be performed by means of a dry etching process. Alternatively, the substrate 100 may be provided with a structured masking layer 150 before carrying out the electrochemical deposition of the layer 210, so that fabrication of the structure element 240 may selectively take place on the surface region of the substrate 100 not being covered by the masking layer 150.

The following FIGS. 17 and 18 show schematic sectional views of a substrate 100 for illustrating steps of an alternative method for fabricating a structure element 241 of an integrated circuit, according to an embodiment of the invention. This method includes steps similar to the method described with reference to FIGS. 12 to 16, i.e. electrochemical deposition of a first layer 210 on the provided substrate 100, electrochemical deposition of a second layer 220 on the first layer 210, and electrochemical conversion of the complete layer 220 into an oxide layer 221 (see FIGS. 12 to 14).

Thereafter, an upper portion of the oxide layer 221 may be converted into a third layer 222 by electrochemical reduction using an electrolyte solution as illustrated in FIG. 17. The layer 222 may include the same material as the originally formed layer 220 (FIG. 13). In one embodiment, formation of the layer 222 by electrochemical reduction may be performed with the same electrolyte solution used for oxidation of the layer 220 to form the oxide layer 221 (e.g. by application of a different external current/voltage), or with a different electrolyte solution. In case the layer 222 is an aluminium oxide layer (cf. the above-mentioned example), the partial reduction of the layer 221 to form the layer 222 may take place according to the above specified chemical reaction (4).

The stack including the three layers 210, 221, 222 located one upon another on the substrate 100 may subsequently be structured to provide the structure element 241 as shown in FIG. 16. The structure element 241 may again represent a MIM-, RIR-, SIS-, MIS-, or RIM-structure, depending on the materials deposited to form the layer 210 and the layer 220. With respect to details regarding patterning of the layers 210, 221, 222, or providing a structured masking layer 150 previous to formation of the layer 210, reference is made to the preceding description.

The following FIGS. 19 to 23 show schematic sectional views of a substrate 100 for illustrating steps of a further method comprising electrochemical processes, according to an embodiment of the invention. The method may be applied to fabricate a structure element 340, which may serve as gate stack of a field effect transistor (FET) 350.

As illustrated in FIG. 19, a layer 310 may be formed on a surface of the provided substrate 100 (e.g. a semiconductor wafer) by electrochemical deposition using an ele-
trolyte solution. The layer 310 may for example be a metal layer. Afterwards, the layer 310 is totally converted into an oxide layer 311 by electrochemical oxidation using an electrolyte solution (FIG. 20). Conversion of the layer 310 into the oxide layer 311 may be performed with the same electrolyte solution used for deposition of the same (e.g. by application of a different external current/voltage), or with a different electrolyte solution.

[0071] Subsequently, an upper portion of the oxide layer 311 may be converted into a layer 312 by electrochemical reduction using an electrolyte solution (FIG. 21). The layer 312 may include the same material as the initially deposited layer 310. In one embodiment, formation of the layer 312 by electrochemical reduction may be performed with the same electrolyte solution used for oxidation of the layer 310 to form the oxide layer 311 (e.g. by application of a different external current/voltage), or with a different electrolyte solution.

[0072] The stack including the oxide layer 311 located on the substrate 100 and the layer 312 located on the oxide layer 311 may subsequently be structured to provide the structure element 340 (FIG. 22). Structuring may e.g. be performed by means of a dry etching process using one or several masking layers (not shown). Alternatively, the substrate 100 may be provided with a structured masking layer 150 previous to formation of the layer 310, so that fabrication of the structure element 340 may selectively be performed on the surface region of the substrate 100 not being covered by the masking layer 150.

[0073] The fabricated structure element 340 may for example be used as a capacitor, wherein the electrodes of the capacitor are formed by the layer 312 and the substrate region of the substrate 100 underneath the oxide layer 311. When the substrate 100 is a semiconductor substrate, the substrate region adjoining to the oxide layer 311 may for example comprise a doped semiconductor material (not depicted).

[0074] The structure element 340 may alternatively be used as gate stack of a transistor 350, wherein the layer 312 acts as gate electrode and the layer 311 as gate dielectric. As illustrated in FIG. 23, further method steps may be carried out for completion of the transistor 350. This includes formation of two doped regions 355 being separated from each other in the substrate 100 in a region below the layer stack 340. The two doped regions 355 may constitute source and drain of the transistor 350. The formation of the doped regions 355 may include carrying out one or several ion implantation processes in order to introduce corresponding dopants into the substrate 100. In order to implant the dopants at a distance with regard to the gate stack 340, spacers 360 may be formed at the sidewalls of the gate stack 340 prior to carrying out the ion implant(s), as indicated in FIG. 23.

[0075] The following FIGS. 24 to 28 show schematic sectional views of a substrate 100 for illustrating steps of a further method comprising electrochemical processes. The method may be applied to fabricate a structure element 440, which may serve as gate stack of a field effect transistor 450.

[0076] As illustrated in FIG. 24, a layer 410 may be formed on a surface of the provided substrate 100 (e.g. a semiconductor wafer) by electrochemical deposition using an electrolyte solution. The layer 410 may for example be a metal layer or a semiconductor layer. Afterwards, the layer 410 may be totally converted into an oxide layer 411 by electrochemical oxidation using an electrolyte solution (FIG. 25). In one embodiment, conversion of the layer 410 into the oxide layer 411 may be performed with the same electrolyte solution used for deposition of the same (e.g. by application of a different external current/voltage), or with a different electrolyte solution.

[0077] Subsequently, a further layer 420 may be formed on the oxide layer 411 by electrochemical deposition using an electrolyte solution (FIG. 26). The layer 420 may for example be a metal layer. In one embodiment the electrolyte solution applied in the deposition of the layer 420 may be a different one compared to the electrolyte solution(s) applied in the preceding electrochemical processes.

[0078] The stack including the oxide layer 411 located on the substrate 100 and the layer 420 located on the oxide layer 411 may subsequently be structured to provide the structure element 440 (FIG. 27). This step may e.g. be performed by means of a dry etching process. Alternatively, the substrate 100 may be provided with a structured masking layer 150 previous to formation of the layer 410, so that fabrication of the structure element 440 may selectively be performed on the surface region of the substrate 100 not being covered by the masking layer 150.

[0079] The fabricated structure element 440 may be used as e.g. a capacitor, wherein the electrodes of the capacitor are formed by the layer 420 and the substrate region of the substrate 100 underneath the oxide layer 411. The structure element 440 may alternatively be used as gate stack of a transistor 450, wherein the layer 420 acts as gate electrode and the layer 411 as gate dielectric. As illustrated in FIG. 28, further method steps may be carried out for completion of the transistor 450, including formation of two doped regions 455 for source and drain of the transistor 450 by means of one or several ion implantation processes. Spacers 460 may additionally be formed at the sidewalls of the gate stack 440 previous to carrying out the ion implant(s).

[0080] The application of electrochemical processes using liquid electrolyte solutions makes it possible to reliably form and convert layers on a substrate surface having a more complex geometry compared to a planar surface. By way of illustration, FIG. 29 shows a substrate 500 (e.g. a semiconductor wafer) having a number of recesses or trenches 505. The trenches 505 comprise a relatively high aspect ratio of depth to width, which is more than 2.

[0081] FIG. 30 depicts the substrate 500 after formation of layers 510, 520 in the trenches 505. As an example, the layer 510 may be an oxide layer, and the layer 520 may be a metal layer in order to provide trench capacitors. The electrodes of the trench capacitors are formed by the layer 520 and the substrate material of the substrate 500 adjoining to the oxide layer 510. In one embodiment, the substrate region adjoining to the oxide layer 510 may for example comprise a doped semiconductor material (not depicted). Formation of the layers 510, 520 may for example include electrochemical method steps similar to the processes depicted in FIGS. 19 to 21 (i.e. layer deposition, total oxidation of the deposited layer, and partial reduction of an upper portion of the oxidized layer) or the processes depicted in FIGS. 24 to 26 (i.e. deposition of a layer, total oxidation of the deposited layer, and deposition of a further layer).

[0082] In order to form the layers 510, 520 only in the trenches 505, a respective masking layer may be applied on the substrate 500 outside of the trenches 505 before layer formation (not depicted). Alternatively, it is for example possible to carry out a polishing process like CMP (Chemical
Mechanical Polishing) after formation of the layers 510, 520 in order to remove the layers 510, 520 outside of the trenches 505. [0083] The trenches 505 may additionally be completely filled up with an insulating material 530, for example poly silicon, as indicated in FIG. 30. The insulating material 530 may be formed by means of electrochemical deposition using an electrolyte solution, as well. Alternatively, it is possible to completely fill up the remaining void of the recesses 505 with the layer 520 (not shown).

[0084] FIG. 31 depicts the substrate 500 after formation of layers 610, 620, 630 in the trenches 505. As an example, the layers 610, 630 may be metal layers, and the layer 620 may be an oxide layer in order to provide trench capacitors. Formation of the layers 610, 620, 630 may for example include electrochemical method steps similar to the processes illustrated with respect to FIGS. 1 to 3 (i.e. layer deposition—partial oxidation of an upper portion of the deposited layer—partial reduction of an upper portion of the oxidized layer), the processes illustrated with respect to FIG. 10 (i.e. layer deposition—partial oxidation of an upper portion of the deposited layer—deposition of a further layer), the processes illustrated with respect to FIGS. 12 to 15 (i.e. deposition of a layer—deposition of a further layer—total oxidation of the deposited further layer—deposition of yet another layer) or the processes illustrated with respect to FIG. 17 (i.e. deposition of a layer—deposition of a further layer—total oxidation of the deposited further layer—partial reduction of an upper portion of the oxidized further layer).

[0085] In order to form the layers 610, 620, 630 only in the trenches 505, a masking layer may be applied on the substrate 500 outside of the trenches 505 before layer formation, or a polishing process may be performed after layer formation. The trenches 505 may additionally be completely filled up with an insulating material 640, for example poly silicon, as indicated in FIG. 31. Alternatively, it is possible to completely fill up the remaining void of the recesses 505 with the layer 630 (not shown).

[0086] FIG. 32 shows another example of a substrate 700 (e.g. a semiconductor wafer) with a number of trenches 705, according to an embodiment of the invention. The trenches 705 again have a relatively high aspect ratio of depth to width (of greater than 2) and additionally comprise an undercut geometry including an upper trench section 706 and a lower trench section 707, the lower trench section 707 being wider than the upper trench section 706. A reliable formation of layers on the substrate 700 in the trenches 705 and conversion of the same is again made possible by means of electrochemical processes using liquid electrolyte solutions.

[0087] FIG. 33 depicts the substrate 700 after electrochemical formation of layers 710, 720 in the trenches 705, according to an embodiment of the invention. As an example, the layer 710 may be an oxide layer, and the layer 720 may be a metal layer in order to provide trench capacitors. The electrodes of the trench capacitors may be formed by the layer 720 and the substrate material adjoining to the oxide layer 710. Formation of the layers 710, 720 may be carried out by means of electrochemical processes similar to formation of the layers 510, 520 in the trenches 505 depicted in FIG. 30.

[0088] FIG. 34 depicts the substrate 700 after electrochemical formation of layers 810, 820, 830 in the trenches 705. In one embodiment, the layers 810, 830 may be metal layers, and the layer 820 may be an oxide layer in order to provide trench capacitors. Formation of the layers 810, 820, 830 may be carried out by means of electrochemical processes similar to formation of the layers 610, 620, 630 in the trenches 505 depicted in FIG. 31.

[0089] The embodiments described with reference to the figures are examples and therefore not to be considered limiting. Further embodiments may be realized which comprise further modifications and variations of the described methods and integrated circuit devices. Instead of the materials indicated for layer deposition, other materials may be used. The same applies to the choice of electrolyte solutions.

[0090] Moreover, electrochemical deposition and conversion processes may be carried out using devices other than the devices 160, 161 illustrated in FIGS. 7 and 9. As an example, instead of partially immersing a substrate in an electrolyte solution, a substrate may be totally immersed in an electrolyte solution by means of a substrate holder. In this case, the substrate may additionally be provided with a sealing or encapsulation except for a region of the substrate surface to be subjected to an electrochemical process.

[0091] The methods may comprise further method steps than those described. These steps may for example relate to the fabrication of further components of an integrated circuit device. It is also possible to carry out e.g. an additional ion implanting process, thereby enhancing the electrical conductivity of a formed semiconductor layer. As an example, the layer 312 of the layer stack 340 depicted in FIG. 22 may be a semiconductor layer instead of a metal layer, and subjected to a further ion implant after formation for this purpose.

[0092] The preceding description describes embodiments of the invention. The features disclosed therein and the claims and the drawings can, therefore, be useful for realizing the invention in various embodiments, both individually and in any combination. While the foregoing is directed to embodiments of the invention, other and further embodiments of this invention may be devised without departing from the basic scope of the invention, the scope of the present invention being determined by the claims that follow.

What is claimed is:
1. A method of fabricating an integrated circuit, comprising:
   providing a substrate;
   forming a first layer on the substrate by electrochemical deposition using a first electrolyte solution; and
   converting at least a portion of the first layer into a second layer by electrochemical oxidation using a second electrolyte solution, the second layer being an oxide layer.
2. The method according to claim 1, further comprising:
   converting a portion of the second layer into a third layer by electrochemical reduction using a third electrolyte solution, the third layer comprising the same material as the first layer.
3. The method according to claim 1, further comprising:
   forming a third layer on the second layer by electrochemical deposition using a third electrolyte solution.
4. The method according to claim 1, wherein providing the substrate comprises forming a fourth layer on the substrate by electrochemical deposition using a fourth electrolyte solution, and wherein the first layer is formed on the fourth layer on the substrate.
5. The method according to claim 1, wherein at least one of forming the first layer and converting at least a portion of the first layer is carried out using an external current source coupled to the substrate and a counter-electrode.
6. The method according to claim 1, wherein at least one of forming the first layer and converting at least a portion of the first layer is carried out in an electroless manner.

7. The method according to claim 1, wherein forming the first layer and converting at least a portion of the first layer is carried out using the same electrolyte solution.

8. The method according to claim 1, wherein the first electrolyte solution is an ionic liquid.

9. The method according to claim 1, wherein the first electrolyte solution is an aqueous electrolyte solution.

10. The method according to claim 1, wherein the first electrolyte solution is an organic electrolyte solution.

11. The method according to claim 1, wherein the second electrolyte solution is an aqueous electrolyte solution.

12. The method according to claim 1, wherein the second electrolyte solution is an organic electrolyte solution.

13. The method according to claim 1, wherein the second electrolyte solution is an ionic liquid.

14. The method according to claim 1, wherein the first layer is a metal layer.

15. The method according to claim 1, wherein the first layer is a semiconductor layer.

16. The method according to claim 1, wherein the first layer comprises any one of the following materials: Cu, Ag, Au, Pd, Pt, Ru, Ni, Cr, Fe, Ti, Ta, Al, Si, Ge, Hf, Zr.

17. The method according to claim 1, wherein the substrate comprises at least one recess, and wherein the first layer is formed on the substrate in at least one recess.

18. The method according to claim 17, wherein the recess comprises an aspect ratio of depth to width that is greater than 2.

19. A method of fabricating an integrated circuit comprising:

   providing a substrate;
   forming a first layer on the substrate by electrochemical deposition using a first electrolyte solution;
   converting a portion of the first layer by electrochemical oxidation using a second electrolyte solution to provide a second layer, the second layer being an oxide layer formed on the first layer; and
   forming a third layer on the second layer, the third layer being separated from the first layer by the second layer.

20. The method according to claim 19, wherein forming the third layer comprises converting a portion of the second layer by electrochemical reduction using a third electrolyte solution, the third layer comprising the same material as the first layer.

21. The method according to claim 20, wherein forming the first layer, converting a portion of the first layer and converting a portion of the second layer is carried out using the same electrolyte solution.

22. The method according to claim 19, wherein the third layer is formed on the second layer by electrochemical deposition using a third electrolyte solution.

23. A method of fabricating an integrated circuit comprising:

   providing a substrate;
   forming a first layer on the substrate by electrochemical deposition using a first electrolyte solution;
   forming a second layer on the first layer by electrochemical deposition using a second electrolyte solution; and
   converting the second layer into an oxide layer by electrochemical oxidation using a third electrolyte solution.

24. The method according to claim 23 further comprising:

   forming a third layer on the second layer by electrochemical deposition using a fourth electrolyte solution.

25. The method according to claim 23 further comprising:

   forming a third layer on the second layer by converting a portion of the second layer by electrochemical reduction using a fourth electrolyte solution.

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