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(54) **Title**: ROBUST NUCLEATION LAYERS FOR ENHANCED FLUORINE PROTECTION AND STRESS REDUCTION IN 3D NAND WORD LINES

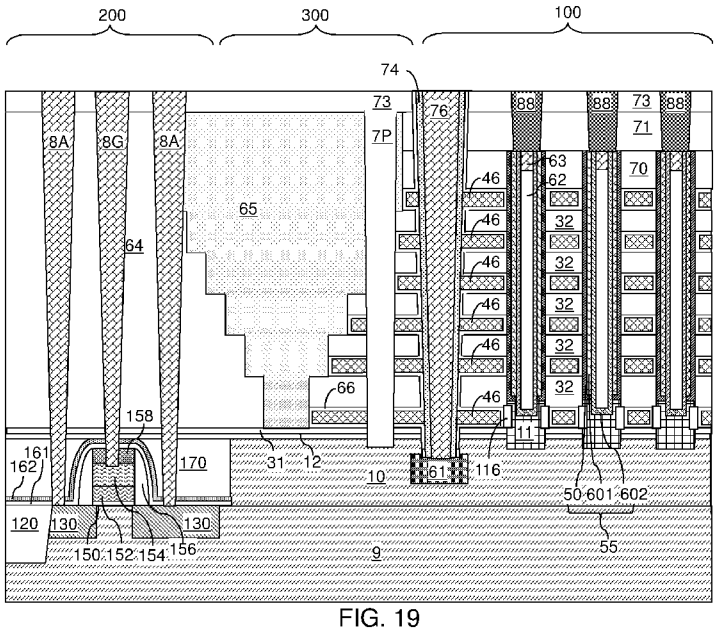


FIG. 19

(57) **Abstract**: A silicon-containing nucleation layer can be employed to provide a self-aligned template for selective deposition of tungsten within backside recesses during formation of a three-dimensional memory device. The silicon-containing nucleation layer may remain as a silicon layer, converted into a tungsten silicide layer, or replaced with a tungsten nucleation layer. Tungsten deposition can proceed only on the surface of the silicon-containing nucleation layer or a layer derived therefrom in a subsequent tungsten deposition process.

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ROBUST NUCLEATION LAYERS FOR ENHANCED FLUORINE PROTECTION AND STRESS REDUCTION IN 3D NAND WORD LINES

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of priority to U.S. Provisional Application Serial No. 62/247,839, filed October 29, 2015 and U.S. Non-Provisional Application Serial No. 15/086,702, filed March 31, 2016, the entire contents of the foregoing applications are incorporated herein by reference.

FIELD

[0002] The present disclosure relates generally to the field of semiconductor devices and specifically to metal word lines of three-dimensional semiconductor devices, such as vertical NAND strings, and methods of making thereof.

BACKGROUND

[0003] Three-dimensional vertical NAND strings having one bit per cell are disclosed in an article by T. Endoh et al., titled "Novel Ultra High Density Memory With A Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell", IEDM Proc. (2001) 33-36.

SUMMARY

[0004] According to an aspect of the present disclosure, a method of manufacturing a semiconductor device is provided. A stack of alternating layers comprising insulating layers and sacrificial material layers is formed over a substrate. A plurality of memory openings is formed through the stack. Memory stack structures are formed in the plurality of memory openings. Each of the memory stack structures comprises, from outside to inside, a memory

material layer, a tunneling dielectric layer, and a semiconductor channel. A backside via trench is formed through the stack of alternating layers. Backside recesses by removing the sacrificial material layers selective to the memory stack structures employing an etchant introduced through the backside via trench. A silicon-containing nucleation layer is deposited in the backside recesses. At least one tungsten layer is deposited in the backside recesses after deposition of the silicon-containing nucleation layer. Control gate electrodes for the memory stack structures are formed at levels of the backside recesses. Each of the control gate electrodes comprises a portion of the at least one tungsten layer.

[0005] According to another aspect of the present disclosure, a three-dimensional memory device is provided, which comprises: a stack of alternating layers comprising insulating layers and electrically conductive layers and located over a substrate; a memory opening extending through the stack; and a memory stack structure located in the memory opening and comprising, from outside to inside, a memory material layer, a tunneling dielectric layer, and a semiconductor channel. Each of the electrically conductive layers comprises: a silicon-containing-material layer; and at least one tungsten layer embedded in the silicon-containing-material layer and contacting horizontal surfaces and an outer sidewall of the silicon-containing material layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1 is a vertical cross-sectional view of an exemplary structure after formation of a stack including an alternating plurality of material layers and memory openings extending through the stack according to an embodiment of the present disclosure.

[0007] FIGS. 2A – 2H are sequential vertical cross-sectional views of a memory opening within the exemplary structure during various processing steps employed to form a memory

stack structure according to an embodiment of the present disclosure.

[0008] FIG. 3 is a vertical cross-sectional view of the exemplary structure after formation of memory stack structures according to an embodiment of the present disclosure.

[0009] FIG. 4 is a vertical cross-sectional view of the exemplary structure after formation of a stepped terrace and a retro-stepped dielectric material portion according to an embodiment of the present disclosure.

[0010] FIG. 5A is a vertical cross-sectional view of the exemplary structure after formation of a backside via trench according to an embodiment of the present disclosure.

[0011] FIG. 5B is a partial see-through top-down view of the exemplary structure of FIG. 5A. The vertical plane A – A' is the plane of the vertical cross-sectional view of FIG. 5A.

[0012] FIG. 6 is a vertical cross-sectional view of the exemplary structure after formation of backside recesses according to an embodiment of the present disclosure.

[0013] FIG. 7 is a vertical cross-sectional view of the exemplary structure after formation of a backside blocking dielectric layer according to an embodiment of the present disclosure.

[0014] FIG. 8 is a vertical cross-sectional view of the backside recess region of the exemplary structure after formation of conductive material layers according to an embodiment of the present disclosure.

[0015] FIG. 9 is a vertical cross-sectional view of the exemplary structure after formation of electrically conductive layers by patterning the conductive material layers according to an embodiment of the present disclosure.

[0016] FIGS. 10A – 10E are sequential vertical cross-sectional views of the exemplary structure during formation of first exemplary electrically conductive layers according to a first embodiment of the present disclosure.

[0017] FIGS. 10F and 10G are variations of the first exemplary electrically conductive

layers according to the first embodiment of the present disclosure.

[0018] FIGS. 11A – 11C are sequential vertical cross-sectional views of the exemplary structure during formation of second exemplary electrically conductive layers according to a second embodiment of the present disclosure.

[0019] FIGS. 12A – 12D are sequential vertical cross-sectional views of the exemplary structure during formation of third exemplary electrically conductive layers according to a third embodiment of the present disclosure.

[0020] FIGS. 13A – 13C are sequential vertical cross-sectional views of the exemplary structure during formation of fourth exemplary electrically conductive layers according to a fourth embodiment of the present disclosure.

[0021] FIGS. 14A and 14B are sequential vertical cross-sectional views of the exemplary structure during formation of fifth exemplary electrically conductive layers according to a fifth embodiment of the present disclosure.

[0022] FIGS. 15A – 15D are sequential vertical cross-sectional views of the exemplary structure during formation of sixth exemplary electrically conductive layers according to a sixth embodiment of the present disclosure.

[0023] FIGS. 16A and 16B are sequential vertical cross-sectional views of the exemplary structure during formation of seventh exemplary electrically conductive layers according to a seventh embodiment of the present disclosure.

[0024] FIGS. 17A – 17E are sequential vertical cross-sectional views of a region around a pair of memory stack structures during formation of the seventh exemplary electrically conductive layers according to the seventh embodiment of the present disclosure.

[0025] FIG. 17F is a vertical cross-sectional view of a region around a pair of memory stack structures after formation of a variation of the seventh exemplary electrically

conductive layers according to the seventh embodiment of the present disclosure.

[0026] FIG. 18 is a vertical cross-sectional view of the exemplary structure after formation of a backside contact via structure according to an embodiment of the present disclosure.

[0027] FIG. 19 is a vertical cross-sectional view of the exemplary structure after formation of additional contact via structures according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0028] As discussed above, the present disclosure is directed to three-dimensional memory structures, such as vertical NAND strings and other three-dimensional devices, and methods of making thereof, the various aspects of which are described below. The embodiments of the disclosure can be employed to form various structures including a multilevel memory structure, non-limiting examples of which include semiconductor devices such as three-dimensional monolithic memory array devices comprising a plurality of NAND memory strings.

[0029] The present inventors realized that fluorine present in metal line structures can diffuse during manufacture or operation of a semiconductor device to cause various performance and reliability issues such as fluorine-induced electrical shorts. For example, fluorine present in word lines of a three-dimensional memory device can diffuse to a dielectric material such as silicon oxide and cause voids, which can be filled with electromigrated or diffused materials to generate electrical shorts. Therefore, embodiments of the present disclosure provide at least one fluorine-free word line layer in the memory device.

[0030] The drawings are not drawn to scale. Multiple instances of an element may be duplicated where a single instance of the element is illustrated, unless absence of duplication of elements is expressly described or clearly indicated otherwise. Ordinals such as "first," "second," and "third" are employed merely to identify similar elements, and different ordinals may be employed across the specification and the claims of the instant disclosure. As used herein, a first element located "on" a second element can be located on the exterior side of a surface of the second element or on the interior side of the second element. As used herein, a first element is located "directly on" a second element if there exist a physical contact between a surface of the first element and a surface of the second element.

[0031] As used herein, a "layer" refers to a material portion including a region having a thickness. A layer may extend over the entirety of an underlying or overlying structure, or may have an extent less than the extent of an underlying or overlying structure. Further, a layer may be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer may be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer may extend horizontally, vertically, and/or along a tapered surface. A substrate may be a layer, may include one or more layers therein, and/or may have one or more layer thereupon, thereabove, and/or therebelow.

[0032] A monolithic three-dimensional memory array is one in which multiple memory levels are formed above a single substrate, such as a semiconductor wafer, with no intervening substrates. The term "monolithic" means that layers of each level of the array are directly deposited on the layers of each underlying level of the array. In contrast, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device. For example, non-monolithic stacked memories have been

constructed by forming memory levels on separate substrates and vertically stacking the memory levels, as described in U.S. Patent No. 5,915,167 titled "Three-dimensional Structure Memory." The substrates may be thinned or removed from the memory levels before bonding, but as the memory levels are initially formed over separate substrates, such memories are not true monolithic three-dimensional memory arrays. The various three-dimensional memory devices of the present disclosure include a monolithic three-dimensional NAND string memory device, and can be fabricated employing the various embodiments described herein.

[0033] Referring to FIG. 1, an exemplary structure according to an embodiment of the present disclosure is illustrated, which can be employed, for example, to fabricate a device structure containing vertical NAND memory devices. The exemplary structure includes a substrate, which can be a semiconductor substrate. The substrate can include a substrate semiconductor layer 9. The substrate semiconductor layer 9 is a semiconductor material layer, and can include at least one elemental semiconductor material (e.g., single crystal silicon wafer), at least one III-V compound semiconductor material, at least one II-VI compound semiconductor material, at least one organic semiconductor material, or other semiconductor materials known in the art. The substrate can have a major surface 7, which can be, for example, a topmost surface of the substrate semiconductor layer 9. The major surface 7 can be a semiconductor surface. In one embodiment, the major surface 7 can be a single crystalline semiconductor (e.g., silicon) surface.

[0034] As used herein, a "semiconductor material" refers to a material having electrical conductivity in the range from 1.0×10^{-6} S/cm to 1.0×10^{5} S/cm, and is capable of producing a doped material having electrical conductivity in a range from 1.0 S/cm to 1.0×10^{5} S/cm upon suitable doping with an electrical dopant. As used herein, an "electrical dopant" refers

to a p-type dopant that adds a hole to a valence band within a band structure, or an n-type dopant that adds an electron to a conduction band within a band structure. As used herein, a "conductive material" refers to a material having electrical conductivity greater than 1.0×10^5 S/cm. As used herein, an "insulating material" or a "dielectric material" refers to a material having electrical conductivity less than 1.0×10^{-6} S/cm. All measurements for electrical conductivities are made at the standard condition. Optionally, at least one doped well (not expressly shown) can be formed within the substrate semiconductor layer 9.

[0035] At least one semiconductor device for a peripheral circuitry can be formed on a portion of the substrate semiconductor layer 9. The at least one semiconductor device can include, for example, field effect transistors. For example, at least one shallow trench isolation structure 120 can be formed by etching portions of the substrate semiconductor layer 9 and depositing a dielectric material therein. A gate dielectric layer, at least one gate conductor layer, and a gate cap dielectric layer can be formed over the substrate semiconductor layer 9, and can be subsequently patterned to form at least one gate structure (150, 152, 154, 158), each of which can include a gate dielectric 150, at least one gate electrode (152, 154), and a gate cap dielectric. A gate electrode (152, 154) may include a stack of a first gate electrode portion 152 and a second gate electrode portion 154. At least one gate spacer 156 can be formed around the at least one gate structure (150, 152, 154, 158) by depositing and anisotropically etching a conformal dielectric layer. Active regions 130 can be formed in upper portions of the substrate semiconductor layer 9, for example, by introducing electrical dopants employing the at least one gate structure (150, 152, 154, 158) as masking structures. Additional masks may be employed as needed. The active region 130 can include source regions and drain regions of field effect transistors. A first dielectric liner 161 and a second dielectric liner 162 can be optionally formed. Each of the first and second

dielectric liners (161, 162) can comprise a silicon oxide layer, a silicon nitride layer, and/or a dielectric metal oxide layer. In an illustrative example, the first dielectric liner 161 can be a silicon oxide layer, and the second dielectric liner 162 can be a silicon nitride layer. The least one semiconductor device for the peripheral circuitry can contain a driver circuit for memory devices to be subsequently formed, which can include at least one NAND device.

[0036] A dielectric material such as silicon oxide can be deposited over the at least one semiconductor device, and can be subsequently planarized to form a planarization dielectric layer 170. In one embodiment the planarized top surface of the planarization dielectric layer 170 can be coplanar with a top surface of the dielectric liners (161, 162). Subsequently, the planarization dielectric layer 170 and the dielectric liners (161, 162) can be removed from an area to physically expose a top surface of the substrate semiconductor layer 9.

[0037] An optional doped well layer 10 can be formed on the top surface of the substrate semiconductor layer 9 by deposition of a single crystalline semiconductor material, for example, single crystal silicon, by selective epitaxy. The deposited semiconductor material can be the same as, or can be different from, the semiconductor material of the substrate semiconductor layer 9. The deposited semiconductor material can be any material that can be employed for the semiconductor substrate layer 9 as described above. The single crystalline semiconductor material of the doped well layer 10 can be in epitaxial alignment with the single crystalline structure of the substrate semiconductor layer 9. Portions of the deposited semiconductor material located above the top surface of the planarization dielectric layer 170 can be removed, for example, by chemical mechanical planarization (CMP). In this case, the doped well layer 10 can have a top surface that is coplanar with the top surface of the planarization dielectric layer 170.

[0038] Optionally, a dielectric pad layer 12 can be formed above the doped well layer 10

and the planarization dielectric layer 170. The dielectric pad layer 12 can be, for example, silicon oxide layer. The thickness of the dielectric pad layer 12 can be in a range from 3 nm to 30 nm, although lesser and greater thicknesses can also be employed.

[0039] A dielectric cap layer 31 can be optionally formed. The dielectric cap layer 31 includes a dielectric material, and can be formed directly on top surfaces of the gate electrodes. Exemplary materials that can be employed for the dielectric cap layer 31 include, but are not limited to, silicon oxide, a dielectric metal oxide, and silicon nitride (in case the material of second material layers to be subsequently formed is not silicon nitride). The dielectric cap layer 31 provides electrical isolation for the select gate electrodes.

[0040] A stack of an alternating plurality of first material layers (which can be insulating layers 32) and second material layers (which can be sacrificial material layer 42) is formed over the top surface of the substrate, which can be, for example, on the top surface of the dielectric cap layer 31. As used herein, a "material layer" refers to a layer including a material throughout the entirety thereof. As used herein, an alternating plurality of first elements and second elements refers to a structure in which instances of the first elements and instances of the second elements alternate. Each instance of the first elements that is not an end element of the alternating plurality is adjoined by two instances of the second elements on both sides, and each instance of the second elements that is not an end element of the alternating plurality is adjoined by two instances of the first elements on both ends. The first elements may have the same thickness thereamongst, or may have different thicknesses. The second elements may have the same thickness thereamongst, or may have different thicknesses. The alternating plurality of first material layers and second material layers may begin with an instance of the first material layers or with an instance of the second material layers, and may end with an instance of the first material layers or with an instance of the

second material layers. In one embodiment, an instance of the first elements and an instance of the second elements may form a unit that is repeated with periodicity within the alternating plurality.

[0041] Each first material layer includes a first material, and each second material layer includes a second material that is different from the first material. In one embodiment, each first material layer can be an insulating layer 32, and each second material layer can be a sacrificial material layer. In this case, the stack can include an alternating plurality of insulating layers 32 and sacrificial material layers 42, and constitutes a prototype stack of alternating layers comprising insulating layers 32 and sacrificial material layers 42. As used herein, a "prototype" structure or an "in-process" structure refers to a transient structure that is subsequently modified in the shape or composition of at least one component therein.

[0042] The stack of the alternating plurality is herein referred to as an alternating stack (32, 42). In one embodiment, the alternating stack (32, 42) can include insulating layers 32 composed of the first material, and sacrificial material layers 42 composed of a second material different from that of insulating layers 32. The first material of the insulating layers 32 can be at least one insulating material. As such, each insulating layer 32 can be an insulating material layer. Insulating materials that can be employed for the insulating layers 32 include, but are not limited to, silicon oxide (including doped or undoped silicate glass), silicon nitride, silicon oxynitride, organosilicate glass (OSG), spin-on dielectric materials, dielectric metal oxides that are commonly known as high dielectric constant (high-k) dielectric oxides (e.g., aluminum oxide, hafnium oxide, etc.) and silicates thereof, dielectric metal oxynitrides and silicates thereof, and organic insulating materials. In one embodiment, the first material of the insulating layers 32 can be silicon oxide.

[0043] The second material of the sacrificial material layers 42 is a sacrificial material

that can be removed selective to the first material of the insulating layers 32. As used herein, a removal of a first material is "selective to" a second material if the removal process removes the first material at a rate that is at least twice the rate of removal of the second material. The ratio of the rate of removal of the first material to the rate of removal of the second material is herein referred to as a "selectivity" of the removal process for the first material with respect to the second material.

[0044] The sacrificial material layers 42 may comprise an insulating material, a semiconductor material, or a conductive material. The second material of the sacrificial material layers 42 can be subsequently replaced with electrically conductive electrodes which can function, for example, as control gate electrodes of a vertical NAND device. Non-limiting examples of the second material include silicon nitride, an amorphous semiconductor material (such as amorphous silicon), and a polycrystalline semiconductor material (such as polysilicon). In one embodiment, the sacrificial material layers 42 can be spacer material layers that comprise silicon nitride or a semiconductor material including at least one of silicon and germanium.

[0045] In one embodiment, the insulating layers 32 can include silicon oxide, and sacrificial material layers can include silicon nitride sacrificial material layers. The first material of the insulating layers 32 can be deposited, for example, by chemical vapor deposition (CVD). For example, if silicon oxide is employed for the insulating layers 32, tetraethyl orthosilicate (TEOS) can be employed as the precursor material for the CVD process. The second material of the sacrificial material layers 42 can be formed, for example, CVD or atomic layer deposition (ALD).

[0046] The sacrificial material layers 42 can be suitably patterned so that conductive material portions to be subsequently formed by replacement of the sacrificial material layers

42 can function as electrically conductive electrodes, such as the control gate electrodes of the monolithic three-dimensional NAND string memory devices to be subsequently formed. The sacrificial material layers 42 may comprise a portion having a strip shape extending substantially parallel to the major surface 7 of the substrate.

[0047] The thicknesses of the insulating layers 32 and the sacrificial material layers 42 can be in a range from 20 nm to 50 nm, although lesser and greater thicknesses can be employed for each insulating layer 32 and for each sacrificial material layer 42. The number of repetitions of the pairs of an insulating layer 32 and a sacrificial material layer (e.g., a control gate electrode or a sacrificial material layer) 42 can be in a range from 2 to 1,024, and typically from 8 to 256, although a greater number of repetitions can also be employed. The top and bottom gate electrodes in the stack may function as the select gate electrodes. In one embodiment, each sacrificial material layer 42 in the alternating stack (32, 42) can have a uniform thickness that is substantially invariant within each respective sacrificial material layer 42.

[0048] Optionally, an insulating cap layer 70 can be formed over the alternating stack (32, 42). The insulating cap layer 70 includes a dielectric material that is different from the material of the sacrificial material layers 42. In one embodiment, the insulating cap layer 70 can include a dielectric material that can be employed for the insulating layers 32 as described above. The insulating cap layer 70 can have a greater thickness than each of the insulating layers 32. The insulating cap layer 70 can be deposited, for example, by chemical vapor deposition. In one embodiment, the insulating cap layer 70 can be a silicon oxide layer.

[0049] Subsequently, a lithographic material stack (not shown) including at least a photoresist layer can be formed over the insulating cap layer 70 and the alternating stack (32,

42), and can be lithographically patterned to form openings therein. The pattern in the lithographic material stack can be transferred through the insulating cap layer 70 and through entirety of the alternating stack (32, 42) by at least one anisotropic etch that employs the patterned lithographic material stack as an etch mask. Portions of the alternating stack (32, 42) underlying the openings in the patterned lithographic material stack are etched to form memory openings 49. In other words, the transfer of the pattern in the patterned lithographic material stack through the alternating stack (32, 42) forms the memory openings 49 that extend through the alternating stack (32, 42). The chemistry of the anisotropic etch process employed to etch through the materials of the alternating stack (32, 42) can alternate to optimize etching of the first and second materials in the alternating stack (32, 42). The anisotropic etch can be, for example, a series of reactive ion etches. Optionally, the dielectric cap layer 31 may be used as an etch stop layer between the alternating stack (32, 42) and the substrate. The sidewalls of the memory openings 49 can be substantially vertical, or can be tapered. The patterned lithographic material stack can be subsequently removed, for example, by ashing.

[0050] The memory openings 49 are formed through the dielectric cap layer 31 and the dielectric pad layer 12 so that the memory openings 49 extend from the top surface of the alternating stack (32, 42) to the top surface of the doped well layer 10 within the substrate between the lower select gate electrodes. In one embodiment, an overetch into the doped well layer 10 may be optionally performed after the top surface of the doped well layer 10 is physically exposed at a bottom of each memory opening 49. The overetch may be performed prior to, or after, removal of the lithographic material stack. In other words, the recessed surfaces of the doped well layer 10 may be vertically offset from the undressed top surfaces of the doped well layer 10 by a recess depth. The recess depth can be, for example, in a

range from 1 nm to 50 nm, although lesser and greater recess depths can also be employed. The overetch is optional, and may be omitted. If the overetch is not performed, the bottom surface of each memory opening 49 can be coplanar with the topmost surface of the doped well layer 10. Each of the memory openings 49 can include a sidewall (or a plurality of sidewalls) that extends substantially perpendicular to the topmost surface of the substrate. The region in which the array of memory openings 49 is formed is herein referred to as a device region. The substrate semiconductor layer 9 and the doped well layer 10 collectively constitutes a substrate (9, 10), which can be a semiconductor substrate. Alternatively, the doped well layer 10 may be omitted, and the memory openings 49 can be extend to a top surface of or into the substrate semiconductor layer 9.

[0051] A memory stack structure can be formed in each of the memory opening employing various embodiments of the present disclosure. FIGS. 2A – 2H illustrate sequential vertical cross-sectional views of a memory opening within the exemplary structure during formation of an exemplary memory stack structure according to a embodiment of the present disclosure. Formation of the exemplary memory stack structure can be performed within each of the memory openings 49 in the exemplary structure illustrated in FIG. 1.

[0052] Referring to FIG. 2A, a memory opening 49 in the exemplary structure of FIG. 1 is illustrated in a magnified view. The memory opening 49 extends through the insulating cap layer 70, the alternating stack (32, 42), the dielectric cap layer 31, the dielectric pad layer 12, and optionally into an upper portion of the doped well layer 10. The recess depth of the bottom surface of each memory opening with respect to the top surface of the doped well layer 10 can be in a range from 0 nm to 30 nm, although greater recess depths can also be employed. Optionally, the sacrificial material layers 42 can be laterally recessed partially to form lateral recesses (not shown), for example, by an isotropic etch.

[0053] Referring to FIG. 2B, an optional epitaxial channel portion 11 can be formed at the bottom portion of each memory opening 49, for example, by selective epitaxy. Each epitaxial channel portion 11 comprises a single crystalline semiconductor material in epitaxial alignment with the single crystalline semiconductor material of the doped well layer 10. In one embodiment, the epitaxial channel portion 11 can be doped with electrical dopants of the same conductivity type as the doped well layer 10. In one embodiment, the top surface of each epitaxial channel portion 11 can be formed above a horizontal plane including the top surface of a sacrificial material layer 42. In this case, at least one source select gate electrode can be subsequently formed by replacing each sacrificial material layer 42 located below the horizontal plane including the top surfaces of the epitaxial channel portions 11 with a respective conductive material layer.

[0054] Referring to FIG. 2C, a series of layers including at least one optional blocking dielectric layer (501L, 503L), a memory material layer 504L, a tunneling dielectric layer 506L, and an optional first semiconductor channel layer 601L can be sequentially deposited in the memory openings 49. The at least one blocking dielectric layer (501L, 503L) can include, for example, a first blocking dielectric layer 501L and a second blocking dielectric layer 503L.

[0055] The first blocking dielectric layer 501L can be deposited on the sidewalls of each memory opening 49 by a conformal deposition method. The first blocking dielectric layer 501L includes a dielectric material, which can be a dielectric metal oxide. As used herein, a dielectric metal oxide refers to a dielectric material that includes at least one metallic element and at least oxygen. The dielectric metal oxide may consist essentially of the at least one metallic element and oxygen, or may consist essentially of the at least one metallic element, oxygen, and at least one non-metallic element such as nitrogen. In one embodiment, the first

blocking dielectric layer 501L can include a dielectric metal oxide having a dielectric constant greater than 7.9, i.e., having a dielectric constant greater than the dielectric constant of silicon nitride.

[0056] Non-limiting examples of dielectric metal oxides include aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), lanthanum oxide (LaO_2), yttrium oxide (Y_2O_3), tantalum oxide (Ta_2O_5), silicates thereof, nitrogen-doped compounds thereof, alloys thereof, and stacks thereof. The first blocking dielectric layer 501L can be deposited, for example, by chemical vapor deposition (CVD), atomic layer deposition (ALD), pulsed laser deposition (PLD), liquid source misted chemical deposition, or a combination thereof. The thickness of the first blocking dielectric layer 501L can be in a range from 1 nm to 20 nm, although lesser and greater thicknesses can also be employed. The first blocking dielectric layer 501L can subsequently function as a dielectric material portion that blocks leakage of stored electrical charges to control gate electrodes. In one embodiment, the first blocking dielectric layer 501L includes aluminum oxide.

[0057] The second blocking dielectric layer 503L can be formed on the first blocking dielectric layer 501L. The second blocking dielectric layer 503L can include a dielectric material that is different from the dielectric material of the first blocking dielectric layer 501L. In one embodiment, the second blocking dielectric layer 503L can include silicon oxide, a dielectric metal oxide having a different composition than the first blocking dielectric layer 501L, silicon oxynitride, silicon nitride, or a combination thereof. In one embodiment, the second blocking dielectric layer 503L can include silicon oxide. The second blocking dielectric layer 503L can be formed by a conformal deposition method such as low pressure chemical vapor deposition, atomic layer deposition, or a combination thereof. The thickness of the second blocking dielectric layer 503L can be in a range from 1 nm to 20

nm, although lesser and greater thicknesses can also be employed. Alternatively, the first blocking dielectric layer 501L and/or the second blocking dielectric layer 503L can be omitted, and a blocking dielectric layer can be formed after formation of backside recesses on surfaces of memory films to be subsequently formed.

[0058] Subsequently, the memory material layer 504L, the tunneling dielectric layer 506L, and the optional first semiconductor channel layer 601L can be sequentially formed. In one embodiment, the memory material layer 504L can be a charge trapping material including a dielectric charge trapping material, which can be, for example, silicon nitride. Alternatively, the memory material layer 504L can include a conductive material such as doped polysilicon or a metallic material that is patterned into multiple electrically isolated portions (e.g., floating gates), for example, by being formed within lateral recesses into sacrificial material layers 42. In one embodiment, the memory material layer 504L includes a silicon nitride layer.

[0059] The memory material layer 504L can be formed as a single memory material layer of homogeneous composition, or can include a stack of multiple memory material layers. The multiple memory material layers, if employed, can comprise a plurality of spaced-apart floating gate material layers that contain conductive materials (e.g., metal such as tungsten, molybdenum, tantalum, titanium, platinum, ruthenium, and alloys thereof, or a metal silicide such as tungsten silicide, molybdenum silicide, tantalum silicide, titanium silicide, nickel silicide, cobalt silicide, or a combination thereof) and/or semiconductor materials (e.g., polycrystalline or amorphous semiconductor material including at least one elemental semiconductor element or at least one compound semiconductor material). Alternatively or additionally, the memory material layer 504L may comprise an insulating charge trapping material, such as one or more silicon nitride segments. Alternatively, the memory material

layer 504L may comprise conductive nanoparticles such as metal nanoparticles, which can be, for example, ruthenium nanoparticles. The memory material layer 504L can be formed, for example, by chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), or any suitable deposition technique for storing electrical charges therein. The thickness of the memory material layer 504L can be in a range from 2 nm to 20 nm, although lesser and greater thicknesses can also be employed.

[0060] The tunneling dielectric layer 506L includes a dielectric material through which charge tunneling can be performed under suitable electrical bias conditions. The charge tunneling may be performed through hot-carrier injection or by Fowler-Nordheim tunneling induced charge transfer depending on the mode of operation of the monolithic three-dimensional NAND string memory device to be formed. The tunneling dielectric layer 506L can include silicon oxide, silicon nitride, silicon oxynitride, dielectric metal oxides (such as aluminum oxide and hafnium oxide), dielectric metal oxynitride, dielectric metal silicates, alloys thereof, and/or combinations thereof. In one embodiment, the tunneling dielectric layer 506L can include a stack of a first silicon oxide layer, a silicon oxynitride layer, and a second silicon oxide layer, which is commonly known as an ONO stack. In one embodiment, the tunneling dielectric layer 506L can include a silicon oxide layer that is substantially free of carbon or a silicon oxynitride layer that is substantially free of carbon. The thickness of the tunneling dielectric layer 506L can be in a range from 2 nm to 20 nm, although lesser and greater thicknesses can also be employed.

[0061] The optional first semiconductor channel layer 601L includes a semiconductor material such as at least one elemental semiconductor material, at least one III-V compound semiconductor material, at least one II-VI compound semiconductor material, at least one organic semiconductor material, or other semiconductor materials known in the art. In one

embodiment, the first semiconductor channel layer 601L includes amorphous silicon or polysilicon. The first semiconductor channel layer 601L can be formed by a conformal deposition method such as low pressure chemical vapor deposition (LPCVD). The thickness of the first semiconductor channel layer 601L can be in a range from 2 nm to 10 nm, although lesser and greater thicknesses can also be employed. A cavity 49' is formed in the volume of each memory opening 49 that is not filled with the deposited material layers (501L, 503L, 504L, 506l, 601L).

[0062] Referring to FIG. 2D, the optional first semiconductor channel layer 601L, the tunneling dielectric layer 506L, the memory material layer 504L, the at least one blocking dielectric layer (501L, 503L) are sequentially anisotropically etched employing at least one anisotropic etch process. The portions of the first semiconductor channel layer 601L, the tunneling dielectric layer 506L, the memory material layer 504L, and the at least one blocking dielectric layer (501L, 503L) located above the top surface of the insulating cap layer 70 can be removed by the at least one anisotropic etch process. Further, the horizontal portions of the first semiconductor channel layer 601L, the tunneling dielectric layer 506L, the memory material layer 504L, and the at least one blocking dielectric layer (501L, 503L) at a bottom of each cavity 49' can be removed to form openings in remaining portions thereof. Each of the first semiconductor channel layer 601L, the tunneling dielectric layer 506L, the memory material layer 504L, and the at least one blocking dielectric layer (501L, 503L) can be etched by anisotropic etch process.

[0063] Each remaining portion of the first semiconductor channel layer 601L constitutes a first semiconductor channel portion 601. Each remaining portion of the tunneling dielectric layer 506L constitutes a tunneling dielectric 506. Each remaining portion of the memory material layer 504L is herein referred to as a charge storage element 504. In one

embodiment, the charge storage element 504 can be a continuous layer, i.e., can be a charge storage layer. Each remaining portion of the second blocking dielectric layer 503L is herein referred to as a second blocking dielectric 503. Each remaining portion of the first blocking dielectric layer 501L is herein referred to as a first blocking dielectric 501. A surface of the epitaxial channel portion 11 can be physically exposed underneath the opening through the first semiconductor channel portion 601, the tunneling dielectric 506, the charge storage element 504, and the at least one blocking dielectric (501, 503). Optionally, the physically exposed portion of the epitaxial channel portion 11 can be vertically recessed. A tunneling dielectric 506 is surrounded by a charge storage element 504. The charge storage element 504 can comprise a charge trapping material or a floating gate material.

[0064] The set of the tunneling dielectric 506, the charge storage element 504, the optional second blocking dielectric 503, and the optional first blocking dielectric 501 collectively constitutes a memory film 50. In one embodiment, the first semiconductor channel portion 601, the tunneling dielectric 506, the charge storage element 504, the second blocking dielectric 503, and the first blocking dielectric 501 can have vertically coincident sidewalls. As used herein, a first surface is "vertically coincident" with a second surface if there exists a vertical plane including both the first surface and the second surface. Such a vertical plane may, or may not, have a horizontal curvature, but does not include any curvature along the vertical direction, i.e., extends straight up and down.

[0065] Referring to FIG. 2E, a second semiconductor channel layer 602L can be deposited directly on the semiconductor surface of the epitaxial channel portion 11 over the substrate (9, 10), and directly on the first semiconductor channel portion 601. The second semiconductor channel layer 602L includes a semiconductor material such as at least one elemental semiconductor material, at least one III-V compound semiconductor material, at

least one II-VI compound semiconductor material, at least one organic semiconductor material, or other semiconductor materials known in the art. In one embodiment, the second semiconductor channel layer 602L includes amorphous silicon or polysilicon. The second semiconductor channel layer 602L can be formed by a conformal deposition method such as low pressure chemical vapor deposition (LPCVD). The thickness of the second semiconductor channel layer 602L can be in a range from 2 nm to 10 nm, although lesser and greater thicknesses can also be employed. The second semiconductor channel layer 602L may partially fill the cavity 49' in each memory opening, or may fully fill the cavity in each memory opening.

[0066] The materials of the first semiconductor channel portion 601 and the second semiconductor channel layer 602L are collectively referred to as a semiconductor channel material. In other words, the semiconductor channel material is a set of all semiconductor material in the first semiconductor channel portion 601 and the second semiconductor channel layer 602L.

[0067] Referring to FIG. 2F, in case the cavity 49' in each memory opening is not completely filled by the second semiconductor channel layer 602L, a dielectric core layer 62L can be deposited in the cavity 49' to fill any remaining portion of the cavity 49' within each memory opening. The dielectric core layer 62L includes a dielectric material such as silicon oxide or organosilicate glass. The dielectric core layer 62L can be deposited by a conformal deposition method such as low pressure chemical vapor deposition (LPCVD), or by a self-planarizing deposition process such as spin coating.

[0068] Referring to FIG. 2G, the horizontal portion of the dielectric core layer 62L can be removed, for example, by a recess etch from above the top surface of the insulating cap layer 70. Further, the horizontal portion of the second semiconductor channel layer 602L located

above the top surface of the insulating cap layer 70 can be removed by a planarization process, which can employ a recess etch or chemical mechanical planarization (CMP). Each remaining portion of the second semiconductor channel layer 602L within a memory opening constitutes a second semiconductor channel portion 602.

[0069] Each adjoining pair of a first semiconductor channel portion 601 and a second semiconductor channel portion 602 can collectively form a semiconductor channel 60 through which electrical current can flow when a vertical NAND device including the semiconductor channel 60 is turned on. A tunneling dielectric 506 is surrounded by a charge storage element 504, and laterally surrounds a portion of the semiconductor channel 60. Each adjoining set of an optional first blocking dielectric 501, an optional second blocking dielectric 503, a charge storage element 504, and a tunneling dielectric 506 collectively constitute a memory film 50, which can store electrical charges with a macroscopic retention time. In some embodiments, a first blocking dielectric 501 and/or a second blocking dielectric 503 may not be present in the memory film 50 at this step, and a blocking dielectric may be subsequently formed after formation of backside recesses. As used herein, a macroscopic retention time refers to a retention time suitable for operation of a memory device as a permanent memory device such as a retention time in excess of 24 hours.

[0070] The top surface of the remaining portion of the dielectric core layer 62L can be further recessed within each memory opening, for example, by a recess etch to a depth that is located between the top surface of the insulating cap layer 70 and the bottom surface of the insulating cap layer 70. Each remaining portion of the dielectric core layer 62L constitutes a dielectric core 62.

[0071] Referring to FIG. 2H, drain regions 63 can be formed by depositing a doped semiconductor material within each recessed region above the dielectric cores 62. The doped

semiconductor material can be, for example, doped polysilicon. Excess portions of the deposited semiconductor material can be removed from above the top surface of the insulating cap layer 70, for example, by chemical mechanical planarization (CMP) or a recess etch to form the drain regions 63.

[0072] The exemplary memory stack structure can be embedded into the exemplary structure illustrated in FIG. 1. FIG. 3 illustrates the exemplary structure that incorporates multiple instances of the exemplary memory stack structure of FIG. 2H. The exemplary structure includes a semiconductor device, which comprises a stack (32, 42) including an alternating plurality of material layers (e.g., the sacrificial material layers 42) and insulating layers 32 located over a semiconductor substrate (9, 10), and a memory opening extending through the stack (32, 42). The semiconductor device further comprises a memory film 50 and semiconductor channel 60 vertically extending from a bottommost layer (e.g., the bottommost sacrificial material layer 42) of the stack to a topmost layer (e.g., the topmost sacrificial material layer 42) of the stack. The memory film 50 contacts a sidewall of the memory opening 49 and the semiconductor channel 60 contacts the epitaxial channel portion 11 (or the doped well layer 10 if channel portion 11 is omitted).

[0073] Referring to FIG. 4, an optional first contact level dielectric layer 71 can be formed over the substrate (9, 10). As an optional structure, the first contact level dielectric layer 71 may, or may not, be formed. In case the first contact level dielectric layer 71 is formed, the first contact level dielectric layer 71 includes a dielectric material such as silicon oxide, silicon nitride, silicon oxynitride, porous or non-porous organosilicate glass (OSG), or a combination thereof. If an organosilicate glass is employed, the organosilicate glass may, or may not, be doped with nitrogen. The first contact level dielectric layer 71 can be formed over a horizontal plane including the top surface of the insulating cap layer 70 and the top

surfaces of the drain regions 63. The first contact level dielectric layer 71 can be deposited by chemical vapor deposition, atomic layer deposition (ALD), spin-coating, or a combination thereof. The thickness of the first contact level dielectric layer 71 can be in a range from 10 nm to 300 nm, although lesser and greater thicknesses can also be employed.

[0074] In one embodiment, the first contact level dielectric layer 71 can be formed as a dielectric material layer having a uniform thickness throughout. The first contact level dielectric layer 71 may be formed as a single dielectric material layer, or can be formed as a stack of a plurality of dielectric material layers. Alternatively, formation of the first contact level dielectric layer 71 may be merged with formation of at least one line level dielectric layer (not shown). While the present disclosure is described employing an embodiment in which the first contact level dielectric layer 71 is a structure separate from an optional second contact level dielectric layer or at least one line level dielectric layer to be subsequently deposited, embodiments in which the first contact level dielectric layer 71 and at least one line level dielectric layer are formed at a same processing step, and/or as a same material layer, are expressly contemplated herein.

[0075] Optionally, a portion of the alternating stack (32, 42) can be removed, for example, by applying and patterning a photoresist layer with an opening and by transferring the pattern of the opening through the alternating stack (32, 42) employing an etch such as an anisotropic etch. An optional trench extending through the entire thickness of the alternating stack (32, 42) can be formed within an area that includes a peripheral device region 200 and a portion of a contact region 300, which is adjacent to a device region 100. The device region 100 includes an array of memory stack structures 55 each of which contains a memory film 50 and a semiconductor channel 60. Subsequently, the trench can optionally be filled with an optional dielectric material such as silicon oxide. Excess portions of the dielectric material

can be removed from above the top surface of the first contact level dielectric layer 71 by a planarization process such as chemical mechanical planarization and/or a recess etch. The top surfaces of the first contact level dielectric layer 71 can be employed as a stopping surface during the planarization. The remaining dielectric material in the trench constitutes an optional dielectric material portion 64.

[0076] A stepped cavity can be formed within the contact region 300, which can straddle the dielectric material portion 64 and a portion of the alternating stack (32, 42). Alternatively, the dielectric material portion 64 may be omitted and the stepped cavity may be formed only in the exposed edge of the stack (32, 42). The stepped cavity can have various stepped surfaces such that the horizontal cross-sectional shape of the stepped cavity changes in steps as a function of the vertical distance from the top surface of the substrate (9, 10). In one embodiment, the stepped cavity can be formed by repetitively performing a set of processing steps. The set of processing steps can include, for example, an etch process of a first type that vertically increases the depth of a cavity by one or more levels, and an etch process of a second type that laterally expands the area to be vertically etched in a subsequent etch process of the first type. As used herein, a "level" of a structure including alternating plurality is defined as the relative position of a pair of a first material layer and a second material layer within the structure.

[0077] The dielectric material portion 64 can have stepped surfaces after formation of the stepped cavity, and a peripheral portion of the alternating stack (32, 42) can have stepped surfaces after formation of the stepped cavity. As used herein, "stepped surfaces" refer to a set of surfaces that include at least two horizontal surfaces and at least two vertical surfaces such that each horizontal surface is adjoined to a first vertical surface that extends upward from a first edge of the horizontal surface, and is adjoined to a second vertical surface that

extends downward from a second edge of the horizontal surface. A "stepped cavity" refers to a cavity having stepped surfaces.

[0078] A retro-stepped dielectric material portion 65 (i.e., an insulating fill material portion) can be formed in the stepped cavity by deposition of a dielectric material therein. A dielectric material such as silicon oxide can be deposited in the stepped cavity. Excess portions of the deposited dielectric material can be removed from above the top surface of the first contact level dielectric layer 71, for example, by chemical mechanical planarization (CMP). The remaining portion of the deposited dielectric material filling the stepped cavity constitutes the retro-stepped dielectric material portion 65. As used herein, a "retro-stepped" element refers to an element that has stepped surfaces and a horizontal cross-sectional area that increases monotonically as a function of a vertical distance from a top surface of a substrate on which the element is present. If silicon oxide is employed for the retro-stepped dielectric material portion 65, the silicon oxide of the retro-stepped dielectric material portion 65 may, or may not, be doped with dopants such as B, P, and/or F. In an alternative method, the steps in the stack (32, 42) and the retro-stepped dielectric material portion 65 may be formed before forming the memory openings 49 and the memory stack structures 55 (e.g., prior to the steps shown in FIGS. 1-3).

[0079] Referring to FIGS. 5A and 5B, at least one dielectric support pillar 7P may be optionally formed through the retro-stepped dielectric material portion 65 and/or through the first contact level dielectric layer 71 and/or through the alternating stack (32, 42). The plane A – A' in FIG. 5B corresponds to the plane of the vertical cross-sectional view of FIG. 5A. In one embodiment, the at least one dielectric support pillar 7P can be formed in the contact region 300, which is located adjacent to the device region 100. The at least one dielectric support pillar 7P can be formed, for example, by forming an opening extending through the

retro-stepped dielectric material portion 65 and/or through the alternating stack (32, 42) and at least to the top surface of the substrate (9, 10), and by filling the opening with a dielectric material that is resistant to the etch chemistry to be employed to remove the sacrificial material layers 42.

[0080] In one embodiment, the at least one dielectric support pillar can include silicon oxide and/or a dielectric metal oxide such as aluminum oxide. In one embodiment, the portion of the dielectric material that is deposited over the first contact level dielectric layer 71 concurrently with deposition of the at least one dielectric support pillar 7P can be present over the first contact level dielectric layer 71 as a second contact level dielectric layer 73. Each of the at least one dielectric support pillar 7P and the second contact level dielectric layer 73 is an optional structure. As such, the second contact level dielectric layer 73 may, or may not, be present over the insulating cap layer 70 and the retro-stepped dielectric material portion 65. The first contact level dielectric layer 71 and the second contact level dielectric layer 73 are herein collectively referred to as at least one contact level dielectric layer (71, 73). In one embodiment, the at least one contact level dielectric layer (71, 73) can include both the first and second contact level dielectric layers (71, 73), and optionally include any additional via level dielectric layer that can be subsequently formed. In another embodiment, the at least one contact level dielectric layer (71, 73) can include only the first contact level dielectric layer 71 or the second contact level dielectric layer 73, and optionally include any additional via level dielectric layer that can be subsequently formed. Alternatively, formation of the first and second contact level dielectric layers (71, 73) may be omitted, and at least one via level dielectric layer may be subsequently formed, i.e., after formation of a backside contact via structure.

[0081] The second contact level dielectric layer 73 and the at least one dielectric support

pillar 7P can be formed as a single continuous structure of integral construction, i.e., without any material interface therebetween. In another embodiment, the portion of the dielectric material that is deposited over the first contact level dielectric layer 71 concurrently with deposition of the at least one dielectric support pillar 7P can be removed, for example, by chemical mechanical planarization or a recess etch. In this case, the second contact level dielectric layer 73 is not present, and the top surface of the first contact level dielectric layer 71 can be physically exposed.

[0082] A photoresist layer (not shown) can be applied over the alternating stack (32, 42) and/or the retro-stepped dielectric material portion 65, and optionally over the and lithographically patterned to form at least one backside via trench 79 in an area in which formation of a backside contact via structure is desired. The pattern in the photoresist layer can be transferred through the alternating stack (32, 42) and/or the retro-stepped dielectric material portion 65 employing an anisotropic etch to form the at least one backside via trench 79, which extends at least to the top surface of the substrate (9, 10). In one embodiment, the at least one backside via trench 79 can include a source contact opening in which a source contact via structure can be subsequently formed.

[0083] Referring to FIG. 6, an etchant that selectively etches the second material of the sacrificial material layers 42 with respect to the first material of the insulating layers 32 can be introduced into the at least one backside via trench 79, for example, employing an etch process. Backside recesses 43 are formed in volumes from which the sacrificial material layers 42 are removed. The removal of the second material of the sacrificial material layers 42 can be selective to the first material of the insulating layers 32, the material of the at least one dielectric support pillar 7P, the material of the retro-stepped dielectric material portion 65, the semiconductor material of the doped well layer 10, and the material of the outermost

layer of the memory films 50. In one embodiment, the sacrificial material layers 42 can include silicon nitride, and the materials of the insulating layers 32, the at least one dielectric support pillar 7P, and the retro-stepped dielectric material portion 65 can be selected from silicon oxide and dielectric metal oxides. In another embodiment, the sacrificial material layers 42 can include a semiconductor material such as polysilicon, and the materials of the insulating layers 32, the at least one dielectric support pillar 7P, and the retro-stepped dielectric material portion 65 can be selected from silicon oxide, silicon nitride, and dielectric metal oxides. In this case, the depth of the at least one backside via trench 79 can be modified so that the bottommost surface of the at least one backside via trench 79 is located within the dielectric pad layer 12, i.e., to avoid physical exposure of the top surface of the semiconductor substrate layer 10.

[0084] The etch process that removes the second material selective to the first material and the outermost layer of the memory films 50 can be a wet etch process employing a wet etch solution, or can be a gas phase (dry) etch process in which the etchant is introduced in a vapor phase into the at least one backside via trench 79. For example, if the sacrificial material layers 42 include silicon nitride, the etch process can be a wet etch process in which the exemplary structure is immersed within a wet etch tank including phosphoric acid, which etches silicon nitride selective to silicon oxide, silicon, and various other materials employed in the art. The at least one dielectric support pillar 7P, the retro-stepped dielectric material portion 65, and the memory stack structures 55 provide structural support while the backside recesses 43 are present within volumes previously occupied by the sacrificial material layers 42.

[0085] Each backside recess 43 can be a laterally extending cavity having a lateral dimension that is greater than the vertical extent of the cavity. In other words, the lateral

dimension of each backside recess 43 can be greater than the height of the backside recess 43. A plurality of backside recesses 43 can be formed in the volumes from which the second material of the sacrificial material layers 42 is removed. The memory openings in which the memory stack structures 55 are formed are herein referred to as front side recesses or front side cavities in contrast with the backside recesses 43. In one embodiment, the device region 100 comprises an array of monolithic three-dimensional NAND strings having a plurality of device levels disposed above the substrate (9, 10). In this case, each backside recess 43 can define a space for receiving a respective word line of the array of monolithic three-dimensional NAND strings.

[0086] Each of the plurality of backside recesses 43 can extend substantially parallel to the top surface of the substrate (9, 10). A backside recess 43 can be vertically bounded by a top surface of an underlying insulating layer 32 and a bottom surface of an overlying insulating layer 32. In one embodiment, each backside recess 43 can have a uniform height throughout. Optionally, a backside blocking dielectric layer can be formed in the backside recesses.

[0087] Physically exposed surface portions of epitaxial channel portions 11 and the doped well layer 10 can be converted into dielectric material portions by thermal conversion and/or plasma conversion of the semiconductor materials into dielectric materials. For example, thermal conversion and/or plasma conversion can be employed to convert a surface portion of each epitaxial channel portion 11 into a dielectric spacer 116, and to convert each physically exposed surface portion of the doped well layer 10 into a sacrificial dielectric portion 616. In one embodiment, each dielectric spacer 116 can be topologically homeomorphic to a torus, i.e., generally ring-shaped. As used herein, an element is topologically homeomorphic to a torus if the shape of the element can be continuously

stretched without destroying a hole or forming a new hole into the shape of a torus. The dielectric spacers 116 include a dielectric material that includes the same semiconductor element as the epitaxial channel portions 11 and additionally includes at least one non-metallic element such as oxygen and/or nitrogen such that the material of the dielectric spacers 116 is a dielectric material. In one embodiment, the dielectric spacers 116 can include a dielectric oxide, a dielectric nitride, or a dielectric oxynitride of the semiconductor material of the epitaxial channel portions 11. Likewise, each sacrificial dielectric portion 616 includes a dielectric material that includes the same semiconductor element as the doped well region 10 and additionally includes at least one non-metallic element such as oxygen and/or nitrogen such that the material of the sacrificial dielectric portions 616 is a dielectric material. In one embodiment, the sacrificial dielectric portions 616 can include a dielectric oxide, a dielectric nitride, or a dielectric oxynitride of the semiconductor material of the doped well layer 10.

[0088] Referring to FIG. 7, an optional backside blocking dielectric layer 66 can be optionally formed. If formed, the backside blocking dielectric layer 66 can be deposited on the physically exposed surfaces of the backside recesses 43, the backside via trench 79, and on the topmost layer of the exemplary structure (such as the second contact level dielectric layer 73. The backside blocking dielectric layer 66 comprises a dielectric material that functions as a control gate dielectric for the control gates to be subsequently formed in the backside recesses 43. In case the at least one blocking dielectric layer (501, 503) is present within each memory opening, the backside blocking dielectric layer 66 is optional. In case the at least one blocking dielectric layer (501, 503) is omitted, the backside blocking dielectric layer 66 is present.

[0089] The optional backside blocking dielectric layer 66 comprises a dielectric material

such as a dielectric metal oxide, silicon oxide, silicon nitride, a nitrogen-including organosilicate glass, or a combination thereof. In one embodiment, the dielectric material of the backside blocking dielectric layer 66 can be a dielectric metal oxide such as aluminum oxide, a dielectric oxide of at least one transition metal element, a dielectric oxide of at least one Lanthanide element, a dielectric oxide of a combination of aluminum, at least one transition metal element, and/or at least one Lanthanide element. The backside blocking dielectric layer 66 can be deposited by a conformal deposition method such as chemical vapor deposition or atomic layer deposition. The thickness of the backside blocking dielectric layer 66 can be in a range from 1 nm to 10 nm, although lesser and greater thicknesses can also be employed. The optional backside blocking dielectric layer 66 can be formed on the sidewalls of the at least one backside via trench 79, horizontal surfaces and sidewalls of the insulating layers 32, the portions of the sidewall surfaces of the memory stack structures 55 that are physically exposed to the backside recesses 43, and a top surface of the doped well layer 10 (if formed prior to formation of the backside blocking dielectric layer 66). A backside cavity 79' is present within the portion of each backside via trench 79 that is not filled with the backside blocking dielectric layer 66. The backside blocking dielectric layer 66 is an optional structure. While the present disclosure is described employing embodiments in which the optional backside blocking dielectric layer 66 is present, each embodiment described herein has a counterpart embodiment in which the optional backside blocking dielectric layer 66 is omitted. Such variations are expressly contemplated herein.

[0090] Referring to FIG. 8, at least one conductive material can be deposited in remaining volumes of the backside recesses 43, and in some embodiments, peripheral volumes of the backside via trench 79. Portions of the at least one conductive material

deposited in the backside recesses 43 constitute electrically conductive layers 46. Depending on embodiments, additional portions of the at least one conductive material can be deposited in peripheral regions of the backside via cavity 79 and over the contact level dielectric layers (71, 73) to form a continuous conductive material layer 46L. In case the continuous conductive material layer 46L, an etch-back process can be performed to remove the continuous conductive material layer 46L from peripheral regions of the backside via cavity 79 and from above the contact level dielectric layers (71, 73) to provide a structure illustrated in FIG. 9. Alternatively, each electrically conductive layer 46 may be selectively deposited in the backside recesses 43 to form the structure of FIG. 9. In this case, the step shown in FIG. 8 may be omitted. Each electrically conductive layer 46 as provided at the processing step of FIG. 9 constitutes control gate electrodes for the memory stack structures 55. The electrically conductive layers 46 are formed at each level of the backside recesses 43 (i.e., at each level of the sacrificial material layers 42 of the alternating stack (32, 42) as originally provided). Each of the control gate electrodes comprises a portion of at least one tungsten layer.

[0091] Various methods can be employed to form the electrically conductive layers 46 illustrated in FIGS. 8 and 9. Embodiments of the present disclosure for forming the electrically conductive layers 46 at the processing steps of FIGS. 8 and 9 are described below.

[0092] FIGS. 10A – 10E illustrate the process of formation of first exemplary electrically conductive layers according to a first embodiment of the present disclosure. Referring to FIG. 10A, a region including a backside recess 43 between a memory film 50 and a backside cavity 79' is illustrated after formation of the optional backside blocking dielectric layer 66, which corresponds to the processing step of FIG. 8.

[0093] Referring to FIG. 10B, an optional conductive metal nitride layer 46A can be

deposited in the backside recesses 43. The conductive metal nitride layer 46A includes a conductive metal nitride such as TiN, TaN, WN, or alloys or stacks thereof. The conductive metal nitride layer 46A can be formed by a conformal deposition process such as chemical vapor deposition or atomic layer deposition. The thickness of the optional conductive metal nitride layer 46A can be in a range from 1 nm to 4 nm, although lesser and greater thicknesses can also be employed.

[0094] A silicon nucleation layer 451 is deposited in the backside recesses 43. In one embodiment, the backside blocking dielectric layer 66 is present, the conductive metal nitride layer 46A is present, and the silicon nucleation layer 451 is deposited directly on the conductive metal nitride layer 46A. In another embodiment, the backside blocking dielectric layer 66 is present, the conductive metal nitride layer 46A is absent, and the silicon nucleation layer 451 is deposited directly on the backside blocking dielectric layer 66. In another embodiment, the backside blocking dielectric layer 66 is absent, the conductive metal nitride layer 46A is present, and the silicon nucleation layer 451 is deposited directly on the conductive metal nitride layer 46A. In another embodiment, the backside blocking dielectric layer 66 is absent, the conductive metal nitride layer 46A is absent, and the silicon nucleation layer 451 is deposited directly on the horizontal surfaces of the insulating layers 32 and portions of the outer sidewall of the memory film 50.

[0095] The silicon nucleation layer 451 includes undoped silicon or doped silicon. Thus, the silicon nucleation layer 451 can consist essentially of silicon atoms (in case undoped silicon is employed), or can consist essentially of silicon atoms and electrical dopant atoms, which may be p-type dopant atoms such as boron, or n-type dopant atoms such as P, As, and/or Sb. Alternatively, the nucleation layer 451 may comprise an alloy of silicon, such as silicon-germanium having at least 50 atomic percentage of silicon.

[0096] In one embodiment, the silicon nucleation layer 451 can be doped with electrical dopants, which can be p-type dopants or n-type dopants. The doping of the silicon nucleation layer 451 lowers the resistivity of the silicon nucleation layer 451. Preferably, the atomic concentration of p-type dopants or n-type dopants in the silicon nucleation layer 451 can be in a range from $1.0 \times 10^{20}/cm^3$ to $5.0 \times 10^{20}/cm^3$, although lesser and greater dopant concentrations can also be employed.

[0097] The silicon nucleation layer 451 can be formed by a conformal deposition process such as chemical vapor deposition or atomic layer deposition. For example, layer 451 may be formed using a disilane source. Disilane may be decomposed at a relatively low temperature of about 400 C or higher (e.g., 425 to 500 C, such as 450 to 475C) to deposit a silicon layer at a relatively high rate. Alternatively, other silicon deposition sources may also be used. The silicon nucleation layer 451 can include silicon atoms in an amorphous phase, i.e., can be an amorphous silicon layer. In one embodiment, the silicon nucleation layer 451 can be an amorphous silicon nucleation layer including at least two atomic monolayers of amorphous silicon. The thickness of the silicon nucleation layer 451 can be in a range from 1 to 15 nm, such as 3 nm to 10 nm, although lesser and greater thicknesses can also be employed. In case the silicon nucleation layer 451 is doped with electrical dopants, in-situ doping or ex-situ doping can be employed to introduce the electrical dopants into the silicon nucleation layer 451.

[0098] Referring to FIG. 10C, at least one tungsten layer 46B is deposited in the backside recesses 43 after deposition of the silicon nucleation layer 451. The silicon nucleation layer 451 provides a nucleation surface upon which the tungsten material of the at least one tungsten layer 46B nucleates. The at least one tungsten layer 46B may be deposited employing a fluorine-free precursor gas, or may be deposited employing a fluorine-

containing precursor gas. The at least one tungsten layer 46B may consist of a single tungsten layer having a same composition, or can include two or more tungsten layers having different compositions of impurities (such as fluorine). The at least one tungsten layer 46B can be formed by at least one conformal deposition process, which may include a chemical vapor deposition process and/or an atomic layer deposition process.

[0099] In one embodiment, the at least one tungsten layer 46B can comprise a fluorine-free tungsten layer having a fluorine concentration less than 1.0 parts per million (p.p.m.) in atomic concentration. As used herein, an element is "fluorine-free" if the atomic concentration of fluorine is zero or at a trace level, i.e., below 1.0 p.p.m.

[0100] In this case, a portion, or all, of the at least one tungsten layer 46B can be formed employing at least one fluorine-free tungsten deposition process, i.e., at least one deposition process that deposits fluorine-free tungsten. In one embodiment, the deposition process can employ only fluorine-free materials for one or more reactants (precursor gases) and one or more additional optional agents (such as a reduction agent). The reduction agent can be a hydrogen-containing gas such as hydrogen, silane, diborane, or a combination thereof. The reduction agent can be a fluorine-free gas.

[0101] In one embodiment, the fluorine-free tungsten deposition process can be a chemical vapor deposition process or an atomic layer deposition process in which a fluorine-free tungsten precursor gas and a reduction agent gas are concurrently or alternately flowed into a process chamber in which the substrate is disposed. In one embodiment, the at least one fluorine-free tungsten deposition process comprises an atomic layer deposition process in which a fluorine-free tungsten precursor gas and a reduction gas are alternately flowed into a process chamber in which the substrate is disposed. In another embodiment, the at least one fluorine-free tungsten deposition process comprises a chemical vapor deposition process in

which a fluorine-free tungsten precursor gas and a reduction gas are simultaneously flowed into a process chamber in which the substrate is disposed.

[0102] In one embodiment, the fluorine-free tungsten precursor gas can be selected from tungsten chloride precursor gases and organometallic precursor gases including a tungsten atom. For example, the fluorine-free tungsten deposition process can be an atomic layer deposition process or a chemical vapor deposition process employing, as a fluorine-free metal precursor gas (i.e., a fluorine-free tungsten precursor gas), a gas selected from WCl_6, $W(CH_3)_6$, tungsten carbonyl, $WCl_2(Nt\text{-}Bu)_2py_2$, $W(Nt\text{-}Bu)_2Cl\{(Ni\text{-}Pr)_2CNi\text{-}Pr_2\}$, $W(Nt\text{-}Bu)_2Cl\{(Ni\text{-}Pr)_2CNMe_2\}$, $W(Nt\text{-}Bu)_2Cl\{(Ni\text{-}Pr)_2CNEt_2\}$, $W(Nt\text{-}Bu)_2Cl\{(NCy)_2CNEt_2\}$, $W(Nt\text{-}Bu)_2NMe_2\{(Ni\text{-}Pr)_2CNi\text{-}Pr_2\}$, $W(Nt\text{-}Bu)_2(NMe_2)\{(Ni\text{-}Pr)_2CNMe_2\}$, $W(Nt\text{-}Bu)_2(N_3)\{(Ni\text{-}Pr)_2CNi\text{-}Pr_2\}$, $W(Nt\text{-}Bu)_2\{(Ni\text{-}Pr)_2CNMe_2\}$, $[W(Nt\text{-}Bu)_2Cl\{NC(NMe_2)_2\}]_2$, $W(Nt\text{-}Bu)_2(N_3)\{NC(NMe_2)_2\}_2$, and $[(W(Nt\text{-}Bu)_2(N_3)(\mu_2\text{-}N_3)py)]_2$. In one embodiment, the at least one tungsten layer 46B can consist of a single fluorine-free tungsten layer.

[0103] The portions of the optional conductive metal nitride layer 46A, the silicon nucleation layer 451, and the at least one tungsten layer 46B located at each level of the backside recesses 43 (i.e., at each level of the sacrificial material layers 42 prior to removal of the sacrificial material layers 42) constitutes an electrically conductive layer 46 illustrated in FIG. 8. The portions of the optional conductive metal nitride layer 46A, the silicon nucleation layer 451, and the at least one tungsten layer 46B located within the backside via cavity 79 and over the contact level dielectric layers (71, 73) constitute the continuous conductive material layer 46L illustrated in FIG. 8.

[0104] Upon removal of the continuous conductive material layer 46L from within the backside via cavity 79 and from above the contact level dielectric layers (71, 73), the structure illustrated in FIG. 10D can be formed. The silicon nucleation layer 451 is a silicon-

containing-material layer, i.e., a layer of a silicon-containing material (a material that includes silicon atoms).

[0105] Referring to FIG. 10E, a thermal anneal at a temperature greater than 525 degrees Celsius can be performed, after, or prior to, removing the continuous conductive material layer 46L. In one embodiment, the temperature of the thermal anneal can be below a temperature range that induces formation of tungsten silicide. The silicon nucleation layer 451 including amorphous silicon can be converted into a polycrystalline silicon nucleation layer 452, which is a silicon nucleation layer having a polycrystalline phase. Thus, the polycrystalline silicon nucleation layer 452 can include undoped polysilicon or doped polysilicon or doped or undoped polycrystalline silicon-germanium. The polycrystalline silicon nucleation layer 452 is a silicon-containing-material layer.

[0106] Referring to FIG. 10F, a first variation of the first exemplary electrically conductive layer 46 is illustrated, which may be derived from the first exemplary electrically conductive layer 46 of FIG. 10C, 10D, or 10E by performing a thermal anneal at a temperature that induces formation of tungsten silicide by reaction of silicon in the silicon nucleation layer 451 (or the polycrystalline silicon nucleation layer 452) and the at least one tungsten layer 46B. The temperature and the duration of the anneal process is selected such that the entirety of the silicon nucleation layer 451 (or the polycrystalline silicon nucleation layer 452) reacts with the at least one tungsten layer 46B, and is converted into a tungsten silicide layer 471. The tungsten silicide layer 471 is a silicon-containing-material layer.

[0107] Referring to FIG. 10G, a second variation of the first exemplary electrically conductive layer 46 is illustrated, which may be derived from the first exemplary electrically conductive layer 46 of FIG. 10C, 10D, or 10E by performing a thermal anneal at a temperature that induces formation of tungsten silicide by reaction of silicon in the silicon

nucleation layer 451 (or the polycrystalline silicon nucleation layer 452) and the at least one tungsten layer 46B. The temperature and the duration of the anneal process is selected such that only a portion of the silicon nucleation layer 451 (or the polycrystalline silicon nucleation layer 452) reacts with the at least one tungsten layer 46B, and is converted into a tungsten silicide layer 471, while leaving an unreacted portion of the silicon nucleation layer 451 (or the polycrystalline silicon nucleation layer 452) that becomes a polycrystalline silicon nucleation layer 452 contacting the tungsten silicide layer 471. The polycrystalline silicon nucleation layer 452 and the tungsten silicide layer 471 are silicon-containing-material layers.

[0108] Referring to FIG. 11A, second exemplary electrically conductive layers according to a second embodiment of the present disclosure can be formed by depositing multiple tungsten layers on the silicon nucleation layer 451. Specifically, a first tungsten layer 461 can be deposited directly on the silicon nucleation layer 451 in the structure illustrated in FIG. 10B. The first tungsten layer 461 can be a fluorine-free tungsten layer including fluorine atoms at an atomic concentration less than 1.0 p.p.m., such as less than 0.1 p.p.m. The first tungsten layer 461 can be deposited employing a fluorine-free precursor gas described above.

[0109] Referring to FIG. 11B, a second tungsten layer 462 can be deposited in remaining volumes of the backside recesses 43 by another conformal deposition. The second tungsten layer 462 can include fluorine at an atomic concentration greater than 3 p.p.m., and can be formed by a conformal tungsten deposition process employing a fluorine-containing tungsten precursor gas, such as WF_6, and a reduction agent, such as hydrogen. A continuous conductive material layer 46L is formed in the backside via trench 79 and over the contact level dielectric layers (71, 73), and an electrically conductive layer 46 is formed within each backside recess 43. In this case, the at least one tungsten layer 46B can comprise the first tungsten layer 461 having a fluorine concentration less than 1.0 parts per million, and a

second tungsten layer 462 having a fluorine concentration greater than 3.0 parts per million and spaced from the memory stack structures by the first tungsten layer 461.

[0110] Referring to FIG. 11C, the continuous conductive material layer 46L can be removed from the periphery of the backside via trench 79 and from above the contact level dielectric layers (71, 73) by a recess etch, which may be an isotropic etch or an anisotropic etch. Optionally, the silicon nucleation layer 451 may be annealed to be converted into a polycrystalline silicon nucleation layer 452. The silicon nucleation layer 451 is a silicon-containing-material layer. Alternatively, a polycrystalline silicon nucleation layer 451 may be formed in lieu of the silicon nucleation layer 451 by a thermal anneal.

[0111] Referring to FIG. 12A, third exemplary electrically conductive layers according to a third embodiment of the present disclosure can be formed by depositing a sacrificial tungsten layer 477 directly on the silicon nucleation layer 451. The sacrificial tungsten layer 477 can have a thickness in a range from 1 nm to 4 nm, although lesser and greater thicknesses can also be employed. The sacrificial tungsten layer 477 can be deposited by a conformal deposition process such as chemical vapor deposition or atomic layer deposition, and may comprise a fluorine-free tungsten layer as described above.

[0112] Referring to FIG. 12B, a tungsten silicide layer 471 can be formed by reacting the sacrificial tungsten layer 477 and the silicon nucleation layer 451 to form tungsten silicide. Reaction between the sacrificial tungsten layer 477 and the silicon nucleation layer 451 can be induced by an anneal at an elevated temperature in a range from 700 degrees Celsius and 900 degrees Celsius, although lower and higher temperatures can also be employed. The duration of the anneal process may be selected to induce complete or partial silicidation of the silicon nucleation layer 451 and complete or partial silicidation of the sacrificial tungsten layer 477.

[0113] Referring to FIG. 12C, at least one tungsten layer 46B can be deposited directly on the tungsten silicide layer 471 (or on a remaining portion of the sacrificial tungsten layer 477 if a rear portion of layer 477 is not silicided). The tungsten silicide layer 471 provides a nucleation surface upon which the tungsten material of the at least one tungsten layer 46B nucleates. The at least one tungsten layer 46B can be deposited employing any of the processes that can be employed at the processing step of FIG. 10C. For example, the at least one tungsten layer 46B can include fluorine at an atomic concentration greater than 3 p.p.m., and can be formed by a conformal tungsten deposition process employing a fluorine-containing tungsten precursor gas, such as WF_6, and a reduction agent, such as hydrogen.

[0114] Upon removal of the continuous conductive material layer 46L from within the backside via cavity 79 and from above the contact level dielectric layers (71, 73), the structure illustrated in FIG. 12D can be formed. The tungsten silicide layer 471 is a silicon-containing-material layer.

[0115] Referring to FIG. 13A, fourth exemplary electrically conductive layers according to a fourth embodiment of the present disclosure can be derived from the structure illustrated in FIG. 12A by exposing the surfaces of the silicon nucleation layer 451 to a tungsten-containing precursor gas such as WF_6 without including the reduction agent, such as hydrogen. Exposure to the tungsten-containing precursor gas can be performed in a vacuum chamber at a partial pressure of the tungsten-containing precursor gas in a range from 0.1 mTorr to 10 mTorr, although lesser and greater partial pressures can also be employed.

[0116] Exposure of the silicon atoms of the silicon nucleation layer 451 to the tungsten-containing precursor gas without the reduction agent at least partially consumes silicon atoms at physically exposed surfaces of the silicon nucleation layer 451, and forms a tungsten nucleation layer 463. In an illustrative example, the tungsten-containing precursor gas can

include WF_6, and the tungsten nucleation layer 463 can include tungsten and impurity atoms of fluorine at an atomic concentration greater than 3 p.p.m. (such as greater than 10 p.p.m. and/or greater than 30 p.p.m.). The tungsten nucleation layer 463 can have a thickness in a range from 0.4 nm to 3 nm, although lesser and greater thicknesses can also be employed. In one embodiment, the tungsten nucleation layer 463 is at least one monolayer thick.

[0117] If a partial conversion of the surface portion of the silicon nucleation layer 451 into the tungsten nucleation layer 463 is performed, a stack of a remaining portion of the silicon nucleation layer 451 and the tungsten nucleation layer 463 is formed. If a full conversion of the silicon nucleation layer 451 into the tungsten nucleation layer 463 is performed, the silicon nucleation layer 451 disappears and the tungsten nucleation layer 463 contacts the conductive metal nitride layer 46A, the backside blocking dielectric layer 66, or the insulating layers 32. While partial conversion of the silicon nucleation layer 451 is illustrated in various embodiments of the present disclosure, additional embodiments are expressly contemplated herein in which the entirety of the silicon nucleation layer 451 is consumed due to exposure of the silicon nucleation layer 451 to the tungsten-containing precursor gas. In each embodiment, at least one monolayer of tungsten is deposited as a nucleation layer.

[0118] Referring to FIG. 13B, at least one tungsten layer can be subsequently deposited in remaining portions of the backside recesses 43. In one embodiment, the at least one tungsten layer can include a fluorine-free tungsten layer such as the first tungsten layer 461 deposited at the processing steps of FIG. 11B. The first tungsten layer 461 can be free of fluorine atoms, i.e., can include fluorine atoms at an atomic concentration less than 1 p.p.m., such as less than 0.1 p.p.m. The first tungsten layer 461 can be deposited employing a fluorine-free precursor gas described above. In one embodiment, the at least one tungsten

layer can consist of the fluorine-free tungsten layer such as the first tungsten layer 461.

[0119] The portions of the optional conductive metal nitride layer 46A, the silicon nucleation layer 451 (if present), and the tungsten layers 46B (which includes the tungsten nucleation layer 463 and the first tungsten layer 461) located at each level of the backside recesses 43 (i.e., at each level of the sacrificial material layers 42 prior to removal of the sacrificial material layers 42) constitutes an electrically conductive layer 46 illustrated in FIG. 8. The portions of the optional conductive metal nitride layer 46A, the silicon nucleation layer 451 (if present), and the tungsten layers 46B located within the backside via cavity 79 and over the contact level dielectric layers (71, 73) constitute the continuous conductive material layer 46L illustrated in FIG. 8. If the entirety of the silicon nucleation layer 451 is removed by exposure of the silicon nucleation layer 451 to the tungsten-containing precursor gas, then the silicon nucleation layer 451 is absent in the structure of FIG. 13B.

[0120] Upon removal of the continuous conductive material layer 46L from within the backside via cavity 79 and from above the contact level dielectric layers (71, 73), the structure illustrated in FIG. 13C can be formed. The silicon nucleation layer 451 is a silicon-containing-material layer.

[0121] Referring to FIG. 14A, fifth exemplary electrically conductive layers according to a fifth embodiment of the present disclosure can be derived from the structure illustrated in FIG. 13A by forming a combination of two tungsten layers, a first tungsten layer 461 and a second tungsten layer 462, can be formed instead of a single first tungsten layer 461 illustrated in FIG. 13B. The first tungsten layer 461 can be the same as the first tungsten layer 461 of FIG. 11A. The second tungsten layer 462 can be the same as the second tungsten layer 462 of FIG. 11B.

[0122] The portions of the optional conductive metal nitride layer 46A, the silicon

nucleation layer 451 (if present), and the tungsten layers 46B (which includes the tungsten nucleation layer 463, the first tungsten layer 461, and the second tungsten layer 462) located at each level of the backside recesses 43 (i.e., at each level of the sacrificial material layers 42 prior to removal of the sacrificial material layers 42) constitutes an electrically conductive layer 46 illustrated in FIG. 8. The portions of the optional conductive metal nitride layer 46A, the silicon nucleation layer 451 (if present), and the at least one tungsten layer 46B located within the backside via cavity 79 and over the contact level dielectric layers (71, 73) constitute the continuous conductive material layer 46L illustrated in FIG. 8. If the entirety of the silicon nucleation layer 451 is removed by exposure of the silicon nucleation layer 451 to the tungsten-containing precursor gas, then the silicon nucleation layer 451 is absent in the structure of FIG. 14B.

[0123] Upon removal of the continuous conductive material layer 46L from within the backside via cavity 79 and from above the contact level dielectric layers (71, 73), the structure illustrated in FIG. 14B can be formed. The silicon nucleation layer 451 is a silicon-containing-material layer.

[0124] Referring to FIG. 15A, sixth exemplary electrically conductive layers according to a sixth embodiment of the present disclosure can be derived from the structure of FIG. 10B. In this embodiment, the tungsten layers are selectively deposited in the backside recesses 43 (i.e., to form the structure of FIG. 9 and skipping the step shown in FIG. 8). The silicon nucleation layer 451 may be deposited as a conformal amorphous silicon layer, and may include at least two atomic monolayers of amorphous silicon. As discussed above, the backside blocking dielectric layer 66 may, or may not, be present. The conductive metal nitride layer 46A may, or may not, be present. Thus, the silicon nitride layer 451 as provided after the processing steps of FIG. 10B may be formed directly on the insulating layers 32 and

the memory film, the backside blocking dielectric layer 66, or the conductive metal nitride layer 46A.

[0125] The silicon nucleation layer 451 is anisotropically etched at the processing steps of FIG. 15A. The etchant can be provided through the backside cavity 79' in a depletive process condition, i.e., a process condition in which depletion of the etchant gas limits etching of the material of the silicon nucleation layer 451. Thus, less supply of the etchant is available for the etch process with a greater lateral distance of the region of the silicon nucleation layer 451 from the backside via trench 79. The remaining portions of the silicon nucleation layer 451 constitute a variable thickness silicon layer 451' having a variable thickness vt that increases with a lateral distance from the backside via trench 79. In one embodiment, the portion of the silicon nucleation layer 451 adjacent to the backside via trench 79 may be completely removed, and the variable thickness silicon layer is laterally spaced from a most proximal sidewall of the backside via trench 79 by a finite distance fd.

[0126] Referring to FIG. 15B, at least a portion of the variable thickness silicon layer 451' can be converted into a variable thickness tungsten layer 464 by exposing the outer surfaces of the variable thickness silicon layer 451' to a tungsten-containing precursor gas such as WF_6. Exposure to the tungsten-containing precursor gas can be performed in a vacuum chamber at a partial pressure of the tungsten-containing precursor gas in a range from 0.1 mTorr to 10 mTorr, although lesser and greater partial pressures can also be employed.

[0127] Exposure of the silicon atoms of the variable thickness silicon layer 451' to the tungsten-containing precursor gas at least partially consumes silicon atoms at physically exposed surfaces of the variable thickness silicon layer 451', and forms a tungsten nucleation layer 464. In an illustrative example, the tungsten-containing precursor gas can include WF_6,

and the variable thickness tungsten layer 464 can include tungsten and impurity atoms of fluorine at an atomic concentration greater than 3 p.p.m. (such as greater than 10 p.p.m. and/or greater than 30 p.p.m.). The variable thickness tungsten layer 464 can have a variable thickness that varies from 0 nm to a maximum thickness in a range from 0.4 nm to 3 nm, although lesser and greater maximum thicknesses can also be employed. The variable thickness tungsten layer 464 can be formed by replacement of the variable thickness silicon layer 451' with tungsten atoms through exposure to the tungsten-containing precursor gas.

[0128] Referring to FIG. 15C, additional tungsten layers (465, 466) can be deposited by at least one selective deposition process that deposits additional tungsten only on pre-existing tungsten surfaces and in remaining volumes of the backside recesses 43. In one embodiment, the additional tungsten layers (465, 466) can include a first tungsten layer 465, which can be a fluorine-free tungsten layer. The first tungsten layer 465 may be deposited employing any of the deposition methods for depositing fluorine-free tungsten described above. The thickness of the first tungsten layer 465 can be in a range from 2 nm to 5 nm, although lesser and greater thicknesses can also be employed. Subsequently, a second tungsten layer 466 can be deposited. The second tungsten layer 466 may, or may not, include fluorine, and may be deposited by any of the tungsten deposition methods described above. Tungsten does not nucleate directly on surfaces of conductive metallic material surfaces (such as surfaces of TiN) or dielectric surfaces (such as surfaces of the backside blocking dielectric layer 66 or the insulating layers 32). Thus, growth region of the additional tungsten layer (465, 466) is limited to pre-existing tungsten surfaces, and therefore, the tungsten layers 46B can be limited to levels of the backside recesses 43 (which are levels of the sacrificial material layers 42).

[0129] Referring to FIG. 15D, the portions of the conductive metal nitride layer 46A

located at the periphery of the backside via trench 79 can be removed by a recess etch, which can be an isotropic etch or an anisotropic etch. Each continuous set of a conductive metal nitride layer 46A, a variable thickness tungsten layer 464, a first tungsten layer 465, and a second tungsten layer 466 constitutes an electrically conductive layer 46. Thus, each electrically conductive layer 46 can include a first tungsten layer 465 having a fluorine concentration less than 1.0 parts per million, and a second tungsten layer 466 having a fluorine concentration greater than 3.0 parts per million and spaced from the memory stack structures 55 by the first tungsten layer 465. If desired, layer 465 may be omitted, as will be described with respect to the seventh exemplary embodiment below.

[0130] FIGS. 16A and 16B and 17A – 17E illustrate formation of seventh exemplary electrically conductive layers according to a seventh embodiment of the present disclosure. FIGS. 16A and 16B provide magnified views, and FIGS. 17A – 17E provide vertical cross-sectional views over a larger area.

[0131] Referring to FIG. 17A, the structure of FIG. 10B can be employed for the seventh embodiment.

[0132] Referring to FIG. 17B, the processing steps of FIG. 15A can be performed to form the variable thickness silicon layer 451'. The variable thickness silicon layer 451' includes a variable thickness region which is located in proximity to a backside cavity 79' and in which the thickness of the variable thickness silicon layer 451' changes. The variable thickness silicon layer 451' can also include a uniform thickness region which is located between memory openings including memory stack structures 55 and having a uniform thickness, which can be the maximum thickness of the variable thickness silicon layer 451'. In other words, by using a more aggressive sidewall silicon etch, will remove the silicon layer 451' between the backside via trench 79' and the outer row of memory stack structures 55 located

adjacent to the backside via trench 79'. However, the silicon layer 451' inside the outer row of the memory stack structures 55 may not be etched.

[0133] Referring to FIG. 17C, the processing steps of FIG. 15B can be performed to form a variable thickness tungsten nucleation layer 464. Layer 464 is not present in the backside trenches 43 adjacent to the trench 79' and has a variable thickness vt adjacent to the outer row of memory stack structures. However, layer 464 may have a uniform thickness and be present on all sidewalls of the backside recesses inside the outer row of the memory stack structures 55.

[0134] Referring to FIGS. 16A and 17D, at least one tungsten layer 466 can be selectively deposited, which may, or may not, be fluorine free. In one embodiment, the at least one tungsten layer 466 can be deposited by chemical vapor deposition process, or other tungsten deposition methods such as a low fluorine tungsten deposition process. Due to the selective nature of tungsten CVD deposition, tungsten growth will not be initiated where layer 464 is not present. Thus, layer 464 may grow inside out to initially fill the backside recess 43 space adjacent to the outer row of memory stack structures 55 and inside the outer row of the memory stack structures 55 before growing outward toward the trench 79'. This ensures that the inner parts of the backside recesses 43 are filled first without forming voids.

[0135] Referring to FIGS. 16B and 17E, the portions of the conductive metal nitride layer 46A located at the periphery of the backside via trench 79 can be removed by a recess etch, which can be an isotropic etch or an anisotropic etch. Each contiguous set of a conductive metal nitride layer 46A, a variable thickness tungsten layer 464, and a tungsten layer 466 constitutes an electrically conductive layer 46.

[0136] Referring to FIG. 17F, a variation of the seventh exemplary electrically conductive layer is illustrated, which can be derived from the seventh exemplary electrically

conductive layer by employing a partial conversion of the variable thickness silicon layer 451' into a tungsten nucleation layer 464. Thus, each electrically conductive layer 46 includes a conductive metal nitride layer 46A, a variable thickness silicon layer 451', a tungsten nucleation layer 464, and a tungsten layer 466.

[0137] Referring to FIG. 18, a source region 61 can be formed by implanting electrical dopants through each backside via trench 79 into a semiconductor portion located on, or within, the substrate (9, 10). For example, a source region 61 may be formed by implantation of dopant atoms into a portion of the doped well layer 10 through each backside via trench 79. Alternatively, a semiconductor portion can be formed on the substrate (9, 10) by deposition of a semiconductor material, for example, by selective epitaxy, and by implantation of electrical dopants into the deposited semiconductor portion.

[0138] An insulating spacer 74 can be formed at the periphery of each backside via trench 79 by deposition of a conformal insulating layer and an anisotropic etch that removes horizontal portions of the conformal insulating layer. A conductive material is deposited within the backside cavity 79' within the insulating spacer to form a backside contact via structure 76, which can be a source contact via structure.

[0139] Referring to FIG. 19, memory contact via structures 88 can be formed through the first and second contact level dielectric layers (73, 71). Specifically, a photoresist layer can be applied over the second contact level dielectric layer 73, and can be lithographically patterned to form openings overlying the drain structures 63. An anisotropic etch can be performed to transfer the pattern in the photoresist layer through the first and second contact level dielectric layers (73, 71) to form memory contact via cavities that extend through the first and second contact level dielectric layers (73, 71). The memory contact via cavities can be filled with at least one conductive material. Excess portions of the at least one conductive

material can be removed from above a horizontal plane including a top surface of the second contact level dielectric layer 73. Each remaining continuous portion of the at least one conductive material constitutes a memory contact via structure 88, which contacts a top surface of an underlying drain region 63. The photoresist layer can be subsequently removed, for example, by ashing.

[0140] Various additional contact via structures can be formed through dielectric material layers/portions of the exemplary structure. For example, peripheral device contact via structures (8G, 8A) can be formed in the peripheral device region to provide electrical contact to various nodes of the peripheral devices. The peripheral device contact via structures (8G, 8A) can include, for example, at least one gate contact via structure 8G and at least one active region contact via structure 8A.

[0141] The various exemplary structures of the present disclosure include a three-dimensional memory device, which may be a monolithic three-dimensional memory device. The three-dimensional memory device includes a stack of alternating layers comprising insulating layers 32 and electrically conductive layers 46 and located over a substrate (9, 10), a memory opening 49 extending through the stack; and a memory stack structure 55 located in the memory opening and comprising, from outside to inside, a memory material layer 504, a tunneling dielectric layer 506, and a semiconductor channel 60. Each of the electrically conductive layers 46 can comprise a silicon-containing-material layer (which may be a silicon nucleation layer 451, an amorphous silicon nucleation layer 452, a variable thickness silicon layer 451', and/or a tungsten silicide layer 471), and at least one tungsten layer embedded in the silicon-containing-material layer and contacting horizontal surfaces and an outer sidewall of the silicon-containing material layer.

[0142] In one embodiment, the silicon-containing-material layer can comprise a silicon

nucleation layer (451, 451', or 452) consisting essentially of silicon atoms or consisting essentially of silicon atoms and electrical dopant atoms. In another embodiment, the silicon-containing material layer can comprise a tungsten silicide layer 471.

[0143] In one embodiment, a backside contact via structure 76 extending through the alternating stack (32, 46) and to the substrate (9, 10) can be provided. The silicon-containing material layer can comprise a variable thickness material layer 451' having a variable thickness that increases with a lateral distance from a most proximal sidewall of the backside contact via structure 76.

[0144] In one embodiment, each of the electrically conductive layers 46 may comprise a conductive metal nitride layer 46A, and each silicon-containing-material layer may be located directly on a respective conductive metal nitride layer.

[0145] The monolithic three-dimensional memory device comprises a stack of alternating layers comprising insulating layers 32 and electrically conductive layers 46 and located over a substrate (9, 10), an array of memory openings extending through the stack; and a plurality of memory stack structures 55 located within a respective memory opening. Each electrically conductive layer 46 can laterally surround the plurality of memory stack structures 55.

[0146] In one embodiment, the memory device of the present disclosure can be a monolithic three-dimensional memory device comprising a vertical NAND device located over the substrate (9, 10), and the electrically conductive layers 46 can comprise, or are electrically connected to, a respective word line of the vertical NAND device. Top and bottom electrically conductive layers in the stack may comprise drain and source select gate electrodes. The substrate (9, 10) can comprise a silicon substrate. The vertical NAND device can comprise an array of monolithic three-dimensional NAND strings located over the silicon substrate. At least one memory cell in a first device level of the three-dimensional array of

NAND strings is located over another memory cell in a second device level of the three-dimensional array of NAND string. The silicon substrate can contain an integrated circuit comprising a driver circuit for the memory device located thereon.

[0147] The array of monolithic three-dimensional NAND strings can comprise a plurality of semiconductor channels. At least one end portion of each of the plurality of semiconductor channels extends substantially perpendicular to a top surface of the substrate (9, 10). In one embodiment, the plurality of semiconductor channels can comprise a common horizontal semiconductor channel portion that is a portion of the doped well layer 10 between a source region 61 and the epitaxial channel portions 11, and the vertical semiconductor channels 60 that are portions of the memory stack structures 55. The array of monolithic three-dimensional NAND strings can comprise a plurality of charge storage elements (which can be embodied as sections of a memory material layer 504 that is present within each memory stack structure 55). Each charge storage element can be located adjacent to a respective one of the plurality of semiconductor channels, i.e., adjacent to a respective vertical semiconductor channel 60. The array of monolithic three-dimensional NAND strings can comprise a plurality of control gate electrodes having a strip shape extending substantially parallel to the top surface of the substrate (9, 10). The plurality of control gate electrodes comprise at least a first control gate electrode located in the first device level and a second control gate electrode located in the second device level.

[0148] The methods of the present disclosure provide various benefits including, but not limited to, the following. The silicon nucleation layer 451 does not include any fluorine atoms. In this regard, the silicon nucleation layer 451 is different from previously known tungsten nucleation layers because previously known tungsten nucleation layers employ fluorine at a concentration of about $1.0 \times 10^{21}/cm^3$. As discussed above, fluorine diffusion

has been associated with formation of voids in the word line oxide layers after thermal processing steps. Since fluorine is absent in the silicon nucleation layer 451, there is less chance of void formation.

[0149] Another drawback of the conventional nucleation layer employed to nucleate tungsten is high resistivity, which can be in the range of several hundreds of microOhm-cm. While intrinsic silicon has an even higher resistivity, introduction of electrical dopants (such as p-type dopants or n-type dopants) can reduce the resistivity to a level lower than the resistivity of conventional nucleation layers. Thus, with electrical doping, the silicon nucleation layer 451 can provide a lower resistivity than conventional nucleation layers. In addition, the contribution of the silicon nucleation layer 451 to the electrical resistivity can be further lowered in embodiments in which a metal silicide material is subsequently formed. Since the nucleation layer is expected to takes up for a greater percentage of the total thickness of a word line in the devices of future generations, the contribution of the resistivity of the nucleation layer to the total resistivity of a word line is expected to increase. Employing doped silicon for the silicon nucleation layer 451 can significantly reduce the total resistivity of each word line in future generations.

[0150] As far as stress is concerned, even though conventional nucleation layers are relatively thin, the conventional nucleation layers contribute significantly to stress in the device structure because of its high moduli of elasticity. The silicon nucleation layer 451 of the present disclosure can significantly lower the component of stress caused by the nucleation layer.

[0151] Although the foregoing refers to particular preferred embodiments, it will be understood that the disclosure is not so limited. It will occur to those of ordinary skill in the art that various modifications may be made to the disclosed embodiments and that such

modifications are intended to be within the scope of the disclosure. Where an embodiment employing a particular structure and/or configuration is illustrated in the present disclosure, it is understood that the present disclosure may be practiced with any other compatible structures and/or configurations that are functionally equivalent provided that such substitutions are not explicitly forbidden or otherwise known to be impossible to one of ordinary skill in the art. All of the publications, patent applications and patents cited herein are incorporated herein by reference in their entirety.

WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, comprising:

forming a stack of alternating layers comprising insulating layers and sacrificial material layers over a substrate;

forming a plurality of memory openings through the stack;

forming memory stack structures in the plurality of memory openings, each of the memory stack structures comprising, from outside to inside, a memory material layer, a tunneling dielectric layer, and a semiconductor channel;

forming a backside via trench through the stack of alternating layers;

forming backside recesses by removing the sacrificial material layers selective to the insulating layers employing an etchant introduced through the backside via trench;

depositing a silicon-containing nucleation layer in the backside recesses; and

forming at least one tungsten layer in the backside recesses after deposition of the silicon-containing nucleation layer;

wherein control gate electrodes for the memory stack structures are formed at levels of the backside recesses; and

wherein each of the control gate electrodes comprises a portion of the at least one tungsten layer.

2. The method of Claim 1, wherein the silicon-containing nucleation layer comprises an amorphous silicon-containing nucleation layer including at least two atomic monolayers of amorphous silicon.

3. The method of Claim 2, further comprising depositing a conductive metal nitride layer in the backside recesses, wherein the silicon-containing nucleation layer is deposited on the conductive metal nitride layer.

4. The method of Claim 2, further comprising depositing a backside blocking dielectric layer in the backside recesses, wherein the silicon-containing nucleation layer is deposited over the backside blocking dielectric layer.

5. The method of Claim 4, further comprising depositing a conductive metal nitride layer directly on the backside blocking dielectric layer, wherein the silicon-containing nucleation layer is deposited on the conductive metal nitride layer.

6. The method of Claim 4, wherein the silicon-containing nucleation layer is deposited directly on the backside blocking dielectric layer.

7. The method of Claim 1, wherein the control gate electrodes comprise portions of the silicon-containing nucleation layer.

8. The method of Claim 1, further comprising forming a tungsten silicide layer by reacting at least a portion of the silicon-containing nucleation layer with a surface portion of the at least one tungsten layer prior to patterning the at least one tungsten layer.

9. The method of Claim 1, further comprising:

depositing a sacrificial tungsten layer directly on the silicon-containing nucleation layer; and

forming a tungsten silicide layer by reacting the sacrificial tungsten layer and the silicon-containing nucleation layer,

wherein the at least one tungsten layer is deposited directly on the tungsten silicide layer.

10. The method of Claim 1, wherein the at least one tungsten layer comprises a fluorine-free tungsten layer having a fluorine concentration less than 1.0 parts per million (p.p.m.) in atomic concentration.

11. The method of Claim 10, wherein the fluorine-free tungsten layer is formed employing a fluorine-free tungsten precursor gas selected from WCl_6, $W(CH_3)_6$, tungsten carbonyl, $WCl_2(Nt\text{-}Bu)_2py_2$, $W(Nt\text{-}Bu)_2Cl\{(Ni\text{-}Pr)_2CNi\text{-}Pr_2\}$, $W(Nt\text{-}Bu)_2Cl\{(Ni\text{-}Pr)_2CNMe_2\}$, $W(Nt\text{-}Bu)_2Cl\{(Ni\text{-}Pr)_2CNEt_2\}$, $W(Nt\text{-}Bu)_2Cl\{(NCy)_2CNEt_2\}$, $W(Nt\text{-}Bu)_2NMe_2\{(Ni\text{-}Pr)_2CNi\text{-}Pr_2\}$, $W(Nt\text{-}Bu)_2(NMe_2)\{(Ni\text{-}Pr)_2CNMe_2\}$, $W(Nt\text{-}Bu)_2(N_3)\{(Ni\text{-}Pr)_2CNi\text{-}Pr_2\}$, $W(Nt\text{-}Bu)_2\{(Ni\text{-}Pr)_2CNMe_2\}$, $[W(Nt\text{-}Bu)_2Cl\{NC(NMe_2)_2\}]_2$, $W(Nt\text{-}Bu)_2(N_3)\{NC(NMe_2)_2\}_2$, and $[(W(Nt\text{-}Bu)_2(N_3)(\mu_2\text{-}N_3)py)]_2$.

12. The method of Claim 1, wherein the at least one tungsten layer comprises:

a first tungsten layer having a fluorine concentration less than 1.0 parts per million; and

a second tungsten layer having a fluorine concentration greater than 3.0 parts per million and spaced from the memory stack structures by the first tungsten layer.

13. The method of Claim 1, further comprising converting at least a portion of the silicon-containing nucleation layer to a tungsten nucleation layer by exposing the silicon-containing nucleation layer to a tungsten-containing precursor gas without hydrogen-containing gas which functions as a reduction agent prior to formation of the at least one tungsten layer.

14. The method of Claim 13, wherein:

the tungsten-containing precursor gas is WF_6; and

the at least one tungsten layer comprises a fluorine-free tungsten layer having a fluorine concentration less than 1.0 parts per million and contacting a remaining portion of the silicon-containing nucleation layer.

15. The method of Claim 13, wherein an entirety of the silicon-containing nucleation layer is removed by exposure of the silicon-containing nucleation layer to the tungsten-containing precursor gas.

16. The method of Claim 1, wherein:

the silicon-containing nucleation layer is deposited as a conformal amorphous silicon layer; and

the method further comprises anisotropically etching the conformal amorphous silicon layer by introducing an etchant through the backside via trench, wherein a variable thickness silicon layer having a variable thickness that increases with a lateral distance from the backside via trench is formed.

17. The method of Claim 16, wherein the variable thickness silicon layer is laterally spaced from a most proximal sidewall of the backside via trench by a finite distance.

18. The method of Claim 16, further comprising converting at least a portion of the variable thickness silicon layer into a tungsten nucleation layer by exposing the outer surfaces of the variable thickness silicon layer to a tungsten-containing precursor gas without hydrogen-containing gas which functions as a reduction agent.

19. The method of Claim 18, wherein:

a variable thickness tungsten layer is formed by replacement of the variable thickness silicon layer with tungsten atoms through exposure to the tungsten-containing precursor gas; and

the at least one tungsten layer is deposited by at least one selective deposition process that deposits additional tungsten only on the tungsten nucleation layer.

20. The method of Claim 1, wherein the silicon-containing nucleation layer comprises doped or undoped amorphous silicon deposited by chemical vapor deposition using a disilane source.

21. The method of Claim 1, wherein:

the semiconductor device is a monolithic three-dimensional memory device comprising a vertical NAND device located over the substrate;

the electrically conductive layers comprise, or are electrically connected to, a respective word line of the vertical NAND device;

the substrate comprises a silicon substrate;

the vertical NAND device comprises an array of monolithic three-dimensional NAND strings located over the silicon substrate;

at least one memory cell in a first device level of the three-dimensional array of NAND strings is located over another memory cell in a second device level of the three-dimensional array of NAND strings;

the silicon substrate contains an integrated circuit comprising a driver circuit for the memory device located thereon; and

the array of monolithic three-dimensional NAND strings comprises:

a plurality of semiconductor channels, wherein at least one end portion of each of the plurality of semiconductor channels extends substantially perpendicular to a top surface of the substrate;

a plurality of charge storage elements, each charge storage element located adjacent to a respective one of the plurality of semiconductor channels; and

a plurality of control gate electrodes having a strip shape extending substantially parallel to the top surface of the substrate, the plurality of control gate electrodes comprise at least a first control gate electrode located in the first device level and a second control gate electrode located in the second device level.

22. A three-dimensional memory device comprising:

a stack of alternating layers comprising insulating layers and electrically conductive layers and located over a substrate;

a memory opening extending through the stack; and

a memory stack structure located in the memory opening and comprising, from outside to inside, a memory material layer, a tunneling dielectric layer, and a semiconductor

channel;

wherein each of the electrically conductive layers comprises:

a silicon-containing-material layer; and

at least one tungsten layer embedded in the silicon-containing-material layer and contacting horizontal surfaces and an outer sidewall of the silicon-containing material layer.

23. The three-dimensional memory device of Claim 22, wherein the silicon-containing-material layer comprises a silicon nucleation layer consisting essentially of silicon atoms or consisting essentially of silicon atoms and electrical dopant atoms.

24. The three-dimensional memory device of Claim 22, wherein the silicon-containing material layer comprises a tungsten silicide layer.

25. The three-dimensional memory device of Claim 22, further comprising a backside contact via structure extending through the alternating stack and to the substrate, wherein the silicon-containing material layer comprises a variable thickness material layer having a variable thickness that increases with a lateral distance from a most proximal sidewall of the backside contact via structure.

26. The three-dimensional memory device of Claim 22, wherein:

each of the electrically conductive layers comprise a conductive metal nitride layer; and

each silicon-containing-material layer is located directly on a respective conductive

metal nitride layer.

27. The three-dimensional memory device of Claim 22, wherein:

the three-dimensional memory device comprises a vertical NAND device located over the substrate;

the electrically conductive layers comprise, or are electrically connected to, a respective word line of the vertical NAND device;

the substrate comprises a silicon substrate;

the vertical NAND device comprises an array of monolithic three-dimensional NAND strings located over the silicon substrate;

at least one memory cell in a first device level of the three-dimensional array of NAND strings is located over another memory cell in a second device level of the three-dimensional array of NAND strings;

the silicon substrate contains an integrated circuit comprising a driver circuit for the memory device located thereon; and

the array of monolithic three-dimensional NAND strings comprises:

a plurality of semiconductor channels, wherein at least one end portion of each of the plurality of semiconductor channels extends substantially perpendicular to a top surface of the substrate;

a plurality of charge storage elements, each charge storage element located adjacent to a respective one of the plurality of semiconductor channels; and

a plurality of control gate electrodes having a strip shape extending substantially parallel to the top surface of the substrate, the plurality of control gate electrodes comprise at least a first control gate electrode located in the first device

level and a second control gate electrode located in the second device level.

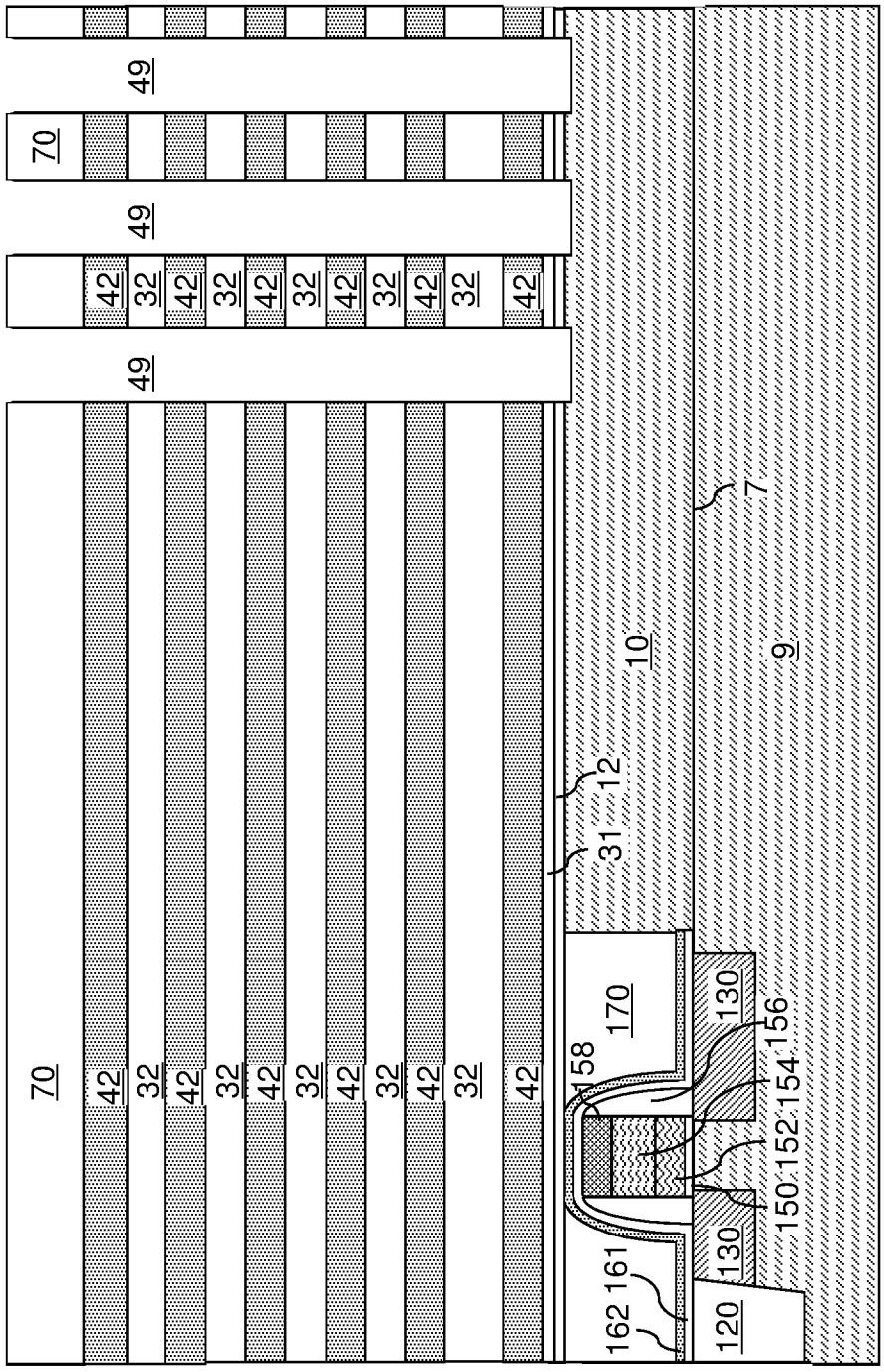


FIG. 1

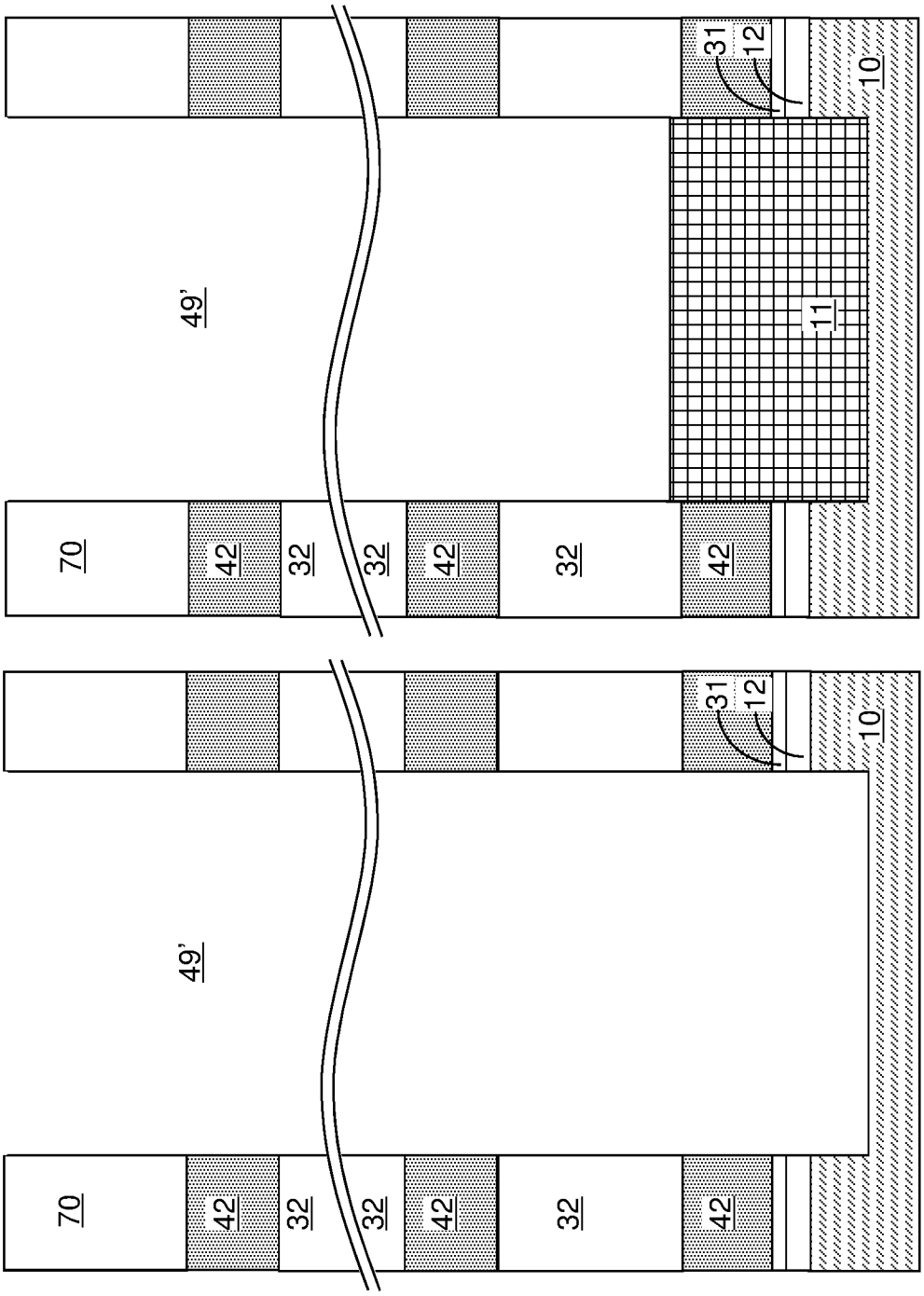


FIG. 2B

FIG. 2A

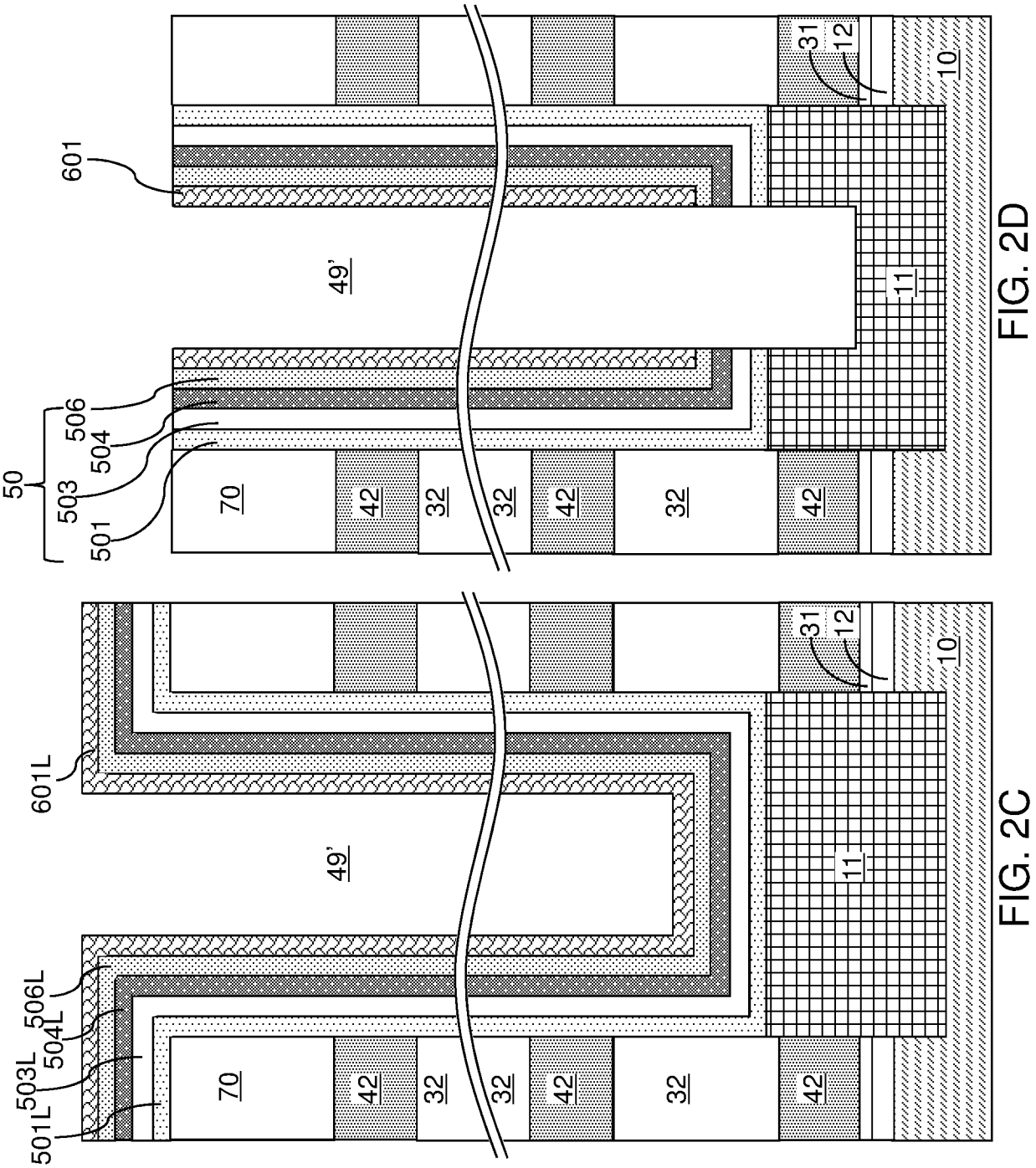

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FIG. 2D

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FIG. 2C

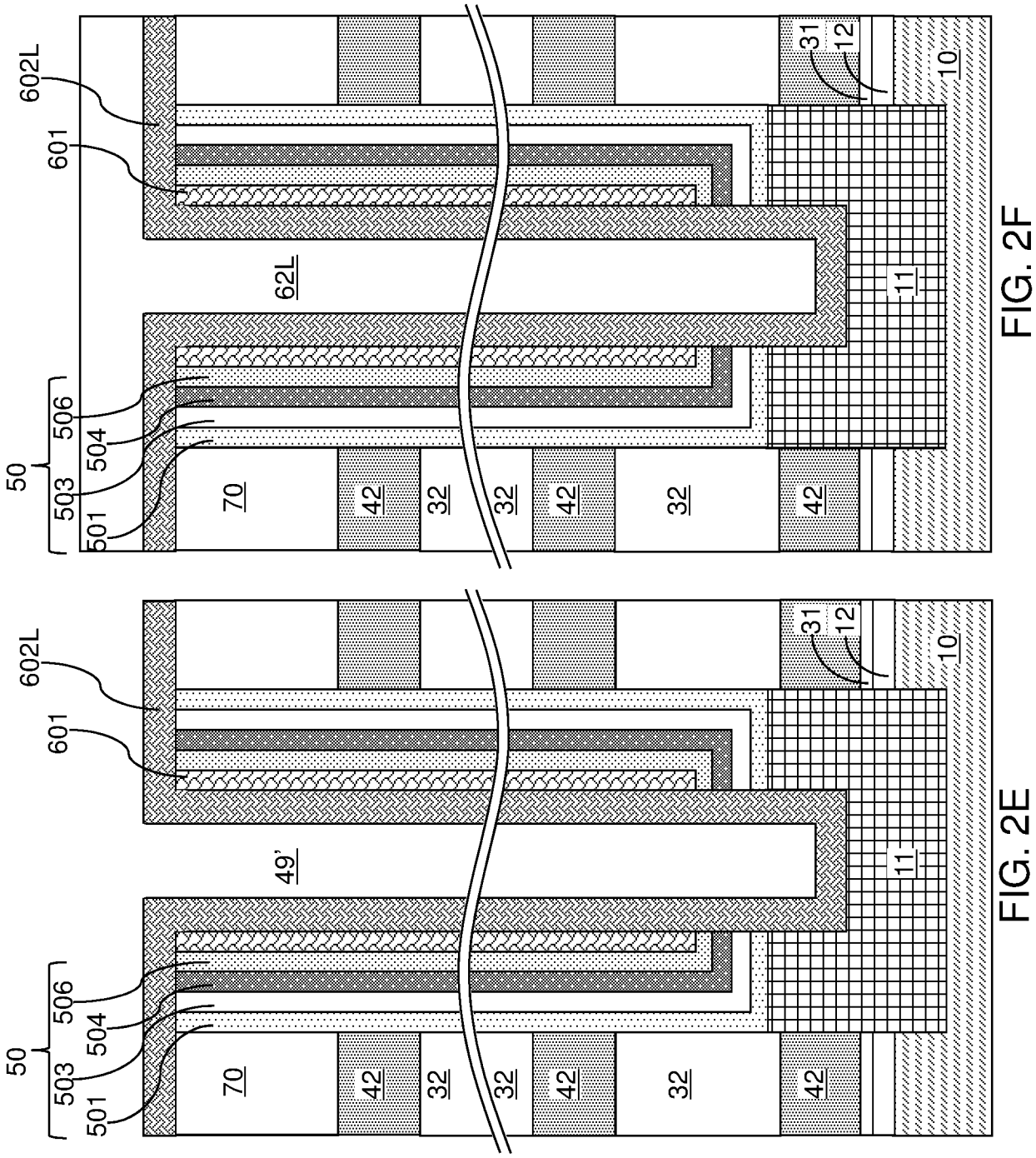

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FIG. 2F

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FIG. 2E

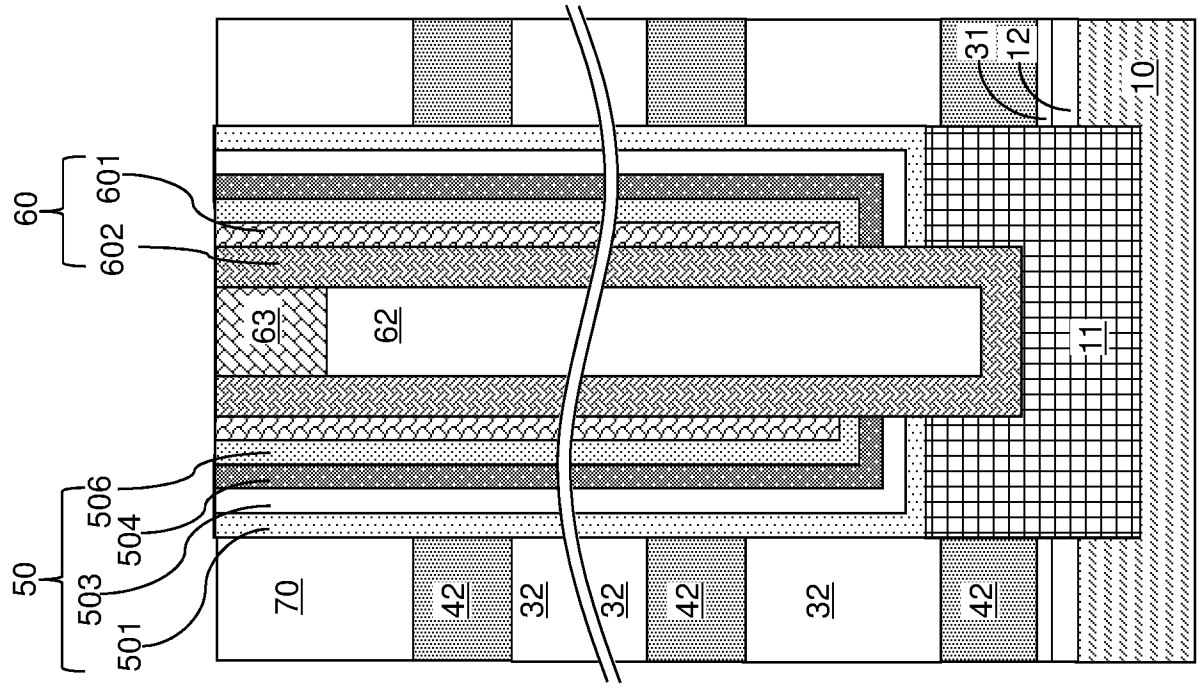

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FIG. 2H

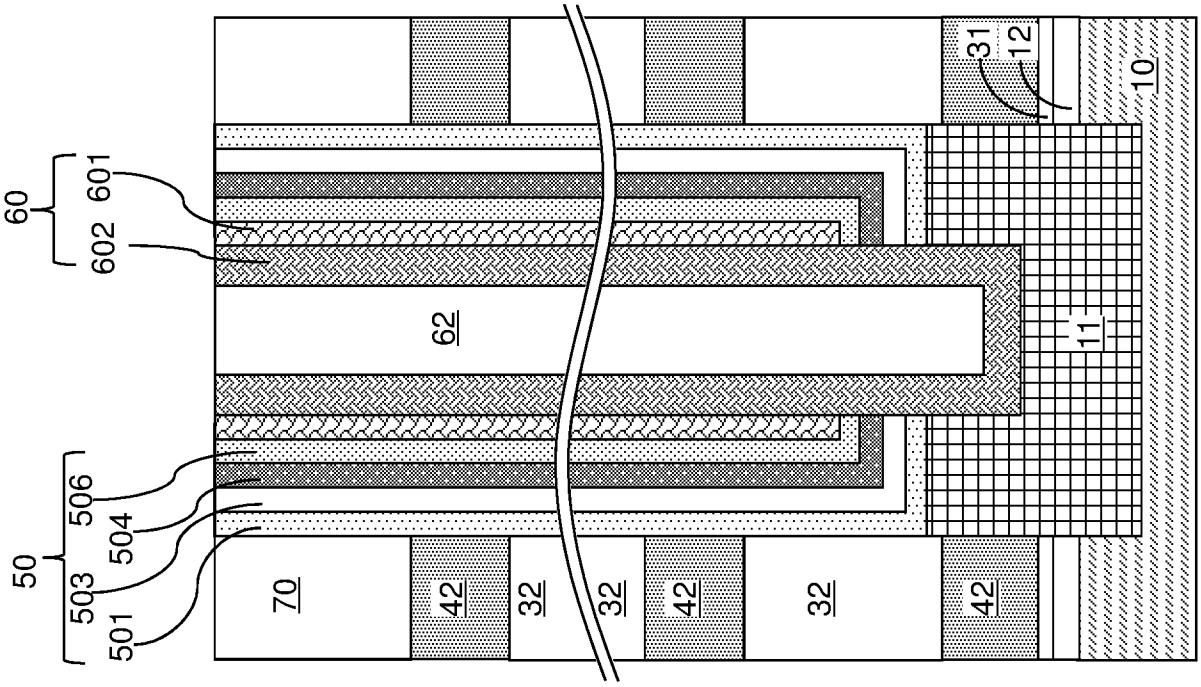

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FIG. 2G

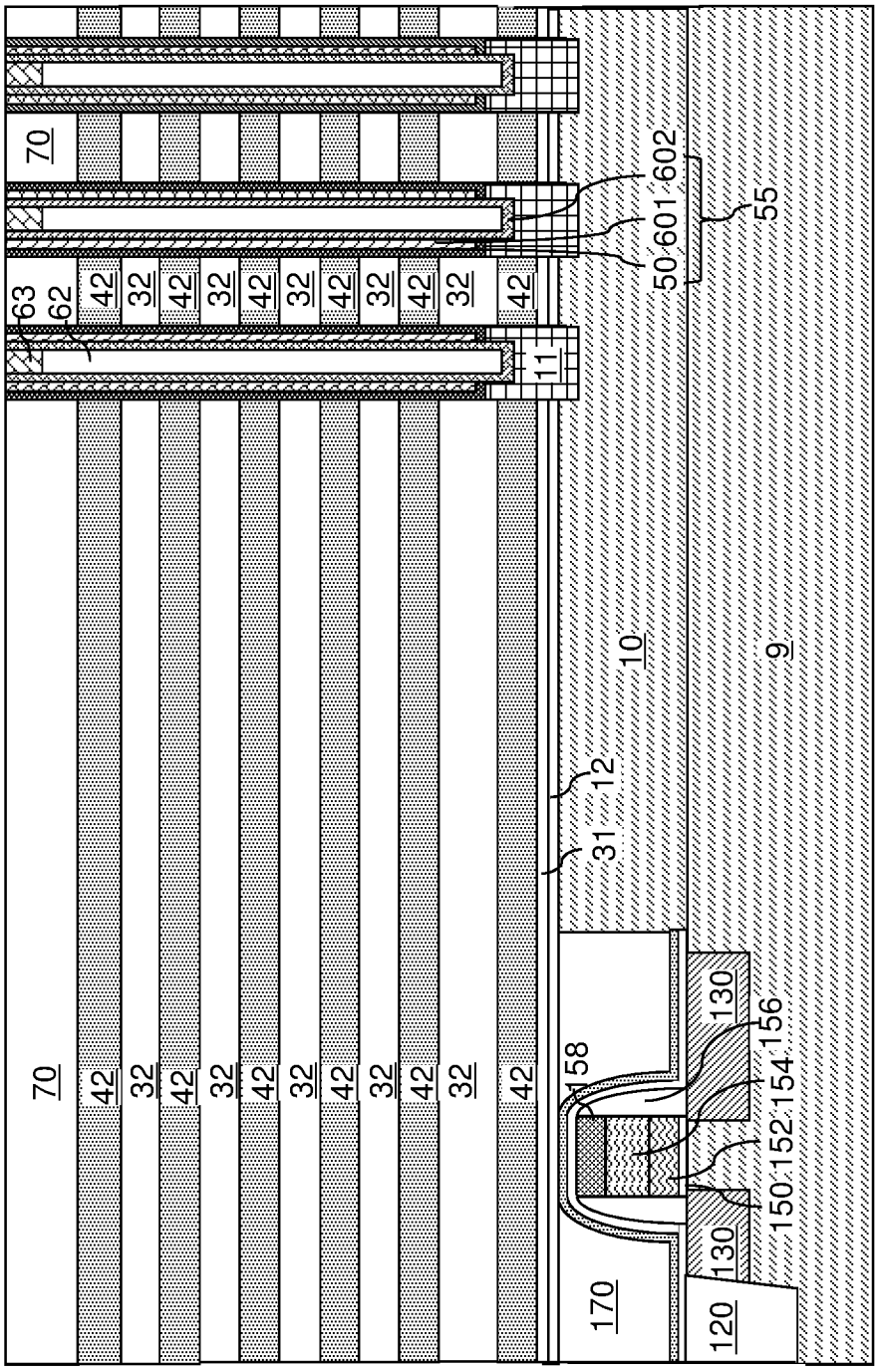

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FIG. 3

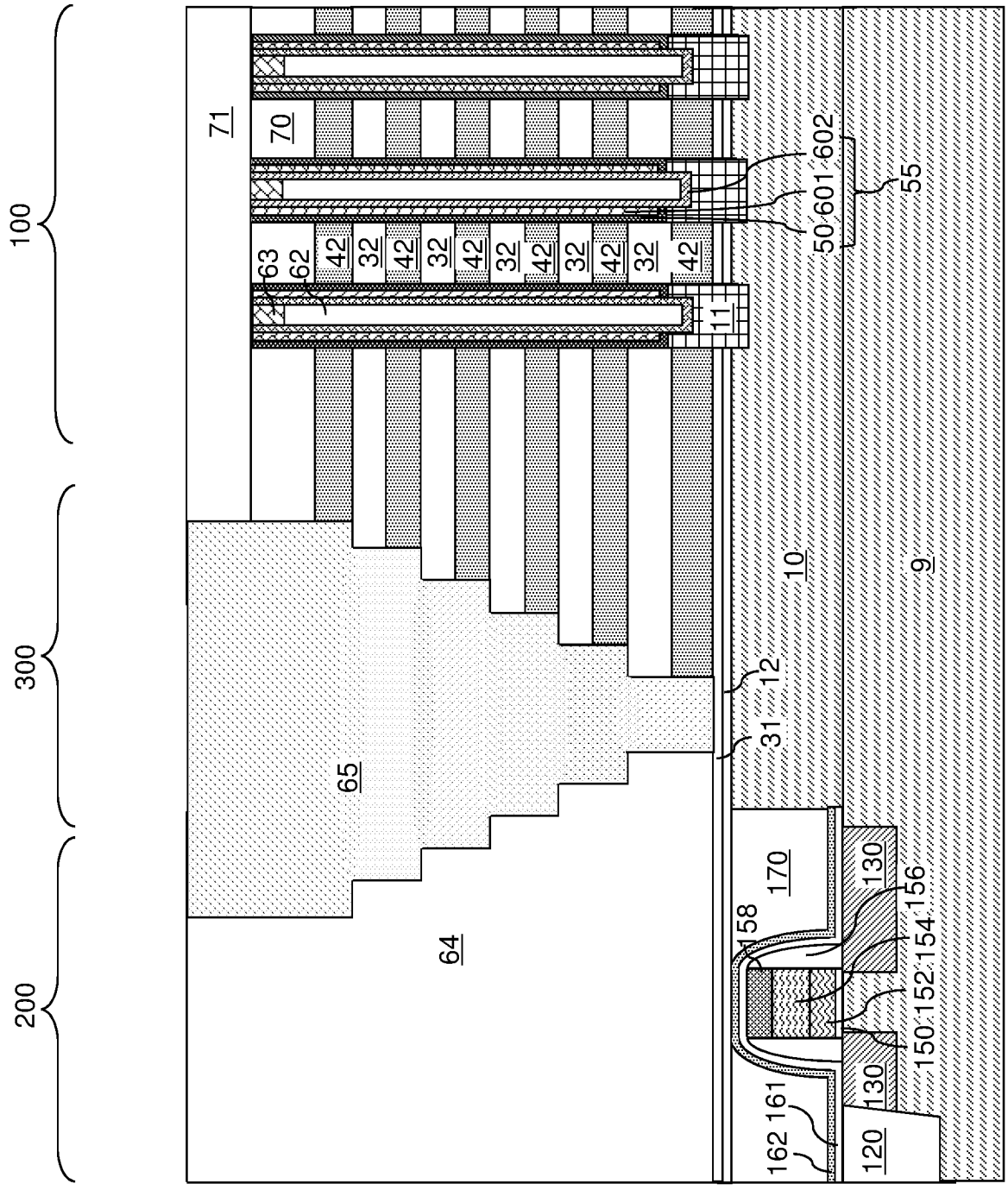

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FIG. 4

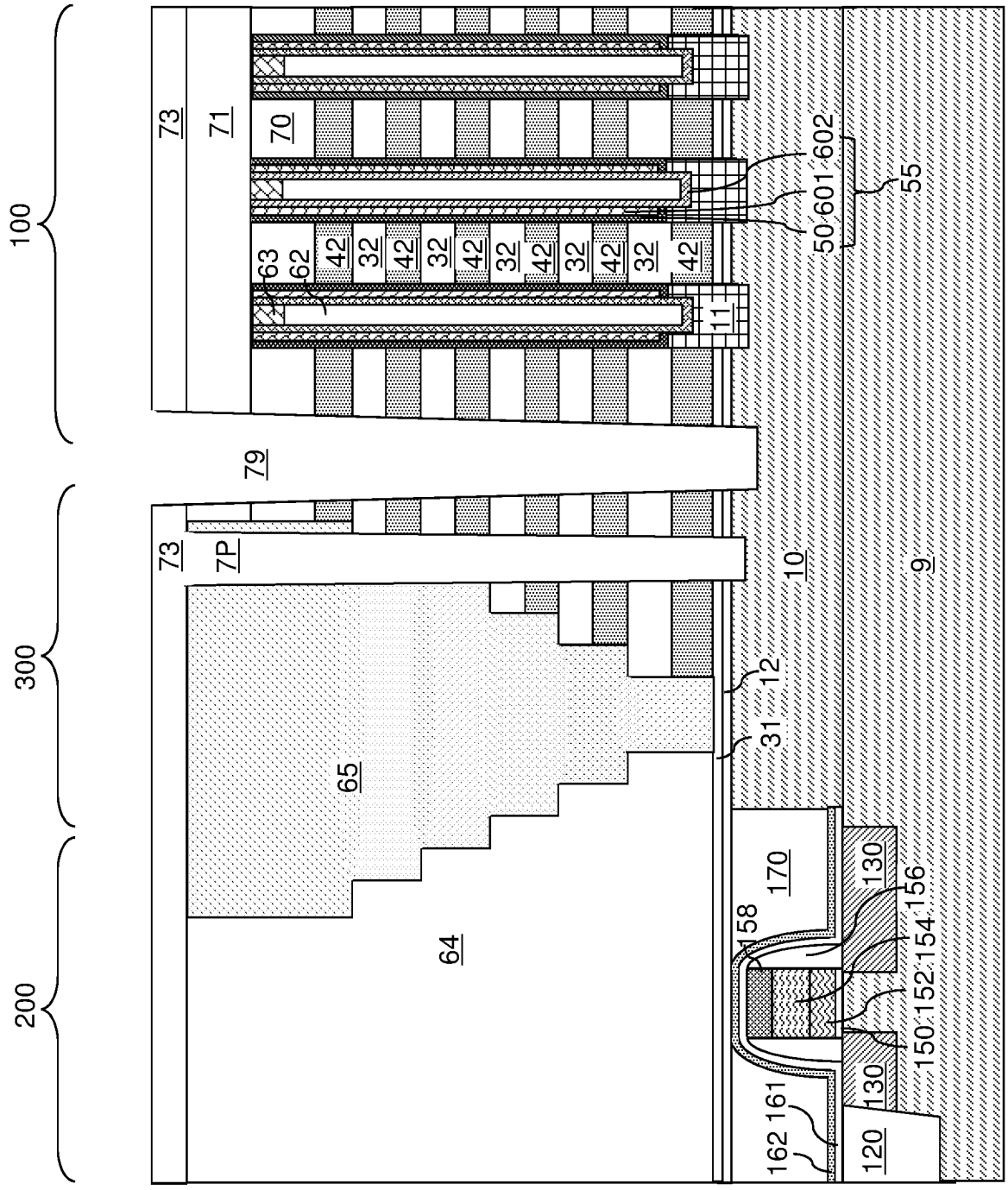

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FIG. 5A

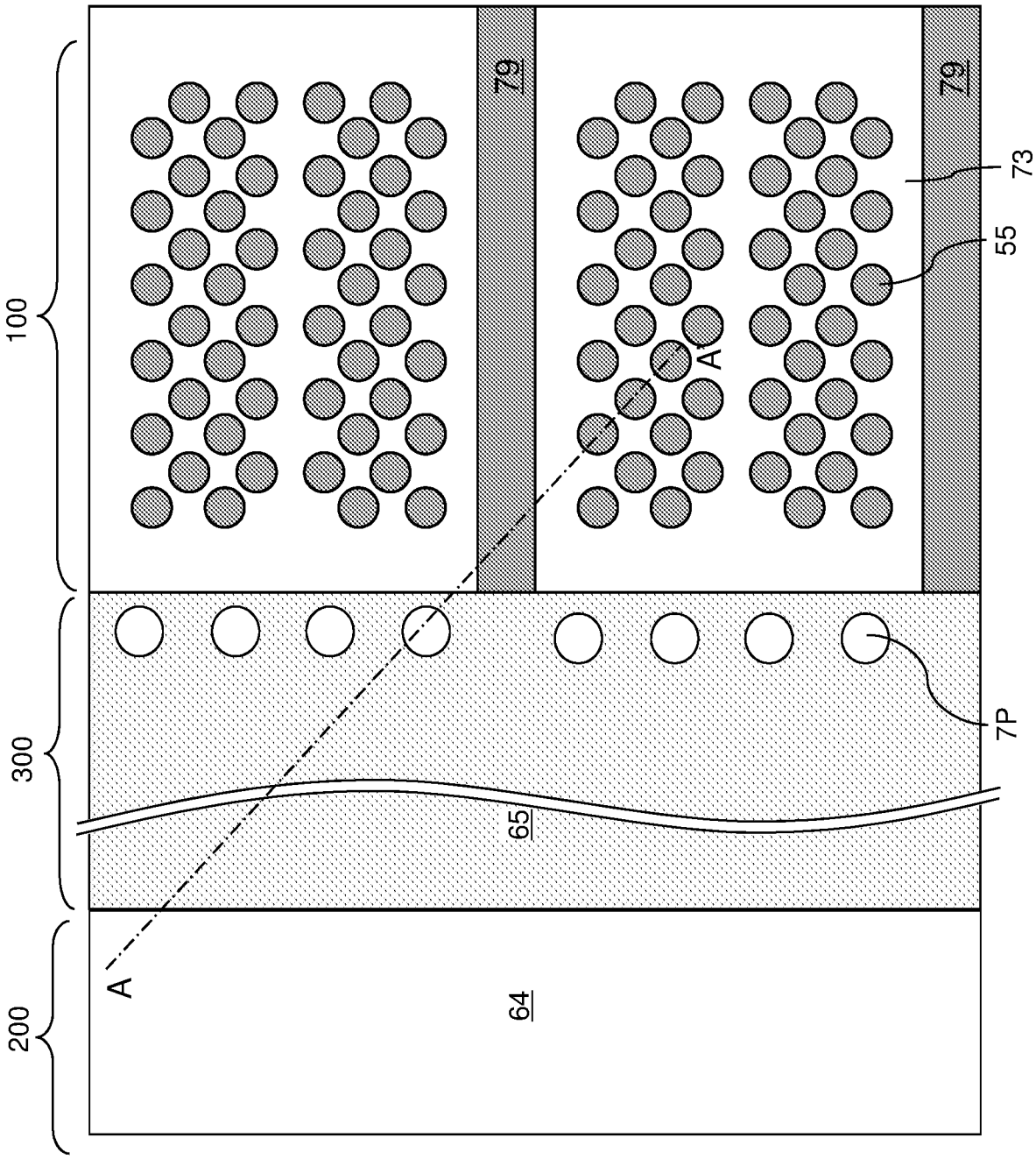


FIG. 5B

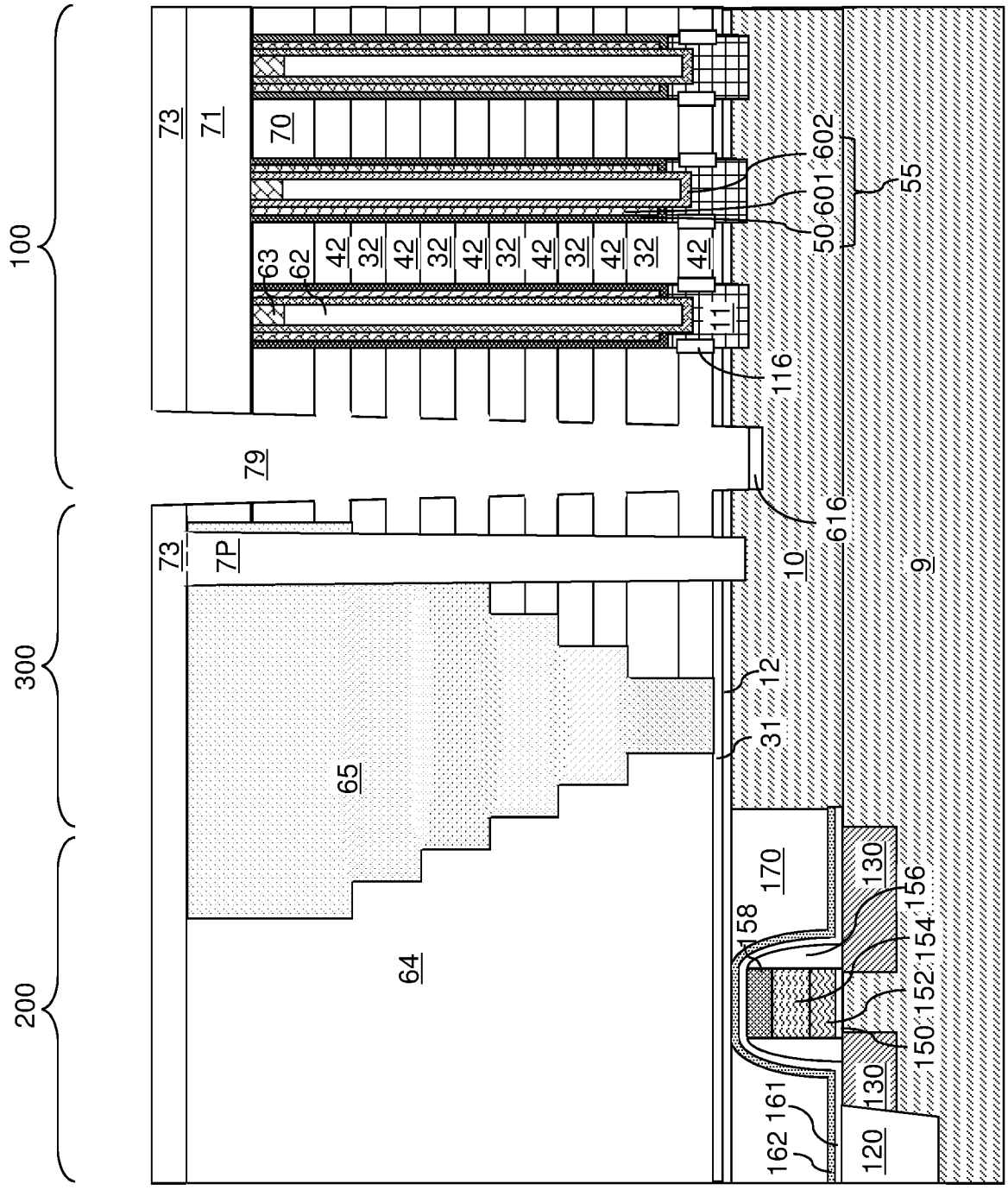

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FIG. 6

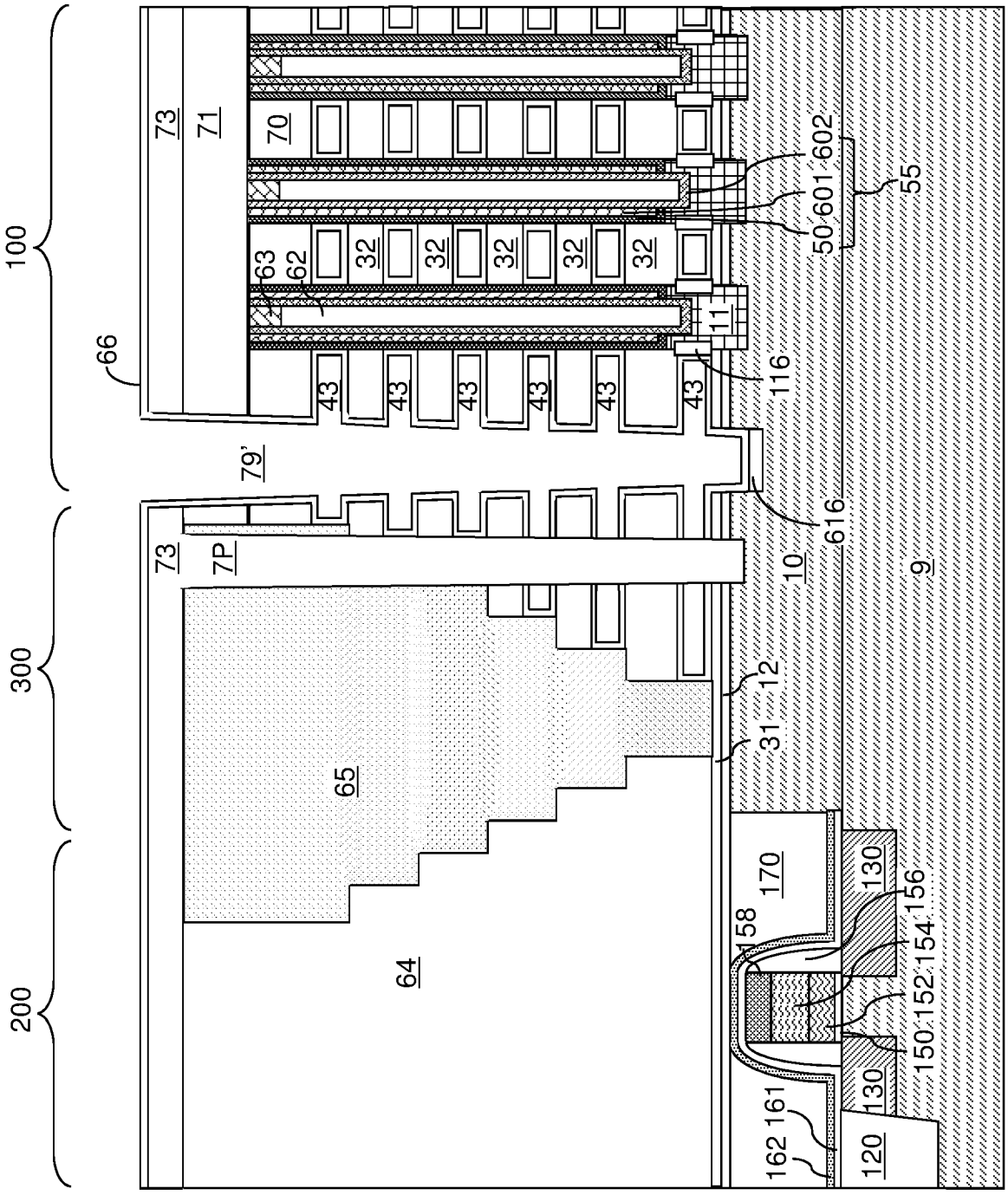

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FIG. 7

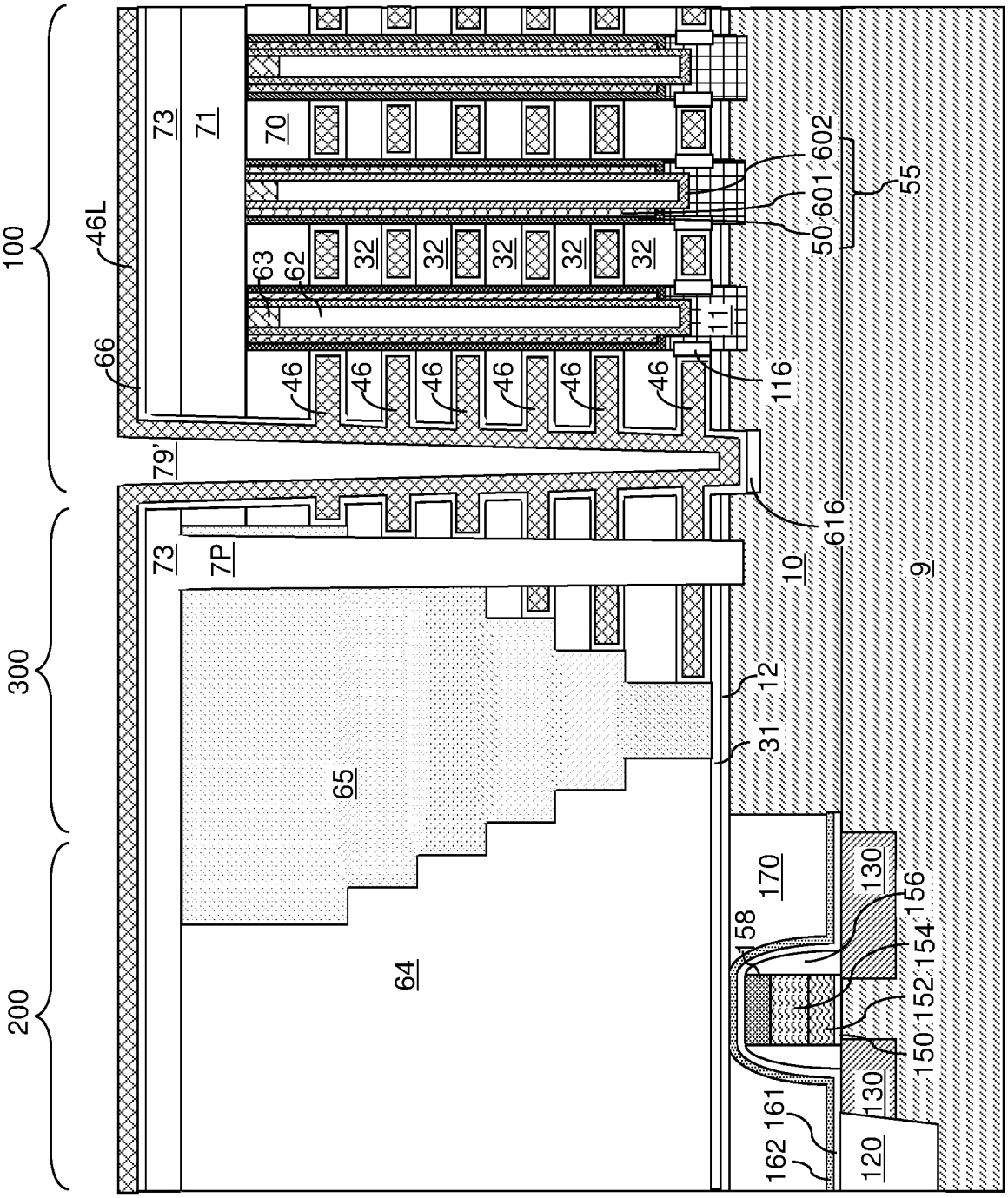

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FIG. 8

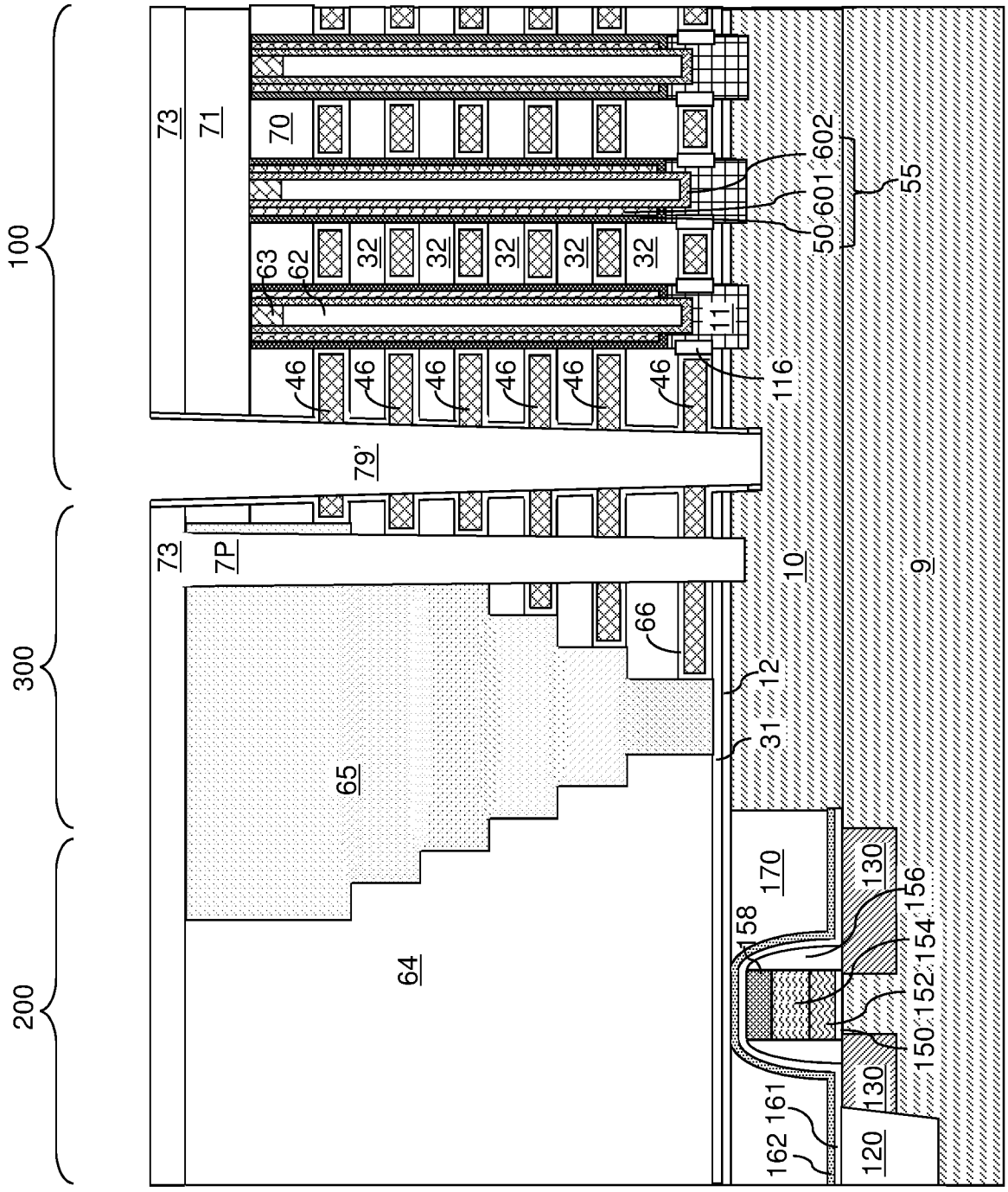

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FIG. 9

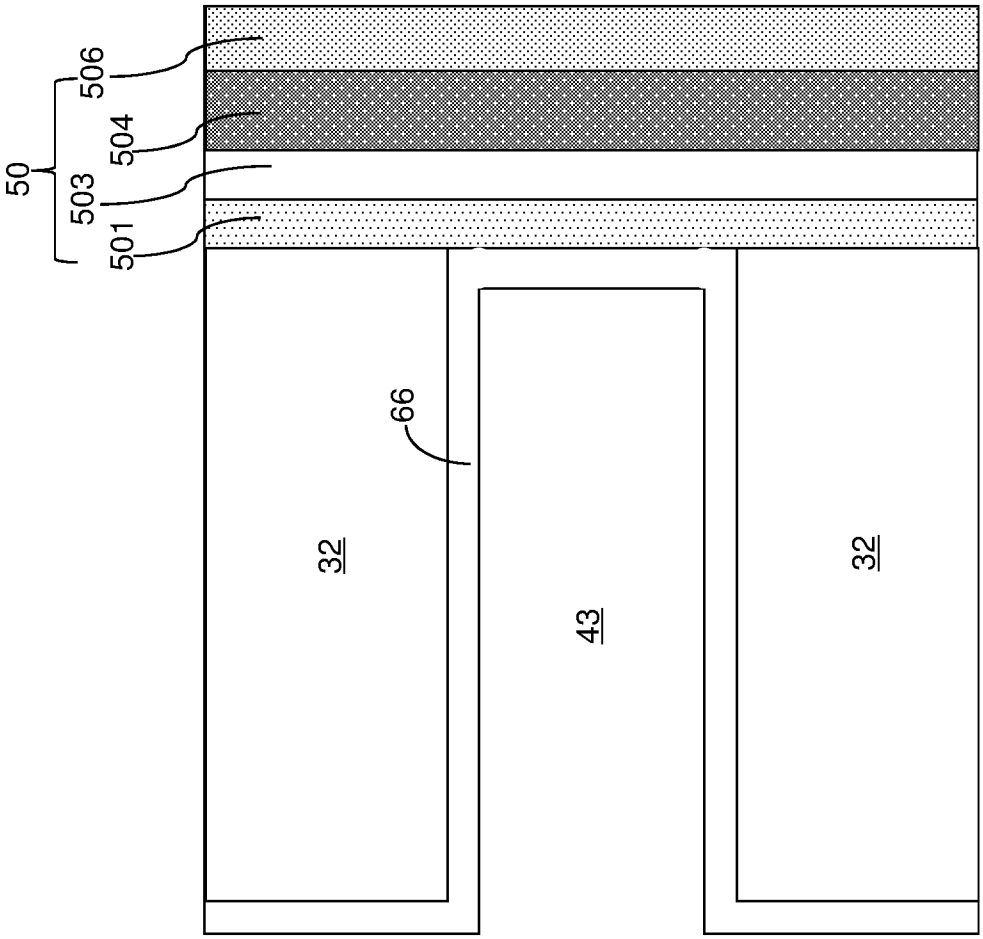


FIG. 10A

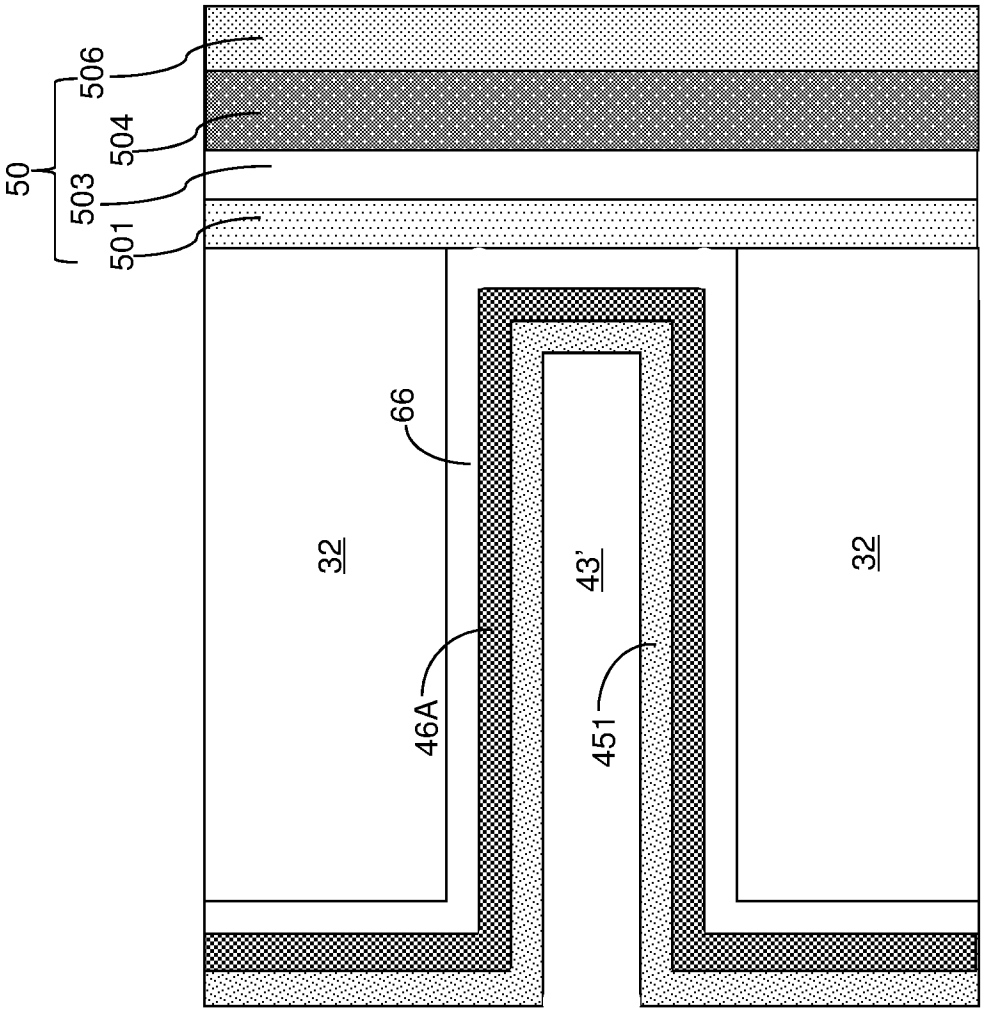


FIG. 10B

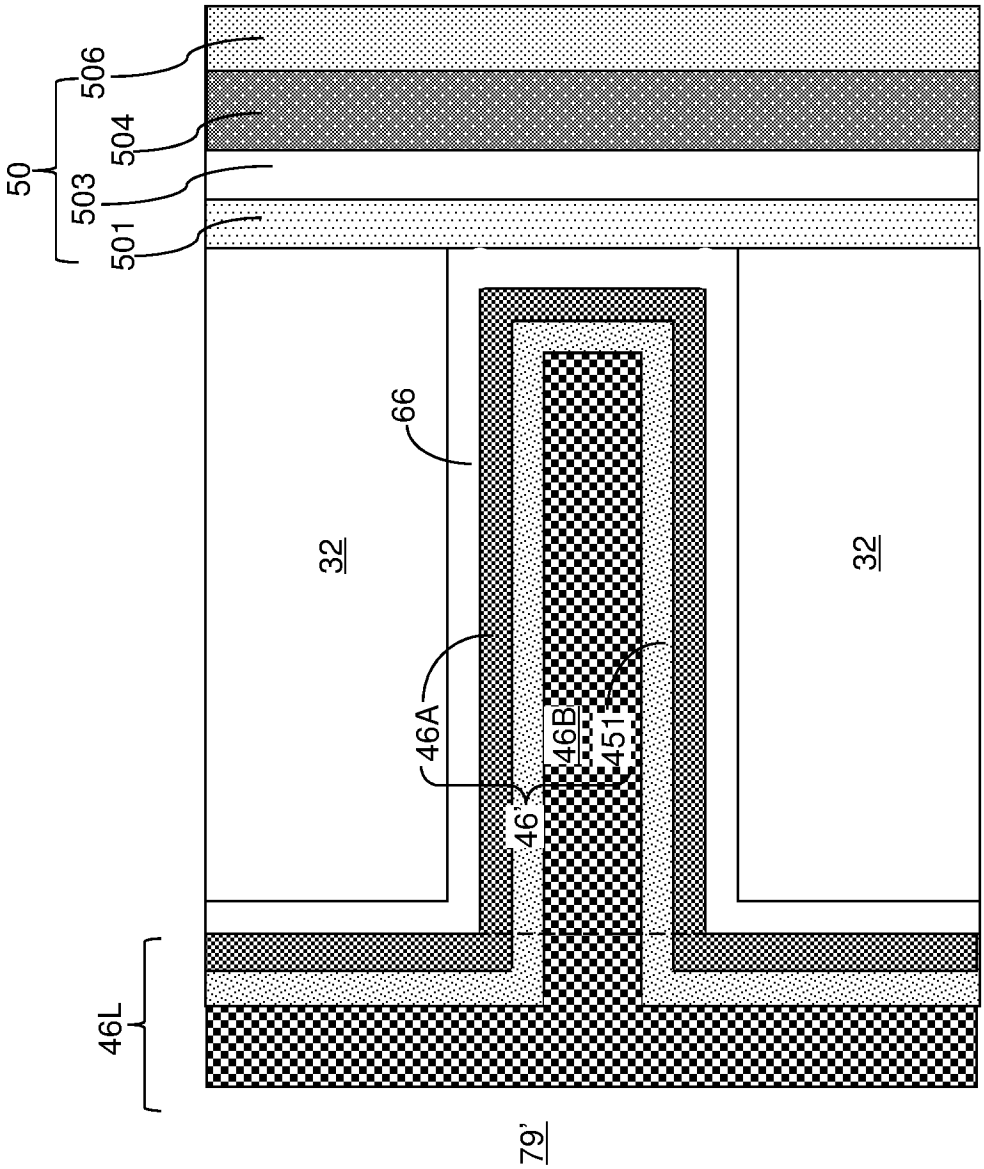


FIG. 10C

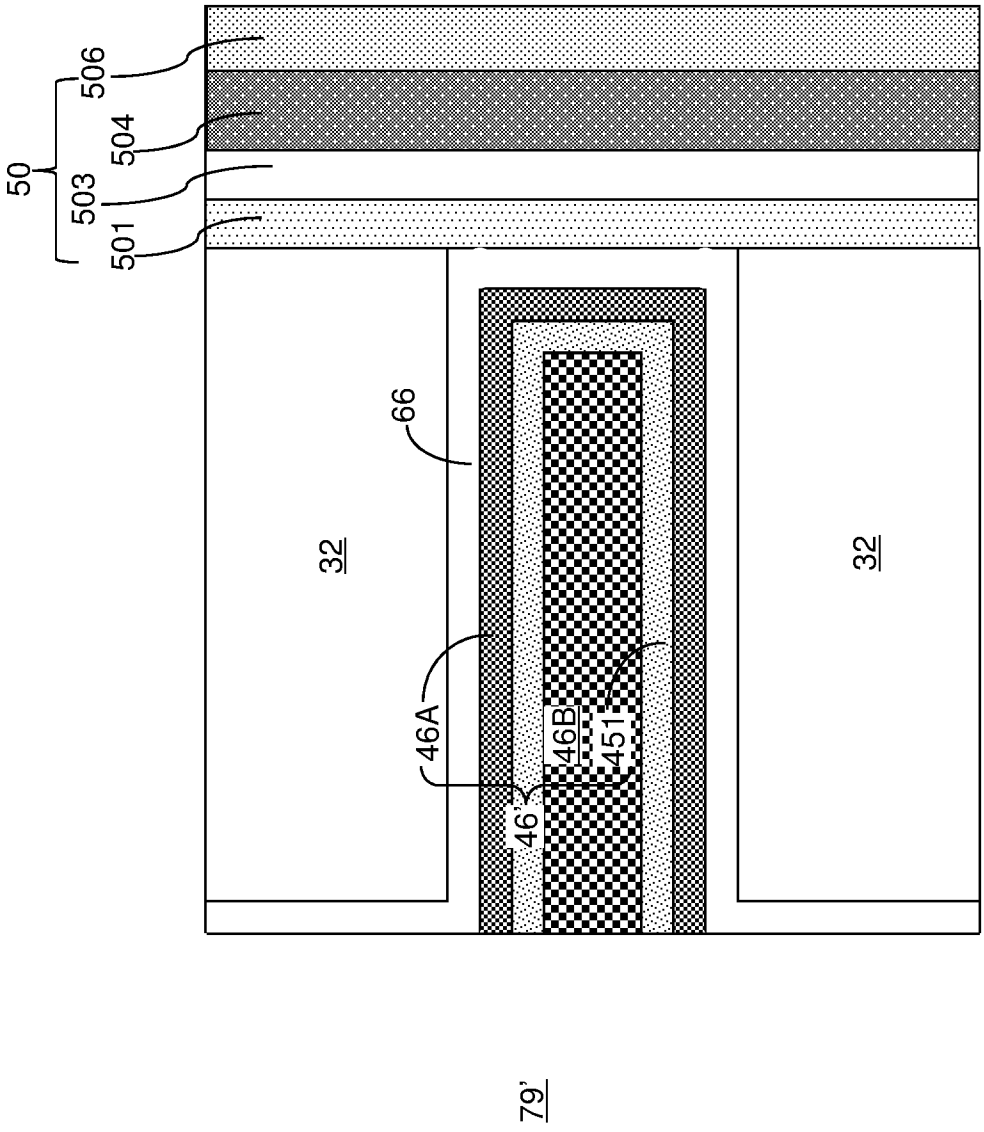


FIG. 10D

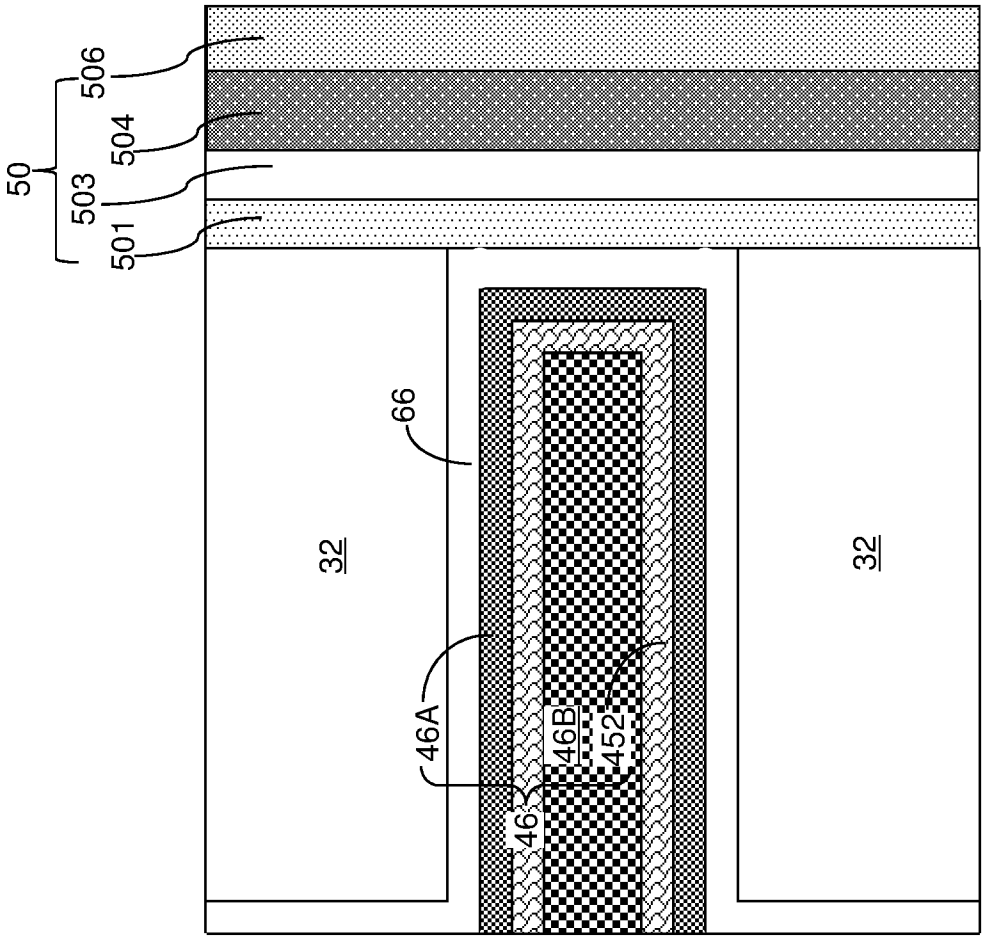


FIG. 10E

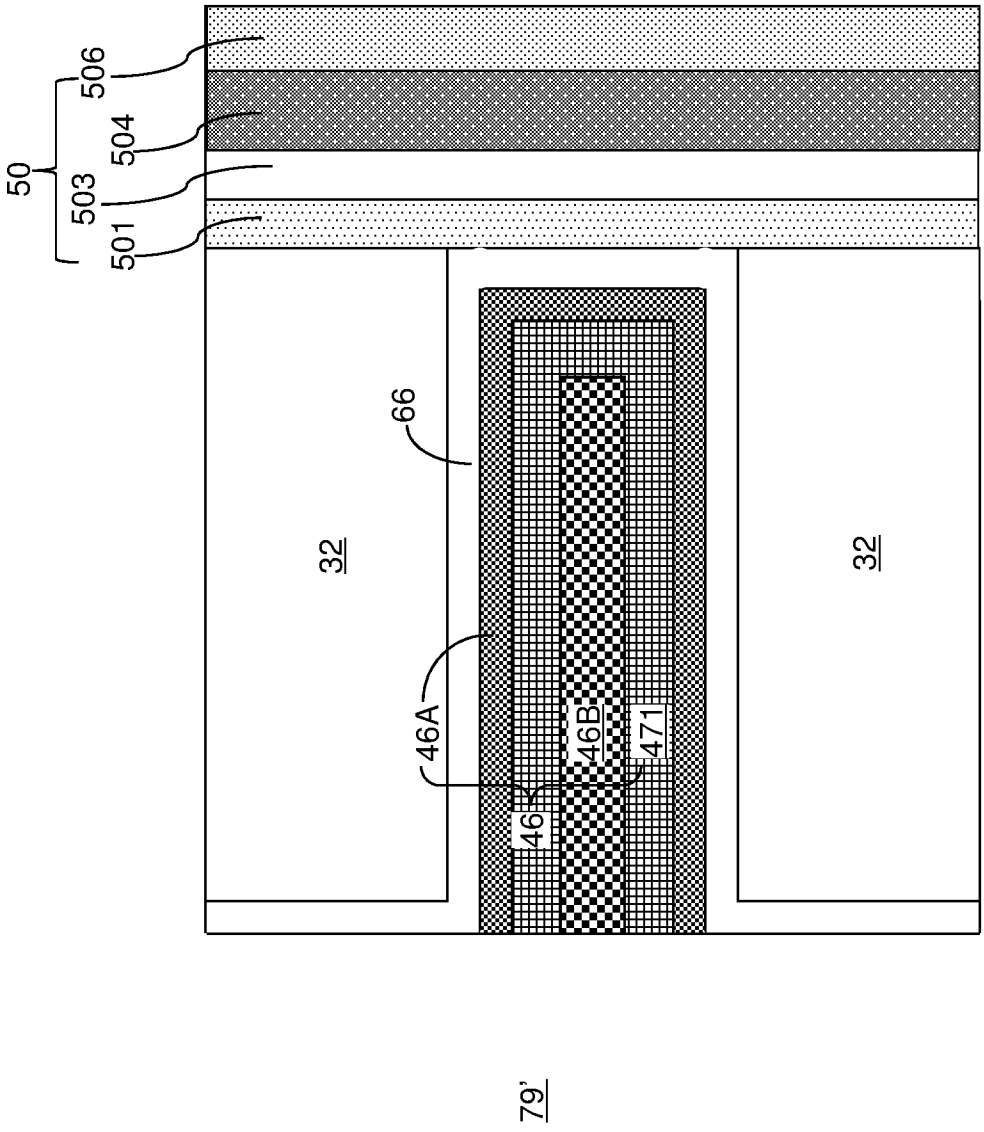


FIG. 10F

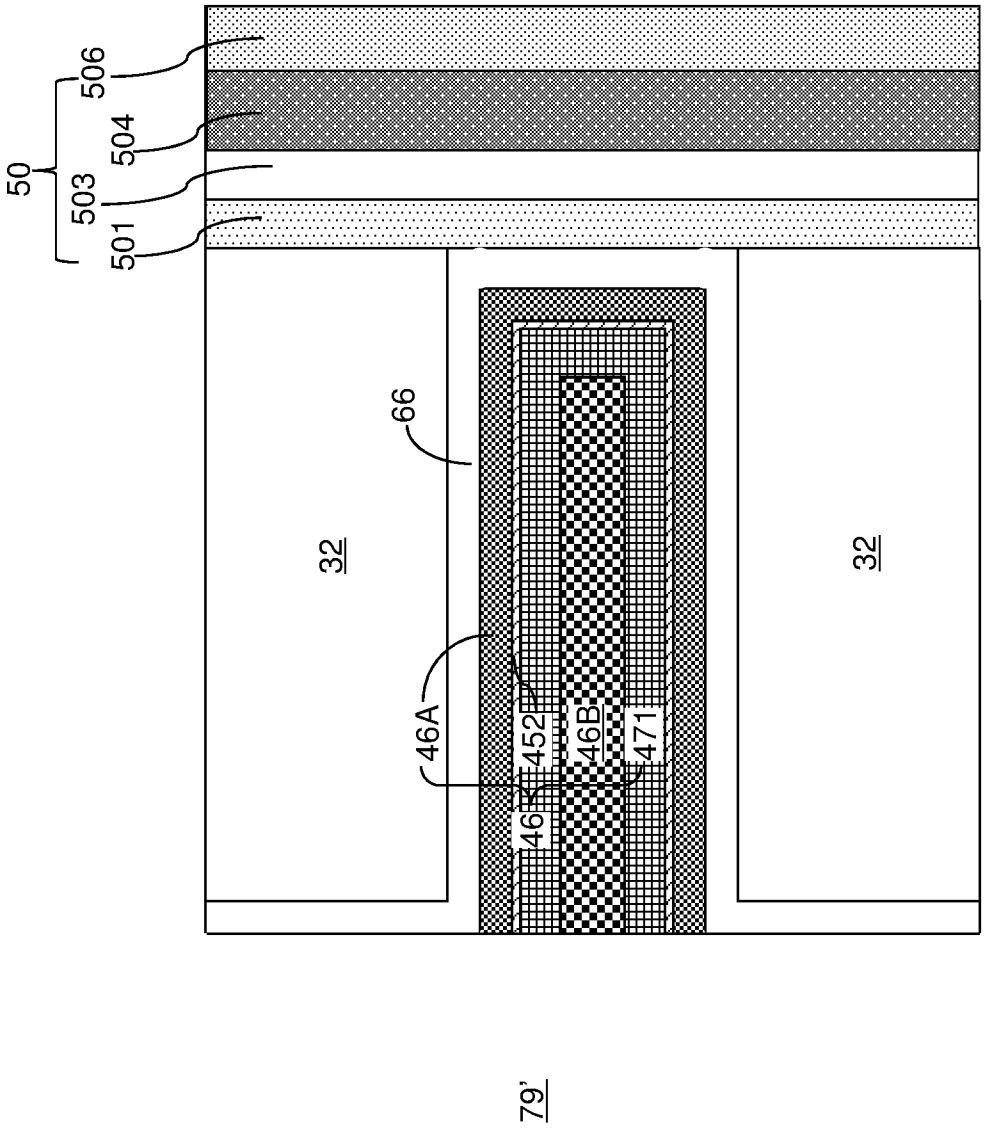


FIG. 10G

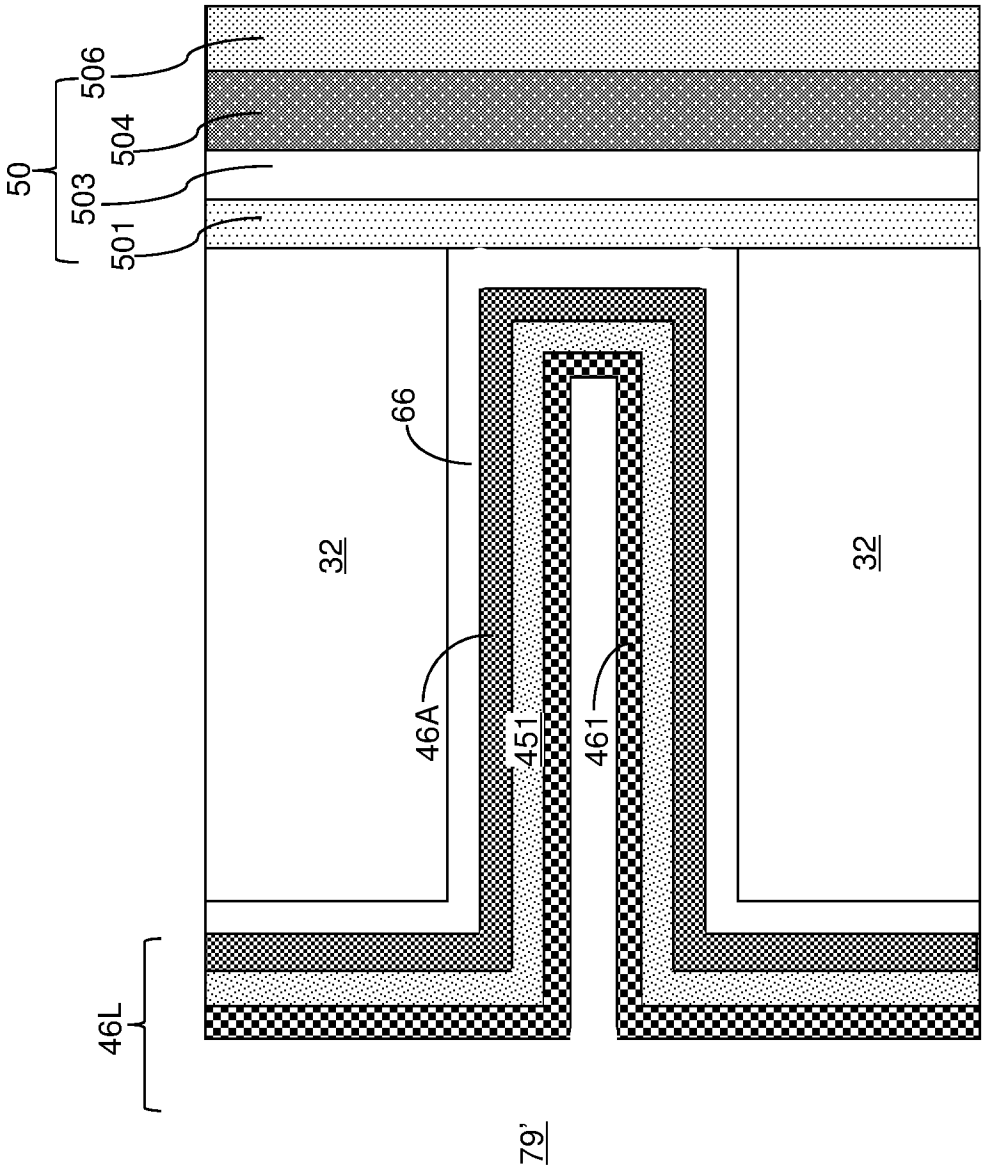


FIG. 11A

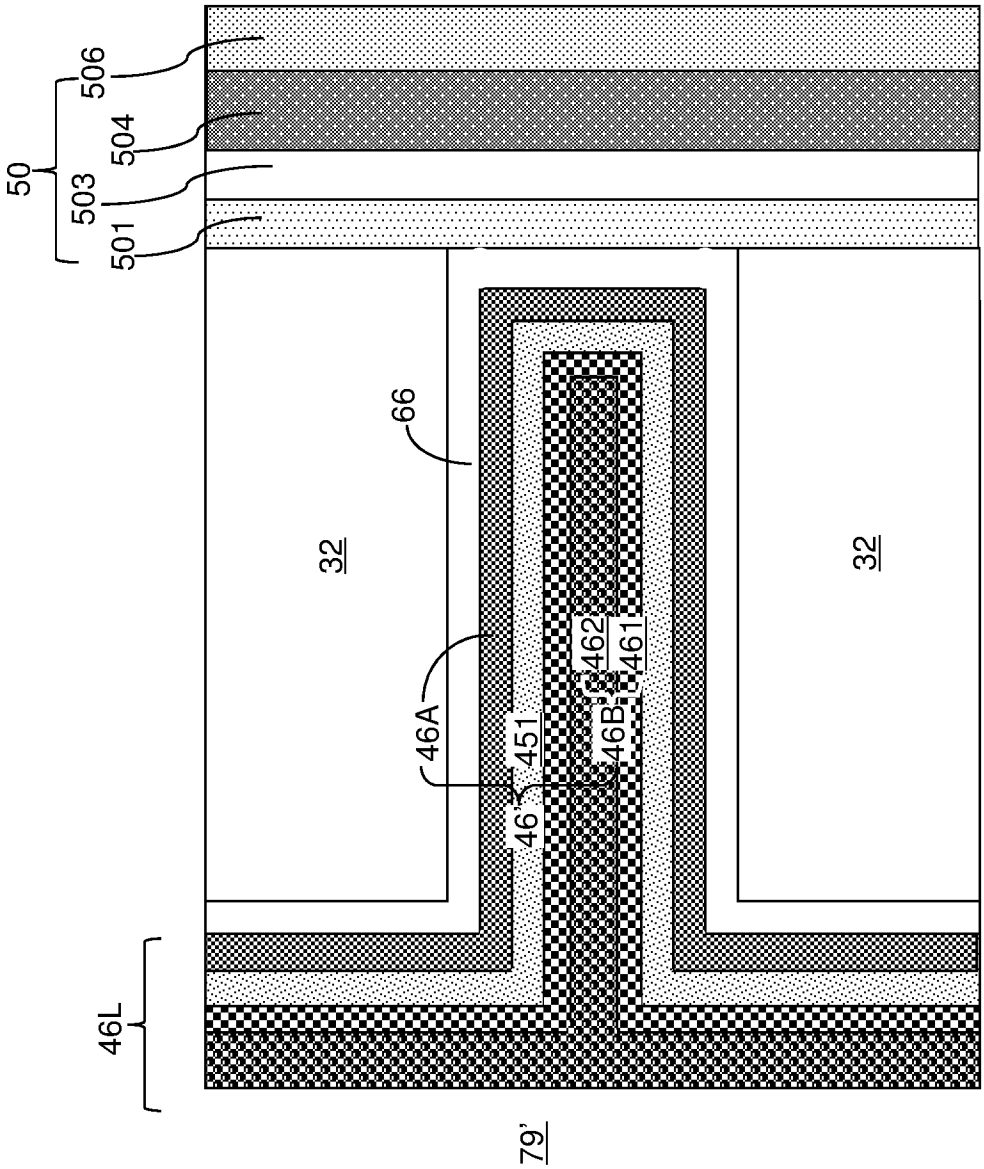


FIG. 11B

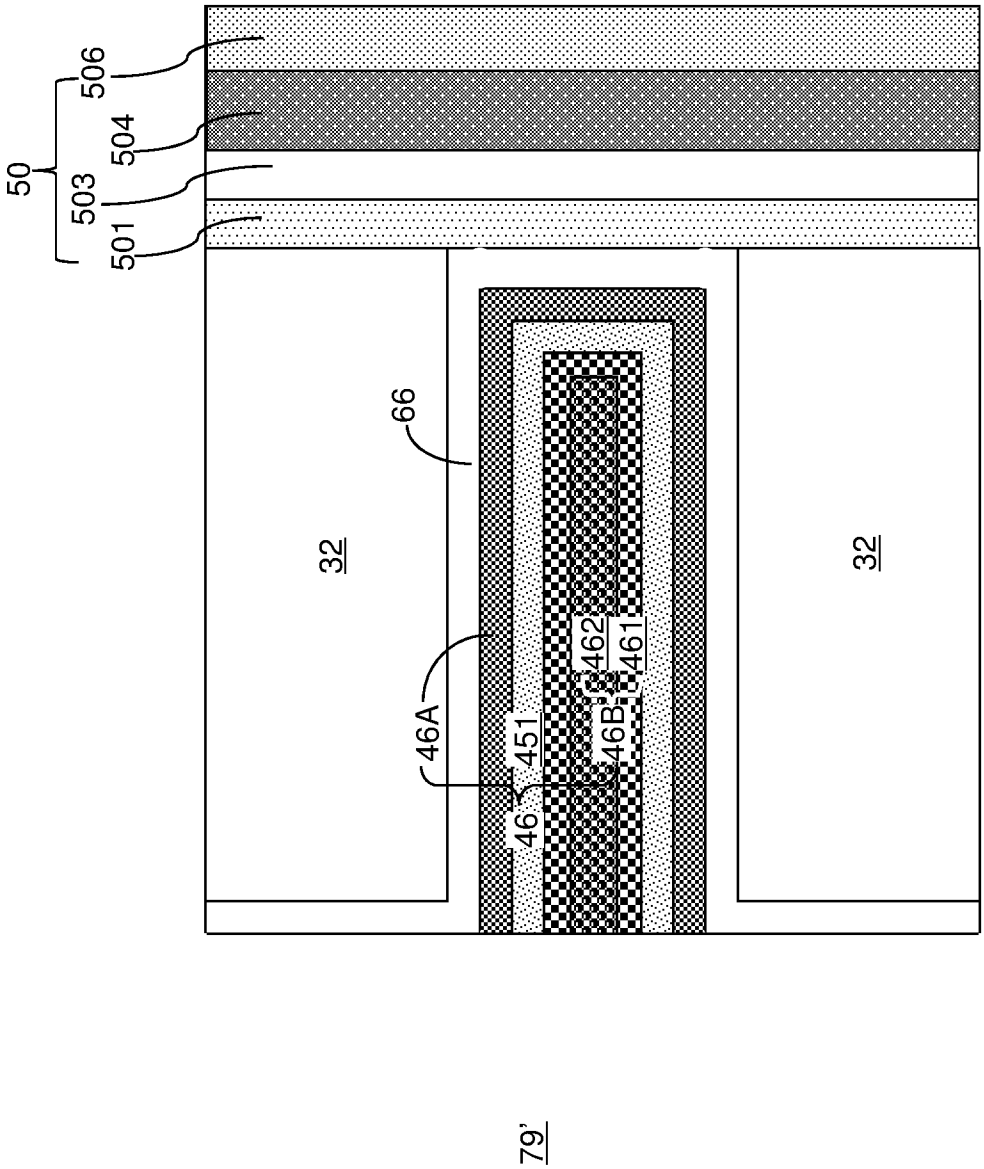


FIG. 11C

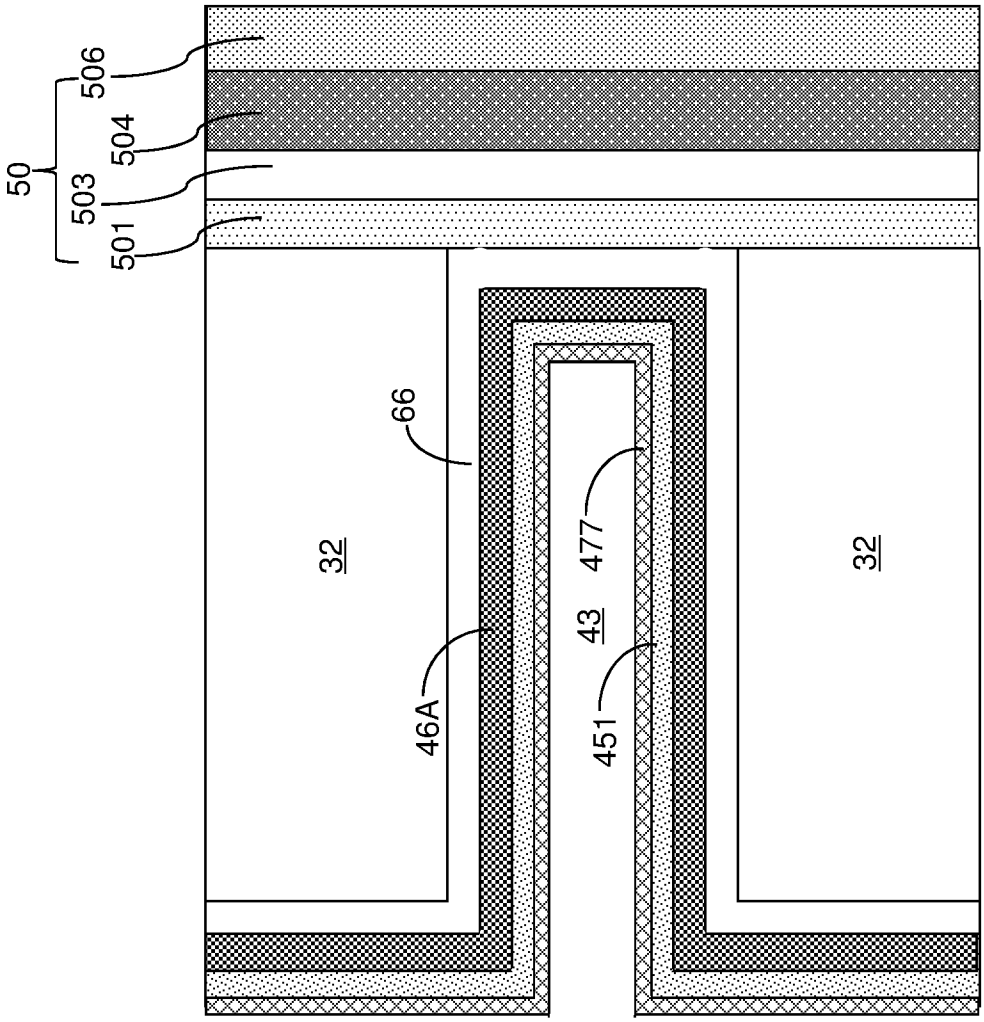


FIG. 12A

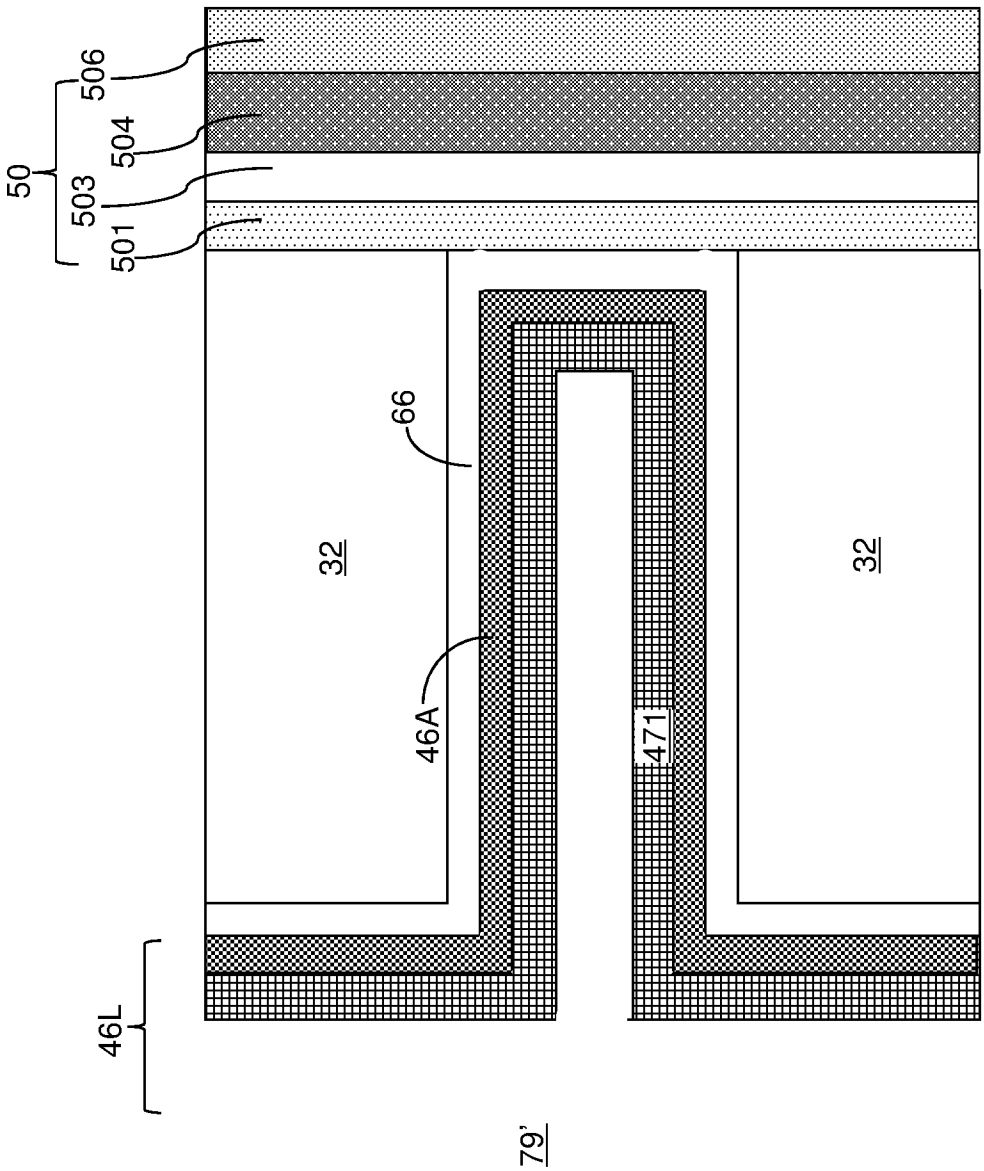


FIG. 12B

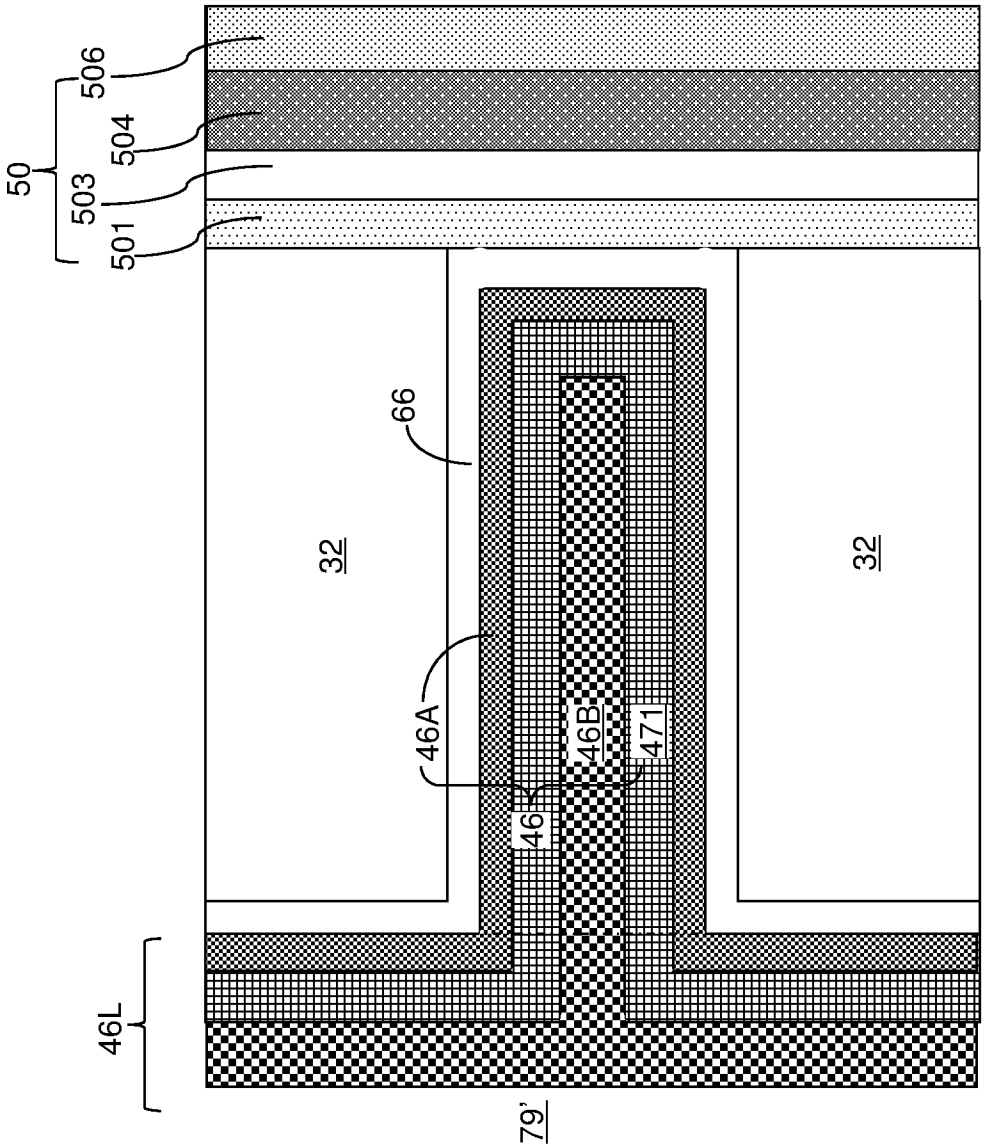


FIG. 12C

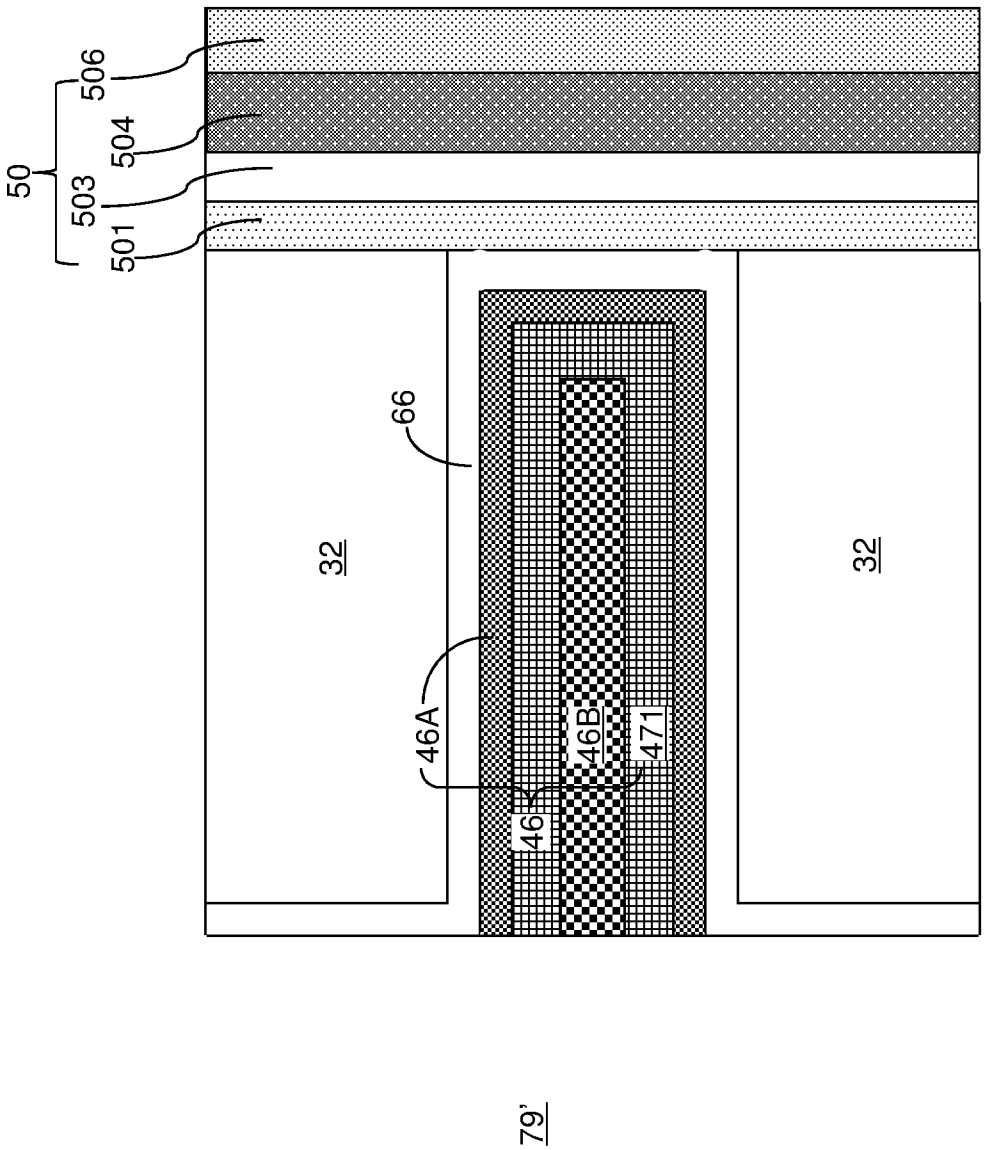


FIG. 12D

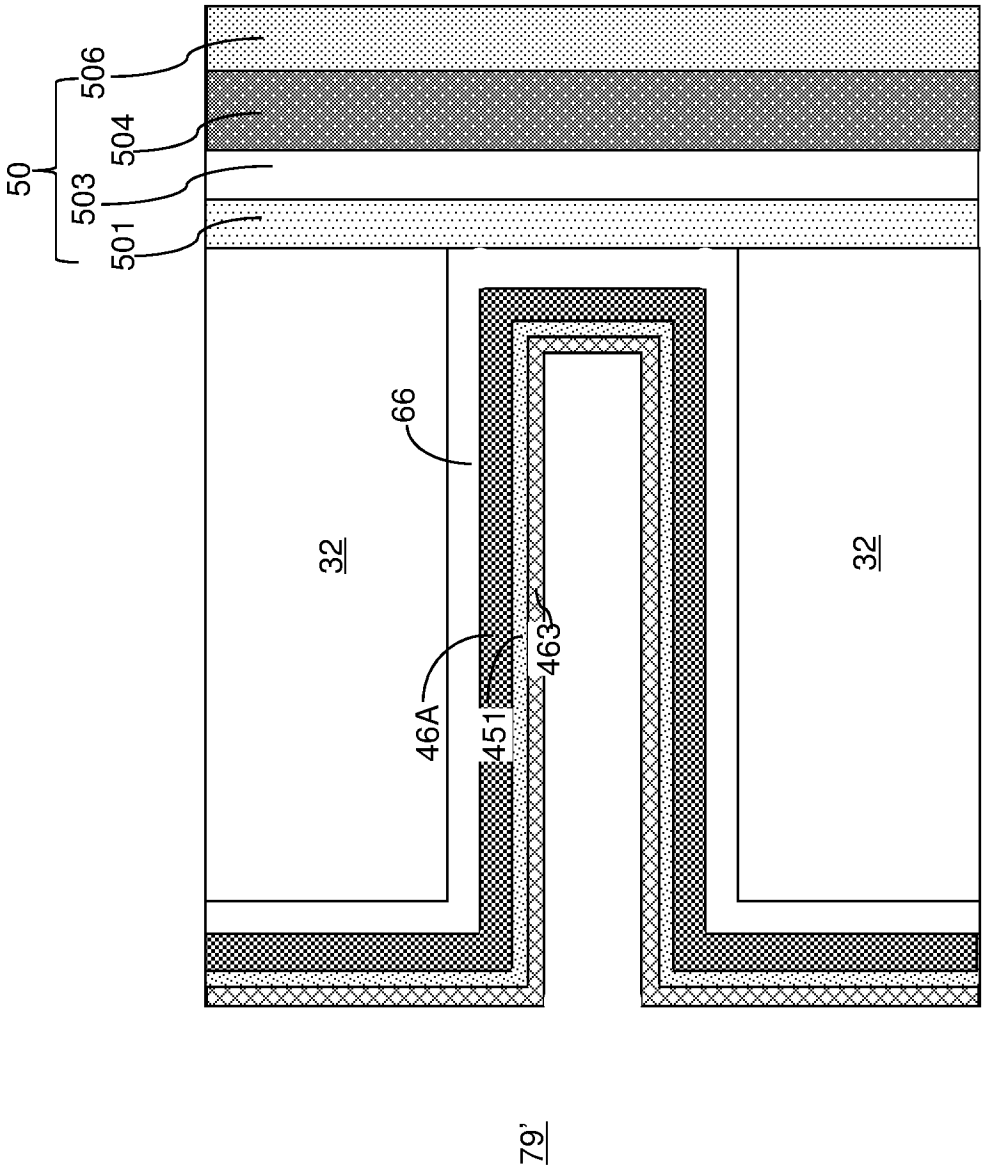


FIG. 13A

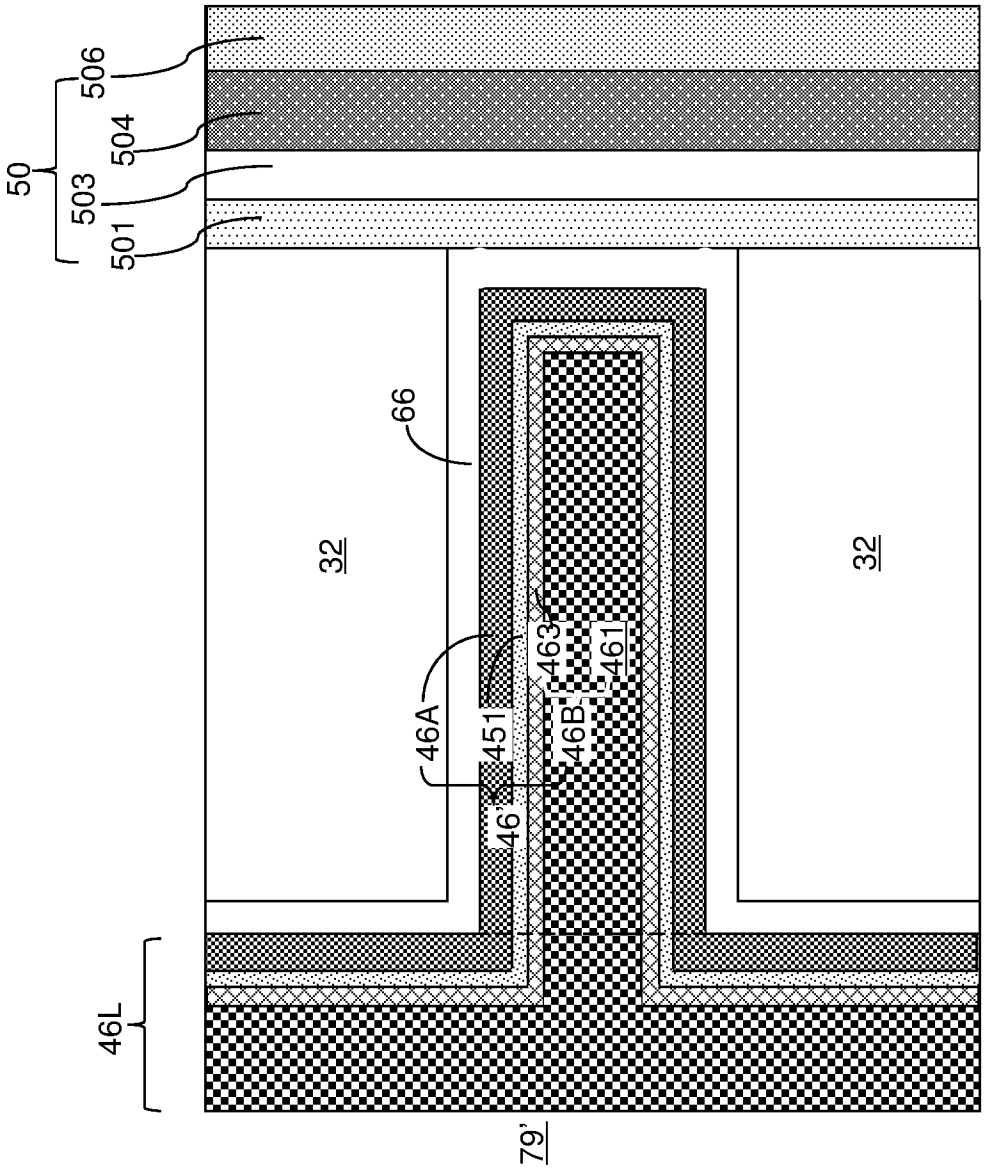


FIG. 13B

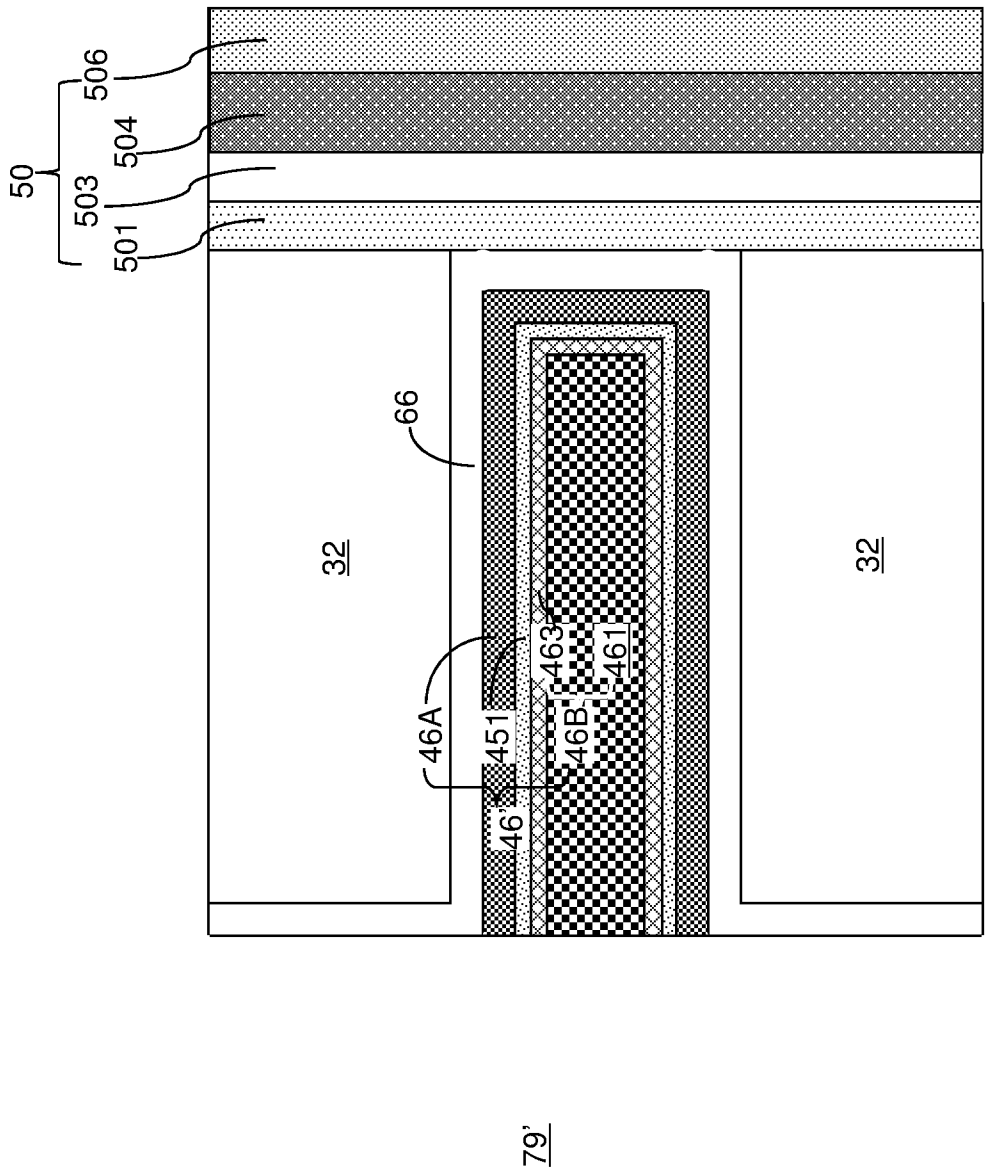


FIG. 13C

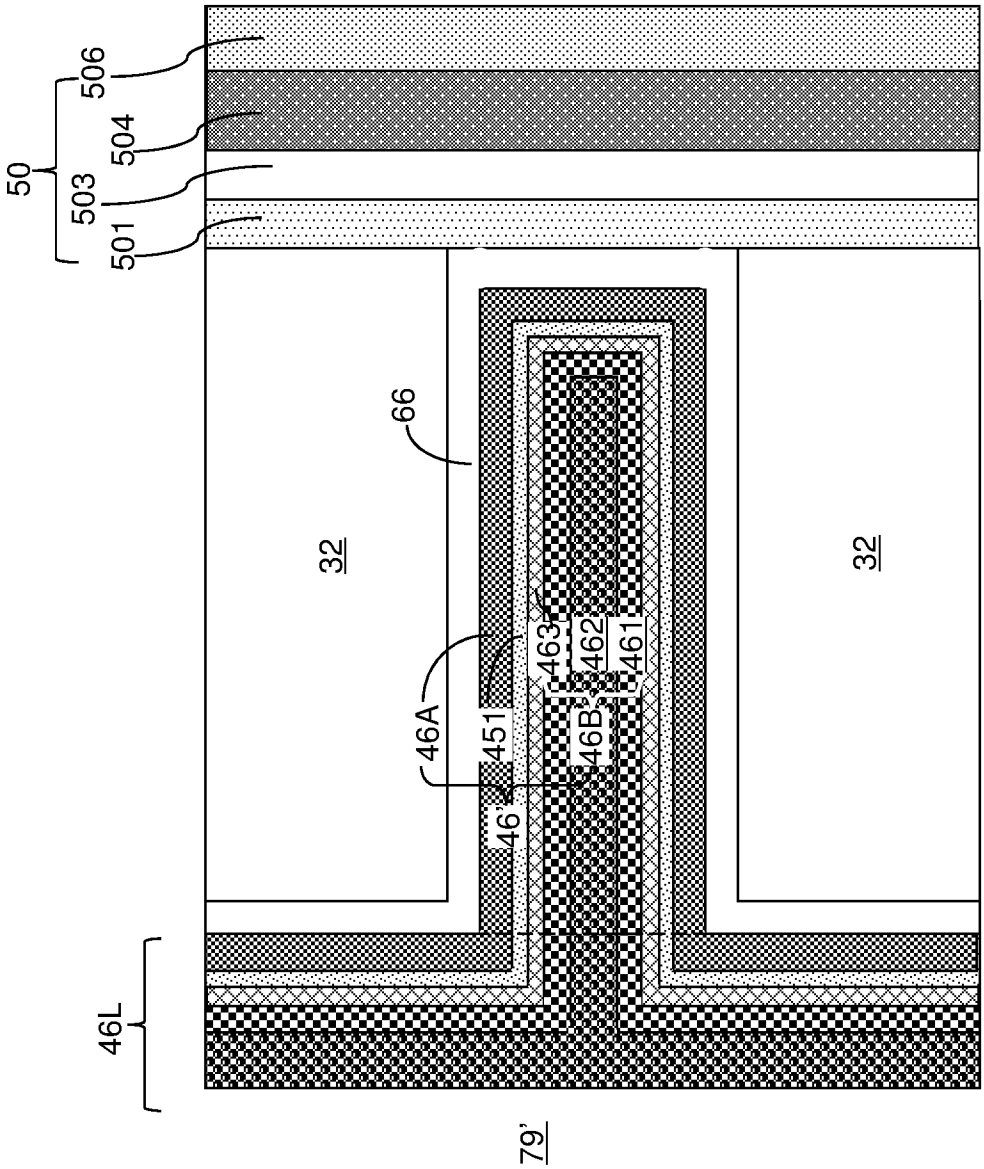


FIG. 14A

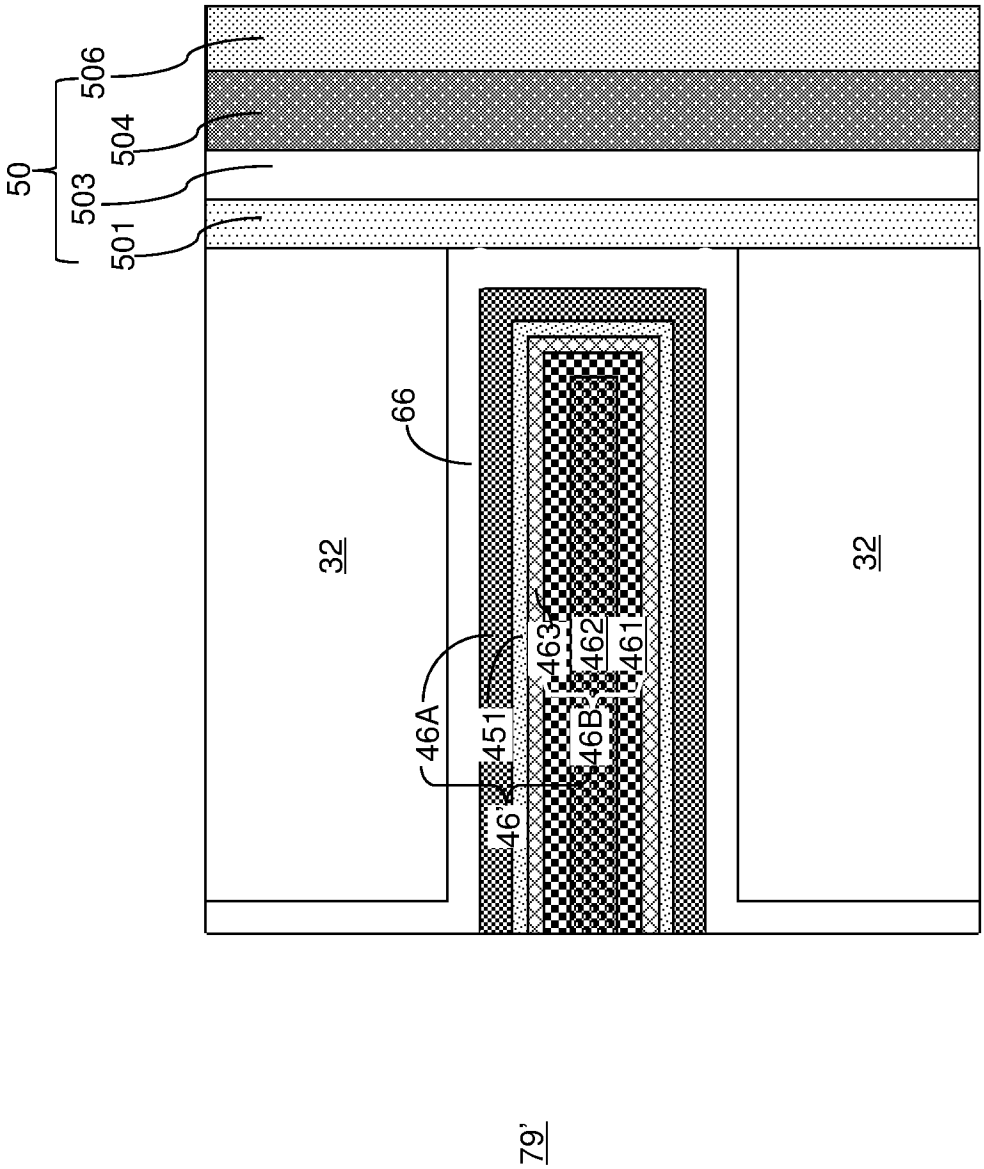


FIG. 14B

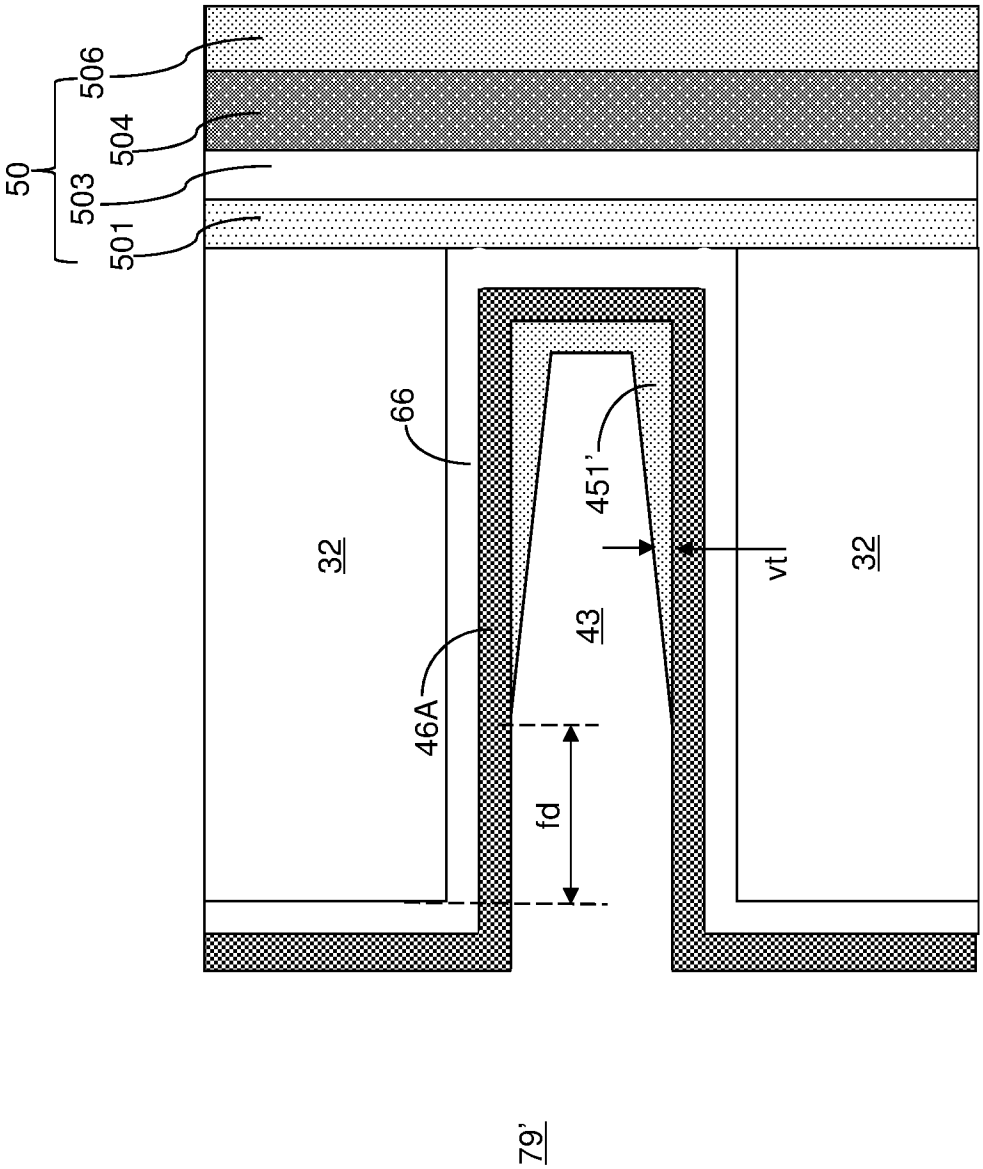


FIG. 15A

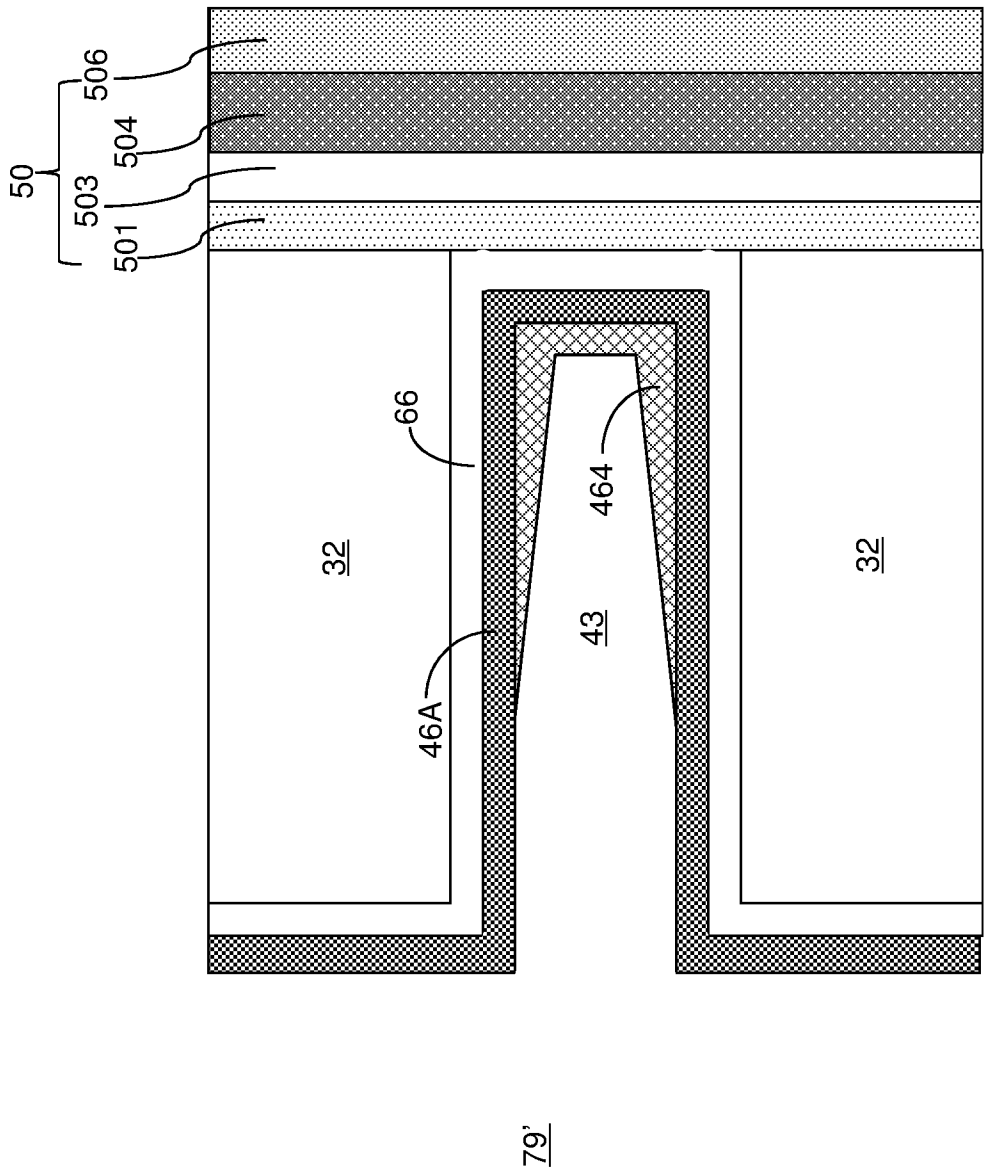


FIG. 15B

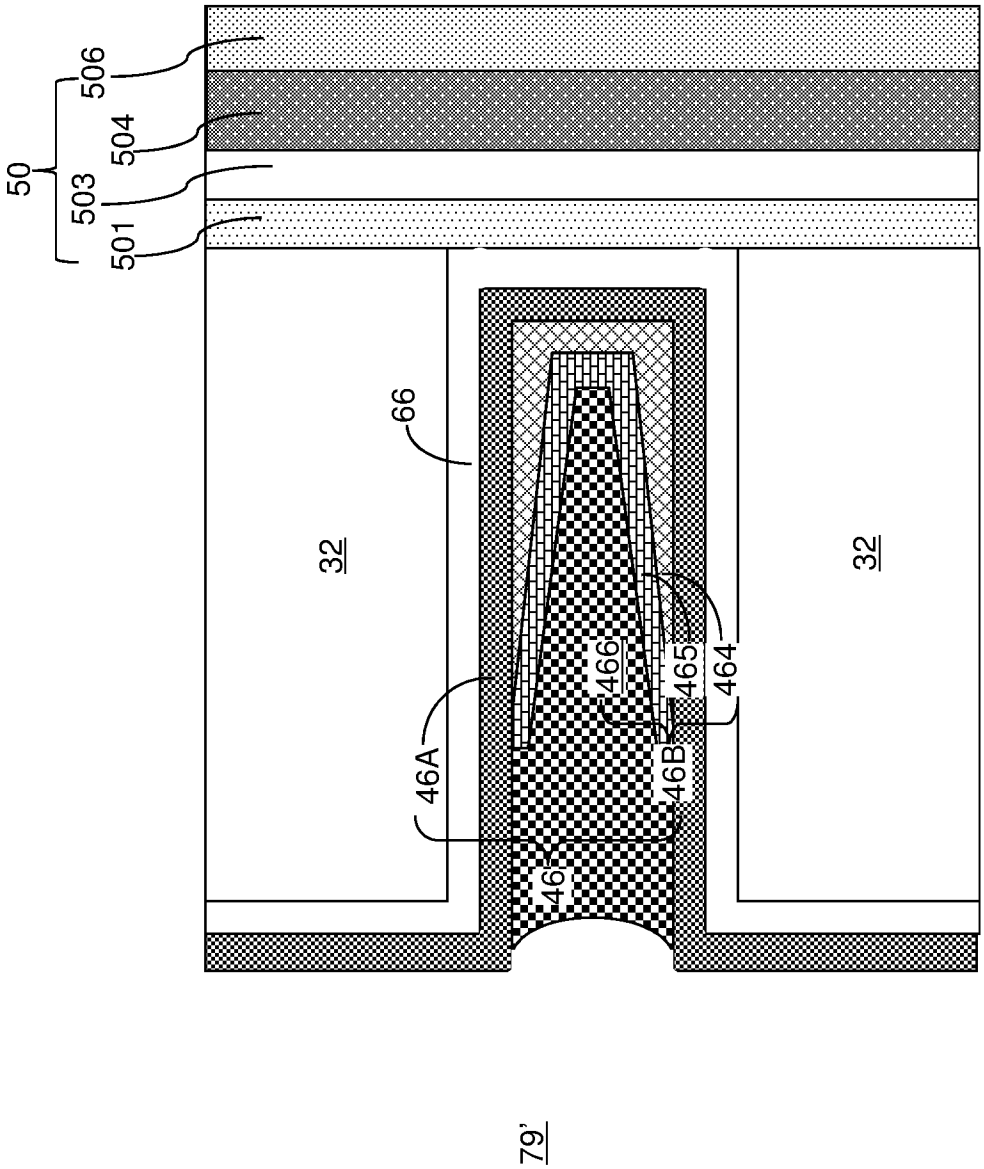


FIG. 15C

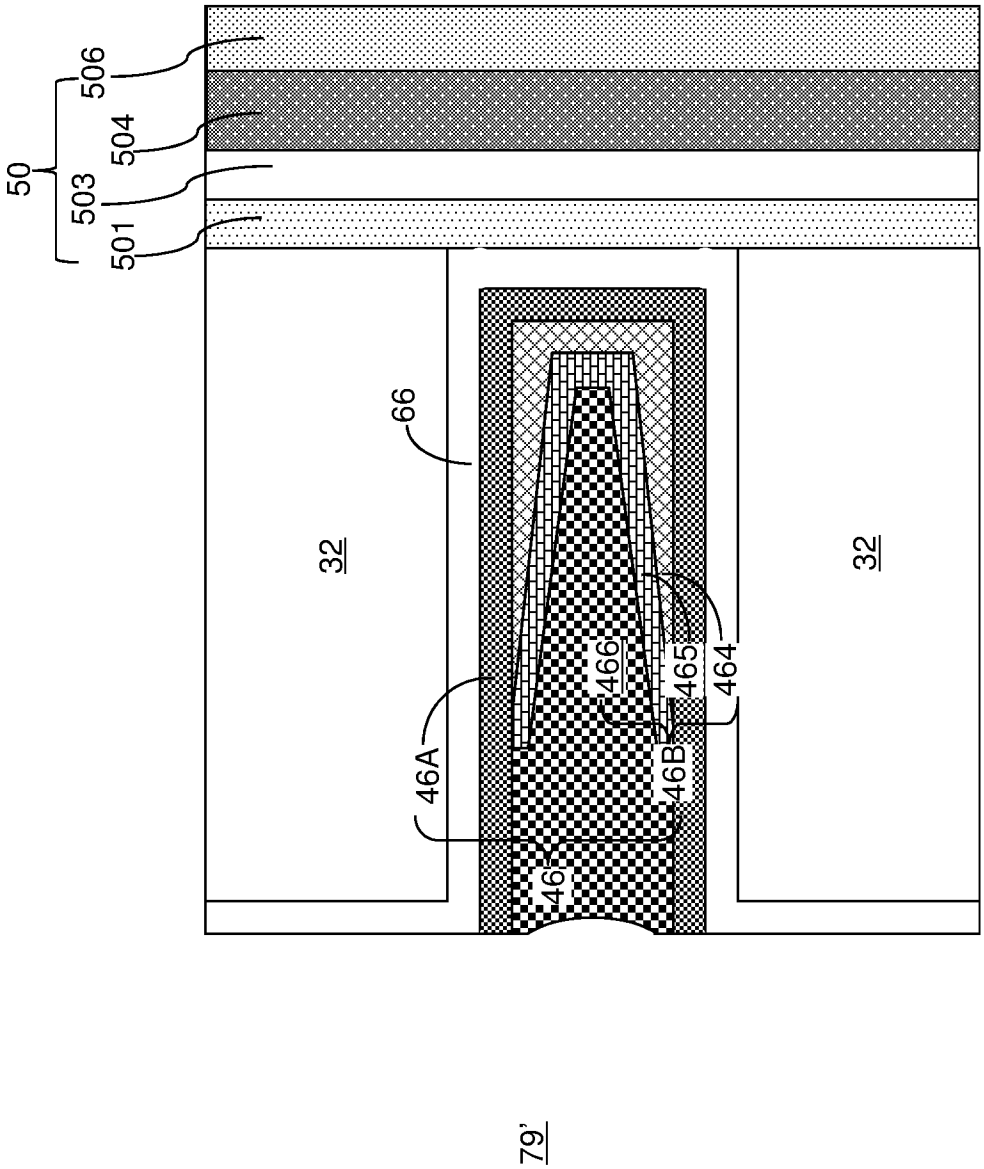


FIG. 15D

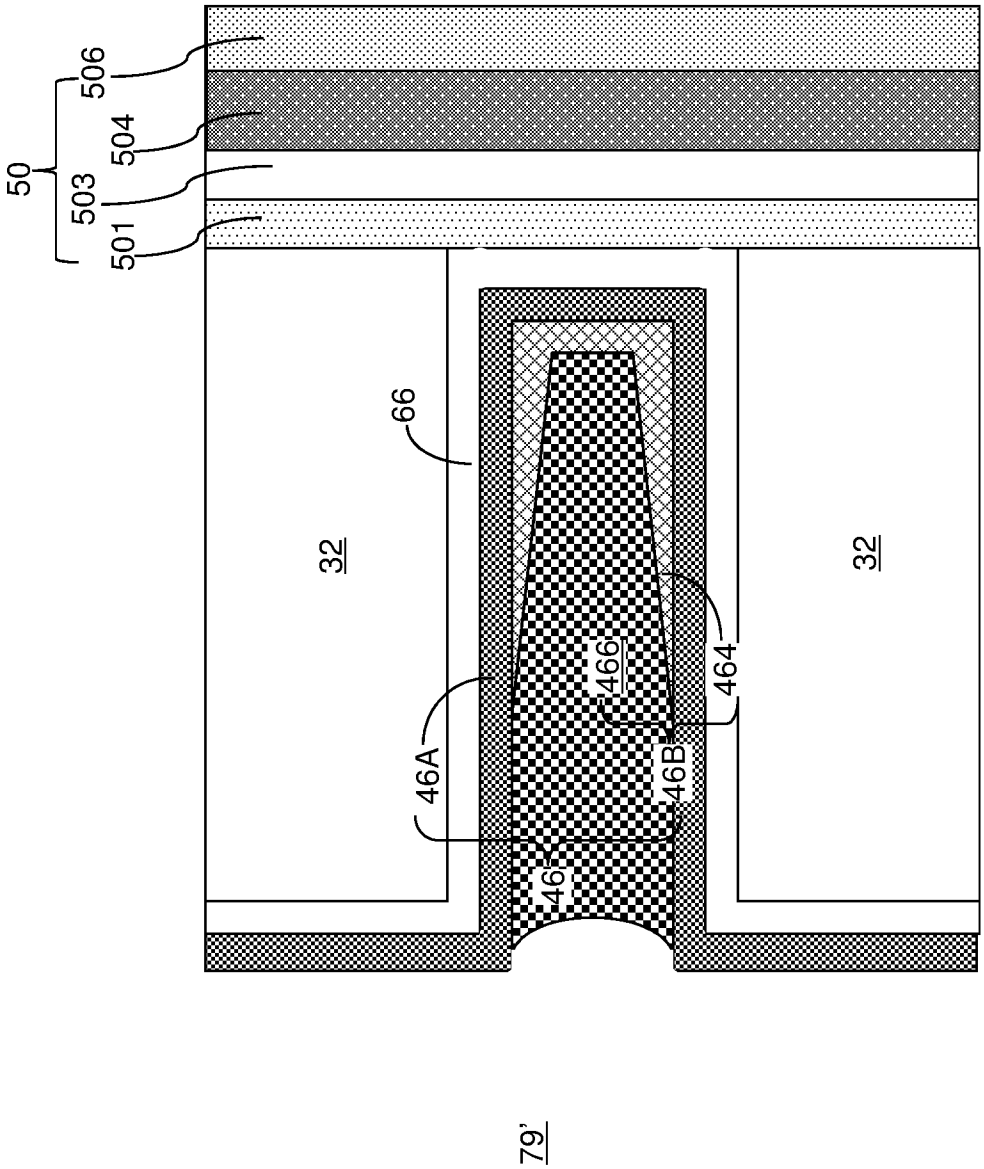


FIG. 16A

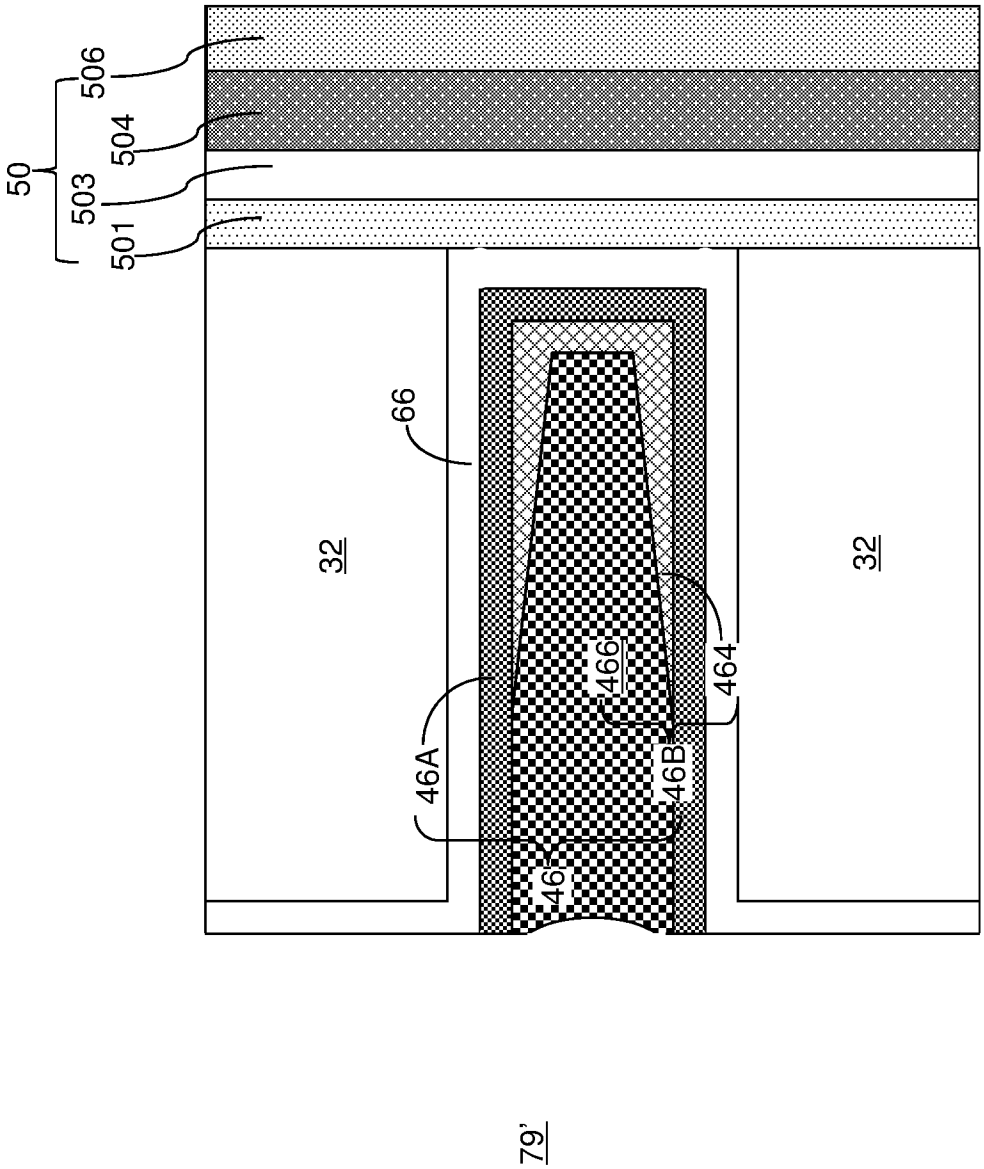


FIG. 16B

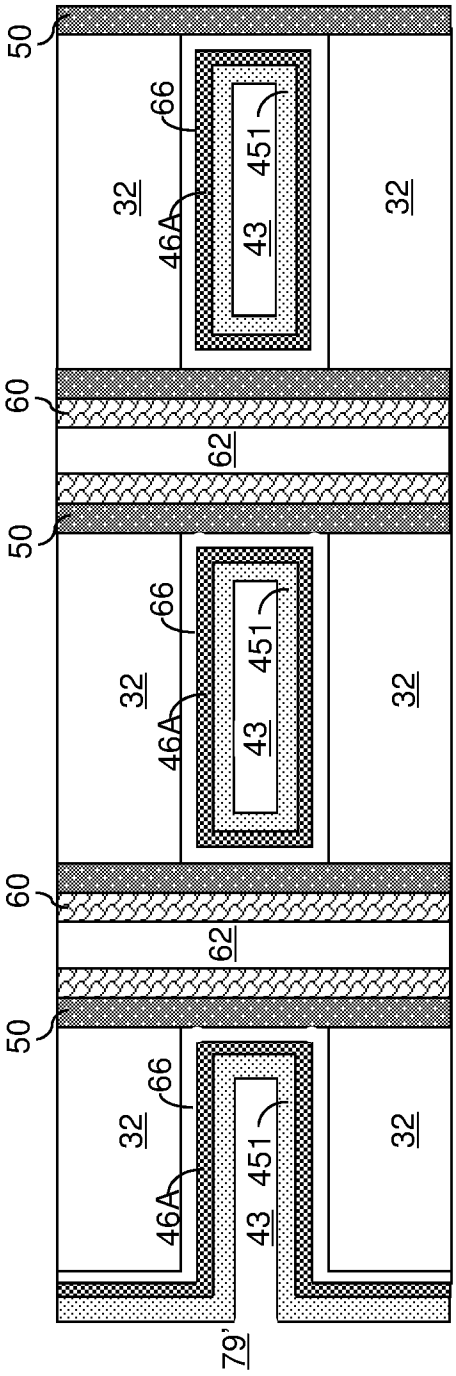


FIG. 17A

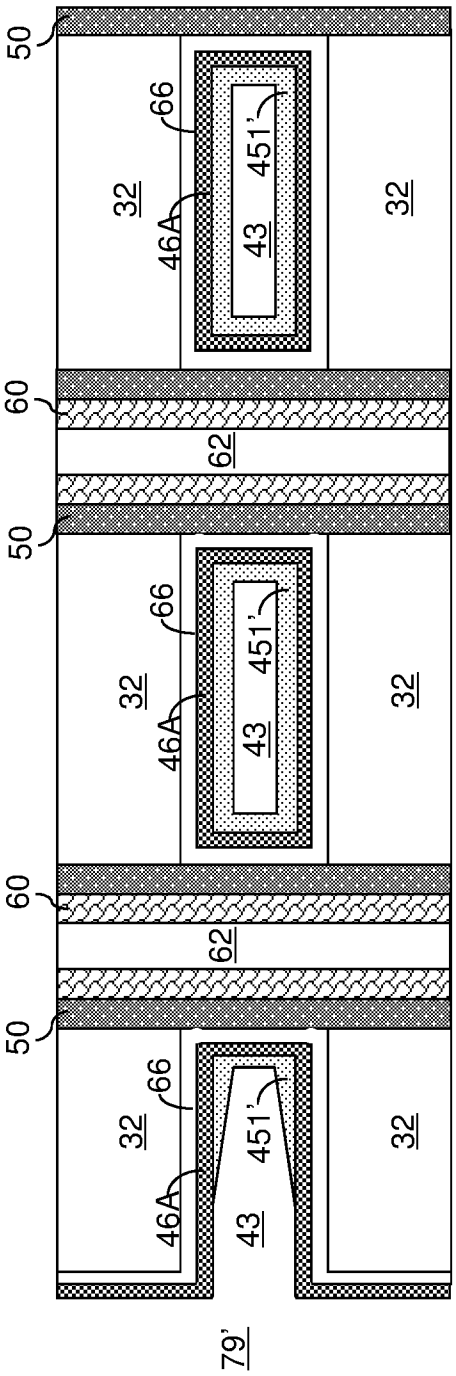


FIG. 17B

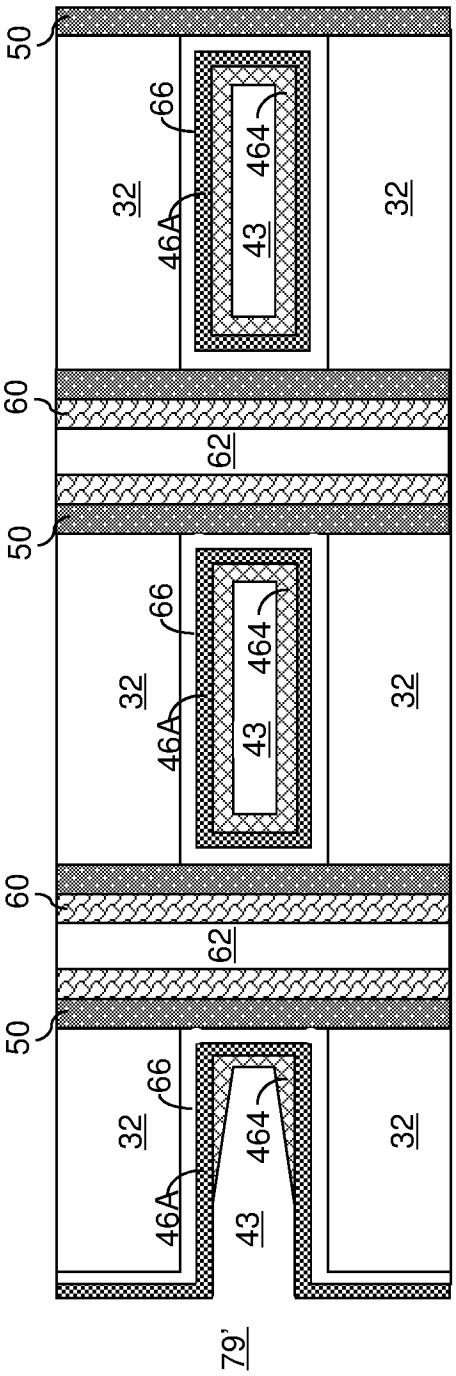


FIG. 17C

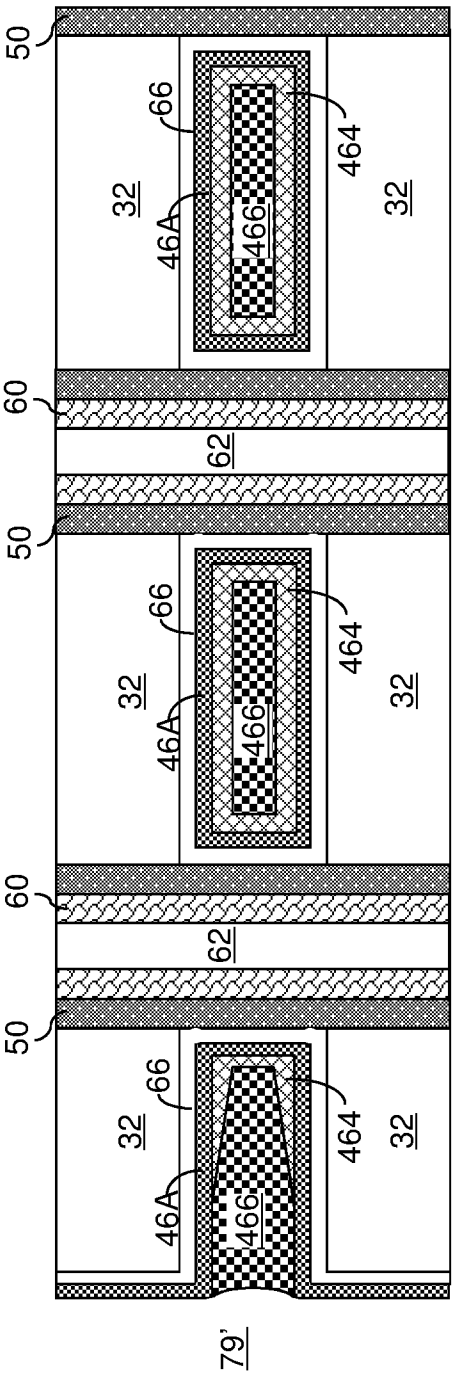


FIG. 17D

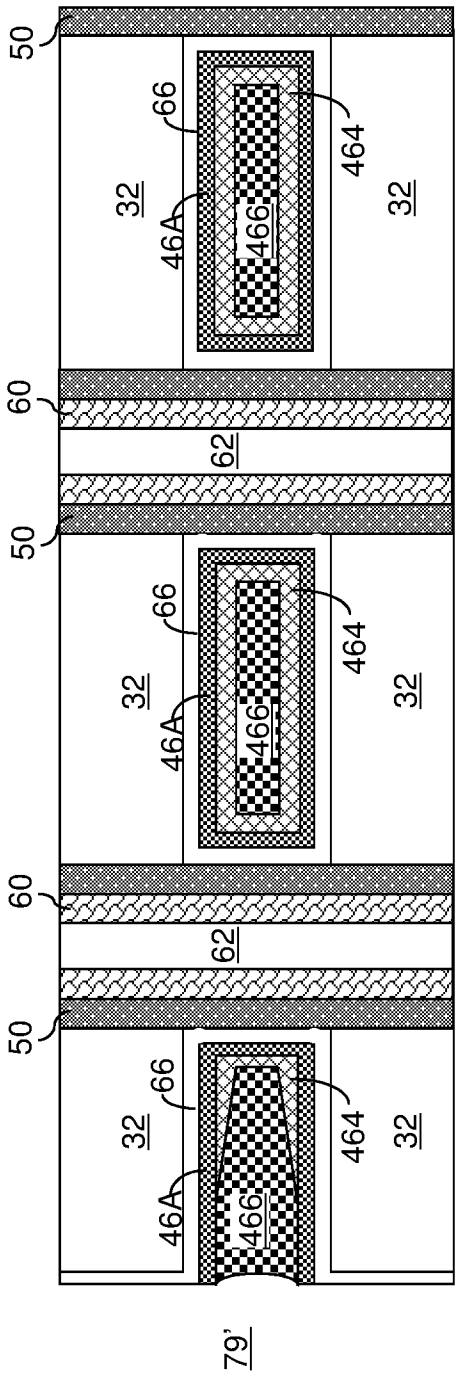

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FIG. 17E

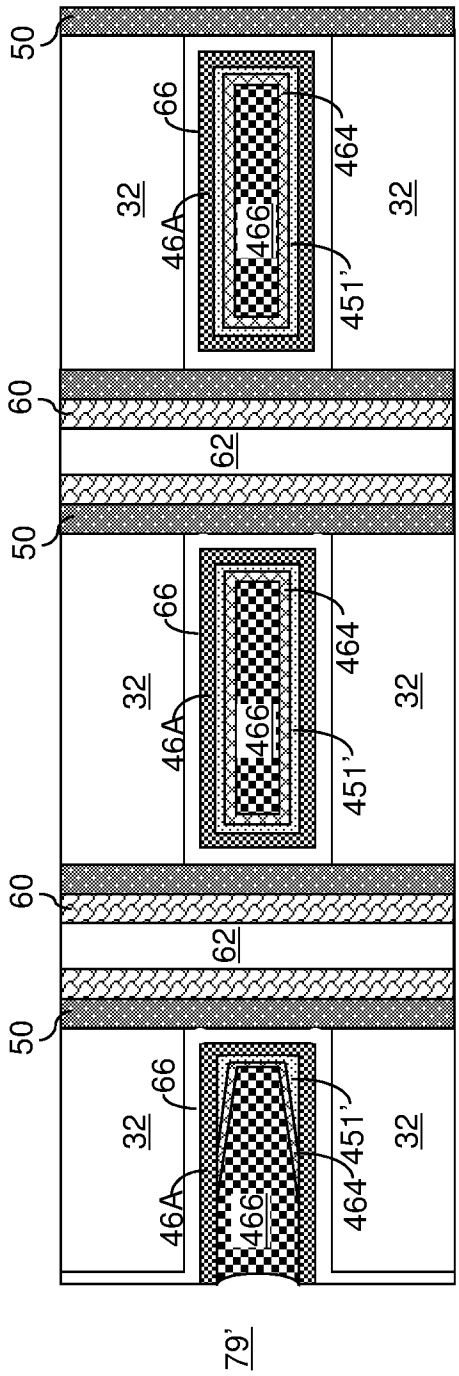

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FIG. 17F

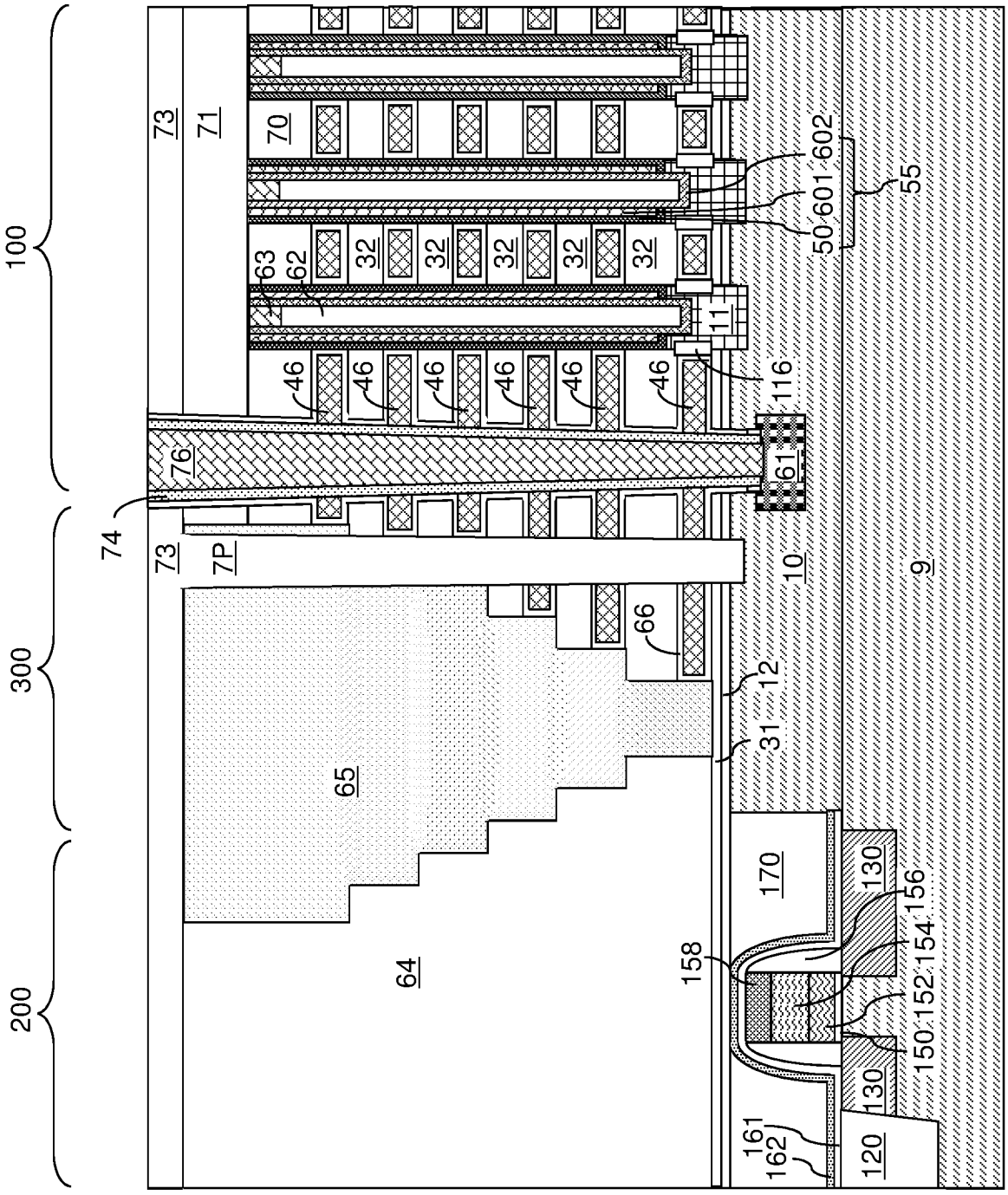

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FIG. 18

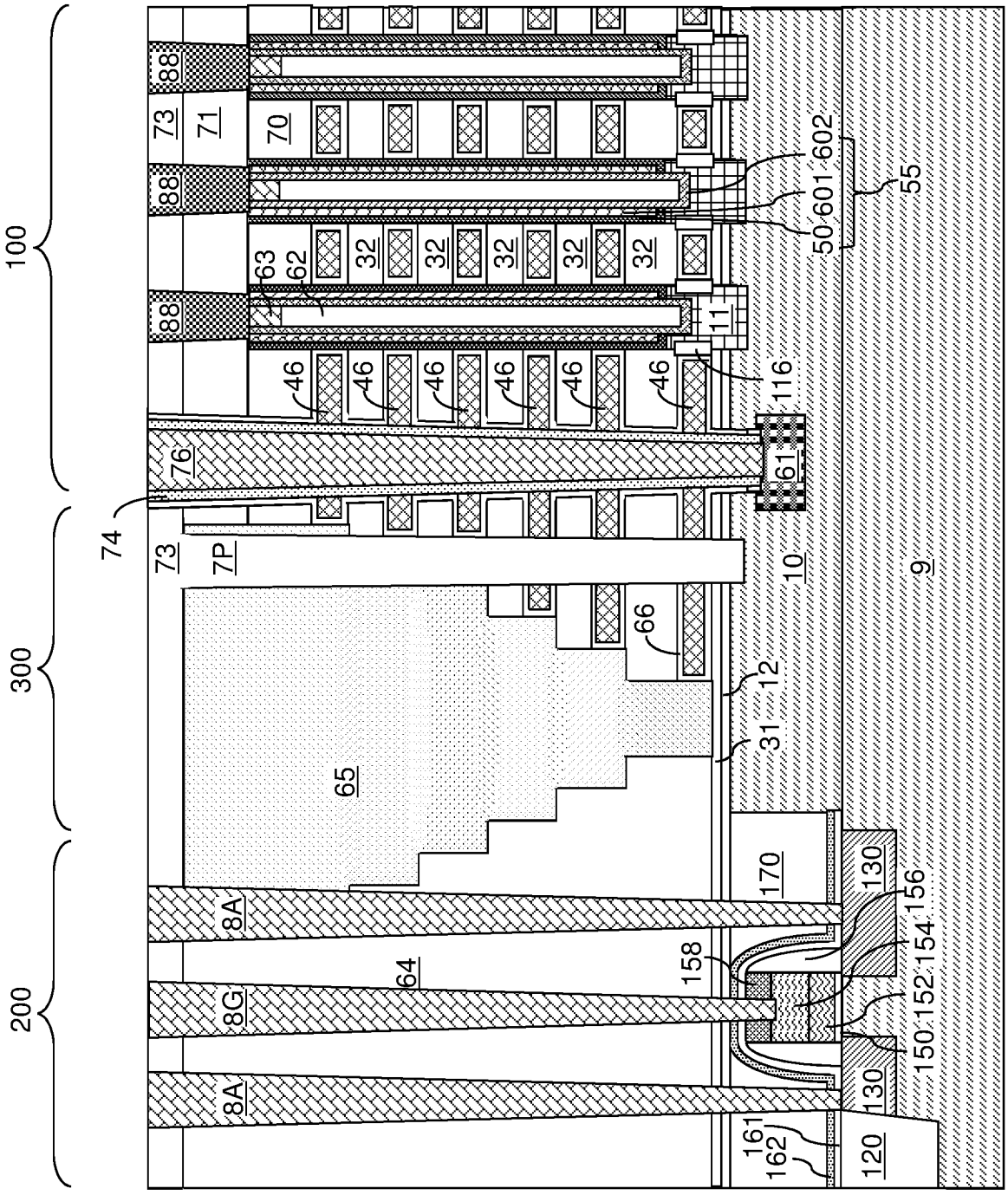

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FIG. 19

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/049496

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/115 H01L21/285
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015/243675 A1 (LIM TAI-SOO [KR] ET AL) 27 August 2015 (2015-08-27) paragraphs [0058] - [0120]; figures 3-20	1-5,7,8, 20,21
X	US 2011/303971 A1 (LEE CHANGWON [KR] ET AL) 15 December 2011 (2011-12-15) paragraphs [0046] - [0115], [0122] - [0138]; figures 3-9, 13, 17-24	1-8,20, 21

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 November 2016	25/01/2017

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Ley, Marc

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/049496

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-8, 20, 21

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-8, 20, 21

   a method according to claim 6
   ---

2. claim: 9

   a method according to claim 9
   ---

3. claims: 10-12

   a method according to claim 10
   ---

4. claims: 13-19

   a method according to claim 13 or claim 19
   ---

5. claims: 22-27

   a device according to claim 22

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2016/049496

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2015243675 A1	27-08-2015	KR 20150100066 A	02-09-2015
		US 2015243675 A1	27-08-2015
US 2011303971 A1	15-12-2011	KR 20110135692 A	19-12-2011
		US 2011303971 A1	15-12-2011