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(54) Title: HIGH BREAKDOWN N-TYPE BURIED LAYER

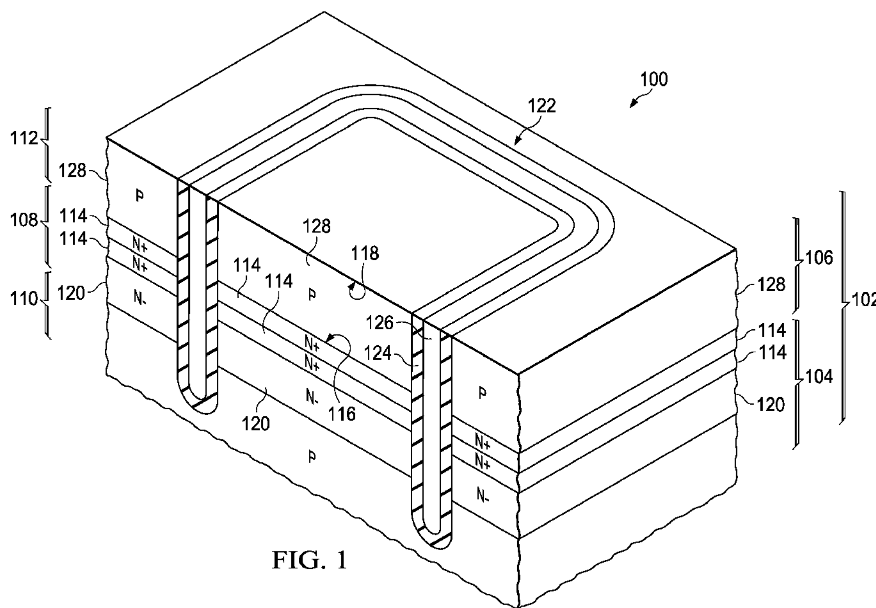

FIG. 1

(57) Abstract: In described examples, a semiconductor device (100) has an n-type buried layer (108) formed by implanting antimony and/or arsenic into a p-type first epitaxial layer (104) at a high dose and low energy, and implanting phosphorus at a low dose and high energy. A thermal drive process diffuses and activates both the heavy dopants and the phosphorus. The antimony and arsenic do not diffuse significantly, maintaining a narrow profile for a main layer (114) of the buried layer (108). The phosphorus diffuses to provide a lightly-doped layer (120) several microns thick below the main layer (114). An epitaxial p-type layer (106) is grown over the buried layer (108).

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— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

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HIGH BREAKDOWN N-TYPE BURIED LAYER

[0001] This relates generally to semiconductor devices, and more particularly to buried layers in semiconductor devices.

BACKGROUND

[0002] An example semiconductor device contains an n-type buried layer in a p-type substrate. The buried layer is biased to a high voltage, above 80 volts, to provide isolated operation at high voltage for a component in the substrate above the buried layer. At the bottom surface of the buried layer, the pn junction exhibits undesirable leakage current and low breakdown.

SUMMARY

[0003] In described examples, a semiconductor device has an n-type buried layer over a p-type first epitaxial layer and under a p-type second epitaxial layer. The buried layer is formed by implanting heavy n-type dopants, antimony and/or arsenic, into the p-type first epitaxial layer at a high dose and low energy, and implanting a lighter n-type dopant, phosphorus, at a low dose and high energy. A thermal drive process diffuses and activates both the heavy dopants and the phosphorus. The heavy dopants do not diffuse significantly, advantageously maintaining a narrow profile for a main layer of the buried layer. The phosphorus diffuses to advantageously provide a lightly-doped layer several microns thick below the main layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 is a cross section of an example semiconductor device containing a high voltage n-type buried layer.

[0005] FIGS. 2A through 2F are cross sections of a semiconductor device, similar to the semiconductor device of FIG. 1, shown in successive stages of fabrication.

[0006] FIGS. 3A through 3F are cross sections of another example semiconductor device containing a high voltage localized n-type buried layer, depicted in successive stages of fabrication.

[0007] FIG. 4 is a cross section of an alternate example semiconductor device containing a high voltage n-type buried layer.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0008] The following co-pending patent applications are hereby incorporated by reference: Application No. US 14/555,209; Application No. US 14/555,300; and Application No. US 14/555,359.

[0009] FIG. 1 is a cross section of an example semiconductor device containing a high voltage n-type buried layer. The semiconductor device 100 has a substrate 102, which includes a first epitaxial layer 104 of semiconductor material, such as single crystal silicon. The substrate 102 also includes a second epitaxial layer 106 disposed on the first epitaxial layer 104. The second epitaxial layer 106 includes a semiconductor material, which may have a same composition as the first epitaxial layer 104. An n-type buried layer 108 is disposed in the substrate 102 at a boundary between the first epitaxial layer 104 and the second epitaxial layer 106, extending into the first epitaxial layer 104 and the second epitaxial layer 106. The first epitaxial layer 104 immediately below the n-type buried layer 108 is referred to as a lower layer 110. The lower layer 110 is p-type and has a resistivity of 5 ohm-cm to 10 ohm-cm. The second epitaxial layer 106 above the n-type buried layer 108 is referred to as an upper layer 112. The upper layer 112 is p-type and has a resistivity of 5 ohm-cm to 10 ohm-cm.

[0010] The n-type buried layer 108 includes a main layer 114, which straddles the boundary between the first epitaxial layer 104 and the second epitaxial layer 106, extending at least a micron into the first epitaxial layer 104 and at least a micron into the second epitaxial layer 106. The main layer 114 has an average doping density greater than 5×10^{18} cm^{-3}. At least 50 percent of the n-type dopants in the main layer 114 are arsenic and/or antimony. A top surface 116 of the main layer 114 is at least 5 microns below a top surface 118 of the substrate 102. The top surface 116 of the main layer 114 may be 8 microns to 12 microns below the top surface 118 of the substrate 102.

[0011] The n-type buried layer 108 includes a lightly-doped layer 120 extending at least 2 microns below the main layer 114. The lightly-doped layer 120 is disposed in the first epitaxial layer 104 over the lower layer 110. The lightly-doped layer 120 has an average doping density of 1×10^{16} cm^{-3} to 1×10^{17} cm^{-3}. At least 90 percent of the n-type dopants in the lightly-doped layer 120 are phosphorus. The n-type buried layer 108 may extend substantially across the semiconductor device 100 as indicated in FIG. 1.

[0012] During operation of the semiconductor device 100, the n-type buried layer 108 may be

biased 80 volts to 110 volts higher than the lower layer 110. The structure of the n-type buried layer 108 with the lightly-doped layer 120 may advantageously prevent breakdown of a pn junction between the n-type buried layer 108 and the lower layer 110, and may advantageously provide a desired low level of leakage current. Moreover, the structure of the n-type buried layer 108 with the main layer 114 advantageously provides a low sheet resistance to maintain a uniform bias for components in the upper layer 112 above the n-type buried layer 108.

[0013] The semiconductor device 100 may include a deep trench structure 122, which extends through the upper layer 112, through the n-type buried layer 108, and into the lower layer 110. The deep trench structure 122 includes a dielectric liner 124, including silicon dioxide contacting the semiconductor material of the substrate 102. The deep trench structure 122 may also include an electrically conductive fill material 126, such as polycrystalline silicon (referred to as polysilicon) on the dielectric liner 124. The structure of the n-type buried layer 108 with the lightly-doped layer 120 is especially advantageous for preventing breakdown of the pn junction between the n-type buried layer 108 and the lower layer 110 at the dielectric liner 124. The deep trench structure 122 may have a closed loop configuration as depicted in FIG. 1, so that a portion 128 of the upper layer 112 is electrically isolated from the remaining upper layer 112 by the deep trench structure 122 and is electrically isolated from the lower layer 110 by the n-type buried layer 108. Components in the portion 128 of the upper layer 112 may be advantageously operated at 85 volts to 110 volts relative to components in the remaining upper layer 112 outside the deep trench structure 122.

[0014] FIG. 2A through FIG. 2F are cross sections of a semiconductor device, similar to the semiconductor device of FIG. 1, shown in successive stages of fabrication. Referring to FIG. 2A, fabrication of the semiconductor device 100 starts with the first epitaxial layer 104. For example, the first epitaxial layer 104 may be a top portion of a stack of epitaxial layers on a heavily-doped single crystal silicon wafer. The first epitaxial layer 104 is p-type with a resistivity of 5 ohm-cm to 10 ohm-cm. A layer of pad oxide 130 is formed over the first epitaxial layer 104, such as by thermal oxidation.

[0015] N-type dopants 132 are implanted into the first epitaxial layer 104 to form a first implanted layer 134. The n-type dopants include at least 50 percent arsenic and/or antimony. In one version of this example, the n-type dopants 132 may be substantially all antimony, as indicated in FIG. 2A. The n-type dopants 132 are implanted at a dose greater than 5×10^{14} cm^{-2},

such as 1×10^{15} cm^{-2} to 5×10^{15} cm^{-2}. Antimony in the n-type dopants 132 may be implanted at energies less than 50 keV. Arsenic in the n-type dopants 132 may be implanted at energies less than 40 keV.

[0016] Referring to FIG. 2B, phosphorus 136 is implanted into the first epitaxial layer 104 to form a second implanted layer 138 below the first implanted layer 134. The phosphorus 136 is implanted at a dose of 1×10^{13} cm^{-2} to 1×10^{14} cm^{-2} and at an energy above 100 keV.

[0017] Referring to FIG. 2C, a first thermal drive process 140 heats the first epitaxial layer 104 to a temperature of 1150 °C to 1225 °C for at least 30 minutes. The first thermal drive process 140 may be performed in a furnace with an oxidizing ambient, which increases a thickness of the layer of pad oxide 130. The first thermal drive process 140 causes the implanted n-type dopants in the first implanted layer 134 and the implanted phosphorus in the second implanted layer 138 to diffuse deeper into the first epitaxial layer 104. The phosphorus in the second implanted layer 138 diffuses farther into the first epitaxial layer 104 than the arsenic and antimony in the first implanted layer 134. The layer of pad oxide 130 is subsequently removed, such as by a wet etch using a dilute aqueous solution of buffered hydrofluoric acid.

[0018] Referring to FIG. 2D, an epitaxy process grows the second epitaxial layer 106 on the first epitaxial layer 104. The epitaxy process may use silane, dichlorosilane, or other silicon-containing reagents. During the epitaxy process, the n-type dopants in the first implanted layer 134 of FIG. 2C diffuse into the second epitaxial layer 106, to form the main layer 114 of the n-type buried layer 108. The main layer 114 straddles the boundary between the first epitaxial layer 104 and the second epitaxial layer 106. The phosphorus in the second implanted layer 138 of FIG. 2C forms the lightly-doped layer 120 of the n-type buried layer 108. The epitaxy process may use a boron-containing reagent (such as diborane) to provide p-type doping in the second epitaxial layer 106. Alternatively, p-type dopants (such as boron) may be implanted into the second epitaxial layer 106 after the epitaxy process is completed. The first epitaxial layer 104 and the second epitaxial layer 106 provide a top portion of the substrate 102.

[0019] Referring to FIG. 2E, a second thermal drive process 142 heats the substrate 102 to a temperature of 1125 °C to 1200 °C for at least 120 minutes. The second thermal drive process 142 may be performed in a furnace with a slightly oxidizing ambient. When the second thermal drive is completed, the main layer 114 of the n-type buried layer 108 extends at least a micron into the first epitaxial layer 104 and at least a micron into the second epitaxial layer 106, and the

lightly-doped layer 120 extends at least 2 microns below the main layer 114. An average doping in the main layer 114 is greater than 5×10^{18} cm^{-3}. An average doping in the lightly-doped layer 120 is 1×10^{16} cm^{-3} to 1×10^{17} cm^{-3}.

[0020] Referring to FIG. 2F, the deep trench structure 122 may be formed by etching a deep trench in the substrate 102 after the second thermal drive process 142 of FIG. 2E. The dielectric liner 124 may be formed by thermal oxidation followed by deposition of silicon dioxide by a sub-atmospheric chemical vapor deposition (SACVD) process. The electrically conductive fill material 126 may be formed by depositing a conformal layer of polysilicon and subsequently removing the polysilicon from over a top surface of the substrate, such as by a chemical mechanical polish (CMP) process. Optional n-type self-aligned sinkers 144 may be formed in the second epitaxial layer 106 abutting the deep trench structures by implanting n-type dopants into the second epitaxial layer 106 after the deep trenches are partially etched. The n-type self-aligned sinkers 144 provide electrical connections to the n-type buried layer 108.

[0021] FIG. 3A through FIG. 3F are cross sections of another example semiconductor device containing a high voltage localized n-type buried layer, depicted in successive stages of fabrication. A localized n-type buried layer extends across only a portion of the semiconductor device. Referring to FIG. 3A, the semiconductor device 300 is formed on a first epitaxial layer 304 containing a semiconductor material, such as single crystal silicon. The first epitaxial layer 304 is p-type with a resistivity of 5 ohm-cm to 10 ohm-cm. A layer of pad oxide 330 is formed over the first epitaxial layer 304. In this example, an implant mask 346 is formed over the layer of pad oxide 330 to expose an area for the localized n-type buried layer 308. The implant mask 346 may include photoresist formed by a photolithographic process or may include hard mask material, such as silicon dioxide formed by a thermal oxidation or a plasma enhanced chemical vapor (PECVD) process. Hard mask material in the implant mask 346 may advantageously facilitate subsequent removal of the implant mask 346 after implanting phosphorus at high energies.

[0022] N-type dopants 332 are implanted through the area exposed by the implant mask 346 into the first epitaxial layer 304 to form a first implanted layer 334. The n-type dopants includes at least 50 percent arsenic and/or antimony. The n-type dopants 332 are implanted at a dose greater than 5×10^{14} cm^{-2}, such as 1×10^{15} cm^{-2} to 5×10^{15} cm^{-2}.

[0023] Referring to FIG. 3B, phosphorus 336 is implanted through the area exposed by the

implant mask 346 into the first epitaxial layer 304 to form a second implanted layer 338 below the first implanted layer 334. The phosphorus 336 is implanted at a dose of 1×10^{13} cm^{-2} to 1×10^{14} cm^{-2} and at an energy above 100 keV. Organic material in the implant mask 346, such as photoresist, is removed before a subsequent first thermal drive process.

[0024] Referring to FIG. 3C, a first thermal drive process 340 heats the first epitaxial layer 304 to a temperature of 1150 °C to 1225 °C for at least 30 minutes, such as described in reference to FIG. 2C. The first thermal drive process 340 causes the implanted n-type dopants in the first implanted layer 334 and the implanted phosphorus in the second implanted layer 338 to diffuse deeper into the first epitaxial layer 304. The phosphorus in the second implanted layer 338 diffuses farther into the first epitaxial layer 304 than the arsenic and antimony in the first implanted layer 334. The implant mask 346 (if any) and the layer of pad oxide 330 are subsequently removed.

[0025] Referring to FIG. 3D, an epitaxy process grows a second epitaxial layer 306 on the first epitaxial layer 304 to provide a substrate 302 of the semiconductor device 300. During the epitaxy process, the n-type dopants in the first implanted layer 334 of FIG. 3C diffuse into the second epitaxial layer 306, to form a main layer 314 of the localized n-type buried layer 308. The main layer 314 straddles a boundary between the first epitaxial layer 304 and the second epitaxial layer 306. The phosphorus in the second implanted layer 338 of FIG. 3C forms a lightly-doped layer 320 of the localized n-type buried layer 308 below the main layer 314. The second epitaxial layer 306 is p-type with a resistivity of 5 ohm-cm to 10 ohm-cm. The first epitaxial layer 304 immediately below the n-type buried layer 308 is referred to as a lower layer 310. Analogously, the second epitaxial layer 306 above the n-type buried layer 308 is referred to as an upper layer 312.

[0026] Referring to FIG. 3E, a second thermal drive process 342 heats the substrate 302 to a temperature of 1125 °C to 1200 °C for at least 120 minutes. When the second thermal drive is completed, the main layer 314 of the localized n-type buried layer 308 extends at least a micron into the first epitaxial layer 304 and at least a micron into the second epitaxial layer 306, and the lightly-doped layer 320 extends at least 2 microns below the main layer 314. A top surface 316 of the main layer 314 is at least 5 microns below a top surface 318 of the substrate 302. The top surface 316 of the main layer 314 may be 8 microns to 12 microns below the top surface 318 of the substrate 302. An average doping in the main layer 314 is greater than 5×10^{18} cm^{-3}. At least

50 percent of the n-type dopants in the main layer 314 are arsenic and/or antimony.

[0027] The lightly-doped layer 320 extends at least 2 microns below the main layer 314. An average doping in the lightly-doped layer 320 is 1×10^{16} cm^{-3} to 1×10^{17} cm^{-3}. At least 90 percent of the n-type dopants in the lightly-doped layer 320 are phosphorus.

[0028] Referring to FIG. 3F, n-type sinkers 348 are formed in the second epitaxial layer 306, extending down to the localized n-type buried layer 308. The n-type sinkers 348 may have a closed-loop configuration to isolate a portion 328 of the upper layer 312 from the remaining upper layer 312. The localized n-type buried layer 308 isolates the portion 328 of the upper layer 312 from the lower layer 310. The structure of the localized n-type buried layer 308 with the main layer 314 and the lightly-doped layer 320 may advantageously provide a low sheet resistance in the localized n-type buried layer 308, while reducing leakage current and preventing breakdown of a pn junction between the localized n-type buried layer 308 and the lower layer 310.

[0029] FIG. 4 is a cross section of an alternate example semiconductor device containing a high voltage n-type buried layer. The semiconductor device 400 has a substrate 402, which includes a first epitaxial layer 404 of p-type semiconductor material, such as single crystal silicon. The substrate 402 also includes a second epitaxial layer 406 disposed on the first epitaxial layer 404. The second epitaxial layer 406 includes a p-type semiconductor material, which may have a same composition as the first epitaxial layer 404. An n-type buried layer 408 is disposed in the substrate 402 at a boundary between the first epitaxial layer 404 and the second epitaxial layer 406, extending into the first epitaxial layer 404 and the second epitaxial layer 406. The first epitaxial layer 404 immediately below the n-type buried layer 408 is referred to as a lower layer 410. The lower layer 410 is p-type and has a resistivity of 5 ohm-cm to 10 ohm-cm. The second epitaxial layer 406 above the n-type buried layer 408 is referred to as an upper layer 412. The upper layer 412 is p-type and has a resistivity of 5 ohm-cm to 10 ohm-cm.

[0030] The n-type buried layer 408 includes a main layer 414, which straddles the boundary between the first epitaxial layer 404 and the second epitaxial layer 406, extending at least a micron into the first epitaxial layer 404 and at least a micron into the second epitaxial layer 406. The main layer 414 has an average doping density greater than 5×10^{18} cm^{-3}. A top surface 416 of the main layer 414 is at least 5 microns below a top surface 418 of the substrate 402. The top surface 416 of the main layer 414 may be 8 microns to 12 microns below the top surface 418 of

the substrate 402. The n-type buried layer 408 includes a lightly-doped layer 420 extending at least 2 microns below the main layer 414. The lightly-doped layer 420 is disposed in the first epitaxial layer 404 over the lower layer 410. The lightly-doped layer 420 has an average doping density of 1×10^{16} cm^{-3} to 1×10^{17} cm^{-3}. The n-type buried layer 408 may be formed as described in any of the examples herein.

[0031] One or more deep trench structures 422 are disposed in the substrate 402, extending below the buried layer 408 into the lower layer 410. The deep trench structures 422 include dielectric liners 424 contacting the substrate 402. The deep trench structures 422 include electrically conductive trench fill material 426 on the dielectric liners 424. In this example, the dielectric liner 424 is removed at bottoms 450 of the deep trench structures 422, and the trench fill material 426 extends to the substrate 402, making electrical connection to the substrate 402 through a p-type contact region 452. The contact region 452 and the method of removing the dielectric liner 424 at the bottom 450 of each deep trench structure 422 may be done as described in Application No. US 14/555,359, which is incorporated herein by reference.

[0032] In this example, the trench fill material 426 includes a first layer of polysilicon 454 disposed on the dielectric liner 424, extending to the bottoms 450 of the deep trench structures 422. A second layer of polysilicon 456 is disposed on the first layer of polysilicon 454. Dopants are distributed in the first layer of polysilicon 454 and the second layer of polysilicon 456 with an average doping density of at least 1×10^{18} cm^{-3}. The trench fill material 426 may be formed as described in Application No. US 14/555,300, which is incorporated herein by reference.

[0033] N-type self-aligned sinkers 444 are disposed in the upper layer 412 abutting the deep trench structures 422 and extending to the buried layer 408. The self-aligned sinkers 444 provide electrical connections to the buried layer 408. The self-aligned sinkers 444 may be formed as described in Application No. US 14/555,209, which is incorporated herein by reference.

[0034] The figures are not drawn to scale.

[0035] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a substrate including p-type semiconductor material; and

an n-type buried layer disposed in the substrate;

the n-type buried layer including: a main layer 2 microns to 10 microns thick with an average doping density greater than 5×10^{18} cm^{-3}, wherein at least 50 percent of n-type dopants in the main layer are selected from the group consisting of antimony and arsenic, and wherein a top surface of the main layer is at least 5 microns below a top surface of the substrate; and a lightly-doped layer extending at least 2 microns below the main layer, the lightly-doped layer having an average doping density of 1×10^{16} cm^{-3} to 1×10^{17} cm^{-3}, wherein at least 90 percent of n-type dopants in the lightly-doped layer are phosphorus.

2. The semiconductor device of claim 1, wherein the p-type semiconductor material has a resistivity of 5 ohm-cm to 10 ohm-cm.

3. The semiconductor device of claim 1, wherein at least 50 percent of the n-type dopants in the main layer are antimony.

4. The semiconductor device of claim 1, wherein the n-type buried layer extends substantially across the semiconductor device.

5. The semiconductor device of claim 1, wherein the n-type buried layer is a localized n-type buried layer that extends across only a portion of the semiconductor device.

6. The semiconductor device of claim 1, comprising a deep trench structure disposed in the substrate, extending through the n-type buried layer, the deep trench structure including a dielectric liner with silicon dioxide contacting the substrate.

7. The semiconductor device of claim 6, wherein the deep trench structure has a closed-loop configuration.

8. The semiconductor device of claim 6, comprising n-type self-aligned sinkers disposed in the substrate abutting the deep trench structure and extending down to the n-type buried layer.

9. The semiconductor device of claim 1, comprising an n-type sinker disposed in the substrate, extending to the n-type buried layer, the n-type sinker having a closed-loop configuration.

10. A method of forming a semiconductor device, comprising:

providing a first epitaxial layer of a substrate including p-type semiconductor material;

implanting n-type dopants into the first epitaxial layer at a dose greater than 5×10^{14} cm^{-2}, the n-type dopants being selected from the group consisting of arsenic and phosphorus;

implanting phosphorus into the first epitaxial layer at a dose of 1×10^{13} cm^{-2} to 1×10^{14} cm^{-2} and at an energy above 100 keV;

heating the first epitaxial layer in a first thermal drive process that heats the first epitaxial layer to a temperature of 1150 °C to 1225 °C for at least 30 minutes; and

forming a p-type epitaxial layer of the substrate on the first epitaxial layer;

wherein the implanted n-type dopants form a main layer of an n-type buried layer, the main layer being 2 microns to 10 microns thick, wherein at least 50 percent of n-type dopants in the main layer are selected from the group consisting of antimony and arsenic, and wherein a top surface of the main layer is at least 5 microns below a top surface of the substrate, and the implanted phosphorus forms a lightly-doped layer of the n-type buried layer, the lightly-doped layer extending at least 2 microns below the main layer, wherein the lightly-doped layer has an average doping density of 1×10^{16} cm^{-3} to 1×10^{17} cm^{-3}, and at least 90 percent of n-type dopants in the lightly-doped layer are phosphorus.

11. The method of claim 10, wherein the p-type semiconductor material in the first epitaxial layer has a resistivity of 5 ohm-cm to 10 ohm-cm.

12. The method of claim 10, wherein the n-type dopants implanted into the first epitaxial layer at a dose greater than 5×10^{14} cm^{-2} are antimony.

13. The method of claim 10, wherein the n-type dopants and the phosphorus are implanted into the first epitaxial layer across the semiconductor device.

14. The method of claim 10, wherein the n-type dopants and the phosphorus are implanted into the first epitaxial layer through areas exposed by an implant mask, so that the n-type buried layer is a localized n-type buried layer.

15. The method of claim 10, comprising heating the substrate in a second thermal drive process that heats the substrate to a temperature of 1125 °C to 1200 °C for at least 120 minutes, after the epitaxial layer is formed.

16. The method of claim 10, comprising forming a deep trench in the substrate extending through the n-type buried layer, and forming a dielectric liner in the deep trench with silicon

dioxide contacting the substrate.

17. The method of claim 16, wherein the deep trench has a closed-loop configuration.

18. The method of claim 16, comprising implanting n-type dopants into the substrate adjacent to the deep trench after the deep trench is formed, to form n-type self-aligned sinkers in the substrate extending down to the n-type buried layer.

19. The method of claim 10, comprising forming an n-type sinker in the substrate extending to the n-type buried layer, the n-type sinker having a closed-loop configuration.

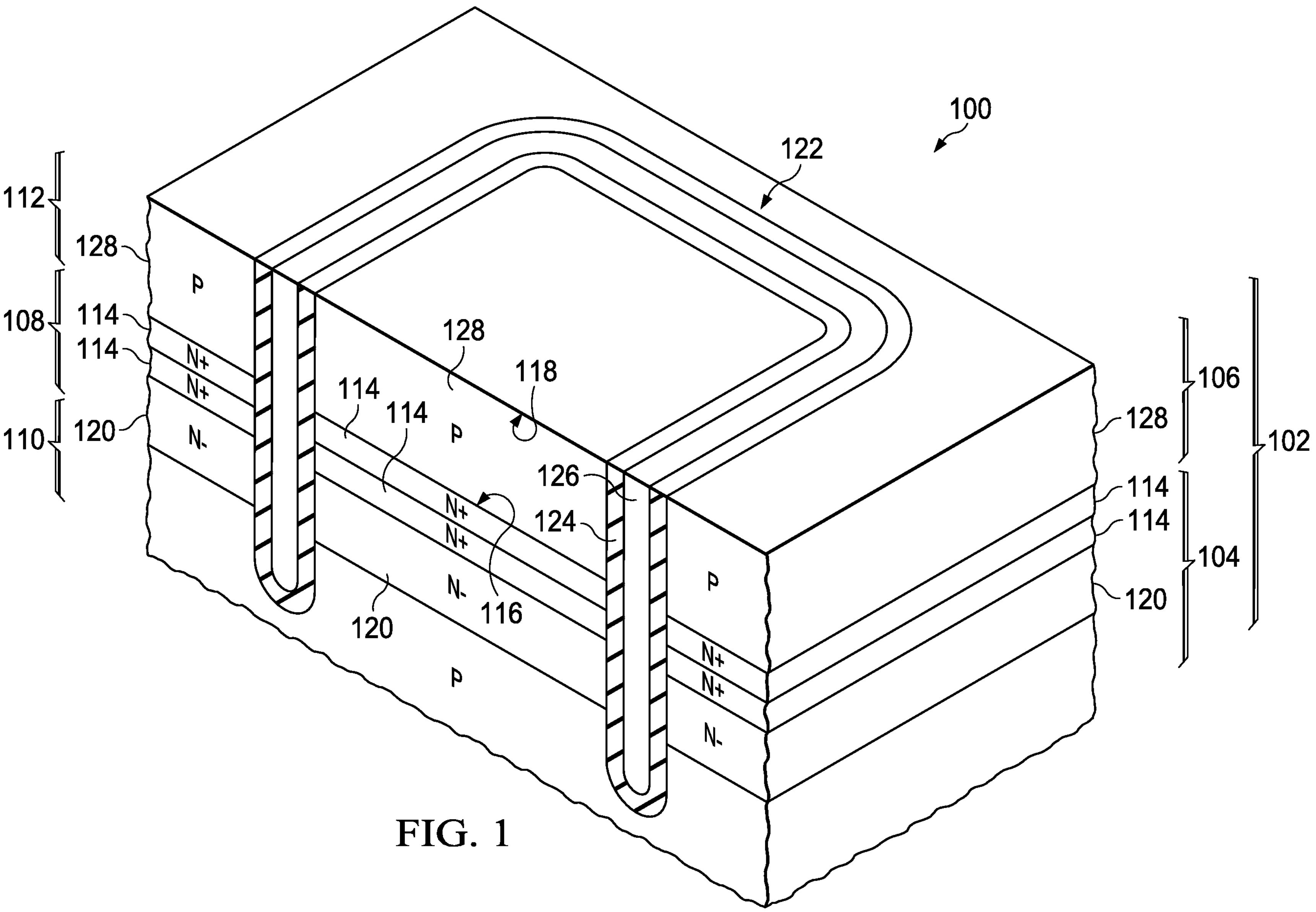

FIG. 1

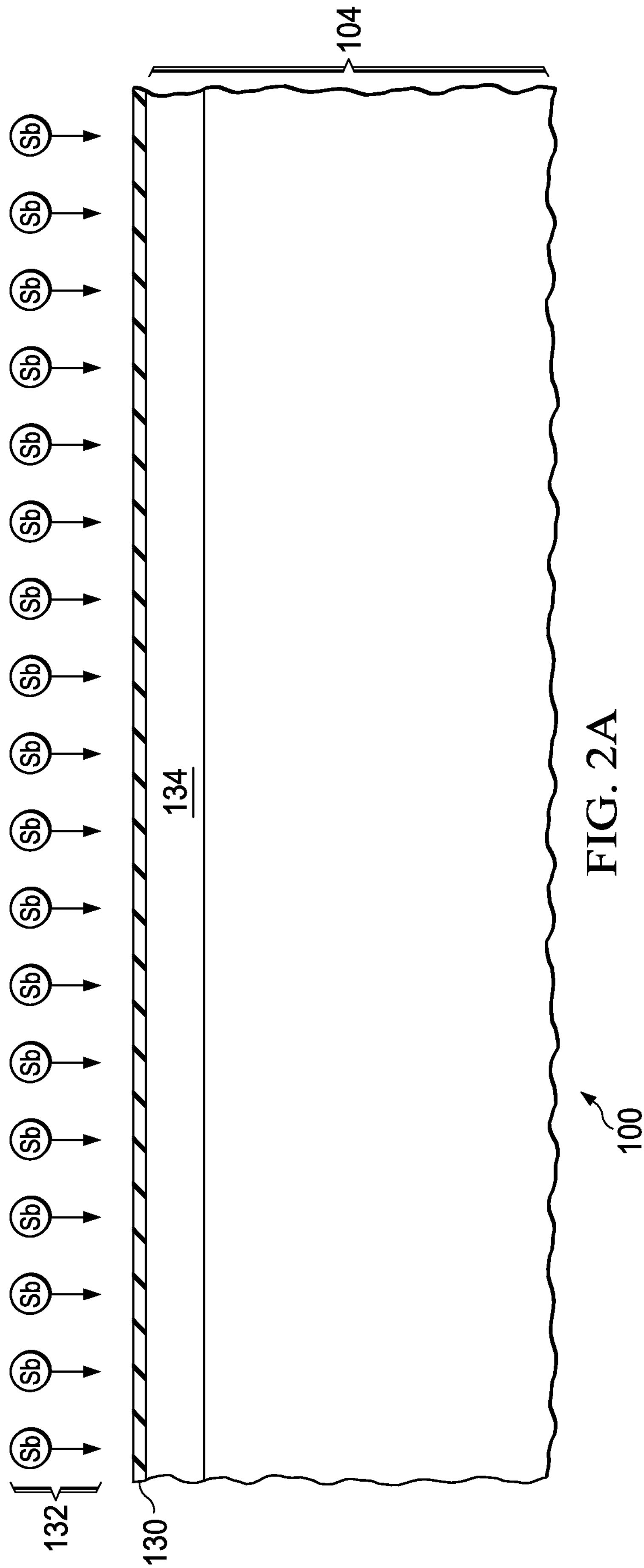

FIG. 2A

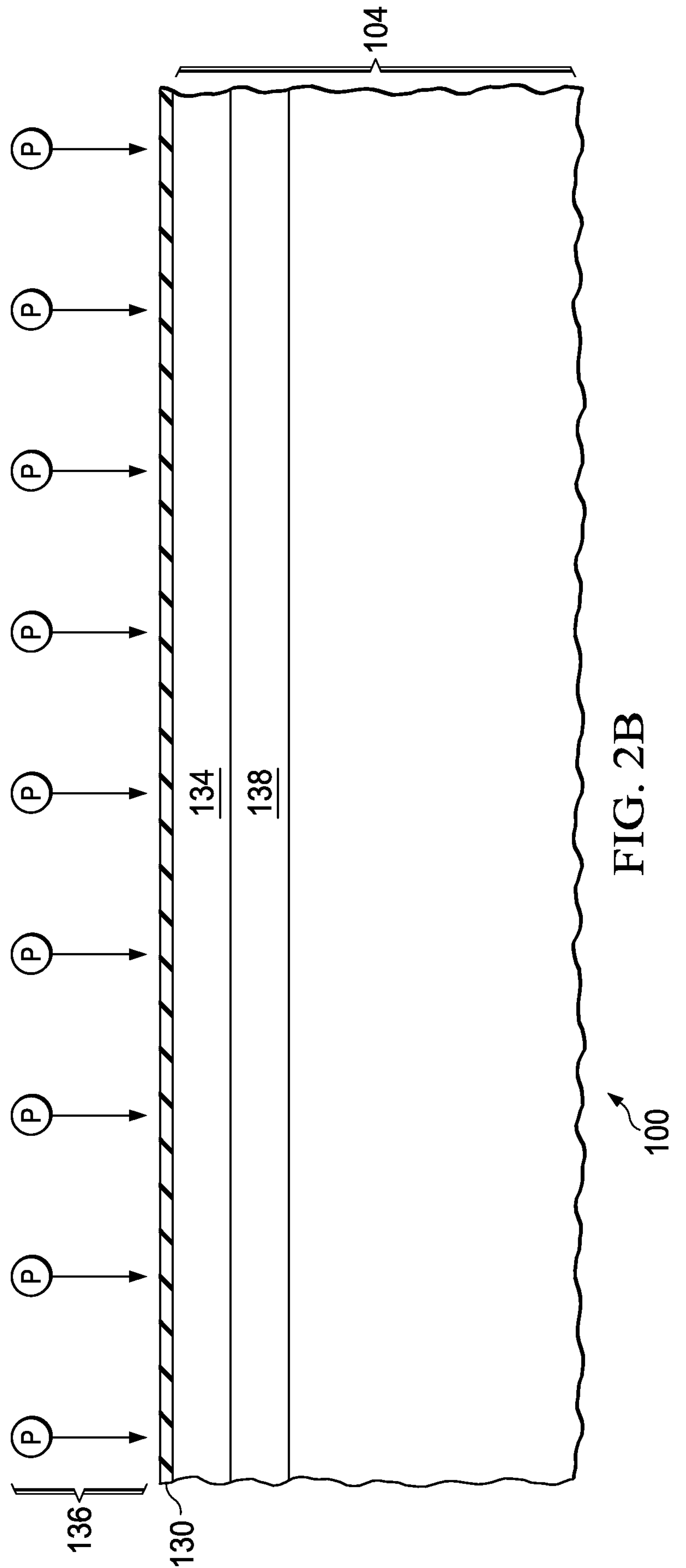

FIG. 2B

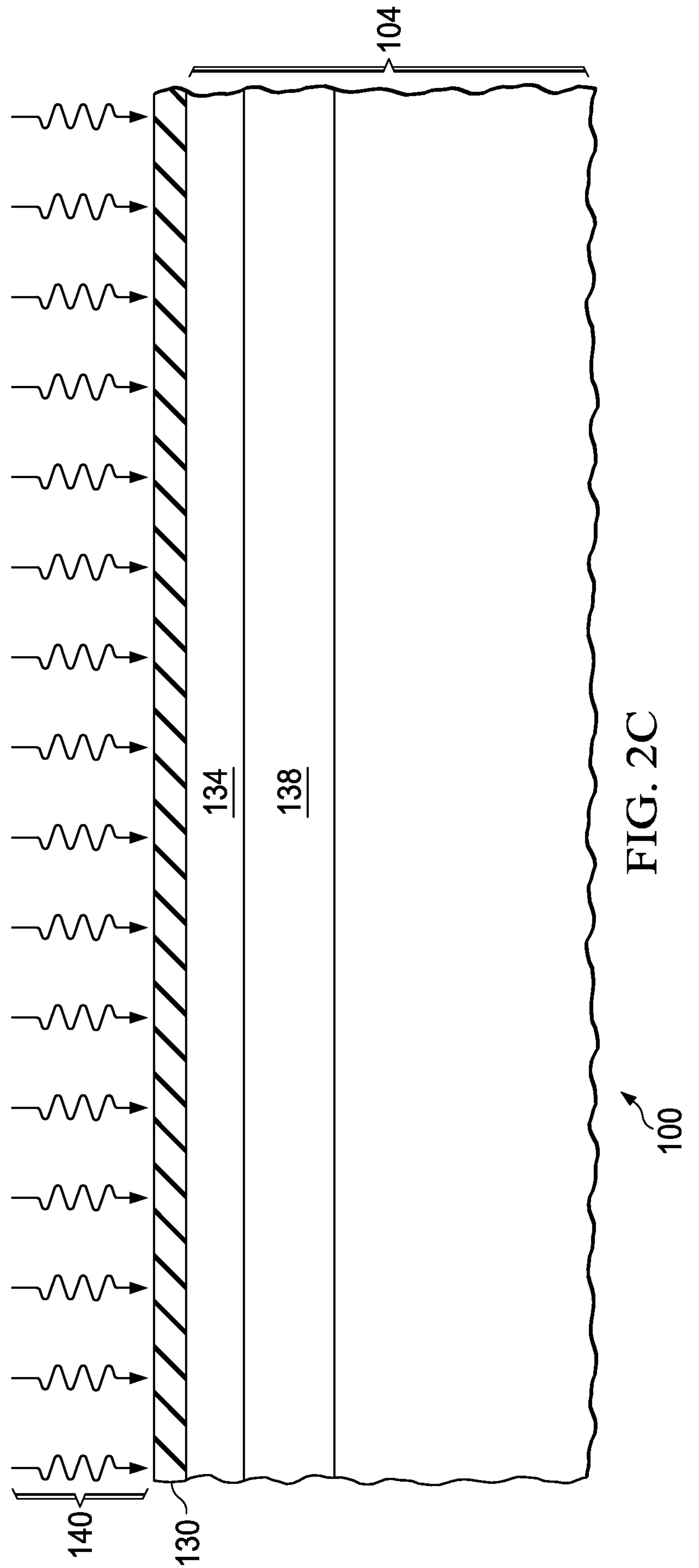

FIG. 2C

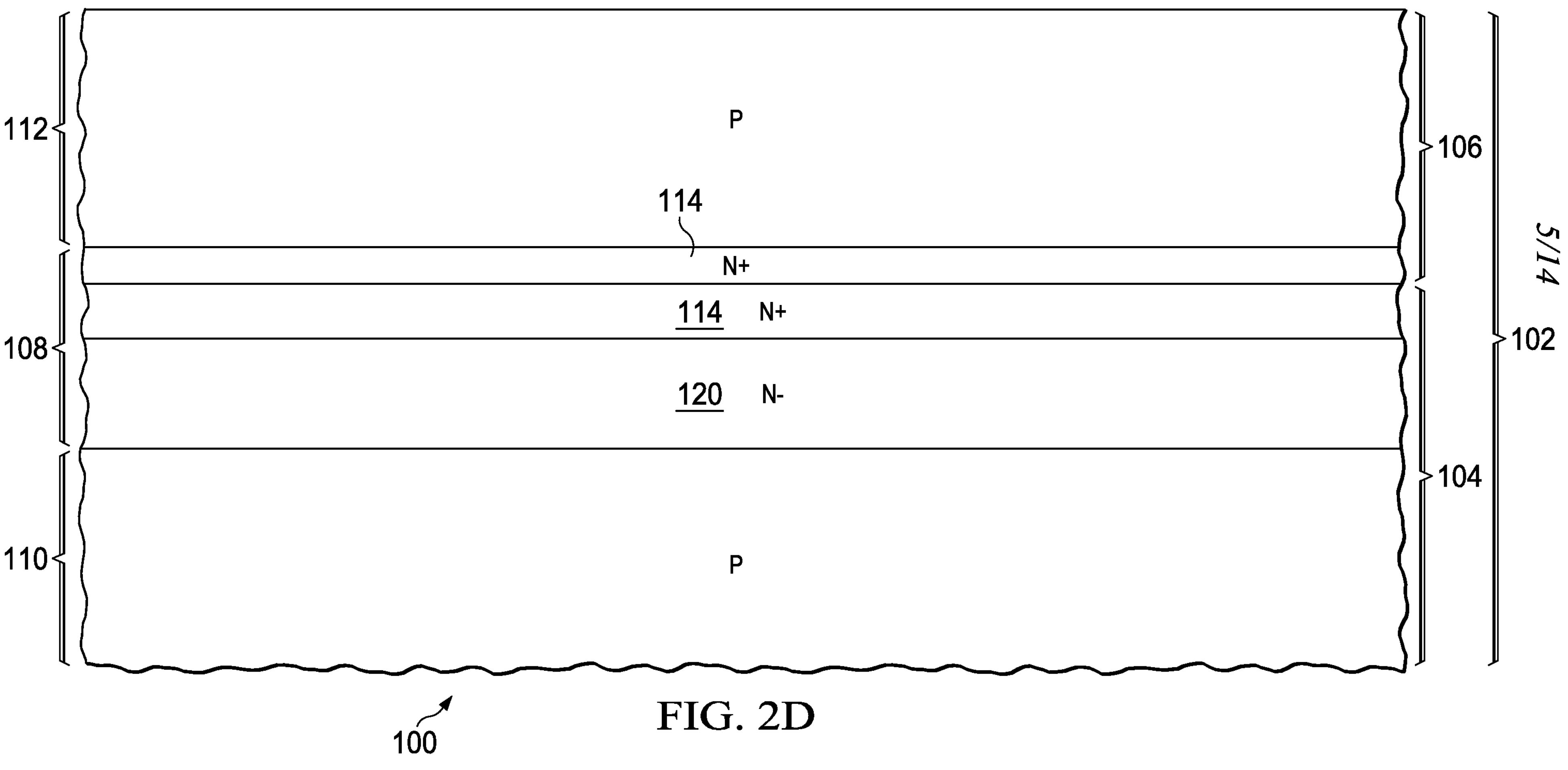

FIG. 2D

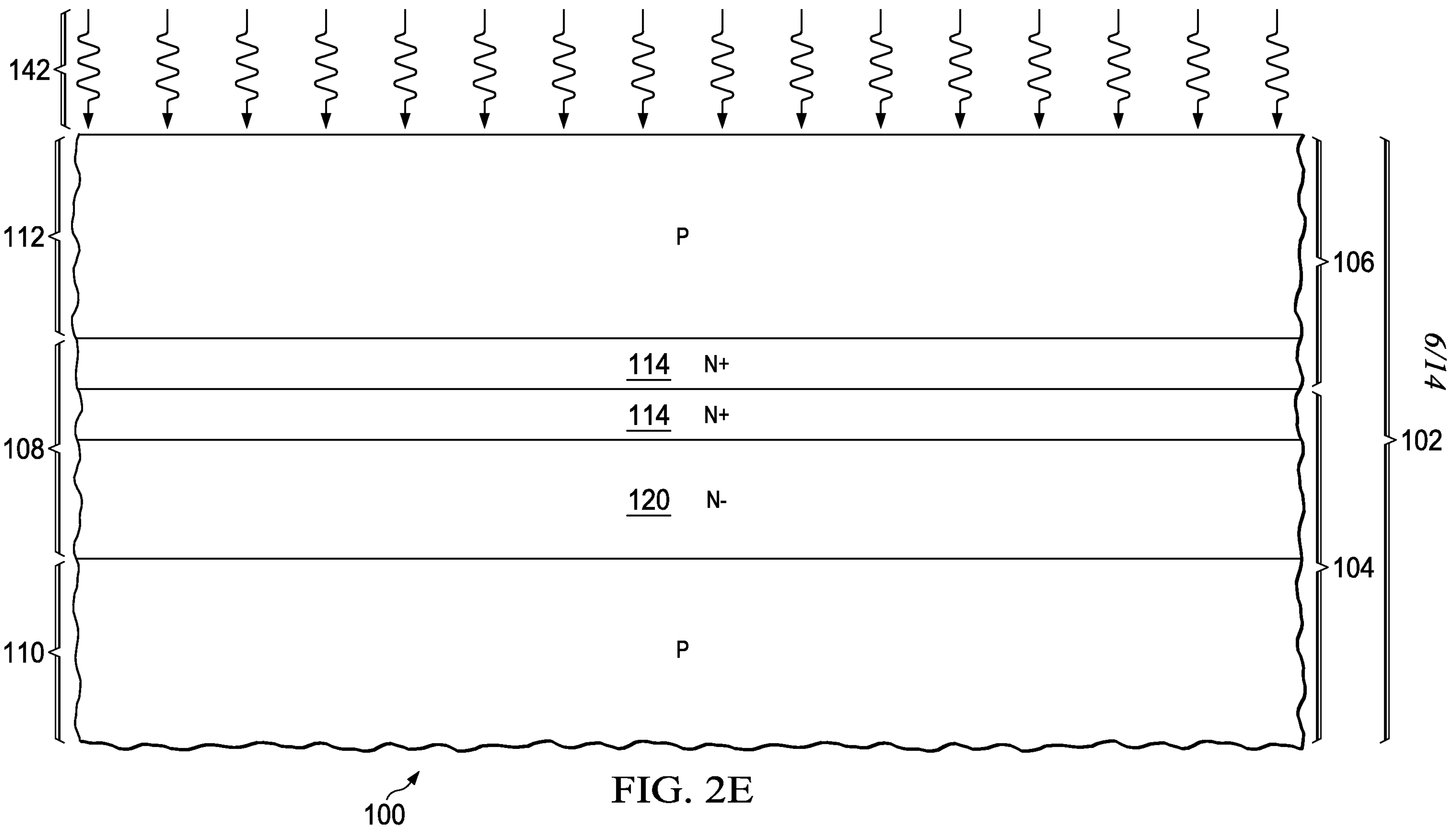

FIG. 2E

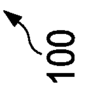

FIG. 2F

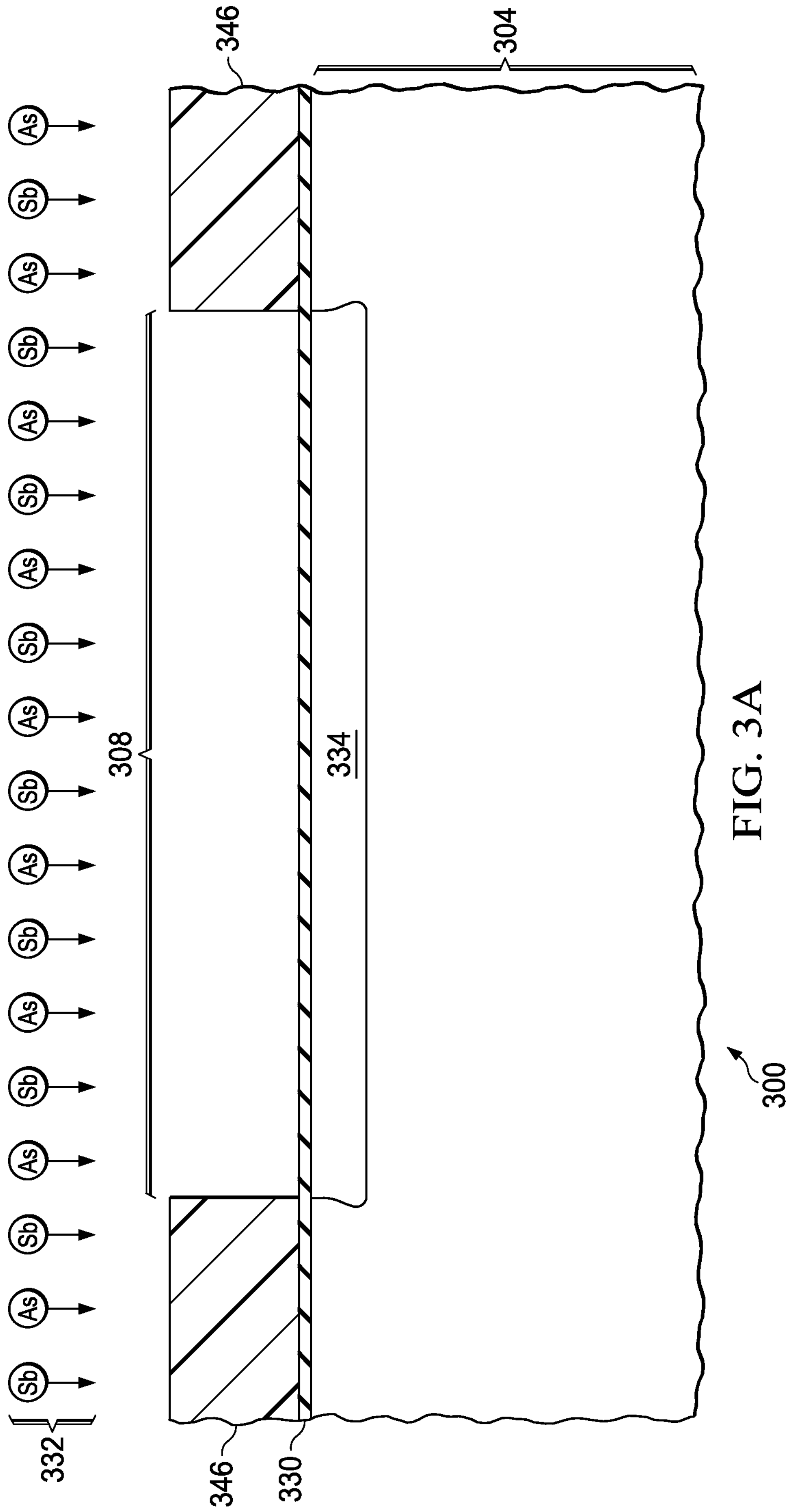

FIG. 3A

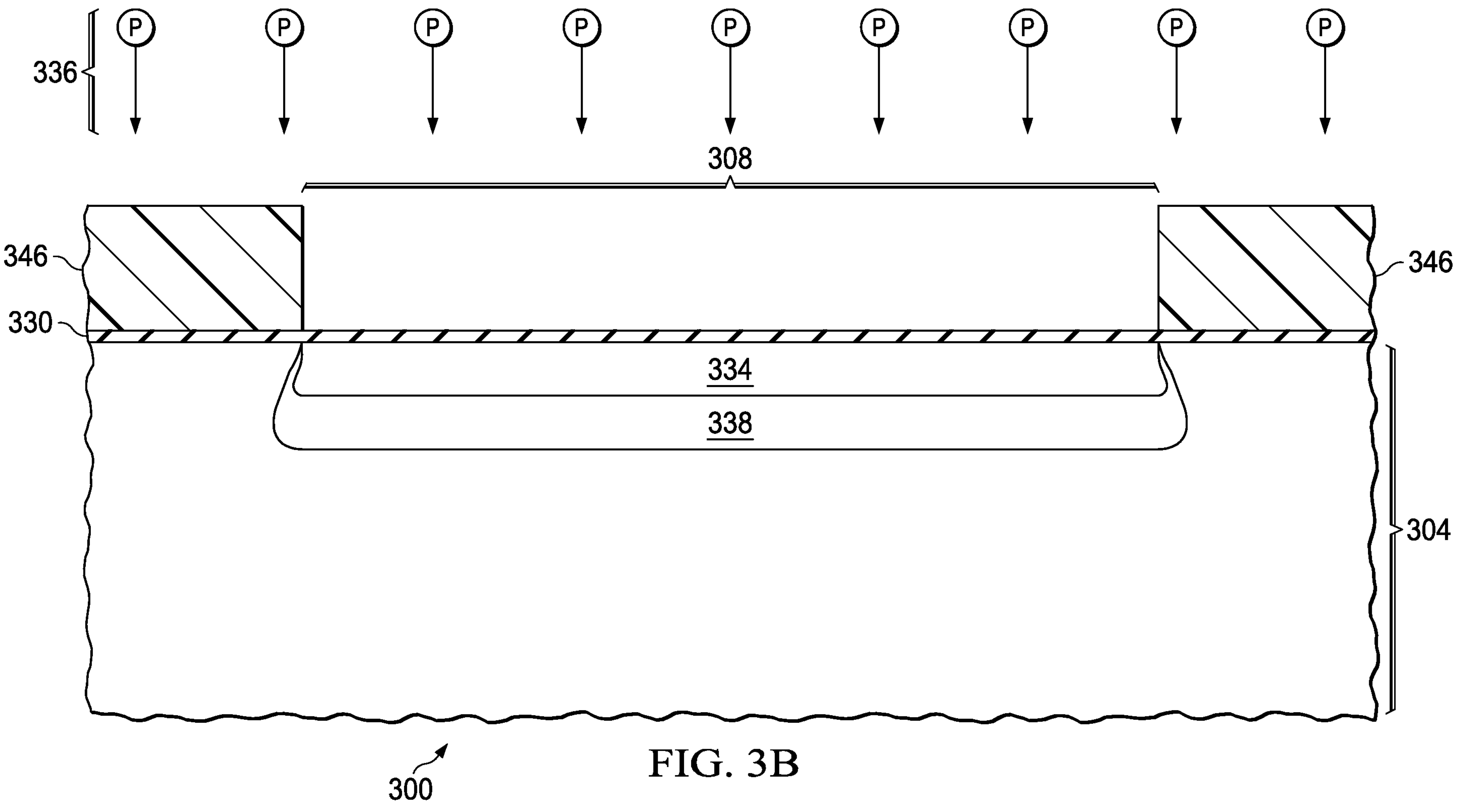

FIG. 3B

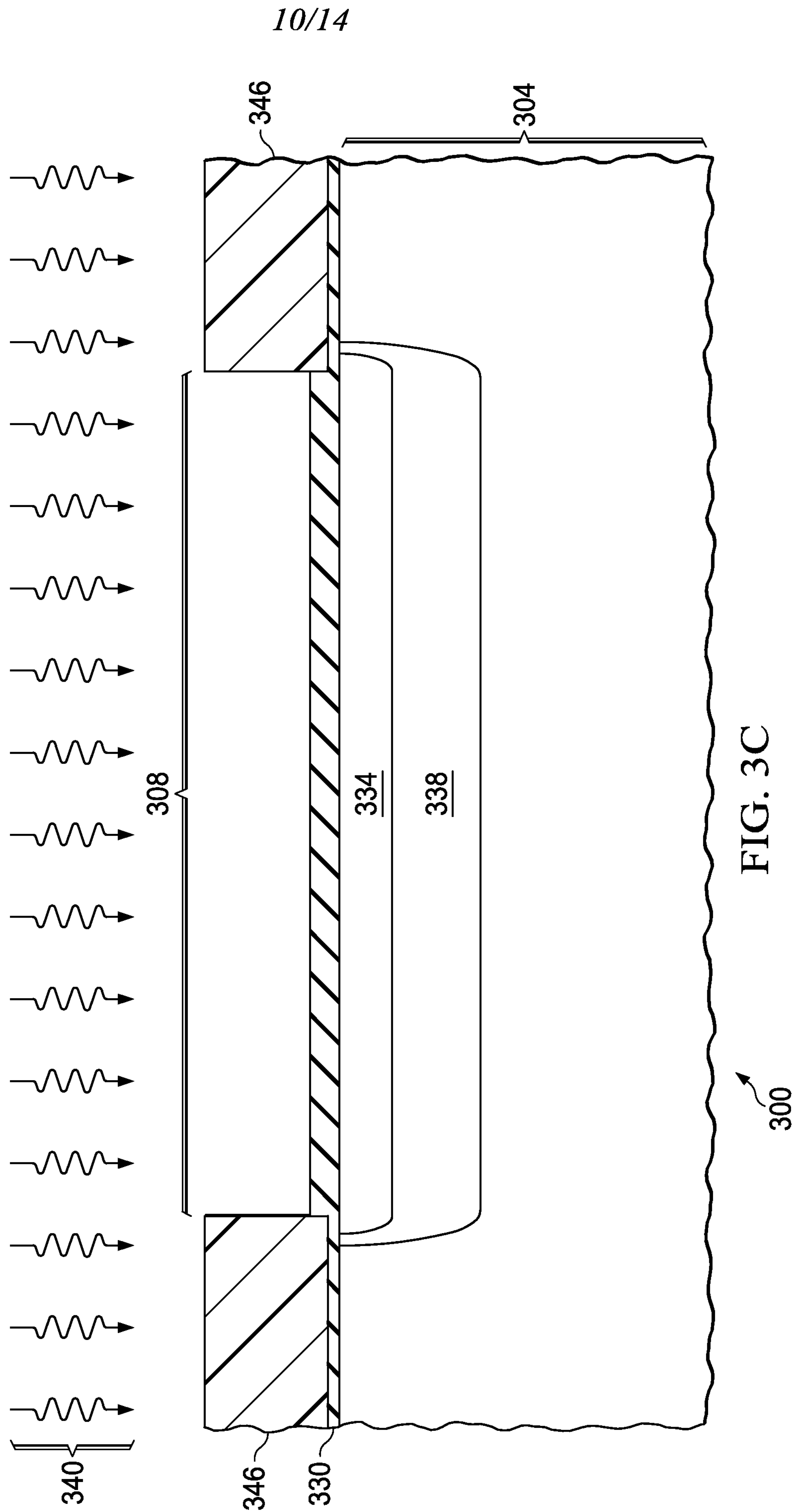

FIG. 3C

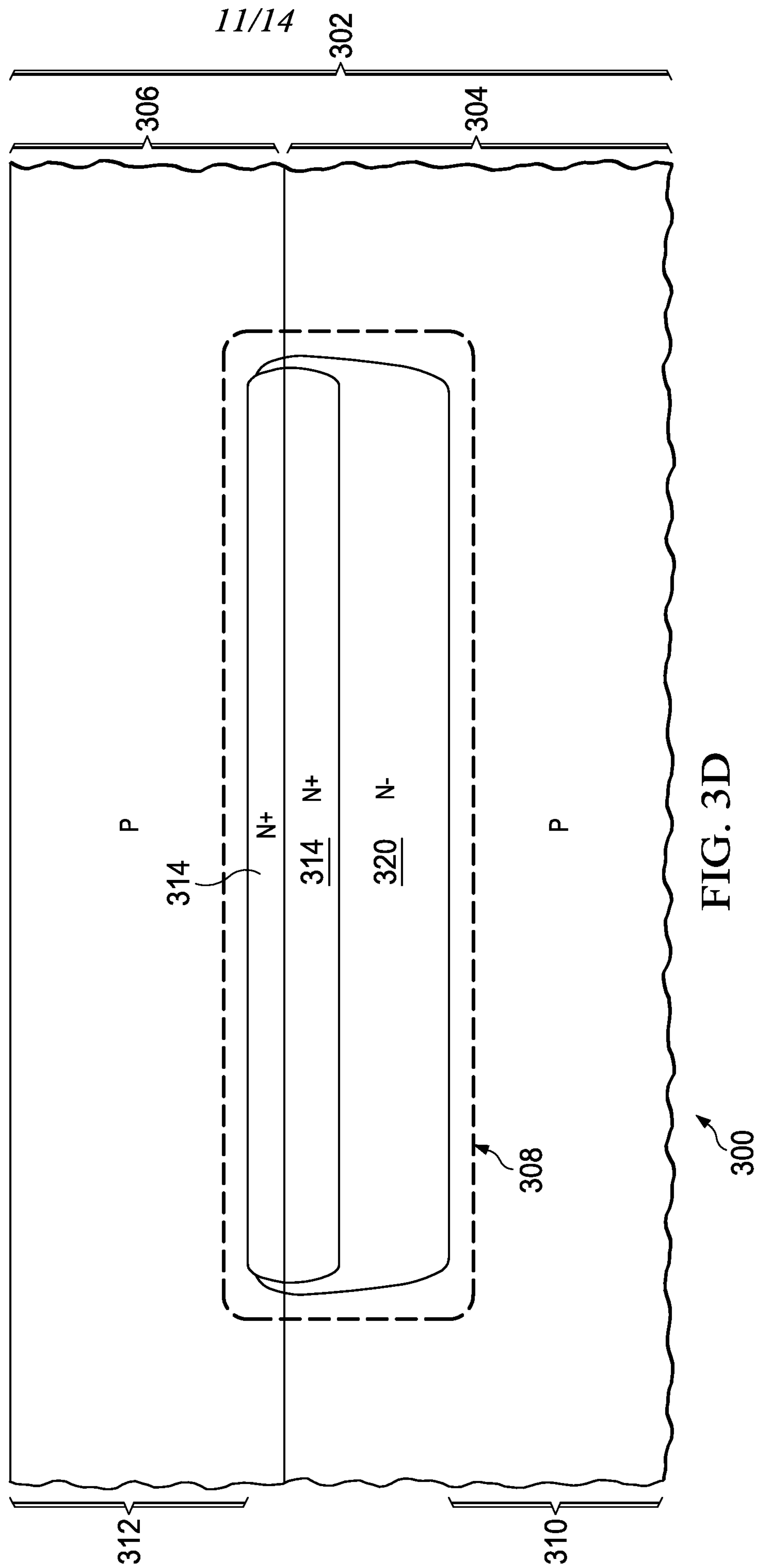

FIG. 3D

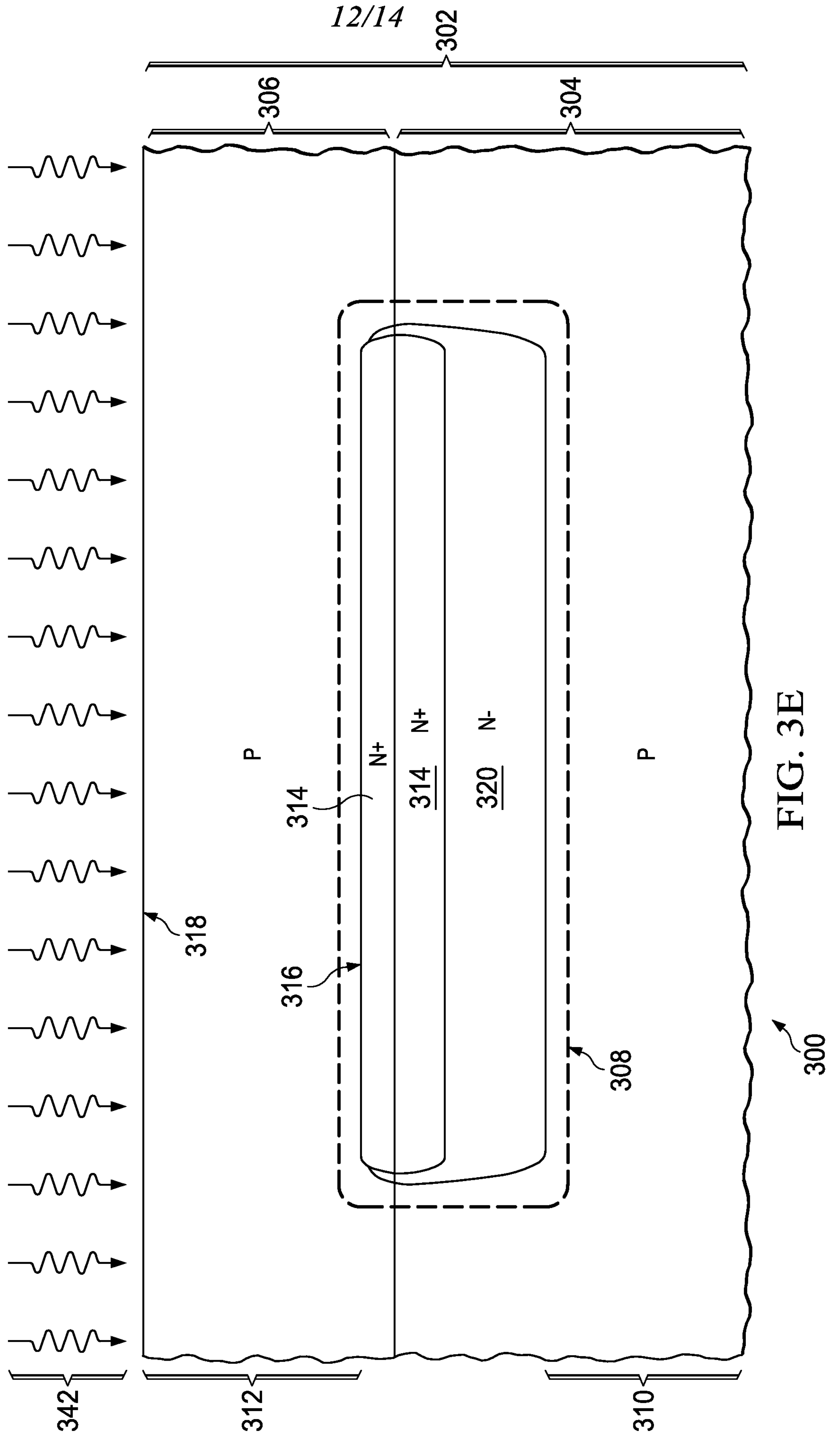

FIG. 3E

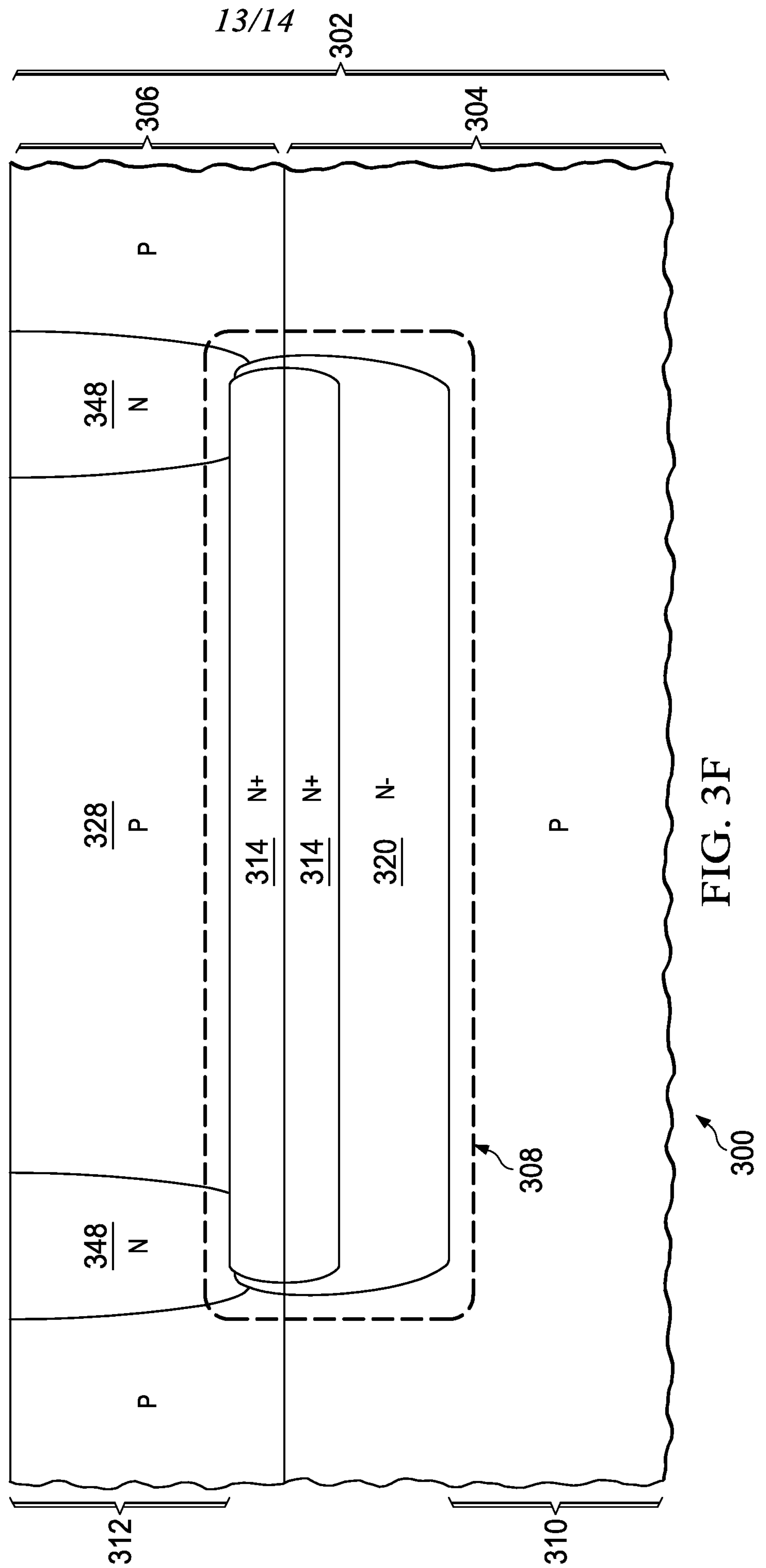

FIG. 3F

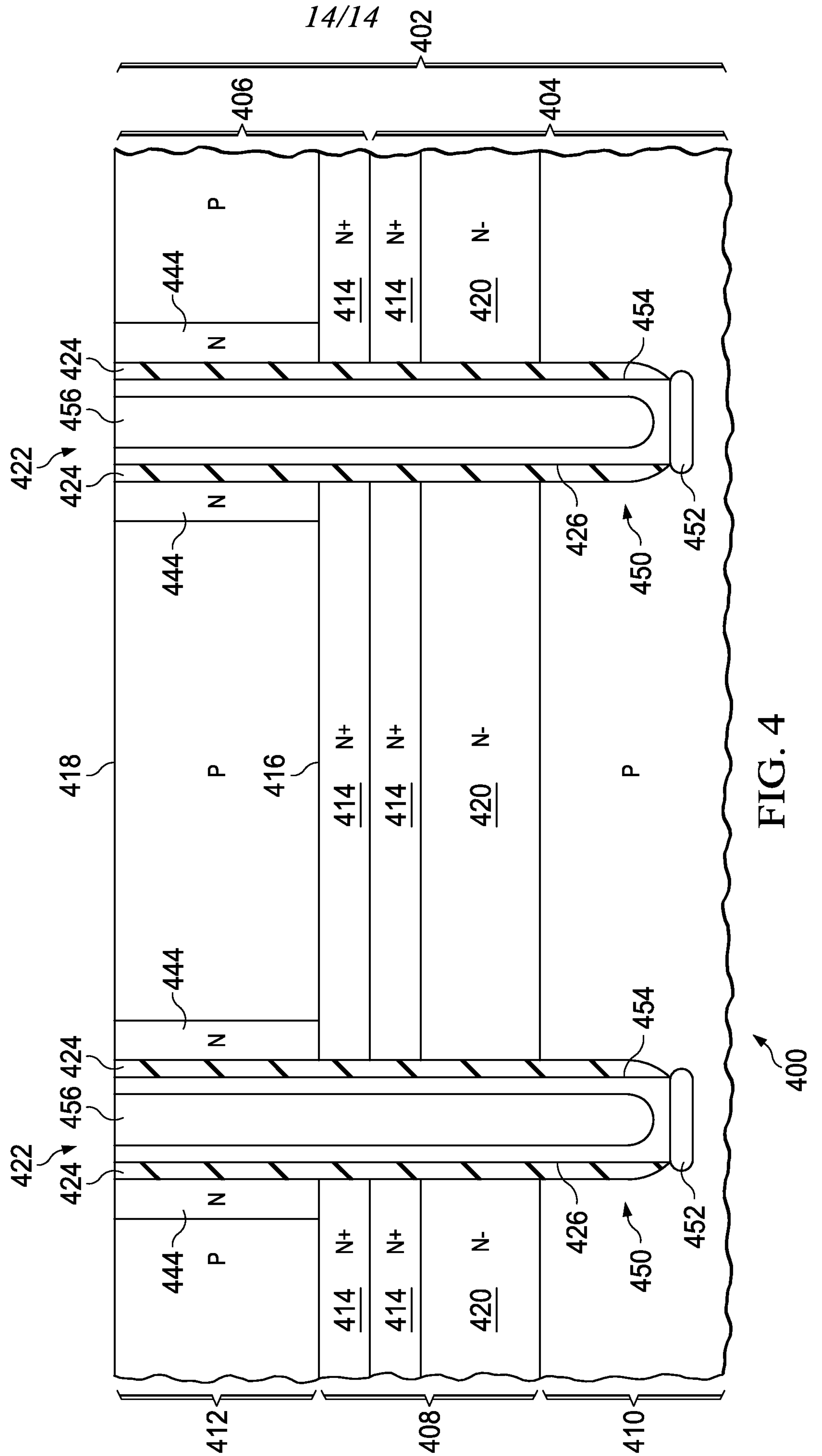

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2015/027699

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/337 *(2006.01)*
H01L 29/26 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/00, 21/02, 21/04, 21/18, 21/28, 21/334, 21/335, 21/336, 21/337, 29/00, 29/02, 29/36, 29/45, 29/66, 29/68, 29/70, 29/76, 29/86, 29/861, 27/00, 27/02, 27/04, 27/08, 27/082, 27/24

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2005/0157756 A1 (ENPIRION, INCORPORATED et al.) 04.08.2005	1-19
A	CN 101937925 A (CHENGDU MONOLITHIC POWER SYSTEM CO., LTD) 05.01.2011	1-19
A	WO 2011/160041 A2 (TEXAS INSTRUMENTS INCORPORATED et al.) 22.12.2011	1-19
A	WO 2008/086348 A2 (MAXPOWER SEMICONDUCTOR, INC. et al.) 17.07.2008	1-19
A	US 2004/0207047 A1 (MOTOROLA, INC.) 21.10.2004	1-19

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

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“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 July 2015 (29.07.2015)	20 August 2015 (20.08.2015)

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