



- (51) International Patent Classification:
C23C 12/00 (2006.01) C23C 20/08 (2006.01)
- (21) International Application Number:
PCT/US2015/034117
- (22) International Filing Date:
4 June 2015 (04.06.2015)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
61/975,098 4 April 2014 (04.04.2014) US
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- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,

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- (54) Title: BASAL PLANE DISLOCATION ELIMINATION IN 4H-SIC BY PULSED RAPID THERMAL ANNEALING

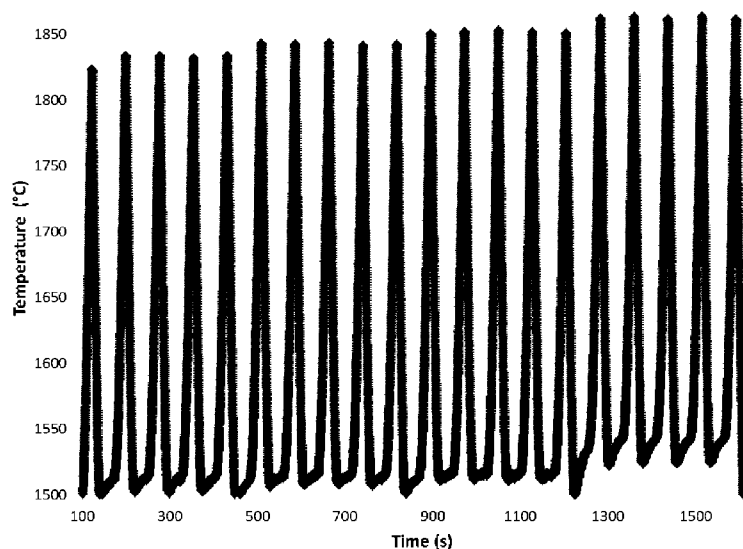


Fig. 1

(57) Abstract: A method for removing existing basal plane dislocations (BPDs) from silicon carbide epilayers by using a pulsed rapid thermal annealing process where the BPDs in the epilayers were eliminated while preserving the epitaxial surface. This high temperature, high pressure method uses silicon carbide epitaxial layers with a carbon cap to protect the surface. These capped epilayers are subjected to a plurality of rapid heating and cooling cycles.



SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,
GW, KM, ML, MR, NE, SN, TD, TG).

— *before the expiration of the time limit for amending the
claims and to be republished in the event of receipt of
amendments (Rule 48.2(h))*

Published:

— *with international search report (Art. 21(3))*

— *with information concerning request for restoration of
the right of priority in respect of one or more priority
claims (Rules 26bis.3 and 48.2(b)(vii))*

BASAL PLANE DISLOCATION ELIMINATION IN 4H-SIC BY PULSED RAPID THERMAL ANNEALING

TECHNICAL FIELD

The present invention relates to the removal of basal plane dislocations in silicon carbide (SiC) epitaxially grown layers.

BACKGROUND ART

High power devices fabricated in 4H-silicon carbide (SiC) epilayers are known to suffer from forward voltage degradation caused by basal plane dislocation (BPD) induced stacking faults (SF). (J. P. Bergman et al., Mater. Sci. Forum 353, 299 (2001) and R. E. Stahlbush et al., Mater. Sci. Forum 389, 427 (2002)). Over the past decade, several efforts have been successful in removal of more than 90% of the BPDs in the substrate by converting them to benign threading edge dislocations (TED) during epigrowth. (S. Ha et al., Phys. Rev. Lett. 92, 175504 (2004) and R. L. Myers-Ward et al., Mat. Sci. Forum 615-617, 105 (2009)). However, BPDs in the many areas of the epilayers are still $> 100 \text{ cm}^{-2}$, which adversely affects the device yield and reliability.

A previous report for BPD removal was published by Mahadik et al., detailing a conventional annealing process which was less effective in preserving the SiC surface than the technique presented herein. (N. A. Mahadik et al., Materials Science Forum Vols. 778-780, pp 324-327 (2014)).

Using multiple heating and cooling cycles has been previously reported for electrical activation of implanted Mg ions in gallium nitride (GaN) and removal of defects introduced during this implantation step. (T. J. Anderson et al., Elect. Lett. 50, 197 (2014); B. N. Feigelson et al., J. Crystal Growth, vol. 350, no. 1, pp. 21-26 (2012); and B. N. Feigelson et al., US Patent #8,518,808 (2013)).

DISCLOSURE OF INVENTION

The present invention provides a means to remove basal plane dislocations already present in silicon carbide (SiC) epitaxially grown layers, while preserving the surface morphology. This method uses a high temperature annealing process under high ambient pressure in ultrapure inert atmosphere and utilizes a surface protective coating on epitaxially grown SiC layers to remove the basal plane dislocations present in it. Unlike previous methods, the high temperature anneal is performed in pulses of very high temperature, leading to an elimination of defects while preserving the surface of the material over a large area.

The subject of the invention is single crystal Silicon Carbide (SiC) substrate material and epilayers grown by any typical methods. This invention provides means to remove defects, while preserving the sample surface in SiC semiconductors.

The invented method uses a high temperature annealing process under gas pressure above atmospheric and utilizes a surface protective coating to eliminate basal plane dislocations (BPD) in SiC samples. More specifically, the high temperature annealing process is one where the temperature profile is pulsed in individual cycles of high temperature and short duration. Even more specifically, the high temperature annealing process is one where the material is subjected to a plurality of short (rapid) heating and cooling cycles without removing the sample from the enclosure.

The present invention can be used to remove BPDs from SiC epitaxial layers after their growth, while preserving the surface morphology. This is important to realize high power density and high voltage SiC devices.

The present invention can be used to transform point defects in SiC and change optical and electrical properties of SiC.

The present invention can be used to anneal n-type and p-type implants in SiC to form higher conductivity n-type and p-type semiconductor regions, while preserving the surface.

The present invention can be used to perform high temperature treatments to SiC to improve carrier lifetime in both p-type and n-type SiC layers.

In an embodiment where the surface does not have a protective coating, this invention can be used to grow Si- or C- containing compounds, such as SiN_x or graphene.

The present invention has many advantages. It results in elimination of BPDs in SiC material, while maintaining good surface morphology. Compared to previously reported methods, the present invention uses higher temperature annealing (up to 1875 °C, but higher is possible) of SiC material with no silicon sublimation from the surface, which prevents surface degradation. This higher temperature annealing could be used to improve the activation/incorporation of implanted species in the SiC lattice.

These and other features and advantages of the invention, as well as the invention itself, will become better understood by reference to the following detailed description, appended claims, and accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

Fig. 1 shows a temperature profile of the pulsed rapid thermal annealing technique.

Fig. 2 compares the surface morphology using conventional annealing with using the pulsed rapid thermal annealing of the present invention. Fig. 2a shows that conventional annealing at above 1750 °C results in an RMS roughness of 5.7 nm. Fig. 2b shows that pulsed rapid thermal annealing results in an RMS roughness of 3.1 nm.

Fig. 3 shows ultraviolet photoluminescence (UVPL) images of the samples before and after the pulsed rapid thermal annealing process. Fig. 2a shows a typical UVPL image of an as grown sample showing a BPD density of $\sim 1000 \text{ cm}^{-2}$. The short horizontal white lines are BPDs. Fig. 2b shows an UVPL sample after pulsed rapid thermal annealing at 1875 °C for 5 min., with no BPDs. The long scratch line is scribe mark on backside for sample identification.

BEST MODE FOR CARRYING OUT THE INVENTION

The present invention provides a technique to remove the existing BPDs from the epilayers by using a pulsed rapid thermal annealing process where the BPDs in the epilayers were eliminated, while preserving the epitaxial surface. This high temperature, high pressure method uses silicon carbide epitaxial layers with a carbon cap to protect the surface. These capped epilayers are subjected to a plurality of rapid heating and cooling cycles.

The method of the present invention may be briefly described as follows. First silicon carbide epilayers are capped with carbon to protect the surface. Other than a carbon cap, materials, including boron nitride, can be used as well. Unlike the MRTA process described by Feigelson et al., where the AlN capping layer is able to absorb and protect the GaN surface from trace amounts of oxygen in the inert annealing atmosphere, the presently described method depends on nearly complete removal of any and all trace amounts of oxygen during the process. The capped silicon carbide epilayers are then placed inside an enclosure, and overpressure of ultra-purified nitrogen is applied. The capped epilayers are then annealed with a plurality of heating and cooling cycles without removing them from the enclosure between cycles. There should be no oxygen present during the annealing process. Each heating and cooling cycle includes heating the epilayers for several seconds to a temperature above 1750 °C, more preferably above 1800 °C and even more preferably up to 1875 °C or above, and rapidly cooling the epilayers for several seconds to a temperature below 1550 °C. In a preferred embodiment, at the end of the plurality of heating and cooling cycles, the capped silicon carbide epilayers have been heated to a temperature between 1750 and 1875 °C for at least five minutes.

In this invention, we used 4° offcut, 15 μm , n-type $6 \times 10^{15} \text{ cm}^{-3}$ 4H-SiC epilayers, commercially obtained. The samples were then carbon capped using the following process. The

samples were cleaned with a pirana solution consisting of $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ in the ratio 1:1:5, followed by a solvent clean (SC-1) process. Then AZ 4620 photoresist was applied using a revolution speed of 5000 rpm for 1 minute. The samples were then introduced in an annealing chamber and kept under ultrapure nitrogen to eliminate traces of oxygen and produce a high quality carbon capping layer. The samples were then heated to a temperature of 1100 °C in ultrapure nitrogen ambient for 30 minutes to form the high quality carbon cap. This was followed by the high temperature high pressure annealing process.

The as-grown samples were imaged using ultraviolet photoluminescence (UVPL) imaging, which shows the BPDs in the epitaxial layers. Carriers were excited with the 334 nm line from an Ar-ion laser, and images were collected in the emission range of 600-1000 nm. The samples were carbon capped and annealed in 20 cycles as shown in Fig. 1. The sample was at an annealing temperature of 1750-1875 °C for a total time of ~5 minutes (Fig. 1). The annealing was performed in a custom designed chamber with inductive sample heating and ultrapure N_2 overpressure at 0.41-0.76 MPa. The base temperature was maintained near 1500 °C, from where the temperature was ramped up and down to the desired temperature in rapid cycles to accumulate sufficient time at the desired high temperature range. The combination of high N_2 overpressure and rapid cycles enabled higher temperature annealing than what conventional methods allow, while preserving the carbon cap, and thus maintaining a pristine epitaxial surface.

Elimination of oxygen during the annealing process was critical to the success of this process. All gas process lines were purged for a long time with ultrapure nitrogen. Maximum inertness of the annealing atmosphere in the chamber was ensured by multiple fills with ultrapure nitrogen. The SiC samples were enclosed in a carbon cap which additionally protected the sample surface from oxygen-induced decomposition.

Post-annealed samples were also imaged to observe the BPDs in the epilayers. The UVPL images of the as grown samples showed an average BPD density $\sim 1000 \text{ cm}^{-2}$. Two goals of annealing were to eliminate BPDs in the epitaxial layers and to preserve the epitaxial surface morphology. There have been several previous attempts to anneal similar samples using high temperature microwave annealing as well as annealing under high N_2 pressure. With microwave annealing, BPDs were eliminated by annealing at above 1750 °C. However, the surface morphology was poor. Fig. 2 compares the surface morphology using conventional annealing at above 1750 °C (Fig. 2a) with using the pulsed rapid thermal annealing of the present invention

(Fig. 2b). Pulsed rapid thermal annealing improved surface morphology by about a factor of 2 compared to conventional annealing (RMS roughness of 3.1 nm compared to 5.7 nm).

The carbon capping technique was optimized but the microwave annealing performed at ambient pressure conditions was not able to achieve a good sample surface. Annealing under high pressure preserved the surface, however, could not go to temperatures higher than 1750 °C without damaging the cap. For complete BPD elimination, a much higher temperature anneal was required. Thus, the pulsed rapid thermal annealing process was adopted, resulting in a higher temperature annealing and preserving of the carbon cap.

Fig. 3 shows UVPL images of the samples before (Fig. 3a) and after (Fig. 3b) the pulsed rapid thermal annealing process and indicates that a surface without any significant pits or generation of any new BPDs during the annealing process was produced. Such defects typically happen using conventional annealing at similar high temperatures. Almost all the BPDs that were previously present disappeared in the epilayer. It is proposed that during annealing BPDs that had not yet converted to threading edge dislocations (TED) during epigrowth forms a TED near the surface. Then the TEDs at the end of all the BPDs glide in a prismatic plane causing the BPD to shorten. Since this glide doesn't occur in the lower energy basal plane, the required energy for this glide is provided by the very high annealing temperature. This way a BPD segment converts to a TED with the TED glide and thus shortens the BPD. The UVPL images of the annealed samples also show a dot where the original BPD had propagated from the substrate, which represents a TED.

The above descriptions are those of the preferred embodiments of the invention. Various modifications and variations are possible in light of the above teachings without departing from the spirit and broader aspects of the invention. It is therefore to be understood that the claimed invention may be practiced otherwise than as specifically described. Any references to claim elements in the singular, for example, using the articles "a," "an," "the," or "said," is not to be construed as limiting the element to the singular.

CLAIMS

1. A method to remove basal plane dislocations in post growth silicon carbide epitaxial layers, comprising:
 - capping silicon carbide epilayers with a carbon cap, wherein the amount of oxygen present during capping is below any measurable limit;
 - placing the capped silicon carbide epilayers into an enclosure;
 - applying a pressure in the 0.41-0.76 MPa range;
 - annealing the capped silicon carbide epilayers with a plurality of heating and cooling cycles without removing the capped silicon carbide epilayers from the enclosure, wherein each heating and cooling cycle includes rapidly heating the silicon carbide epilayers for several seconds to a temperature above 1800 °C and rapidly cooling the sample for several seconds to a temperature below 1550 °C; and
 - ensuring that any oxygen present in the enclosure during the annealing is below any measurable limit.
2. The method of claim 1, wherein at the end of the plurality of heating and cooling cycles, the capped silicon carbide epilayers have been heated to a temperature between 1750 °C and 1875 °C for at least five minutes.
3. The method of claim 1, wherein after annealing the capped silicon carbide epilayers have an RMS roughness of 3.1 nm or lower.
4. A silicon carbide substrate material, made by the method comprising:
 - capping silicon carbide epilayers with a carbon cap, wherein the amount of oxygen present during capping is below any measurable limit;
 - placing the capped silicon carbide epilayers into an enclosure;
 - applying a pressure in the 0.41-0.76 MPa range;
 - annealing the capped silicon carbide epilayers with a plurality of heating and cooling cycles without removing the capped silicon carbide epilayers from the enclosure, wherein each heating and cooling cycle includes rapidly heating the silicon carbide epilayers for several seconds to a temperature above 1800 °C and rapidly cooling the sample for several seconds to a temperature below 1550 °C; and
 - ensuring that any oxygen present in the enclosure during the annealing is below any measurable limit.

5. The silicon carbide substrate material of claim 4, wherein at the end of the plurality of heating and cooling cycles, the capped silicon carbide epilayers have been heated to a temperature between 1750 °C and 1875 °C for at least five minutes.

6. The silicon carbide substrate material of claim 4, wherein after annealing the capped silicon carbide epilayers have an RMS roughness of 3.1 nm or lower.

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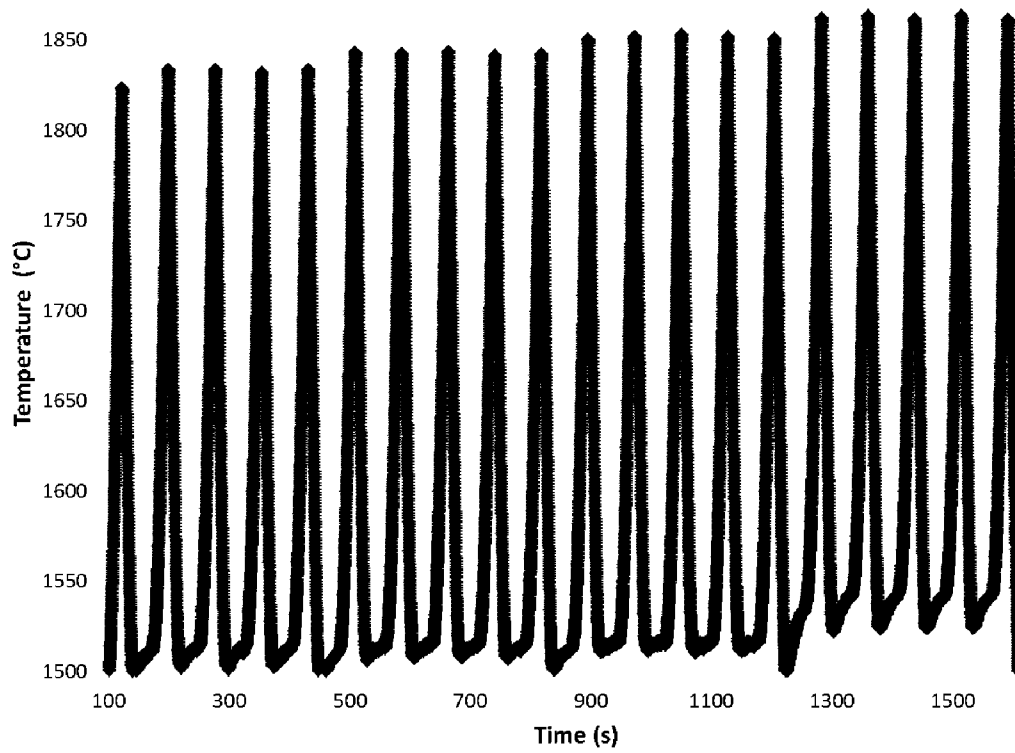


Fig. 1

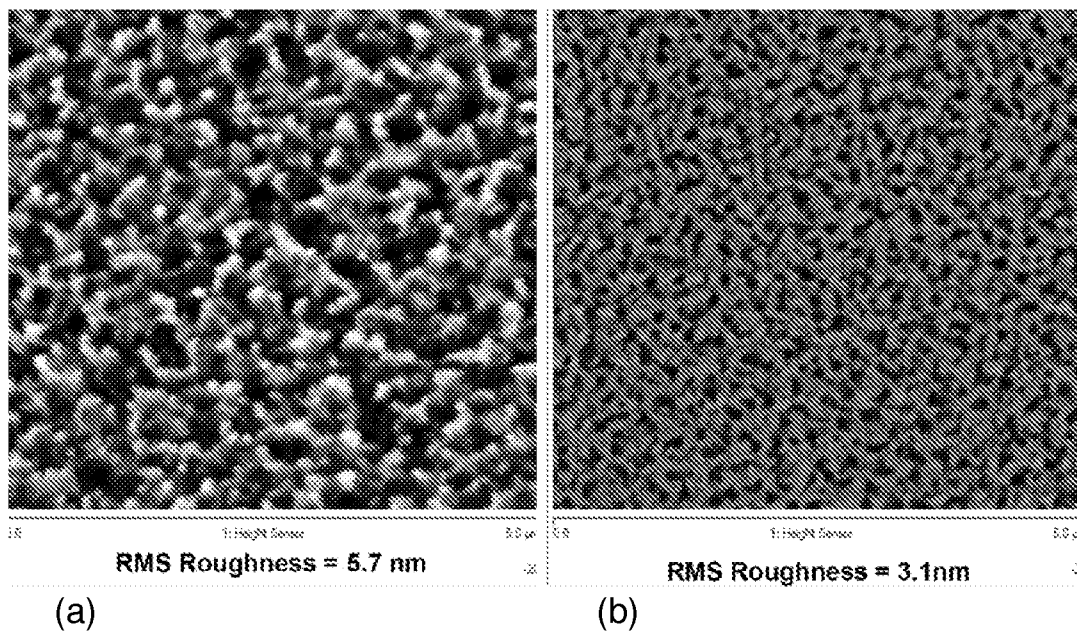


Fig. 2

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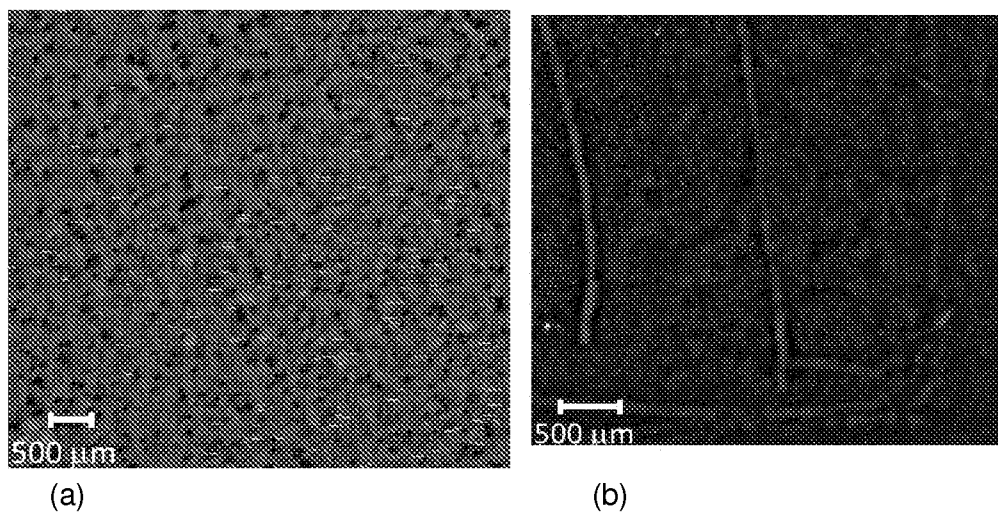


Fig. 3

A. CLASSIFICATION OF SUBJECT MATTER**C23C 12/00(2006.01)i, C23C 20/08(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

C23C 12/00; H01L 21/30; H01L 29/20; H01L 21/00; H01L 21/265; C23C 20/08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: basal plane dislocation, silicon carbide, capping, annealing, epilayer, and epitaxial layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	MAHADIK, N. A. et al., 'Basal Plane Dislocation Mitigation Using High Temperature Annealing in 4H-SiC Epitaxy,' In: ECS Transactions, 224th ECS Meeting, Edited by Shenai, K. et al., San Francisco, CA: ECS, 27 October 2013 - 1 November 2013, vol. 58, no. 4, pages 325-329 See pages 325-328.	1-6
Y	US 2012-0068188 A1 (FEIGELSON, BORIS N. et al.) 22 March 2012 See abstract; paragraphs [0007], [0046]-[0051]; and claims 1-17.	1-6
A	ZHAO, FENG et al., 'Effect of crystallographic dislocations on the reverse performance of 4H-SiC p-n diodes,' Materials Letters, 31 October 2009 (Online), vol. 64, no. 3, pages 281-283 See abstract and pages 281-283.	1-6
A	US 8617965 B1 (QUICK, NATHANIEL R. et al.) 31 December 2013 See abstract; and claims 1-8.	1-6
A	US 6703294 B1 (SCHONER, ADOLF et al.) 09 March 2004 See abstract; and claims 1-5.	1-6



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

21 August 2015 (21.08.2015)

Date of mailing of the international search report

24 August 2015 (24.08.2015)

Name and mailing address of the ISA/KR


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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/034117

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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US 8617965 B1	31/12/2013	None	
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