(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
28 April 2011 (28.04.2011)

PCT

(10) International Publication Number
WO 2011/049428 A1

(51) International Patent Classification:
G01N 27/414 (2006.01)

(21) International Application Number:
PCT/MY2010/000215

(22) International Filing Date:
19 October 2010 (19.10.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
PI20094402 20 October 2009 (20.10.2009) MY

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

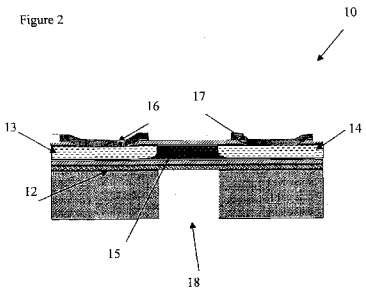
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) Title: INVERTED ISFET

Figure 2



(57) Abstract: An inverted ion-sensitive field effect transistor (ISFET) (10) comprises a substrate layer (11), a sensing membrane (12) on said substrate layer (11), a layer of field oxide (19) on said sensing membrane (12), doped source (13) and drain (14) regions on said layer of field oxide (19), and characterized in that electrical contacts (16, 17) are provided to the respective source (13) and drain (14) regions on the opposing side of said sensing membrane (12) and said substrate layer (11) is windowed with an opening access (18) to said sensing membrane (12) to provide electrical isolation of the electrical contacts (16, 17) from said sensing membrane (12).

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Inverted ISFET

Field of Invention

The present invention relates to ion-sensitive field effect transistor (ISFET) , more particularly relates to a ISFET having isolation of the fluid interacting sensing membrane area with the electrical conducting area.

Background of Invention

Chemical sensors for detecting chemical compounds are widely used in different field such as medical diagnosis, water treatment system, food processing and the like. Conventional chemical sensor such as glass electrode and spectrophotometer are relatively large in size, difficult to be handled, and expensive as required lots of building parts for construction. In view of this, miniaturized semiconductor sensors were devised and now replacing the use of conventional chemical sensor.

Ion-sensitive field effect transistor (ISFET) is one of the most widely employed semiconductor at present which is incorporated

into chemical sensor for chemical compounds detection and specifically for pH sensing. Since fabrication of the ISFET is through integrated circuit process technology, the chemical sensor produced are much smaller in size, easier for standardization with high reproducibility and is ready for mass produce hence reducing the manufacturing cost. Nevertheless, attempts to reduce the manufacturing cost by introducing more functionality and integration with other semiconductor devices, while further improve the performance of the ISFET, have never end. Reducing the number of substrates or fabrication processes involved are known to be one of the more effective ways to attain the aforesaid purposes. A basic schematic of the ISFET fabricated using micromachining technology is shown in Figure 1.

Recent advancement in technologies generates a strong trend towards miniaturized analysis system. Conventional ISFETs have metal contacts and the sensing gate on the same surface of the wafer hence they require separate packaging module so that only the gate will be in contact with the liquid sample. The metal contacts and the sensing gate are on different thickness level, therefore this creates packaging problem such as alignment during packaging process, leakage, bonding performance, etc. Those

ISFETs have high current losses and leakage issues as only a minimum part of the substrate itself would be required to build the FET while other large silicon conducting area will be omitted from the device application but which, will indirectly affect the performance of the ISFET. They are also fabricated on bulk thick substrate where it has been associated with problems such as low saturation current and reduced short-channel/floating body effects.

US Patent Publication No. 7321143 discloses an ion-sensitive field effect transistor includes a substrate on which there are formed a source region and a drain region. Above a channel region, the ion-sensitive field effect transistor has a gate with a sensitive layer including a metal oxide nitride mixture and/or a metal oxide nitride mixture compound.

US Patent Publication No. 7321143 discloses an integrated ion sensor, which comprises at least one ion selective membrane sensitive to ions contained in a solution to be measured for detecting the concentration of the ions, a signal processing circuit for inputting a detected signal obtained by the ion selective membrane through a conductive member and fetching the

detected signal through MOSFETs or the like included in an input stage to process the same, a reference electrode disposed in the measuring environment made by the solution to be measured and to be set to a predetermined voltage relationship between the reference electrode and the ion selective membrane, and a power supply having negative and positive terminals for supplying a driving power to the signal processing circuit through the terminals, one of the terminals being connected to the reference electrode, wherein the signal processing circuit is set to an active state at a voltage set to the reference electrode by controlling the threshold value of at least one of the MOSFETs of the signal processing circuit.

From the foregoing, it will be noted that the sensors formed with the contact pad and sensing membrane on same surface and thus requires packaging process to isolate electrical contacts from the sensing area. Further there is no injection or opening window on basic device and thus requires additional passivation layers for isolation of electrical conducting area with fluid interface area.

The present invention is an inverted ISFET with the sensing membrane and metal contact pads on opposing sides of the substrate. This improved configuration allow isolation of the fluid interacting sensing membrane area with the electrical conducting area by reducing the possibility of the electrical circuit being shorted due to the presence of the conducting fluids. It is formed with a thin silicon-based substrate for development of the FET region for improved performance as it has been shown that FET made on fully depleted ultra thin films have additional benefits of nearly ideal sub-threshold slope, increased saturation current and reduced short-channel/floating body effects due to the lower effective substrate electric field.

Other objective of the present invention is to provide a more cost effective ISFET sensor which is integrated or self-formed with sensing window on the sensing membrane hence allowing the elimination of the bonding requirement to attach the sensing window or packaging onto the sensing membrane and therefore fluid leakage problems will be improved and addressed leading to a leakage-free fluid-sensing membrane interface area.

Still another objective of the present invention is to provide the ISFET sensor which can be microfabricated for miniaturization purpose.

Other objects of this invention will become apparent on the reading of this entire disclosure.

Summary of Invention

In one aspect of the present invention, an inverted ion-sensitive field effect transistor (ISFET) comprises a substrate layer, a sensing membrane on the substrate layer, a layer of field oxide on the sensing membrane, doped source and drain regions on the layer of field oxide, and characterized in that electrical contacts are provided to the respective source and drain regions on the opposing side of the sensing membrane and the substrate layer is windowed with an opening access to the sensing membrane to provide electrical isolation of the electrical contacts from the sensing membrane.

A method of manufacturing an inverted ISFET comprising the steps of providing a substrate layer, depositing a layer of sensing

membrane on the substrate layer, depositing a layer of field oxide on the sensing membrane, depositing a layer of doped polysilicon on the field oxide layer, etching the respective source and drain regions using photoresist, and providing the electrical contacts for the source and drain regions, characterized in that the electrical contacts are provided on the opposing side of the sensing membrane to provide electrical isolation of the electrical contacts from the sensing membrane.

Brief Description of the Drawings

Other objects, features, and advantages of the invention will be apparent from the following description when read with reference to the accompanying drawings. In the drawings, wherein like reference numerals denote corresponding parts throughout the several views:

Figure 1 shows a schematic diagram of the ISFET of (a) basic elements (b) cross sectional view of the microfabricated ISFET and (c) the ISFET device;

Figure 2 depicts an inverted ISFET of the present invention;

Figure 3 is a step by step fabrication process flow of the inverted ISFET of the present invention which are shown in Figure 3a to 3m.

Detailed Description of the Preferred Embodiments

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be understood by those of ordinary skill in the art that the invention may be practiced without these specific details. In other instances, well-known methods, procedures and/or components have not been described in detail so as not to obscure the invention. Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

Referring now to Figures 2 and 3 , an inverted ion-sensitive field effect transistor (ISFET) of the present invention generally designated as numeral reference 10。 Figure 2 shows a cross sectional view of the inverted ISFET (10) having the desired configuration as obtained when manufactured in accordance to the present invention。 The substrate (11) of the inverted ISFET (10) is a polysilicon layer which is a thin film silicon based layer

in order to provide an improved performance of the ISFET。However, the substrate (11) is not limited to silicon but other types of substrates such as glass, SOI, etc can also be used to realize the device fabrication。

On the front side of the substrate (11), it is deposited with a layer of sensing membrane (12) which is preferably a nitride sensing membrane such as silicon nitride (Si_3N_4)。The inverted ISFET (10) is doped to have a source region (13) and a drain region (14)。In between the source (13) and drain (14) regions there is a doped polysilicon area (15). The source region (13) is provided with a metal source contact (16) and the drain region (14) is provided with a metal drain contact (17)。These contacts (16, 17) and the sensing membrane (12) are on the opposing side of the substrate (11)。The substrate (11) is windowed with a window opening (18) towards the sensing membrane (12) hence allowing the elimination of the bonding requirement to attach the opening window or packaging onto the sensing membrane area。

The method of manufacturing the inverted ISFET (10) of the present invention is now described。The process is started with a wafer of silicon as the substrate (11) of the inverted ISFET (10)。The

substrate (11) is then deposited (31) with a layer of sensing membrane (12) and a layer of field oxide (19) at the front of the substrate (11) as shown in Figure 3a. The sensing membrane (12) is a silicon nitride (Si_3N_4) layer and the field oxide layer (19) is a silicon dioxide (SiO_2) layer. A layer of doped polysilicon (15) is then deposited (32) on the field oxide layer (19) as shown in Figure 3b. Then a sacrificial layer of field oxide (20) is deposited (33) on the doped polysilicon layer (15) and followed by a layer of silicon nitride (Si_3N_4) (21) as shown in Figure 3c. The sacrificial layer of field oxide (20) is a layer of silicon dioxide (SiO_2).

The process is then followed with a resist coating and patterning (34) to cover the part that is not to be etched as shown in Figure 3d. The doped polysilicon layer (15) is etched (35) with the source (13) and drain (14) regions using photoresist as shown in Figure 3e. The resist coating is then removed and performed (36) a channeling implant as shown in Figure 3f. The sacrificial layer of field oxide (20) and the layer of silicon nitride (Si_3N_4) are then removed (37) as shown in Figure 3g. A protective layer of field oxide (23) is then deposited (38) on the wafer as shown in Figure

3h. The protective layer of field oxide (23) is a layer of silicon dioxide (SiO_2).

A resist coating and patterning (25) for contact pad (22) is then performed (39) on the wafer leaving openings to provide access to the source (13) and drain (14) regions as shown in Figure 3i. The protective layer of silicon dioxide (SiO_2) is etched (40) respectively towards both source (13) and drain (14) regions to provide contact access to said regions as shown in Figure 3j. The resist coating (23) is then removed and the metal contact pad (22) is sputtered (41) on the wafer as shown in Figure 3k.

A resist coating and patterning (24) for metal etching is then performed (42) on the wafer leaving the center portion uncovered as shown in Figure 3l. The middle portion of the metal contact pad (22) is then etched (43) and leaving the metal source contact (16) and the metal drain contact (17) in contacts with the source (13) and drain (14) regions respectively as shown in Figure 3m. The resist coating (24) is then removed (44) as shown in Figure 3n.

The middle portion from the back of the substrate (11) is then etched (45) using deep reactive ion etching (DRIE) or wet etching

until the sensing membrane layer (12) to provide the window opening (18) to the sensing membrane (12) hence eliminating the requirement of the bonding process and additional substrate or packaging material. The metal contacts (16, 17) are provided on the opposing side of the sensing membrane (12), thus, when user injects samples to the opening window at the sensing membrane (12) the fluid will be isolated from the electrical conducting area hence prevents electrical shorting from occurring as shown in Figure 3o. The present invention is not limited in its present form and can be configured with additional features. For instance, the bottom of the substrate (11) can be etched or constructed with, but not limited to, microfluidic features such as microchannel, reservoir, micromixers, etc near the sensing membrane (12) area upon the formation of the opening window.

As will be readily apparent to those skilled in the art, the present invention may easily be produced in other specific forms without departing from its essential characteristics. The present embodiments is, therefore, to be considered as merely illustrative and not restrictive, the scope of the invention being indicated by the claims rather than the foregoing description, and all

changes which come within therefore intended to be embraced therein.

Claims

1. An inverted ion-sensitive field effect transistor (ISFET) (10) comprising:

a substrate layer (11);

a sensing membrane (12) on said substrate layer (11);

a layer of field oxide (19) on said sensing membrane (12);

doped source (13) and drain (14) regions on said layer of field oxide (19); and

characterized in that electrical contacts (16, 17) are provided to the respective source (13) and drain (14) regions on the opposing side of said sensing membrane (12) and said substrate layer (11) is windowed with an opening access (18) to said sensing membrane (12) to provide electrical isolation of the electrical contacts (16, 17) from said sensing membrane (12).

2. The inverted ISFET (10) as claimed in claim 1, wherein said substrate layer (11) is a thin film silicon based layer.

3. The inverted ISFET (10) as claimed in claim 2, wherein said substrate layer (11) is a polysilicon layer.

4. The inverted ISFET (10) as claimed in claim 1, wherein said substrate layer (11) could be other types of substrates such as glass, silicon on insulator (SOI) and the likes.

5. The inverted ISFET (10) as claimed in claim 1, wherein said sensing membrane (12) is a nitride sensing membrane.

6. The inverted ISFET (10) as claimed in claim 5, wherein said sensing membrane (12) is silicon nitride (Si_3N_4).

7. The inverted ISFET (10) as claimed in claim 1, wherein said substrate layer (11) can be etched at the bottom of said substrate (11) with microfludic features such as microchannel, reservoir, micromixers and the likes.

8. A method of manufacturing an inverted ISFET (10) comprising the steps of:

providing a substrate layer (11);

depositing (31) a layer of sensing membrane (12) on said substrate layer (11);

depositing (31) a layer of field oxide (19) on said sensing membrane (12);

depositing (32)a layer of doped polysilicon (15) on said field oxide layer (19);

etching (35) the respective source (13) and drain (14) regions using photoresist; and

providing (44) the electrical contacts (16, 17) for said source (13) and drain (14) regions,

characterized in that said electrical contacts (16, 17) are provided on the opposing side of said sensing membrane (12) to provide electrical isolation of the electrical contacts (16, 17) from said sensing membrane (12).

9. The method as claimed in claim 8, wherein said method further comprising the step of etching (45) a window opening (18) from the back of said substrate (11) to provide opening access to said sensing membrane (12).

10. The method as claimed in claim 8, wherein said step of etching (35) the respective source (13) and drain (14) regions using photoresist includes the steps of:

providing (33) a sacrificial layer of field oxide (20) on said doped polysilicon layer (15);

providing (33) a layer of silicon nitride on said sacrificial layer of field oxide (20);

patterning and resist coating (34) to cover the part that is not to be etched;

removing (36) said resist coating after said source (13) and drain (14) regions are etched;

removing (37) said sacrificial layer of field oxide (20) and layer of silicon nitride; and

providing (38) a protective layer of field oxide (21) on said ISFET.

11. The method as claimed in claim 8, wherein said providing (44) the electrical contacts (16, 17) for said source (13) and drain (14) regions includes the steps of:

patterning and resist coating (39) to cover the part that is not to be etched;

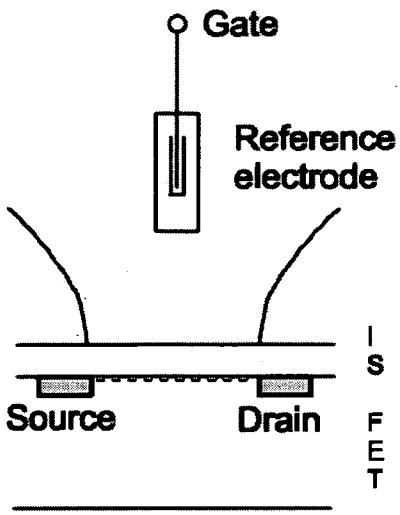
etching (40) towards said source (13) and drain (14) regions to provide contact access to said regions;

removing (41) said resist coating (23);

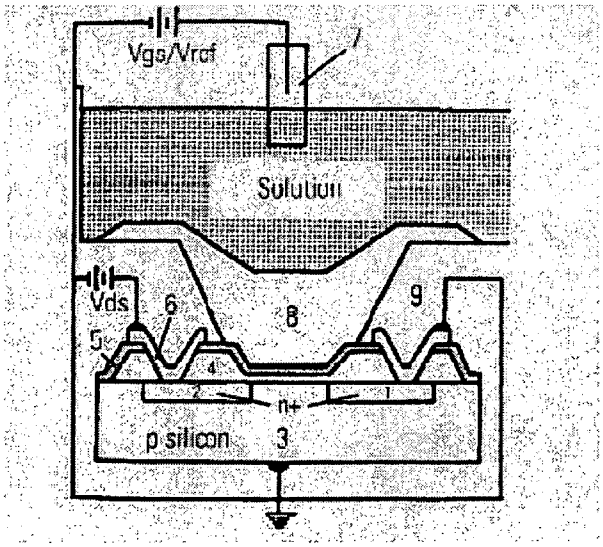
sputtering (41) a metal contact pad (22) on said ISFET;

patterning (42) and resist coating (24) for metal etching with the center portion uncovered; and

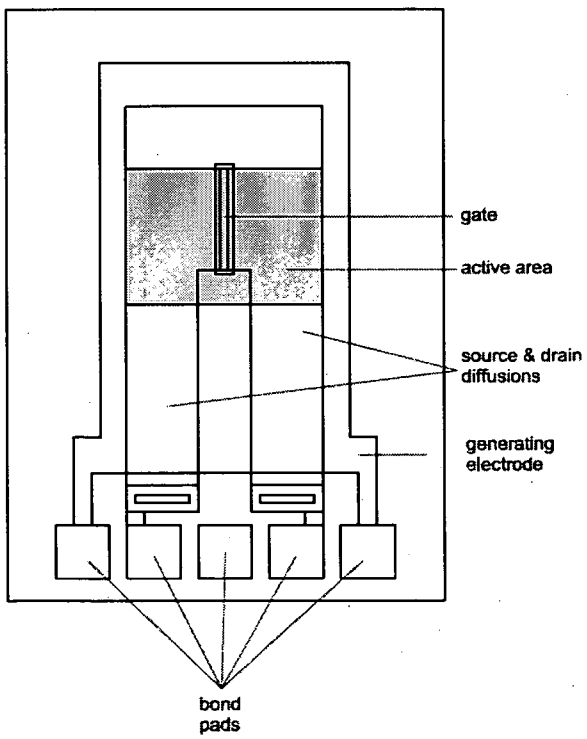
etching (43) said center portion of said metal contact pad (22) for forming said metal source contact (16) and metal drain contact (17).


Gate
Reference electrode
Source
Drain
ISFET

(a)


Vgs/Vref
Solution
Vds
6
8
9
5
4
2
1
n+
p silicon
3

(b)


gate
active area
source & drain diffusions
generating electrode
bond pads

(c)

Figure 1

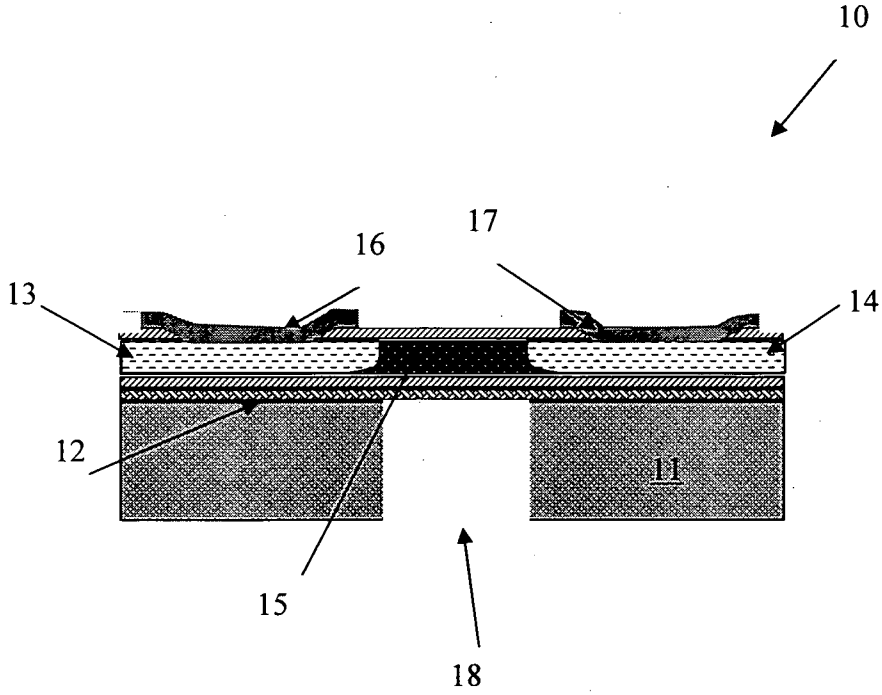


Figure 2

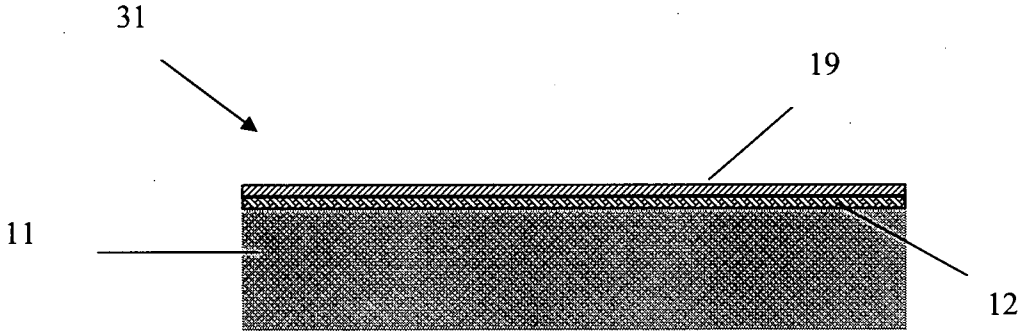


Figure 3a

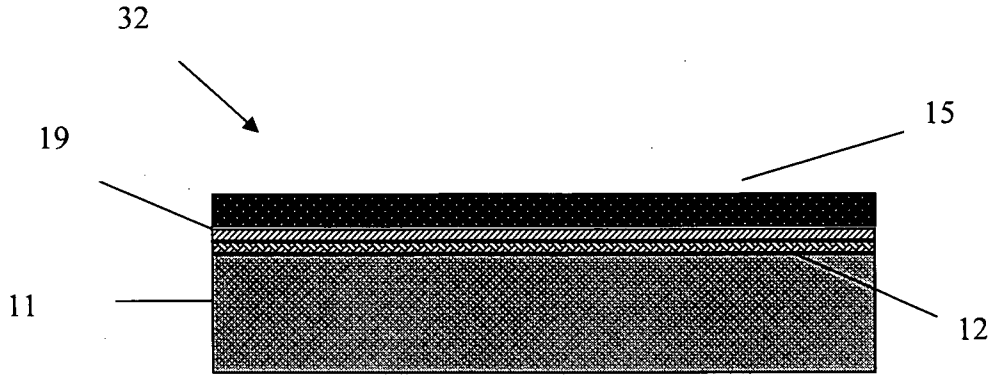


Figure 3b

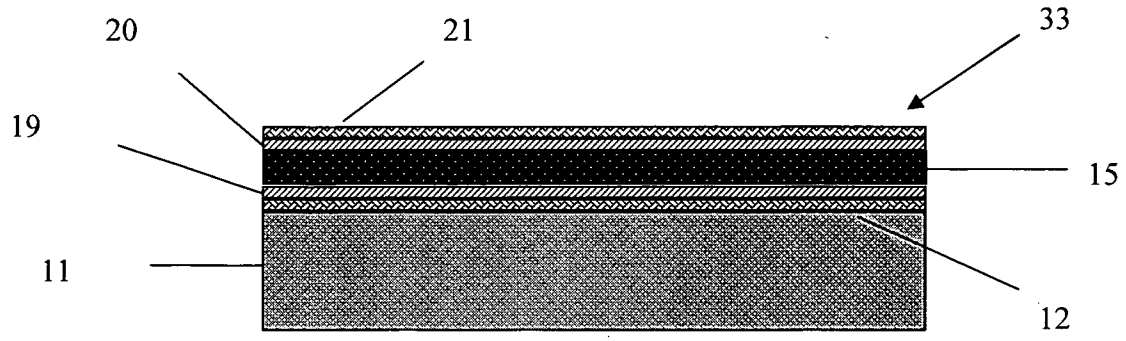


Figure 3c

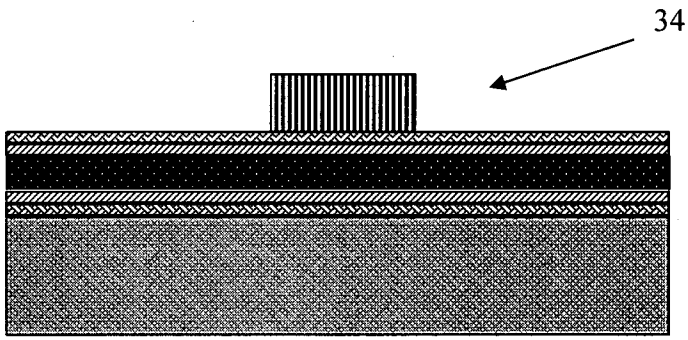


Figure 3d

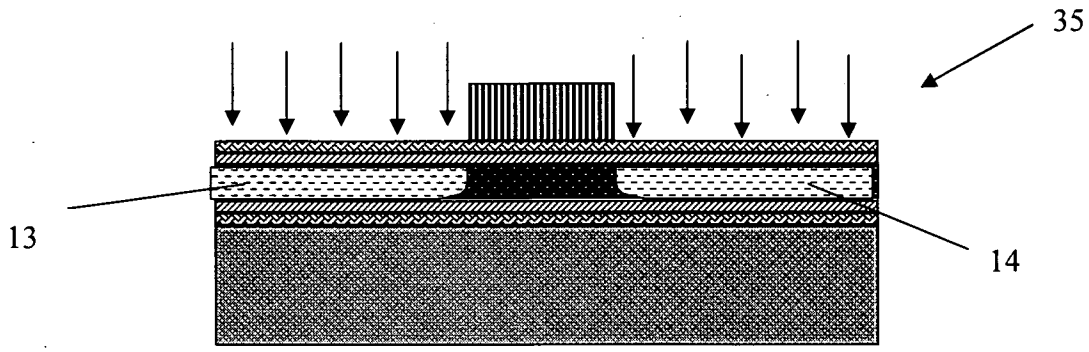


Figure 3e

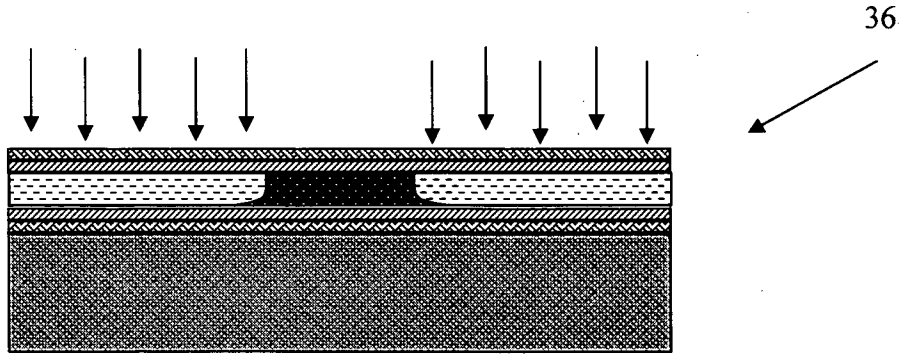


Figure 3f

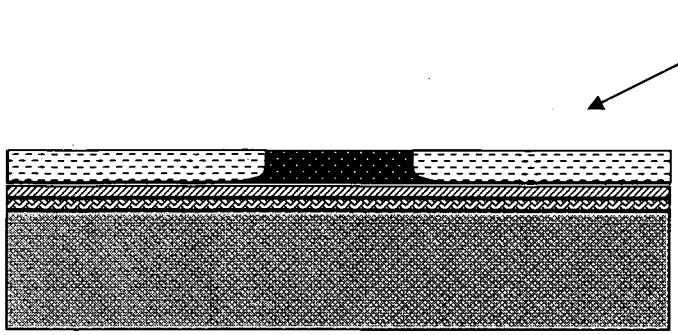


Figure 3g

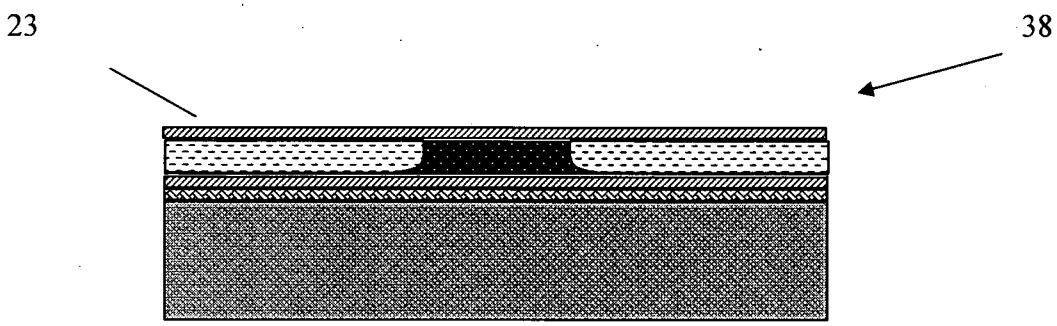


Figure 3h

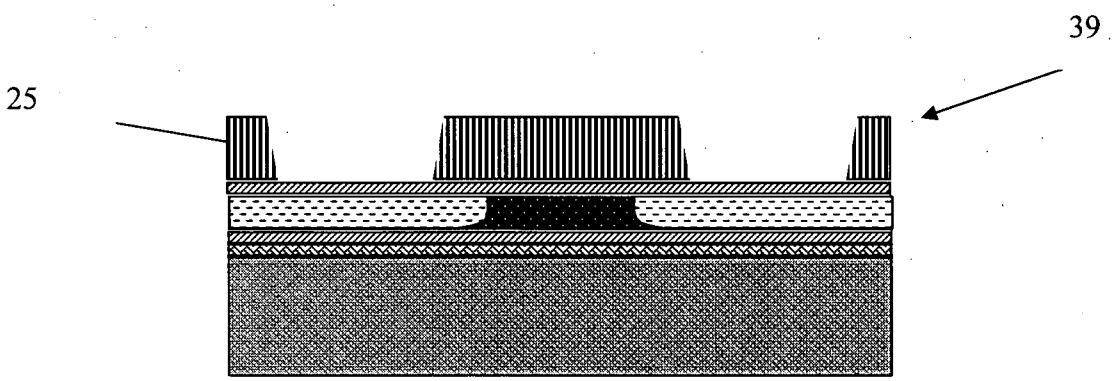


Figure 3i

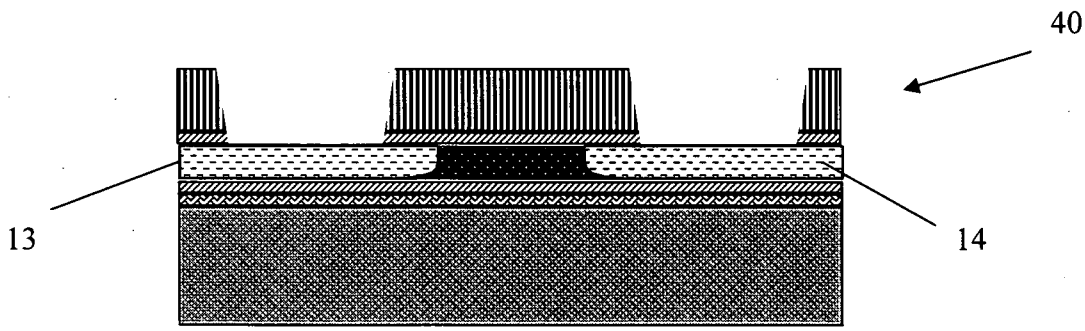


Figure 3j

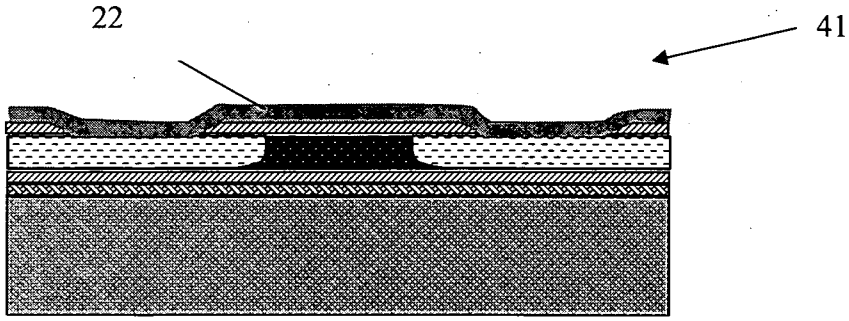


Figure 3k

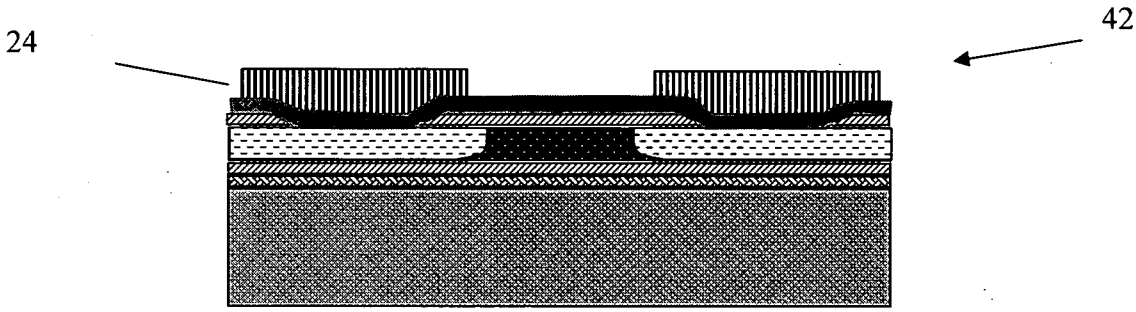


Figure 3l

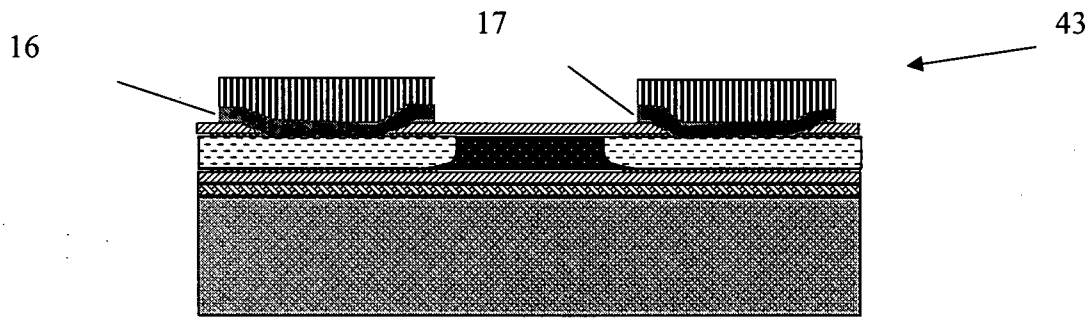


Figure 3m

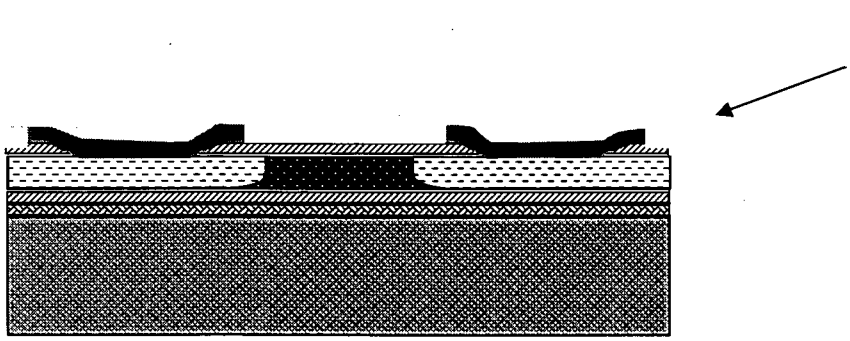


Figure 3n

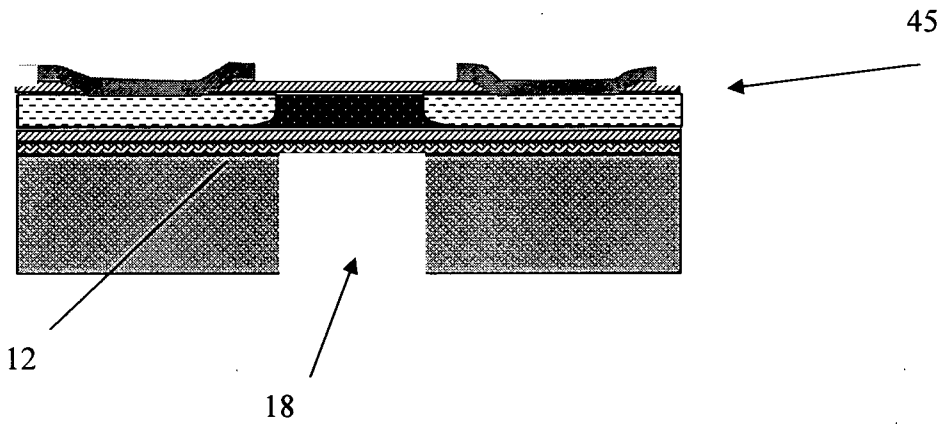


Figure 3o

INTERNATIONAL SEARCH REPORT

International application No.
PCT/MY2010/000215

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

G01N 27/414 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
WPI, EPODOC, USPTO, Esp@cenet, GooglePatents (Keywords: ISFET, Field Effect Transistor, Ion_Sensitive, Oxide etc)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 1994/022006 A1 (FRAUNHOFER-GESELLSCHAFT ZUR FORDERUNG DER ANGEWANDTEN FORSCHUNG E.V.) 29 September 1994 (English Translation retrieved 24 January 2011, URL: http://translationgateway.epo.org/emtp/gw/?ACTION=description-retrieval&OPS=ops.epo.org&LOCALE=en_EP&FORMAT=docdb&COUNTRY=DE&NUMBER=4308081&KIND=A1&T=1). See Page 2, Paragraph 4, Page 7, Paragraph 4 &7, Page 8, Paragraph 5, Figure 4.	1-9
A	US 2005/0186697 A1 (YANG) 25 August 2005. See All.	1-11
A	US 4961833 A1 (SAKAI et al.) 9 October 1990. See All.	1-11
A	EP 0363805 A1 (ENIRICERCHE S.p.A) 18 April 1990. See All.	1-11

☐ Further documents are listed in the continuation of Box C ☒ See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 January 2011	01 FEB 2011
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. +61 2 6283 7999	Authorized officer **STEVEN HOWELL** AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No : +61 2 6283 7996

INTERNATIONAL SEARCH REPORT

International application No.
PCT/MY2010/000215

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a)

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

See Supplemental Box 1

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☒ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

Supplemental Box 1
(To be used when the space in any of Boxes I to IV is not sufficient)

Continuation of Box No: III

This International Application does not comply with the requirements of unity of invention because it does not relate to one invention or to a group of inventions so linked as to form a single general inventive concept.

In assessing whether there is more than one invention claimed, I have given consideration to those features which can be considered to potentially distinguish the claimed combination of features from the prior art. Where different claims have different distinguishing features they define different inventions.

This International Searching Authority has found that there are different inventions as follows:

- Claim 1-7 are directed to an inverted ISFET comprising a substrate layer, a sensing membrane on said substrate layer, a layer of field oxide on said sensing membrane, doped source and drain regions on said layer of field oxide, characterised in that electrical contacts are provided to the respective source and drain regions on the opposing side of said sensing membrane, and said substrate layer is windowed with an opening access to said sensing membrane to provide electrical isolation of the electrical contacts from said sensing membrane. It is considered that the said substrate layer being windowed with an opening access to said sensing membrane comprises a first distinguishing feature.

- Claims 8-11 are directed to a method of manufacturing an inverted ISFET comprising the steps of providing a substrate layer, depositing a layer of sensing membrane on said substrate layer, depositing a layer of field oxide on said sensing membrane, depositing a layer of doped polysilicon on said field oxide layer, etching the respective source and drain regions using photoresist, and providing the electrical contacts for said source and drain regions, characterised in that said electrical contacts are provided on the opposing side of said membrane to provide electrical isolation of the electrical contacts from said sensing membrane. It is considered that depositing a layer of doped polysilicon on said field oxide layer comprises a second distinguishing feature.

PCT Rule 13.2, first sentence, states that unity of invention is only fulfilled when there is a technical relationship among the claimed inventions involving one or more of the same or corresponding special technical features. PCT Rule 13.2, second sentence, defines a special technical feature as a feature which makes a contribution over the prior art.

Each of the abovementioned groups of claims has a different distinguishing feature and they do not share any feature which could satisfy the requirement for being a special technical feature. Because there is no common special technical feature it follows that there is no technical relationship between the identified inventions. Therefore the claims do not satisfy the requirement of unity of invention *a priori*.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/MY2010/000215

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member			
WO	9422006	DE	4308081		
US	2005186697	US	7211459	US	2004222446
US	4961833	JP	1250849		
EP	0363805	US	5077229		

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX