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Balanced drive symmetric MIM diode configuration for liquid crystal displays and method of operating same.

An active matrix liquid crystal display (10) and method for rapidly storing and efficiently retaining electric charge in selected ones of a plurality of storage elements (46) are disclosed. Each storage element (46) is addressable through a pair of parallel row select address lines (12, 12', 14, 14') and a column address line (18, 20). A pair of MIM devices (34, 36) are coupled between the row select address lines (12, 12') and the storage element (46) is coupled between the common node (38) of the MIM devices (34, 36) and the column address line (18) to which charging potential is applied. During the charging of the storage element, operating potentials which are substantially equal and opposite in polarity are applied to the row select line pair to forward bias both MIM devices and thereafter operating potentials which are also substantially equal and opposite in polarity are applied to the two select line pair to reverse bias both MIM devices to provide retention of the charge in the storage element.

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FIELD OF THE INVENTION

The present invention generally relates to an electronic matrix system and method of operating the same. The present invention more particularly relates to a matrix system including storage elements, and employing MIM diode blocking elements ; and a drive method for rapidly storing electric charge in selected storage elements and efficiently retaining the charge stored therein the present invention is particularly useful in active matrix liquid crystal displays wherein the storage elements take the form of display picture elements.

BACKGROUND

In many electronic matrix systems, an array of storage elements, each having a unique address, are utilized in storing electric charge and can include for example, memory arrays and light influencing displays. In light influencing displays, the storage elements take the form of picture elements. The picture elements or pixels generally include a pair of spaced apart and facing electrodes having light influencing material disposed therebetween. As a result, each pixel constitutes a capacitor in which electric charge can be stored. The charge stored in a pixel results in a voltage potential across the electrodes and an electric field across the light influencing material. By controlling the amount of charge stored, the properties of the light influencing material can in turn be controlled to obtain a desired light influencing effect.

When the light influencing material is liquid crystal material, alignment of the liquid crystal material molecules can be obtained when the field applied to the material is above a certain threshold value. As is well known, liquid crystal displays generally include polarizers disposed on both sides of the display and alignment layers disposed on both side of the liquid crystal display material. When the field across the liquid crystal display material is above the threshold value, a pixel can be made light transmissive or light absorptive depending on the relative alignment of the polarizers and alignment layers ; when the field is below the threshold value, an opposite light influencing effect can be obtained. Since a display generally includes many pixels, an image can be formed by selectively controlling which pixels are transmissive to light and which pixels are absorptive to light.

In liquid crystal displays, (LCD's) it is necessary to update the condition of each pixel at regular intervals, for example, at a frame rate of thirty frames per second. This is required because the pixels can retain or store the applied potentials for a finite time. Updating is also required when nematic liquid crystal display material is employed because the applied potential must be reversed during alternate frames to avoid degradation of such liquid crystal display material.

Updating is further required when the displayed images are intended to change regularly, such as when the displayed images are constantly moving. Hence, the ability to rapidly transfer to and store electric charge in the pixels and to efficiently retain the stored charge for at least one frame period is essential.

To accurately drive the pixels of liquid crystal displays, active matrixes have been utilized. In such active matrixes, each pixel is associated with one or more threshold devices through which the potential to be stored in the pixel is applied to the pixel. The threshold devices have taken the form of field effect transistors or p-i-n diodes, for example various active matrixes employing differing configuration of threshold devices are disclosed in a number of references including for example: U.S. patent NO. 3,654,606 to Marlowe, et al, disclosing discrete, crystalline silicon diodes in an anode-to-cathode diode configuration ; U.S. patent No. 4,251,136 to Miner, et al teaching ring diode structures ; and a publication entitled Active Addressing for Flat Panel Display, 62 Japan Display 1986.

Active matrix liquid crystal displays employing amorphous silicon diodes as the threshold devices are disclosed, for example, in U.S. patent No. 4,868,616 issued September 19, 1989 in the names of Robert R. Johnson, Vincent D. Cannella and Zvi Yaniv. In accordance with at least one embodiment disclosed therein, each pixel includes a pair of p-i-n diodes coupled in non-opposing, anode-to-cathode relation between an address line pair and a common node. One electrode of the pixel is coupled to the common node and the other electrode is coupled to another address line or data line to which the pixel charging potential is applied. A nematic liquid crystal display material is disposed between the electrodes. When charging potential is applied to a pixel, one p-i-n diode is biased off and the other p-i-n diode is biased on by potential applied to the address line pair and to the data line. Hence, to charge the pixel, the charging potential is applied through one of the p-i-n diodes. As a result, the non-linear characteristics of the p-i-n diode which is in the ON condition must be overcome to provide the pixel with enough current to charge the pixel. The voltage drop across the p-i-n diode must be overcome to provide this current and the charge potential must also be applied for sufficient time to accommodate the series resistance imposed by the p-i-n diode. During the next frame, the state of the diodes is reversed to accommodate the reversal in the charge potential polarity. This can cause the voltage at the common node to vary. Such variance in the potential at the common node presents difficulties in controlling the ultimate voltage to which the pixel is to be charged and can adversely affect gray scale operation of the display.

More particularly, a p-i-n diode has a characteri-

stic capacitance associated therewith, which capacitance can degrade the operation of the pixel. As an example of the derogatory effects of the capacitance of the p-i-n diode, a charge of opposite polarity to the charge stored in the capacitance of the liquid crystal pixel may decrease the sensitivity of the pixel to charges being applied thereto. This effect has been found in virtually every scheme heretofore utilized for addressing (i.e. applying a series of electrical pulses to the liquid crystal matrix array so as to charge and discharge individual picture elements within the active matrix liquid crystal display), and is commonly known as the "capacitive kick" effect. When the p-i-n diode is switched from an off or a blocking condition to an on or conducting condition as to store or dissipate charge on the pixel as by recharging capacitance associated therewith, the current required to dissipate the charge present on the p = i-n diode cannot be distinguished from the current required to recharge the pixel capacitance. This situation may lead to the charging of the liquid crystal pixel at inappropriate times; the very problem the diode device was employed to prevent. Examples of these types of driving schemes are taught in, for example, U.S. patent No. 3,654,606 to Marlowe, et al.,; and U.S. patent No. 3,765,747 to Pankratz, et al.

A similar and possibly more serious problem, known as "capacitive kickback" occurs at the end of the charging period, at which point in time the p-i-n diode is switched from its on or conductive condition to its off or blocking condition. Typically, the p-i-n diode at this point in time has a significant voltage drop impressed across the current carrying electrodes thereof, which voltage drop could cause a significant transfer of charge from the capacitance of the liquid crystal element of the pixel to the capacitance of the isolation devices. This transfer of charge disturbs the voltage being maintained across the liquid crystal elements, and is not readily distinguishable from the current which is being stored upon said element, thereby adversely affecting the accuracy of the information stored thereupon.

In conventional arrays of liquid crystal elements, "capacitive kick" effect is always present and always adversely effects the signal to noise ratio of said element. The magnitude of the "capacitive kick" or "capacitive kickback" problem is directly related to the relative size difference between (and hence, the ratio of the capacitances of) the p-i-n diodes and the liquid crystal elements. This is because the capacitance of circuit elements is directly related to their physical size. In order to prevent the aforementioned transfer of charge from interfering with the storage of video voltages on the liquid crystal elements, it has heretofore been desirable to maintain a minimum of a 5 to 1 ratio is the size of the liquid crystal element to the size of the p-i-n diodes (and preferably a ratio of 10 to 1 or more).

The "capacitive kick" becomes a significant problem and severely limits the performance of high resolution liquid crystal displays which include a relatively small area liquid crystal elements. The reason for the increase in the "capacitive kick" problem in such array, is that the ratio of the area of the liquid crystal elements to the areas of the blocking elements is significantly decreased. The desired larger ratios cannot be maintained because of physical constraints upon lithography and processing which set a lower limit on blocking element size, particularly in large area displays where yield problems become much more severe as minimum lithography feature sizes decrease. As a result, the absolute sensitivity and speed of operation have heretofore decreased as the resolution of the liquid crystal displays has increased.

The lone teaching of a driving scheme which avoids the hereinabove described problems associated with "capacitance kick and capacitance kick-back" is presented in U.S. Patent No. 4,731,610 to Baron, et al. However, this patent is limited to a teaching of LCD's employing p-i-n diodes and field effect transistors as the blocking elements disposed around the common node. As is described in greater detail hereinbelow, these types of devices have inherent deficiencies when employed in LCD's, which deficiencies are overcome by the subject invention.

More particularly, FET's and p-i-n diodes, when employed in LCD's, require up to 7 or 4 mask steps respectively for fabrication, and require critical alignments of down to 1 micrometer. Accordingly, these complex structures reduce the yield of usable components per fabrication run and hence increase production costs. Additionally, FET's require the presence of crossing address lines on a common substrate, leading to short circuits, and hence further decreased yield. Alternatively, the LCD device disclosed and claimed herein is equipped with metal-insulator-metal (MIM) type blocking elements which can be fabricated by as few as two mask steps, thus making fabrication easier and hence yield greater. Additionally, by driving the MIM-equipped LCD described hereinbelow by the balanced drive address scheme described herein, the myriad problems discussed hereinabove (i.e., capacitance kick, etc.) may be avoided. Prior art MIM device equipped LCD's included but a single MIM disposed in series with the liquid crystal pixel. This resulted in poor displays characterized by: 1.) device instability resulting in image retention, e.e. a memory effect which degrades image quality 2.) large device capacitance resulting in the hereinabove described "kickback effect"; and 3.) lack of gray scale control and gray scale uniformity due to device non-uniformity across the display area.

In addition to the foregoing problems, it was difficult to manufacture a large area electronic matrix, such as a large area display, with devices having precisely the same I-V characteristics over the entire

length and width of the matrix. Thus, voltages applied to one pixel to achieve a particular gray scale effect or level may not product the exact same gray scale effect or level when applied to other pixels, especially those located some distance away from the first pixel.

Accordingly, there exists a need for an active matrix LCD configuration and addressing scheme which accommodates easy to fabricate threshold devices such as MIM's while circumventing the limitations inherent therein.

SUMMARY OF THE INVENTION

The invention provides an active matrix liquid crystal display system for rapidly storing and efficiently retaining electric charge in selected ones of a plurality of liquid crystal pixels. The system includes a plurality of substantially parallel address line pairs, a plurality of substantially parallel additional address lines crossing the address line pairs at an angle and being spaced from the address line pairs to form a plurality of crossover points therewith, and a pair of threshold devices coupled together at a common node and in series relation between the address line pairs associated with the crossover points. The threshold devices employed herein are limited exclusively to MIM type devices which block current at low bias (i.e., $I_{10^{-11}}$ A at V_{5} v) and conduct current at high bias i.e., ($I_{10^{-8}}$ A at V_{15} v) independent of the polarity, since the MIM device is bidirectional and therefore the IV curve thereof is symmetric with respect to polarity.

Each of the liquid crystal pixels is coupled between a respective one of the common nodes and one of the additional address lines. The system further includes first means for applying first operating potentials which are substantially equal in magnitude and opposite in polarity between the address line pairs to bias the threshold devices into a conducting condition for facilitating the storage of charge in the storage elements coupled thereto and second means for applying charging potential to selected ones of the additional address lines for providing electric charge to be stored in the selected storage elements during the application of the first operating potentials to the address line pairs.

Since the MIM devices are of the type which provide a high impedance to current flow at low bias, said first potential applying means applies second operating potentials which are substantially equal, and below the MIM devices conducting voltage, between the address line pairs to facilitate the retention of the charge stored in the pixels coupled thereto.

The invention further provides a method of operating an active matrix LCD including MIM devices, to rapidly store and efficiently retain electric charge in selected ones of the plurality of pixels of the display. The method includes the steps of providing a

plurality of substantially parallel address line pairs, providing a plurality of substantially parallel additional address lines crossing the address line pairs at an angle and being spaced from the address line pairs to form a plurality of crossover points therewith, and coupling a pair of MIM devices together at a common node between the address line pairs associated with the crossover points. The MIM devices are of the type which block current at low bias and conduct current at high bias, irrespective of polarity, since MIM devices are bidirectional, and therefore the IV characteristics thereof are symmetric with respect to polarity. The method further includes the steps of coupling each of the pixels between a respective one of the common nodes and one of the additional address lines, applying first operating potentials (which are substantially equal in magnitude and opposite in polarity) between the address line pairs to facilitate the storage of charge in the storage elements coupled thereto, and applying charging potential to selected ones of the additional address lines during the application of the first operating potentials to the address line pairs to store electric charge in the selected pixels.

Since the MIM devices are of the type which provide a high impedance to current flow at low bias, and the method further includes the step of applying second operating potentials which are substantially equal in magnitude between the address line pairs to bias the MIM devices into a second condition to facilitate the retention of the charge stored in the pixels coupled thereto.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic circuit diagram of an active matrix liquid crystal display embodying the present invention ;

Figs. 2A-2C are a first set of illustrative waveforms of the signals provided at output C, and row select signals provided at outputs R_1 and R_1' and respectively of the column and row select driver of Fig. 1 ;

Figs. 3A-3C are a second set of illustrative waveforms of the signals provided at output C, and row select signals provided at outputs R_1 and R_1' respectively of the column and row select driver of Fig. 1 ;

Fig. 4 is a current versus voltage curve to further illustrate the operation and method of the present invention ;

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to Fig. 1, it illustrates in schematic circuit diagram form an active matrix liquid crystal display 10 embodying the present invention. The system 10 includes a plurality of substantially parallel address

line pairs 12, 12', 14, 14', and 16, 16' which are row select lines, and a plurality of substantially parallel additional or column address lines 18 and 20. The column address lines 18 and 20 cross the row select address line pairs at an angle and are spaced from the row select address line pairs to form a plurality of crossover points therewith. Preferably, the column address lines 18 and 20 cross the row select address line pairs substantially perpendicularly thereto.

The system further includes a pixel at each of the crossovers defined by the crossing row select lines and the column address lines. To that end, the system includes pixels 22, 24, 26, 28, 30 and 32. Although just six pixels are illustrated, it is of course to be understood that the system 10 includes additional row select line pairs and column address lines with a corresponding additional number of pixels arranged in rows and columns to provide a display having a sufficient number of pixels so as to form a usable image.

Since the pixels are preferably substantially identical, only pixel 22 will be described in detail herein. Pixel 22, as can be seen in the figure, includes a pair of threshold devices 34 and 36 which are coupled together at a common node 38. The threshold devices 34 and 36 are metal-insulator-metal (MIM) devices and are coupled together between the row select address line pair 12 and 12'. The MIM devices are of the type which provide a high impedance to current flow when a low bias, i.e., $I_{10^{-11}}$ A at $V_{0.5}$ V (or no bias) is applied thereto, and a low impedance to current flow at high bias, i.e., $I_{10^{-8}}$ A at V_{15} v. Further, this characteristic is independent of the polarity of the applied bias since MIM devices are bidirectional, and accordingly the IV characteristic is symmetric with respect to polarity. The symmetric MIM configuration of two MIM devices disposed about a common node in electrical communication with the first electrode of the pixel, provides significant operational advantages over prior art, single MIM display pixels. These advantages will be discussed in detail hereinbelow.

The pixel 22 further includes a pair of electrodes 40 and 41 which are spaced apart and facing one another. Between the electrodes 40 and 42 is a light influencing material 44. The term "light influencing material" is meant to include any material which emits light or can be used to selectively vary the intensity, phase, or polarization of light either being reflected from or transmitted through the material. In accordance with this preferred embodiment, the light influencing material 44 is liquid crystal display material, such as a nematic liquid crystal material.

The electrodes 40 and 42 with the liquid crystal display material 44 disposed therebetween form a storage element 46 or capacitor in which electric charge can be stored. The storage element 46 is coupled between the common node 38 formed by the MIM devices 34 and 36 and to the column address line 18.

The MIM devices 34 and 36 are preferably formed from layers of deposited metallic or metal and insulating material. more specifically, the MIM's employed herein typically include a first metallic layer of a transparent conductive oxide material such as indium tin oxide (ITO). Deposited thereover is a layer of an insulating material such as SiN_x or Ta_2O_5 and preferably SiN_x ; and disposed thereover is the second layer of metal, in a preferred embodiment, a layer of chromium. The deposited layer of chromium must typically be etched in order to form for example, address lines, electrical interconnects, busines, etc.. However, in a preferred embodiment, the SiN_x layer can be made substantially transparent (i.e. 90% transparent) and therefore, said SiN_x layer does not require etching, as opposed to displays employing, for example, p-i-n diodes, wherein the amorphous semiconductor layers are not transparent and hence require additional mask and etch steps. Of course, should the SiN_x layer be high in Si content, the layer will appear yellow and requires etching. Additionally, said Si-rich layer will be more light sensitive and hence requires a separator mask step for the fabrication of a light shield.

The system 10 further includes a row select driver 50 having outputs R_1 , R_1' , R_2 , R_3 , and R_3' coupled to the row select address line pairs 12, 12', 14, 14', 16, and 16' respectively. The row select driver 50, as will be described subsequently, provides drive signals at its outputs to apply first operating potentials of high bias between the row select address line pairs to render the MIM devices conducting which facilitates the storage of charge in the storage elements coupled thereto. The row select driver also applies second operating potentials of low bias between the row select address line pairs to render the MIM devices non-conducting, to facilitate the retention of the charge stored in the storage elements coupled thereto.

Lastly, the system 10 includes a column driver 52. The column driver 52 includes a plurality of outputs, C_1 and C_2 , which are coupled to the column address lines 18 and 20 respectively. The column driver applies charging potential to selected ones of the column address lines for providing electric charge to be stored in selected storage elements during the application of the first operating potentials to the row select address line pairs by the row select driver 50.

It is important to emphasize the insensitivity of the symmetric MIM (SMIM) configuration to changes in the performance characteristic of the MIM devices, particularly when compared to conventional single MIM display pixels. In the equivalent circuit of a conventional single MIM display, the voltage across the MIM device decreases while the pixel is charged up, i.e., while a charging potential is being applied thereto. This reduces the MIM current and the charging will therefore slow down and not reach saturation.

The final voltage at the end of the scan time is then critically dependent on the MIM IV characteristic. In the MIM circuit configuration, there is an extra current path to the second MIM diode in the simultaneous scan mode. A high current keeps flowing until the end of the scan period and the charging will saturate. The final voltage across the LC at the end of the scan time is thus much less dependent of the MIM IV curve (see Figure 4). The image retention in SiN_x displays is caused by a decrease in K, the charging characteristic, for devices at pixels which have been ON for an extended period of time as compared to surrounding OFF pixels. Device non-uniformity (for instance due to a lack of accurate control of the SiN_x layer thickness across the display area) also causes a variation in K. Since in the SMIM configuration holding voltage does not depend on K, this approach is insensitive to device degradation and device non-uniformity. The capacitance kickback discussed hereinabove, (and in more detail hereinbelow) is also eliminated in an SMIM pixels, because the kickbacks for the two diodes have opposite polarity in the simultaneous scan mode and compensate each other.

Referring now to Figs. 2A, 2B and 2C, they collectively illustrate a first set of waveforms which demonstrate how charge is stored in the storage element 46 of pixel 22 and thereafter retained therein. More specifically, Fig. 2A illustrates the waveform of the signal provided at output C_1 of the column drive 52, Fig. 2B illustrates the waveform of the signal provided at output R_1 of the row select driver 50, and Fig. 2C illustrates the waveform of the signal provided at output R_1 , of the row select driver 50.

At t_0 , the row select driver 50 applies -15 volts to the row select address line 12 and +15 volts to row select line 12^1 to bias the MIM devices 34 and 36 into a conducting condition. With the MIM devices 34 and 36 thus biased, any charge previously stored in the storage element 46 is retained therein. In the immediately succeeding frame, if charge is to be once again stored in the storage element 46, the column driver 52 provides at its output C_1 which is coupled to the column address line 18 a + 3 volts at t_1 . Immediately thereafter, the row select driver 50 provides at t_2 a 0 volts to row select line 12 and a 0 volts to row select line 12^1 . Hence, the row select driver has provided at t_2 operating potentials to the address line pair formed by lines 12 and 12^1 which are substantially equal in magnitude and opposite in polarity to bias the MIM devices 34 and 36 into a non-conducting condition. With the MIM devices 34 and 36 thus biased, the +3 volts applied to electrode 42 of the storage element 46 will charge the storage element 46 through a current path which extends from the column address line 18, through the storage element 46, and through MIM device 36.

At t_3 , the storage element 46 is charged to an extent sufficient to exceed the threshold voltage of the

liquid crystal display material 44 and the row select driver 50 returns the row select line 12 to a -15volts and the row select line 12^1 to a 15 volts to bias the diodes 34 and 36 to their conducting condition. Immediately thereafter at t_4 , the column driver 52 terminates the charging potential of +3 volts and the column address line 18 applied to -3 volts. It is preferred that all of the storage elements within the row defined by the row select address line pairs 12 and 12^1 are charged in parallel so that once these storage elements are charged, the next row defined by the row address lines 14 and 14^1 can be selected by the row select driver 50 to bias the MIM devices coupled therebetween. Hence, during the time in which the storage elements of the row defined by the row select lines 12 and 12^1 are charged, the other row select lines are provided with operating potentials from the row select driver 50 to bias the MIM devices coupled therebetween. To that end, as the storage element 46 is charged, the row select address lines 14 and 16 receive from the row select driver a -15 volts and the row select lines 14^1 and 16^1 receive a +15 volts.

In accordance with this preferred embodiment, the liquid crystal display material 44 is a nematic liquid crystal display material and thus the sense of the potential applied thereto is preferably reversed during the next succeeding frame. Those in the art should appreciate that the MIM device pairs associated with the storage elements need only be biased sufficiently to allow for current flow, and establish a common node voltage which remains at approximately 0 volts as the individual storage elements are being charged to achieve the basic benefits of the present invention.

Referring now to Figs. 3A, 3B, 3C, 3D and 3E, they collectively illustrate a second set of waveforms which demonstrate how charge is stored in the storage element 46 of pixel 22, and thereafter retained therein. More specifically, Figure 3E illustrates the waveform of the signal provided at output C_1 of the column driver 52, Figure 3A illustrates the waveform of the signal provided at output R_1 of row select driver 50, Figure 3B illustrates the waveform of the signal provided at output R_1^1 of row select driver 50, Figure 3C illustrates the waveform of the signal provided at output R_2 of row select driver 50 and Figure 3D illustrates the waveform of the signal provided at output R_2^1 of row select driver 50. Significant characteristics of this driving scheme include a holding voltage to keep leakage minimal during frame time and the voltage change at the end of the scan time are equal for both MIM devices in a display so that voltage kickback from the devices cancel out.

At this t_0 , the row select driver 50 has been holding row select address line 12 and 12^1 at their respective holding voltages of -2 volts each. From time t_0 , to time t_1 , row select pair 12, 12^1 , i.e., that row addressed by outputs R_1 and R_1^1 , is selected by applying a select voltage to said outputs R_1 and R_1^1 . At output R_1 , at

time t_0 the voltage applied thereto by the row select driver is 17 volts. At output R_1' , the voltage applied thereto at time t_0 is -13 volts. The effect of applying voltages as described hereinabove is to bias the MIM devices 34 and 36 into their conductive condition. With the MIM devices 34 and 36 thus biased, any charge stored in the storage element 46 is retained therein. Accordingly, from time 0 to time t_1 , a voltage from +2 volts to -2 volts is applied along column address line 18 at output C_1 . In this way, storage element 46 is selected during the time period from time t_1 , it is not desired to select storage element 46, thus in order to retain the charge stored or applied thereto, it is necessary to remove the voltages at outputs R_1 and R_1' . This is accomplished at output R_1 by reducing the applied voltage thereto +17 volts to +2 volts ; at the same time the voltage at output R_1' is reduced from -13 volts to +2 volts. Thus, it can be seen that at the end of the scan time the holding voltages of output R_1 and R_1' are such that the voltage change for output R_1 and R_1' at the end of said scan time are equal (i.e. 15 volts) so that the capacitance kickback from MIM device 34 and 36 are equal and thus cancel out thereby eliminating the kickback phenomena. During the remainder of the non-select time, i.e. for example, from time t_1 through t_6 , outputs R_1 and R_1' are maintained at their holding voltage of 2 volts. As referred to hereinabove, the use of a holding voltage is employed on both scan lines to keep the voltage across the two MIM devices and therefore their leakage, minimal during the frame time.

At time t_1 , at which point in time, outputs R_1 and R_1' have been returned to their holding voltage thus "turning off" storage device 46 so that the charge applied thereto is retained until such time as that row is next selected. At time T_1 through T_2 , the storage element of pixel 26 is addressed so as to store a charge applied by column address line 18 from output C_1 of the column driver. As can be seen in Figures 3C and 3D, the voltage at output R_2 and R_2' at the start of time t_1 is the holding voltage of 2 volts. As the storage element of pixel 26 is to be selected, the voltage applied to output R_2 is -17 volts while the voltage applied to output R_2' is +13 volts. These voltages are maintained for one frame — time during which period the output from column driver 52 and output C_1 along column address line 18 is at +2 volts so as to store charge on the storage element of pixel 26. At time t_2 , once said charge has been stored at pixel 26, it is necessary to remove the voltage applied at outputs R_2 and R_2' . This is accomplished by reducing the output at R_2 from -17 to a holding voltage of -2 volts while simultaneously reducing the voltage R_2' from +13 volts to the holding voltage of -2 volts. Thus, it can be appreciated that the holding voltages for both output R_2 and R_2' are equal and further that the change in voltage at the end of this scan time, i.e. +15 volts and -15 volts are equal for both MIM devices in the pixel so that the voltage kick-

back from the devices cancel one another out. Employing the driving scheme illustrated in Figures 3A through 3E, can be seen that the wave form for driving pixels within an active matrix liquid crystal display repeats every four select scans. More specifically, it can be seen that after the fourth select, output R_1 holding voltage has returned to -2 volts. Thus, the same wave form as illustrated in Figure 2A is repeated. Similarly, repetitions of the waveform of Figures 3B, 3C, and 3D begin after the fourth select scan time for each row.

The driving scheme illustrated in Figs. 3A-3E has several advantages over prior art driving schemes. These include : 1. A holding voltage employed on both scan lines to keep the voltage across the two MIM devices and therefore their leakage minimal during the frame time ; 2) the video and LC polarity are alternated every row to eliminate flicker and grey scale non-uniformity ; 3) the amplitude of the video signal is kept small to reduce cross-talk from the columns ; 4) the voltage change for output 1 output 2 of a given row pair at the end of the scan time are equal so that voltage kickbacks from the MIM devices in that pixel cancel out ; 5) the driving levels for output 1 and output 2 of a given row pair are exactly the same so that the MIM devices degrade exactly the same so that the MIM devices degrade exactly the same and the center point voltage is not affected ; 6) the driving method and pixel configuration are insensitive to small residual asymmetry in the IV characteristics of the MIM devices, which is difficult to eliminate ; and 7) no DC component averaged in time appears on either column or row address lines, so that the passivation layer on address lines can be eliminated or reduced in thickness.

Referring now to Fig. 4, the curve shown therein dramatically illustrates the improved operation of the matrix in accordance with the present invention when the MIM devices 34 and 36 of the pixel 22 of Fig. 1 are biased into a non-conducting condition during the retention of the charge stored within the charge storage element 46. Curve 66 is the current versus voltage characteristic of, for example, MIM devices 34 when line 12 is held at -10 volts and impedance of storage element 46 is assumed to be 0 ohms. As can be noted, when the voltage V_v is more positive than -10 volts on line 23, the current through the diode 34 is represented by only leakage current, which typically is very low (e.g., orders of magnitude lower than the diodes conducting current). Similarly, 66 further illustrates the current versus voltage characteristic of diode 34 when line 12 is held at +10 volts and the impedance of element 46 is assumed to be 0 ohms. When the voltage across element 46 is less positive than the 10 volts on line 12, the current through the diode 36 is also represented by leakage current which is similarly very low. The characteristic is substantially uniform from one MIM device to the next ; As a result,

as long as the voltage across storage element 46 remains between +10 volts and -10 volts (or another suitable voltages) very little current will flow from the charge storage element 46, and thus, the system will efficiently retain the charge stored within the charge storage element 46.

For example, in a high resolution display system having pixels can theoretically be charged in a charging time on the order of 1-2 microseconds, a time much shorter than is obtainable in a conventional transistor active matrix display using a thin film field effect transistor of the usual size as the active matrix element at each pixel.

While the invention has been described with respect to certain preferred exemplification and embodiments thereof, it is not intended to limit the scope of the invention thereby, but solely by the claims appended hereto.

Claims

1. An active matrix liquid crystal display system (10) for rapidly storing and efficiently retaining electric charge in selected ones of a plurality of pixel elements (46), said system comprising :
 - a plurality of substantially parallel address line pairs (12, 12', 14, 14') ;
 - a plurality of substantially parallel additional address lines (18, 20) crossing said address line pairs (12, 12', 14, 14') at an angle and being spaced from said address line pairs to form a plurality of crossover points therewith ;
 - a pair of MIM devices (34, 36) coupled together at a common node (38) and between said address line pairs associated with said crossover points, and MIM device being of the type which block current flow at a low bias, and provide a low impedance to current flow when high biased ;
 - each of said pixel elements (46) being coupled between a respective one of said common nodes (38) and one of said additional address lines (18) ;
 - first means for applying first operating potentials (50) which are substantially equal in magnitude and opposite in polarity between said address line pairs (12, 12', 14, 14') to bias said MIM devices (34, 36) into said low impedance condition to facilitate the storage of charge in the pixel elements (46) coupled thereto ; and
 - second means for applying charging potential (52) to selected ones of said additional address lines (18, 20) for providing electric charge to be stored in said selected storage elements (46) during the application of said first operating potentials to said address line pairs.
2. A system as defined in Claim 1, wherein said MIM devices (34, 36) also provide a high impedance to current flow when high biased, and wherein said first means further includes means for applying second operating potentials which are substantially equal in magnitude and opposite in polarity between said address line pairs to bias said MIM devices into said second condition to facilitate the retention of the charge stored in said storage elements coupled thereto.
3. A system as defined in Claim 1, wherein said MIM devices are multilayered devices which comprise a first layer of a transparent conduction oxide material, a layer of substantially insulating material overlying said substantially insulating layer of material.
4. A system as defined in Claim 3, wherein said first layer is a layer of indium tin oxide ; said layer of substantially insulating material is SiN_x and said layer of metallic material is chromium.
5. A method of operating an active matrix liquid crystal display (10) to rapidly store and efficiently retain electric charge in selected ones of a plurality of pixel elements (46) of the matrix system, said method comprising the steps of :
 - providing, a plurality of substantially parallel address line pairs (12, 12', 14, 14') ;
 - providing a plurality of substantially parallel additional address lines (18, 20) crossing said address line pairs (12, 12', 14, 14') at an angle and being spaced from said address line pairs to form a plurality of crossover points therewith ;
 - coupling a pair of MIM devices (34, 36) together at a common node (38) and in series relation between said address line pairs and associated with said crossover points, said MIM devices being of the type which provide a low impedance to current flow when forward biased into an [first] on condition ;
 - coupling each of said pixel elements (46) between a respective one of said common nodes (38) and one of said additional address line (18) ;
 - applying first operating potentials which are substantially equal in magnitude and opposite in polarity between said address line pairs to bias said threshold devices into said [first] on condition to facilitate the storage of charge in the storage elements coupled thereto ; and
 - applying charging potential to selected ones of said additional address lines during the application of said first operating potentials to said address line pairs to store electric charge in said selected storage elements.

6. A method as defined in Claim 5, wherein said MIM devices (34, 36) are also of the type which provide a high impedance to current flow when reverse biased into an off condition, and wherein said method further includes the step of applying second operating potentials which are substantially equal in magnitude and opposite in polarity between said address line pairs to reverse bias said threshold devices into said [second] off condition to facilitate the retention of the charge stored in said storage elements coupled thereto.
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7. A method as defined in Claim 6, wherein said step of applying said first operating potentials includes commencing the application of said first operating potentials after commencing the application of said charging potentials and terminating the application of said first operating potentials before terminating the application of said charging potentials.
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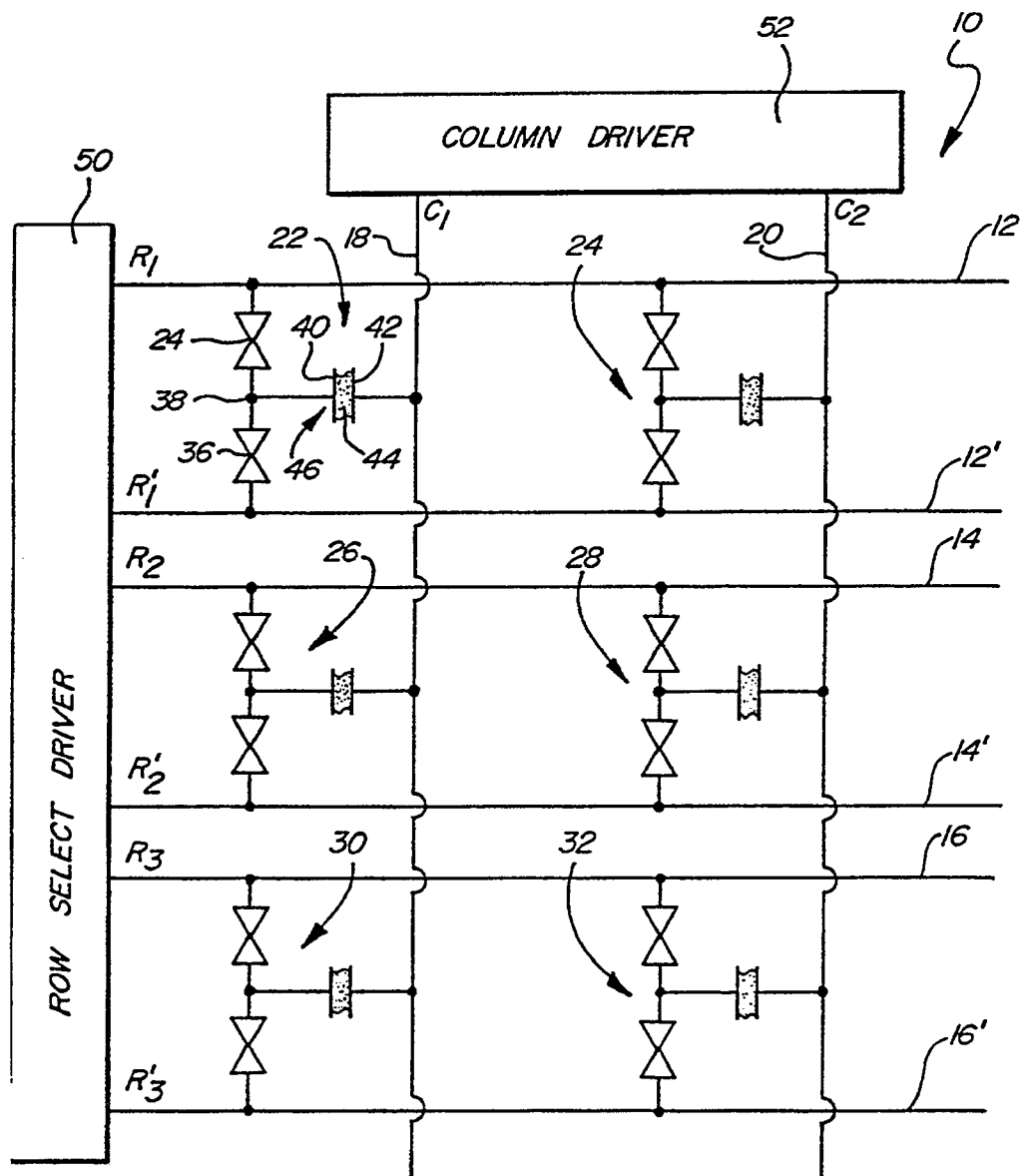


FIG - 1

FIG - 2A

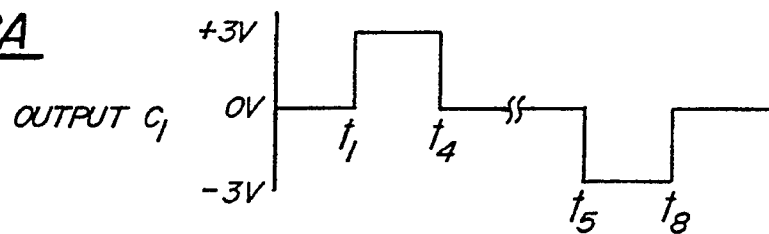


FIG - 2B

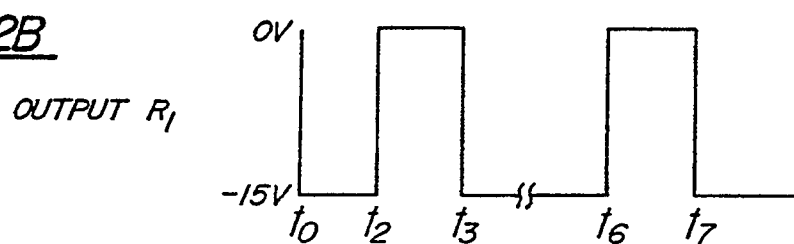


FIG - 2C

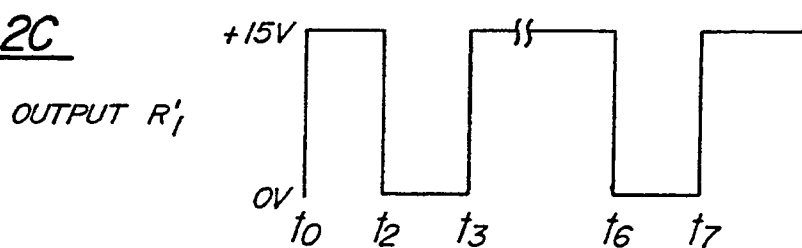


FIG - 4

