PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 :		(11) International Publication Number:	WO 90/12421
H01L 21/335, 27/105, 27/108	A1	(43) International Publication Date:	18 October 1990 (18.10.90)

(21) International Application Number: PCT/US90/00239

(22) International Filing Date: 9 January 1990 (09.01.90)

(30) Priority data:
331,952 3 April 1989 (03.04.89) US

(71) Applicant: GRUMMAN AEROSPACE CORPORATION [US/US]; 1111 Stewart Avenue, Bethpage, NY 11714-3580 (US).

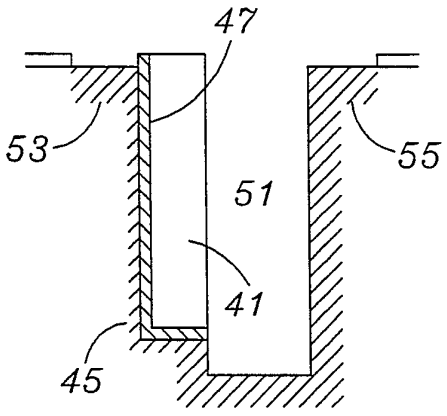
(72) Inventor: SOLOMON, Allen, L. ; 1800 Fairford Drive, Fullerton, CA 92633 (US).

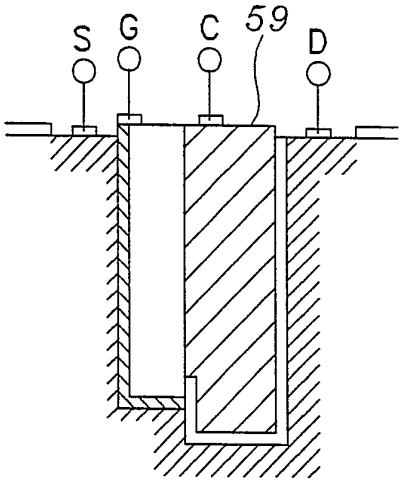
(74) Agents: BRUNDA, Bruce, B. et al.; Stetina and Brunda, 24221 Calle de la Louisa, Ste. 401, Laguna Hills, CA 92653 (US).

(81) Designated States: AT (European patent), BE (European + patent), CH (European patent), DE (European patent), DK (European patent), ES (European patent), FR (European patent), GB (European patent), IT (European patent), JP, KR, LU (European patent), NL (European patent), SE (European patent).

Published
With international search report.
With amended claims and statement.

(54) Title: TRENCH JFET INTEGRATED CIRCUIT ELEMENTS





(57) Abstract

The invention comprises forming a first trench (41) in a semiconductor substrate (20), forming a gate channel (45) about the trench (41) and forming a conductive layer (47) upon the surface of the gate channel (45). The conductive layer (47) interfaces with the gate channel (45) to form a p-n junction. Source and drain regions (53, 55) are formed adjacent to a trench and disposed in electrical contact with the gate channel (45). An integral capacitor may be added to the construction by forming a second trench (51), which extends through and excavates a portion of the first trench (41). The drain region (55) is extended about the surface of the second trench (51) to remain in electrical contact with the gate channel (45). A layer of insulating material (57) is applied to the second trench (51), which is then filled with a body of conductive material (59). The conductive material is insulated from the conductive layer (59) by the insulating layer (57).

+ See back of page

DESIGNATIONS OF "DE"

Until further notice, any designation of "DE" in any international application whose international filing date is prior to October 3, 1990, shall have effect in the territory of the Federal Republic of Germany with the exception of the territory of the former German Democratic Republic.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	ES	Spain	MG	Madagascar
AU	Australia	FI	Finland	ML	Mali
BB	Barbados	FR	France	MR	Mauritania
BE	Belgium	GA	Gabon	MW	Malawi
BF	Burkina Faso	GB	United Kingdom	NL	Netherlands
BG	Bulgaria	HU	Hungary	NO	Norway
BJ	Benin	IT	Italy	RO	Romania
BR	Brazil	JP	Japan	SD	Sudan
CA	Canada	KP	Democratic People's Republic of Korea	SE	Sweden
CF	Central African Republic			SN	Senegal
CG	Congo	KR	Republic of Korea	SU	Soviet Union
CH	Switzerland	LI	Liechtenstein	TD	Chad
CM	Cameroon	LK	Sri Lanka	TG	Togo
DE	Germany, Federal Republic of	LU	Luxembourg	US	United States of America
DK	Denmark	MC	Monaco		

TRENCH JFET INTEGRATED CIRCUIT ELEMENTS

Background of the Invention

The present invention finds application in connection with thin silicon plates or wafers formed to support a multiplicity of monolithically integrated data processor circuits. More particularly, the invention is for the production of junction field effect transistor (JFET) integrated circuit elements formed on silicon wafers and used to interface devices such as infrared detector elements to a processing network that amplifies, stores and interprets detected infrared frequency signals.

The infrared spectrum covers a range of wavelengths longer than the visible wavelengths, but shorter than microwave wavelengths. Visible wavelengths are generally regarded as between 0.4 and 0.75 micrometers. The infrared wavelengths extend from 0.75 micrometers to 1 millimeter. The function of infrared detectors is to respond to the energy of a wavelength within some particular portion of the infrared region.

Heated objects generate radiant energy having characteristic wavelengths within the infrared spectrum. Many current infrared image detection systems incorporate arrays with large numbers of discrete, highly sensitive detector elements, the electrical outputs of which are connected to processing circuitry. By analyzing the pattern and sequence of detector element excitation, the processing circuitry can identify and track sources of infrared radiation. Though the theoretical performance of such contemporary systems is satisfactory for many applications, it is difficult to construct structures that adequately interface large numbers of detector elements with associated circuitry in a practical and reliable manner. Consequently, practical applications for contemporary infrared image detector systems have necessitated further advances in the areas of

miniaturization of the detector array and accompanying circuitry, of minimization of circuit generated noise that results in lower sensitivity of the detected signal, and of improvements in the reliability and economical production of detector arrays and the accompanying circuitry.

Contemporary arrays of detectors, useful for some applications, may be sized to include 256 detector elements on a side, or a total of 65,536 detectors, the size of each square detector being approximately 0.009 centimeters on a side, with 0.00116 centimeters spacing between detectors. Such a subarray would therefore be 2.601 centimeters on a side. Interconnection of such a subarray to processing circuitry would require connecting each of the 65,536 detectors to processing circuitry within a square, a little more than one inch on a side. Each subarray may, in turn, be joined to other subarrays to form an array that connects to 25,000,000 detectors or more. As would be expected considerable difficulties are presented in electrically connecting the detector elements to associated circuitry, and laying out the circuitry in a minimal area. The problems of forming processing circuitry in such a dense environment require minimization of the surface area used for the circuitry.

The outputs of the detector elements typically undergo a series of processing steps in order to permit derivation of the informational content of the detector output signal. The more fundamental processing steps, such as preamplification, tuned band pass filtering, clutter and background rejection, multiplexing and fixed noise pattern suppression, are preferably done at a location adjacent the detector array focal plane. As a consequence of such on-focal plane, or up-front signal processing, reductions in size, power and cost of the main processor may be achieved. Moreover, on-focal plane signal processing helps alleviate performance, reliability

and economic problems associated with the construction of millions of closely spaced conductors connecting each detector element to the signal processing network.

Aside from the aforementioned physical limitations on the size of the detector module, limitations on the performance of contemporary detection systems can arise due to the presence of electronic circuit generated noise, in particular, from the preamplifier. Such noise components can degrade the minimal level of detectivity available from the detector.

A type of noise that is particularly significant where the preamplifier operates at low frequency is commonly called flicker or 1/f noise. Because 1/f noise can be the principal noise component at low frequencies of operation, it is highly desirable that circuits operating within such frequencies be constructed in such a manner as to decrease 1/f noise to an acceptably low level.

U.S. Patent No. 4,633,086, to Parrish, Input Circuit For Infrared Detector, assigned to the common assignee, describes one technique for biasing the on-focal-plane processing circuit to maintain the associated detector in a zero bias condition, thus reducing 1/f noise and enhancing the signal to noise ratio of the circuit.

Reduction of 1/f noise in the preamplifier, where the preamplifier transistor is a field effect device, is conventionally obtained by increasing the area of the channel region under the gate. This large area over the semiconductor substrate surface results in a decrease in circuit component density or decreased circuit component miniaturization. In the present invention, the channel region of a juncttion field effect transistor (JFET) is formed in a trench in the semiconductor. The transistor then occupies far less semiconductor substrate surface and so enables a high component density circuit to be obtained.

In co-pending applications, applicant has disclosed constructions of a trench gate MOS field effect transistor (MOSFET) alone and integrated with a capacitor in a single trench. Such constructions provide large area trench gate regions to obtain low 1/f noise without consuming large amounts of semiconductor surface area. The present invention expands on the disclosure of applicants co-pending applications by modifying the transistor construction to provide additional radiation hardness to the circuit. Conventional construction of a MOSFET utilizes a layer of silicon dioxide separating the gate electrode from the channel semiconductor region. When such a transistor it is irradiated by gamma rays; one result is to establish a residual charge in the silicon dioxide, which provides a constant bias on the transistor channels. This bias typically impedes the operation of the transistor by, for example, keeping the transistor in an on state, or by varying its threshold.

Radiation hardness is provided by a different transistor construction wherein an insulating layer in the gate region is eliminated. The junction field effect transistor (JFET) is characterized by a construction wherein the insulating layer is replaced by a p-n junction which does not accumulate a bias charge on irradiation. Consequently, the JFET construction avoids the need to use materials that would result in storing a residual charge upon irradiation. It further extensively utilizes silicon nitride as a dielectric and insulator in place of silicon dioxide. Since silicon nitride does not accumulate charge from ionizing radiation, it avoids spurious residual charge effects that can otherwise appear at silicon dioxide, silicon interfaces.

Summary of the Invention

A method and construction are disclosed to form a trench gate JFET transistor. The invention comprises forming a first trench in a semiconductor substrate,

forming a gate channel in the trench and forming a conductive layer upon the surface of the gate channel. Source and drain regions are formed adjacent to a trench and disposed in electrical contact with the gate channel. An integral capacitor may be added to the construction by forming a second trench, which extends through and excavates a portion of the first trench. The drain region is extended about the surface of the second trench to remain in electrical contact with the gate channel. A layer of insulating material is applied to the second trench, which is then filled with a body of conductive material. The conductive material is insulated from the conductive layer by the insulating layer.

The present invention may be embodied in the construction of the trench gate JFET transistor alone, or with the construction of an integral capacitor. In either case the construction may be supplemented by the formation of a complementary trench gate JFET in an additional region of doped material isolating the source region, drain region and gate channel from the substrate.

In another embodiment the present invention includes a complementary trench gate JFET that can be connected to the integral JFET-capacitor device to form a circuit wherein a complementary JFET preamplifier is connected in series with a storage capacitor.

In the presently preferred embodiment the substrate is formed of p-type silicon, the gate channel is formed of n-type material formed within the trench by shallow diffusion and a conductive layer is formed of p-type material grown on the gate channel. For the complementary JFET a region of doped material isolating the substrate from the source, drain and gate regions is formed of n+ type material in the preferred embodiment.

Where an integral capacitor is not desired, it may not be necessary to fill the transistor trench. However,

if desired, the trench may be filled with a body of insulating material, such as silicon dioxide.

Brief Description of the Drawings

Figure 1 is a cross sectional view of a contemporary JFET structure;

Figure 2 is a cross sectional view of a trench gate JFET in accordance with the present invention;

Figures 3-10 are cross sectional views illustrating the construction of an integrated trench JFET-capacitor circuit element in accordance with the present invention;

Figures 11-16 are cross sectional views illustrating the construction of a complementary trench JFET integrated circuit element in accordance with the present invention; and

Figure 17 is a schematic representation of a trench JFET-capacitor integrated circuit element in accordance with the present invention.

Figure 18 is a cross sectional view of an integral JFET-capacitor circuit element and a complementary JFET where the transistor drains are connected in series with the capacitor.

Detailed Description of the Presently Preferred Embodiment

The detailed description set forth below in connection with the appended drawings is intended as a description of the presently preferred embodiment of the invention, and is not intended to represent the only form in which the present invention may be constructed or utilized. The description sets forth the functions and sequence of steps for construction of the invention in connection with the illustrated embodiment. It is to be understood, however, that the same or equivalent functions and sequences may be accomplished by different embodiments that are also intended to be encompassed within the spirit and scope of the invention. Furthermore, a similar trench gate embodiment can be used to form complementary MOS field effect transistors as well as the junction field

effect transitors described here.

As previously noted large numbers of closely spaced, high component density integrated circuit processor channels may be used in on-focal-plane signal processors. Each detector element in the detector array may be connected to a preamplifier, such as a CMOS preamplifier, in an analog processor circuit. Low preamplifier noise is essential to prevent degradation of detector sensitivity. Since the preamplifiers are operated at low frequency, a principal source of noise if flicker or 1/f noise. The 1/f noise is inversely proportional to the area of the channel or gate regions of an MOS transistor, as expressed in the following equation:*:

$$\overline{v^2} = \frac{K\Delta f}{C_{OX}WLf,}$$ where

v = the characteristic noise in microvolts;

K = a constant;

Δf = bandwidth

f = the frequency of operation;

C_{ox} = characteristic capacitance of the oxide layer;

W = the width of the gate; and

L = the length of the gate.

*See: R. Gregorian and G.C. Temes, Analog MOS Integrated Circuits In Signal Processing, John Wiley & Sons, N.Y., N.Y. (1986).

A large area gate region in a MOS transistor will produce a low 1/f noise component. However, such a structure requires a large amount of semiconductor surface area. This makes it difficult to obtain a high density of such integrated circuit functions. The present invention is directed to a structure and process for enhancing the area of the gate region without enhancing the semiconductor surface area.

The MOS transistor gate region may be regarded as a capacitor, which is formed by a metal oxide semiconductor

cross section. Large area capacitors that preserve semiconductor surface are obtained in bulk silicon by using the walls of trenches, grooves or holes, which are cut in silicon, for example, by plasma or reactive ion etching. In such a manner, gate region area may be enhanced by using the depth of the trench to enlarge the electrode channel area without the need to use a large amount of the semiconductor surface. The present invention recognizes the capacitive characteristics of the MOS transistor gate region and applies particular trench forming techniques to the construction of the MOS transistor. In such a manner the MOS transistor gate channel area or gate channel region, is enhanced, mitigating 1/f noise, without the need to use large amounts of the semiconductor surface.

Figure 1 illustrates a junction field effect transistor (JFET) constructed in accordance with conventional techniques. As shown therein n-JFET 11 is formed of an n-doped source region 21 and an n-doped drain region 23 formed in p-doped silicon 20. The channel between source and drain is the shallow n-type region 25. The gate junction is formed by the p-type layer 27 over region 35.

In relation to Figure 1 the characteristic 1/f noise is related to the width and length of the gate area intermediate to the source and drain. The length of the gate area, labeled L, is shown at Figure 1. The width of the gate area is orthogonal to the plane of the drawing. By increasing the length of the gate L, 1/f noise is reduced, though the maximum speed at which the circuit will efficiently operate is reduced. The present invention is directed to a construction and technique wherein the gate area is enhanced without the need to appropriate greater surface area of the semiconductor wafer.

Figure 2 illustrates one embodiment of the present invention. As with the JFET 11 shown at Figure 1, JFET 13 comprises an n-doped source region 21, and an n-doped drain region 23, both formed in p-doped silicon 20. Unlike the construction shown at Figure 1, a trench 31 is formed in the silicon substrate. The trench may be formed by any of a variety of techniques, such as reactive ion etching. A shallow n-type layer 33 is formed by dopant diffusion in the vertical and bottom silicon surfaces of trench 31. The gate junction can be formed by growing a p-type epitaxial layer of silicon 35 over layer 33. It may be necessary to apply a supporting conductive layer, such as metal or degenerately doped polycrystalline silicon, over layer 35 to provide sufficiently high gate electrode conductivity. In an alternative structure the trench can be filled with an insulator material such as silicon nitride or silicon dioxide or with a conductive material without the need for a supporting conductive film. Electrodes 37, 39 may be formed on the upper exposed surfaces of source 21 and drain 23, respectively. An additional electrode (not shown) may be formed to facilitate contact with the gate layer 35.

In accordance with the construction shown at Figure 2 the gate region intermediate to the source 21 and drain 23 is enlarged by means of a formation of trench 31. In the presently preferred embodiment trench 31 is formed to be up to approximately 10 to 20 microns deep and 2 to 3 microns wide. The width of the trench (orthogonal to the plane of Figure 2) is in the range of 10 to 20 microns. The particular dimensions may be selected in accordance with the desired noise characteristics and speed of the transistor, and the available surface area.

The construction illustrated at Figure 2 provides the advantages of low 1/f noise without the penalty in terms of semiconductor surface area. Unlike a MOSFET with a silicon dioxide gate insulator layer, there is virtually

no residual bias charge accumulation in the p-n junction gate of the JFET caused by irradiation by a source of gamma rays. In addition, the present invention provides for integration of a capacitor in series with the transistor drain, as schematically represented at Figure 17.

Two construction sequences are illustrated and described below. The first, illustrated at Figures 3-10 results in the construction of a trench gate n-JFET integrated circuit element, which may optionally incorporate a series capacitor. The second technique, illustrated at Figures 11-16, results in the construction of a complimentary p-JFET integrated circuit.

The construction of the n-JFET, and integrated series capacitor, proceeds as follows. First, a trench 31 is formed in the silicon dioxide or nitride 43 coated substrate 20. Contemporary techniques such as reactive ion etching may be used to form the trench. The depth of the trench may vary in accordance with the desired operating characteristics of the circuit. It is presently anticipated that the trench 31 could extend up to approximately 20 microns. The substrate may be p-type bulk silicon.

As illustrated in Figure 4 an n-type region 45 is then formed at the surface of trench 41. The region 45 may be formed by shallow diffusion. The n-type region 45 forms a transistor channel as described more fully below.

As shown in Figure 5 a p-type epitaxial layer 47 is then grown on the n-type region 45 to form the gate junction characteristic of a JFET. The p-type layer 47 is preferably doped to assure operation at low temperature. It is anticipated that in some applications it may be desirable to form an additional conductive layer, such as a metal film, above p-type layer 47 to insure sufficient gate electrode conductivity in such low temperature applications.

As shown at Figure 6, trench 41 is then substantially filled with a body of insulating material 49, such as silicon dioxide. It should be noted that the use of silicon dioxide as such insulating material to form body 49 will not result in the undesirable residual gate bias conditions described above.

Beginning with Figure 7 a construction is illustrated wherein a capacitor is integrated into the construction of the trench gate JFET. It is to be understood, however, that the present invention finds application without the construction of an integral series capacitor. In the embodiments illustrated the construction steps are sequenced for the most convenient formation of an integral JFET-capacitor circuit. However, as will be recognized by those of ordinary skill in the art, certain of the steps may be excluded or modified in sequence in the event that an integral capacitor circuit is not desired.

As shown in Figure 7 a second trench 51 is then formed in the substrate 20. In the illustrated embodiment the second trench 51 extends through and excavates a portion of trench 41. However, the depth of both trenches may be varied in accordance with the desired characteristics of the JFET and the series capacitor. The trench 51 provides space for the formation of a film capacitor disposed in series with the JFET.

As shown in Figure 8 the construction further proceeds by the removal of segments of the insulating layer 43 and the formation of drain and source regions 53, 55, respectively. Source region 53 and drain region 55 are preferrably formed by diffusion to form n+ type regions. The regions 53 and 55 extend to layer 47. The n+ type regions 53 and 55 are heavily doped in relation to n-type region 45. The channel region 45 is constructed to be thin and less heavily doped than the source and drain regions 53 and 55 to enable charge carriers to be depleted and so to reduce current flow in the channel when

a small signal is applied to gate layer 47.

Figure 9 illustrates the formation of the capacitor dielectric 57. The dielectric 57 may be formed by thermal oxidation of the exposed surface trench 51. The oxidation of the surface of trench 51 produces an insulating layer of silicon dioxide, which comprises the dielectric 57. The dielectric 57 can also be made by vapor depositing a film of either silicon dioxide or silicon nitride. Chemical vapor deposition, of either materials is well practiced process.

Figure 10 illustrates the formation of the capacitor electrode 59. The electrode 59 may be formed by filling the trench 51 with a body of conductive material, such as metal or degenerately doped polycrystalline silicon. Metal film contact pad and lead may be formed on the surface of the wafer (not shown) to facilitate communication of signals to and from the circuit. Figure 17 schematically illustrates the physical circuit depicted at Figure 10, and includes corresponding source, gate, drain and capacitor output terminals.

Figures 11-16 illustrate the fabrication of a complementary trench p-JFET transistor in a p-type silicon wafer. The construction technique differs from that described in connection with Figures 3-10 in that the source and drain regions are p-type material and a gate n-p junction, as opposed to the previously described p-n junction, is isolated from the p-type silicon substrate by an n+ type region diffused into the substrate. Additionally, the construction illustrated at Figures 11-16 does not incorporate an integral series capacitor. However, it is to be understood that the construction of the complementary p-JFET transistor may be supplemented to incorporate an integral capacitor in accordance with the same construction steps illustrated in connection with Figures 7-10.

Referring to Figure 11 a trench 61 is formed in

insulator coated substrate 20. The substrate 20 in this embodiment is a p-type bulk silicon substrate. The trench 20 may be formed, for example, by reactive ion etching of the substrate. An insulating layer 63 is formed on the upper surface of the substrate. The insulating layer may commonly be silicon dioxide or silicon nitride. As shown in Figure 12 a deep n+ region is then formed, by diffusion, within the substrate 20 about trench 61. The n+ region 65 serves to isolate the n-p gate junction, as well as the source and drain regions from the bulk silicon.

Figures 13 and 14 illustrate the construction of the gate n-p junction. First, a thin, lightly doped p-type epitaxial layer 67 is grown in the trench to form the gate channel. An n-type epitaxial layer 69 is then grown on the p-type layer 67 to form the gate junction. It should be understood that it may also be necessary to form an additional conductive layer, such as a metal film, upon n-type layer 69.

Figure 15 illustrates filling trench 61 with a body of material 71. In the presently preferred embodiment the body of material 71 is either silicon dioxide or silicon nitride which has been vapor deposited within trench 61. Should an integral series capacitor be added to the circuit, as illustrated in connection with Figures 7-10, an additional trench may be formed in the substrate. However, both the n-JFET illustrated at Figure 6 and the p-JFET illustrated at Figure 16 have application independent of the inclusion of a series capacitor.

Because the construction illustrated Figures 15 and 16 does not include an integral series capacitor, it should be understood that the body of material 71 may be conductive material instead of insulating material. Similarly, the body of material 49 (Figure 6) may also be a conductive material where the capacitor is not formed integral with the n-JFET.

Figure 16 illustrates the formation of source region 73 and drain region 75. In practice, the source and drain regions are formed by removing a portion of the insulating layer 63 and diffusing p+ type material into the substrate 20 within the n+ region 65. The source and drain regions are isolated from the substrate 20 by the n+ region 65. Consequently, the diffusion of n+ region 65 must be sufficiently deep to facilitate such isolation.

Figure 16 illustrates the types of materials applied to form the p-JFET, as well as the location of source, gate and drain terminals. It is to be understood that the gate terminal may be relocated anywhere along layer 69, or upon the surface of body 71, where body 71 is formed of conductive material.

Figure 18 illustrates the connection of the integral n-JFET-capacitor and the p-JFET to form a circuit where the output of a complementary JFET circuit element is stored in the capacitor. It should be noted that the gate region of the n-JFET and the p-JFET may be sized to be substantially the same area.

As described above it is to be understood that various modifications in the construction and fabrication processes described above may be implemented without departing from the broader aspects of the invention.

CLAIMS

What is claimed is:

1. A method of forming a trench gate JFET comprising:

forming a first trench in a semiconductor substrate;

forming a gate channel region about the first trench;

forming a conductive layer within the first trench upon the surface of said gate channel, said conductive layer interfacing with said gate channel region to form a p-n junction; and

forming source and drain regions within said substrate adjacent to said first trench, said gate and source regions being in contact with said gate channel region.

2. The process as recited in Claim 1 further comprising forming a first region of doped material within said substrate prior to forming said gate channel, said first region of doped material being of a type material opposite to that of the substrate, said first region being diffused into the substrate to a depth sufficient to isolate the source region, drain region and gate channel from the substrate.

3. The process as recited in Claim 1 wherein said substrate is formed of p-type silicon.

4. The process as recited in Claim 2 wherein said first doped region is formed of n+ type material.

5. The process as recited in Claim 1 wherein said gate channel region is formed of n-type material formed within the first trench by shallow diffusion.

6. The process as recited in Claim 1 wherein said conductive layer is formed of a p-type material formed over the gate channel region.

7. The process as recited in Claim 1 further comprising forming a body of material within the first trench upon said conductive layer.

8. The process as recited in Claim 7 wherein said body of material is formed of insulating material.

9. A process of forming an integral trench gate JFET transistor-capacitor comprising:

forming a first trench in a semiconductor substrate;

forming a gate channel about the first trench;

forming a conductive layer within the first trench upon said gate channel;

forming a second trench within the substrate, said second trench extending through and excavating a portion of said first trench;

forming source and drain regions within said substrate adjacent to said first and second trenches respectively, said source and drain regions being in contact with said gate channel;

forming a layer of insulating material within said second trench; and

filling said second trench with a body of conductive material, said body of conductive material being insulated from said conductive layer by said insulating layer;

wherein an output taken from the body of conductive material is representative of a capacitor in series with the drain region.

10. The process as recited in Claim 9 wherein said step of forming said source and drain regions comprises forming a drain region extending about a substantial portion of said second trench.

11. A trench gate JFET comprising:

a first trench formed in a semiconductor substrate;

a gate channel formed about the first trench;

a conductive layer formed within the first trench upon said gate channel; and

source and drain regions formed upon the semiconductor substrate surface adjacent opposite sides of said first trench.

12. A trench gate JFET as recited in Claim 10 further comprising a first region of doped material formed within the substrate about said source drain and gate channel, said first region of doped material being formed of a type material opposite to that of the substrate, said first region of doped material being of sufficient thickness to isolate the source region, drain region and gate channel from the substrate.

13. The trench gate JFET as recited in Claim 11 wherein said substrate is formed p-type silicon and said first doped region is formed on n+type material and the gate channel is formed of of n-type material.

14. The trench gate JFET as recited in Claim 10 further comprising a body of insulating material formed within said first trench upon said conductive layer.

15. An integral trench gate JFET transistor/capacitor comprising:

a first trench formed in a semiconductor substrate;

a gate channel formed about the first trench;

a conductive layer formed about the first trench upon said gate channel;

a second trench formed within the substrate, said second trench extending through and excavating a portion of said first trench;

a layer of insulating material formed about a substantial portion of said second trench;

a body of conductive material disposed within said second trench, said body of conductive material being isolated from said conductive layer by said insulating layer;

source and drain regions within said semiconductor substrate adjacent said first and second trenches, respectively, said source and drain regions each being in contact with said gate channel; and

wherein an output taken from the body of conductive material is representative of a capacitor in series with the transistor drain region.

16. An integral trench gate JFET transistor-capacitor as recited in Claim 15 wherein said drain region extends about said second trench from the substrate upper surface to the gate channel.

17. A method of forming a complementary JFET circuit including an integral and JFET-capacitor and a p-JFET, the method comprising:

forming a first trench in a semi-conductor substrate;

forming a first gate channel about the first trench;

forming a first conductive layer within the first trench upon said first gate channel;

forming a second trench within the substrate, said second trench extending through and excavating a portion of said first trench;

forming first source and drain regions within said substrate adjacent to said first and second trenches respectively, said first source and drain regions being in contact with said first gate channel;

forming a first layer of insulating material within said second trench;

filling said second trench with a first body of conductive material, said first body of conductive material being insulated from said conductive layer by said insulating layer;

wherein an output taken from said first body of conductive material is representative of a capacitor in series with the first drain region;

forming a third trench in the semi-conductor substrate;

forming a second gate channel within said third trench;

forming a second conductive layer within said third trench upon the surface of said second gate channel, said second conductive layer interfacing with said second gate channel region to form a p-n junction;

forming second source and drain regions within said substrate adjacent to said third trench, said second gate and source regions being in contact with said second channel region;

connecting said first and second drain regions; and

connecting said first and second gate regions.

AMENDED CLAIMS

[received by the International Bureau on 03 August 1990 (03.08.90); original claims 1,5 amended; new claims 18-23 added; other claims unchanged (4 pages)]

1. A method of forming a trench gate JFET comprising:

forming a first trench in a semiconductor substrate of a first type;

forming a region of a semiconductor material of a second type about the first trench;

forming a layer of semicondcutor material of the first type within the first trench upon the surface of said semiconductor material of the second type, said layer of semiconductor material of the first type interfacing with said region of semiconductor material of the second type to form a p-n junction; and

forming source and drain regions within said substrate adjacent to said first trench, said gate and source regions being in contact with said region of semiconductor material of a second type.

2. The process as recited in Claim 1 further comprising forming a first region of doped material within said substrate prior to forming said gate channel, said first region of doped material being of a type material opposite to that of the substrate, said first region being diffused into the substrate to a depth sufficient to isolate the source region, drain region and gate channel from the substrate.

3. The process as recited in Claim 1 wherein said substrate is formed of p-type silicon.

4. The process as recited in Claim 2 wherein said first doped region is formed of n+ type material.

5. The process as recited in Claim 1 wherein said region of semiconductor material of a second type is formed of n-type material formed within the first trench by shallow diffusion.

6. The process as recited in Claim 1 wherein said conductive layer is formed of a p-type material formed over the gate channel region.

wherein an output taken from said first body of conductive material is representative of a capacitor in series with the first drain region;

forming a third trench in the semi-conductor substrate;

forming a second gate channel within said third trench;

forming a second conductive layer within said third trench upon the surface of said second gate channel, said second conductive layer interfacing with said second gate channel region to form a p-n junction;

forming second source and drain regions within said substrate adjacent to said third trench, said second gate and source regions being in contact with said second channel region;

connecting said first and second drain regions; and

connecting said first and second gate regions.

18. The process as recited in Claim 1 further comprising the steps of:

forming a second trench within the substrate, said second trench extending through and excavating a portion of said first trench;

forming a layer of insulating material within said second trench;

filling said second trench with a body of conductive material, said body of conductive material being insulated from said layer of semiconductor material of the first type by said insulating layer;

said source and drain regions being formed within said substrate adjacent to said first and second trenches respectively;

wherein an output taken from the body of conductive material is representative of a capacitor in series with the drain region.

19. The process as recited in Claim 18 wherein said step of forming said source and drain regions comprises forming a drain region extending about a substantial portion of said second trench.

20. A method of forming a trench gate JFET comprising:

providing a substrate of a semiconductor material of a first type;

forming a region of semiconductor material of a second type within said substrate;

forming a first trench in said substrate, such that said trench is within said region of semiconductor material of a second type;

forming a region of semiconductor material of a first type about the first trench;

forming a layer of semiconductor material of a second type within the first trench upon the surface of said semiconductor material of the first type, said layer of semiconductor material of the second type interfacing with said region of semiconductor material of a first type to form a p-n junction; and

forming source and drain regions within said substrate adjacent to said first trench, said gate and source regions being in contact with said region of semiconductor material of the first type.

21. The process as recited in Claim 20 wherein said region of semiconductor material of a second type formed within said substrate is formed of n-type material.

22. The process as recited in Claim 21 further comprising the steps of:

forming a second trench within the substrate, said second trench extending through and excavating a portion of said first trench;

forming a layer of insulating material within said second trench;

filling said second trench with a body of conductive

material, said body of conductive material being insulated from said layer of semicondcuctor material of the second type by said insulating layer;

said source and drain regions being formed within said substrate adjacent to said first and second trenches respectively;

wherein an output taken from the body of conductive material is representative of a capacitor in series with the drain region.

23. The process as recited in Claim 22 wherein said step of forming said source and drain regions comprises forming a drain region extending about a substantial portion of said second trench.

STATEMENT UNDER ARTICLE 19

The Examiner's International Search Report of May 7, 1990 indicated that U.S. Patent Nos. 3,953,879 (O'Connor-d'Arlach et al.), 4,633,281 (Benjamin et al.) and 4,455,740 (Iwai), Japanese Patent Nos. 63 0128769 (Victor Company of Japan LTD), and 1 0086561 (NEC Corp) are particularly relevant to the invention. However, after reviewing these references, it is clear that they neither anticipate nor render obvious the subject matter of the claimed invention.

The step of "forming a region of semiconductor material of a second type about the first trench" provides the JFET of the present invention with an extra layer of semiconductor material which acts as one element of the device rather than using the substrate itself as that element. The use of a discrete separate layer instead of the substrate itself has four separate advantages. First it makes the pinch off or depletion of charge carriers in the layer take place more completely and more readily with a lower gate voltage. This occurs because the field effect phenomena now occurs through a much thinner region (the region of semiconductor material of a second type) than is the case where the substrate is used as a device element.

Secondly, a closer construction of adjacent devices is facilitated by the electrical isolation provided by the "region of semiconductor material of a second type" formed about the first trench. The additional layer thus electrically isolates adjacent transistors and thereby permits increased device density.

Thirdly, the extra layer facilitates the contruction of an integral capacitor by functioning as one electrode of the capacitor and thereby eliminating the requirement that a portion of the substrate so function. Thus, the capacitor is effectively isolated from the substrate.

Fourthly, by fabricating the "layer of semiconductor material of a second type" over an extended area, a complimentary JFET can be easily formed within that area in close proximity to the first JFET since such an extra layer is required for the construction of a complimentary device.

It is respectfully submitted that none of the cited prior art patents, either alone or in combination with one another, disclose or make obvious such inventive structure and/or methodology. These facts will become apparent upon reference to the cited prior art patents.

By this Amendment, all of the pending method claims of the subject application have been amended to define the novel and unobvious aspects of the method of forming a trench gate JFET of the present invention. It is respectfully submitted that as amended all of the pending claims are in a condition for allowance.

The Commissioner is hereby authorized to charge any additional fees which may be required by this paper and during the entire pendency of this application to Deposit Account No. 19-4330.

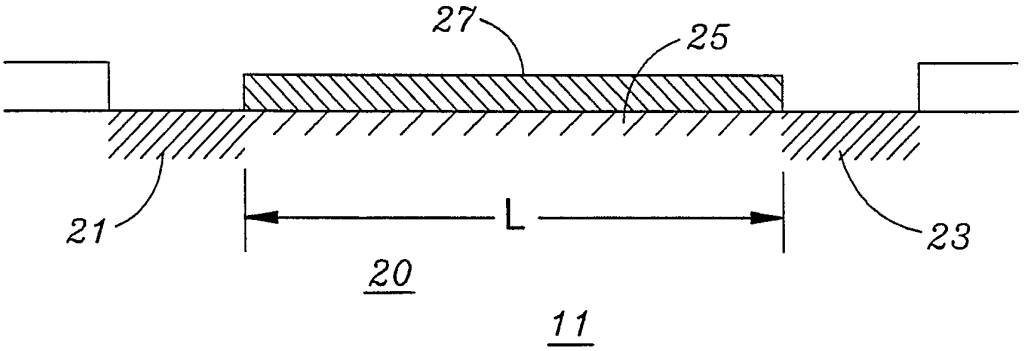


FIG. 1

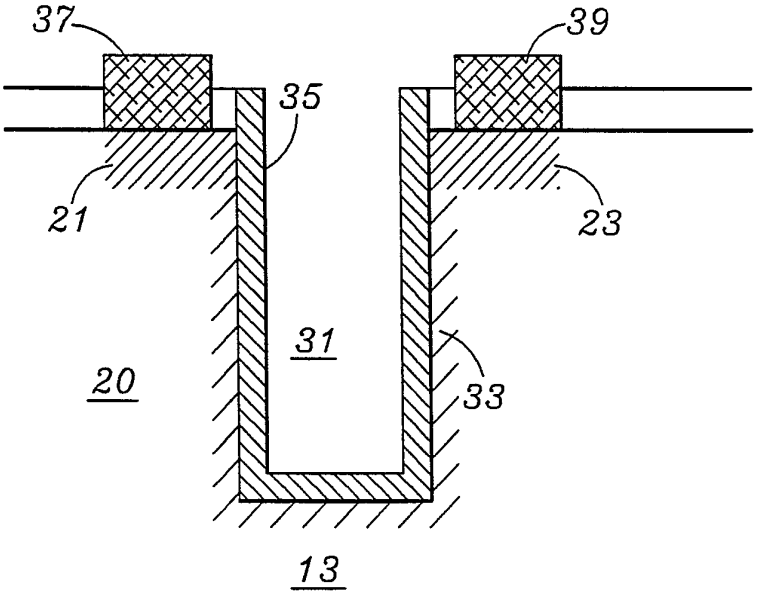


FIG. 2

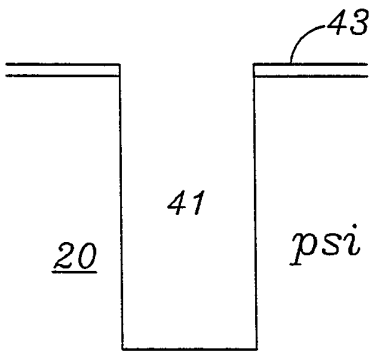


FIG. 3

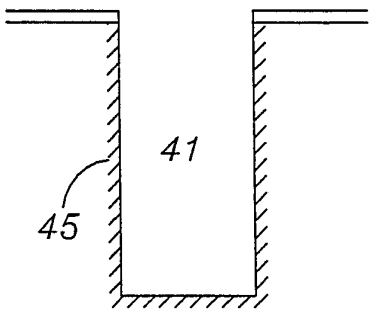


FIG. 4

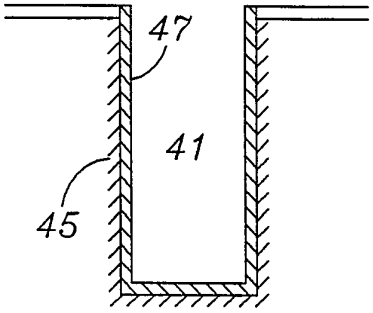


FIG. 5

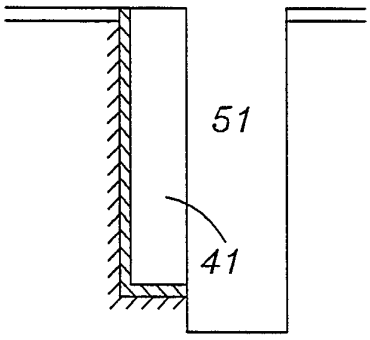


FIG. 7

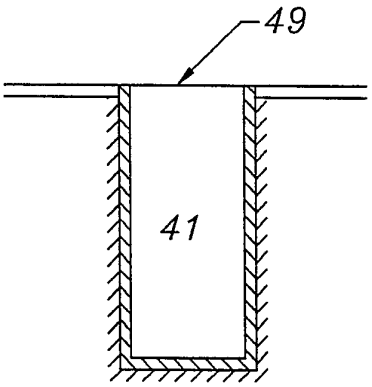


FIG. 6

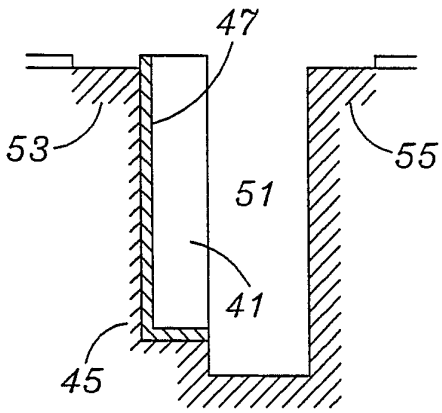


FIG. 8

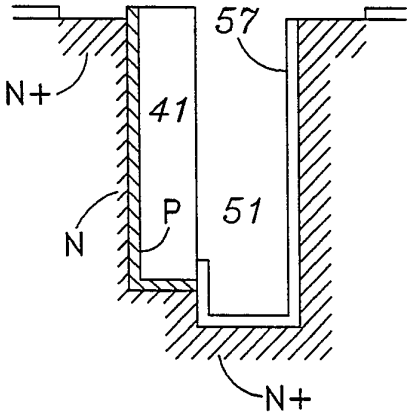


FIG. 9

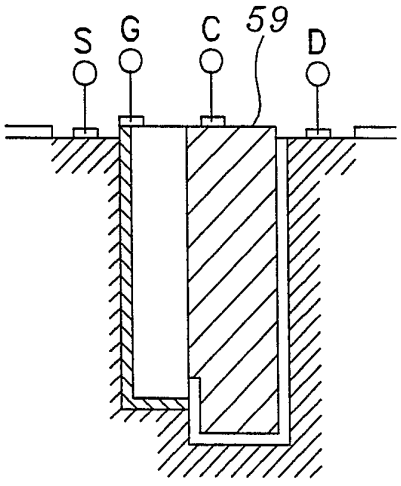


FIG. 10

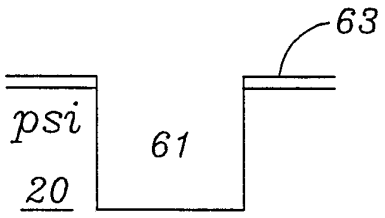


FIG. 11

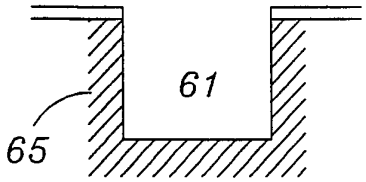


FIG. 12

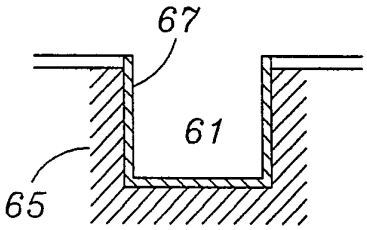


FIG. 13

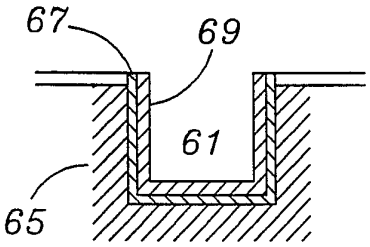


FIG. 14

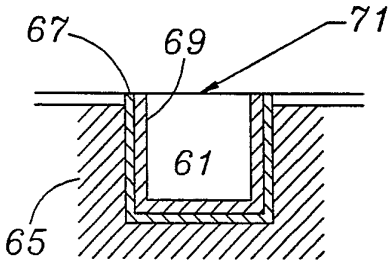


FIG. 15

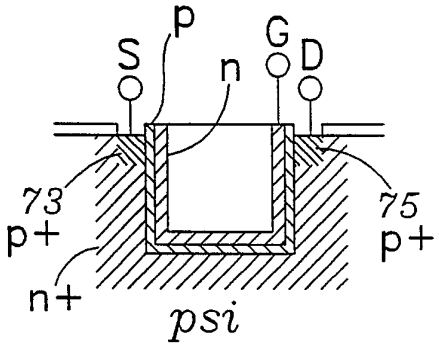


FIG. 16

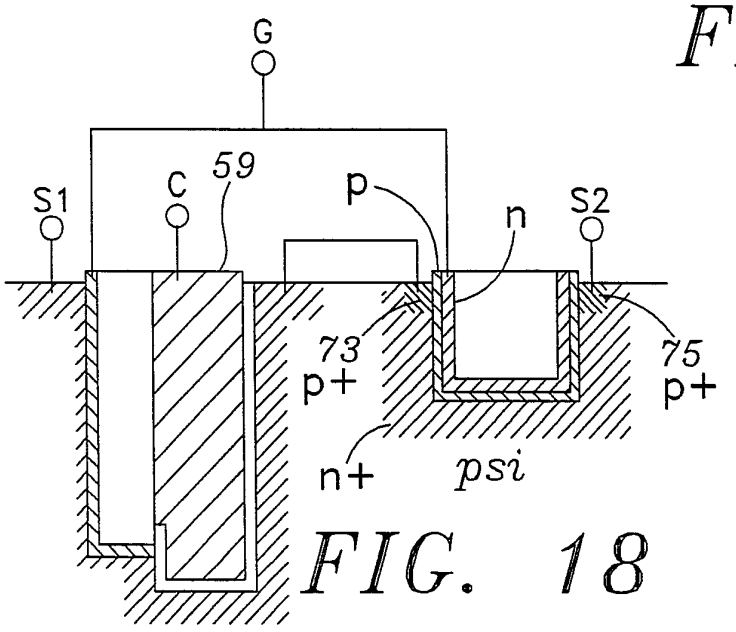


FIG. 18

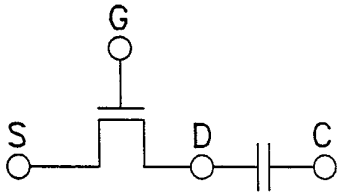


FIG. 17

INTERNATIONAL SEARCH REPORT

International Application No. PCT/US90/00239

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) 6

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC (5) : H01L 21/335, 27/105, 27/108
US Cl : 437/29, 437/47, 357/22, 357/51

II. FIELDS SEARCHED

Minimum Documentation Searched 7

Classification System	Classification Symbols
US	437/29,38,47,51,52,60,228,203 357/22,23.4,23.6,51

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched 8

III. DOCUMENTS CONSIDERED TO BE RELEVANT 9

Category *	Citation of Document, 11 with indication, where appropriate, of the relevant passages 12	Relevant to Claim No. 13
Y	US,A 3,953,879 (O'Connor-d'Arlach ET AL) 27 April 1976 See the entire document	1-17
Y	US,A 4,633,281 (Benjamin ET AL) 30 December 1986 See the entire document	1-17
Y	JP,A 63 0128769 (Victor Company of Japan LTD) 01 June 1986 See abstract and figures	9-16
Y	JP,A 1 00865G1 (NEC CORP) 31 March 1989 See abstract and figures	1-17
A	US,A 4,049,476 (HORIE) 20 September 1977 See the entire document	1-17
A	US,A 4,754,310 (Coe) 28 June 1988 See the entire document	1-17
A	US,A 4,774,556 (Fujii ET AL) 27 September 1988 See the entire document	1-17
Y	US,A 4,555,740 (Iwai) 26 June 1984 See the entire document	1-8

* Special categories of cited documents: 10

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
27 March 1990	19 APR 1990
International Searching Authority	**Signature of Authorized Officer**
ISA/US	T. Thomas Tom Thomas