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Myren

[11] **3,800,234**

[45] **Mar. 26, 1974**

[54] **METHOD FOR IDENTIFICATION OF DIFFERENT TIME INTERVALS BETWEEN PULSES IN AN ELECTRICAL PULSE TRAIN AND A DEVICE FOR PERFORMING THE METHOD**

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Related U.S. Application Data

[63] Continuation of Ser. No. 819,202, April 25, 1969, abandoned.

[52] **U.S. Cl.** **328/112,** 307/227, 307/234, 307/246, 328/186

[51] **Int. Cl.** **H03k 5/20**

[58] **Field of Search** 307/234, 232, 246, 227; 328/109–112, 186

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[57] **ABSTRACT**

A method and circuit for detecting two different time intervals between consecutive pulses of a pulse train includes a first counter to provide a count value which represents the elapsed time between two consecutive pulses in the pulse train, this value then being transferred to a second counter which counts backward a predetermined amount such that if the second counter reaches the value zero, a first time interval is indicated, and if the second counter does not reach zero during the said predetermined amount, a second time interval is indicated.

5 Claims, 5 Drawing Figures

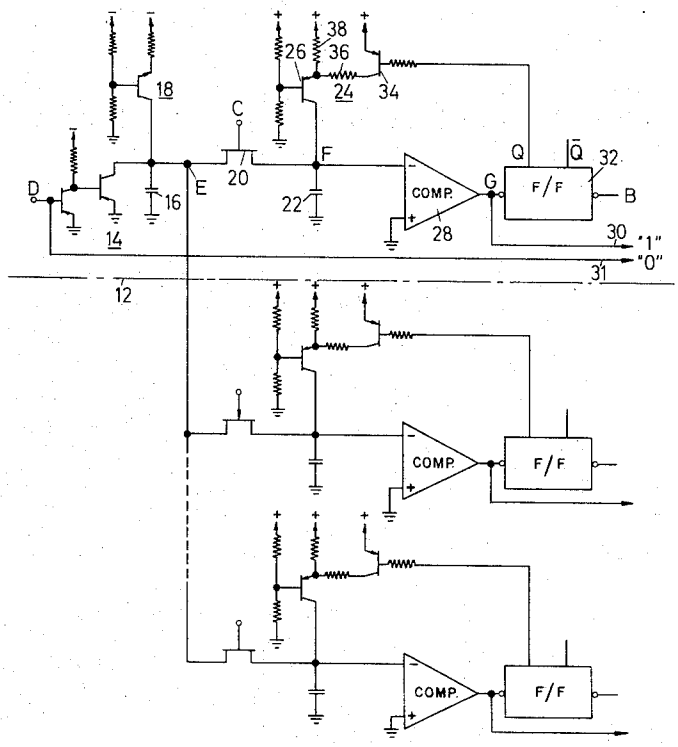

FIG. 1

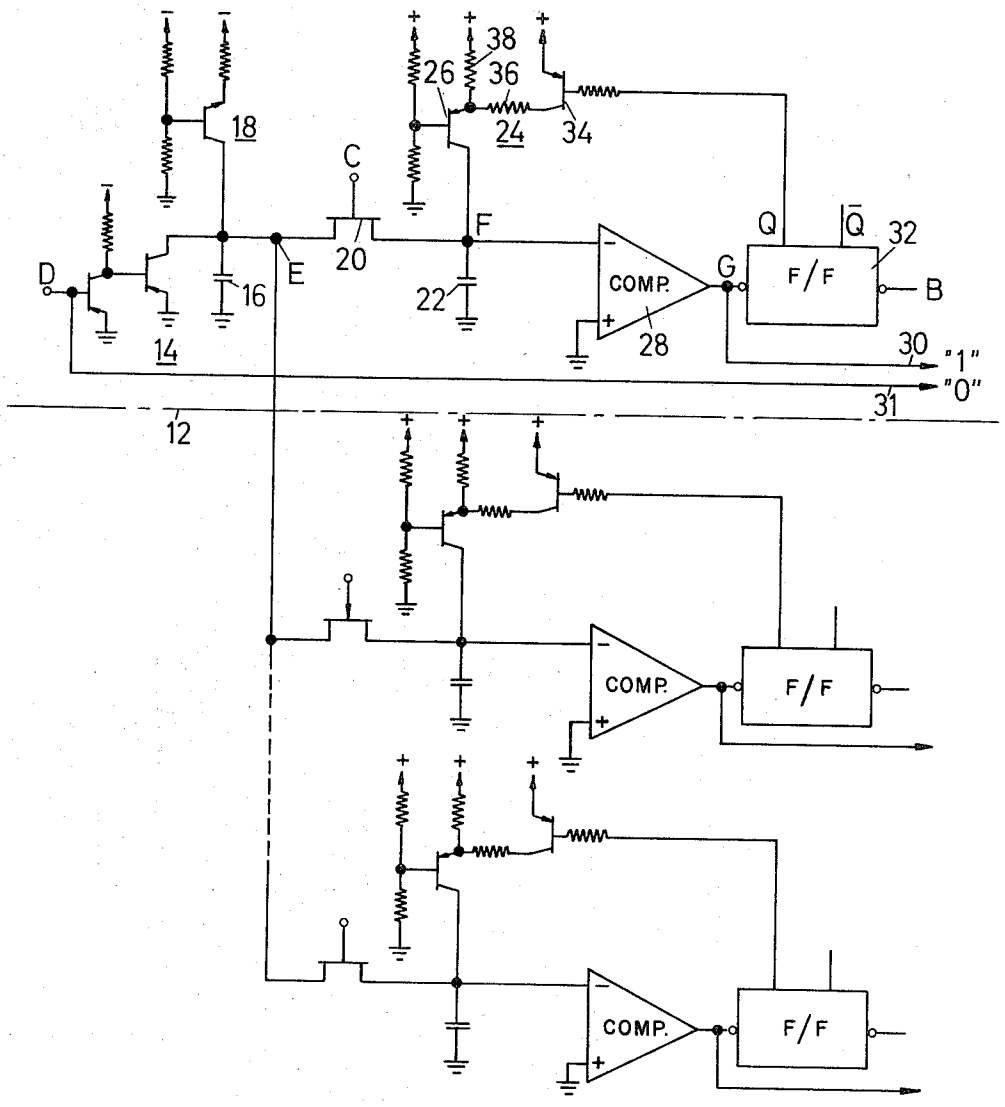

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FIG. 2

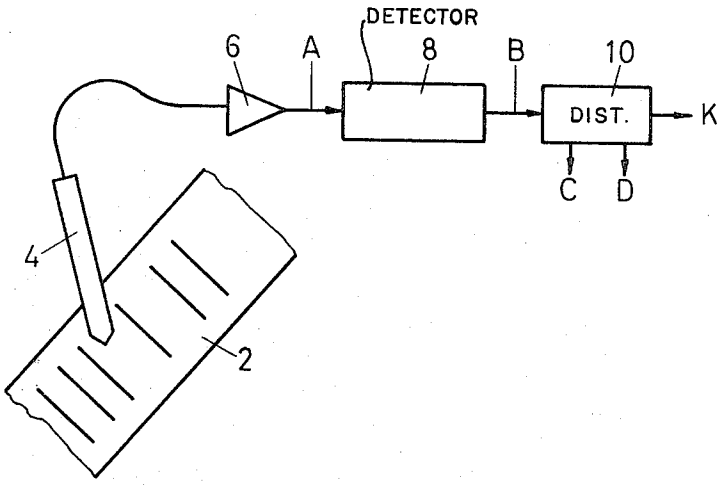

FIG. 3

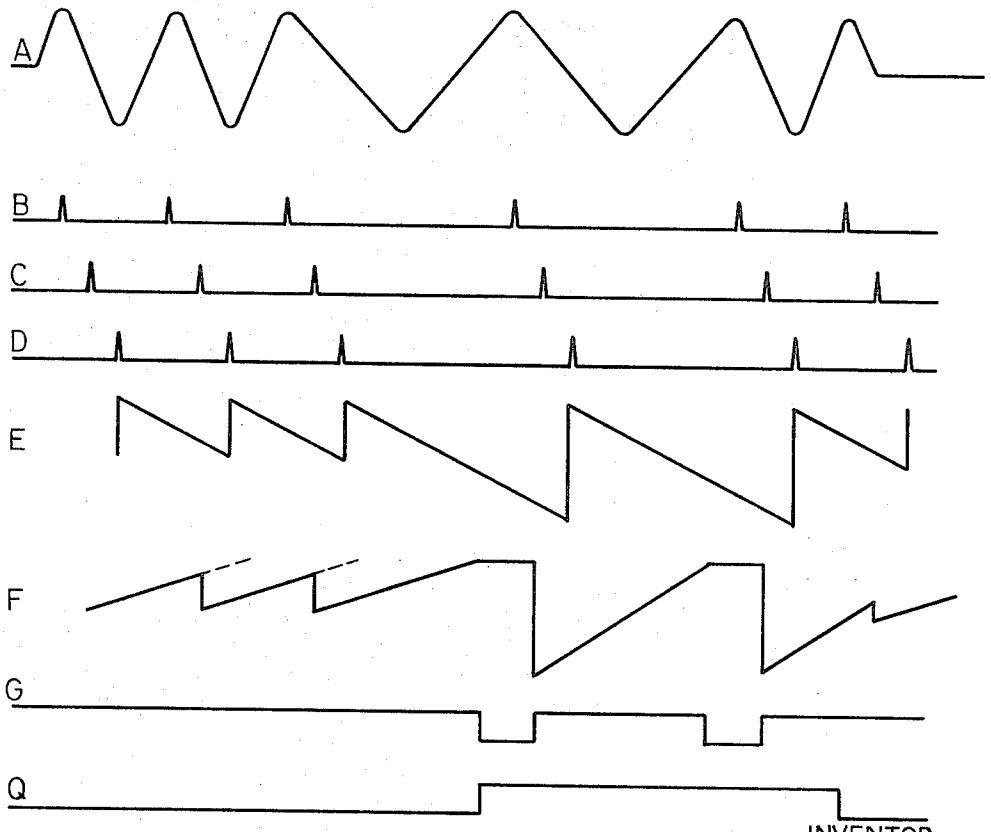

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FIG. 4

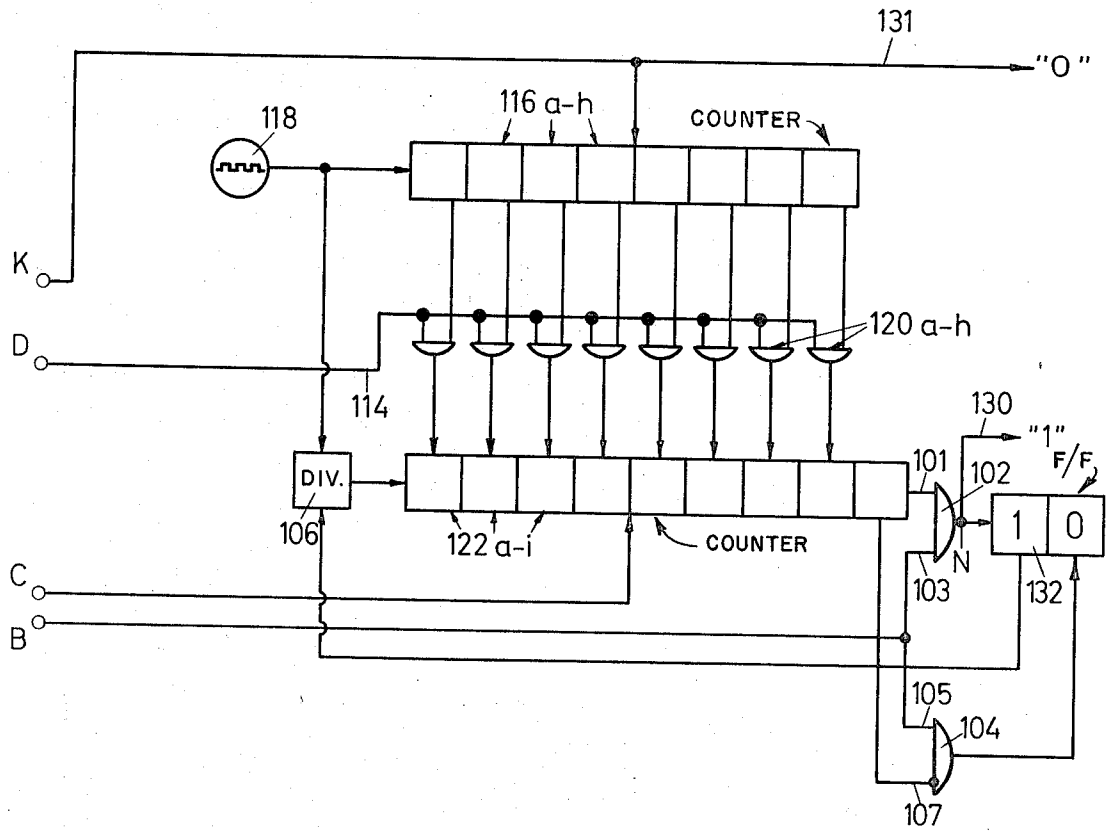

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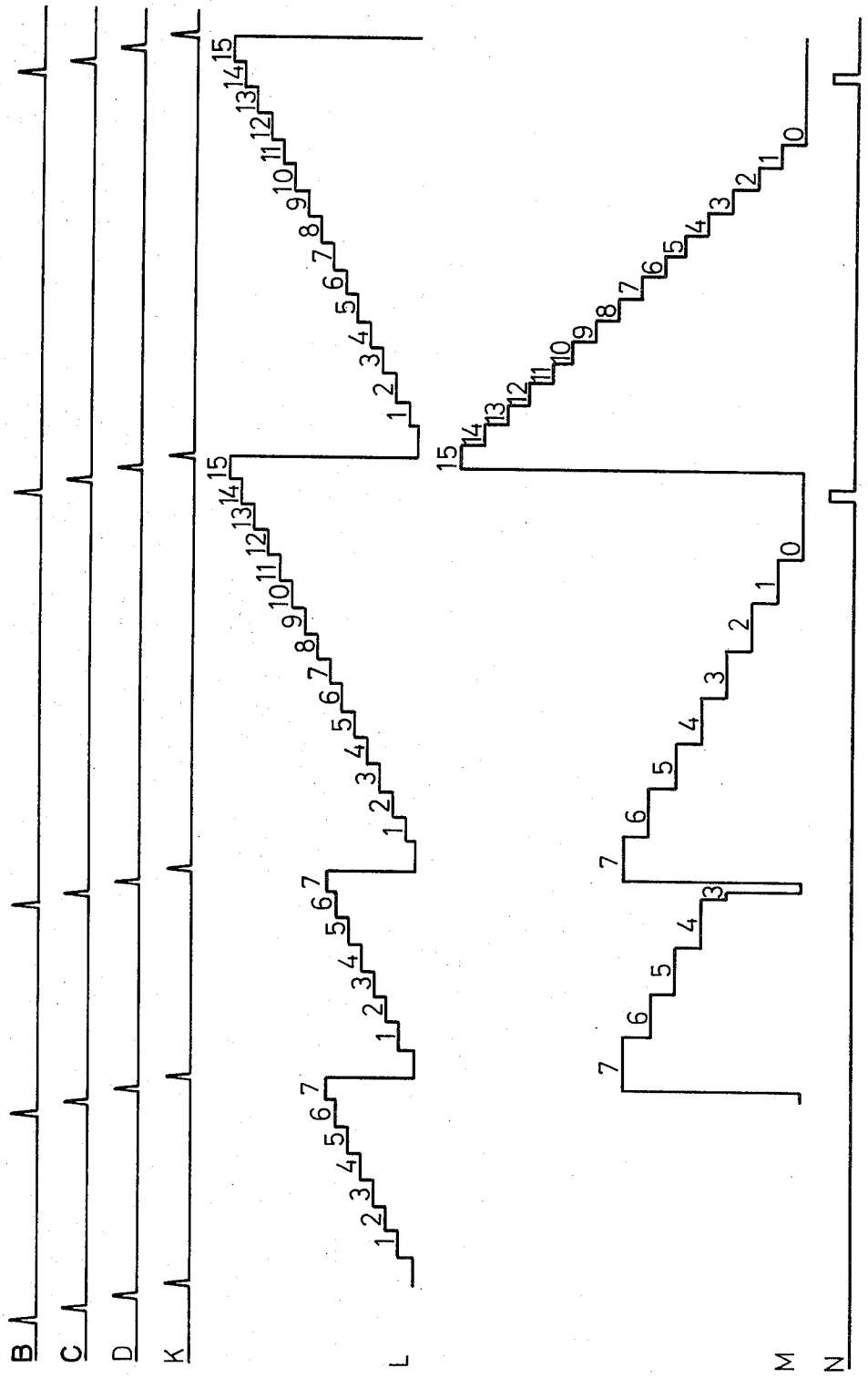
FIG. 5



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METHOD FOR IDENTIFICATION OF DIFFERENT TIME INTERVALS BETWEEN PULSES IN AN ELECTRICAL PULSE TRAIN AND A DEVICE FOR PERFORMING THE METHOD

This is a continuation of application Ser. No. 819,202 filed on Apr. 25, 1969, now abandoned.

The present invention refers to a method for identification of a number of different time intervals between consecutive pulses of an electrical pulse train. The invention also refers to a device for performing the method.

When identifying information in the form of pulses in a pulse train originating from marks arranged on a label or the like, e.g. in the form of black strokes separated by light portions, it is desired that the information packing density be as great as possible. Heretofore, a binary representation of the digits 0–9 has required at least eight positions in which pulses may occur. For example, four pulses were equally spaced to generate timing signals. The presence or absence of a pulse half-way between the consecutive clock pulse positions indicated one or the otherof two binary states.

To increase the packing density, the present invention uses the principle of comparing a number of different time intervals between consecutive pulses of a pulse train. If, for instance, two time intervals are used, only five positions in which pulses may occur are sufficient for the binary representation of the digits 0–9. By using this principle the detecting device will be very simple and inexpensive as compared with the detecting devices required in prior art systems where clock pulses were utilized.

A better understanding of the invention will be obtained from the following description of two embodiments and with reference to the accompanying drawings in which:

FIG. **1** is a circuit diagram of a device according to the invention in which capacitors are used as storing means;

FIG. **2** schematically shows a label and a device for reading the label;

FIG. **3** is a curve chart showing voltage waveforms at different points in FIGS. **1** and **2**;

FIG. **4** is a circuit diagram of an embodiment in which binary counters are used as storing means; and

FIG. **5** is a curve chart showing voltage waveforms at different points in FIG. **4**, also explaining the function of the binary counters.

In the embodiments which will be described below, the time intervals between the pulses of a pulse train can take two different values, a short and a long interval. The short interval is identified by the detecting device as a binary "0" while the long interval is identified as a binary "1". The long interval is chosen to be twice the short interval.

In accordance with the principle of the invention, the first described embodiment comprises a first capacitor which is linearly charged by a constant-current generator in the time interval between two consecutive pulses in a pulse train. The next pulses causes first the voltage on the first capacitor to be transferred to a second capacitor. The capacitance of the second capacitor is substantially lower than that of the first capacitor in order not to lower the voltage. During the transfer of the voltage from the first to the second capacitor, the first capacitor is shorted out thereby being made ready

for a new charging in the next interval. Simultaneously with the charging of the first capacitor the second capacitor is linearly discharged through a second constant current generator. The discharge rate can take two different values, one for the short interval and another for the long interval. As will appear, for the detection of a short interval between signals, the second capacitor is not permitted to fully discharge (to zero), whereas during the detection of a long interval, the second capacitor is permitted to fully discharge thereby providing an output signal. If a short interval followed a short interval or a long interval followed a short interval, only one discharge rate would be sufficient for the second capacitor. However, a long interval may be followed by another long interval which will then be wrongly identified. This depends upon the fact that when a voltage corresponding to a long interval is transferred to the second capacitor it will be charged, positively or negatively, to a value such that the capacitor, in spite of another long interval, will not fully discharge before the next pulse arrives. To solve this problem a control circuit is provided which when a long interval appears doubles the discharge current through the second capacitor. The second capacitor now fully discharge so that the second long interval will be correctly identified. The control circuit will be reset as soon as a short interval appears again.

In the second of the embodiments to be described binary counters are used instead of capacitors. The counters operate in a manner similar to the capacitors. A first binary counter counts to a value which represents the elapsed time between two consecutive pulses in the pulse train. The value of the counter is then being transferred to a second counter which counts "backward". A binary "0" will be indicated if the second counter does not reach the value 0, and a binary "1" will be indicated if the second counter reaches the value 0.

In FIG. **2** a label **2** is shown which is being sensed by an optical reader **4.** The reader **4** converts into electrical signals the information on the label **12.** The information is in the form of black strokes separated by light portions. The signals are amplified in an amplifier **6** and are then applied to a peak detector **8** which operates to sense the peak amplitudes of the applied signals and convert these to **8** positive pulses with appropriate intermediate short and long intervals. The output from the peak detector **8** is applied to a pulse distributor **10** which produces two output signals identical to the input signal but somewhat out of phase with respect to each other and to the input signal. The various signals are shown in FIG. **3** where, as in FIGS. **1** and **2,** A designates the signal sensed from the label, B designates the pulse train from the peak detector **8,** C designates one of the pulse trains from the pulse distributor **10** and D designates the other pulse distributor output pulse train.

In FIG. **1** there is shown a device for detecting n different intervals between consecutive pulses in a pulse train. The device comprises two main portions, vix. a first storage device consisting of a capacitor which is being charged in the interval between two consecutive pulses, and a second storage devices also consisting of a capacitor to which is applied the voltage on the first capacitor. The second capacitor then discharged to indicate whether the shortest or any one of the longer intervals is present. As stated above, only the identifi-

cation of two different time intervals (short and long respectively) will be described in greater detail. In this connection reference is made only to the part of FIG. 1 located above the broken dotted line **12.**

With reference to FIG. **1,** the pulse train D (FIG. 2) is applied to an input terminal D connected to the control electrode of a switch **14.** In the figure the switch is shown as a circuit arrangement of two transistors. However, any suitable type of switch circuit may be used. A capacitor **16,** which is utilized as the first storage device, is connected parallel with the switch **14** and is linearly charged by a constant-current generator **18** during the interval between each pair of pulses in the pulse train D. The generator **18** operates similarly to another constant-current generator circuit indicated at **124,** and which will later be described. A junction E between the capacitor **16** and the output terminal of the constant-current generator **18** is connected to one terminal of a switch **20,** which is a field effect transistor. The other terminal of the switch **20** is connected to a point F and to one side of a capacitor **22.** The other side of capacitor **22** is connected to ground. The control electrode of the switch **20** receives the pulse train C (FIG. 2).

The capacitor **22** is discharged through the constant current generator circuit **24.** The generator **24** comprises a transistor **26** which, when conducting, draws a constant-current to provide for the linear discharge of the capacitor **22.** The one side of capacitor **22** is also, connected to one input terminal of a comparator **28.** The other input terminal of the comparator **28** is connected to ground. The output terminal G of the comparator **28** provides an output signal indicating a binary "1" and thus a long interval. When the signal applied to both inputs is equal, i.e. the signal coupled from the capacitor **22** is equal to zero. This output signal may be transferred to a memory (not shown) via a line **30** for storage.

The output terminal of the comparator **28** is also connected to flip-flop **32** which, upon reception of an output signal from the comparator, provides a signal Q (FIG. 3) which is coupled to the base of a transistor **34** causing it to conduct. The conduction of transistor **34** connects a resistor **36** in parallel with the emitter resistor **38** of the transistor **26,** whereby the discharge current of the capacitor **22** through the transistor **26** is increased. In the embodiment described, the long interval, as stated above, has been chosen to be twice the short interval and therefore the discharge current will be doubled for the long interval.

The function of the device shown in FIG. **1** will now be described with reference to FIGS. **2** and **3.** The signal A which is obtained from the optical reader **4** is converted by the peak detector **8** to provide a corresponding pulse train B conssisting of positive pulses with, from left to right, two short intervals, two long intervals and another short interval. In the pulse distributor **10** the pulse train B is converted to two pulse trains C and D identical to the pulse train B except for a small phase difference existing between the pulse trans C. and D and between the pulse train B and each of the pulse trains C and D. It is assumed that a start code (not shown) on the label **2** has set the short interval, i.e. that the capacitor **16** has been charged to a voltage corresponding to the short interval before the first pulse of the pulse train C operates the switch **20** to transfer the voltage on capacitor **16** to capacitor **22.**

The first pulse of the pulse train B operates to reset the flip-flop **32.** As no output is produced by the capacitor **28,** flip-flop **32** will be in the reset condition. Thus, the discharge time for the capacitor **22** will take the value corresponding to a short interval. The first pulse of the pulse train C operates to close switch **20** thereby to transfer the voltage on the capacitor **16** to the capacitor **22.** Thereafter the first pulse in the pulse train D operates to close the switch **14** whereby the capacitor **16** is rapidly discharged and then again charges to measure the time between the first and second pulses os the pulse train D. The pulse trains B, C and D, as mentioned above, do not have the same phase. The time difference between corresponding pulses in the three pulse trains, however, is small (magnitude microsecodns) and therefore the pulses can be said to appear simultaneously when compared to the shortest time interval between two pulses in any of the pulse trains. The necessary time interval between corresponding pulses in the pulse trains C and D is determined by the charging time for the capacitor **22.**

As appears from FIG. **3,** line E, the capacitor **16** is charged from zero to a negative potential. When the switch **20** is closed, this negative potential is transferred to the capacitor **22.** Capacitor **22** then discharges towards zero, see FIG. **3,** line F. The discharge is, however, stopped before zero by the second pulse in the pulse train C which operates to close switch **20** and a negative potential from the capacitor **16** is again transferred to the capacitor **22.** This time the interval is short and the second pulse in the pulse train B insures that the flip-flop **32** remains reset. Flip-flop cannot be set as the comparator **28** has not produced an output signal. A binary "0" will be indicated in that the second pulse in the pulse train D is transferred via a line **31** to a memory for storage without any output signal being present on the line **30.** The second pulse in the pulse train D further operates to short-circuit the capacitor **16** which is thereby made ready for another time measuring sequence.

The time interval between the second and third pulses of the pulse trains B, C and D is short too and the third pulses operate in the same manner as the second pulses, see FIG. **3.** The capacitor **22** is not fully discharged, the comparator **28** will not produce any output signal, and a binary "0" is thereby indicated.

Between the third and fourth pulses a long interval exists, resulting the circuit operating in a different manner. The third pulse (pulse train C) causes a negative potential corresponding to a short interval to be transferred to the capacitor **22.** As appears from FIG. **3,** line F, the voltage on the capacitor **22** is permitted to reach 0 volts during the time interval between the occurrence of the third and fourth pulses (pulse train C). The comparator **28** now has 0 volts on both of its two input terminals, and therefore produces an output (G in FIG. **3**) which, via the line 0, is transmitted to the memory (not shown) for storage of a binary "1". The time interval between the fourth and fifth pulses in the pulse trains B, C and D is also a long one and this causes certain difficulties for the detecting circuit **22, 24, 28.** The voltage which upon the appearance of the fourth pulse in the pulse train C is transferred to the capacitor **22** is twice the voltage transferred after a short interval as the capacitor **16** has been charged for a period which is two times the short interval. This appears in FIG. **3,** lines E and F. The capacitor **22** will now discharge from

a negative voltage which is twice the voltage for a short interval. With the same discharge rate the capacitor **22** voltage will not normally reach 0 volts before the appearance of the fifth pulse of the pulse train C, in spite of the long interval. Thus, in this case the discharge rate of the capacitor **22** has to be increased. To do this, the output signal from the comparator **28,** indicating the first long interval (between the third and fourth pulses in pulse train C), is applied to the flip-flop **32,** which is thereby set applying an output signal Q to a control circuit comprising the transistor **34.** This transistor **34** starts to conduct thereby connecting the resistor **36** in parallel with the emitter resistor **38** for the transistor **26** of the constant-current generator **24.** The resistors **36** and **38** have the same value and therefore the current through the transistor **26** and through the capacitor **22** is doubled thereby increasing the discharge rate of the capacitor **22.** The voltage on the capacitor **22** will now reach 0 volts prior to the occurrence of the fifth pulse of the pulse train C see FIG. **3,** line F, and the comparator **28** will correctly indicate a binary "1" applying an output on the line **30.**

The fourth pulse of the pulse train B, as do all of the pulses of this pulse train tries to reset the flip-flop **32,** see FIG. **3,** line B. However, if at the same time that a line B pulse occurs the comparator 2B provides its first output, see FIG. **3,** line G, the flip-flop **32** will not be reset. The signal Q will remain also when the fifth line B pulse appears and will not be removed until the sixth pulse of the pulse train B appears at the reset input terminal of the flip-flop **32** simultaneously with no output from the comparator **28,** the last mentioned condition being caused by the short interval between the fifth and sixth pulses of the pulse trains. When the signal Q is removed from the base of transistor **34,** the transistor **34** will be cutoff thereby disconnecting the resistor **36.** The rate of discharge current through the transistor **26** and the capacitor **22** will again be set at a value corresponding to a short interval.

The pulse trains described above with reference to FIG. **3** represent one of the decimal digits 0–9. As stated above, using the method and device according to the invention, only six pulse generating strokes are required on an information carrier for the representation of any one of the digits 0–9.

In the foregoing embodiment of the invention it has been described a system for the identification of different time intervals of a pulse train by means of capacitors. In the following, another embodiment of the invention will be described with reference to FIGS. **4** and **5.** In this embodiment the capacitors have been replaced by binary counters.

The circuit shown in FIG. **4** is supplied with the pulse trains B, C and D and further with a pulse train K, having a phase difference with respect to pulse train D, and which is also provided at an output of the pulse distributor **10** (FIG. **2**). An oscillator **118** continuously stops a conventional binary counter **116.** Each flip-flop **116** *a-h*, of the counter **116** is connected to one input of a corresponding AND-gate **120** *a-h* the output of which is connected to a corresponding flip-flop **122** *a-h* of a binary counter **122** which is also conventional. The last flip-flop **122** *i* of the counter **122** is connected to an inhibiting input **107** of a gate **104.** The second inputs **103** and **105** of gates **102** and **104,** respectively, are supplied with gate pulses (pulse train 3) from the peak detector **8** (FIG. **2**). The counter **122** is stepped by pulses from the oscillator **118,** the pulses first having been converted to a lower frequency in a frequency divider **106.** When a value has been transferred from the counter **122,** the last-mentioned counter is not permitted to count to zero before the next pulse of the pulse train D causes a new value representing a short interval to be transferred. If, however, the interval is long, the counter **122** is permitted to count to zero to indicate the long interval. When a long interval follows another long interval the frequency of the pulses supplied to the counter **122** must be increased and, in the present embodiment, two times. Therefore a flip-flop **132** receives a signal from the AND-gate **102** when the counter **122** has counted to zero and when at the same time a gating pulse of the pulse train B appears. The signal from the AND-gate **102** operates to set the flip-flop **132** which produces an output signal which operates the frequency divider **106** to double the frequency.

The function of the device according to FIG. **4** will now be described. The first pulse of the pulse train K resets the binary counter **116** which is then stepped by pulses from the oscillator **118** in the interval between the first and second pulses of the pulse train K. The second pulse of the pulse train is applied to the input B of the circuit shown in FIG. **4** and thus to the inputs **103** and **105** of the gates **102** and **104.** As no output is produced by the counter **122** and applied to the input **101** of the gate **102,** no inhibiting signal is applied to the inhibiting input **107** or the gate **104** and therefore the gate will produce an output which operates to reset the flip-flop **132** (if not already reset). The frequency divider is adjusted to a frequency intended for a short interval. The second pulse of the pulse train C then operates to reset the counter **122** to make it ready to receive the number set in counter **116** and representing the short interval between the first and second pulses of the pulse train K when the second pulse of the pulse train D appears on the line **114** to the first inputs, connected together, of the gates **120** *a-h*. Following the transfer of data from the counter **116,** the second pulse of the pulse train K operates to reset the counter **115** which is thereby made ready to be stepped to a value corresponding to the interval between the second and third pulses.

In FIGS. **5,** line L, it is shown haw the value in the counter **116** is increased step-by-step between each pair of pulses of the pulse train K and on line M it is shown how the value of the counter **122** is decreased step-by-step, however not reaching zero in a short interval and reading zero in a long interval. Such a long interval is present between the third and fourth pulses of the pulse trains. As appears from FIG. **5,** line L, the counter **116** in the long interval counts to a value two times the value for a short interval. At the same time the counter **122** counts to zero applying an output signal to the input **101** of the gate **102.** This signal remains until the fourth pulse of the pulse train D appears and is thus present when the fourth gating pulse of the pulse train B appaears on the input **103.** The gate **102,** therefore, provides a signal on the line **130** intended to be connected to a memory (not shown) for the storage of a binary "1". At the same time the counter **122** applies a signal to the flip-flop **132** which is thereby being set producing a signal which is applied to the frequency divider **106** to double the frequency of the pulses applied to the counter **122.** As stated above, this doubling is necessary for the correct identification of a subsequent

long interval. As the counter **116**, during the long interval between the third and fourth pulses, has counted to a value twice the short interval value and this value is transmitted to the counter **122** upon the occurrence of the fourth pulse in line D, the counter **122** will not have time to count to zero from that value with the pulse frequency used for a short interval and hence the counting must be done faster if a long interval is followed by another long interval. Then when a short interval is present between the fifth and sixth pulses the flip-flop **132** is reset by the sixth gating pulse (pulse train B) whereby the frequency for the pulses from the frequency divider **106** returns to the value for a short interval.

A binary "1" (long interval) is thus identified by the circuit in that the counter **122** produces a signal which is applied to line **130** leading to the memory (not shown). In a similar manner a binary "0" (short interval) is identified in that the pulses of the pulse train K are transmitted to the memory via line **131**. In the memory the signals on lines **130** and **131** may be coordinated to determine if a binary "0" or a binary "1" is to be stored.

In the foregoing has been described two embodiments of the invention, in the form of devices for the identification of two different time intervals between consecutive pulses of a pulse train, the pulses being derived from information on an information carrier, such as a label or the like. However, the invention is not limited to the embodiments described but generally refers to a method and a device for identifying an arbitrary number of time intervals between pulses in a pulse train, whereby the pulses of course may be derived from an arbitrary source. The invention is thus limited only through the subsequent claims.

I claim:

1. The method of identification of a number of different time intervals between consecutive pulses in an electrical pulse train comprising the steps of:

a. storing in a first storage unit a quantity value, the magnitude of said quantity being representative of the time interval between a first and the next succeeding pulse in said electrical pulse train; and counting with a digital counter pulses received from a pulse generator during the time interval between two consecutive pulses in said electrical pulse train;

b. transferring said quantity from said first storage unit to a second storage unit for storage therein upon the occurrence of said next succeeding pulse; and supplying the count of said pulses of said first digital counter to a second digital counter upon the termination of said time interval;

c. repeating steps a) and b) for each next succeeding pulse thereafter occurring in said electrical pulse train; and

d. sensing the quantities stored in said second storage unit with an identification circuit, siad identification circuit providing a signal indicative of a quantity value stored in said second storage unit exceeding a predetermined value, said predetermined value representing a predetermined time interval between consecutive pulses of said electrical pulse train, and counting backwards towards zero with said second counter from the supplied count value during the time interval between the second of said two consecutive pulses and the next consecutive pulse in said electrical pulse train.

2. The method as recited in claim **1** wherein step d) further includes:

increasing the rate of counting backwards of said second counter in dependence upon the relative time intervals between successive pulses of said electrical pulse train with said intervals being substantially equal to or exceeding said predetermined time interval.

3. A device for identifying time intervals between consecutive pulses of an electrical pulse train comprising:

first and second storage means;

means having a circuit path coupling to said first storage means during the time interval between two consecutive pulses of said pulse train and providing said storage means with a signal for storage therein, the quantity value of the stored signal varying in response to the time interval between said two consecutive pulses;

a first switch means coupling said second storage means to said first storage means and responsive to the second of said two consecutive pulse signals for causing the signal stored in said first storage means to be transferred to said second storage means; and

identification circuit means coupled to said second storage means and responsive to the signal stored therein for providing a predetermined output signal in accordance with a predetermined value for the signal in said second storage means,

said first and second storage means include a first and second digital counter, respectively;

said circuit path coupling means includes a first oscillatory circuit operative at a first frequency to step said first digital counter to provide at an output therefrom a count signal indication of the number of steps applied to said first digital counter during a time interval between two consecutive pulses of said pulse train;

said second switch means being responsive to the second of said two consecutive pulses for coupling the count signal in said first digital counter to said second digital counter; and

a second oscillatory circuit selectively operative at a second and higher third frequency not greater than said first frequency, to step said second digital counter in a direction to reduce the count value received therein from said first digital counter;

said identification circuit means being responsive to the count output signal from said second digital counter prior to the coupling thereto of the count signal from said first digital counter to provide a predetermined output signal in accordance with the value of the count output signal from said second digital counter.

4. A device as recited in claim **3** wherein:

said second switch means comprises a plurality of AND gates and wherein said first and second digital counters are first and second binary counters, respectively;

said first and second binary counters being coupled to each other by said AND gates such that said count signal stored in said first binary counter is transferred to said second binary counter in re-

sponse to a coupling to said AND gates of said second of two consecutive pulse signals.

5. A device as recited in claim 4 wherein:

said identification circuit means includes a flip-flop circuit having an input coupled to the output of said second counter and an output coupled to said second oscillatory circuit to provide a control signal thereto for selecting the operation thereof at one of said second and third frequencies in response to the signal output from said second counter indicating the presence of a predetermined count value representing a predetermined time interval between consecutive pulses of said electrical pulse train.

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