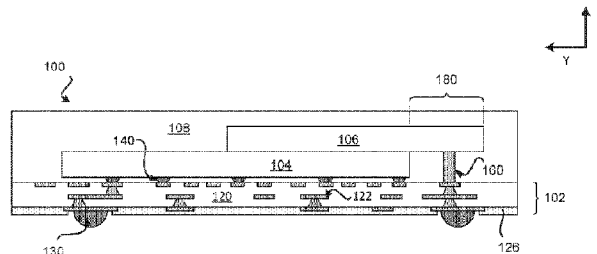


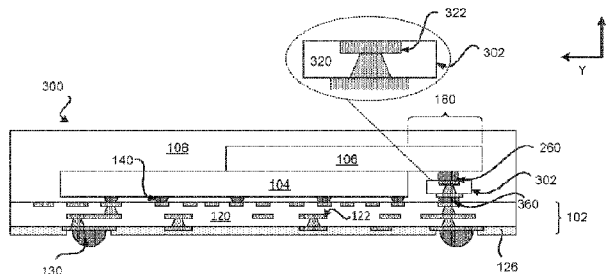


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(54) **Title:** PACKAGE COMPRISING STACKED INTEGRATED DEVICES WITH OVERHANG



CROSS SECTIONAL PROFILE VIEW
FIG. 1



CROSS SECTIONAL PROFILE VIEW
FIG. 3

(57) **Abstract:** A package that includes a substrate, a first integrated device coupled to the substrate, and a second integrated device coupled to the first integrated device. A portion of the second integrated device overhangs over the first integrated device. The second integrated device is configured to be coupled to the substrate. The second integrated device includes a front side and a back side. The front side of the second integrated device faces the substrate.



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- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
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**PACKAGE COMPRISING
STACKED INTEGRATED DEVICES WITH OVERHANG**

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of Non-Provisional Application Serial No. 17/375,931 filed in the United States Patent Office on July 14, 2021, the entire content of which is incorporated herein by reference as if fully set forth below in its entirety and for all applicable purposes.

Field

[0002] Various features relate to packages with integrated devices.

Background

[0003] A package may include a substrate and integrated devices. These components are coupled together to provide a package that may perform various electrical functions. How the integrated devices and the substrate are coupled together affects how the package performs overall. There is an ongoing need to provide better performing packages and reduce the overall size of packages.

SUMMARY

[0004] Various features relate to packages with integrated devices.

[0005] One example provides a package that includes a substrate, a first integrated device coupled to the substrate, and a second integrated device coupled to the first integrated device. A portion of the second integrated device overhangs over the first integrated device. The second integrated device is configured to be coupled to the substrate. The second integrated device includes a front side and a back side. The front side of the second integrated device faces the substrate.

[0006] Another example provides an apparatus that includes a substrate, a first integrated device coupled to the substrate, and a second integrated device coupled to the first integrated device. A portion of the second integrated device overhangs over the first integrated device. The second integrated device is configured to be coupled to the substrate. The second integrated device includes a front side and a back side. The front side of the second integrated device faces the substrate.

[0007] Another example provides a method for fabricating a package. The method provides a substrate. The method couples a first integrated device to the substrate. The method couples a second integrated device to the first integrated device such that a portion of the second integrated device overhangs over the first integrated device. The second integrated device is configured to be coupled to the substrate. The second integrated device includes a front side and a back side. The front side of the second integrated device faces the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Various features, nature and advantages may become apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout.

[0009] FIG. 1 illustrates a cross sectional profile view of a package that includes stacked integrated devices with overhang.

[0010] FIG. 2 illustrates a cross sectional profile view of a package that includes stacked integrated devices with overhang.

[0011] FIG. 3 illustrates a cross sectional profile view of a package that includes stacked integrated devices with overhang.

[0012] FIG. 4 illustrates a cross sectional profile view of a package that includes stacked integrated devices with overhang.

[0013] FIG. 5 illustrates a cross sectional profile view of a package that includes stacked integrated devices with overhang.

[0014] FIG. 6 illustrates a cross sectional profile view of a package that includes stacked integrated devices with overhang.

[0015] FIGS. 7A--7B illustrate an exemplary sequence for fabricating a package with stacked integrated devices with overhang.

[0016] FIGS. 8A--8B illustrate an exemplary sequence for fabricating a package with stacked integrated devices with overhang.

[0017] FIGS. 9A--9B illustrate an exemplary sequence for fabricating a package with stacked integrated devices with overhang.

[0018] FIG. 10 illustrates an exemplary flow diagram of a method for fabricating a package with stacked integrated devices with overhang.

[0019] FIGS. 11A--11B illustrate an exemplary sequence for fabricating a substrate.

[0020] FIG. 12 illustrates an exemplary flow diagram of a method for fabricating a substrate.

[0021] FIG. 13 illustrates various electronic devices that may integrate a die, an electronic circuit, an integrated device, an integrated passive device (IPD), a passive component, a package, and/or a device package described herein.

DETAILED DESCRIPTION

[0022] In the following description, specific details are given to provide a thorough understanding of the various aspects of the disclosure. However, it will be understood by one of ordinary skill in the art that the aspects may be practiced without these specific details. For example, circuits may be shown in block diagrams in order to avoid obscuring the aspects in unnecessary detail. In other instances, well-known circuits, structures and techniques may not be shown in detail in order not to obscure the aspects of the disclosure.

[0023] The present disclosure describes a package that includes a substrate, a first integrated device coupled to the substrate, and a second integrated device coupled to the first integrated device. A portion of the second integrated device overhangs over the first integrated device. The second integrated device is configured to be coupled to the substrate. The second integrated device includes a front side and a back side. The front side of the second integrated device faces the substrate. The second integrated device is coupled to the substrate through at least one pillar interconnect, at least one solder interconnect, and/or an interposer. The package may bypass the use of wire bonds, which helps reduce the overall size of the package and helps improve the performance of the package by reducing the interconnect length between integrated devices. The configuration of the package that includes putting one integrated device over another integrated device may also decrease the size and/or footprint of the package, while still providing improved package performance.

Exemplary Package Comprising Stacked Integrated Devices with Overhang

[0024] FIG. 1 illustrates a cross sectional profile view of a package 100 that includes stacked integrated devices with overhang. The package 100 includes a substrate 102, an integrated device 104, an integrated device 106, and an encapsulation layer 108. The integrated device 104 may be a first integrated device. The integrated device 106 may be a second integrated device. The substrate 102 includes at least one dielectric layer 120, a

plurality of interconnects 122 and a solder resist layer 126. A plurality of solder interconnects 130 may be coupled to the substrate 102.

[0025] The integrated device 104 is coupled to the substrate 102 through a plurality of solder interconnects 140. The integrated device 106 is located over the integrated device 104. The integrated device 106 may be coupled to the integrated device 104 through an adhesive (not shown). A portion 180 of the integrated device 106 may overhang over the integrated device 104. At least one pillar interconnect 160 may be coupled to the substrate 102 and to the front side of the portion 180 of the integrated device 106. The at least one pillar interconnect 160 may be coupled to the plurality of interconnect 122 through at least one solder interconnect (not shown). The integrated device 106 may be coupled to the substrate 102 through at least one pillar interconnect 160. The at least one pillar interconnect 160 may be located between the substrate 102 and the portion 180 of the integrated device 106. The integrated device 106 may be configured to be electrically coupled to the integrated device 104 through the at least one pillar interconnect 160, the plurality of interconnects 122, and/or the plurality of solder interconnects 140. For example, an electrical path for at least one signal between the integrated device 104 and the integrated device 106 may include the at least one pillar interconnect 160, at least one interconnect from the plurality of interconnects 122, and/or at least one solder interconnect from the plurality of solder interconnects 140. In the instance there is solder interconnect between the at least one pillar interconnect 160 and the plurality of interconnects 122, the electrical path may also include the solder interconnect between the at least one pillar interconnect 160 and the plurality of interconnects 122.

[0026] The integrated device 104 may include a front side and a back side. Similarly, the integrated device 106 may include a front side and a back side. The front side of the integrated device 104 may face the substrate 102. A back side of an integrated device may include the die substrate (e.g., silicon) side of the integrated device. The front side of the integrated device 106 may face the back side of the integrated device 104 and/or the substrate 102. For example, the front side of the portion 180 of the integrated device 106 may face the substrate 102. The front side of the integrated device 106 may be coupled to the back side of the integrated device 104 (e.g., mechanically coupled through an adhesive).

[0027] The encapsulation layer 108 may be located over the substrate 102, the integrated device 104 and the integrated device 106. The encapsulation layer 108 may at

least partially encapsulate the integrated device 104, the integrated device 106 and the at least one pillar interconnect 160. The encapsulation layer 108 may include a mold, a resin and/or an epoxy. The encapsulation layer 108 may be a means for encapsulation. The encapsulation layer 108 may be provided by using a compression and transfer molding process, a sheet molding process, or a liquid molding process.

[0028] The configuration of the package 100 may help bypass the use of wire bonds. Bypassing the use of wire bonds helps reduce the overall size of the package 100 and helps improve the performance of the package 100 by reducing the interconnect length between integrated devices (e.g., 104, 106). Since the front side of the integrated device 106 faces towards the substrate 102, there is a shorter and more direct electrical path between the substrate 102 the integrated device 106, helping improve signals speed between integrated devices. Packages that use wire bonds may require more space between the integrated device and the edge of the package to accommodate the placement of wire bonds. Since there are no wire bonds needed in the package 100, the edge of the package 100 may be located closer to the edge of the integrated devices (e.g., 104, 106), which helps reduce the overall form factor of the package 100. The same benefits and advantages may also be found for other packages described in the disclosure.

[0029] Different implementations may have packages with different configurations of integrated devices. FIG. 2 illustrates a package 200 that includes stacked integrated devices with overhang. The package 200 is similar to the package 100, and includes similar components, the same components, and/or similar arrangements as the package 100. Thus, the description of the package 100 may be applicable to the package 200. FIG. 2 illustrates that the package 200 includes at least one pillar interconnect 160 and at least one solder interconnect 260. The at least one solder interconnect 260 is coupled to the integrated device 106 and the at least one pillar interconnect 160. The at least one solder interconnect 260 may be coupled to the front side of the portion 180 of the integrated device 106. The at least one pillar interconnect 160 may be coupled to the substrate 102. In some implementations, the at least one pillar interconnect 160 may considered part of the substrate 102. The integrated device 106 may be coupled to the substrate 102 through the at least one solder interconnect 260 and the at least one pillar interconnect 160. The at least one solder interconnect 260 and the at least one pillar interconnect 160 may be located between the substrate 102 and the portion 180 of the integrated device 106. The integrated device 106 may be configured to be electrically coupled to the integrated device 104 through the at least one solder interconnect 260, the at least one pillar

interconnect 160, the plurality of interconnects 122, and/or the plurality of solder interconnects 140. For example, an electrical path for at least one signal between the integrated device 104 and the integrated device 106 may include the at least one solder interconnect 260, the at least one pillar interconnect 160, at least one interconnect from the plurality of interconnects 122, and/or at least one solder interconnect from the plurality of solder interconnects 140.

[0030] FIG. 3 illustrates a package 300 that includes stacked integrated devices with overhang. The package 300 is similar to the package 100, and includes similar components, the same components, and/or similar arrangements as the package 100. Thus, the description of the package 100 may be applicable to the package 300. FIG. 3 illustrates that the package 300 includes an interposer 302, at least one solder interconnect 260, and at least one solder interconnect 360. The at least one solder interconnect 260 is coupled to the integrated device 106 and the interposer 302. The at least one solder interconnect 260 may be coupled to the front side of the portion 180 of the integrated device 106. The at least one solder interconnect 360 may be coupled to the substrate 102 and the interposer 302. The integrated device 106 may be coupled to the substrate 102 through the at least one solder interconnect 260, the interposer 302 and the at least one solder interconnect 360. The interposer 302 may be a substrate. The interposer 302 includes at least one dielectric layer 320 and at least one interconnect 322 (e.g., interposer interconnect). The at least one solder interconnect 260, the interposer 302 and/or the at least one solder interconnect 360 may be located between the substrate 102 and the portion 180 of the integrated device 106.

[0031] The integrated device 106 may be configured to be electrically coupled to the integrated device 104 through the at least one solder interconnect 260, the interposer 302, the at least one solder interconnect 360, the plurality of interconnects 122, and/or the plurality of solder interconnects 140. For example, an electrical path for at least one signal between the integrated device 104 and the integrated device 106 may include the at least one solder interconnect 260, at least one interconnect 322, the at least one solder interconnect 360, at least one interconnect from the plurality of interconnects 122, and/or at least one solder interconnect from the plurality of solder interconnects 140.

[0032] FIGS. 1–3 illustrate that the at least one pillar interconnect 160, the at least one solder interconnect 260, the interposer 302, and/or the at least one solder interconnect 360 may be located between the substrate 102 and the portion 180 of the integrated device 106 that overhangs the integrated device 104.

[0033] Different implementations may include different numbers of integrated devices. For example, a package may include more than one integrated device that overhangs over one or more integrated devices.

[0034] FIG. 4 illustrates a package 400 that includes stacked integrated devices with overhang. The package 400 is similar to the package 100, and includes similar components, the same components, and/or similar arrangements as the package 100. Thus, the description of the package 100 may be applicable to the package 400. FIG. 4 illustrates two integrated devices that overhang over an integrated device. FIG. 4 illustrates that the package 400 includes the substrate 102, the integrated device 104 (e.g., first integrated device), the integrated device 106 (e.g., second integrated device), an integrated device 406 (e.g., third integrated device), the encapsulation layer 108, at least one pillar interconnect 160 (e.g., at least one first pillar interconnect), and at least one pillar interconnect 460 (e.g., at least one second pillar interconnect).

[0035] The integrated device 406 is located over the integrated device 104. The integrated device 406 may be coupled to the integrated device 104 through an adhesive (not shown). A portion 480 of the integrated device 406 may overhang over the integrated device 104. The front side of the integrated device 406 may face the back side of the integrated device 104 and/or the substrate 102. For example, the front side of the portion 480 of the integrated device 406 may face the substrate 102. The front side of the integrated device 406 may be coupled to the back side of the integrated device 104 (e.g., mechanically coupled through an adhesive).

[0036] At least one pillar interconnect 460 may be coupled to the substrate 102 and to the front side of the portion 480 of the integrated device 406. The at least one pillar interconnect 460 may be coupled to the plurality of interconnect 122 through at least one solder interconnect (not shown). The integrated device 406 may be coupled to the substrate 102 through at least one pillar interconnect 460. The integrated device 406 may be configured to be electrically coupled to the integrated device 104 through the at least one pillar interconnect 460, the plurality of interconnects 122, and/or the plurality of solder interconnects 140. For example, an electrical path for at least one signal between the integrated device 104 and the integrated device 406 may include the at least one pillar interconnect 460, at least one interconnect from the plurality of interconnects 122, and/or at least one solder interconnect from the plurality of solder interconnects 140. In the instance there is solder interconnect between the at least one pillar interconnect 460 and the plurality of interconnects 122, the electrical path may also include the solder

interconnect between the at least one pillar interconnect 460 and the plurality of interconnects 122.

[0037] The portion 480 of the integrated device 406 that overhangs over the integrated device 104 may have a different size and/or length than the portion 180 of the integrated device 106 that overhangs over the integrated device 104. Different implementations may have similar or different overhangs for different integrated devices. It is noted that the at least one pillar interconnect 160 may be from a plurality of pillar interconnects (e.g., rows of pillar interconnects) that are coupled between the integrated device 106 and the substrate 102. Similarly, the at least one pillar interconnect 460 may be from a plurality of pillar interconnects (e.g., rows of pillar interconnects) that are coupled between the integrated device 406 and the substrate 102.

[0038] FIG. 5 illustrates a package 500 that includes stacked integrated devices with overhang. The package 500 is similar to the packages 200 and/or 400, and includes similar components, the same components, and/or similar arrangements as the packages 200 and/or 400. Thus, the description of the packages 200 and 400 may be applicable to the package 500. FIG. 5 illustrates two integrated devices that overhang over another integrated device. FIG. 5 illustrates that the package 500 includes the substrate 102, the integrated device 104, the integrated device 106, the integrated device 406, the encapsulation layer 108, at least one pillar interconnect 160 (e.g., at least one first pillar interconnect), at least one pillar interconnect 460 (e.g., at least one second pillar interconnect), at least one solder interconnect 260 (e.g., at least one first solder interconnect) and at least one solder interconnect 560 (e.g., at least one second solder interconnect).

[0039] A portion 480 of the integrated device 406 may overhang over the integrated device 104. The at least one solder interconnect 560 is coupled to the integrated device 406 and the at least one pillar interconnect 460. The at least one solder interconnect 560 may be coupled to the front side of the portion 480 of the integrated device 406. The at least one pillar interconnect 460 may be coupled to the substrate 102. In some implementations, the at least one pillar interconnect 460 may be considered part of the substrate 102. The integrated device 406 may be coupled to the substrate 102 through the at least one solder interconnect 560 and the at least one pillar interconnect 460. The integrated device 406 may be configured to be electrically coupled to the integrated device 104 through the at least one solder interconnect 560, the at least one pillar interconnect 460, the plurality of interconnects 122, and/or the plurality of solder

interconnects 140. For example, an electrical path for at least one signal between the integrated device 104 and the integrated device 406 may include the at least one solder interconnect 560, the at least one pillar interconnect 460, at least one interconnect from the plurality of interconnects 122, and/or at least one solder interconnect from the plurality of solder interconnects 140.

[0040] It is noted that the at least one pillar interconnect 160 and the at least one solder interconnect 260 may be from a plurality of pillar interconnects (e.g., rows of pillar interconnects) and from a plurality of solder interconnects (e.g., rows of solder interconnects) that are coupled between the integrated device 106 and the substrate 102. Similarly, the at least one pillar interconnect 460 and the at least one solder interconnect 560 may be from a plurality of pillar interconnects (e.g., rows of pillar interconnects) and from a plurality of solder interconnects (e.g., rows of solder interconnects) that are coupled between the integrated device 406 and the substrate 102.

[0041] FIG. 6 illustrates a package 600 that includes stacked integrated devices with overhang. The package 600 is similar to the packages 300 and/or 400, and includes similar components, the same components, and/or similar arrangements as the packages 300 and/or 400. Thus, the description of the packages 300 and 400 may be applicable to the package 600. FIG. 6 illustrates two integrated devices that overhang over another integrated device. FIG. 6 illustrates that the package 600 includes the substrate 102, the integrated device 104, the integrated device 106, the integrated device 406, the encapsulation layer 108, an interposer 302 (e.g., first interposer), an interposer 602 (e.g., second interposer), at least one solder interconnect 260, at least one solder interconnect 360, at least one solder interconnect 660 and at least one solder interconnect 670.

[0042] A portion 480 of the integrated device 406 may overhang over the integrated device 104. The at least one solder interconnect 670 is coupled to the integrated device 406 and the interposer 602. The at least one solder interconnect 670 may be coupled to the front side of the portion 480 of the integrated device 406. The at least one solder interconnect 660 may be coupled to the substrate 102 and the interposer 602. The integrated device 406 may be coupled to the substrate 102 through the at least one solder interconnect 670, the interposer 602 and the at least one solder interconnect 660. The interposer 602 may be a substrate. The interposer 602 includes at least one dielectric layer 620 and at least one interconnect 622 (e.g., interposer interconnect). The interposer 602 may be similar to the interposer 302.

[0043] The integrated device 406 may be configured to be electrically coupled to the integrated device 104 through the at least one solder interconnect 670, the interposer 602, the at least one solder interconnect 660, the plurality of interconnects 122, and/or the plurality of solder interconnects 140. For example, an electrical path for at least one signal between the integrated device 104 and the integrated device 406 may include the at least one solder interconnect 670, at least one interconnect 622, the at least one solder interconnect 660, at least one interconnect from the plurality of interconnects 122, and/or at least one solder interconnect from the plurality of solder interconnects 140.

[0044] It is noted that the at least one interposer 302, the at least one solder interconnect 260, and the at least one solder interconnect 360 may be from a plurality of interposers (e.g., rows of interposer) and from a plurality of solder interconnects (e.g., rows of solder interconnects) that are coupled between the integrated device 106 and the substrate 102. Similarly, the at least one interposer 602, the at least one solder interconnect 670, and the at least one solder interconnect 660 may be from a plurality of interposers (e.g., rows of interposer) and from a plurality of solder interconnects (e.g., rows of solder interconnects) that are coupled between the integrated device 406 and the substrate 102.

[0045] It is noted that orientation of the interposer 302 and/or the interposer 602 shown in the disclosure is exemplary. The interposer 302 and/or the interposer 602 may be oriented in different ways. The interposer 302 and/or the interposer 602 may include a substrate. The interposer 302 and/or the interposer 602 may be fabricated using the process described in FIGS. 11A–11B. FIGS. 4–6 illustrate that the at least one pillar interconnect 160, the at least one solder interconnect 260, the interposer 302, and/or the at least one solder interconnect 360 may be located between the substrate 102 and the portion 180 of the integrated device 106 that overhangs the integrated device 104. FIGS. 4–6 also illustrate that the at least one pillar interconnect 460, the at least one solder interconnect 560, the interposer 602, and/or the at least one solder interconnect 660 may be located between the substrate 102 and the portion 480 of the integrated device 406 that overhangs the integrated device 104. It is noted that a package may include integrated devices that are coupled to the substrate using different combinations of pillar interconnects, solder interconnects and/or interposers. For example, one integrated device may be coupled to the substrate through a pillar interconnect, while another integrated device may be coupled to the substrate through an interposer. FIGS. 1–6 illustrate examples of integrated devices stacked on top of another, where one or more integrated

devices (e.g., 106, 406) are coupled (e.g., mechanically coupled, electrically coupled) to a substrate (e.g., 102) through at least one non-wire bond. Examples of non-wire bonds include a pillar interconnect, a solder interconnect and/or an interposer. The non-wire bonds provide at least one electrical path between the integrated device and the substrate. The non-wire bonds may also provide structural support for the portion of the integrated device that overhangs over another integrated device.

[0046] An integrated device (e.g., 104, 106, 406) may include a die (e.g., semiconductor bare die). The integrated device may include a power management integrated circuit (PMIC). The integrated device may include an application processor. The integrated device may include a modem. The integrated device may include a radio frequency (RF) device, a passive device, a filter, a capacitor, an inductor, an antenna, a transmitter, a receiver, a gallium arsenide (GaAs) based integrated device, a surface acoustic wave (SAW) filters, a bulk acoustic wave (BAW) filter, a light emitting diode (LED) integrated device, a silicon (Si) based integrated device, a silicon carbide (SiC) based integrated device, a memory, power management processor, and/or combinations thereof. An integrated device (e.g., 104, 106, 406) may include at least one electronic circuit (e.g., first electronic circuit, second electronic circuit, etc...).

[0047] In some implementations, the integrated device 104 (e.g., first integrated device) may include a processor and/or a modem. In some implementations, the integrated device 106 (e.g., second integrated device) and/or the integrated device 406 (e.g., third integrated device) may include memory. The integrated device 106 and the integrated device 406 may be planar to each other. The integrated device 106 and the integrated device 406 may have similar or different thicknesses.

[0048] Having described various packages, several methods for fabricating a package will now be described below.

Exemplary Sequence for Fabricating a Package Comprising Stacked Integrated Devices with Overhang

[0049] In some implementations, fabricating a package includes several processes. FIGS. 7A–7B illustrate an exemplary sequence for providing or fabricating a package. In some implementations, the sequence of FIGS. 7A–7B may be used to provide or fabricate the package 100 of FIG. 1. However, the process of FIGS. 7A–7B may be used to fabricate any of the packages (e.g., 400) described in the disclosure.

[0050] It should be noted that the sequence of FIGS. 7A–7B may combine one or more stages in order to simplify and/or clarify the sequence for providing or fabricating a package. In some implementations, the order of the processes may be changed or modified. In some implementations, one or more of processes may be replaced or substituted without departing from the scope of the disclosure.

[0051] Stage 1, as shown in FIG. 7A, illustrates a state after a substrate 102 is provided. The substrate 102 includes at least one dielectric layer 120, a plurality of interconnects 122 and a solder resist layer 126. Different implementations may use different substrates with different numbers of metal layers. A substrate may include a coreless substrate, a cored substrate, or an embedded trace substrate (ETS). FIGS. 11A–11B illustrate and describe an example of fabricating a substrate.

[0052] Stage 2 illustrates a state after at least one pillar interconnect 160 is formed over the substrate 102. A plating process may be used to form the at least one pillar interconnect 160. The at least one pillar interconnect 160 may be coupled to at least one interconnect from the plurality of interconnects 122. It is noted that in some implementations, the at least one pillar interconnect 160 may be provided with the substrate 102, when the substrate 102 is provided at Stage 1. In some implementations, the at least one pillar interconnect 160 may be considered part of the substrate 102.

[0053] Stage 3 illustrates a state after an integrated device 104 (e.g., first integrated device) is coupled to the substrate 102. The integrated device 104 may be coupled to the substrate 102 through a plurality of solder interconnects 140. A solder reflow process may be used to couple the integrated device 104 to the substrate 102.

[0054] Stage 4 illustrates a state after the integrated device 106 (e.g., second integrated device) is coupled to the integrated device 104, such that a portion (e.g., 180) of the integrated device 106 overhangs over the integrated device 104. An adhesive may be used to couple the integrated device 106 to the integrated device 104. For example, the front side of the integrated device 106 may be coupled to the back side of the integrated device 104 through an adhesive. The integrated device 106 may be coupled to the substrate 102 through the at least one pillar interconnect 160. A solder reflow process may be used to couple the integrated device 106 to the at least one pillar interconnect 160, which may include using solder interconnects.

[0055] In some implementations, the integrated device 106 may include the at least one pillar interconnect 160. That is, in some implementations, the at least one pillar interconnect 160 may be formed and/or coupled to the integrated device 106 prior to being

coupled to the substrate 102. In such instances, it may not be necessary to form the at least one pillar interconnect 160 (at Stage 2). A solder reflow process may be used to couple the at least one pillar interconnect 160 (e.g., of the integrated device 106) to the substrate 102. In such an instance, at least one solder interconnect may be coupled to the at least one pillar interconnect 160 and at least one interconnect from the plurality of interconnects 122. Different implementations may couple different integrated devices to the integrated device 104 and/or the substrate 102. For example, an integrated device 406 may be coupled to the integrated device 104.

[0056] Stage 5, as shown in FIG. 7B, illustrates a state after an encapsulation layer 108 is provided (e.g., formed) over the substrate 102 and the integrated devices (e.g., 104, 106). The encapsulation layer 108 may encapsulate the integrated devices(s) and/or the components. The encapsulation layer 108 may include a mold, a resin and/or an epoxy. A compression molding process, a transfer molding process, or a liquid molding process may be used to form the encapsulation layer 108. The encapsulation layer 108 may be photo etchable. The encapsulation layer 108 may be a means for encapsulation.

[0057] Stage 6 illustrates a state after a plurality of solder interconnects 130 is coupled to the substrate 102. A solder reflow process may be used to couple the plurality of solder interconnects 130 to interconnects from the plurality of interconnects 122 of the substrate 102. Stage 6 may illustrate an example of a package 100 that includes stacked integrated devices with overhang.

Exemplary Sequence for Fabricating a Package Comprising Stacked Integrated Devices with Overhang

[0058] In some implementations, fabricating a package includes several processes. FIGS. 8A–8B illustrate an exemplary sequence for providing or fabricating a package. In some implementations, the sequence of FIGS. 8A–8B may be used to provide or fabricate the package 200 of FIG. 2. However, the process of FIGS. 8A–8B may be used to fabricate any of the packages (e.g., 500) described in the disclosure.

[0059] It should be noted that the sequence of FIGS. 8A–8B may combine one or more stages in order to simplify and/or clarify the sequence for providing or fabricating a package. In some implementations, the order of the processes may be changed or modified. In some implementations, one or more of processes may be replaced or substituted without departing from the scope of the disclosure.

[0060] Stage 1, as shown in FIG. 8A, illustrates a state after a substrate 102 is provided. The substrate 102 includes at least one dielectric layer 120, a plurality of interconnects 122 and a solder resist layer 126. Different implementations may use different substrates with different numbers of metal layers. A substrate may include a coreless substrate, a cored substrate, or an embedded trace substrate (ETS). FIGS. 11A–11B illustrate and describe an example of fabricating a substrate.

[0061] Stage 2 illustrates a state after at least one pillar interconnect 160 is formed over the substrate 102. A plating process may be used to form the at least one pillar interconnect 160. The at least one pillar interconnect 160 may be coupled to at least one interconnect from the plurality of interconnects 122. It is noted that in some implementations, the at least one pillar interconnect 160 may be provided with the substrate 102, when the substrate 102 is provided at Stage 1. In some implementations, the at least one pillar interconnect 160 may be considered part of the substrate 102.

[0062] Stage 3 illustrates a state after at least one solder interconnect 260 is formed over the at least one pillar interconnect 160. A solder reflow process may be used to couple the at least one solder interconnect 260 to the at least one pillar interconnect 160.

[0063] Stage 4 illustrates a state after an integrated device 104 (e.g., first integrated device) is coupled to the substrate 102. The integrated device 104 may be coupled to the substrate 102 through a plurality of solder interconnects 140. A solder reflow process may be used to couple the integrated device 104 to the substrate 102.

[0064] Stage 5, as shown in FIG. 8B, illustrates a state after the integrated device 106 (e.g., second integrated device) is coupled to the integrated device 104, such that a portion (e.g., 180) of the integrated device 106 overhangs over the integrated device 104. An adhesive may be used to couple the integrated device 106 to the integrated device 104. For example, the front side of the integrated device 106 may be coupled to the back side of the integrated device 104 through an adhesive. The integrated device 106 may be coupled to the substrate 102 through the at least one solder interconnect 260 and the at least one pillar interconnect 160. A solder reflow process may be used to couple the integrated device 106 to the at least one pillar interconnect 160 through the at least one solder interconnect 260. Different implementations may couple different integrated devices to the integrated device 104 and/or the substrate 102. For example, an integrated device 406 may be coupled to the integrated device 104.

[0065] Stage 6 illustrates a state after an encapsulation layer 108 is provided (e.g., formed) over the substrate 102 and the integrated devices. The encapsulation layer 108

may encapsulate the integrated device(s) and/or the components. The encapsulation layer 108 may include a mold, a resin and/or an epoxy. A compression molding process, a transfer molding process, or a liquid molding process may be used to form the encapsulation layer 108. The encapsulation layer 108 may be photo etchable. The encapsulation layer 108 may be a means for encapsulation.

[0066] Stage 7 illustrates a state after a plurality of solder interconnects 130 is coupled to the substrate 102. A solder reflow process may be used to couple the plurality of solder interconnects 130 to interconnects from the plurality of interconnects 122 of the substrate 102. Stage 7 may illustrate an example of a package 200 that includes stacked integrated devices with overhang.

Exemplary Sequence for Fabricating a Package Comprising Stacked Integrated Devices with Overhang

[0067] In some implementations, fabricating a package includes several processes. FIGS. 9A–9B illustrate an exemplary sequence for providing or fabricating a package. In some implementations, the sequence of FIGS. 9A–9B may be used to provide or fabricate the package 300 of FIG. 3. However, the process of FIGS. 9A–9B may be used to fabricate any of the packages (e.g., 600) described in the disclosure.

[0068] It should be noted that the sequence of FIGS. 9A–9B may combine one or more stages in order to simplify and/or clarify the sequence for providing or fabricating a package. In some implementations, the order of the processes may be changed or modified. In some implementations, one or more of processes may be replaced or substituted without departing from the scope of the disclosure.

[0069] Stage 1, as shown in FIG. 9A, illustrates a state after a substrate 102 is provided. The substrate 102 includes at least one dielectric layer 120, a plurality of interconnects 122 and a solder resist layer 126. Different implementations may use different substrates with different numbers of metal layers. A substrate may include a coreless substrate, a cored substrate, or an embedded trace substrate (ETS). FIGS. 11A–11B illustrate and describe an example of fabricating a substrate.

[0070] Stage 2 illustrates a state after an integrated device 104 (e.g., first integrated device) is coupled to the substrate 102. The integrated device 104 may be coupled to the substrate 102 through a plurality of solder interconnects 140. A solder reflow process may be used to couple the integrated device 104 to the substrate 102.

[0071] Stage 3 illustrates a state after an interposer 302 is coupled to the substrate 102. The interposer 302 may be coupled to the substrate 102 through at least one solder interconnect 360. The at least one solder interconnect 360 may be coupled to interconnects from the plurality of interconnects 122. A solder reflow process may be used to couple the interposer 302 to the substrate 102.

[0072] Stage 4 illustrates a state after at least one solder interconnect 260 is formed over the interposer 302. A solder reflow process may be used to couple the at least one solder interconnect 260 to the interposer 302.

[0073] Stage 5, as shown in FIG. 9B, illustrates a state after the integrated device 106 (e.g., second integrated device) is coupled to the integrated device 104, such that a portion (e.g., 180) of the integrated device 106 overhangs over the integrated device 104. An adhesive may be used to couple the integrated device 106 to the integrated device 104. For example, the front side of the integrated device 106 may be coupled to the back side of the integrated device 104 through an adhesive. The integrated device 106 may be coupled to the substrate 102 through the interposer 302. A solder reflow process may be used to couple the integrated device 106 to the interposer 302 through the at least one solder interconnect 260. Different implementations may couple different integrated devices to the integrated device 104 and/or the substrate 102. For example, an integrated device 406 may be coupled to the integrated device 104.

[0074] Stage 6 illustrates a state after an encapsulation layer 108 is provided (e.g., formed) over the substrate 102 and the integrated devices. The encapsulation layer 108 may encapsulate the integrated device(s) and/or the components. The encapsulation layer 108 may include a mold, a resin and/or an epoxy. A compression molding process, a transfer molding process, or a liquid molding process may be used to form the encapsulation layer 108. The encapsulation layer 108 may be photo etchable. The encapsulation layer 108 may be a means for encapsulation.

[0075] Stage 7 illustrates a state after a plurality of solder interconnects 130 is coupled to the substrate 102. A solder reflow process may be used to couple the plurality of solder interconnects 130 to interconnects from the plurality of interconnects 122 of the substrate 102. Stage 7 may illustrate an example of a package 300 that includes stacked integrated devices with overhang.

Exemplary Flow Diagram of a Method for Fabricating a Package that Includes Stacked Integrated Devices with Overhang

[0076] In some implementations, fabricating a package that includes a substrate and stacked integrated devices with overhang includes several processes. FIG. 10 illustrates an exemplary flow diagram of a method 1000 for providing or fabricating a package. In some implementations, the method 1000 of FIG. 10 may be used to provide or fabricate the package 100 of FIG. 1 described in the disclosure. However, the method 1000 may be used to provide or fabricate any of the packages (e.g., 200, 300, 400, 500, 600) described in the disclosure.

[0077] It should be noted that the method of FIG. 10 may combine one or more processes in order to simplify and/or clarify the method for providing or fabricating a package. In some implementations, the order of the processes may be changed or modified.

[0078] The method provides (at 1005) a substrate (e.g., 102). The substrate 102 may be provided by a supplier or fabricated. A process similar to the process shown in FIGS. 11A–11B may be used to fabricate the substrate 102. However, different implementations may use different processes to fabricate the substrate 102. Examples of processes that may be used to fabricate the substrate 612 include a semi-additive process (SAP) and a modified semi-additive process (mSAP). The substrate 102 includes at least one dielectric layer 120, a plurality of interconnects 122, and a solder resist layer 126. The substrate 102 may include an embedded trace substrate (ETS). In some implementations, the at least one dielectric layer 120 may include prepreg layers. In some implementations, the substrate 102 may include at least one pillar interconnect (e.g., 160). Stage 1 of FIG. 7A illustrates and describes an example of providing a substrate.

[0079] The method couples (at 1010) at least one integrated device (e.g., first integrated device) to the substrate. For example, the integrated device 104 is coupled to a first surface (e.g., top surface) of the substrate 102. The integrated device 104 may be coupled to the substrate 102 through a plurality of solder interconnects 140. In some implementations, the integrated device 104 may be coupled to the substrate 102 through a plurality of pillar interconnects (not shown) and the plurality of solder interconnects 140. A solder reflow process may be used to couple the integrated device 104 to the substrate 102 through the plurality of solder interconnects 140. Stage 2 of FIG. 7A illustrates and describes an example of coupling at least one integrated device to a substrate.

[0080] The method couples (at 1015) another integrated device to an integrated device. For example, the integrated device 106 (e.g., second integrated device) is coupled

to the integrated device 104, such that a portion (e.g., 180) of the integrated device 106 overhangs the integrated device 104. An adhesive may be used to couple the integrated device 106 to the integrated device 104. For example, the front side of the integrated device 106 may be coupled to the back side of the integrated device 104 through an adhesive. The integrated device 106 may include at least one pillar interconnect 160. The integrated device 106 may be coupled to the substrate 102 through the at least one pillar interconnect 160. A solder reflow process may be used to couple the at least one pillar interconnect 160 to the substrate 102. In such an instance, at least one solder interconnect may be coupled to the at least one pillar interconnect 160 and at least one interconnect from the plurality of interconnects 122. It is noted that the at least one pillar interconnect 160 may be part of the substrate 102 and/or be part of the integrated device 106, prior to coupling the integrated device 106 to the substrate 102. Stage 4 of FIG. 7A illustrates and describes an example of coupling an integrated devices through at least one pillar interconnect.

[0081] In some implementations, the integrated device 106 may be coupled to the substrate 102 through the at least one solder interconnect 260 and the at least one pillar interconnect 160. In some implementations, the at least one pillar interconnect 160 may be considered part of the integrated device 106. In some implementations, the at least one pillar interconnect 160 may be considered part of the substrate 102. A solder reflow process may be used to couple the integrated device 106 to the at least one pillar interconnect 160 through the at least one solder interconnect 260. Stage 5 of FIG. 8B illustrates and describes an example of coupling an integrated devices through at least one pillar interconnect and at least one solder interconnect.

[0082] In some implementations, the integrated device 106 may be coupled to the substrate 102 through an interposer 302. A solder reflow process may be used to couple the integrated device 106 to the interposer 302 through the at least one solder interconnect 260. The interposer 302 may be coupled to the substrate 102 through a solder reflow process. Stage 5 of FIG. 9B illustrates and describes an example of coupling an integrated devices through at least interposer.

[0083] The method forms (at 1020) an encapsulation layer (e.g., 108) over the substrate (e.g., 102). The encapsulation layer 108 may be provided and formed over the substrate 102 and the integrated devices (e.g., 104, 106). The encapsulation layer 108 may encapsulate the integrated devices(s) and/or the components. The encapsulation layer 108 may include a mold, a resin and/or an epoxy. A compression molding process, a transfer

molding process, or a liquid molding process may be used to form the encapsulation layer 108. The encapsulation layer 108 may be photo etchable. The encapsulation layer 108 may be a means for encapsulation. Stage 5 of FIG. 7B illustrates and describes an example of forming an encapsulation layer.

[0084] The method couples (at 1025) a plurality of solder interconnects (e.g., 130) to the second surface of the substrate (e.g., 102). The plurality of solder interconnects 130 may be coupled to interconnects (e.g., 122) that are located over a second surface of the at least one dielectric layer 120. A solder reflow process may be used to couple the plurality of solder interconnects 130 to the substrate 102. Stage 6 of FIG. 7B illustrates and describes an example of coupling solder interconnects to a substrate.

[0085] The packages (e.g., 100) described in the disclosure may be fabricated one at a time or may be fabricated together as part of one or more wafers and then singulated into individual packages.

Exemplary Sequence for Fabricating a Substrate

[0086] In some implementations, fabricating a substrate includes several processes. FIGS. 11A–11B illustrate an exemplary sequence for providing or fabricating a substrate. In some implementations, the sequence of FIGS. 11A–11B may be used to provide or fabricate the substrate 102 of FIG. 1. However, the process of FIGS. 11A–11B may be used to fabricate any of the substrates described in the disclosure.

[0087] It should be noted that the sequence of FIGS. 11A–11B may combine one or more stages in order to simplify and/or clarify the sequence for providing or fabricating a substrate. In some implementations, the order of the processes may be changed or modified. In some implementations, one or more of processes may be replaced or substituted without departing from the scope of the disclosure.

[0088] Stage 1, as shown in FIG. 11A, illustrates a state after a carrier 1100 is provided and a metal layer is formed over the carrier 1100. The metal layer may be patterned to form interconnects 1102. A plating process and etching process may be used to form the metal layer and interconnects. In some implementations, the carrier 1100 may be provided with a metal layer that is patterned to form the interconnects 1102.

[0089] Stage 2 illustrates a state after a dielectric layer 1120 is formed over the carrier 1100 and the interconnects 1102. A deposition and/or lamination process may be used to form the dielectric layer 1120. The dielectric layer 1120 may include polyimide. However, different implementations may use different materials for the dielectric layer.

[0090] Stage 3 illustrates a state after a plurality of cavities 1110 is formed in the dielectric layer 1120. The plurality of cavities 1110 may be formed using an etching process (e.g., photo etching process) or laser process.

[0091] Stage 4 illustrates a state after interconnects 1112 are formed in and over the dielectric layer 1120, including in and over the plurality of cavities 1110. For example, a via, pad and/or traces may be formed. A plating process may be used to form the interconnects.

[0092] Stage 5 illustrates a state after another dielectric layer 1122 is formed over the dielectric layer 1120. A deposition and/or lamination process may be used to form the dielectric layer 1122. The dielectric layer 1122 may be the same material as the dielectric layer 1120. However, different implementations may use different materials for the dielectric layer.

[0093] Stage 6, as shown in FIG. 11B, illustrates a state after a plurality of cavities 1130 is formed in the dielectric layer 1122. An etching process or laser process may be used to form the cavities 1130.

[0094] Stage 7 illustrates a state after interconnects 1114 are formed in and over the dielectric layer 1122, including in and over the plurality of cavities 1130. For example, via, pad and/or trace may be formed. A plating process may be used to form the interconnects.

[0095] It is noted that Stages 5 through 7 may be iteratively repeated to form additional metal layers and additional dielectric layers. Some or all of the interconnects 1102, 1112, and/or 1114 may define a plurality of interconnects 122 of the substrate 102. The dielectric layers 1120, and 1122 may be represented by the at least one dielectric layer 120.

[0096] Stage 8 illustrates a state after the carrier 1100 is decoupled (e.g., removed, grinded out) from the dielectric layer 120, leaving the substrate 102 that includes the at least one dielectric layer 120 and the plurality of interconnects 122.

[0097] Stage 9 illustrates a state after the solder resist layer 124 and the solder resist layer 126 are formed over the substrate 102. A deposition process may be used to form the solder resist layer 124 and the solder resist layer 126. In some implementations, none or one solder resist layer may be formed over the at least one dielectric layer 120.

[0098] Different implementations may use different processes for forming the metal layer(s). In some implementations, a chemical vapor deposition (CVD) process and/or a physical vapor deposition (PVD) process for forming the metal layer(s). For example, a

sputtering process, a spray coating process, and/or a plating process may be used to form the metal layer(s).

Exemplary Flow Diagram of a Method for Fabricating a Substrate

[0099] In some implementations, fabricating a substrate includes several processes. FIG. 12 illustrates an exemplary flow diagram of a method 1200 for providing or fabricating a substrate. In some implementations, the method 1200 of FIG. 12 may be used to provide or fabricate the substrate(s) of FIG. 1. For example, the method of FIG. 12 may be used to fabricate the substrate 102.

[0100] It should be noted that the method 1200 of FIG. 12 may combine one or more processes in order to simplify and/or clarify the method for providing or fabricating a substrate. In some implementations, the order of the processes may be changed or modified.

[0101] The method provides (at 1205) a carrier 1100. Different implementations may use different materials for the carrier. The carrier may include a substrate, glass, quartz and/or carrier tape. Stage 1 of FIG. 11A illustrates and describes an example of a carrier that is provided.

[0102] The method forms (at 1210) a metal layer over the carrier 1100. The metal layer may be patterned to form interconnects. A plating process may be used to form the metal layer and interconnects. In some implementations, the carrier may include a metal layer. The metal layer over the carrier may be patterned to form interconnects (e.g., 1102). Stage 1 of FIG. 11A illustrates and describes an example of a metal layer and interconnects that are formed over a carrier.

[0103] The method forms (at 1215) a dielectric layer 1120 over the carrier 1100 and the interconnects 1102. A deposition and/or lamination process may be used to form the dielectric layer. The dielectric layer 1120 may include polyimide. Forming the dielectric layer may also include forming a plurality of cavities (e.g., 1110) in the dielectric layer 1120. The plurality of cavities may be formed using an etching process (e.g., photo etching) or laser process. Stages 2–3 of FIG. 11A illustrate and describe an example of forming a dielectric layer and cavities in the dielectric layer.

[0104] The method forms (at 1220) interconnects in and over the dielectric layer. For example, the interconnects 1112 may be formed in and over the dielectric layer 1120. A plating process may be used to form the interconnects. Forming interconnects may include providing a patterned metal layer over and/or in the dielectric layer. Forming

interconnects may also include forming interconnects in cavities of the dielectric layer. Stage 4 of FIG. 11A illustrates and describes an example of forming interconnects in and over a dielectric layer.

[0105] The method forms (at 1225) a dielectric layer 1122 over the dielectric layer 1120 and the interconnects. A deposition and/or lamination process may be used to form the dielectric layer. The dielectric layer 1122 may include polyimide. Forming the dielectric layer may also include forming a plurality of cavities (e.g., 1130) in the dielectric layer 1122. The plurality of cavities may be formed using an etching process or laser process. Stages 5–6 of FIGS. 11A–11B illustrate and describe an example of forming a dielectric layer and cavities in the dielectric layer.

[0106] The method forms (at 1230) interconnects in and/or over the dielectric layer. For example, the interconnects 1114 may be formed. A plating process may be used to form the interconnects. Forming interconnects may include providing a patterned metal layer over an in the dielectric layer. Forming interconnects may also include forming interconnects in cavities of the dielectric layer. Stage 7 of FIG. 11B illustrates and describes an example of forming interconnects in and over a dielectric layer.

[0107] The method may form additional dielectric layer(s) and additional interconnects as described at 1225 and 1230.

[0108] Once all the dielectric layer(s) and additional interconnects are formed, the method may decouple (e.g., remove, grind out) the carrier (e.g., 1100) from the dielectric layer 1120, leaving the substrate. In some implementations, the method may form one or more solder resist layers (e.g., 124, 126) over the substrate.

[0109] Different implementations may use different processes for forming the metal layer(s). In some implementations, a chemical vapor deposition (CVD) process and/or a physical vapor deposition (PVD) process for forming the metal layer(s). For example, a sputtering process, a spray coating process, and/or a plating process may be used to form the metal layer(s).

Exemplary Electronic Devices

[0110] FIG. 13 illustrates various electronic devices that may be integrated with any of the aforementioned device, integrated device, integrated circuit (IC) package, integrated circuit (IC) device, semiconductor device, integrated circuit, die, interposer, package, package-on-package (PoP), System in Package (SiP), or System on Chip (SoC). For example, a mobile phone device 1302, a laptop computer device 1304, a fixed

location terminal device 1306, a wearable device 1308, or automotive vehicle 1310 may include a device 1300 as described herein. The device 1300 may be, for example, any of the devices and/or integrated circuit (IC) packages described herein. The devices 1302, 1304, 1306 and 1308 and the vehicle 1310 illustrated in FIG. 13 are merely exemplary. Other electronic devices may also feature the device 1300 including, but not limited to, a group of devices (e.g., electronic devices) that includes mobile devices, hand-held personal communication systems (PCS) units, portable data units such as personal digital assistants, global positioning system (GPS) enabled devices, navigation devices, set top boxes, music players, video players, entertainment units, fixed location data units such as meter reading equipment, communications devices, smartphones, tablet computers, computers, wearable devices (e.g., watches, glasses), Internet of things (IoT) devices, servers, routers, electronic devices implemented in automotive vehicles (e.g., autonomous vehicles), or any other device that stores or retrieves data or computer instructions, or any combination thereof.

[0111] One or more of the components, processes, features, and/or functions illustrated in FIGS. 1–6, 7A–7B, 8A–8B, 9A–9B, 10, 11A–11B, and/or 12–13 may be rearranged and/or combined into a single component, process, feature or function or embodied in several components, processes, or functions. Additional elements, components, processes, and/or functions may also be added without departing from the disclosure. It should also be noted FIGS. 1–6, 7A–7B, 8A–8B, 9A–9B, 10, 11A–11B, and/or 12–13 and its corresponding description in the present disclosure is not limited to dies and/or ICs. In some implementations, FIGS. 1–6, 7A–7B, 8A–8B, 9A–9B, 10, 11A–11B, and/or 12–13 and its corresponding description may be used to manufacture, create, provide, and/or produce devices and/or integrated devices. In some implementations, a device may include a die, an integrated device, an integrated passive device (IPD), a die package, an integrated circuit (IC) device, a device package, an integrated circuit (IC) package, a wafer, a semiconductor device, a package-on-package (PoP) device, a heat dissipating device and/or an interposer.

[0112] It is noted that the figures in the disclosure may represent actual representations and/or conceptual representations of various parts, components, objects, devices, packages, integrated devices, integrated circuits, and/or transistors. In some instances, the figures may not be to scale. In some instances, for purpose of clarity, not all components and/or parts may be shown. In some instances, the position, the location, the sizes, and/or the shapes of various parts and/or components in the figures may be

exemplary. In some implementations, various components and/or parts in the figures may be optional.

[0113] The word “exemplary” is used herein to mean “serving as an example, instance, or illustration.” Any implementation or aspect described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other aspects of the disclosure. Likewise, the term “aspects” does not require that all aspects of the disclosure include the discussed feature, advantage or mode of operation. The term “coupled” is used herein to refer to the direct or indirect coupling (e.g., mechanical coupling) between two objects. For example, if object A physically touches object B, and object B touches object C, then objects A and C may still be considered coupled to one another—even if they do not directly physically touch each other. An object that is coupled to another object may be coupled to part of the object or all of the object. The term “electrically coupled” may mean that two objects are directly or indirectly coupled together such that an electrical current (e.g., signal, power, ground) may travel between the two objects. Two objects that are electrically coupled may or may not have an electrical current traveling between the two objects. The use of the terms “first”, “second”, “third” and “fourth” (and/or anything above fourth) is arbitrary. Any of the components described may be the first component, the second component, the third component or the fourth component. For example, a component that is referred to a second component, may be the first component, the second component, the third component or the fourth component. The term “encapsulating” means that the object may partially encapsulate or completely encapsulate another object. The terms “top” and “bottom” are arbitrary. A component that is located on top may be located over a component that is located on a bottom. A top component may be considered a bottom component, and vice versa. As described in the disclosure, a first component that is located “over” a second component may mean that the first component is located above or below the second component, depending on how a bottom or top is arbitrarily defined. In another example, a first component may be located over (e.g., above) a first surface of the second component, and a third component may be located over (e.g., below) a second surface of the second component, where the second surface is opposite to the first surface. It is further noted that the term “over” as used in the present application in the context of one component located over another component, may be used to mean a component that is on another component and/or in another component (e.g., on a surface of a component or embedded in a component). Thus, for example, a first component that is over the second component may mean that (1) the first component is over the second

component, but not directly touching the second component, (2) the first component is on (e.g., on a surface of) the second component, and/or (3) the first component is in (e.g., embedded in) the second component. A first component that is located “in” a second component may be partially located in the second component or completely located in the second component. The term “about ‘value X’”, or “approximately value X”, as used in the disclosure means within 10 percent of the ‘value X’. For example, a value of about 1 or approximately 1, would mean a value in a range of 0.9–1.1.

[0114] In some implementations, an interconnect is an element or component of a device or package that allows or facilitates an electrical connection between two points, elements and/or components. In some implementations, an interconnect may include a trace, a via, a pad, a pillar, a metallization layer, a redistribution layer, and/or an under bump metallization (UBM) layer / interconnect. In some implementations, an interconnect may include an electrically conductive material that may be configured to provide an electrical path for a signal (e.g., a data signal), ground and/or power. An interconnect may include more than one element or component. An interconnect may be defined by one or more interconnects. An interconnect may include one or more metal layers. An interconnect may be part of a circuit. Different implementations may use different processes and/or sequences for forming the interconnects. In some implementations, a chemical vapor deposition (CVD) process, a physical vapor deposition (PVD) process, a sputtering process, a spray coating, and/or a plating process may be used to form the interconnects.

[0115] Also, it is noted that various disclosures contained herein may be described as a process that is depicted as a flowchart, a flow diagram, a structure diagram, or a block diagram. Although a flowchart may describe the operations as a sequential process, many of the operations can be performed in parallel or concurrently. In addition, the order of the operations may be re-arranged. A process is terminated when its operations are completed.

[0116] In the following, further examples are described to facilitate the understanding of the disclosure.

[0117] Aspect 1: A package comprising a substrate; a first integrated device coupled to the substrate; and a second integrated device coupled to the first integrated device. A portion of the second integrated device overhangs over the first integrated device. The second integrated device is configured to be coupled to the substrate. The second

integrated device includes a front side and a back side. The front side of the second integrated device faces the substrate.

[0118] Aspect 2: The package of aspect 1, wherein the second integrated device is coupled to the substrate through at least one pillar interconnect.

[0119] Aspect 3: The package of aspect 1, wherein the second integrated device is coupled to the substrate through an interposer and at least one solder interconnect.

[0120] Aspect 4: The package of aspect 3, wherein the interposer includes a dielectric layer and at least one interposer interconnect.

[0121] Aspect 5: The package of aspects 3 through 4, wherein the interposer is located between the substrate and the portion of the second integrated device that overhangs the first integrated device.

[0122] Aspect 6: The package of aspects 1 through 5, wherein the second integrated device is coupled to the first integrated device through an adhesive.

[0123] Aspect 7: The package of aspects 1 through 6, wherein the first integrated device includes a first front side and a first back side, and wherein the front side of the second integrated device faces the first back side of the first integrated device.

[0124] Aspect 8: The package of aspects 1 through 7, wherein the first integrated device is coupled to the substrate through a plurality of solder interconnects.

[0125] Aspect 9: The package of aspects 1 through 8, further comprising a third integrated device coupled to the first integrated device, wherein a portion of the third integrated device overhangs over the first integrated device, and wherein the third integrated device is configured to be coupled to the substrate.

[0126] Aspect 10: The package of aspect 9, wherein the third integrated device is coupled to the substrate through at least one pillar interconnect, at least one solder interconnect, and/or an interposer.

[0127] Aspect 11: An apparatus comprising a substrate; a first integrated device coupled to the substrate; and a second integrated device coupled to the first integrated device. A portion of the second integrated device overhangs over the first integrated device. The second integrated device is configured to be coupled to the substrate. The second integrated device includes a front side and a back side. The front side of the second integrated device faces the substrate.

[0128] Aspect 12: The apparatus of aspect 11, wherein the second integrated device is coupled to the substrate through at least one pillar interconnect, at least one solder interconnect, and/or an interposer.

[0129] Aspect 13: The apparatus of aspect 12, wherein the interposer includes a dielectric layer and at least one interposer interconnect.

[0130] Aspect 14: The apparatus of aspects 12 through 13, wherein the interposer is located between the substrate and the portion of the second integrated device that overhangs the first integrated device.

[0131] Aspect 15: The apparatus of aspects 11 through 14, wherein the second integrated device is coupled to the first integrated device through an adhesive.

[0132] Aspect 16: The apparatus of aspects 11 through 15, wherein the first integrated device includes a first front side and a first back side, and wherein the front side of the second integrated device faces the first back side of the first integrated device.

[0133] Aspect 17: The apparatus of aspects 11 through 16, wherein the first integrated device is coupled to the substrate through a plurality of solder interconnects.

[0134] Aspect 18: The apparatus of aspects 11 through 17, further comprising a third integrated device coupled to the first integrated device, wherein a portion of the third integrated device overhangs over the first integrated device, and wherein the third integrated device is configured to be coupled to the substrate.

[0135] Aspect 19: The apparatus of aspect 18, wherein the third integrated device is coupled to the substrate through at least one pillar interconnect, at least one solder interconnect, and/or an interposer.

[0136] Aspect 20: The apparatus of aspects 11 through 19, wherein the apparatus includes a device selected from a group consisting of a music player, a video player, an entertainment unit, a navigation device, a communications device, a mobile device, a mobile phone, a smartphone, a personal digital assistant, a fixed location terminal, a tablet computer, a computer, a wearable device, a laptop computer, a server, an internet of things (IoT) device, and a device in an automotive vehicle.

[0137] Aspect 21: A method for fabricating a package. The method provides a substrate. The method couples a first integrated device to the substrate. The method couples a second integrated device to the first integrated device such that a portion of the second integrated device overhangs over the first integrated device. The second integrated device is configured to be coupled to the substrate. The second integrated device includes a front side and a back side. The front side of the second integrated device faces the substrate.

[0138] Aspect 22: The method of aspect 21, wherein the second integrated device is coupled to the substrate through at least one pillar interconnect, at least one solder interconnect, and/or an interposer.

[0139] Aspect 23: The method of aspects 21 through 22, wherein the second integrated device is coupled to the first integrated device through an adhesive.

[0140] Aspect 24: The method of aspects 21 through 23, further comprising forming an encapsulation layer over the substrate.

[0141] Aspect 25: The method of aspects 21 through 24, further comprising coupling a third integrated device to the first integrated device, wherein a portion of the third integrated device overhangs over the first integrated device, and wherein the third integrated device is configured to be coupled to the substrate.

[0142] Aspect 26: The method of aspect 25, wherein the third integrated device is coupled to the substrate through at least one pillar interconnect, at least one solder interconnect, and/or an interposer.

[0143] The various features of the disclosure described herein can be implemented in different systems without departing from the disclosure. It should be noted that the foregoing aspects of the disclosure are merely examples and are not to be construed as limiting the disclosure. The description of the aspects of the present disclosure is intended to be illustrative, and not to limit the scope of the claims. As such, the present teachings can be readily applied to other types of apparatuses and many alternatives, modifications, and variations will be apparent to those skilled in the art.

CLAIMS

1. A package comprising:
 - a substrate;
 - a first integrated device coupled to the substrate; and
 - a second integrated device coupled to the first integrated device,
 - wherein a portion of the second integrated device overhangs over the first integrated device,
 - wherein the second integrated device is configured to be coupled to the substrate,
 - wherein the second integrated device includes a front side and a back side, and
 - wherein the front side of the second integrated device faces the substrate.
2. The package of claim 1, wherein the second integrated device is coupled to the substrate through at least one pillar interconnect.
3. The package of claim 1, wherein the second integrated device is coupled to the substrate through an interposer and at least one solder interconnect.
4. The package of claim 3, wherein the interposer includes a dielectric layer and at least one interposer interconnect.
5. The package of claim 3, wherein the interposer is located between the substrate and the portion of the second integrated device that overhangs the first integrated device.
6. The package of claim 1, wherein the second integrated device is coupled to the first integrated device through an adhesive.
7. The package of claim 1,
 - wherein the first integrated device includes a first front side and a first back side,
 - and
 - wherein the front side of the second integrated device faces the first back side of the first integrated device.

8. The package of claim 1, wherein the first integrated device is coupled to the substrate through a plurality of solder interconnects.
9. The package of claim 1, further comprising a third integrated device coupled to the first integrated device,
 - wherein a portion of the third integrated device overhangs over the first integrated device, and
 - wherein the third integrated device is configured to be coupled to the substrate.
10. The package of claim 9, wherein the third integrated device is coupled to the substrate through at least one pillar interconnect, at least one solder interconnect, and/or an interposer.
11. An apparatus comprising:
 - a substrate;
 - a first integrated device coupled to the substrate; and
 - a second integrated device coupled to the first integrated device,
 - wherein a portion of the second integrated device overhangs over the first integrated device,
 - wherein the second integrated device is configured to be coupled to the substrate,
 - wherein the second integrated device includes a front side and a back side, and
 - wherein the front side of the second integrated device faces the substrate.
12. The apparatus of claim 11, wherein the second integrated device is coupled to the substrate through at least one pillar interconnect, at least one solder interconnect, and/or an interposer.
13. The apparatus of claim 12, wherein the interposer includes a dielectric layer and at least one interposer interconnect.
14. The apparatus of claim 12, wherein the interposer is located between the substrate and the portion of the second integrated device that overhangs the first integrated device.

15. The apparatus of claim 11, wherein the second integrated device is coupled to the first integrated device through an adhesive.

16. The apparatus of claim 11,
wherein the first integrated device includes a first front side and a first back side,
and
wherein the front side of the second integrated device faces the first back side of the first integrated device.

17. The apparatus of claim 11, wherein the first integrated device is coupled to the substrate through a plurality of solder interconnects.

18. The apparatus of claim 11, further comprising a third integrated device coupled to the first integrated device,
wherein a portion of the third integrated device overhangs over the first integrated device, and
wherein the third integrated device is configured to be coupled to the substrate.

19. The apparatus of claim 18, wherein the third integrated device is coupled to the substrate through at least one pillar interconnect, at least one solder interconnect, and/or an interposer.

20. The apparatus of claim 11, wherein the apparatus includes a device selected from a group consisting of a music player, a video player, an entertainment unit, a navigation device, a communications device, a mobile device, a mobile phone, a smartphone, a personal digital assistant, a fixed location terminal, a tablet computer, a computer, a wearable device, a laptop computer, a server, an internet of things (IoT) device, and a device in an automotive vehicle.

21. A method for fabricating a package, comprising:
providing a substrate;
coupling a first integrated device to the substrate; and
coupling a second integrated device to the first integrated device such that a portion of the second integrated device overhangs over the first integrated device,

wherein the second integrated device is configured to be coupled to the substrate,

wherein the second integrated device includes a front side and a back side, and

wherein the front side of the second integrated device faces the substrate.

22. The method of claim 21, wherein the second integrated device is coupled to the substrate through at least one pillar interconnect, at least one solder interconnect, and/or an interposer.

23. The method of claim 21, wherein the second integrated device is coupled to the first integrated device through an adhesive.

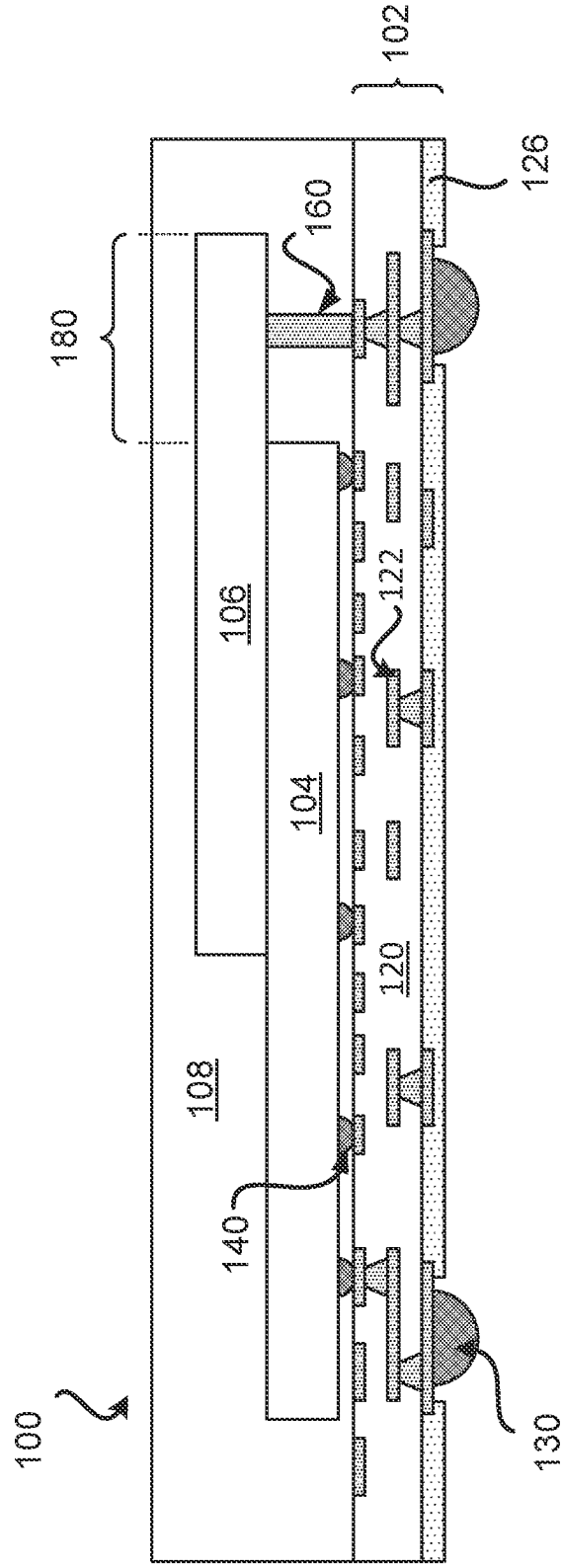
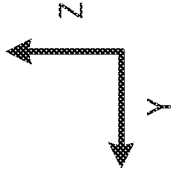
24. The method of claim 21, further comprising forming an encapsulation layer over the substrate.

25. The method of claim 21, further comprising coupling a third integrated device to the first integrated device,

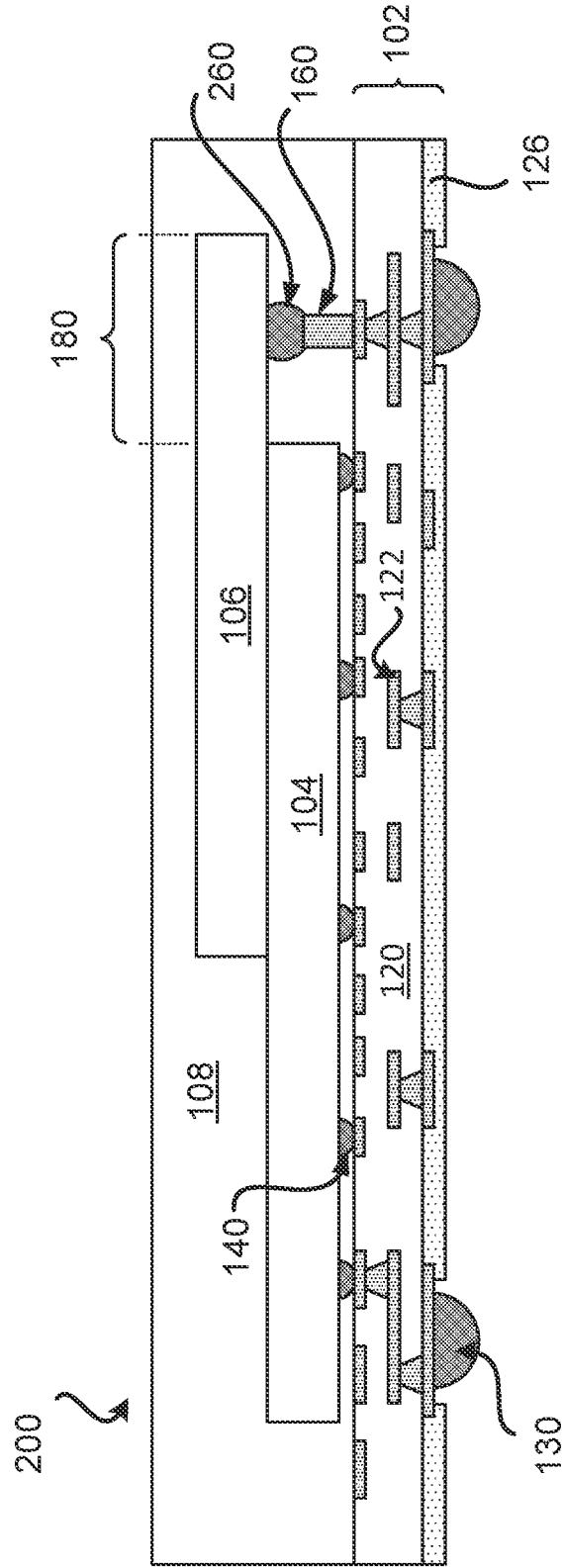
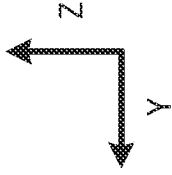
wherein a portion of the third integrated device overhangs over the first integrated device, and

wherein the third integrated device is configured to be coupled to the substrate.

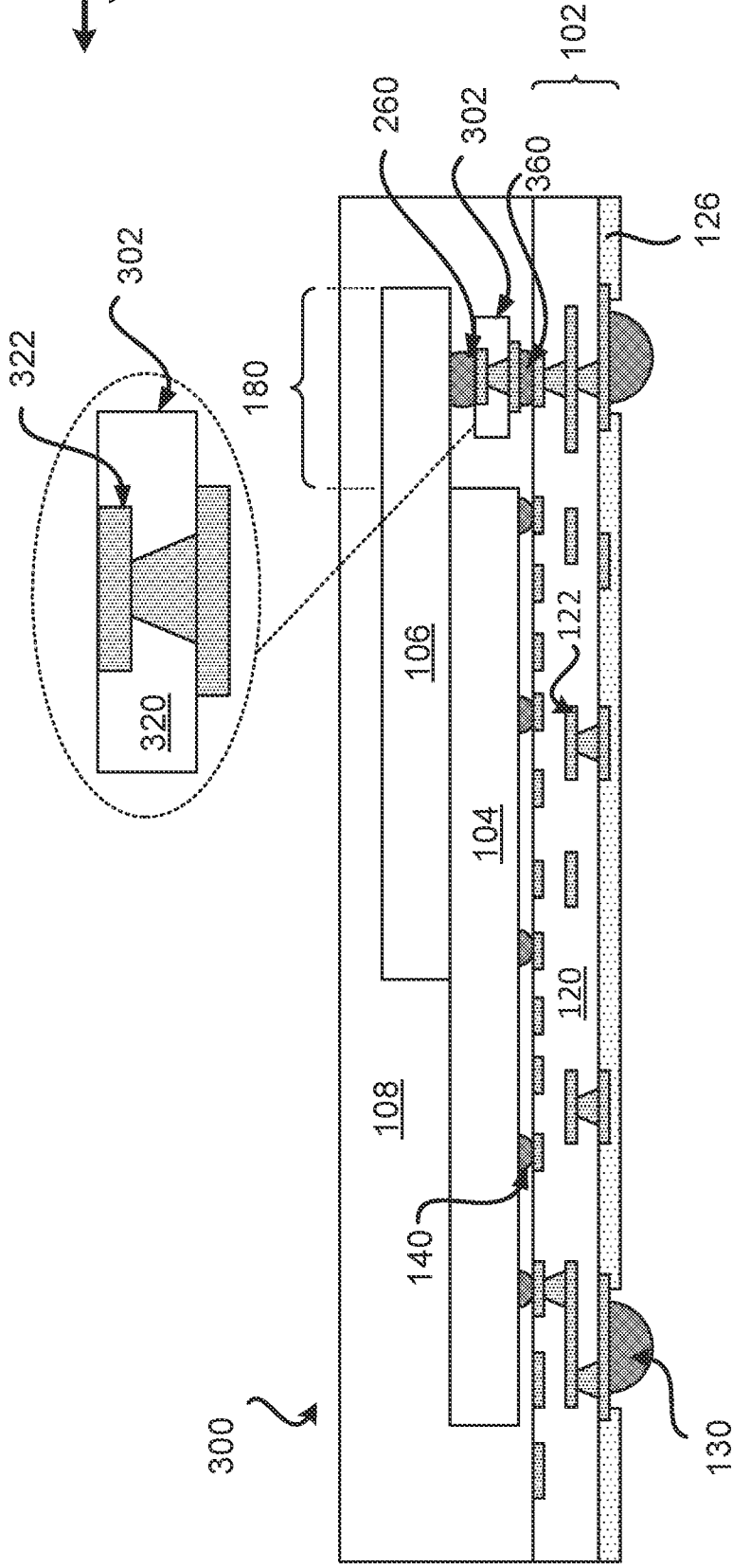
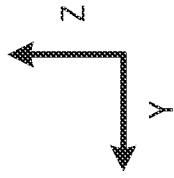
26. The method of claim 25, wherein the third integrated device is coupled to the substrate through at least one pillar interconnect, at least one solder interconnect, and/or an interposer.



CROSS SECTIONAL PROFILE VIEW
FIG. 1

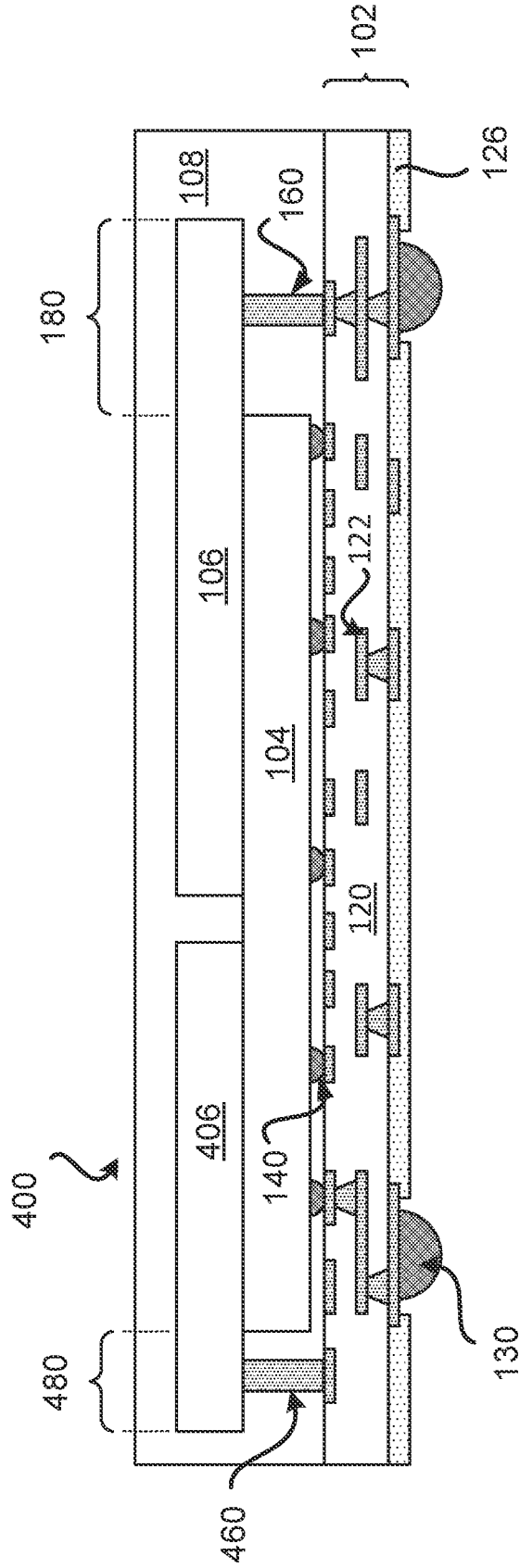
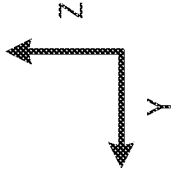


CROSS SECTIONAL PROFILE VIEW
FIG. 2

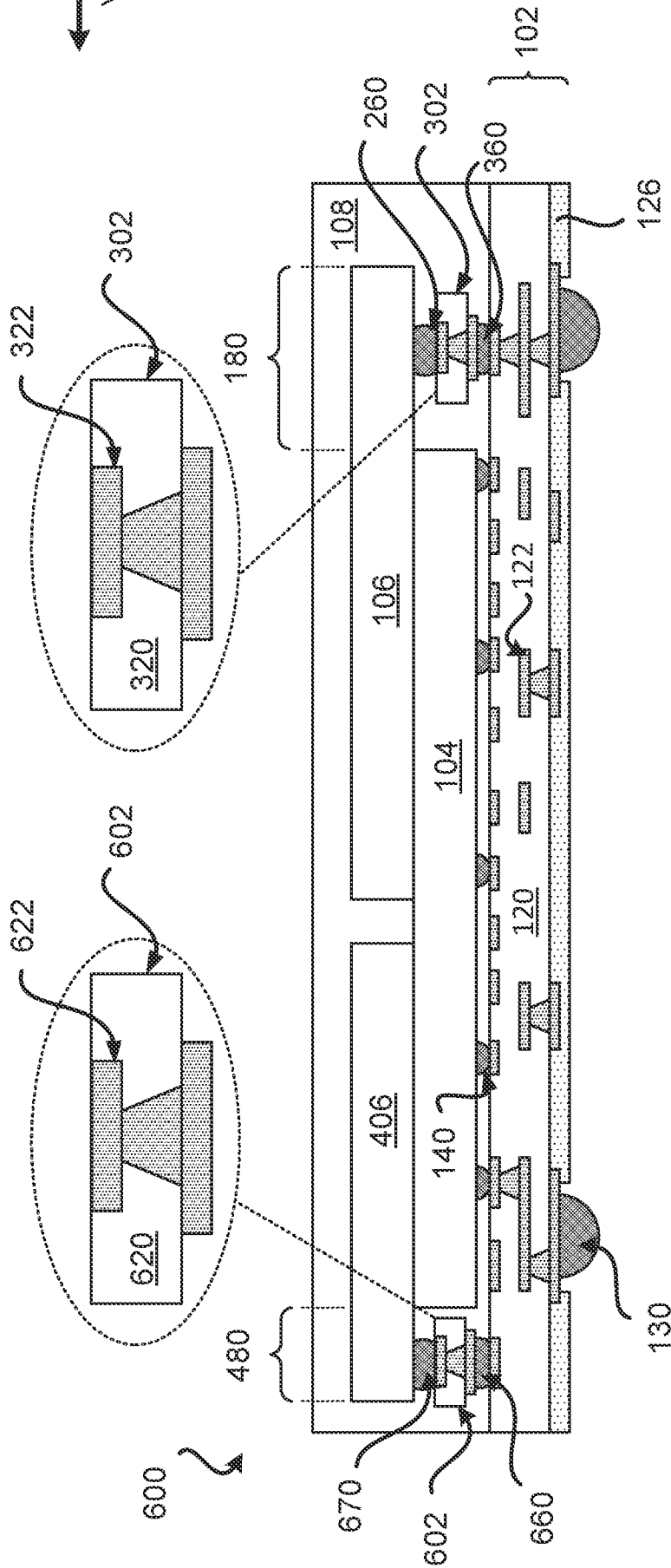
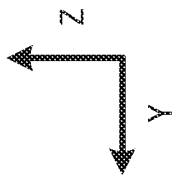


CROSS SECTIONAL PROFILE VIEW

FIG. 3



CROSS SECTIONAL PROFILE VIEW
FIG. 4



CROSS SECTIONAL PROFILE VIEW
FIG. 6

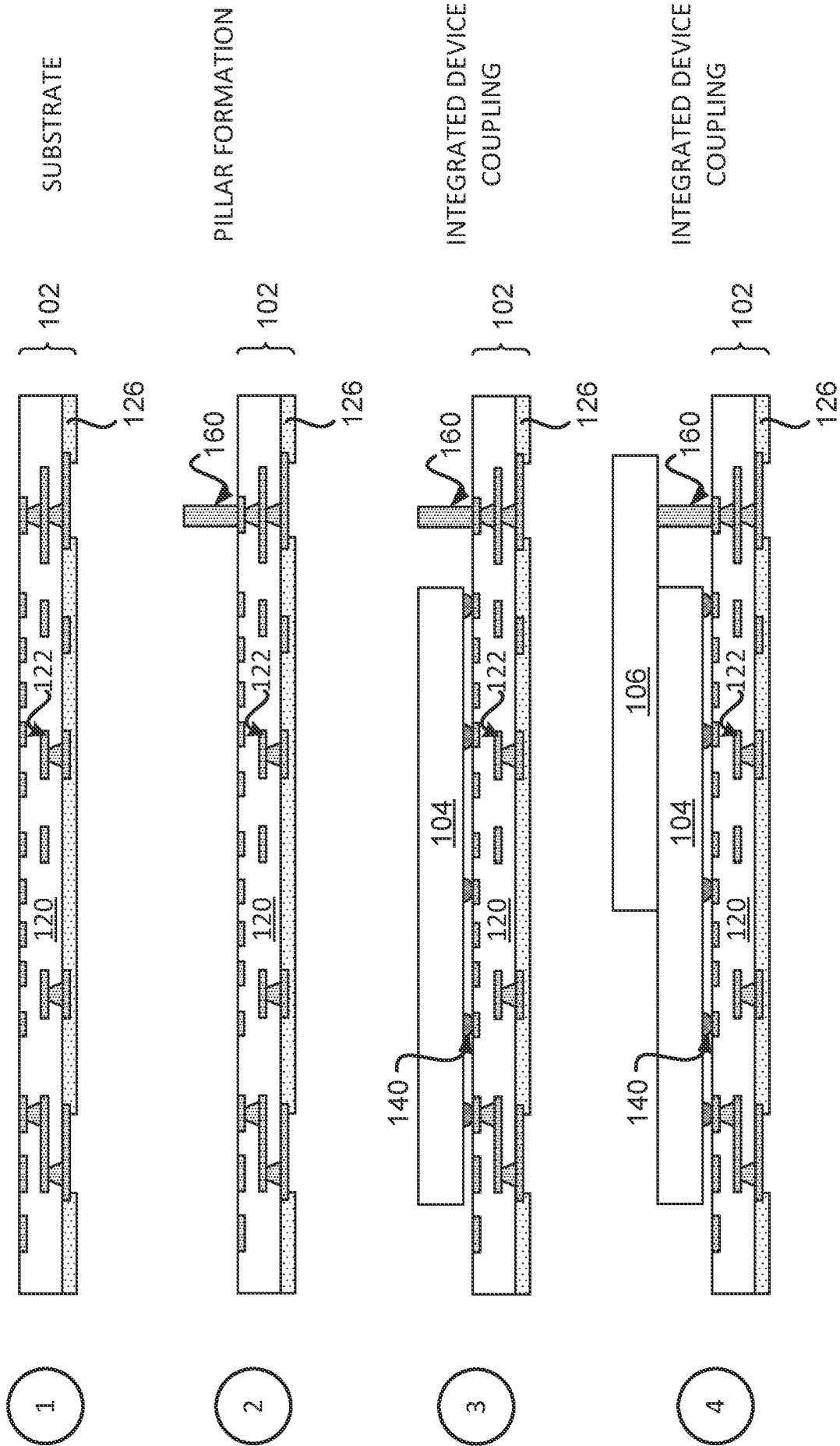


FIG. 7A

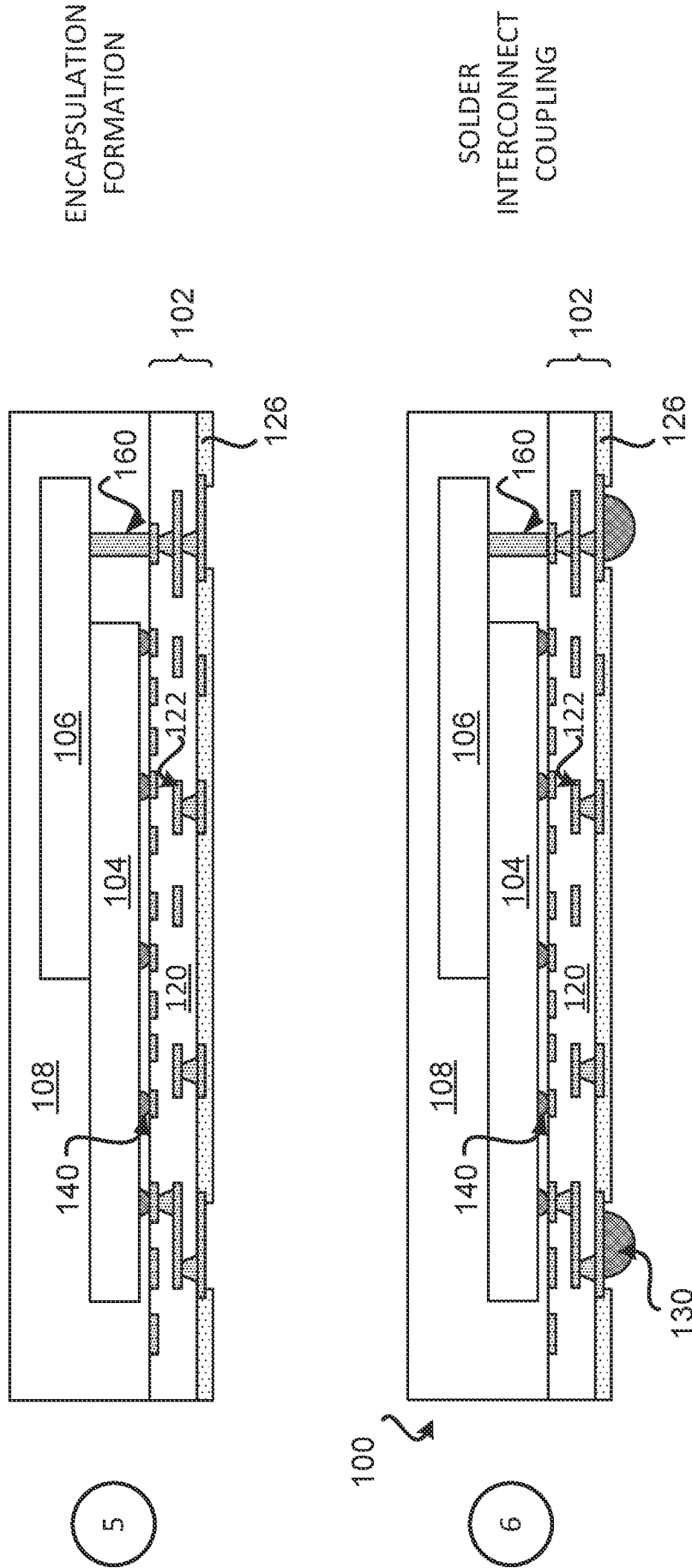


FIG. 7B

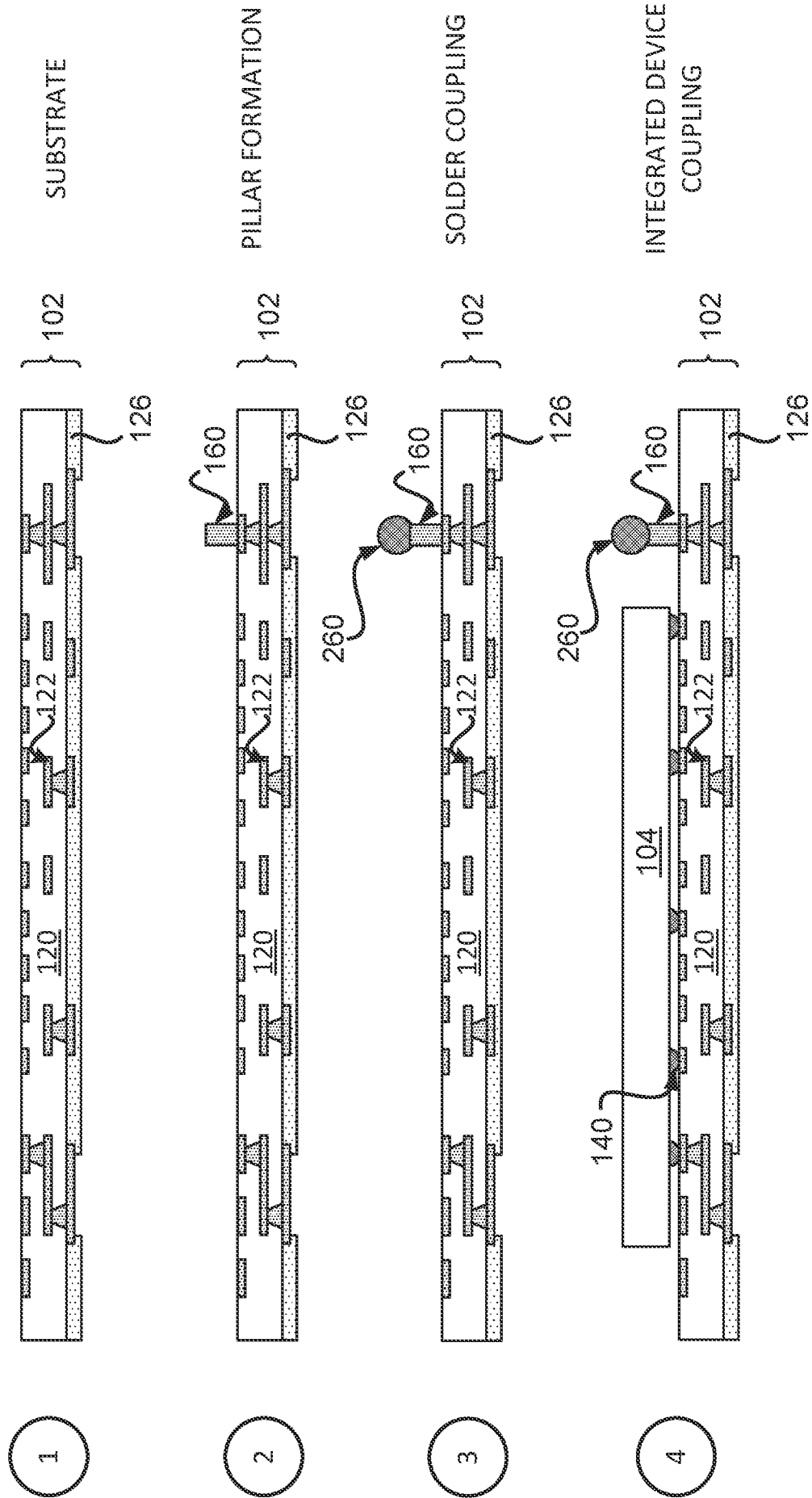


FIG. 8A

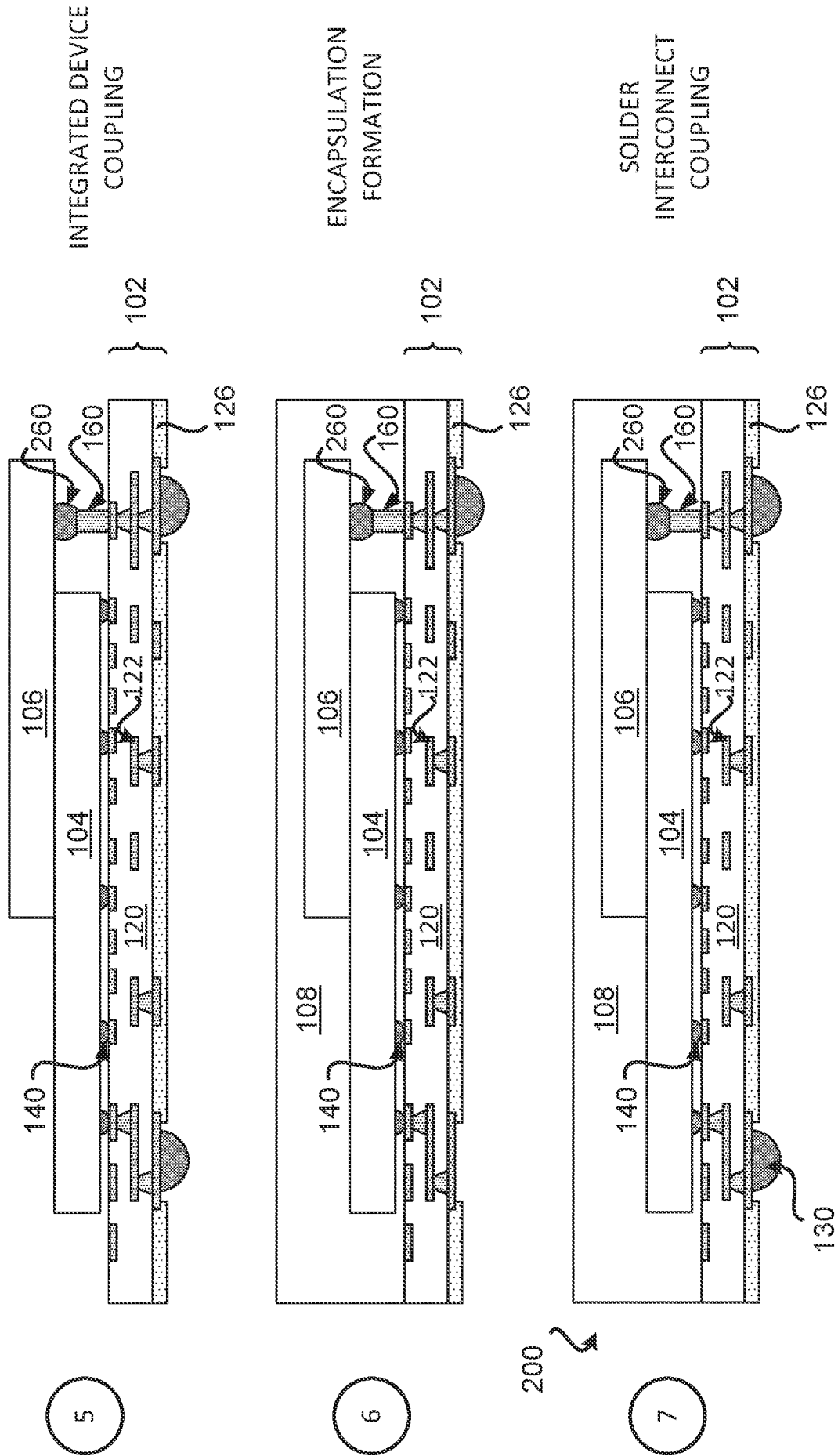


FIG. 8B

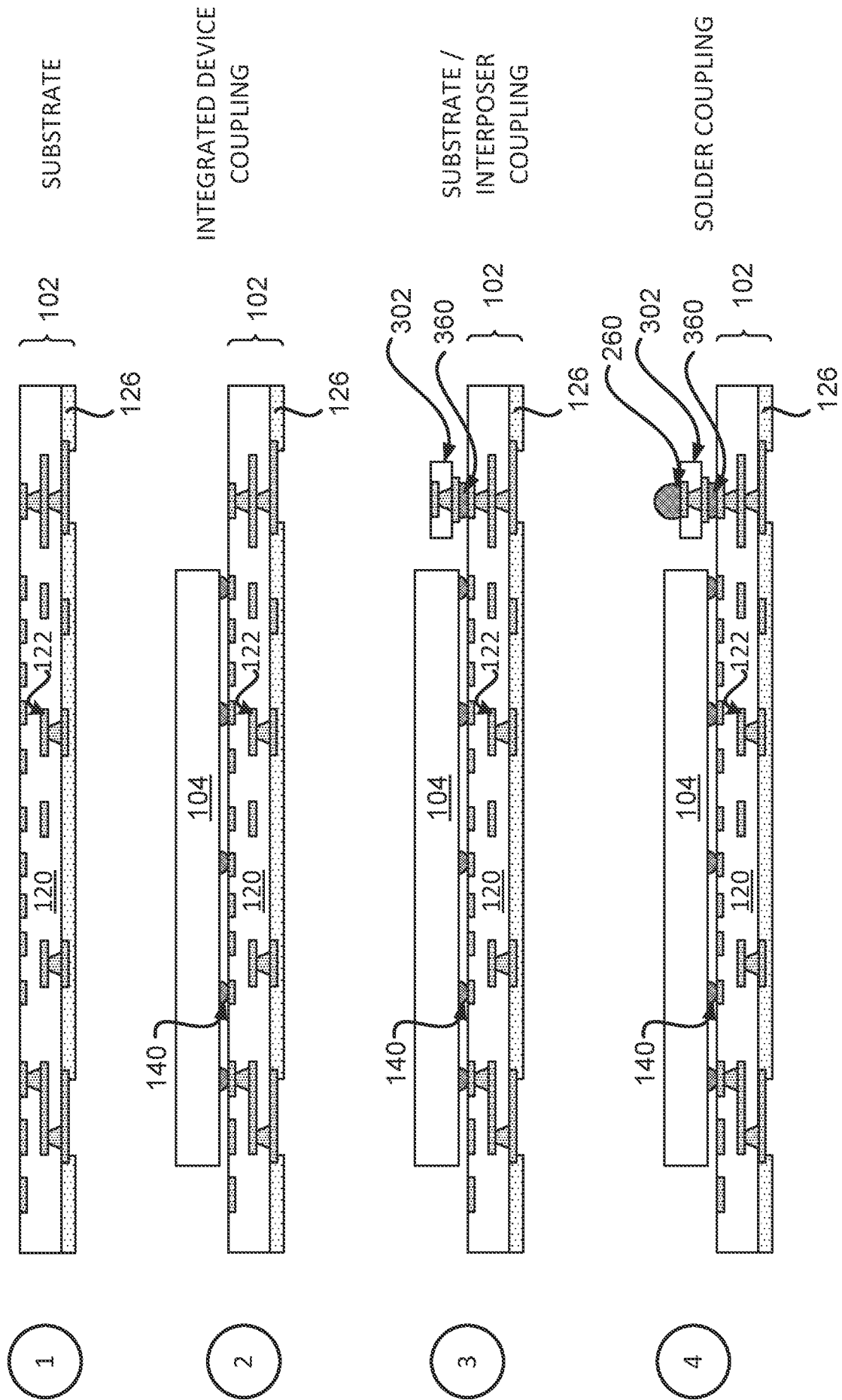


FIG. 9A

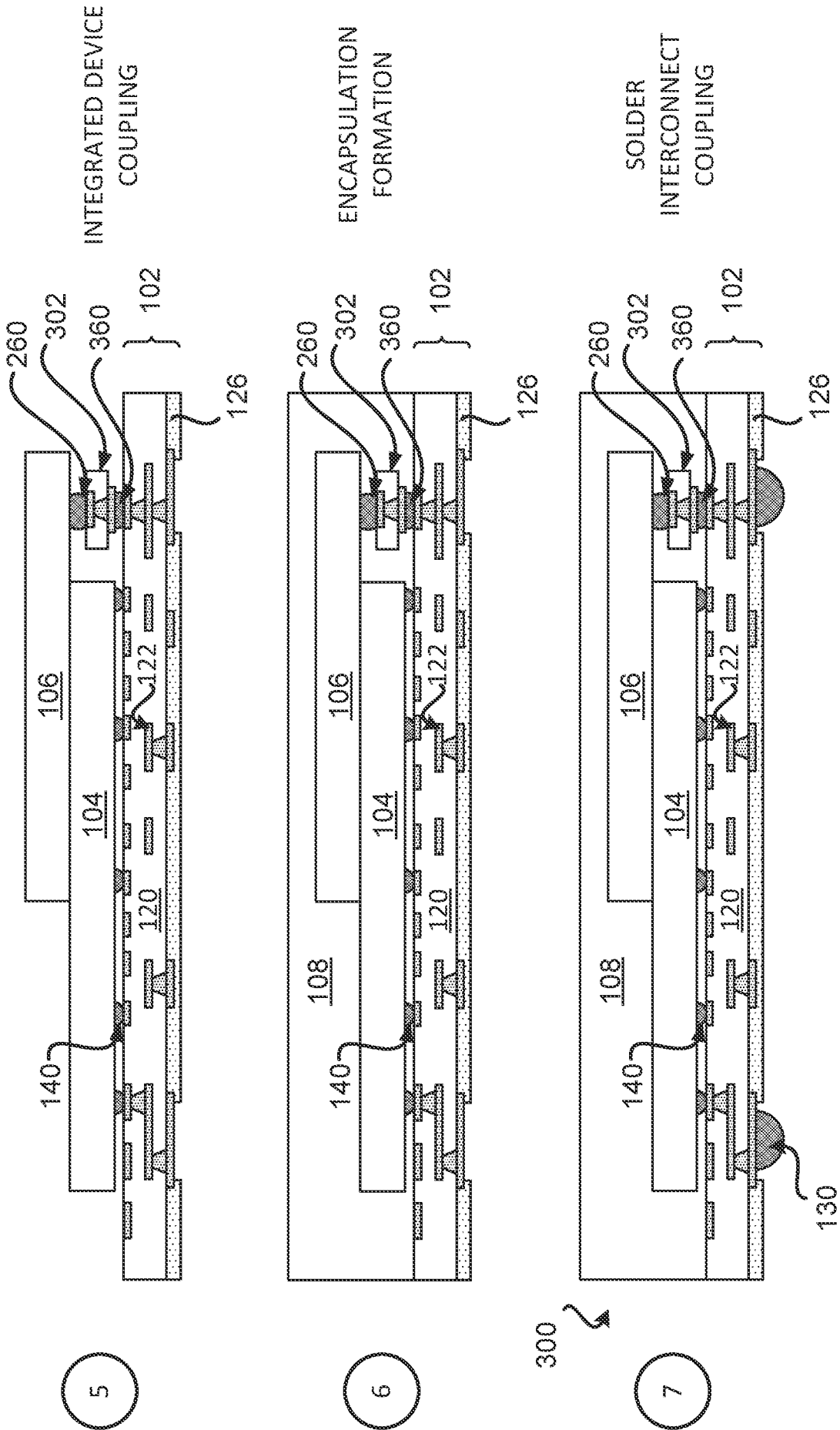


FIG. 9B

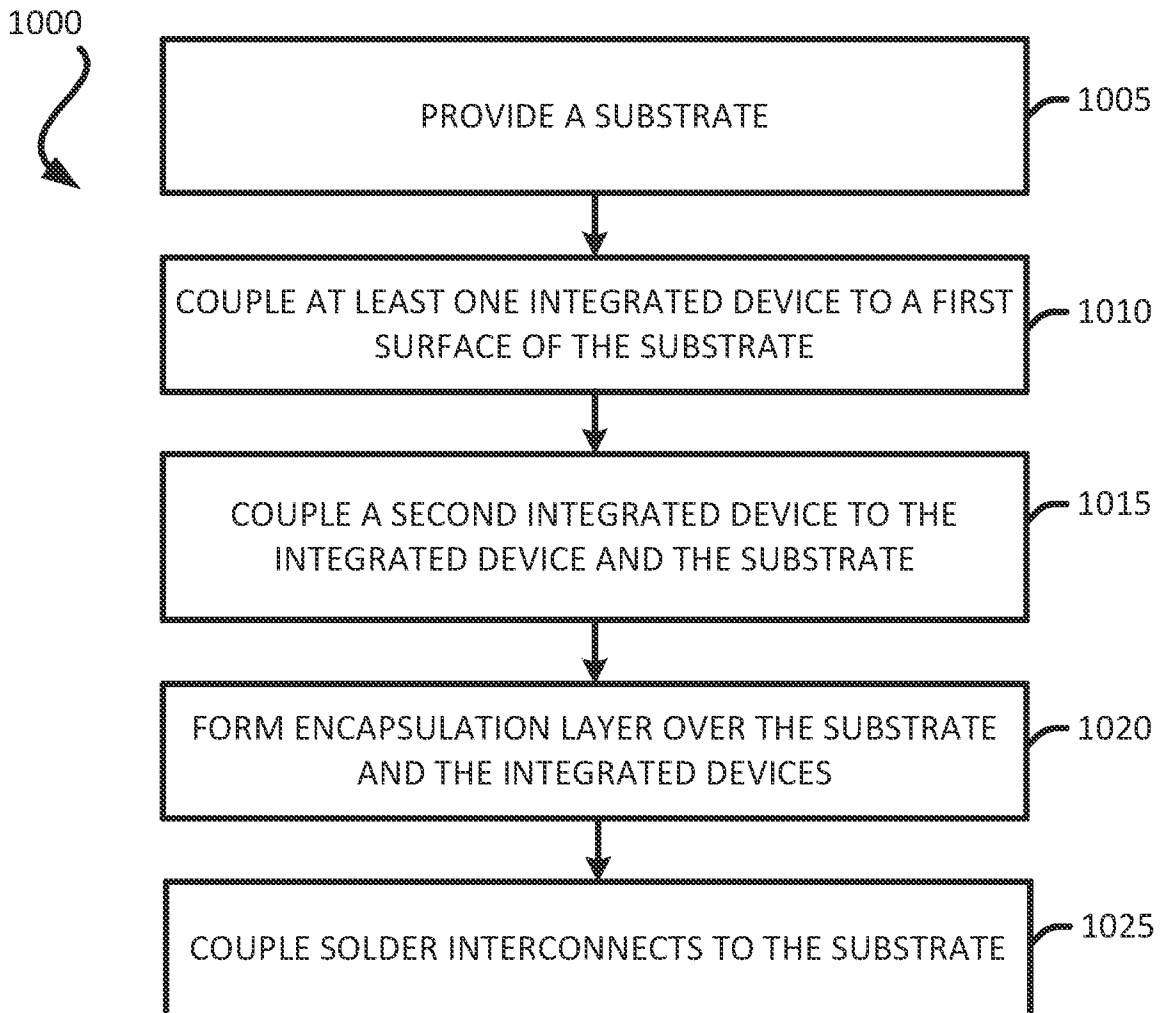


FIG. 10

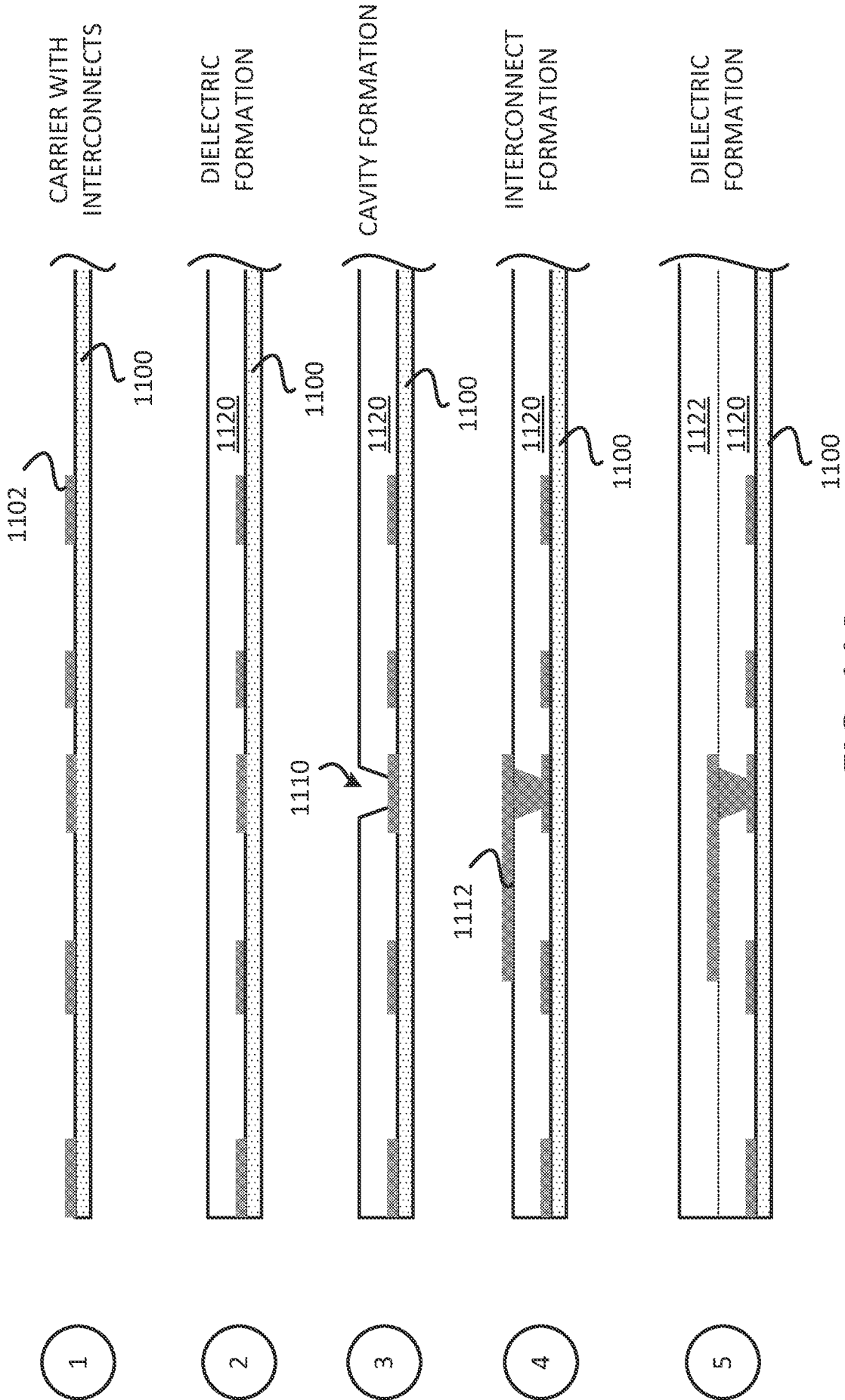


FIG. 11A

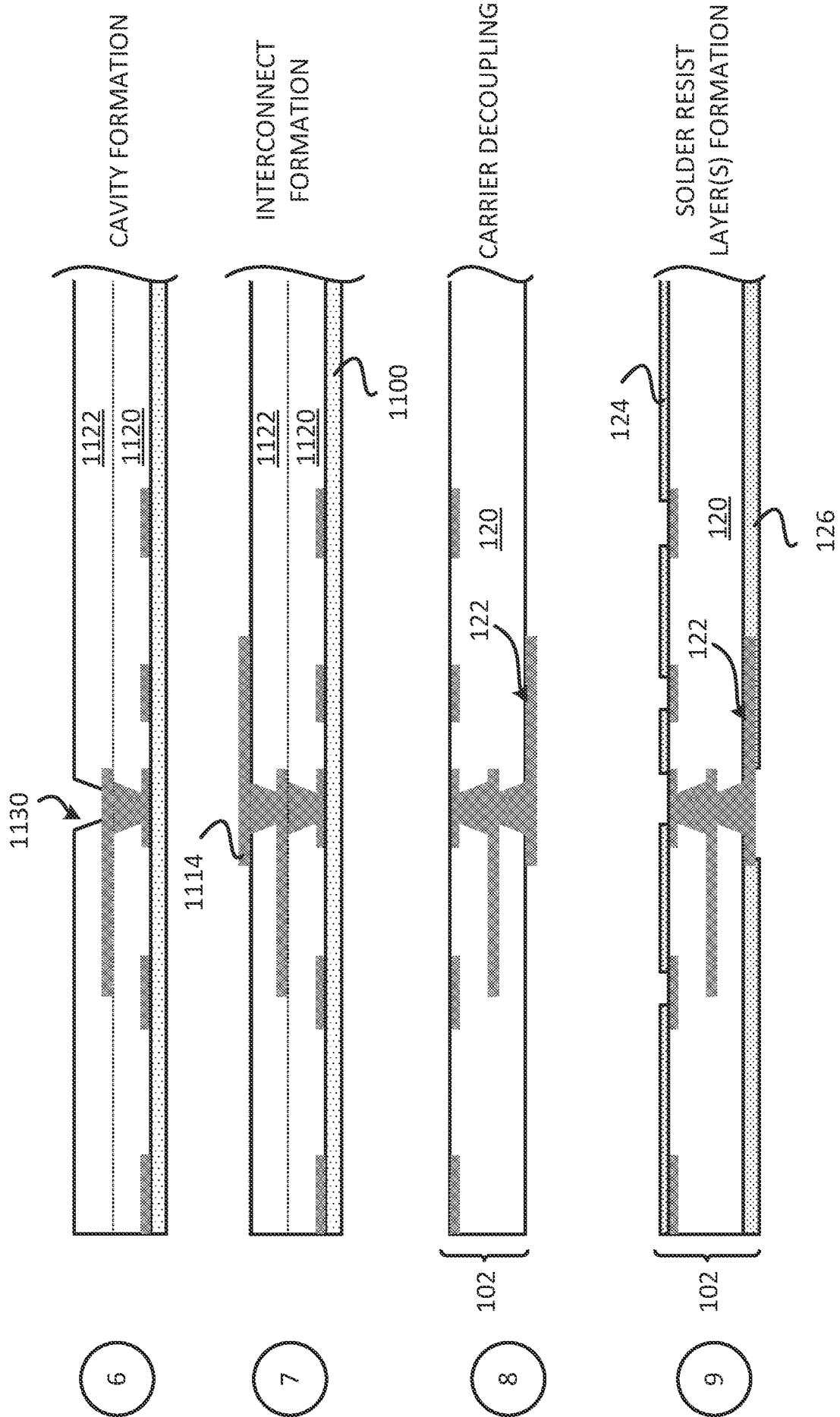


FIG. 11B

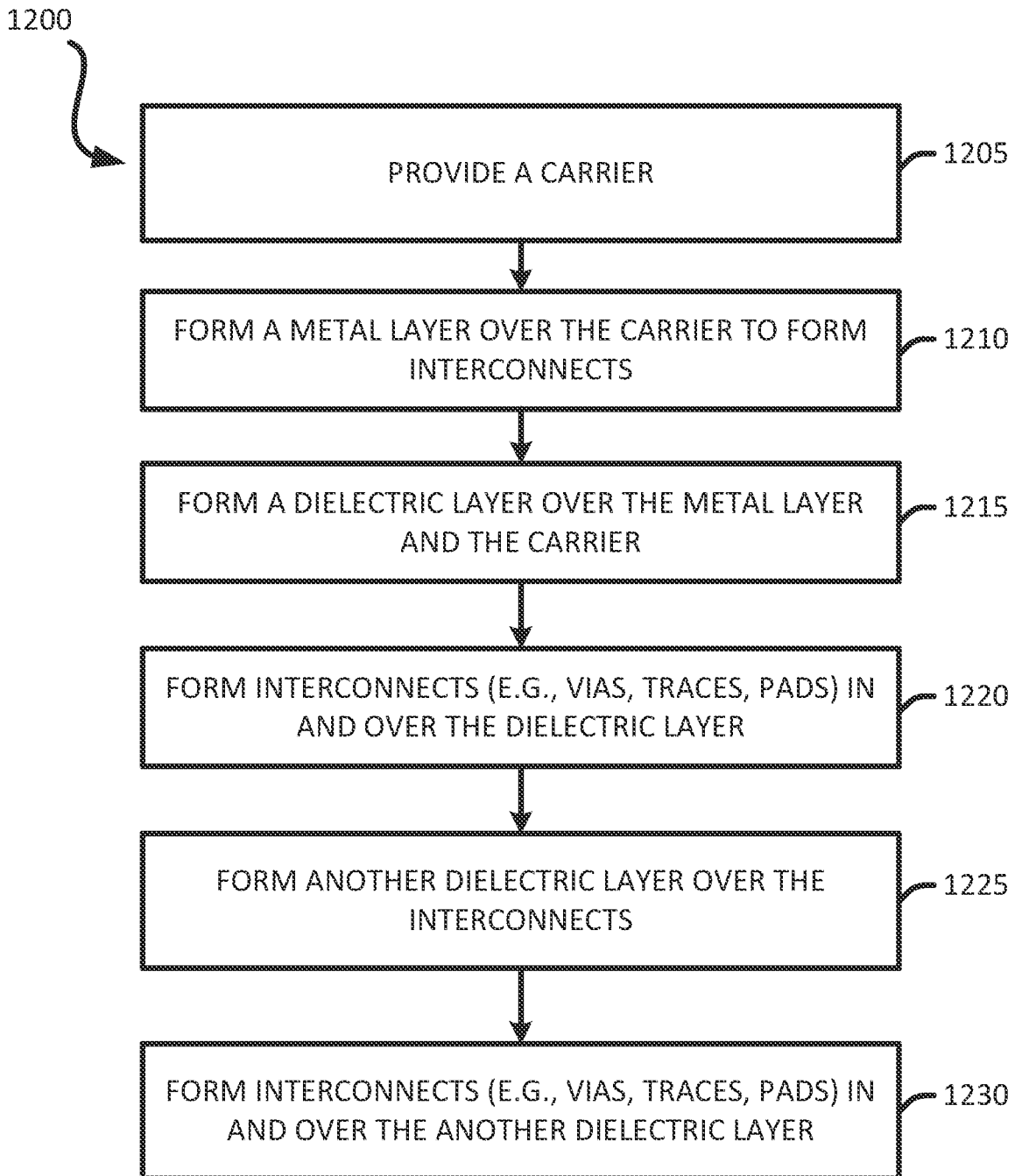


FIG. 12

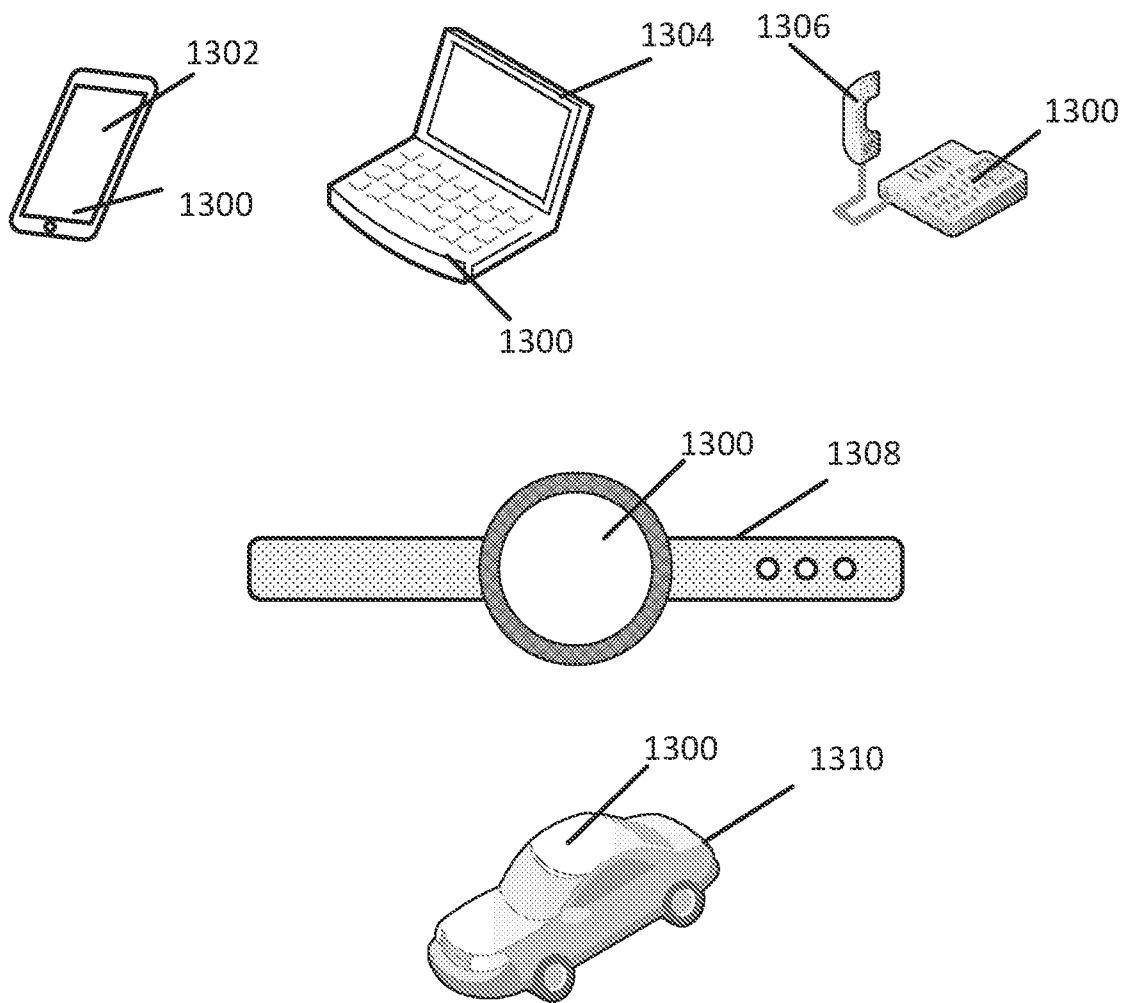


FIG. 13

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2022/033003

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L25/065 H01L23/538
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013/009303 A1 (TSAI PEI-CHUN [TW] ET AL) 10 January 2013 (2013-01-10) figure 1 <p style="text-align: center;">-----</p>	1, 2, 4, 8-13, 17-22, 24-26
X	US 2020/273800 A1 (KIM JONG HOON [KR] ET AL) 27 August 2020 (2020-08-27) figure 1 <p style="text-align: center;">-----</p>	1, 3-8, 11-17, 20-23

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents :

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- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "&" document member of the same patent family

Date of the actual completion of the international search

Date of mailing of the international search report

21 September 2022

29/09/2022

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 Fax: (+31-70) 340-3016

Authorized officer

Kästner, Martin

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2022/033003

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2013009303 A1	10-01-2013	CN 102867800 A	09-01-2013
		KR 20130006260 A	16-01-2013
		TW 201304116 A	16-01-2013
		US 2013009303 A1	10-01-2013

US 2020273800 A1	27-08-2020	CN 111613600 A	01-09-2020
		KR 20200102928 A	01-09-2020
		TW 202036832 A	01-10-2020
		TW 202040769 A	01-11-2020
		US 2020273800 A1	27-08-2020
