A magnetic Tape Peripheral Controller (data link processor, 20t) is used to manage data transfer between a peripheral tape unit (TCU 50t) and a main host computer (10). A buffer memory (22t) in the peripheral controller (20t) is provided with a status counter unit (34c) to monitor the amount of data-in-transit which momentarily resides in the buffer (22). The status counter unit (34c) provides output signals to the peripheral-controller (20t) to elicit action calling for more data from the peripheral tape unit (50tc) or from the host computer (22) or to indicate that the amount of data in the buffer memory was loaded before the main host computer responded to allow the acceptance of it.
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SYSTEM FOR REGULATING DATA TRANSFER OPERATIONS

FIELD OF THE INVENTION

This invention is related to systems where data transfers are effectuated between a peripheral terminal unit and a main host computer wherein an intermediate I/O subsystem is used to perform the housekeeping duties of the data transfer.

BACKGROUND OF THE INVENTION

A continuing area of developing technology involves the transfer of data between a main host computer system and one or more peripheral terminal units. To this end, there has been developed I/O subsystems which are used to relieve the monitoring and housekeeping problems of the main host computer and to assume the burden of controlling a peripheral terminal unit and to monitor control of data transfer operations which occur between the peripheral terminal unit and the main host computer system.

A particular embodiment of such an I/O subsystem has been developed which uses peripheral controllers known as data link processors whereby initiating commands from the
main host computer are forwarded to a peripheral-controller which manages the data transfer operations with one or more peripheral units. In these systems the main host computer also provides a "data link word" which identifies each task that has been initiated for the peripheral-controller. After the completion of a task, the peripheral-controller will notify the main host system with a result/descriptor word as to the completion, incompletion or problem involved in the particular task.

These types of peripheral-controllers have been described in a number of patents issued to the assignee of the present disclosure and these patents are included herein by reference as follows:

U.S. Patent 4,106,092 issued August 8, 1978, entitled "Interface System Providing Interfaces to Central Processing Unit and Modular Processor-Controllers for an Input-Output Subsystem", inventor D.A. Millers, II.

U.S. Patent 4,074,352 issued February 14, 1978, entitled "Modular Block Unit for Input-Output Subsystem", inventors D.J. Cook and D.A. Millers, II.

U.S. Patent 4,162,520 issued July 24, 1979, entitled "Intelligent Input-Output Interface Control Unit for Input-Output Subsystem", inventors D.J. Cook and D.A. Millers, II.


The above patents, which are included herein by reference, provide a background understanding of the use of the type of peripheral-controllers known as "data link processors", DLP, used in a data transfer network between a main host computer and peripheral terminal unit.

In the above mentioned Baun patent, there was described a peripheral-controller which was built of modular components consisting of a common front end control circuit which was of a universal nature for all types of peripheral controllers and which was connected with a peripheral dependent board circuit. The peripheral dependent circuit was particularized to handle the idiosyncrasies of specific peripheral terminal units.

The present disclosure likewise uses a peripheral-controller (data link processor) which follows the general pattern of the above described system, in that the peripheral-controller uses a common control circuit or common front end which works in coordination with a peripheral dependent circuit which is particularly suited to handle a specific type of peripheral terminal unit, such as a Tape Control Unit (TCU) which connects to one or more magnetic tape units.

SUMMARY OF THE INVENTION

The present invention involves a data transfer network wherein a peripheral-controller known as a data link processor is used to manage and control data transfer operations between a peripheral such as a magnetic tape unit...
(or a tape control unit) and the main host computer system, whereby data is transferred rapidly in large blocks, such as a block of 256 words.

The data link processor provides a RAM buffer memory means for temporary storage of data being transferred between peripheral and host system. In this case, the RAM buffer is capable of holding at least six blocks or units of data, each of which consists of 256 words, each word being of 16 bits.

In order to facilitate and control those activities in which (a) data is sometimes being "shifted into" the RAM buffer memory means from either the peripheral unit or from the main host computer and (b) the data in the RAM buffer memory is being "shifted out" either to the magnetic tape unit peripherals, for example, or to the main host computer, it is necessary that the peripheral-controller and the system have data which informs it of the condition of the RAM buffer memory means with regard to the amount of data residing therein at any given period of time.

Thus, there is disclosed a system for regulating data transfer operations between host and peripheral whereby a peripheral-controller senses blocks of data stored in its RAM buffer in order to choose routines for data transfer appropriate to the data condition of the RAM buffer. The peripheral-controller makes use of a block counter monitoring system which will inform the peripheral-controller and the main host system of the "numerical block status" of data in the RAM buffer memory means.

In particular, the present invention discloses a system whereby the common front end (common control) circuit uses routines providing microcode instructions to address registers which access locations in the RAM buffer memory for the insertion of data or the withdrawal of data. There are
two address registers, one for addresses of data taken from/to the peripheral unit and one for addresses of data which are to be forwarded from/to the main host computer.

A block counter logic circuit receives input from the peripheral address register and the system address register. In addition, a flip-flop output to the block counter logic circuit indicates the direction of data flow as being a "Write" (host-to-peripheral) or a "Read" (peripheral-to-Host). The block counter logic circuit provides two output logic signals which control a block counter. This enables the block counter to be shifted up or shifted down so that the internal signal data indicates the number of blocks of data residing in the RAM buffer memory. Certain parameters may be set to trigger signal output conditions when the amount of data in the RAM buffer memory falls below a certain figure.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates the block counter system of the present disclosure which is used to inform the data transfer system of the status of a buffer memory means.

FIG. 2 is a system diagram showing the host computer cooperating with a peripheral-controller in order to control data transfer to and from a peripheral unit.

FIG. 3 is a drawing showing an eight bit shift register which can be shifted up or down according to conditions which occur between certain logic signals and clock signals.

FIG. 4 is a diagram showing how the block counter logic unit of FIG. 1 is organized to operate during Read or Write operations and the effect of either shifting up or shifting down the shift register.

FIG. 5A is a schematic drawing illustrating the significance of each bit-position in the block counter.
FIG. 5B is a chart indicating various "shift" relationships of the block counter with regard to "Read" and "Write" operations.

A "Read" operation takes data from a peripheral magnetic tape unit and temporarily stores it in a RAM memory buffer for later transfer to the host system.

A "Write" operation takes data from the main host system for temporary storage in the RAM buffer memory for subsequent transfer to a selected magnetic tape unit via a TCU or Tape Control Unit.
General System Operation

To initiate an operation, the host system 10, FIG. 2, sends the peripheral-controller (data link processor 20_L) an I/O descriptor and also descriptor link words. The I/O descriptor specifies the operation to be performed. The descriptor link contains path selection information and identifies the task to be performed, so that when a report is later sent back to the main host system 10, the main host system will be able to recognize what task was involved.

After receipt of the I/O descriptor link, the data link processor (DLP) makes a transition to one of the following message level interface states:

(a) Result Descriptor: this state transition indicates that the data link processor 20_L is returning a result descriptor immediately without disconnection from the host computer 10. For example, this transition is used when the DLP detects an error in the I/O descriptor.

(b) DISCONNECT: This state transition indicates that the Magnetic Tape-Data Link Processor (MT-DLP) cannot accept any more operations at this time and that the I/O descriptor and the descriptor link were received without errors. This state also indicates that data transfers or result descriptor transfers can occur.

(c) IDLE: this state transition indicates that the DLP 20_L can accept another legal I/O operation immediately and that the I/O descriptor and the descriptor link were received without errors.

When the operation is completed, the DLP 20_L returns a result descriptor indicating the status of the operation in the main host system. If the DLP detects a parity error on the I/O descriptor or the descriptor link, or if the DLP cannot recognize the I/O descriptor it received, then the DLP
cannot proceed with execution of the operation. In this case, the DLP returns a one-word result descriptor to the host. In all other cases the DLP returns a two-word result descriptor.

The data link processor 20£ is a multiple-descriptor data link processor capable of queuing one I/O descriptor for each magnetic tape unit to which it is connected. There are certain descriptors (Test/Cancel; Test/Discontinue; and Test/ID) which are not queued, but which can be accepted at any time by the DLP. Test/Cancel and Test/Discontinue OPs are issued against a single magnetic tape unit in a queue dedicated to that peripheral unit, and require that an I/O descriptor for that particular magnetic tape unit already be present within the DLP. If an I/O descriptor is received and violates this rule, the DLP immediately returns a result descriptor to the host. This result descriptor indicates "descriptor error" and "incorrect state".

As previously discussed in the referenced patents, the MT-DLP utilizes the following status states (STC) transitions when "disconnected" from the host:

\[
\begin{align*}
    &STC = 3 \text{ to } STC = 1 & \text{IDLE to DISCONNECT} \\
    &STC = 1 \text{ to } STC = 3 & \text{DISCONNECT to IDLE} \\
    &STC = 3 \text{ to } STC = 5 & \text{IDLE to SEND DESCRIPTOR LINK} \\
    &STC = 1 \text{ to } STC = 5 & \text{DISCONNECT to SEND DESCRIPTOR LINK}
\end{align*}
\]

Indicates that the DLP is attempting to process a queued OP.
Indicates that the DLP is prepared to accept a new I/O descriptor.
Indicates that the DLP is executing an OP, and that the DLP requires access to the host computer.
Indicates that the DLP is executing an OP, and that the DLP requires access to the host computer.

The DLP status states can be represented in a shorthand notation such as STC = n.
Upon completion of an I/O operation, the data link processor forms and sends the result descriptor to the host system. This descriptor contains information sent by the tape control unit 50 tc to the DLP in the result status word, and also information generated within the DLP. The result descriptor describes the results of the attempt to execute the operation desired.

**DESCRIPTOR MANAGEMENT**

All communications between the DLP 20 t and the host system 10 are controlled by standard DLP status states as described in the previously referenced patents. These status states enable information to be transferred in an orderly manner. When a host computer 10 connects to the DLP 20 t, the DLP can be in one of two distinct states: (a) ready to receive a new descriptor, or (b) busy.

When in STC = 3 (IDLE), the DLP can accept a new I/O descriptor. When in STC = 1 (DISCONNECT) or in STC = 5 (SEND DESCRIPTOR LINK), then the DLP is busy performing a previously transferred operation.

When the DLP receives an I/O descriptor and descriptor link that does not require immediate attention, the DLP stores the descriptor in its descriptor queue. The DLP is then able to receive another I/O descriptor from the host system.

When the host system 10 "Disconnects" from the DLP 20 t after issuing one or more queued I/O descriptors, then the DLP initiates a search of its descriptor queue. This search continues until the DLP finds an I/O descriptor that needs DLP attention, or until the host "reconnects" to send additional I/O descriptors. If the DLP finds an I/O descriptor that requires attention, and if the descriptor specifies neither a Test/Wait for Unit Available OP, nor a Test/Wait for Unit Not Available OP, then the DLP verifies
that the host is still "disconnected". If these conditions are met, the DLP goes to STC = 1 (DISCONNECT) and initiates execution of the descriptor. Once the DLP goes to STC = 1, then no further I/O descriptors are accepted from the host until the initiated operation has been completed and a result descriptor has been returned to the host.

The DLP searches its descriptor queue on a rotational basis. The order for search is not disturbed by the receipt of one or more new I/O descriptors, nor by the execution of operations. This means that all queued entries are taken in turn regardless of DLP activity and all units have equal priority.

When cleared, the DLP halts all operations in progress with the peripherals and invalidates all the queued I/O descriptors, and returns to Status STC = 3 (IDLE).

**DLP-DATA BUFFERS AND DATA TRANSMISSION**

The data buffer 22 (FIG. 1) of the DLP provides storage for six blocks of data which are used in a "cyclic" manner. Each of the six blocks holds a maximum of 512 bytes of data. Data is transferred to or transferred from the host system one block at a time, via the buffer 22, followed by a longitudinal parity word (LPW). Data is always transferred in full blocks (512 bytes) except for the final block of data for a particular operation. This last block can be less than the 512 bytes, as may be required by the particular operation.

As seen in FIG. 1, logic circuitry (to be described hereinafter) is used to feed information to a block counter 34c which will register the number of blocks of data residing in buffer 22 at any given moment. When certain conditions occur, such as a full buffer, or empty buffer, or "n" number of blocks, the counter 34c can set to trigger a flip-flop 34e which will signal the common control circuit unit 10c to
start routines necessary to either transfer data to the host
10 (after reconnecting to the host) or to get data from the
host 10 to transfer to the buffer 22; or else the unit 10c
5 can arrange to connect the DLP 20t to the peripheral (as tape
control unit 50tc) for receipt of data or for transmission of

Data During a Write operation, the block counter 34c counts
the number of blocks of data received from the host system
10. The data link processor "disconnects" from the host
system once the DLP has received six buffers; or it will
disconnect upon receipt of the "Terminate" command from the
host system (a Terminate indicates the "end" of the Write
data for that entire I/O operation). After disconnecting
from the host, the data link processor connects to the

15 peripheral tape control unit (TCU 50tc). Once proper
connection is established between the data link processor and
the tape subsystem, the data link processor activates logic
which allows the tape control unit 50tc a direct access to
the DLP RAM buffer 22 for use in data transfers.

20 After the data link processor has transmitted one
block of data to the tape control unit, the data link
processor attempts to "reconnect" to the host system by means
of a "poll request" (as long as the host 10 has not
"terminated" the operation). Once this reconnection is

25 established, the host transfers additional data to the data
link processor. This transfer continues until either the six
blocks of RAM buffer memory 22 are again full (a buffer which
is in the process of being transferred to the tape control
unit is considered full during this procedure), or until the
host 10 sends a "Terminate" command. Data transfer

30 operations between the data link processor 20t and the tape
control unit 50tc continue simultaneously with the host data
transfers occurring between host 10 and DLP 20t (via the
buffer 22).
If the data link processor has not successfully reconnected to the host before the DLP has transmitted, for example, three blocks of data to the tape control unit 50_{tc}, the data link processor sets "emergency request" on the data link interface 20_i, FIG. 1. If the "emergency request" is not successfully serviced before the DLP has only one block of data remaining for transmission to the tape control unit, the data link processor sets a "Block Error" condition by signal from flip-flop 34_e to circuit 10_c. This is reported to the host system as a "host access error" in the result descriptor.

The last block of data for any given I/O operation is transferred to the tape control unit 50_{tc} directly under micro-code control. During a "Read" operation, the data link processor first attempts to connect to the tape control unit 50_{tc}. Once a successful connection is accomplished, the data link processor initiates logic to begin accepting data from the tape subsystem. Once the data link processor has received two blocks of data (or once the DLP receives all the data from the operation if the total length is less than two blocks), the data link processor attempts to connect to the host using a "poll request". The data link processor continues to accept tape data while at the same time affecting this host connection.

If the host does not respond to the "poll request" before four blocks of data are present in the DLP RAM buffer 22, the data link processor sets "emergency request" on the data link interface 20_i. If no connection to the host system is effectuated before all of the six RAM buffers are filled, then the data link processor sets "host access error" in the result descriptor.

Once the host system answers a "poll request", the data link processor 20_t starts to send data to the host.
system 10 while at the same time continuing to receive data from the tape control unit 50_{TC}. After the host 10; FIG. 2, has received one block of data, the data link processor checks whether or not two full blocks of data remain to be transferred to the host. If this is so, the DLP uses a "break enable". If a "break enable" request is granted, then transmission of the next data buffer to the host continues to occur. If there are less than two full blocks of data in the RAM buffer 22 (or if the "break enable" is refused), the data link processor disconnects from the host and waits for two full blocks of data to be present. If a "break enable" is refused, the data link processor initiates another "poll request" immediately after disconnection.

When the data link processor has completed data transfer, the tape control unit 50_{TC} enters the result phase and sends two words of result status to the data link processor 20_{t}. The DLP then incorporates this information, plus any internal result flags, into the result descriptor which the DLP then sends to the host.

DESCRIPTION OF PREFERRED EMBODIMENTS

Referring to FIG. 2, the overall system diagram is shown whereby a host computer 10 is connected through an I/O subsystem to a peripheral unit, here, for illustrative purposes, shown as a tape control unit 50_{TC}. This tape control unit (TCU) is used to manage connection to a plurality of Magnetic Tape Unit (MTU) peripherals. As per previous descriptions in the above cited patents which were included by reference, the I/O subsystem may consist of a base module which supports one or more peripheral-controllers, in addition to other connection and distribution circuitry such as the distribution control circuit 20_{OD} and the data link interface 20_{i}. The peripheral-controller 20_{t} is shown in modular form as being
composed of a common front end circuit 10C and a peripheral
dependent circuit shown, in this case, as being composed of
two peripheral dependent boards designated 80p1 and 80p2.

In this network situation, it is often desired that
data from the main host computer be transferred on to a
peripheral unit, such as a magnetic tape unit, for recording
on tape. This would be done via a peripheral tape control
unit TCU such as 50tc. Likewise, at times it is desired that
data from the magnetic tape unit be passed through the tape
control unit to be read out by the host computer. Thus, data
is transferred in a bidirectional sense, that is, in two
directions at various times in the activities of the network.

The key monitoring and control unit is the data link
processor 20t which when initiated by specific commands of
the host computer will arrange for the transfer of the
desired data in the desired direction.

As seen in FIG. 1, the RAM buffer 22 is used for
temporary storage of data being transferred between
peripherals and the main host computer. In the preferred
embodiment this RAM buffer has the capability of storing at
least six "blocks" of data, each block of which consists of
256 words.

Again referring to FIG. 1, a block counter logic unit
33c is used to receive input from two address registers
designated as the peripheral address register, Pa, and the
system address register, Sa. The peripheral address
register, Pa, handles addresses required when data is
retrieved from the peripheral tape unit or when data is being
sent to the peripheral tape unit. The system address
register, Sa, is used when data is being received from the
host system into the buffer 22 when data is being sent to the
host system from the buffer 22. These two address registers
in FIG. 1 are seen to receive their address data via microcode signals from the common front end circuit \(10_C\) of FIG. 1.

The address data outputs from \(P_A\) and \(S_A\) are fed to the RAM buffer 22 in order to address the desired location in the buffer memory. Further, the block counter logic unit 33_\(_C\) receives one input designated "P Carry" from the peripheral address register and another input "S Carry" from the system address register, in addition to a Read/Write control signal from read-write flip-flop 33_f. The flip-flop 33_f is controlled by microcode signals from the peripheral-controller common front end unit \(10_C\). The block counter logic unit 33_\(_C\) provides a first logic signal \(L_S1\) and a second logic signal \(L_S0\) which are fed to OR gates \(G_1\) and \(G_0\). These gates also have additional inputs from the microcode of the common front end card \(10_C\) which inputs can be used to simulate the \(L_S1\) and \(L_S0\) signals for diagnostic or other control purposes. The OR gates provide two output signals designated \(S_1\) and \(S_0\) which are fed to the block counter 34_\(_C\). As will be seen in FIG. 3, the output signals \(S_1\) and \(S_0\) are combined at certain times on occurrence of rising clock signals in order to provide conditions which will make the block counter either "shift up" or "shift down" or "no shift".

Referring to FIG. 3, there is seen a schematic drawing which illustrates the use of the block counter 34_\(_C\) of FIG. 1.

Referring to FIG. 3, there is seen, schematically, an eight bit shift register which will be affected at selected points in time where the clock signal is in its "rising" state as illustrated by the arrows shown in FIG. 3.

Referring to the leftmost schematic of the shift register, it will be seen that there are two "ones" which illustrate that the RAM buffer 22 has been loaded with two full blocks of
data. At time $T_1$ it will be seen that conditions are such that "no shift" has occurred and the two "ones" remain in the shift register. At time $T_2$ there is a "shift up" and the shift register now has three bits with the "1" signal. At time $T_3$ there is a "shift down" signal and the shift register is back where two bit positions include a "1". At time $T_4$ there is a "shift up" and the shift register now has three bit positions manifesting the "1" signal, which indicates three full blocks of data residing in buffer 22 at that moment.

Referring to FIG. 4, there is seen a chart whereby the block counter logic unit 33C is organized to show overall operating conditions. Thus, as seen in the FIG. 4 chart, the conditions of the S Carry and P Carry during the "Read" condition show that there is a no shift or no change when S Carry and P Carry are the same, that is to say they are both 0 or they are both 1.

However, when S Carry is "0" and the P Carry is equal to "1", then there is an up shift, while if the S Carry is "1" and the P Carry is "0", there is a down shift during "Read" operations.

Referring to FIG. 4, it is seen that during "Write" operations, again when the S Carry and the P Carry are equal (both "0" or both "1") to each other, then there is no change or shift in the shift register. However, when the S Carry equals "0" and the P Carry equals "1" there is a down shift in this situation, and when the S Carry is equal to "1" and the P Carry is equal to "0" there is an up shift.

The block counter 34C will reflect the situation that when data is being taken out of the magnetic tape unit in order to be fed to RAM buffer 22 ("Read" operation), the block counter will shift up unless at the same time there is data being removed from buffer 22 for transfer to the main
host computer system in which case the block counter will shift down. Thus, the condition of the block counter's numerical status will indicate the "balance" between what data has gone out of and what data has come into the buffer 22.

Referring to FIG. 4, if there is a "Write" operation, this determines that data is to be written into the magnetic tape unit. Then, as data is removed from the RAM buffer over to the magnetic tape unit, the block counter will shift down but if more data is transferred from the main host computer into the RAM buffer 22, the block counter will be shifted up. Thus, again the placement of "ones" in various bit positions provides a running balance of the data blocks taken out as against the data blocks taken in at any given period.

Referring to FIG. 4 there are certain logic equations which indicate the logic used in the block counter logic unit 33c.

In the following logic equations it should be indicated that the asterisk refers to AND logic operation while the plus sign refers to OR logic operation.

(a) If signal counter S₁ equals "1" and signal S₀ equals "0", there occurs what may be called a condition of "Up enable" which is equal to (Read * S Carry * P Carry) + (Write * S Carry * P Carry).

(b) Under the conditions where the signal S₁ equals "0" and the signal S₀ equals "1", this could be considered as a "Down enable" which is equal to (Read * S Carry * P Carry) + (Write * S Carry * P Carry).

(c) In the condition where the signal S₁ equals "0" and the signal S₀ equals "0", there is the condition called "no change". This is equal to (Read * S Carry * P Carry) + (Write * S Carry * P Carry).
(d) The condition known as the "host access error", \( H_e \), causes the setting of a flip-flop \( 34_e \), FIG. 1. (This is also called a block counter error). Thus, the host access error signal or block counter error signal is a result of:

\[
H_e = (\text{Read} \times 6 \text{ BLKFUL}) + (\text{Write} \times 1 \text{ BLKFUL}).
\]

Thus, on a Read operation, a full RAM buffer (six blocks of data) will signal an error condition.

Likewise, on a Write operation, a single (one) remaining block of data will trigger an error condition.

Referring to FIG. 5A, a schematic drawing of the block counter \( 34_c \) is shown to indicate that when a "1" resides in a series of bit positions, it is an indication of how many blocks of data reside in the RAM buffer 22 (FIG. 1).

For example, if a "1" resides in each of bit positions 1, 2, 3, 4, this indicates that "4 blocks" of data reside in RAM 22. Each "block" consists of 256 words (512 bytes of eight bits each).

In FIG. 5B the chart illustrates that during "Read" operations:

(a) As the P Carry increases (data being transferred from peripheral tape to buffer memory 22), the block counter \( 34_c \) will "shift up" indicating the buffer is being "loaded".

(b) As the S Carry increases (data from buffer memory being transferred to main host system), the block counter \( 34_c \) will "shift down" indicating the buffer memory is being "emptied".

In FIG. 5B the chart illustrates that during "Write" operations:

(c) As S Carry increases (data being loaded in buffer memory from main host system), the block counter \( 34_c \) will "shift up" to indicate the number of blocks of data in the buffer.
(d) As P Carry increases (data in buffer being unloaded for transfer to peripheral tape unit), the block counter $34_3$ will "shift down" and show how much data is left remaining in buffer 22.

In FIG. 5B, during "Read" operations, when a "1" appears in the 6th bit position of block counter $34_3$, then a flip-flop circuit $34_e$ (FIG. 1) is "set" and provides a signal to the common front end circuit $10_3$ which will inform the main system of an "access-error" condition. This signifies that the buffer memory 22 was "overfilled" in that the main host system did not accept data quickly enough.

During "Write" operations, when the buffer memory 22 has received six blocks of data from the host system, and the 1st bit position (1 BLKFUL) becomes "0", this indicates that the buffer memory has been completely unloaded (cleared) and then the flip-flop $34_e$ is set to signal the common front end circuit $10_3$ that more data is required from the host. This indicates the host did not supply data quickly enough to the RAM buffer 22.

There has been thus described a system for the control of data transfers which is sensitive to the condition of the data-in-transit residing in a RAM buffer memory and by which it is possible to monitor blocks of data being transferred between peripheral units and a main host computer when there are simultaneous flows of data being put into or taken out of the RAM buffer means.

While the disclosure herein illustrates one embodiment of the described system, the described system is not to be deemed limited to but rather to embrace those systems as defined in the following claims.
What is claimed is:

1. In a network wherein data is transferred between a main host computer and a magnetic tape peripheral unit via a peripheral-controller, wherein said peripheral-controller is initiated by commands from said host computer to execute data transfer operations and said peripheral-controller includes a common control circuit unit for sequencing microcode instructions and a peripheral dependent circuit unit for managing said tape peripheral unit, the system for regulating data transfer operations comprising:

   (a) buffer memory means in said peripheral-controller for temporarily storing blocks of data being transferred, said buffer memory means having channels of connection to said tape peripheral unit and said host computer;

   (b) status means in said peripheral dependent circuit unit for providing information data for indicating the number of blocks of data residing in said buffer memory means;

   (c) signal output means connected to said status means and functioning to provide status signals to said common control circuit unit.

2. The system of claim 1, wherein said host system initiates a Write operation command to said peripheral-controller to transfer data from main host computer, and said common control circuit unit initiates routines to transfer data from said host computer to said buffer memory means.
3. The system of claim 2, wherein said status means includes:
   (a) shift register means which shifts up to count the number of blocks of data received into said buffer memory means.

4. The system of claim 3 wherein, when said buffer memory is filled with blocks of data from said host computer, said shift register causes said signal output means to pass information data to said common control circuit unit; and wherein said common control circuit unit disconnects said host computer from said buffer memory means.

5. The system of claim 4 wherein, after disconnection of said host computer, said common control circuit unit connects said peripheral tape unit to said buffer memory means.

6. The system of claim 5 wherein, upon connection of said peripheral tape unit to said buffer memory means, said common control circuit unit causes execution of data transfer from said buffer memory means to said peripheral tape unit.

7. The system of claim 6 wherein said shift register shifts down each time a block of data is removed from said buffer memory means to said peripheral tape unit.

8. The system of claim 7 wherein, when said shift register is reduced by one block count, said signal output means will pass information to said common control circuit causing it to reconnect to said main host computer for enablement of more data transfer to said buffer memory means.
9. The system of claim 1, wherein said host system initiates a Read operation command to said peripheral-controller to transfer data from said peripheral tape unit to said buffer memory means.

10. The system of claim 9, wherein said status means includes:
   (a) shift register means which operates to shift up one unit for each block of data received by said buffer memory means from said peripheral tape unit.

11. The system of claim 10 wherein, when said shift register means indicates two blocks of data have been received, said signal output means provides a signal to said common control circuit unit causing said buffer memory means to be connected to said main host computer.

12. The system of claim 11, wherein data is simultaneously transferred from said peripheral tape unit to said buffer memory means, and also from said buffer memory means to said main host computer.

13. The system of claim 12, wherein said shift register shifts up for each data block received by said buffer memory means, and said shift register shifts down for each block of data transferred to said main host computer.
FIG. 3.  8-Bit Shift Register.
FIG. 4

<table>
<thead>
<tr>
<th>$S_{CARRY}$</th>
<th>$P_{CARRY}$</th>
<th>READ</th>
<th>WRITE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>NO SHIFT</td>
<td>NO SHIFT</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>UP</td>
<td>DOWN</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>DOWN</td>
<td>UP</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>NO CHANGE</td>
<td>NO CHANGE</td>
</tr>
</tbody>
</table>

$S_1 = 1$ UP $= (READ * S_{CARRY} * P_{CARRY}) +$

$S_0 = 0$ ENABLE $= (WRITE * S_{CARRY} * P_{CARRY})$

$S_1 = 1$ DOWN $= (READ * S_{CARRY} * P_{CARRY}) +$

$S_0 = 0$ ENABLE $= (WRITE * S_{CARRY} * P_{CARRY})$

$S_1 = 0$ NO CHANGE $= \text{for}(READ * S_{CARRY} * P_{CARRY})$

$S_0 = 0$ NO CHANGE $= \text{for}(WRITE * S_{CARRY} * P_{CARRY})$

HOST ACCESS ERROR OR BLOCK COUNTER ERROR

NOTE: + = OR  \* = AND
**FIG. 5A.**

**BLOCK COUNTER**

```
<table>
<thead>
<tr>
<th></th>
<th>0</th>
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<tbody>
<tr>
<td>DOWN</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>WHEN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S1 = 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S0 = 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>&quot;O&quot;</td>
<td>B</td>
<td>B</td>
</tr>
<tr>
<td>&quot;1&quot;</td>
<td>F</td>
<td>B</td>
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```

**FIG. 5B.**

<table>
<thead>
<tr>
<th>READ</th>
<th>WRITE</th>
</tr>
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<tbody>
<tr>
<td>SCRY ⇒ SCR8</td>
<td>SHIFT DOWN</td>
</tr>
<tr>
<td>PCRY ⇒ PCR8</td>
<td>SHIFT UP</td>
</tr>
<tr>
<td>SCRY ⇒ SCR8</td>
<td>S1 = S0 = 1</td>
</tr>
<tr>
<td>PCRY ⇒ PCR8</td>
<td>NO SHIFT</td>
</tr>
<tr>
<td>IN THE SAME CLOCK CYCLE</td>
<td></td>
</tr>
<tr>
<td>INITIALLY</td>
<td>CLEARED</td>
</tr>
<tr>
<td>HOST ACCESS ERROR CONDITION WILL BE SET</td>
<td>WHEN 6BLKFUL BECOMES &quot;1&quot;</td>
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### INTERNATIONAL SEARCH REPORT

**International Application No.** PCT/US83/01915

#### I. CLASSIFICATION OF SUBJECT MATTER

According to International Patent Classification (IPC) or to both National Classification and IPC

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<tr>
<th>INT. CL</th>
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#### II. FIELDS SEARCHED

Minimum Documentation Searched

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Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched

#### III. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of Document, 14 with indication, where appropriate, of the relevant passages 17</th>
<th>Relevant to Claim No. 16</th>
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<tr>
<td>A</td>
<td>US, 4,357,681, (Chadra et al) 02 November 1982</td>
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<td>A</td>
<td>US, 4,040,037, (Lawlor) 02 August 1977</td>
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* Special categories of cited documents:
  - "A" document defining the general state of the art which is not considered to be of particular relevance
  - "E" earlier document but published on or after the international filing date
  - "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
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**"X"** document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

**"Y"** document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

**"W"** document member of the same patent family

#### IV. CERTIFICATION

Date of the Actual Completion of the International Search 5

13 February 1984

Date of Mailing of this International Search Report 8

23 Feb 1984

International Searching Authority 1

Signature of Authorized Officer 20

ISA/US

Form PCT/ISA/210 (second sheet) (October 1981)
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<td>A</td>
<td>US, 4,177,515, (Jenkins et al) 04 December 1979</td>
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