

(19)



**Octrooi­centrum
Nederland**

(11)

2019845

(12) B1 OCTROOI

(21)

Aanvraagnummer: **2019845**

(51)

Int. Cl.:

H01L 29/78 (2018.01) **H01L 29/06** (2018.01) **H01L 29/08** (2018.01)

(22)

Aanvraag ingediend: **2 november 2017**

(30)

Voorrang:

11 november 2016 JP PCT/JP2016/083604
17 maart 2017 JP PCT/JP2017/011066

(73)

Octrooihouder(s):

Shindengen Electric Manufacturing Co., Ltd
te Tokyo, Japan, JP.

(41)

Aanvraag ingeschreven:

23 mei 2018

(72)

Uitvinder(s):

Daisuke Arai te Hanno-shi (JP).
Mizue Kitada te Hanno-shi (JP).

(43)

Aanvraag gepubliceerd:

25 mei 2018

(47)

Octrooi verleend:

12 oktober 2018

(74)

Gemachtigde:

mr. drs. A.J.W. Hooiveld c.s. te Den Haag.

(45)

Octrooischrift uitgegeven:

11 januari 2019

(54)

MOSFET and power conversion circuit

(57)

A MOSFET 100 according to the present invention includes:

a semiconductor base substrate 110 having a super junction structure 117; and a gate electrode 126 formed on a first main surface side of the semiconductor base substrate 110 by way of a gate insulation film 124. In a graph where a depth x at a predetermined depth position in the super junction structure 117 is taken on an axis of abscissas, and an average positive charge density $p(x)$ at the predetermined depth position in the super junction structure 117 is taken on an axis of ordinates, the average positive charge density $p(x)$ at a predetermined depth position of the super junction structure 117 when the super junction structure 117 is depleted by turning off the MOSFET is expressed by an upward convex curve projecting in a right upward direction. According to MOSFET 100 of the present invention, even when an irregularity exists in a charge balance around a gate, an irregularity in switching characteristics when the MOSFET is turned off can be decreased compared to a prior art.

DESCRIPTION

Title of the Invention:

MOSFET and power conversion circuit

5

Technical Field

[0001]

The present invention relates to a Metal-Oxide
Semiconductor Field-Effect Transistor (MOSFET) and a power
10 conversion circuit.

Background Art

[0002]

Conventionally, there has been known a MOSFET which
includes a semiconductor base substrate having a super junction
15 structure which is formed of an n-type column region and a
p-type column region (see patent document 1, for example).

[0003]

In this specification, "super junction structure" means
a structure where an n-type column region and a p-type column
20 region are alternately and repeatedly arranged as viewed in
a predetermined cross section.

[0004]

As shown in Fig. 17, a conventional MOSFET 900 is a
planar-gate-type MOSFET which includes: a semiconductor base
25 substrate 910 having a super junction structure 917 formed of

an n-type column region 914 and a p-type column region 916,
a base region 918 formed on a surface of a first main surface
and a whole surface of the p-type column region 916 and a part
of a surface of the n-type column region 914, an n-type surface
5 high concentration region 919 formed on the surface of the first
main surface and the surface of the n-type column region 914
such that the n-type surface high concentration region 919 is
disposed adjacently to the base region 918, and an n-type source
region 920 formed on a surface of the base region 918; and a
10 gate electrode 936 formed on the surface of the base region
918 sandwiched between the source region 920 and the n-type
surface high concentration region 919 by way of a gate
insulation film 93.

[0005]

15 In the conventional MOSFET 900, the n-type column region
914 and the p-type column region 916 are formed such that a
total amount of a dopant in the n-type column region 914 is
equal to a total amount of a dopant in the p-type column region
916. That is, the n-type column region 914 and the p-type
20 column region 916 are well-balanced with each other in terms
of a charge. Both dopant concentration in the n-type column
region 914 and dopant concentration in the p-type column region
916 are set to a fixed value regardless of a depth of the n-type
column region 914 and a depth of the p-type column region 916.
25 Further, side walls of the n-type column region 914 are formed

in a tapered shape narrowed toward a first main surface side,
and side walls of the p-type column region 916 are formed in
a tapered shape with a narrow bottom.

[0006]

5 In the specification, "total amount of a dopant" means
a total amount of a dopant in a constitutional element (the
n-type column region or the p-type column region) in the MOSFET.

[0007]

 According to the conventional MOSFET 900, the MOSFET
10 includes the semiconductor base substrate 910 having the super
junction structure 917 which is formed of the n-type column
region 914 and the p-type column region 916 and hence, it is
possible to provide a switching element having a low ON
resistance and a high withstand voltage.

15 Prior Art Document

Patent Document

[0008]

Patent document 1: JP-A-2004-119611

Patent document 2: JP-A-2013-93560

20 Summary of Invention

Problem to be solved by the invention

[0009]

 In the conventional MOSFET 900, there exists a drawback
that when there is an irregularity in a charge balance around
25 a gate, an irregularity in switching characteristics when the

MOSFET is turned off becomes large.

[0010]

Accordingly, the present invention has been made so as to overcome the above-mentioned drawback, and it is an object of the present invention to provide a MOSFET and a power conversion circuit which uses the MOSFET where an irregularity in switching characteristics when the MOSFET is turned off can be decreased compared to a prior art even when an irregularity in a charge balance occurs around the gate.

10 Solution to Problem

[0011]

[1] According to the present invention, there is provided a MOSFET which includes: a semiconductor base substrate having the super junction structure which is formed of an n-type column region and a p-type column region; and a gate electrode formed on a first main surface side of the semiconductor base substrate by way of a gate insulation film, wherein

using a deepest position of a surface of a depletion layer on the first main surface side when the depletion layer extends most in the super junction structure by turning off the MOSFET as a reference, in a graph where a depth x at a predetermined depth position in the super junction structure when the super junction structure is depleted by turning off the MOSFET is taken on an axis of abscissas, and an average positive charge density $\rho(x)$ at the predetermined depth position in the super

junction structure expressed by a following formula (1) when the super junction structure is depleted by turning off the MOSFET is taken on an axis of ordinates,

the average positive charge density $\rho(x)$ is expressed
 5 by an upward convex curve projecting in a right upward direction, and

using a deepest position of a surface of a depletion layer on the first main surface side when the depletion layer extends most in the super junction structure by turning off the MOSFET
 10 as a reference, assuming a depth of a surface of the depletion layer on a second main surface side at a shallowest position when the depletion layer extends most in the super junction structure by turning off the MOSFET as a,

a value of the average positive charge density $\rho(0)$ when
 15 $x=0$ becomes a negative value and a value of the average positive charge density $\rho(a)$ when $x=a$ becomes a positive value, and

an area of a region surrounded by a curve which expresses the average positive charge density $\rho(x)$, a straight line where $x=0$ and the axis of abscissas is equal to an area of a region
 20 surrounded by the curve which expresses the average positive charge density $\rho(x)$, a straight line where $x=a$ and the axis of abscissas.

[Formula 1]

$$\rho(x) = \frac{q}{2w} \left[w_n(x) \cdot N_d(x) - w_p(x) \cdot N_a(x) \right] \cdot \cdot \cdot (1)$$

(In the formula (1), $w_n(x)$ indicates a width of the n-type column region at the predetermined depth position, $N_d(x)$ indicates average density of a positive charge at the predetermined depth position in the n-type column region when the super junction structure is depleted by turning off the MOSFET, $w_p(x)$ indicates a width of the p-type column region at the predetermined depth position, $N_a(x)$ indicates average density of a negative charge at the predetermined depth position in the p-type column region when the super junction structure is depleted by turning off the MOSFET, q indicates an elementary charge, and w indicates a positive constant which satisfies $w_n(x) + w_p(x) = 2w$.)

[0012]

In this specification, "a depth at a predetermined depth position in the super junction structure" means a depth at a predetermined depth position in the super junction structure using a deepest position of a surface of a depletion layer on the first main surface side when the depletion layer extends most in the super junction structure by turning off the MOSFET as a reference. Accordingly, the depth x becomes 0 at the deepest position of the surface of the depletion layer on the first main surface side when the depletion layer extends most in the super junction structure by turning off the MOSFET. "second main surface" means a main surface on a side opposite to the first main surface. "average density of a positive

charge at the predetermined depth position in the n-type column region" means average density of a positive charge generated by a donor in the n-type column region when the n-type column region is depleted by turning off the MOSFET, and "average
5 density of a negative charge at the predetermined depth position in the p-type column region" means average density of a negative charge generated in an acceptor of the p-type column region when the p-type column region is depleted by turning off the MOSFET. Further, "average positive charge
10 density $\rho(x)$ at a predetermined depth position of the super junction structure is expressed by an upward convex curve projecting in a right upward direction" means not only the case where the average positive charge density is expressed by a monotonous upward convex curve projecting in a right upward
15 direction but also a case where the average positive charge density is expressed in a stepped shape (a line (an envelope) which connects corner portions of steps forming a monotonous upward convex curve projecting in a right upward direction), and a case where the average positive charge density is formed
20 of a curve where a concave shape and a convex shape are repeated (an envelope forming a monotonous upward convex curve projecting in a right upward direction).

[0013]

[2] According to the MOSFET of the present invention,
25 it is preferable that using a deepest position of a surface

of a depletion layer on the first main surface side when the depletion layer extends most in the super junction structure by turning off the MOSFET as a reference, assuming a depth of a surface of the depletion layer on the second main surface side at a shallowest position when the depletion layer extends most in the super junction structure by turning off the MOSFET as a, and a depth of a depth position where the average positive charge density $\rho(x)$ becomes 0 in the super junction structure as d, a relationship of $0 < d < a/2$ be satisfied.

10 [0014]

[3] According to the MOSFET of the present invention, it is preferable that in a graph where the depth x at the predetermined depth position in the super junction structure is taken on an axis of abscissas, and a width $w_n(x)$ at the predetermined depth position in the n-type column region or a width $w_p(x)$ at the predetermined depth position in the p-type column region is taken on an axis of ordinates,

the width $w_n(x)$ at the predetermined depth position in the n-type column region be expressed by an upward convex curve projecting in a right upward direction, and

the width $w_p(x)$ at the predetermined depth position in the p-type column region be expressed by a downward convex curve projecting in a right downward direction.

[0015]

25 [4] According to the MOSFET of the present invention,

it is preferable that in a graph where the depth x at the predetermined depth position in the super junction structure is taken on an axis of abscissas, and average density $N_d(x)$ of a positive charge at the predetermined depth position in the n-type column region or average density $N_a(x)$ of a negative charge at the predetermined depth position in the p-type column region when the super junction structure is depleted by turning off the MOSFET is taken on an axis of ordinates,

average density $N_d(x)$ of a positive charge at the predetermined depth position in the n-type column region when the super junction structure is depleted by turning off the MOSFET be expressed by an upward convex curve projecting in a right upward direction, and

average density $N_a(x)$ of a negative charge at the predetermined depth position in the p-type column region when the super junction structure is depleted by turning off the MOSFET be expressed by a downward convex curve projecting in a right downward direction.

[0016]

[5] According to the MOSFET of the present invention, it is preferable that the semiconductor base substrate further have a p-type base region formed on a surface of the n-type column region and a surface of the p-type column region, and an n-type source region formed on a surface of the base region,

the MOSFET further include, in a region where the n-type

column region is positioned as viewed in a plan view, a trench formed so as to extend from a surface of a first main surface of the semiconductor base substrate to a depth position deeper than a deepest portion of the base region and a portion of the source region be exposed on an inner peripheral surface of the trench,

the gate insulation film be formed on the inner peripheral surface of the trench, and

the gate electrode be embedded in the trench by way of the gate insulation film.

[0017]

[6] According to the MOSFET of the present invention, it is preferable that the semiconductor base substrate further have: a base region formed on a surface of the first main surface of the semiconductor base substrate, a whole surface of the p-type column region, and a portion of a surface of the n-type column region; an n-type surface high concentration region formed on a surface of the first main surface of the semiconductor base substrate and a surface of the n-type column region such that the n-type surface high concentration region is formed adjacently to the base region; and an n-type source region formed on a surface of the base region, and

the gate electrode be formed on a surface of the base region sandwiched between the source region and the n-type surface high concentration region by way of the gate insulation

film.

[0018]

[7] According to the MOSFET of the present invention, it is preferable that using a deepest position of a surface of a depletion layer on the first main surface side when the depletion layer extends most in the super junction structure by turning off the MOSFET as a reference, in a graph where an axis along a depth direction is set as an x axis, an x coordinate at a depth position of a lowermost surface of the base region is set as $-t$, an x coordinate at depth position of a lowermost portion of the p-type column region is set as b , and an x coordinate at a depth position where the average positive charge density $\rho(x)$ becomes 0 is set as d , a relationship of $0 < t + d < (t + b) / 2$ be satisfied.

15 [0019]

[8] According to the present invention, there is provided a power conversion circuit which includes at least: a reactor; a power source which supplies an electric current to the reactor; the MOSFET according to any one of [1] to [7] for controlling an electric current supplied from the power source to the reactor; and a rectifier element which performs a rectifying operation of the electric current supplied from the power source to the reactor or an electric current from the reactor.

25 [0020]

[9] According to the power conversion circuit of the present invention, it is preferable that the rectifier element be a fast recovery diode.

[0021]

5 [10] According to the power conversion circuit of the present invention, it is preferable that the rectifier element be a built-in diode of the MOSFET.

[0022]

10 [11] According to the power conversion circuit of the present invention, it is preferable that the rectifier element be a silicon-carbide Schottky barrier diode.

[Advantageous effects of the present invention]

[0023]

According to the MOSFET and the power conversion circuit
15 of the present invention, average positive charge density $\rho(x)$ at a predetermined depth position of the super junction structure when the super junction structure is depleted by turning off the MOSFET is expressed by an upward convex curve projecting in a right upward direction. With such a
20 configuration, in a depth position around the gate (a region where x is close to 0), the average positive charge density $\rho(x)$ becomes smaller than (larger on a negative side) a conventional MOSFET 900, and the difference between a charge amount of a negative charge in the p-type column region and
25 a charge amount of a positive charge in the n-type column region

becomes large compared to the conventional MOSFET 900. Accordingly, the following advantages can be acquired.

(1) The n-type column region around the gate becomes easily depleted compared to the conventional MOSFET 900 and hence, even when a drain voltage is increased, a potential of the n-type column region around the gate is minimally increased.

(2) A distance between a non-depleted region in the n-type column region and the gate electrode becomes long compared to the conventional MOSFET 900 and hence, a feedback capacitance C_{rss} (equal to a gate-drain capacitance C_{gd}) becomes small compared to the conventional MOSFET 900. Accordingly, even when a potential of the n-type column region (the non-depleted region of the n-type column region) is increased along with the increase of a drain voltage which takes place when the MOSFET is turned off, the gate electrode is minimally affected by a change in potential of the n-type column region. As a result, even when an irregularity exists in a charge balance around the gate, an irregularity in switching characteristics when the MOSFET is turned off can be reduced compared to the prior art.

[0024]

Further, according to the MOSFET of the present invention, average positive charge density $\rho(x)$ at a predetermined depth position of the super junction structure when the super

junction structure is depleted by turning off the MOSFET is expressed as an upward convex curve projecting in a right upward direction. With such a configuration, at a depth position around the gate, an average positive charge density $\rho(x)$ becomes small (large on a negative side) and hence, a charge amount of a negative charge in the p-type column region becomes larger than a charge amount of a positive charge in the n-type column region. Accordingly, holes around the gate in the p-type column region can be easily extracted by a negative charge in the p-type column region. As a result, an L-load avalanche breakdown resistance can be increased compared to a prior art.

[0025]

Further, the MOSFET according to the present invention includes the semiconductor base substrate where the super junction structure is formed of the n-type column region and the p-type column region. Accordingly, in the same manner as the conventional MOSFET 900, the MOSFET becomes a switching element having a low ON resistance and a high withstand voltage.

[0026]

In the MOSFET according to the present invention, the average positive charge density $\rho(0)$ when $x=0$ takes a negative value, and the average positive charge density $\rho(a)$ when $x=a$ takes a positive value. Accordingly, at a depth position in the vicinity of a bottom portion of the p-type column region,

a total amount of a dopant in the p-type column region becomes smaller than a total amount of a dopant in the n-type column region (becoming n-type dopant rich). With such a configuration, a depletion layer generated from the p-type column region when the MOSFET is turned off minimally extends toward a second main surface side. Accordingly, it is possible to provide an MOSFET where a breakdown in a reach through mode minimally occurs so that a withstand voltage is minimally lowered.

10 [0027]

Patent document 2 discloses a MOSFET 902 where a width of the p-type column region 816 is increased from a center portion to a bottom portion of the p-type column region 816 in a depth direction (see Fig. 18). However, an average positive charge density $\rho(x)$ of a MOSFET 902 according to patent document 2 is expressed by a downward convex curve projecting in a right upward direction. Accordingly, the MOSFET 902 according to patent document 2 differs from the MOSFET of the present invention where average positive charge density $\rho(x)$ is expressed by an upward convex curve projecting in a right upward direction.

Brief Description of Drawings

[0028]

25 Fig. 1 is a circuit diagram showing a power conversion

circuit 1 according to Embodiment 1.

Fig. 2 is a cross-sectional view of a MOSFET 100 according to Embodiment 1.

Fig. 3 is a schematic view for explaining an average
5 positive charge density $\rho(x)$ at a predetermined depth position
of a super junction structure when the super junction structure
is depleted by turning off the MOSFET. In Fig. 3, the
illustration of constitutional elements other than the super
junction structure 117 (an n-type column region 114 and a p-type
10 column region 116), and a buffer layer 113 are omitted. In
Fig. 3, an x axis on a left side is an axis taken along a depth
direction using a deepest position of a surface of a depletion
layer on a first main surface side when the depletion layer
extends most in the super junction structure by turning off
15 the MOSFET as a reference. A position $-t$ on the x coordinate
indicates a depth position of a lowermost surface of a base
region 118, a position b on the x coordinate indicates a depth
position of a lowermost portion of a p-type column region 116,
and a position a on the x coordinate is a shallowest position
20 of a surface of a depletion layer on a second main surface side
when the depletion layer extends most in the super junction
structure by turning off the MOSFET (the same definition
applicable to Fig. 4(a) to Fig. 4(d) and Fig. 5(a) to Fig. 5(d)).

Fig. 4(a) to Fig. 4(d) are graphs expressing changes when
25 a super junction structure is depleted by turning off a MOSFET

800 according to Comparative example 1, that is, a change in width $w_n(x)$ at a predetermined depth position of an n-type column region with respect to a depth x , a change in a width $w_p(x)$ at a predetermined depth position in a p-type column
5 region with respect to the depth x , a change in average density $N_d(x)$ of a positive charge at a predetermined depth position of the n-type column region with respect to the depth x , a change in average density $N_a(x)$ of a negative charge at a predetermined depth position of the p-type column region with respect to the
10 depth x , and a change in average positive charge density $\rho(x)$ and an electric field $E(x)$ at the predetermined depth position of the super junction structure with respect to the depth x . Fig. 4(a) is a graph expressing a change in the width $w_n(x)$ at the predetermined depth position of the n-type column region
15 and the width $w_p(x)$ at the predetermined depth position of the p-type column region with respect to the depth, Fig. 4(b) is a graph expressing a change in average density $N_d(x)$ of a positive charge at the predetermined depth position of the n-type column region and average density $N_a(x)$ of a negative
20 charge at the predetermined depth position of the p-type column region with respect to the depth, Fig. 4(c) is a graph expressing a change in average positive charge density $\rho(x)$ at the predetermined depth position of the super junction structure with respect to the depth x , and Fig. 4(d) is a graph
25 expressing a change in an electric field $E(x)$ at the

predetermined depth position of the super junction structure with respect to the depth x . On the x coordinate, the position d is the depth position where the average positive charge density $\rho(x)$ becomes 0.

5 Fig. 5(a) to Fig. 5(d) are graphs expressing changes when a super junction structure 117 is depleted by turning off a MOSFET 100 according to Embodiment 1, that is, a change in width $w_n(x)$ at a predetermined depth position of an n-type column region 114 with respect to a depth x , a change in a width $w_p(x)$
 10 at a predetermined depth position in a p-type column region 116 with respect to the depth x , a change in average density $N_d(x)$ of a positive charge at a predetermined depth position of the n-type column region 114 with respect to the depth x , a change in average density $N_a(x)$ of a negative charge at a
 15 predetermined depth position of the p-type column region 116 with respect to the depth x , and a change in average positive charge density $\rho(x)$ and an electric field $E(x)$ at the predetermined depth position of the super junction structure 117 with respect to the depth x . Fig. 5(a) is a graph expressing
 20 a change in the width $w_n(x)$ at the predetermined depth position of the n-type column region 114 and the width $w_p(x)$ at the predetermined depth position of the p-type column region 116 with respect to the depth x , Fig. 5(b) is a graph expressing a change in average density $N_d(x)$ of a positive charge at the
 25 predetermined depth position of the n-type column region 114

and average density $N_a(x)$ of a negative charge at the predetermined depth position of the p-type column region 116 with respect to the depth x , Fig. 5(c) is a graph expressing a change in average positive charge density $p(x)$ at the predetermined depth position of the super junction structure 117 with respect to the depth x , and Fig. 5(d) is a graph expressing a change in an electric field $E(x)$ at the predetermined depth position of the super junction structure 117 with respect to the depth x .

Fig. 6 is a graph showing a result of time transition simulation of a drain-source voltage V_{ds} , a drain current I_d and a gate-source voltage V_{gs} when a MOSFET 800 according to a Comparative example 1 is turned off in a power conversion circuit using the MOSFET 800. In Fig. 6, "p-type dopant rich" means a case where a total amount of a dopant in a p-type column region is 10% larger than a total amount of a dopant in an n-type column region, "n-type dopant rich" means a case where a total amount of a dopant in a n-type column region is 10% larger than a total amount of a dopant in a p-type column region, and "Just" means a case where a total amount of a dopant in a n-type column region and a total amount of a dopant in an p-type column region are equal (the same definition applicable to Fig. 7). Further, a power source voltage is 300V (the same definition applicable to Fig. 7).

Fig. 7 is a graph showing a result of time transition

simulation of a drain-source voltage V_{ds} , a drain current I_d and a gate-source voltage V_{gs} when a MOSFET according to Embodiment 1 is turned off in a power conversion circuit 1 according to Embodiment 1.

5 Fig. 8 is a schematic view showing a mode of a depletion layer at a moment during a turn-off period in the MOSFET 800 according to Comparative example 1. In Fig. 8, the illustration of a source region is omitted (the same definition applicable to Fig. 9).

10 Fig. 9 is a schematic view showing a mode of a depletion layer at a moment during a turn-off period in the MOSFET 100 according to Embodiment 1. Fig. 9 shows a mode of a depletion layer at the same timing as Fig. 8.

Fig. 10(a) and Fig. 10(b) are cross-sectional views
15 showing a MOSFET 700 according to Comparative example 2 and a MOSFET 100A according to a present invention example. Fig. 10(a) is a cross-sectional view showing the MOSFET 700 according to Comparative example 2. Fig. 10(b) is a cross-sectional view showing the MOSFET 100A according to the
20 present invention example. Fig. 10(a) and Fig. 10(b) are schematic views and do not strictly reflect sizes and shapes of the structures used in a simulation result shown in Fig. 6.

Fig. 11(a) and Fig. 11(b) are views showing a simulation
25 result of equal potential lines when the MOSFET is turned off

in the MOSFET 700 according to the Comparative example 2 and the MOSFET 100A according to the present invention example. Fig. 11(a) is a view showing the simulation result of equal potential lines when the MOSFET is turned off in the MOSFET 700 according to the Comparative example 2. Fig. 11(b) is a view showing the simulation result of equal potential lines when the MOSFET is turned off in the MOSFET 100A according to the present invention example. Fig. 11(a) is a view corresponding to a region surrounded by a chain line shown in Fig. 10(a), and Fig. 11(b) is a view corresponding to a region surrounded by a chain line shown in Fig. 10(b). In Fig. 11(a) and Fig. 11(b), a bold black solid line indicates a boundary between an n-type column region and a p-type column region, a black fine solid line indicates equal potential lines drawn at an interval of 3V, and a white solid line indicates a boundary between a region where carriers become 5% at a normal time and remaining other regions.

Fig. 12(a) to Fig. 12(c) are views for explaining a MOSFET 102 according to Embodiment 2. Fig. 12(a) is a cross-sectional view showing the MOSFET 102 according to Embodiment 2, Fig. 12(b) is a graph expressing changes when a super junction structure 117 is depleted by turning off the MOSFET, that is, a change in width $w_n(x)$ at a predetermined depth position of an n-type column region 114 with respect to a depth x , a change in a width $w_p(x)$ at a predetermined depth position in a p-type

column region 116 with respect to the depth x , and Fig. 12(c) is a graph expressing changes when a super junction structure 117 is depleted by turning off the MOSFET, that is, a change in average density $N_d(x)$ of a positive charge at a predetermined depth position of the n-type column region with respect to the depth x , a change in average density $N_a(x)$ of a negative charge at a predetermined depth position of the p-type column region with respect to the depth x .

Fig. 13 is cross-sectional view showing a MOSFET 200 according to Embodiment 3.

Fig. 14 is a circuit diagram showing a power conversion circuit 2 according to Embodiment 4.

Fig. 15 is a cross-sectional view showing a MOSFET 104 according to Modification 1.

Fig. 16 is a cross-sectional view showing a MOSFET 106 according to Modification 2.

Fig. 17 is a cross-sectional view showing a conventional MOSFET 900. In the drawing, symbol 912 indicates a low-resistance semiconductor layer, symbol 913 indicates a buffer layer, symbol 915 indicates an n-type semiconductor layer, symbol 930 indicates a source electrode, symbol 932 indicates a drain electrode.

Fig. 18 is a cross-sectional view showing a MOSFET 902 disclosed in patent document 2.

Description of Embodiments

[0029]

Hereinafter, a MOSFET and a power conversion circuit according to the present invention are described in accordance with Embodiments shown in the drawings. The respective drawings are schematic drawings, and do not always strictly reflect actual sizes of the MOSFET and the power conversion circuit.

[0030]

10 [Embodiment 1]

1. Structure and operation of power conversion circuit 1 according to Embodiment 1

A power conversion circuit 1 according to Embodiment 1 is a chopper circuit which is a constitutional element such as a DC-DC converter or an inverter. The power conversion circuit 1 according to Embodiment 1 includes, as shown in Fig. 1, a reactor 10, a power source 20, a MOSFET 100 according to Embodiment 1, and a rectifier element 30.

[0031]

20 The reactor 10 is a passive element which can store energy in a magnetic field generated by an electric current which flows through the reactor 10.

The power source 20 is a DC power source which supplies an electric current to the reactor 10. The MOSFET 100 controls an electric current supplied from the power source 20 to the

25

reactor 10. To be more specific, the MOSFET 100 is switched to assume an ON state in response to a clock signal applied from a drive circuit (not shown in the drawing) to a gate electrode of the MOSFET 100, and makes the reactor 10 and a negative pole of the power source 20 electrically conductive with each other. The specific structure of the MOSFET 100 is described later.

The rectifier element 30 is a fast recovery diode which performs a rectifying operation of an electric current supplied from the power source 20 to the reactor 10. To be more specific, the rectifier element 30 is a lifetime-controlled PIN diode. [0032]

A positive pole (+) of the power source 20 is electrically connected to one end 12 of the reactor 10 and a cathode electrode of the rectifier element 30, and a negative pole (-) of the power source 20 is electrically connected to a source electrode of the MOSFET 100. A drain electrode of the MOSFET 100 is electrically connected to the other end 14 of the reactor 10 and an anode electrode of the rectifier element 30.

[0033]

In such a power conversion circuit 1, when the MOSFET 100 is in an ON state, an electric current path from a positive pole (+) of the power source 20 to the negative pole (-) of the power source 20 through the reactor 10 and the MOSFET 100 is formed, and an electric current flows through the electric

current path. In this case, electric energy of the power source
20 is stored in the reactor 10.

When the MOSFET 100 is turned off, an electric current
which flows through the electric current path from the positive
5 pole (+) of the power source 20 to the negative pole (-) of
the power source 20 through the reactor 10 and the MOSFET 100
is decreased and becomes 0 soon. On the other hand, the reactor
10 generates an electromotive force in a direction in which
a change in an electric current is obstructed (electric energy
10 stored in the reactor 10 is discharged) due to a self induction
effect. An electric current generated due to an electromotive
force of the reactor 10 flows to the rectifier element 30, and
a forward electric current flows in the rectifier element 30.

A sum of an amount of an electric current which flows
15 through the MOSFET 100 and an amount of an electric current
which flows through the rectifier element 30 is equal to an
amount of an electric current which flows through the reactor
10. A switching period of the MOSFET 100 is short (possibly
100 nsec at maximum) and hence, an amount of an electric current
20 which flows through the reactor 10 minimally changes during
such a period. Accordingly, a sum of an amount of an electric
current which flows through the MOSFET 100 and an amount of
an electric current which flows through the rectifier element
30 minimally changes in either case, that is, an ON state, a
25 turn-off period or an OFF state.

[0034]

In such a power conversion circuit 1, a case is considered where a MOSFET where side walls of the n-type column region 914 are formed in a tapered shape narrowed toward a first main surface side, and side walls of the p-type column region 916 are formed in a tapered shape with a narrow bottom (for example, a conventional MOSFET 900) is used as the MOSFET. In this case, when an irregularity exists in a charge balance around the gate, there arises a drawback that an irregularity in switching characteristics when the power conversion circuit 1 is turned off is increased (see Fig. 6 described later).

[0035]

Accordingly, in the present invention, as the MOSFET, the MOSFET 100 according to Embodiment 1 having the following structure is used.

[0036]

2. Structure of MOSFET 100 according to Embodiment 1

As shown in Fig. 2, the MOSFET 100 according to Embodiment 1 is a trench-gate-type MOSFET which includes a semiconductor base substrate 110, a trench 122, a gate electrode 126, an interlayer insulation film 128, a source electrode 130, and a drain electrode 132. A drain-source withstand voltage of the MOSFET 100 is 300V or more, for example, 600V.

[0037]

The semiconductor base substrate 110 has an n-type

low-resistance semiconductor layer 112, an n-type buffer layer 113 formed on the low-resistance semiconductor layer 112 and having a lower dopant concentration than dopant concentration in the low-resistance semiconductor layer 112, a super junction structure 117 formed of n-type column regions 114 and p-type column regions 116 which are formed on the buffer layer 113 where the n-type column region 114 and the p-type column region 116 are alternately arranged along a horizontal direction, a p-type base region 118 formed on surfaces of the n-type column regions 114 and surfaces of the p-type column regions 116, and n-type source regions 120 formed on a surface of the base region 118. The buffer layer 113 and the n-type column regions 114 are integrally formed with each other, and the buffer layer 113 and the n-type column regions 114 form an n-type semiconductor layer 115.

[0038]

Although a total amount of a dopant in the n-type column region 114 is set equal to a total amount of a dopant in the p-type column region 116, a total amount of a dopant in the n-type column region 114 may be set larger than a total amount of a dopant in the p-type column region 116 or a total amount of a dopant in the n-type column region 114 may be set smaller than a total amount of a dopant in the p-type column region 116.

25 [0039]

With respect to the n-type column region 114 and the p-type column region 116, in a graph where the depth x at the predetermined depth position in the super junction structure is taken on an axis of abscissas, and a width $w_n(x)$ at the predetermined depth position in the n-type column region or a width $w_p(x)$ at the predetermined depth position in the p-type column region is taken on an axis of ordinates, the width $w_n(x)$ is expressed by an upward convex curve projecting in a right upward direction, and the width $w_p(x)$ is expressed by a downward convex curve projecting in a right downward direction (see Fig. 5(a)). That is, the n-type column region 114 has a shape of a cup with its open side down in cross section, while the p-type column region 116 has a shape of a funnel in cross section. Dopant concentration in the n-type column region 114 and dopant concentration in the p-type column region 116 are set to a fixed value regardless of depth (see Fig. 5(b)).

[0040]

All of the n-type column regions 114, the p-type column regions 116, the source regions 120, the trenches 122 and the gate electrodes 126 are formed in a stripe shape as viewed in a plan view.

[0041]

A thickness of the low-resistance semiconductor layer 112 falls within a range of $100\mu\text{m}$ to $400\mu\text{m}$, for example, and dopant concentration in the low-resistance semiconductor

layer 112 falls within a range of $1 \times 10^{19} \text{cm}^{-3}$ to $1 \times 10^{20} \text{cm}^{-3}$, for example. A thickness of the n-type semiconductor layer 115 falls within a range of $5 \mu\text{m}$ to $120 \mu\text{m}$, for example. Dopant concentration in the n-type semiconductor layer 115 falls within a range of $5 \times 10^{13} \text{cm}^{-3}$ to $1 \times 10^{16} \text{cm}^{-3}$, for example. Dopant concentration of the p-type column region 116 falls within a range of $5 \times 10^{13} \text{cm}^{-3}$ to $1 \times 10^{16} \text{cm}^{-3}$, for example. A depth position of a deepest portion of the base region 118 falls within a range of $0.5 \mu\text{m}$ to $4.0 \mu\text{m}$, for example, and dopant concentration in the base region 118 falls within a range of $5 \times 10^{16} \text{cm}^{-3}$ to $1 \times 10^{18} \text{cm}^{-3}$, for example. A depth position of a deepest portion of the source region 120 falls within a range of $0.1 \mu\text{m}$ to $0.4 \mu\text{m}$, for example, and dopant concentration in the source region 120 falls within a range of $5 \times 10^{19} \text{cm}^{-3}$ to $2 \times 10^{20} \text{cm}^{-3}$, for example.

[0042]

The trench 122 is formed in a region where the n-type column region 114 is positioned as viewed in a plan view. The trench 122 is formed such that the trench 122 extends from a surface of a first main surface of the semiconductor base substrate 110 to a depth position deeper than a deepest portion of the base region 118 and a portion of the source region 120 is exposed to an inner peripheral surface of the trench 122. A depth of the trench 122 is $5 \mu\text{m}$ for example.

[0043]

The gate electrode 126 is embedded in the inside of the

trench 122 by way of the gate insulation film 124 formed on an inner peripheral surface of the trench 122. The gate insulation film 124 is formed of a silicon dioxide film formed by a thermal oxidation method and the gate insulation film 124 has a thickness of 100nm, for example. The gate electrode 126 is formed by a CVD method and an ion implantation method and is made of low-resistance polysilicon.

[0044]

The interlayer insulation film 128 is formed so as to cover a portion of the source region 120, the gate insulation film 124 and the gate electrode 126. The interlayer insulation film 128 is formed by a CVD method and is formed of a PSG film having a thickness of 1000nm, for example.

[0045]

The source electrode 130 is formed so as to cover the base region 118, portions of the source regions 120, and the interlayer insulation film 128 and electrically connected with the source region 120. The drain electrode 132 is formed on a surface of the low-resistance semiconductor layer 112. The source electrode 130 is made of aluminum-based metal (Al-Cu-based alloy, for example) having a thickness of 4 μ m formed by a sputtering method, for example. The drain electrode 132 is formed of a multi-layered metal film such as a Ti-Ni-Au film. A total thickness of the multi-layered metal film is 0.5 μ m, for example.

[0046]

3. Average positive charge density $\rho(x)$ at predetermined depth position of super junction structure

To evaluate a charge amount of a positive charge in the
 5 n-type column region 114 and a charge amount of a negative
 charge in the p-type column region 116 when the MOSFET is turned
 off, average positive charge density $\rho(x)$ at a predetermined
 depth position of the super junction structure when the super
 junction structure is depleted by turning off the MOSFET
 10 (hereinafter, simply referred to as average positive charge
 density $\rho(x)$) is used.

[0047]

Assuming a depth at a predetermined depth position in
 the super junction structure 117 (hereinafter, simply referred
 15 to as a depth x) as x using a deepest position of a surface
 of a depletion layer on the first main surface side when the
 depletion layer extends most in the super junction structure
 by turning off the MOSFET as a reference, average positive
 charge density $\rho(x)$ is expressed by the following formula (1).

20 [Formula 1]

$$\rho(x) = \frac{q}{2w} \left[w_n(x) \cdot N_d(x) - w_p(x) \cdot N_a(x) \right] \cdots (1)$$

(In the formula (1), $w_n(x)$ indicates a width of the n-type
 column region 114 at the predetermined depth position, $N_d(x)$
 indicates average density of a positive charge at the

predetermined depth position in the n-type column region 114 when the super junction structure 117 is depleted by turning off the MOSFET, $w_p(x)$ indicates a width of the p-type column region at the predetermined depth position, $N_a(x)$ indicates average density of a negative charge at the predetermined depth position in the p-type column region 116 when the super junction structure 117 is depleted by turning off the MOSFET, q indicates an elementary charge, and w indicates a positive constant which satisfies $w_n(x) + w_p(x) = 2w$. See Fig. 3.)

10 [0048]

In Embodiment 1, in a state where a depletion layer extends most in the super junction structure by turning off the MOSFET, average positive charge density $\rho(x)$ within a range of $0 \leq x \leq a$ is evaluated assuming a deepest position of a surface of the depletion layer on a first main surface side as $x=0$ and a depth of a shallowest position of a surface of the depletion layer on the second main surface side as a .

[0049]

In this embodiment, assuming that dopant concentration in the n-type column region 114 and dopant concentration in the p-type column region 116 are respectively set to a fixed value regardless of depth, $N_a(x)$ and $N_d(x)$ becomes N_0 ($N_a(x) = N_d(x) = N_0$) and hence, average positive charge density $\rho(x)$ is expressed by the following formula (2).

25 [Formula 2]

$$\rho(x) = \frac{q N_o}{2w} [w_n(x) - w_p(x)] \cdot \cdot \cdot (2)$$

[0050]

An electric field $E(x)$ at a predetermined depth position of the super junction structure 117 (hereinafter, simply referred to as an electric field $E(x)$) when the super junction structure 117 is depleted by turning off the MOSFET expresses an electric field generated by a positive charge (donor) at a predetermined depth position of the n-type column region 114 and an electric field generated by a negative charge (acceptor) at a predetermined depth position of the p-type column region 116 when the super junction structure 117 is depleted by turning off the MOSFET, and is expressed by the following formula (3).

[Formula 3]

$$E(x) = \int_0^x \frac{\rho(x)}{\epsilon} dx \cdot \cdot \cdot (3)$$

(In the formula (3), ϵ : dielectric constant of a material (for example, silicon) of a semiconductor base substrate)

[0051]

To describe the MOSFET 100 according to Embodiment 1, a MOSFET 800 according to Comparative example 1 is described first.

The MOSFET 800 according to Comparative example 1 (see Fig. 8) basically has substantially the same structure as the MOSFET 100 according to Embodiment 1. However, in the same

manner as the conventional MOSFET 900, the MOSFET 800 according to Comparative example 1 differs from the MOSFET 100 according to Embodiment 1 with respect to a point that side walls of the n-type column region 814 are formed in a tapered shape narrowed toward the first main surface side, and side walls of the p-type column region 816 are formed in a tapered shape with a narrow bottom.

[0052]

In the MOSFET 800 according to Comparative example 1, in a graph where a depth x is taken on an axis of abscissas and a width $w_n(x)$ at a predetermined depth position in the n-type column region 814 or a width $w_p(x)$ at a predetermined depth position in the p-type column region 816 is taken on an axis of ordinates, the width $w_p(x)$ is expressed by a straight line extending in a right downward direction, and the width $w_n(x)$ is expressed by a straight line extending in a right upward direction (see Fig. 4(a)).

Further, in the MOSFET 800 according to Comparative example 1, in the same manner as the MOSFET 100 according to Embodiment 1, dopant concentration in the n-type column region 814 and dopant concentration in the p-type column region 816 are set to a fixed value regardless of depth (see Fig. 4(b)).

[0053]

From the above, in the MOSFET 800 according to Comparative example 1, average positive charge density $\rho(x)$

is expressed by a straight line extending in a right upward direction (see Fig. 4(c)).

To describe the straight line which expresses average positive charge density $\rho(x)$ in detail, using a deepest position of a surface of a depletion layer on the first main surface side when the depletion layer extends most in the super junction structure by turning off the MOSFET as a reference, in a graph where an axis along a depth direction is set as an x axis, an x coordinate at a depth position of a lowermost surface of the base region is set as $-t$, an x coordinate at depth position of a lowermost portion of the p-type column region is set as b , and an x coordinate at a depth position where the average positive charge density $\rho(x)$ becomes 0 is set as d , and an x coordinate at a shallowest position of a surface of a depletion layer on a second main surface side when the depletion layer extends most in the super junction structure by turning off the MOSFET is set as a , the following (1) to (3) are established.

(1) The x coordinate d satisfies the relationship of $d=a/2$. That is, the depth at the depth position where the average positive charge density $\rho(x)$ becomes 0 becomes as follows. The depth d at the predetermined depth position when the average positive charge density $\rho(x)$ becomes 0 using a deepest position of a surface of a depletion layer on the first main surface side when the depletion layer extends most in the

super junction structure by turning off the MOSFET as a reference becomes a depth half of the depth a at the shallowest position of a surface of a depletion layer on the second main surface side when the depletion layer extends most in the super junction structure by turning off the MOSFET (that is, a charge balance being taken at the depth position where $x=a/2$).

(2) A value of the average positive charge density $\rho(0)$ when $x=0$ is negative, and a value of the average positive charge density $\rho(a)$ at $x=a$ is positive.

(3) An area of a region surrounded by the straight line expressing the average positive charge density $\rho(x)$, the straight line at $x=0$ and the axis of abscissas (x axis) is equal to an area of a region surrounded by the straight line expressing the average positive charge density $\rho(x)$, the straight line at $x=a$ and the axis of abscissas (x axis).

[0054]

Further, in the MOSFET 800 according to Comparative example 1, an electric field $E(x)$ becomes a downwardly convex quadratic function having a peak at $x=a/2$ (see Fig. 4(d)).

State where the electric field $E(x)$ becomes negative means that an electric field vector is directed in a direction that x approaches 0.

[0055]

To the contrary, in the MOSFET 100 according to Embodiment 1, in a graph where the depth x is taken on an axis

of abscissas, and a width $w_n(x)$ at the predetermined depth position in the n-type column region or a width $w_p(x)$ at the predetermined depth position in the p-type column region is taken on an axis of ordinates, the width $w_n(x)$ is expressed
 5 by a monotonous upward convex curve projecting in a right upward direction, and the width $w_p(x)$ is expressed by a monotonous downward convex curve projecting in a right downward direction (see Fig. 5(a)).

Further, in the MOSFET 100 according to Embodiment 1,
 10 dopant concentration in the n-type column region 114 and dopant concentration in the p-type column region 116 are set to a fixed value regardless of depth (see Fig. 5(b)).

[0056]

From these, in the MOSFET 100 according to Embodiment
 15 1, average positive charge density $\rho(x)$ is expressed by a monotonous upward convex curve projecting in a right upward direction (see Fig. 5(c)).

To describe the curve which expresses average positive charge density $\rho(x)$ in detail, using a deepest position of a
 20 surface of a depletion layer on the first main surface side when the depletion layer extends most in the super junction structure by turning off the MOSFET as a reference, in a graph where an axis along a depth direction is set as an x axis, an x coordinate at a depth position of a lowermost surface of the
 25 base region is set as $-t$, an x coordinate at the depth position

of a lowermost portion of the p-type column region is set as b , and an x coordinate at a depth position where the average positive charge density $\rho(x)$ becomes 0 is set as d , and an x coordinate at a shallowest position of the surface of the depletion layer on a second main surface side when the depletion layer extends most in the super junction structure by turning off the MOSFET is set as a , the following relationships (1) to (4) are satisfied.

(1) The relationship of $0 < d < a/2$ is satisfied. That is, using a deepest position of a surface of a depletion layer on the first main surface side when the depletion layer extends most in the super junction structure by turning off the MOSFET as a reference, the depth d at a predetermined depth position when the average positive charge density $\rho(x)$ becomes 0 is shallower than a depth half of the depth a at the shallowest position of a surface of a depletion layer on the second main surface side when the depletion layer extends most in the super junction structure by turning off the MOSFET (that is, the depth position where a charge balance is taken is shallower than the depth position where a charge balance is taken in the MOSFET according to Comparison example 1).

(2) A value of the average positive charge density $\rho(0)$ when $x=0$ is negative, and a value of the average positive charge density $\rho(a)$ at $x=a$ is positive.

(3) An area of a region surrounded by the curve expressing

the average positive charge density $\rho(x)$, the straight line at $x=0$ and the axis of abscissas (x axis) is equal to an area of a region surrounded by the curve expressing the average positive charge density $\rho(x)$, the straight line at $x=a$ and the
 5 axis of abscissas (x axis).

(4) The relationship of $0 < t+d < (t+b)/2$ is satisfied.

[0057]

Further, an electric field $E(x)$ becomes a downwardly convex quadratic function having a peak at $x=d$ (see Fig. 5(d)).
 10 In this case, the electric field $E(x)$ is rapidly decreased when $x < d$, and the electric field $E(x)$ is gently increased when $x > d$.
 [0058]

4. Manner of operation and waveform of MOSFET 100 when MOSFET 100 is turned off

15 In the power conversion circuit 1 according to Embodiment 1, in the case where the MOSFET 800 according to Comparative example 1 is used in place of the MOSFET 100, the MOSFET 800 according to Comparative example 1 is operated as follows.

(1) Drain current I_d

20 In the case where a total amount of a dopant in the n -type column region and a total amount of a dopant in the p -type column region are equal (hereinafter referred to as "in the case of Just"), the MOSFET 800 is operated such that, during a period from a point of time that a drain current I_d starts to be
 25 decreased to a point of time that the drain current I_d becomes

0 for the first time, a period where the drain current I_d is temporarily increased slightly appears (the MOSFET 800 being operated such that a hump waveform slightly appears in a waveform of the drain current I_d , see $I_d(\text{Just})$ in Fig. 6). The period from a point of time that a drain current I_d starts to be decreased to a point of time that the drain current I_d becomes 0 for the first time is approximately $0.02\mu\text{sec}$ (20nsec).

In the case where an irregularity exists in a charge balance such that a total amount of a dopant in the n-type column region is larger than a total amount of a dopant in the p-type column region (hereinafter referred to as "in the case of n-type dopant rich"), the MOSFET 800 is operated such that, during a period from a point of time that a drain current I_d starts to be decreased to a point of time that the drain current I_d becomes 0 for the first time, a period where the drain current I_d is temporarily increased appears (the MOSFET 800 being operated such that a large hump waveform appears in a waveform of the drain current I_d , see $I_d(\text{n-type dopant rich})$ in Fig. 6). With respect to the hump waveform, the drain current I_d is increased to a current value higher than a current value in the case of Just and, at the same time, a period until the drain current I_d becomes 0 is largely prolonged compared to the case of Just (approximately $0.02\mu\text{sec}$ (20nsec) in the case of Just and approximately $0.04\mu\text{sec}$ (40nsec) in the case of n-type dopant rich).

In the case where a total amount of a dopant in the p-type column region is larger than a total amount of a dopant in the n-type column region (hereinafter referred to as "in the case of p-type dopant rich"), the MOSFET 800 is operated such that the drain current I_d is monotonously decreased (the MOSFET 800 being operated such that no hump waveform appears in a waveform of the drain current I_d , see I_d (p-type dopant rich) in Fig. 6).

(2) Drain-source voltage V_{ds}

In the case of n-type dopant rich, the MOSFET 800 is operated such that a drain-source voltage V_{ds} is increased to approximately 350V more gently compared to the case of Just and, thereafter, the drain-source voltage V_{ds} is gradually decreased and becomes stable at a power source voltage (300V). A time until a drain-source voltage V_{ds} becomes stable from a point of time that the drain-source voltage V_{ds} starts to be increased is longer than that of the case of Just and is approximately 0.05 μ sec (50nsec) (see V_{ds} (n-type dopant rich) in Fig. 6).

In the case of p-type dopant rich, the MOSFET 800 is operated such that a drain-source voltage V_{ds} is increased to approximately 370V more steeply compared to the case of Just and, thereafter, becomes stable at a power source voltage (300V) (see V_{ds} (p-type dopant rich) in Fig. 6). A time until a drain-source voltage V_{ds} becomes stable from a point of time

that the drain-source voltage V_{ds} starts to be increased is approximately $0.02\mu\text{sec}$ (20nsec).

(3) Gate-source voltage V_{gs}

In the case of n-type dopant rich, the MOSFET 800 is
5 operated such that a period during which a gate-source voltage V_{gs} is temporarily increased slightly appears after completion of a mirror period (see V_{gs} (n-type dopant rich) in Fig. 6). On the other hand, in the case of Just and in the case of p-type dopant rich, the MOSFET 800 is operated such that a gate-source
10 voltage V_{gs} minimally changes and is monotonously decreased (see V_{gs} (p-type dopant rich) and V_{gs} (Just) in Fig. 6).
[0059]

As can be understood from the above-mentioned (1) to (3), in the MOSFET 800 according to the Comparative example 1, when
15 an irregularity exists in a charge balance around the gate (in case such as Just being changed to an n-type dopant rich state or a p-type dopant rich state), an irregularity in switching characteristics when the MOSFET is turned off, particularly an irregularity in a drain current I_d and a drain-source voltage
20 V_{ds} is increased. When an irregularity in a charge balance exists in an n-type dopant rich state, an irregularity in switching characteristics is particularly increased.
[0060]

On the other hand, in the power conversion circuit 1
25 according to Embodiment 1, the MOSFET 100 according to

Embodiment 1 is operated as follows.

(1) Drain current I_d

In all cases, that is, in case of Just, in case of n-type dopant rich and in case of p-type dopant rich, a turn-off period becomes short. Further, in all cases, the MOSFET 100 is operated such that the drain current I_d adopts a similar waveform (see respective I_d in Fig. 7). Particularly, in case of n-type dopant rich, a hump waveform hardly appears in a waveform of the drain current I_d and hence, the MOSFET 100 is operated such that the waveform of the drain current I_d becomes similar to a waveform of the drain current I_d in case of Just and the drain current I_d in case of p-type dopant rich.

(2) Drain-source voltage V_{ds}

In all cases, that is, in case of Just, in case of n-type dopant rich and in case of p-type dopant rich, a turn-off period becomes short. Further, in all cases, the MOSFET is operated such that the drain-source voltage V_{ds} adopts a similar waveform (see respective V_{ds} in Fig. 7). Although ringing occurs in case of p-type dopant rich, ringing can be made small by including a mechanism to remove ringing such as a snubber circuit.

(3) Gate-source voltage V_{gs}

In all cases, that is, in case of Just, in case of n-type dopant rich and in case of p-type dopant rich, the MOSFET is operated such that there is substantially no difference in the

gate-source voltage V_{gs} between these cases (see respective V_{gs} in Fig. 7).

[0061]

As can be understood from the above-mentioned (1) to (3),
5 in the MOSFET 100 according to Embodiment 1, even when an
irregularity in a charge balance exists around the gate (case
of Just being changed to case of an n-type dopant rich state,
case of Just being changed to case of a p-type dopant rich state
or the like), an irregularity in switching characteristics when
10 the MOSFET is turned off can be made small.

[0062]

Next, the reason is explained why the MOSFET 100
according to Embodiment 1 and the MOSFET 800 according to
Comparative example 1 take the above-mentioned waveforms.

15 Firstly, in the MOSFET 800 according to Comparative
example 1, when the MOSFET is turned off, the depletion layer
extends to the n-type column region 814 and the p-type column
region 816 from the PN junction between the p-type column region
816 (and the base region 818) and the n-type column region 814.
20 However, in the MOSFET 800 according to Comparative example
1, although the depletion layer extends to an area directly
below the trench, the depletion layer hardly extends to a drain
electrode side and hence, it is difficult to increase a distance
between the region which is not depleted in the n-type column
25 region 814 and the gate electrode 826 whereby it is difficult

to decrease a feedback capacitance C_{rss} (see Fig. 8). Accordingly, the gate electrode 826 is liable to be easily affected by a change in potential of the n-type column region 814 and hence, when there is an irregularity in charge balance around the gate, it is difficult to decrease an irregularity in switching characteristic when the MOSFET is turned off.

[0063]

To the contrary, in the MOSFET 100 according to Embodiment 1, the depletion layer easily extends to also a drain electrode side and hence, a distance between the region which is not depleted in the n-type column region 114 and the gate electrode 126 can be easily increased whereby a feedback capacitance C_{rss} can be easily increased (see Fig. 9). Accordingly, the gate electrode 126 is minimally affected by a change in potential of the n-type column region 114 and hence, when there is an irregularity in charge balance around the gate, an irregularity in switching characteristic when the MOSFET is turned off can be decreased.

[0064]

The above-mentioned reason is explained from an aspect of equal potential lines.

The MOSFET 700 according to Comparative example 2 is a MOSFET substantially having the same configuration as the MOSFET 800 according to Comparative example 1 except for a point that a portion of the MOSFET 700 which is brought into contact

with the source electrode is dug to a depth position of a lowermost portion of the source region (see Fig. 10(a)). A MOSFET 100A according to a present invention example is a MOSFET substantially having the same configuration as the MOSFET 100 according to Embodiment 1 except for a point that a portion of the MOSFET 100A which is brought into contact with the source electrode is dug to a depth position of a lowermost portion of the source region (see Fig. 10(b)).

[0065]

10 In the MOSFET 700 according to Comparative example 2, when the MOSFET is turned off, a state arises where a distance between the equal potential lines on a bottom portion of the trench is narrow (see Fig. 11(a)). This is because a distance between a non-depleted region in the n-type column region 714 and the gate electrode 726 is short. Accordingly, a potential gradient in the vicinity of the bottom portion of the trench is increased and hence, the gate electrode 726 is liable to be easily affected by a change in potential of the n-type column region 714. Accordingly, when an irregularity occurs in a charge balance around the gate, it is difficult to decrease an irregularity in switching characteristics when the MOSFET 700 is turned off.

[0066]

On the other hand, in the MOSFET 100A according to the present invention example, when the MOSFET is turned off, a

state arises where a distance between the equal potential lines on a bottom portion of the trench 122 is wide (see Fig. 11(b)). This is because a distance between a non-depleted region in the n-type column region 114 and the gate electrode 126 is long.

5 Accordingly, a potential gradient in the vicinity of the bottom portion of the trench 122 is decreased and hence, the gate electrode 126 is minimally affected by a change in potential of the n-type column region 114. Accordingly, even when an irregularity occurs in a charge balance around the gate, an
10 irregularity in switching characteristics when the MOSFET 100A is turned off can be decreased.

[0067]

5. Advantageous effects acquired by MOSFET 100 and power conversion circuit 1 according to Embodiment 1

15 According to the MOSFET 100 and the power conversion circuit 1 of Embodiment 1, average positive charge density $\rho(x)$ at a predetermined depth position of the super junction structure 117 when the super junction structure 117 is depleted by turning off the MOSFET is expressed by an upward convex curve
20 projecting in a right upward direction. With such a configuration, in a depth position around the gate (a region where x is close to 0), the average positive charge density $\rho(x)$ becomes smaller than (larger on a negative side) a conventional MOSFET 900, and the difference between a charge
25 amount of a negative charge in the p-type column region 116

and a charge amount of a positive charge in the n-type column region 114 becomes large compared to the conventional MOSFET 900. Accordingly, the following advantages can be acquired.

(1) The n-type column region 114 around the gate becomes easily depleted compared to the conventional MOSFET 900 and hence, even when a drain voltage is increased, a potential of the n-type column region 114 around the gate is minimally increased.

(2) A distance between a non-depleted region in the n-type column region 114 and the gate electrode 126 becomes long compared to the conventional MOSFET 900 and hence, a feedback capacitance C_{rss} (equal to a gate-drain capacitance C_{gd}) becomes small compared to the conventional MOSFET 900. Accordingly, even when a potential of the n-type column region 114 (the non-depleted region of the n-type column region 114) is increased along with the increase of a drain voltage which takes place when the MOSFET is turned off, the gate electrode 126 is minimally affected by a change in potential of the n-type column region 114. As a result, even when an irregularity exists in a charge balance around the gate, an irregularity in switching characteristics when the MOSFET is turned off can be reduced compared to the prior art.

[0068]

Further, according to the MOSFET 100 of Embodiment 1, average positive charge density $\rho(x)$ at a predetermined depth

position of the super junction structure 117 when the super junction structure 117 is depleted by turning off the MOSFET is expressed as an upward convex curve projecting in a right upward direction. With such a configuration, at a depth
5 position around the gate, an average positive charge density $\rho(x)$ becomes small (large on a negative side) and hence, a charge amount of a negative charge in the p-type column region 116 becomes larger than a charge amount of a positive charge in the n-type column region. Accordingly, holes around the
10 gate in the p-type column region can be easily extracted by a negative charge in the p-type column region 116. As a result, an L-load avalanche breakdown resistance can be increased.
[0069]

Further, the MOSFET 100 according to Embodiment 1
15 includes the semiconductor base substrate 110 where the super junction structure 117 is formed of the n-type column region 114 and the p-type column region 116. Accordingly, in the same manner as the conventional MOSFET 900, the MOSFET becomes a switching element having a low ON resistance and a high
20 withstand voltage.
[0070]

In the MOSFET 100 according to Embodiment 1, the average positive charge density $\rho(0)$ when $x=0$ takes a negative value, and the average positive charge density $\rho(a)$ when $x=a$ takes
25 a positive value. Accordingly, at a depth position in the

vicinity of a bottom portion of the p-type column region 116,
a total amount of a dopant in the p-type column region 116
becomes smaller than a total amount of a dopant in the n-type
column region 114 (becoming n-type dopant rich). With such
5 a configuration, a depletion layer generated from the p-type
column region 116 when the MOSFET is turned off minimally
extends toward a second main surface side. Accordingly, it
is possible to provide an MOSFET where a breakdown in a reach
through mode minimally occurs so that a withstand voltage is
10 minimally lowered.

[0071]

In the MOSFET 100 according to Embodiment 1, using a
deepest position of a surface of a depletion layer on the first
main surface side when the depletion layer extends most in the
super junction structure 117 by turning off the MOSFET as a
15 reference, assuming a depth of a surface of the depletion layer
on the second main surface side at a shallowest position when
the depletion layer extends most in the super junction
structure 117 by turning off the MOSFET as a, and a depth of
20 a depth position where the average positive charge density $\rho(x)$
becomes 0 in the super junction structure 117 as d , a
relationship of $0 < d < a/2$ be satisfied. Accordingly, the
difference between a charge amount of a negative charge in the
p-type column region 116 and a charge amount of a positive
25 charge in the n-type column region 114 becomes large at a depth

position around the gate and hence, the n-type column region 114 around the gate becomes easily depleted. Accordingly, even when an irregularity exists in a charge balance around the gate, an irregularity in switching characteristics when the MOSFET is turned off can be further reduced.

[0072]

In the MOSFET 100 according to Embodiment 1, in a graph where the depth x at the predetermined depth position in the super junction structure 117 is taken on an axis of abscissas, and a width $w_n(x)$ at the predetermined depth position in the n-type column region 114 or a width $w_p(x)$ at the predetermined depth position in the p-type column region 116 is taken on an axis of ordinates, the width $w_p(x)$ is expressed by a downward convex curve projecting in a right downward direction, and the width $w_n(x)$ is expressed by an upward convex curve projecting in a right upward direction. Accordingly, in implanting a dopant in steps of manufacturing a semiconductor device, it is unnecessary to perform a complicated step that concentration of a dopant to be implanted is changed corresponding to a depth.

[0073]

The MOSFET 100 according to Embodiment 1 is a trench-gate-type MOSFET. With such a configuration, also in the trench-gate-type MOSFET where the gate electrode and the drain electrode are arranged close to each other so that a potential of the n-type column region 114 around the gate is

liable to be increased compared to a planar-gate-type MOSFET, it is possible to reduce irregularity in switching characteristics when the MOSFET is turned off compared to a prior art.

5 [0074]

In the power conversion circuit 1 according to Embodiment 1, using a deepest position of a surface of a depletion layer on the first main surface side when the depletion layer extends most in the super junction structure 117 by turning off the MOSFET as a reference, in a graph where an axis along a depth direction is set as an x axis, an x coordinate at a depth position of a lowermost surface of the base region is set as $-t$, an x coordinate at depth position of a lowermost portion of the p-type column region 116 is set as b , and an x coordinate at a depth position where the average positive charge density $\rho(x)$ becomes 0 is set as d , a relationship of $0 < t + d < (t + b) / 2$ is satisfied. With such a configuration, the difference between a charge amount of a negative charge in the p-type column region 116 and a charge amount of a positive charge in the n-type column region 114 becomes large at a depth position around the gate and hence, the n-type column region 114 around the gate becomes easily depleted. As a result, even when an irregularity exists in a charge balance around the gate, an irregularity in switching characteristics when the MOSFET is turned off can be further reduced.

10
15
20
25

[0075]

In the MOSFET 100 according to Embodiment 1, the rectifier element is a fast recovery diode and hence, a turn-off period is short and hence, when the MOSFET is turned off, a potential of the n-type column region 114 is minimally increased along with the increase of a drain voltage. Accordingly, a potential of the gate electrode is also minimally increased. As a result, even when an irregularity exists in a charge balance around the gate, an irregularity in switching characteristics when the MOSFET is turned off can be further reduced.

[0076]

[Embodiment 2]

MOSFET 102 according to Embodiment 2 basically has substantially the same structure as MOSFET 100 according to Embodiment 1. However, MOSFET 102 according to Embodiment 2 differs from MOSFET 100 according to Embodiment 1 with respect to a point that average density $N_d(x)$ of a positive charge at the predetermined depth position in the n-type column region and average density $N_a(x)$ of a negative charge at the predetermined depth position in the p-type column region when the super junction structure is depleted by turning off the MOSFET are changed in place of changing of a width $w_n(x)$ at a predetermined depth position of an n-type column region and a width $w_p(x)$ at a predetermined depth position in a p-type

column region. That is, in the MOSFET 102 according to Embodiment 2, as shown in Fig. 12(a) to Fig. 12(c), in a graph where a depth x is taken on an axis of abscissas, average density $N_d(x)$ of a positive charge at the predetermined depth position in the n-type column region 114 or average density $N_a(x)$ of a negative charge at the predetermined depth position in the p-type column region 116 is taken on an axis of ordinates, average density $N_d(x)$ of a positive charge is expressed by a monotonous upward convex curve projecting in a right upward direction, and average density $N_a(x)$ of a negative charge is expressed by a monotonous downward convex curve projecting in a right downward direction (see Fig. 12(c)). The width of the n-type column region 114 and the width of the p-type column region 116 are set to a fixed value regardless of depth (see Fig. 12(b)).

[0077]

In this manner, the MOSFET 102 according to Embodiment 2 differs from the MOSFET 100 according to Embodiment 1 with respect to the point that average density $N_d(x)$ of a positive charge at the predetermined depth position in the n-type column region and average density $N_a(x)$ of a negative charge at the predetermined depth position in the p-type column region when the super junction structure is depleted by turning off the MOSFET are changed in place of changing of a width $w_p(x)$ at a predetermined depth position in a p-type column region and

a width $w_n(x)$ at a predetermined depth position of an n-type column region. However, in the same manner as the MOSFET 100 according to Embodiment 1, average positive charge density $\rho(x)$ at a predetermined depth position of the super junction structure 117 when the super junction structure 117 is depleted by turning off the MOSFET is expressed by an upward convex curve projecting in a right upward direction. With such a configuration, in a depth position around the gate (a region where x is close to 0), the average positive charge density $\rho(x)$ becomes smaller than (larger on a negative side) a conventional MOSFET 900, and the difference between a charge amount of a negative charge in the p-type column region and a charge amount of a positive charge in the n-type column region becomes large compared to the conventional MOSFET 900. Accordingly, the following advantages can be acquired.

(1) The n-type column region 114 around the gate becomes easily depleted compared to the conventional MOSFET 900 and hence, even when a drain voltage is increased, a potential of the n-type column region 114 around the gate is minimally increased.

(2) A distance between a non-depleted region in the n-type column region 114 and the gate electrode 126 becomes long and hence, a feedback capacitance C_{rss} becomes small compared to the conventional MOSFET 900. Accordingly, even when a potential of the n-type column region 114 (the

non-depleted region of the n-type column region) is increased along with the increase of a drain voltage which takes place when the MOSFET is turned off, the gate electrode 126 is minimally affected by a change in potential of the n-type column region 114. Accordingly, even when an irregularity exists in a charge balance around the gate, an irregularity in switching characteristics when the MOSFET is turned off can be reduced compared to the prior art.

[0078]

10 The MOSFET 102 according to Embodiment 2 has substantially the same structure as the MOSFET 100 according to Embodiment 1 except for the point that average density $N_d(x)$ of a positive charge at the predetermined depth position in the n-type column region and average density $N_a(x)$ of a negative charge at the predetermined depth position in the p-type column region when the super junction structure is depleted by turning off the MOSFET are changed in place of changing of a width $w_n(x)$ at a predetermined depth position of an n-type column region and a width $w_p(x)$ at a predetermined depth position in a p-type column region. Accordingly, the MOSFET 102 according to Embodiment 2 can acquire the advantageous effects by the constitutional parts corresponding to the corresponding constitutional parts of the MOSFET 102 according to Embodiment 2 among the advantageous effects acquired by the MOSFET 100 according to Embodiment 1.

[0079]

[Embodiment 3]

MOSFET 200 according to Embodiment 3 basically has substantially the same structure as MOSFET 100 according to Embodiment 1. However, MOSFET 200 according to Embodiment 3 differs from MOSFET 100 according to Embodiment 1 with respect to a point that the MOSFET 200 according to Embodiment 3 is not a trench-gate-type MOSFET but is a planar-gate-type MOSFET.

That is, in the MOSFET 200 according to Embodiment 3, as shown in Fig. 13, a semiconductor base substrate 210 has: a base region 218 which is formed on a surface of a first main surface of the semiconductor base substrate 210, a whole surface of a p-type column region 216 and on a portion of a surface of an n-type column region 214; an n-type surface high concentration region 219 formed on a surface of a first main surface of the semiconductor base substrate 210 and on a surface of the n-type column region 214 in a state where the n-type surface high concentration region 219 is disposed adjacently to a base region 218; and an n-type source region 220 formed on a surface of the base region 218. A gate electrode 236 is formed on the surface of the base region 218 sandwiched between source regions 220 and n-type surface high concentration regions 219 by way of gate insulation films 234. A depth position of the n-type surface high concentration region 219 falls within a range of $1.0\mu\text{m}$ to $4.0\mu\text{m}$, and dopant concentration

of the n-type surface high concentration region 219 falls within a range of $1 \times 10^{14} \text{cm}^{-3}$ to $1 \times 10^{16} \text{cm}^{-3}$.

[0080]

In this manner, the MOSFET 200 according to Embodiment 3 differs from the MOSFET 100 according to Embodiment 1 with respect to the point that the MOSFET 200 according to Embodiment 3 is not a trench-gate-type MOSFET but is a planar-gate-type MOSFET. However, in the same manner as the MOSFET 100 according to Embodiment 1, average positive charge density $\rho(x)$ at a predetermined depth position of the super junction structure 217 when the super junction structure 217 is depleted by turning off the MOSFET is expressed by an upward convex curve projecting in a right upward direction. With such a configuration, in a depth position around the gate (a region where x is close to 0), the average positive charge density $\rho(x)$ becomes smaller than (larger on a negative side) a conventional MOSFET 900, and the difference between a charge amount of a negative charge in the p-type column region 216 and a charge amount of a positive charge in the n-type column region 214 becomes large compared to the conventional MOSFET 900. Accordingly, the following advantages can be acquired.

(1) A n-type column region 214 around a gate becomes easily depleted compared to a conventional MOSFET and hence, even when a drain voltage is increased, a potential of the n-type column region 214 around the gate is minimally

increased.

(2) A distance between a non-depleted region in the n-type column region 214 and a gate electrode 236 becomes long and hence, a feedback capacitance C_{rss} becomes small compared to a conventional MOSFET. Accordingly, even when a potential of the n-type column region 214 (the non-depleted region of the n-type column region) is increased along with the increase of a drain voltage which takes place when the MOSFET is turned off, the gate electrode 236 is minimally affected by a change in potential of the n-type column region 214. Accordingly, even when an irregularity exists in a charge balance around the gate, an irregularity in switching characteristics when the MOSFET is turned off can be reduced compared to the prior art.

15 [0081]

The MOSFET 200 according to Embodiment 3 has substantially the same structure as the MOSFET 100 according to Embodiment 1 except for the point that the MOSFET 200 according to Embodiment 3 is not a trench-gate-type MOSFET but is a planar-gate-type MOSFET. Accordingly, the MOSFET 200 according to Embodiment 3 can acquire the advantageous effects by the constitutional parts corresponding to the corresponding constitutional parts of the MOSFET 100 according to Embodiment 1 among the advantageous effects acquired by the MOSFET 100 according to Embodiment 1.

[0082]

[Embodiment 4]

A power conversion circuit 2 according to Embodiment 4 basically has substantially the same structure as the power conversion circuit 1 according to Embodiment 1. However, the power conversion circuit 2 according to Embodiment 4 differs from the power conversion circuit 1 according to Embodiment 1 with respect to a point that the power conversion circuit is a full bridge circuit. That is, the power conversion circuit 2 according to Embodiment 4 includes, as shown in Fig. 14, four MOSFETs 100 (100a to 100d) as MOSFET, and also includes built-in diodes of the respective MOSFETs as rectifying elements.

[0083]

In this manner, the power conversion circuit 2 according to Embodiment 4 differs from the power conversion circuit 1 according to Embodiment 1 with respect to the point that the power conversion circuit 2 is a full bridge circuit. However, in the same manner as the power conversion circuit 1 according to Embodiment 1, average positive charge density $\rho(x)$ at a predetermined depth position of the super junction structure 117 when the super junction structure 117 is depleted by turning off the MOSFET is expressed by an upward convex curve projecting in a right upward direction. With such a configuration, in a depth position around the gate (a region where x is close to 0), the average positive charge density $\rho(x)$ becomes smaller

than (larger on a negative side) a conventional MOSFET 900,
and the difference between a charge amount of a negative charge
in the p-type column region 116 and a charge amount of a positive
charge in the n-type column region 114 becomes large compared
5 to the conventional MOSFET 900. Accordingly, the following
advantages can be acquired.

(1) The n-type column region 114 around the gate becomes
easily depleted compared to a conventional MOSFET and hence,
even when a drain voltage is increased, a potential of the
10 n-type column region 114 around a gate is minimally increased.

(2) A distance between a non-depleted region in the
n-type column region 114 and a gate electrode 126 becomes long
and hence, a feedback capacitance C_{rss} becomes small compared
to the conventional MOSFET. Accordingly, even when a
15 potential of the n-type column region 114 (the non-depleted
region of the n-type column region) is increased along with
the increase of a drain voltage which takes place when the
MOSFET is turned off, the gate electrode 126 is minimally
affected by a change in potential of the n-type column region
20 114. Accordingly, even when an irregularity exists in a charge
balance around the gate, an irregularity in switching
characteristics when the MOSFET is turned off can be reduced
compared to the prior art.

[0084]

25 In the power conversion circuit 2 according to Embodiment

4, average positive charge density $\rho(x)$ at the predetermined depth position in the super junction structure 117 when the super junction structure 117 is depleted by turning off the MOSFET is expressed by an upward convex curve projecting in
5 a right upward direction. Accordingly, as described above, even when a potential of the n-type column region 114 (the non-depleted region of the n-type column region 114) is increased along with the increase of a drain voltage which takes place when the MOSFET is turned off, the gate electrode 126
10 is minimally affected by a change in potential of the n-type column region 114. Accordingly, a phenomenon referred to as false turn-on (erroneous turn-on) minimally occurs.

[0085]

The phenomenon referred to as false turn-on (erroneous
15 turn-on) is a phenomenon where, in a circuit where two or more MOSFETs are connected to each other, when either one of the MOSFETs is turned on, another MOSFET is also turned on by an error due to a change in potential.

[0086]

20 Further, according to the power conversion circuit 2 of Embodiment 4, a rectifier element is the built-in diode in the MOSFET and hence, it is unnecessary to additionally prepare a rectifier element.

[0087]

25 The power conversion circuit 2 according to Embodiment

4 has substantially the same structure as the power conversion circuit 1 according to Embodiment 1 except for the point that the power conversion circuit is a full bridge circuit. Accordingly, the power conversion circuit 2 according to Embodiment 4 can acquire the advantageous effects by the constitutional parts corresponding to the corresponding constitutional parts of the power conversion circuit 2 according to Embodiment 4 among the advantageous effects acquired by the power conversion circuit 1 according to Embodiment 1.

[0088]

Although the present invention has been described with reference to the above-described Embodiments, the present invention is not limited to the above-described Embodiments. The present invention can be carried out in various modes without departing from the gist of the present invention. For example, the following modifications are also conceivable.

[0089]

(1) The numbers, materials, shapes, positions, sizes and the like of the constitutional elements described in the above-mentioned respective Embodiments are provided only for an exemplifying purpose, and can be changed within a scope where advantageous effects of the present invention are not impaired.

[0090]

(2) In the above-mentioned embodiments 1 and 3, a width $w_n(x)$

of the n-type column region at a predetermined depth position is expressed by a monotonous upward convex curve projecting in a right upward direction, and a width $w_p(x)$ of the p-type column region at a predetermined depth position is expressed

5 by a monotonous downward convex curve projecting in a right downward direction. However, the present invention is not limited to such a configuration. For example, the width $w_n(x)$ of the n-type column region at a predetermined depth position may be expressed by a stepped shape (a line (envelope) which

10 connects corner portions of steps forming a monotonous upward convex curve projecting in a right upward direction), and the width w_p of the p-type column region at a predetermined depth position may be expressed by a stepped shape (a line (envelope) which connects corner portions of steps forming a monotonous

15 downward convex curve projecting in a right downward direction) (see Fig. 15). Further, the width $w_n(x)$ of the n-type column region at a predetermined depth position may be expressed by a curve where a concave shape and a convex shape are repeated (an envelope made by the concaves and the convexes

20 forming a monotonous upward convex curve projecting in a right upward direction), and the width w_p of the p-type column region at a predetermined depth position may be expressed by a curve where a concave shape and a convex shape are repeated (an envelope made by the concaves and the convexes forming a

25 monotonous downward convex curve projecting in a right downward

direction)(see Fig. 16).

[0091]

(3) In the above-mentioned Embodiment 2, an average density $N_d(x)$ of a positive charge at a predetermined depth position
5 in the n-type column region is expressed by a monotonous upward convex curve projecting in a right upward direction. However, the present invention is not limited to such a case. For example, an average density $N_d(x)$ of a positive charge at a predetermined depth position in the n-type column region may
10 be expressed by a stepped shape (a line which connects corner portions of steps forming a monotonous upward convex curve projecting in a right upward direction) or may be expressed by a curve where a concave shape and a convex are repeated (an envelope made by the concaves and the convexes forming a
15 monotonous upward convex curve projecting in a right upward direction).

[0092]

(4) In the above-mentioned Embodiment 2, an average density $N_a(x)$ of a negative charge at a predetermined depth position
20 in the p-type column region is expressed by a monotonous downward convex curve projecting in a right downward direction. However, the present invention is not limited to such a case. For example, an average density $N_a(x)$ of a negative charge at a predetermined depth position in the p-type column region may
25 be expressed by a stepped shape (a line which connects corner

portions of steps forming a monotonous downward convex curve projecting in a right downward direction) or may be expressed by a curve where a concave shape and a convex are repeated (an envelope made by the concaves and the convexes forming a monotonous downward convex curve projecting in a right downward direction).

[0093]

(5) In the above-mentioned respective Embodiments, the n-type column region 114, the p-type column region 116, the trench 122 and the gate electrode 126 are formed in a stripe shape as viewed in a plan view. However, the present invention is not limited to such a structure. The n-type column region 114, the p-type column region 116, the trench 122 and the gate electrode 126 may be formed in a circular shape (a columnar shape as viewed stereoscopically), a quadrangular frame shape, a circular frame shape or a grid shape as viewed in a plan view.

[0094]

(6) In the above-mentioned respective Embodiments, a DC power source is used as the power source. However, the present invention is not limited to such a structure. An AC power source may be used as the power source.

[0095]

(7) A chopper circuit is used as the power conversion circuit in the above-mentioned Embodiments 1 to 3, while a full bridge circuit is used as the power conversion circuit in the

above-mentioned Embodiment 4. However, the present invention is not limited to such a structure. As the power conversion circuit, a half bridge circuit, a three-phase AC converter, a non-insulating-type full bridge circuit, a non-insulating-type half bridge circuit, a push-pull circuit, an RCC circuit, a forward converter, a flyback converter or other circuits may be used.

[0096]

(8) A PIN diode is used as the rectifier element in the above-mentioned Embodiments 1 to 3, while a built-in diode of the MOSFET is used as the rectifier element in Embodiment 4. However, the present invention is not limited to such a structure. As the rectifier element, a fast recovery diode such as a JBS or an MPS, silicon-carbide Schottky barrier diodes or other diodes may be used.

[0097]

(9) In the above-mentioned Embodiment 4, as the rectifier element, only a built-in diode of the MOSFET is used. However, the present invention is not limited to such a structure. When a recovery loss of a built-in diode is excessively large, an additional rectifier element may be connected in parallel with the MOSFET.

Explanation of Symbols

[0098]

1, 2: power conversion circuit

10: reactor
 12: first terminal
 14: second terminal
 20: power source
 5 30: rectifier element
 100, 100A, 100a, 100b, 100c, 100d, 102, 104, 106, 200,
 700, 800, 900: MOSFET
 110, 210, 710, 910: semiconductor base substrate
 112, 212, 712, 912: low-resistance semiconductor layer
 10 113, 213, 713, 913: buffer layer
 114, 214, 714, 814, 914: n-type column region
 115, 215, 715, 915: n-type semiconductor layer
 116, 216, 716, 816, 916: p-type column region
 117, 217, 717, 917: super junction structure
 15 118, 218, 718, 818, 918: base region
 219, 919: n-type surface high concentration region
 120, 220, 720, 920: source region
 122, 722, 822: trench
 124, 234, 724, 824, 934: gate insulation film
 20 126, 236, 726, 826, 936: gate electrode
 128, 238, 728: interlayer insulation film
 130, 230, 730, 930: source electrode
 132, 232, 732, 932: drain electrode

CONCLUSIES

1. MOSFET omvattende:

een halfgeleiderbasissubstraat met een super-overgangsstructuur die is gevormd door een n-type kolomgebied en een p-type kolomgebied; en

een poortelektrode gevormd op een eerste hoofdoppervlakzijde van het halfgeleiderbasissubstraat middels een poortisolatiefolie, waarbij

gebruik wordt gemaakt van een diepste positie van een oppervlak van een uitputtingslaag op de eerste hoofdoppervlakzijde wanneer de uitputtingslaag zich het meest uitstrekt in de super-overgangsstructuur door het uitschakelen van de MOSFET als een referentie, in een grafiek waar een diepte x op een voorafbepaalde diepte positie in de super-overgangsstructuur wanneer de super-overgangsstructuur is uitgeput door het uitschakelen van de MOSFET is genomen op een as van abcissen, en een gemiddelde positieve ladingsdichtheid $\rho(x)$ op de voorafbepaalde diepte positie in de super-overgangsstructuur uitgedrukt door een volgende formule (1) wanneer de super-overgangsstructuur is uitgeput door het uitschakelen van de MOSFET is genomen op een as van ordinaten,

de gemiddelde positieve ladingsdichtheid $\rho(x)$ is uitgedrukt door een opwaarts convexe kromme projecterend in een rechts opwaartse richting, en

gebruik wordt gemaakt van een diepste positie van een oppervlak van een uitputtingslaag op de eerste hoofdoppervlakzijde wanneer de uitputtingslaag zich het meest uitstrekt in de super-overgangsstructuur door het uitschakelen van de MOSFET als een referentie, ervan uitgaande dat a een diepte van een oppervlak van de uitputtingslaag op een tweede hoofdoppervlakzijde op een ondiepste positie wanneer de uitputtingslaag zich het meest uitstrekt in de super-overgangsstructuur door het uitschakelen van de MOSFET is, een waarde van de gemiddelde positieve ladingsdichtheid $\rho(0)$ wanneer $x=0$ een negatieve waarde wordt en een waarde van de gemiddelde positieve ladingsdichtheid $\rho(a)$ wanneer $x=a$ een positieve waarde wordt, en

een oppervlakte van een gebied omgeven door een kromme die de gemiddelde positieve ladingsdichtheid $\rho(x)$ uitdrukt, een rechte lijn waar $x=0$ en de as van abcissen gelijk is aan een oppervlakte van een gebied omgeven door de kromme die de gemiddelde positieve ladingsdichtheid $\rho(x)$ uitdrukt, een rechte lijn waar $x=a$ en de as van abcissen.

[Formule 1]

$$\rho(x) = \frac{q}{2w} [w_n(x) \cdot N_d(x) - w_p(x) \cdot N_a(x)] \cdots (1)$$

(In de formule (1), duidt $w_n(x)$ op een breedte van het n-type kolomgebied op de voorafbepaalde diepte positie, duidt $N_d(x)$ op gemiddelde dichtheid van een positieve

lading op de voorafbepaalde dieptepositie in het n-type kolomgebied wanneer de super-overgangsstructuur is uitgeput door het uitschakelen van de MOSFET, duidt $w_p(x)$ op een breedte van het p-type kolomgebied op de voorafbepaalde dieptepositie, duidt $N_a(x)$ op gemiddelde dichtheid van een negatieve lading op de voorafbepaalde dieptepositie in het p-type kolomgebied wanneer de super-overgangsstructuur is uitgeput door het uitschakelen van de MOSFET, duidt q op een elementaire lading, en duidt w op een positieve constante die aan $w_n(x) + w_p(x) = 2w$ voldoet.)

2. MOSFET volgens conclusie 1, waarbij gebruik wordt gemaakt van een diepste positie van een oppervlak van een uitputtingslaag op de eerste hoofdoppervlakzijde wanneer de uitputtingslaag zich het meest uitstrekt in de super-overgangsstructuur door het uitschakelen van de MOSFET als een referentie, er vanuit gaande dat a een diepte van een oppervlak van de uitputtingslaag op de tweede hoofdoppervlakzijde bij een ondiepste positie wanneer de uitputtingslaag zich het meest uitstrekt in de super-overgangsstructuur door het uitschakelen van de MOSFET is, en dat d een diepte van een dieptepositie waar de gemiddelde positieve ladingsdichtheid $\rho(x) > 0$ wordt in de super-overgangsstructuur is, aan een verhouding van $0 < d < a/2$ wordt voldaan.

3. MOSFET volgens conclusie 1 of 2, waarbij in een grafiek waar de diepte x op de voorafbepaalde dieptepositie in de super-overgangsstructuur is genomen op een as van abscissen, en een breedte $w_n(x)$ op de voorafbepaalde dieptepositie in het n-type kolomgebied of een breedte $w_p(x)$ op de voorafbepaalde dieptepositie in het p-type kolomgebied is genomen op een as van ordinaten,

de breedte $w_n(x)$ op de voorafbepaalde dieptepositie in het n-type kolomgebied is uitgedrukt door een opwaarts convexe kromme projecterend in een rechts opwaartse richting, en

de breedte $w_p(x)$ op de voorafbepaalde dieptepositie in het p-type kolomgebied is uitgedrukt door een neerwaartse convexe kromme projecterend in een rechts neerwaartse richting.

4. MOSFET volgens conclusie 1 of 2, waarbij in een grafiek waar de diepte x op de voorafbepaalde dieptepositie in de super-overgangsstructuur is genomen op een as van abscissen, en gemiddelde dichtheid $N_d(x)$ van een positieve lading op de voorafbepaalde dieptepositie in het n-type kolomgebied of gemiddelde dichtheid $N_a(x)$ van een negatieve lading op de voorafbepaalde dieptepositie in het p-type kolomgebied wanneer de super-overgangsstructuur is uitgeput door het uitschakelen van de MOSFET is genomen op een

as van ordinaten,

gemiddelde dichtheid $N_d(x)$ van een positieve lading op de voorafbepaalde dieptepositie in het n-type kolomgebied wanneer de super-overgangsstructuur is uitgeput door het uitschakelen van de MOSFET is uitgedrukt door een opwaartse convexe kromme projecterend in een rechts opwaartse richting, en

gemiddelde dichtheid $N_a(x)$ van een negatieve lading op de voorafbepaalde dieptepositie in het p-type kolomgebied wanneer de super-overgangsstructuur is uitgeput door het uitschakelen van de MOSFET is uitgedrukt door een neerwaartse convexe kromme projecterend in een rechts neerwaartse richting.

5. MOSFET volgens een van de conclusies 1 tot en met 4, waarbij het halfgeleiderbasissubstraat voorts een p-type basisgebied gevormd op een oppervlak van het n-type kolomgebied en een oppervlak van het p-type kolomgebied, en een n-type brongebied gevormd op een oppervlak van het basisgebied omvat,

de MOSFET voorts omvattende, in een gebied waar het n-type kolomgebied is gepositioneerd als gezien vanuit een bovenaanzicht, een sleuf gevormd zodat deze zich vanaf een oppervlak van een eerste hoofdoppervlak van het halfgeleiderbasissubstraat uitstrekt tot aan een dieptepositie dieper dan een diepste deel van het basisgebied en een deel van het brongebied is blootgesteld op een binnenrandoppervlak van de sleuf,

de poortisolatiefolie is gevormd op het binnenrandoppervlak van de sleuf, en de poortelektrode is ingebed in de sleuf middels de poortisolatiefolie.

6. MOSFET volgens een van de conclusies 1 tot en met 4, waarbij het halfgeleiderbasissubstraat voorts omvat: een basisgebied gevormd op een oppervlak van het eerste hoofdoppervlak van het halfgeleiderbasissubstraat, een heel oppervlak van het p-type kolomgebied, en een deel van een oppervlak van het n-type kolomgebied; een n-type oppervlak hoog-concentratiegebied is gevormd op een oppervlak van het eerste hoofdoppervlak van het halfgeleiderbasissubstraat en een oppervlak van het n-type kolomgebied zodat het n-type oppervlak hoog-concentratiegebied is gevormd aangrenzend aan het basisgebied; en een n-type brongebied is gevormd op een oppervlak van het basisgebied, en

de poortelektrode is gevormd op een oppervlak van het basisgebied ingeklemd tussen het brongebied en het n-type oppervlak hoog-concentratiegebied middels de poortisolatiefolie.

7. MOSFET volgens conclusie 5 of 6, waarbij gebruikmakende van een diepste positie van een oppervlak van een uitputtingslaag op de eerste hoofdoppervlakzijde wanneer de uitputtingslaag zich het meest uitstrekt in de super-overgangsstructuur door het uitschakelen van de MOSFET als een referentie, in een grafiek waar een as langs een diepterichting als x-as is ingesteld, een x-coördinaat op een dieptepositie van een laagste oppervlak van het basisgebied als $-t$ is ingesteld, een x-coördinaat op dieptepositie van een laagste deel van het p-type kolomgebied als b is ingesteld, en een x-coördinaat op een dieptepositie waar de gemiddelde positieve ladingsdichtheid $\rho(x) > 0$ wordt als d is ingesteld, aan een verhouding van $0 < t+d < (t+b)/2$ wordt voldaan.

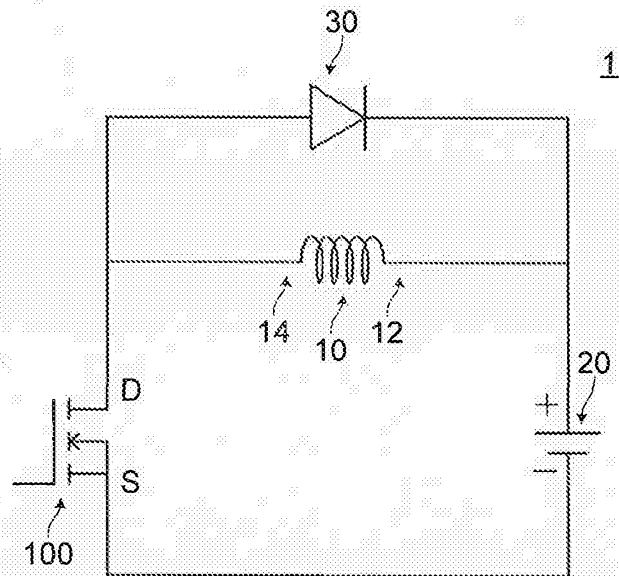
8. Vermogensconversieschakeling ten minste omvattende:
 een zelfinductiespoel;
 een vermogensbron die een elektrische stroom aan de zelfinductiespoel verschaft;
 MOSFET volgens een van de conclusies 1 tot en met 7 voor het beheren van een elektrische stroom verschaft vanuit de vermogensbron aan de zelfinductiespoel; en
 een gelijkrichterelement dat een gelijkrichtende handeling verricht op de elektrische stroom verschaft vanuit de vermogensbron aan de zelfinductiespoel of een elektrische stroom vanuit de zelfinductiespoel.

9. Vermogensconversieschakeling volgens conclusie 8, waarbij het gelijkrichterelement een snel-herstellende diode is.

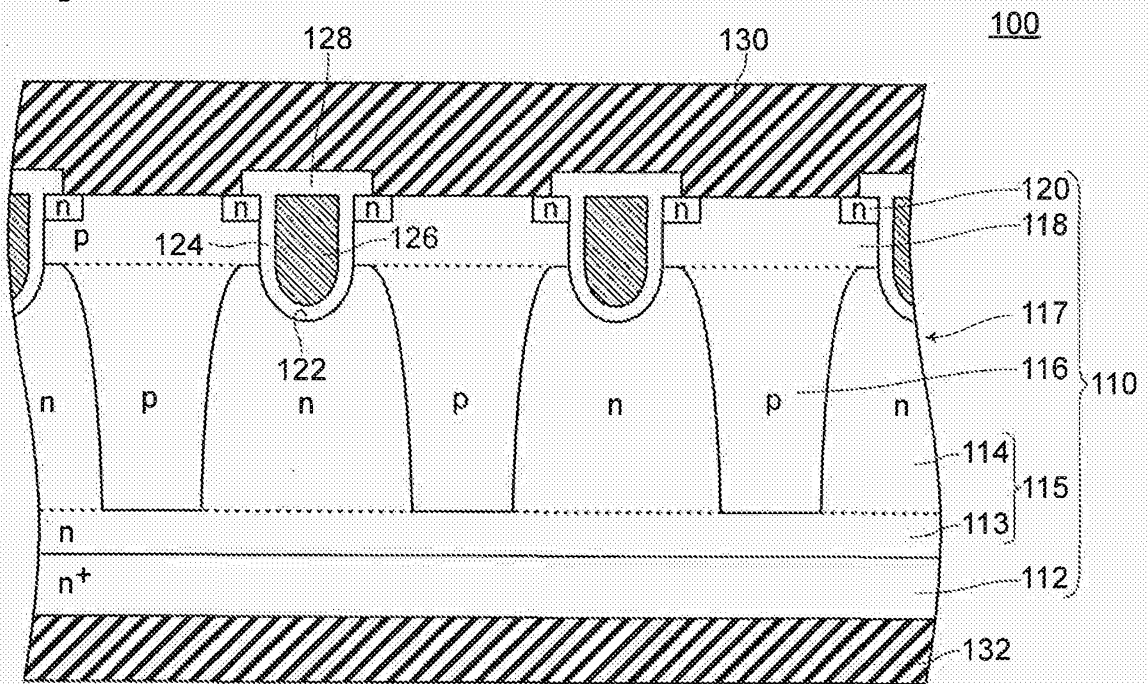
10. Vermogensconversieschakeling volgens conclusie 8, waarbij het gelijkrichterelement een ingebouwde diode van de MOSFET is.

11. Vermogensconversieschakeling volgens conclusie 8, waarbij het gelijkrichterelement een siliciumcarbide Schottky sperdiode is.

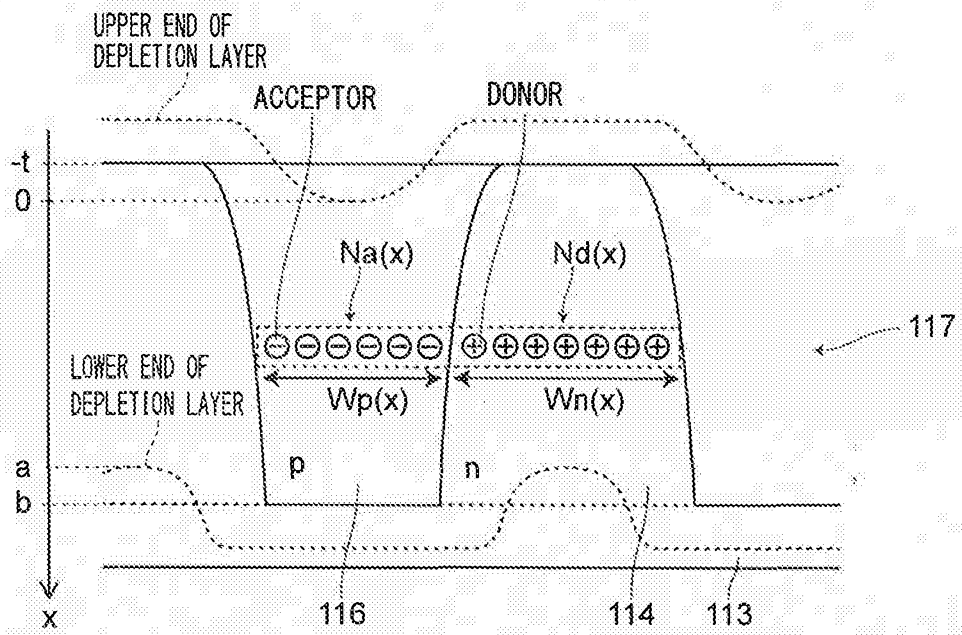
【FIG.1】



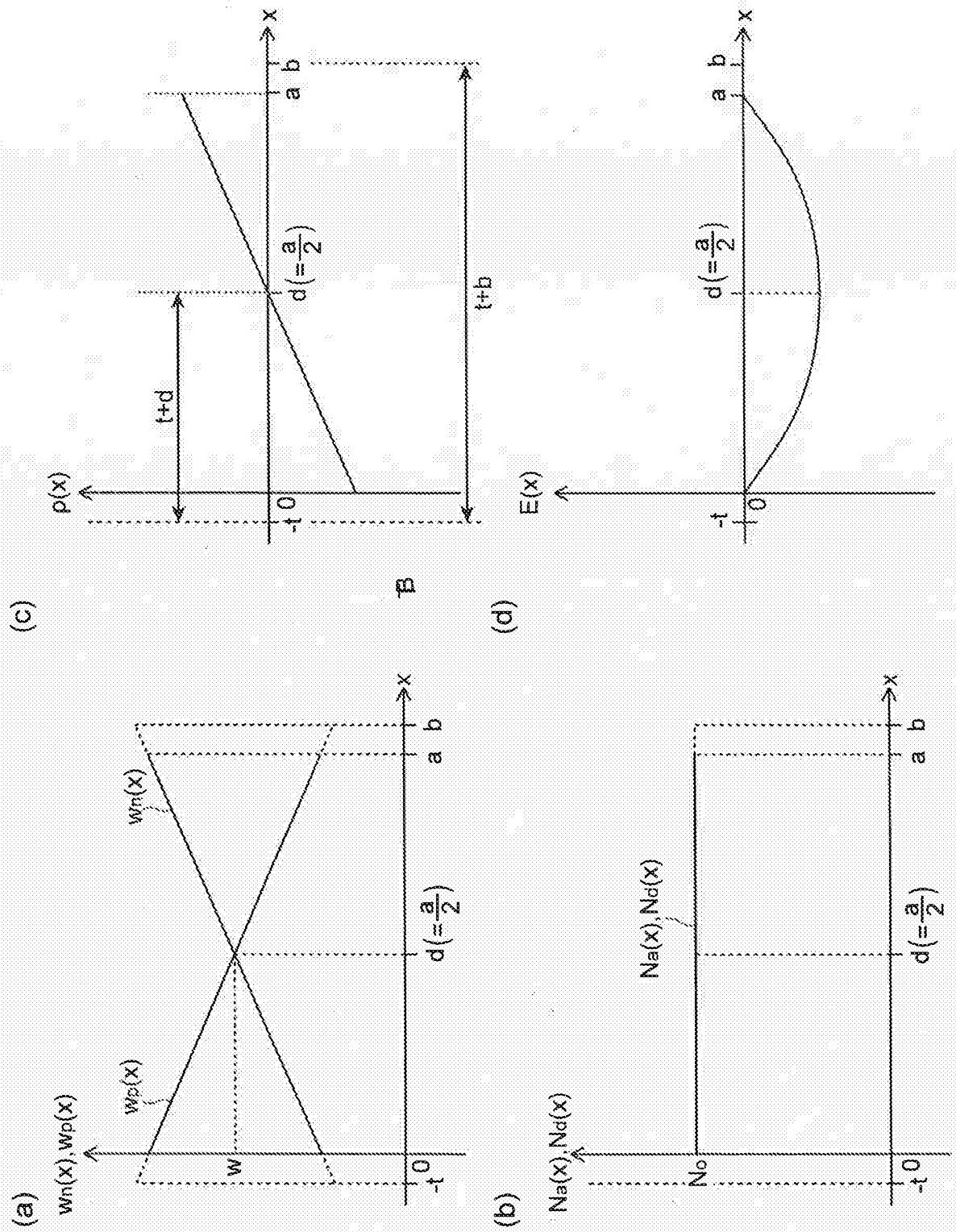
【FIG.2】



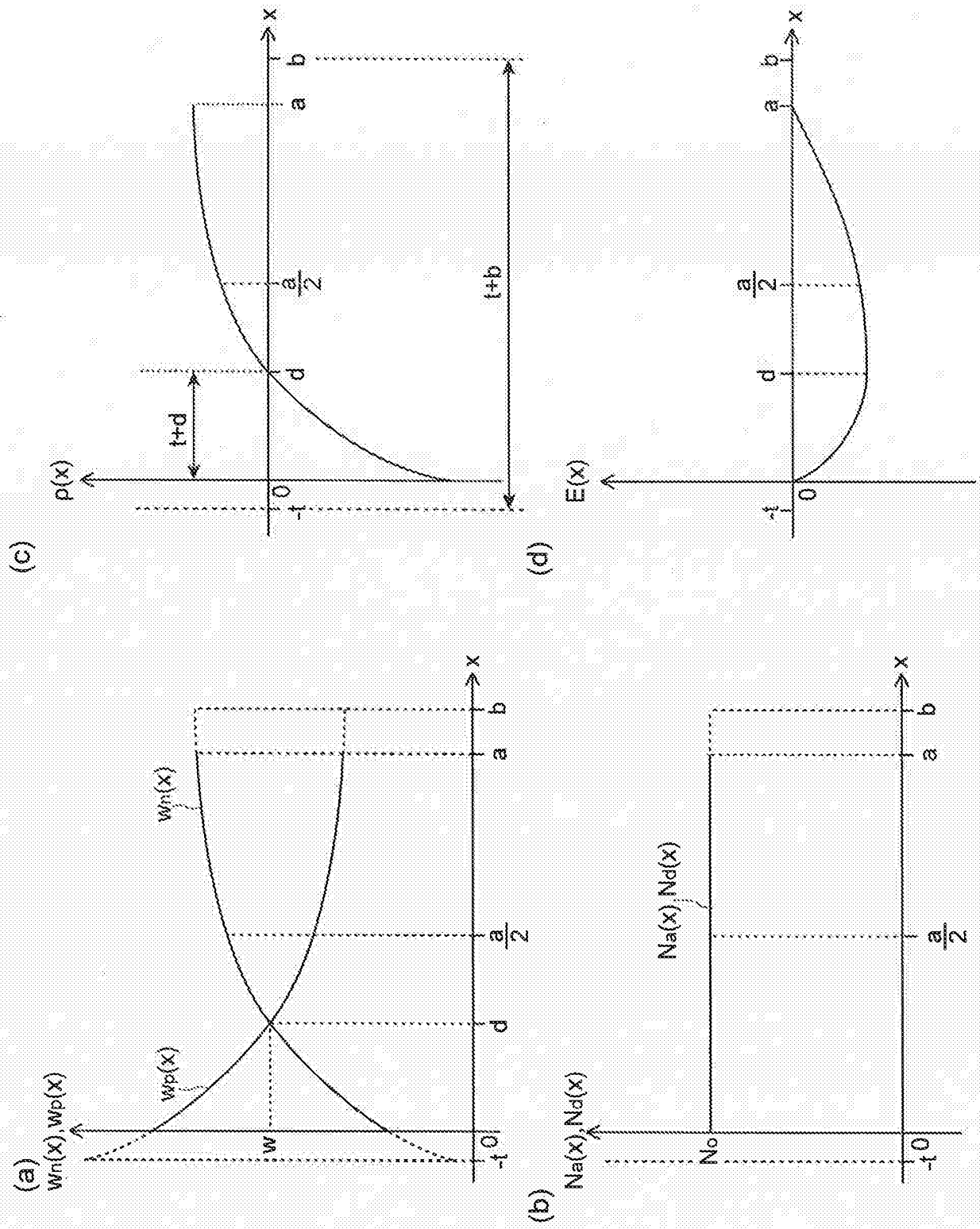
【FIG.3】



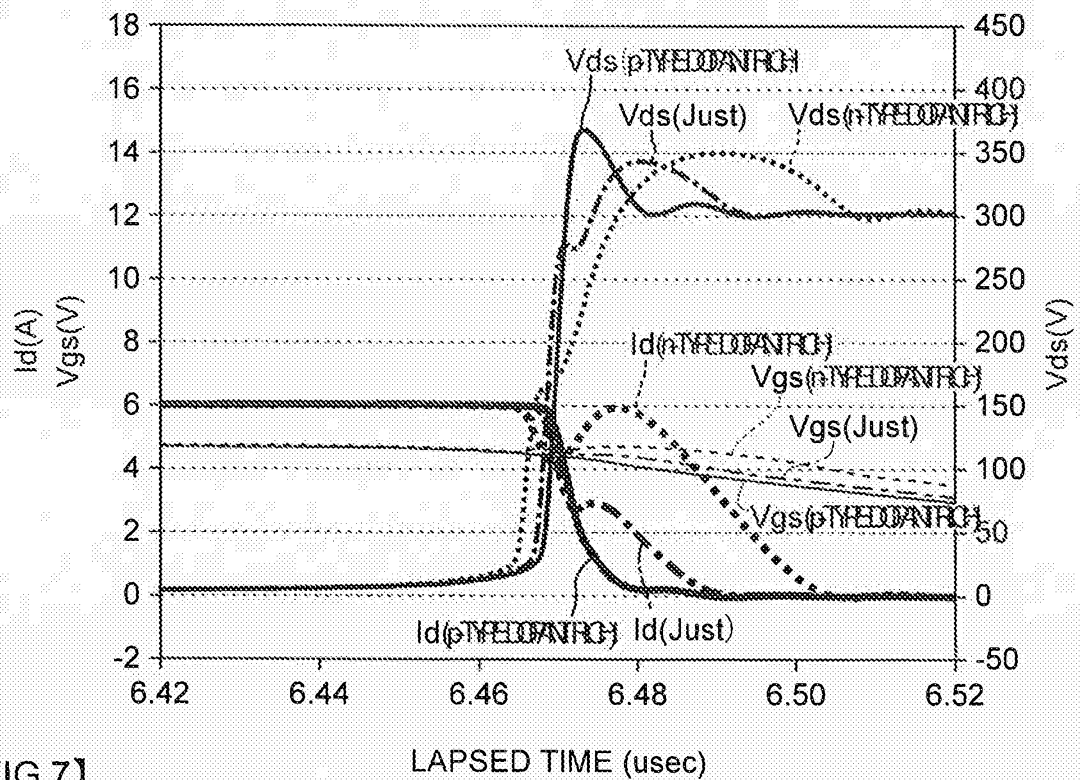
【FIG.4】



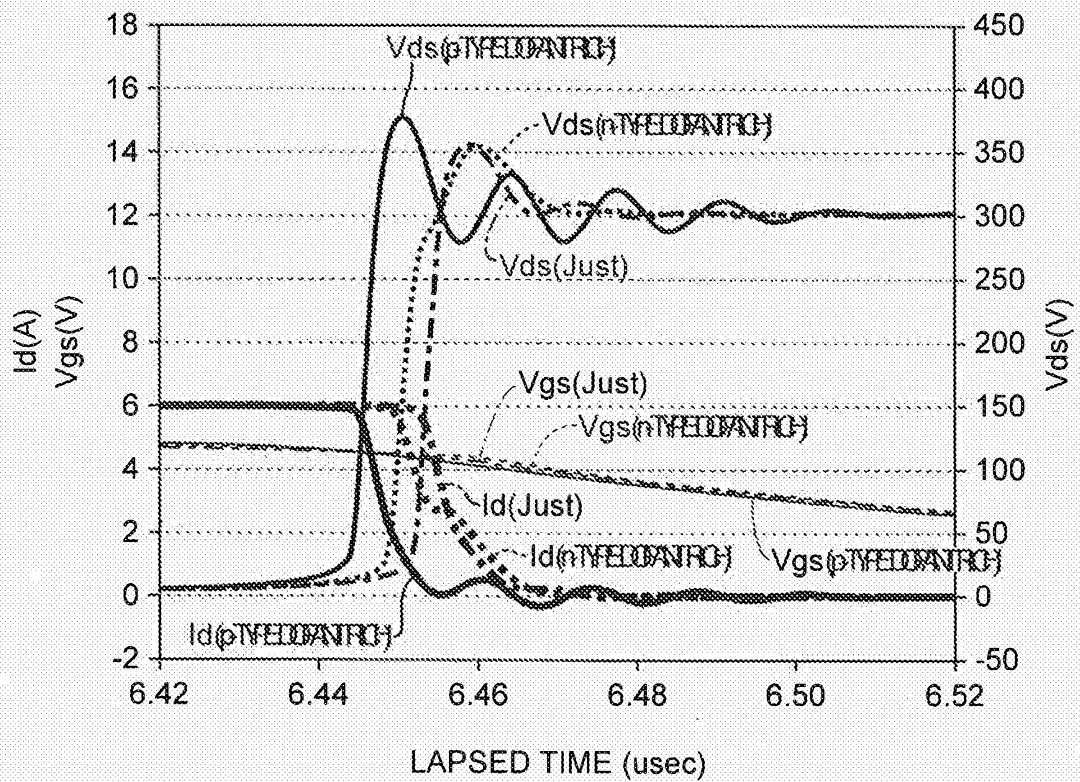
【FIG.5】



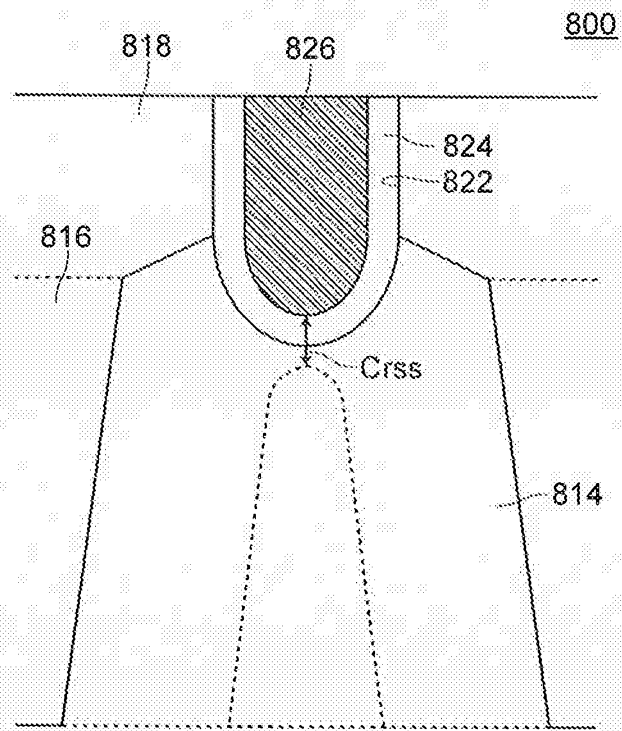
【FIG.6】



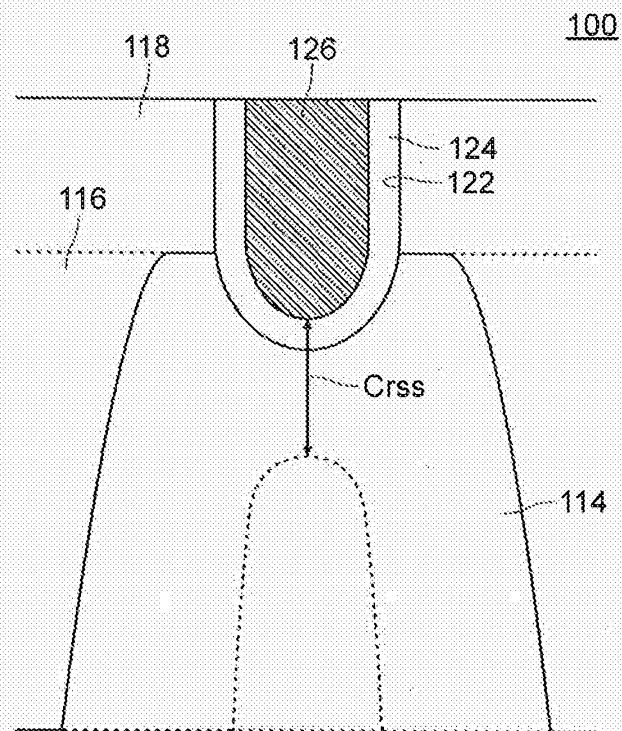
【FIG.7】



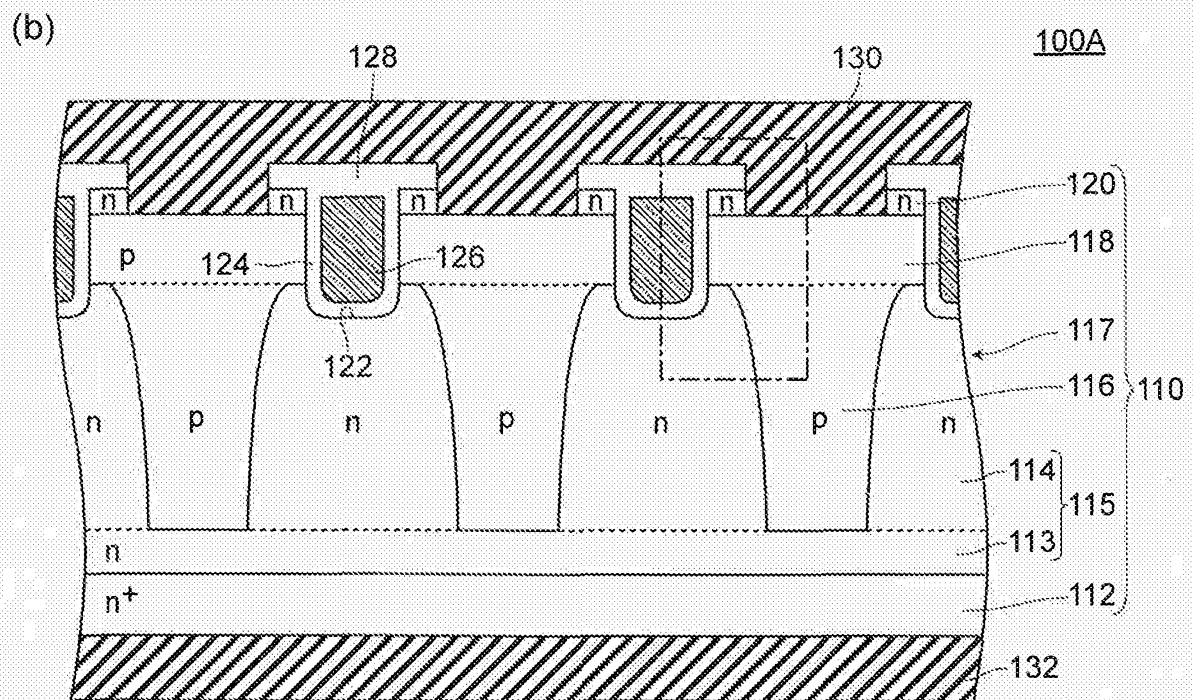
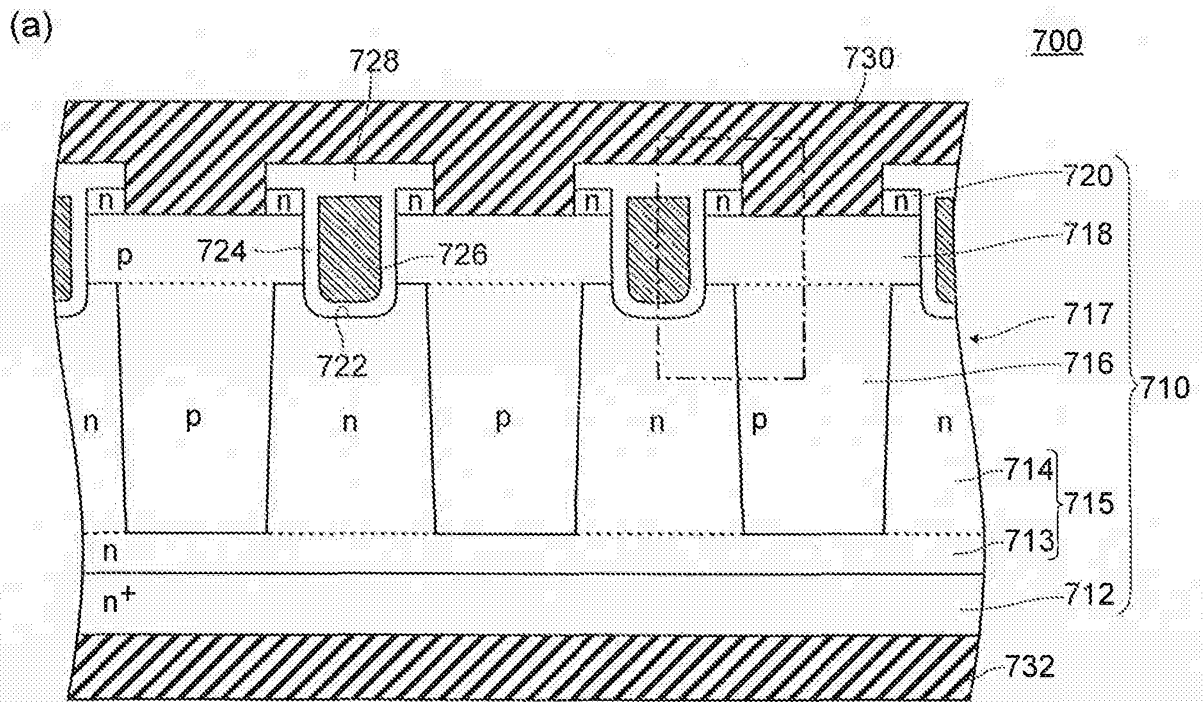
【FIG.8】



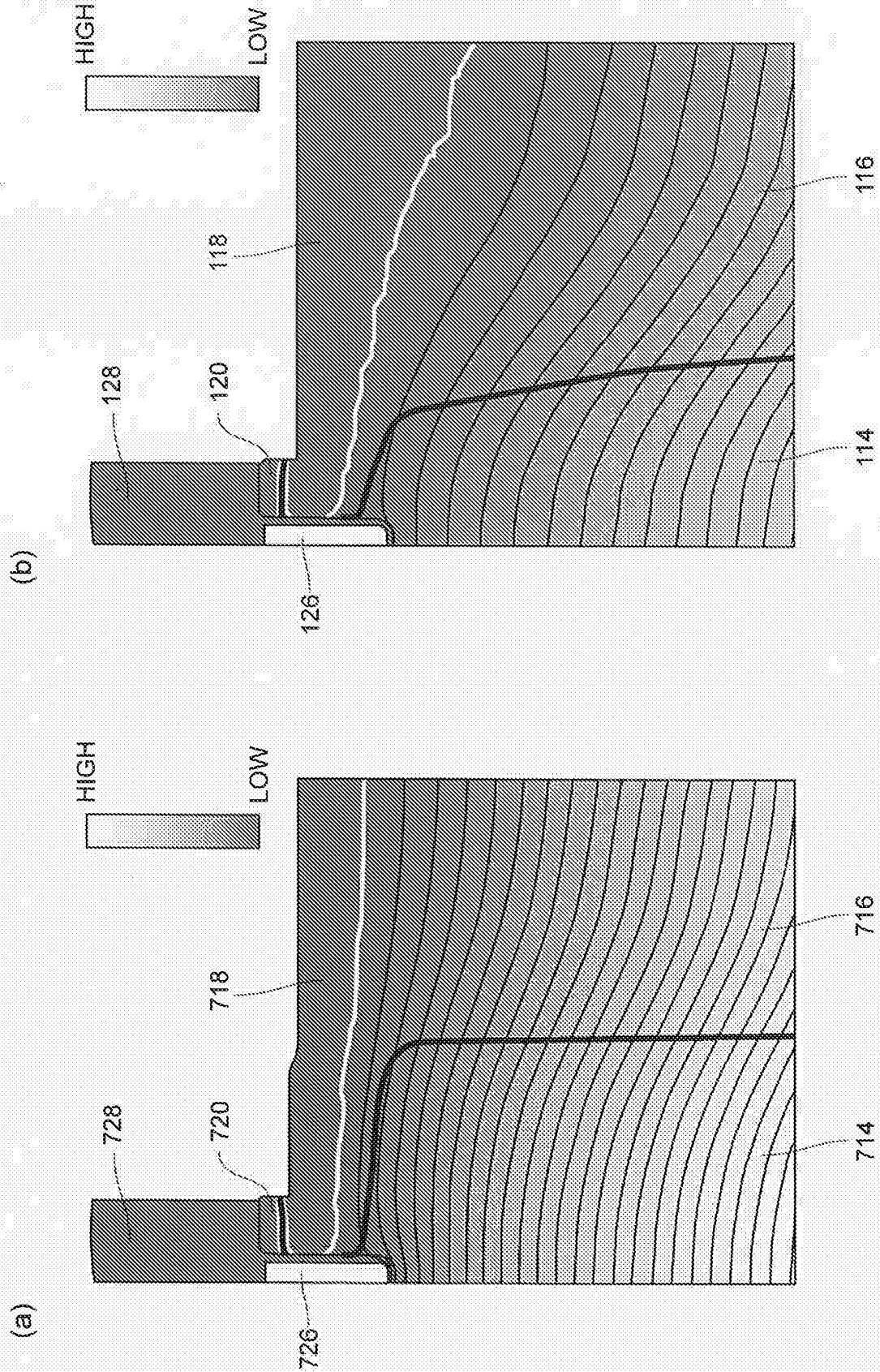
【FIG.9】



【FIG.10】

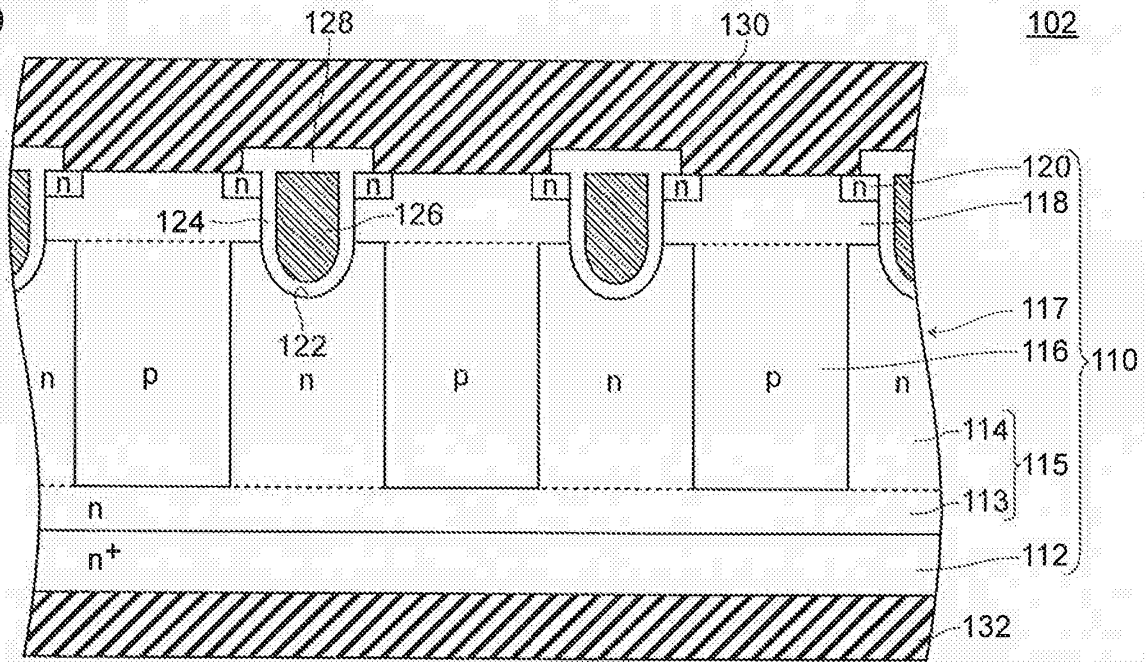
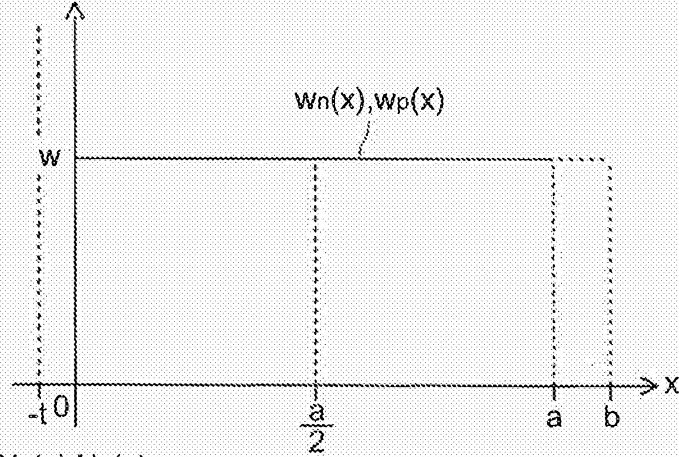
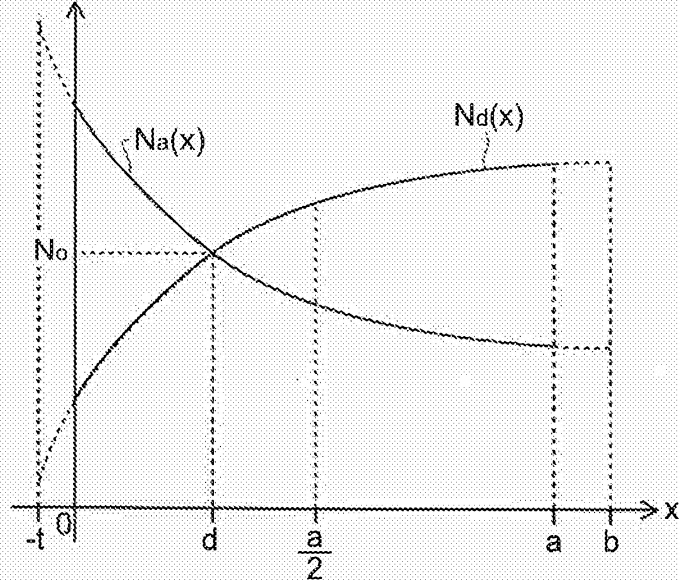


【FIG. 11】

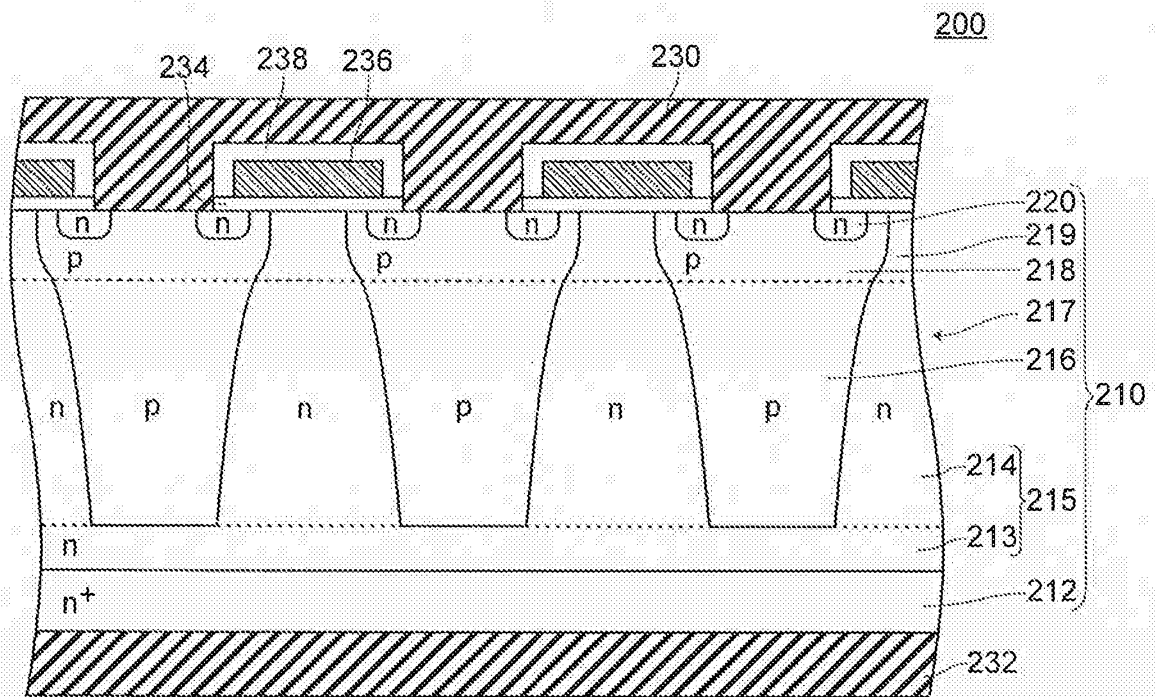


【FIG.12】

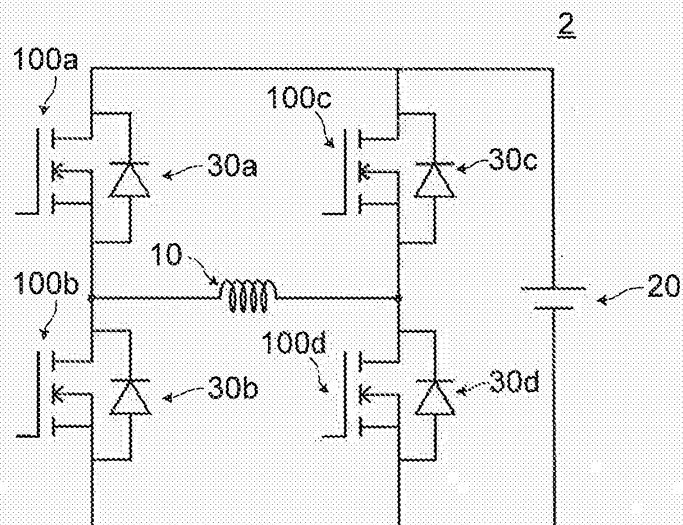
(a)

(b) $w_n(x), w_p(x)$ (c) $N_a(x), N_d(x)$ 

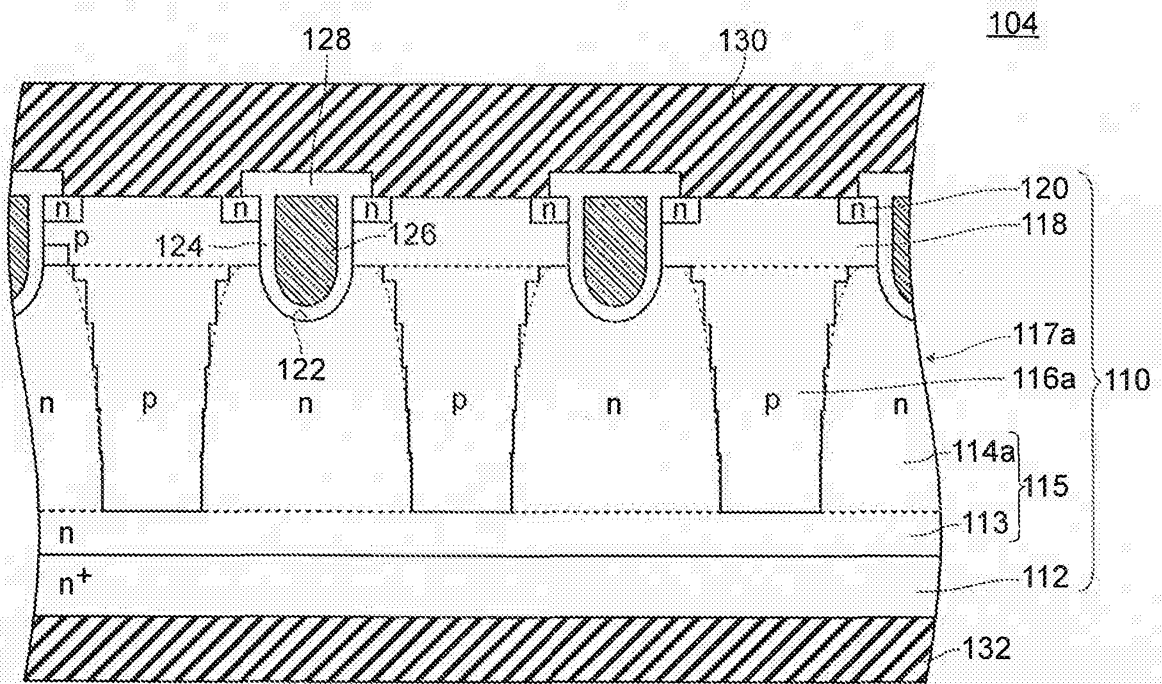
【FIG.13】



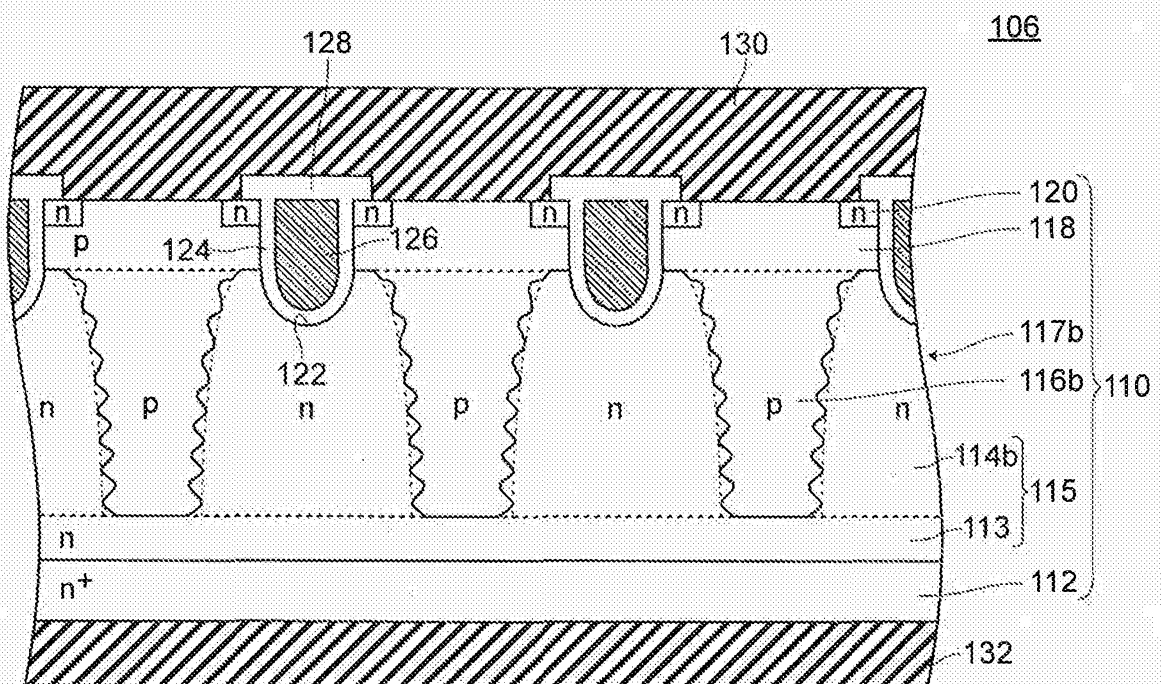
【FIG.14】



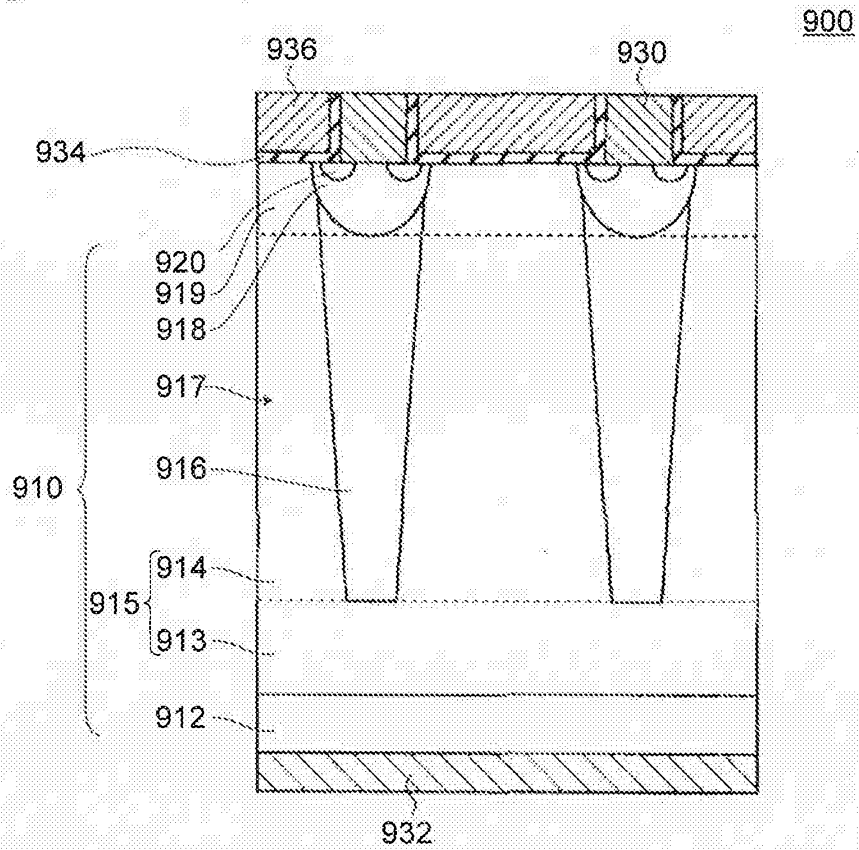
【FIG.15】



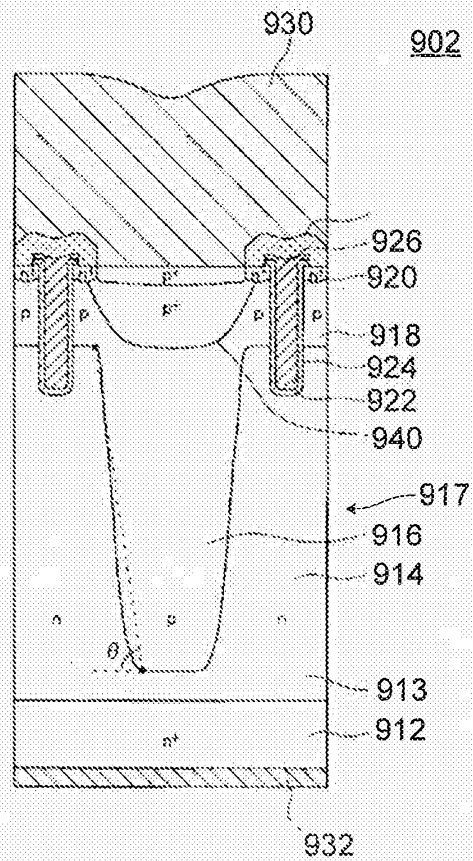
【FIG.16】



【FIG.17】



【FIG.18】



ABSTRACT

A MOSFET 100 according to the present invention includes:
a semiconductor base substrate 110 having a super junction
structure 117; and a gate electrode 126 formed on a first main
5 surface side of the semiconductor base substrate 110 by way
of a gate insulation film 124. In a graph where a depth x at
a predetermined depth position in the super junction structure
117 is taken on an axis of abscissas, and an average positive
charge density $\rho(x)$ at the predetermined depth position in the
10 super junction structure 117 is taken on an axis of ordinates,
the average positive charge density $\rho(x)$ at a predetermined
depth position of the super junction structure 117 when the
super junction structure 117 is depleted by turning off the
MOSFET is expressed by an upward convex curve projecting in
15 a right upward direction. According to MOSFET 100 of the
present invention, even when an irregularity exists in a charge
balance around a gate, an irregularity in switching
characteristics when the MOSFET is turned off can be decreased
compared to a prior art.



ONDERZOEKSRAPPORT

BETREFFENDE HET RESULTAAT VAN HET ONDERZOEK NAAR DE STAND VAN DE TECHNIEK

RELEVANTE LITERATUUR			
Categorie	Literatuur met, voor zover nodig, aanduiding van speciaal van belang zijnde tekstgedeelten of figuren	Van belang voor conclusie(s) nr.	Classificatie (IPC)
X	US 2007/013000 A1 (SHIRAISHI MASAKI [JP]) 18 januari 2007 (2007-01-18)	1,3,5,8,10	INV. H01L29/78
Y	* alinea [0078] - alinea [0089]; figuren	9,11	H01L29/06
A	8-10 *	2,4,6,7	H01L29/08
Y	US 2010/025760 A1 (KAWASHIMA YOSHIYA [JP]) 4 februari 2010 (2010-02-04)	9	
	* alinea [0061] - alinea [0119]; figuren 1-24 *		
Y	US 2006/151806 A1 (FUKUDA KENJI [JP] ET AL) 13 juli 2006 (2006-07-13)	11	
	* alinea [0022] - alinea [0028]; figuur 1 *		
	* alinea [0040] - alinea [0052]; figuur 4 *		
	* alinea [0056]; figuur 6 *		
A	US 2004/038467 A1 (DARWISH MOHAMED N [US] ET AL) 26 februari 2004 (2004-02-26)	1-7	Onderzochte gebieden van de techniek
	* alinea [0051] - alinea [0055]; figuur 5A *		H01L
	* alinea [0071] - alinea [0072]; figuren 12H-K *		
A	US 6 084 264 A (DARWISH MOHAMED N [US]) 4 juli 2000 (2000-07-04)	1-7	
	* kolom 3, regel 64 - kolom 4, regel 47; figuren 3, 8A-9B *		
	* kolom 7, regel 11 - regel 29; figuur 6 *		
	-/--		
Indien gewijzigde conclusies zijn ingediend, heeft dit rapport betrekking op de conclusies ingediend op:			
Plaats van onderzoek: München		Datum waarop het onderzoek werd voltooid: 11 juli 2018	Bevoegd ambtenaar: Lantier, Roberta
CATEGORIE VAN DE VERMEDELDE LITERATUUR			
X: de conclusie wordt als niet nieuw of niet inventief beschouwd ten opzichte van deze literatuur Y: de conclusie wordt als niet inventief beschouwd ten opzichte van de combinatie van deze literatuur met andere geciteerde literatuur van dezelfde categorie, waarbij de combinatie voor de vakman voor de hand liggend wordt geacht A: niet tot de categorie X of Y behorende literatuur die de stand van de techniek beschrijft O: niet-schriftelijke stand van de techniek P: tussen de voorrangsdatum en de indieningsdatum gepubliceerde literatuur T: na de indieningsdatum of de voorrangsdatum gepubliceerde literatuur die niet bezwarend is voor de octrooiaanvraag, maar wordt vermeld ter verheldering van de theorie of het principe dat ten grondslag ligt aan de uitvinding E: eerdere octrooi(aanvraag), gepubliceerd op of na de indieningsdatum, waarin dezelfde uitvinding wordt beschreven D: in de octrooiaanvraag vermeld L: om andere redenen vermelde literatuur S: lid van dezelfde octrooifamilie of overeenkomstige octrooipublicatie			

RELEVANTE LITERATUUR		
Categorie ¹	Literatuur met, voor zover nodig, aanduiding van speciaal van belang zijnde tekstgedeelten of figuren.	Van belang voor conclusie(s) nr.
A	US 5 216 275 A (CHEN XINGBI [CN]) 1 juni 1993 (1993-06-01) * kolom 1, regel 55 - kolom 4, regel 54; figuren 2-5 * -----	1-7

1	<u>CATEGORIE VAN DE VERMELDE LITERATUUR</u>	
	X: de conclusie wordt als niet nieuw of niet inventief beschouwd ten opzichte van deze literatuur Y: de conclusie wordt als niet inventief beschouwd ten opzichte van de combinatie van deze literatuur met andere geïsoleerde literatuur van dezelfde categorie, waarbij de combinatie voor de vakman voor de hand liggend wordt geacht A: niet tot de categorie X of Y behorende literatuur die de stand van de techniek beschrijft O: niet-schriftelijke stand van de techniek P: tussen de voorrangsdatum en de indieningsdatum gepubliceerde literatuur	T: na de indieningsdatum of de voorrangsdatum gepubliceerde literatuur die niet bezwarend is voor de octrooiaanvraag, maar wordt vermeld ter verheldering van de theorie of het principe dat ten grondslag ligt aan de uitvinding E: eerdere octrooi(aanvraag), gepubliceerd op of na de indieningsdatum, waarin dezelfde uitvinding wordt beschreven D: in de octrooiaanvraag vermeld L: om andere redenen vermelde literatuur &: lid van dezelfde octrooifamilie of overeenkomstige octrooipublicatie

**AANHANGSEL BEHORENDE BIJ HET RAPPORT BETREFFENDE
HET ONDERZOEK NAAR DE STAND VAN DE TECHNIEK,
UITGEVOERD IN DE OCTROOIAANVRAGE NR.**

NO 140065
NL 2019845

Het aanhangsel bevat een opgave van elders gepubliceerde octrooiaanvragen of octrooien (zogenaamde leden van dezelfde octroofamilie), die overeenkomen met octrooischriften genoemd in het rapport.

De opgave is samengesteld aan de hand van gegevens uit het computerbestand van het Europees Octrooibureau per
De juistheid en volledigheid van deze opgave wordt noch door het Europees Octrooibureau, noch door het Bureau voor de Industriële eigendom gegarandeerd; de gegevens worden verstrekt voor informatiedoeleinden.

11-07-2018

In het rapport genoemd octrooigeschrift		Datum van publicatie		Overeenkomend(e) geschrift(en)	Datum van publicatie
US 2007013000	A1	18-01-2007	JP	2007027193 A	01-02-2007
			US	2007013000 A1	18-01-2007
US 2010025760	A1	04-02-2010	JP	2010056510 A	11-03-2010
			US	2010025760 A1	04-02-2010
US 2006151806	A1	13-07-2006	AU	2003284665 A1	18-06-2004
			DE	10393777 T5	20-10-2005
			JP	4340757 B2	07-10-2009
			JP	W02004049449 A1	30-03-2006
			KR	20050084685 A	26-08-2005
			US	2006151806 A1	13-07-2006
			US	2009057686 A1	05-03-2009
			WO	2004049449 A1	10-06-2004
US 2004038467	A1	26-02-2004	AU	2003300924 A1	29-07-2004
			DE	10393853 B4	02-10-2013
			DE	10393853 T5	28-12-2006
			JP	4388017 B2	24-12-2009
			JP	2006511974 A	06-04-2006
			US	2004038467 A1	26-02-2004
			US	2004227182 A1	18-11-2004
			WO	2004061975 A1	22-07-2004
US 6084264	A	04-07-2000	DE	69936090 T2	14-02-2008
			EP	1014450 A2	28-06-2000
			JP	4601092 B2	22-12-2010
			JP	2000164869 A	16-06-2000
			US	6084264 A	04-07-2000
US 5216275	A	01-06-1993	CN	1056018 A	06-11-1991
			US	5216275 A	01-06-1993

SCHRIFTELIJKE OPINIE

DOSSIER NUMMER NO140065	INDIENINGSDATUM 02.11.2017	VOORRANGSDATUM 11.11.2016	AANVRAAGNUMMER NL2019845
CLASSIFICATIE INV. H01L29/78 H01L29/06 H01L29/08			
AANVRAGER Shindengen Electric Manufacturing Co., Ltd			

Deze schriftelijke opinie bevat een toelichting op de volgende onderdelen:

- ☒ Onderdeel I Basis van de schriftelijke opinie
- ☐ Onderdeel II Voorrang
- ☐ Onderdeel III Vaststelling nieuwheid, inventiviteit en industriële toepasbaarheid niet mogelijk
- ☐ Onderdeel IV De aanvraag heeft betrekking op meer dan één uitvinding
- ☒ Onderdeel V Gemotiveerde verklaring ten aanzien van nieuwheid, inventiviteit en industriële toepasbaarheid
- ☐ Onderdeel VI Andere geciteerde documenten
- ☐ Onderdeel VII Overige gebreken
- ☒ Onderdeel VIII Overige opmerkingen

	DE BEVOEGDE AMBTENAAR Lantier, Roberta
--	---

SCHRIFTELIJKE OPINIE

Aanvraag nr.:

NL2019845

Onderdeel I Basis van de Schriftelijke Opinie

1. Deze schriftelijke opinie is opgesteld op basis van de meest recente conclusies ingediend voor aanvang van het onderzoek.
2. Met betrekking tot **nucleotide en/of aminozuur sequenties** die genoemd worden in de aanvraag en relevant zijn voor de uitvinding zoals beschreven in de conclusies, is dit onderzoek gedaan op basis van:
 - a. type materiaal:
 - ☐ sequentie opsomming
 - ☐ tabel met betrekking tot de sequentie lijst
 - b. vorm van het materiaal:
 - ☐ op papier
 - ☐ in elektronische vorm
 - c. moment van indiening/aanlevering:
 - ☐ opgenomen in de aanvraag zoals ingediend
 - ☐ samen met de aanvraag elektronisch ingediend
 - ☐ later aangeleverd voor het onderzoek
3. ☐ In geval er meer dan één versie of kopie van een sequentie opsomming of tabel met betrekking op een sequentie is ingediend of aangeleverd, zijn de benodigde verklaringen ingediend dat de informatie in de latere of additionele kopieën identiek is aan de aanvraag zoals ingediend of niet meer informatie bevatten dan de aanvraag zoals oorspronkelijk werd ingediend.
4. Overige opmerkingen:

SCHRIFTELIJKE OPINIE

Aanvraag nr. NL2019845

Onderdeel V Gemotiveerde verklaring ten aanzien van nieuwheid, inventiviteit en industriële toepasbaarheid

1. Verklaring

Nieuwheid	Ja: Conclusies 2, 4, 6, 7, 9, 11 Nee: Conclusies 1, 3, 5, 8, 10
Inventiviteit	Ja: Conclusies 2, 4, 6, 7 Nee: Conclusies 1, 3, 5, 8-11
Industriële toepasbaarheid	Ja: Conclusies 1-11 Nee: Conclusies

2. Citaties en toelichting:

Zie aparte bladzijde

Onderdeel VIII Overige opmerkingen

De volgende opmerkingen met betrekking tot de duidelijkheid van de conclusies, beschrijving, en figuren, of met betrekking tot de vraag of de conclusies nawerkbaar zijn, worden gemaakt:

Zie aparte bladzijde

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

- 1 Reference is made to the following documents:
 - D1 US 2007/013000 A1 (SHIRAISHI MASAKI [JP]) 18 januari 2007 (2007-01-18)
 - D2 US 5 216 275 A (CHEN XINGBI [CN]) 1 juni 1993 (1993-06-01)
 - D3 US 2010/025760 A1 (KAWASHIMA YOSHIYA [JP]) 4 februari 2010 (2010-02-04)
 - D4 US 2006/151806 A1 (FUKUDA KENJI [JP] ET AL) 13 juli 2006 (2006-07-13)
- 2 The below-mentioned lack of clarity notwithstanding, the subject-matter of claims 1, 3, 5, 8, 10 is not new and the subject-matter of claims 9 and 11 does not involve an inventive step, the criteria of patentability are therefore not met.
- 2.1 Document D1 (see D1: Fig. 8 considered together with Figs. 9A-D and pars. [0078-0086]), the references in parentheses apply to this document) discloses a semiconductor substrate having a super junction (SJ) structure including an n-type column region (15) and a p-type column region (14), and a gate electrode (5) formed on a first main surface side of the semiconductor substrate via a gate insulating film (4).

The therein disclosed not linear variations of the thickness of the two column regions evidently result in an average positive charge density, as defined in the present application, having an upward convex profile projecting in a right upward direction from a negative to a positive value.

Since this structure is explicitly indicated as a superjunction structure, it is evident that a charge balance is realized in this structure (straightforward feature in view of D2: col. 3, l. 7-19), no other options are explicitly disclosed. Since the total charge in the n-type column region (15) and the total charge in the p-type column region (14) are substantially equal, this corresponds to the area underlying the average positive charge density $\rho(x)$ curve where this density has a negative value being equal to the area underlying the average positive charge density $\rho(x)$ curve where this density has a positive value.

The subject-matter of claim 1 is therefore not new.

- 2.2 Dependent claims 3, 5, 8-11 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of novelty and/or inventive step, see the following:
- 2.2.1 Regarding claim 3, consider that in the device of Fig. 8 of D1 the width of the n-type column (15) is represented by an upwardly convex upward sloping curve in the depth direction x and a width of the p-type column (14) is represented by a downwardly convex downward curve in the depth direction x.
- 2.2.2 Regarding claim 5, consider the trench gate (4,5) in Fig. 8 of D1.
- 2.2.3 Regarding claims 8 and 10, consider the power conversion circuit disclosed in Fig. 10 and pars. [0087-0089] of D1 including a reactor (smoothing inductor L), a power source (DRIVER IC) and MOSFETs that can be designed as the one of Fig. 8 of D1. In this circuit of Fig. 10 a built-in diode of the MOSFET is disclosed.
- 2.2.4 Regarding claim 9, this corresponds to a well known design option for the circuit of Fig. 10 of D1, see e.g. document D3 (D3: Figs. 1 - 24 and pars. [0061-0119]) disclosing a vertical MOSFET (20) with a superjunction structure structurally integrated with a fast recovery diode (30).
- 2.2.5 Regarding claim 11, this corresponds to a well known design option for circuits similar to the one of Fig. 10 of D1, see e. g. document D4 (D4: Fig. 6 and par. [0056] together with Figs. 1 and 4 and pars. [0022-0028], [0040-0052])
- 3 The combination of the features of dependent claim 2 is neither known from, nor rendered obvious by, the available prior art. The reasons are as follows. Document D1 is regarded as being the prior art closest to the subject-matter of claim 2. This document does not disclose explicitly at which depth the average positive charge density (as defined in claim 1 of the present application) becomes 0.
Designing the depth where the average positive charge density becomes 0 in the range indicated in present claim 2 leads to an easier depletion of the n-type column around the trench.
This feature thus provides the following advantages:
- a minimal increase of the potential around the gate, even when the drain voltage is increased;
 - a reduced gate-drain capacitance, because a distance between a non-

depleted region in the n-type column and the gate electrode becomes longer when compared to a conventional MOSFET.

Re Item VIII

Certain observations on the application

1. Claim1 is not clear. In present claim 1 the regions having equal area are not well defined, because not specifying between which points on the axis of abscissas they have to be considered. In order to overcome this objection it is suggested to add the following feature "the axis of abscissas until the x point where the average positive charge density $\rho(x)=0$ ".