(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) **World Intellectual Property Organization**
International Bureau

(43) **International Publication Date**
25 September 2014 (25.09.2014)

WIPO | PCT

(10) **International Publication Number**
WO 2014/149581 A1

(51) **International Patent Classification**:
H04L 12/40 (2006.01) *H04L 25/02* (2006.01)

(21) **International Application Number**:
PCT/US2014/019733

(22) **International Filing Date**:
1 March 2014 (01.03.2014)

(25) **Filing Language**: English

(26) **Publication Language**: English

(30) **Priority Data**:
13/842,386 15 March 2013 (15.03.2013) US

(71) **Applicant**: **MICROCHIP TECHNOLOGY INCORPORATED** [US/US]; 2355 West Chandler Blvd., Chandler, AZ 85224-6199 (US).

(72) **Inventors**: **DEVAL, Philippe**; Chemin De La Combe 3, CH-1095 Lutry (CH). **FERNANDEZ, Marija**; Route De Plaines Du Loup 36, CH-1018 Lausanne (CH). **BESSEUX, Patrick**; Route De L'etraz 6, CH-1185 Mont-sur-Rolle (CH).

(74) **Agent**: **SLAYDEN, II, Bruce, W.**; King & Spalding LLP, 401 Congress Ave., Suite 3200, Austin, TX 78701 (US).

(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

[Continued on next page]

(54) **Title**: MULTI-CURRENT HARMONIZED PATHS FOR LOW POWER LOCAL INTERCONNECT NETWORK (LIN) RECEIVER

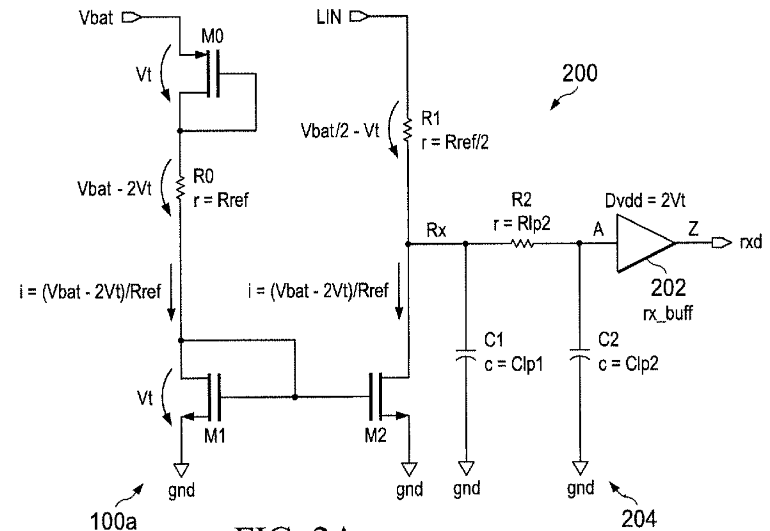


FIG. 2A

(57) **Abstract**: A LIN receiver includes a single, low power structure for both sleep and silent modes, with a single comparator for detecting LIN signaling during both sleep and silent modes as well as during active mode. In some embodiments, full receiving capability is implemented with a current as low as 5 microamps. In particular, dominant and recessive levels for the wakeup bloc are identical to those of standard LIN levels, fixed at about 3.5 V. Consequently, full LIN receiving capability is available during sleep mode.

WO 2014/149581 A1

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

MULTI-CURRENT HARMONIZED PATHS FOR LOW POWER LOCAL INTERCONNECT NETWORK (LIN) RECEIVER

BACKGROUND

TECHNICAL FIELD

The present disclosure relates to local interconnect networks (LIN) and, particularly, to local interconnect network receivers.

DESCRIPTION OF THE RELATED ART

The Local Interconnect Network (LIN) is a serial network protocol used for communicating between components in vehicles. It is defined as a time-triggered, master-slave network, eliminating the need for arbitration among simultaneously reporting devices. It is implemented using a single wire communications bus, which reduces wiring and harness requirements and thus helps save weight, space and cost.

Defined specifically for low-cost implementation of vehicle sub-network applications by the LIN Consortium, the LIN protocol achieves significant cost reduction since it is fairly simple and operates via an asynchronous serial interface (UART/SCI), and the slave nodes are self-synchronizing and can use an on-chip RC oscillator instead of crystals or ceramic resonators.

In order to maintain total current consumption in a LIN network at acceptable levels, increasing the number of slave nodes in a LIN network requires lower and lower current consumption for each of the nodes.

LIN network operational modes include an active mode with full receiving and transmitting capability; a silent (low-power) mode, in which full receiving capability, but no transmitting capability, is provided; and a sleep (power-down) mode, in which only waking-up capability is enabled. Current consumption in silent mode is about 50 microamps, while that in sleep mode is about 5 – 10 microamps. Thus, a consumer needing only receiving capability has to operate in silent mode, consuming 50 microamps.

Usually, the silent mode and the sleep mode functionality are implemented using distinct dedicated blocs in a given integrated circuit.

In particular, LIN bus signaling thresholds for "dominant" (logic low) and "recessive" (logic high) levels are centered on half the battery voltage (Vbat/2), with a 0.1Vbat hysteresis typically required. That is, the recessive-to-dominant threshold is approximately 0.45*Vbat, while the dominant-to-recessive threshold is approximately 0.55*Vbat. Consequently, a window comparator is required to identify bus signals. However, Vbat can range from 6-30 V, which requires wide common mode range compliance for a window comparator. That is, Vbat/2 (and the LIN signal) voltages can dramatically exceed the input voltage range of a window comparator during voltage modes (i.e., silent and operational). As a consequence, matched voltage dividers are commonly used to generate matched fractions of the Vbat/2 and LIN voltages that stay within the input voltage range of the window comparator.

Because significant overhead (a voltage regulator, external bias, etc.) around the voltage mode window comparator is required, overall current consumption of the LIN receiver in voltage mode exceeds requirements during sleep mode. Thus, the voltage mode LIN receiver comparator cannot be used as the wake circuit comparator.

In order to save power during sleep mode, the wake circuit comparator typically compares the LIN bus voltage to a transistor Vt (threshold voltage) or a sum of transistors Vt. This results in a very simple and low-power circuit, but on the other hand, it requires as well a constant detection level, in the range of 3.5-4V, rather than the standard half battery voltage Vbat/2. Thus the wake circuit cannot be used for receiving bus data.

SUMMARY

These and other drawbacks in the prior art are overcome in large part by a system and method according to embodiments of the present invention.

A LIN receiver in accordance with some embodiments includes a single, low power structure for both sleep and silent modes, with a single comparator for detecting LIN signaling during both sleep and silent modes as well as during active mode. In some embodiments, full receiving capability is implemented with a current lower than 10 microamps, and as low as 5 microamps. In particular, dominant and recessive levels for this receiver, when used as the wakeup bloc, are identical to those of standard LIN levels, half the battery voltage (Vbat/2), rather than fixed at about 3.5-4V for the basic wake receiver. Consequently, full LIN receiving capability is available during sleep mode.

A local interconnect network receiver, in accordance with embodiments includes a battery voltage input; an input from a local interconnect network (LIN) bus; and a current mirror configured to mirror a current defined by a reference resistor coupled to the battery voltage input in a sense resistor, such that a voltage at an output point of the sense resistor defines dominant and recessive states of the LIN bus in silent and sleep modes. A local interconnect network (LIN) receiver in accordance with embodiments includes a common circuit configured to detect dominant and recessive states of a LIN bus during active, silent and sleep modes. In some embodiments, the common circuit includes a current mirror configured to mirror a current defined by a reference resistor coupled to a battery voltage input in a sense resistor, such that a voltage at an output point of the sense resistor defines dominant and recessive states of the LIN bus.

A method, according to embodiments includes operating a local interconnect network (LIN) receiver in a sleep mode; operating the LIN receiver in a silent mode; wherein operating in the sleep mode and operating in the silent/active modes comprise detecting dominant and recessive states of a LIN bus using a common circuit. In some embodiments, the common circuit includes a current mirror configured to mirror a current defined by a reference resistor coupled to a battery voltage input in a sense resistor, such that a voltage at an output point of the sense resistor defines dominant and recessive states of the LIN bus.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings. The use of the same reference symbols in different drawings indicates similar or identical items.

FIG. 1 is a diagram illustrating exemplary circuit operation.

FIG. 2A – FIG. 2C are diagrams illustrating exemplary receivers according to various embodiments.

FIG. 3 is a diagram illustrating an exemplary receiver according to embodiments.

FIG. 4 is a diagram illustrating an exemplary supply and comparator circuit according to embodiments.

FIG. 5 is a diagram illustrating an exemplary receiver according to embodiments.

FIG. 6 is a diagram illustrating an exemplary receiver according to embodiments.

FIG. 7 is a diagram illustrating an exemplary circuit according to embodiments.

DETAILED DESCRIPTION

The disclosure and various features and advantageous details thereof are explained more fully with reference to the exemplary, and therefore non-limiting, embodiments illustrated in the accompanying drawings and detailed in the following description. Descriptions of known programming techniques, computer software, hardware, operating platforms and protocols may be omitted so as not to unnecessarily obscure the disclosure in detail. It should be understood, however, that the detailed description and the specific examples, while indicating the preferred embodiments, are given by way of illustration only and not by way of limitation. Various substitutions, modifications, additions and/or rearrangements within the spirit and/or scope of the underlying inventive concept will become apparent to those skilled in the art from this disclosure.

As used herein, the terms “comprises,” “comprising,” "includes," "including," "has," "having," or any other variation thereof, are intended to cover a non-exclusive inclusion. For example, a process, product, article, or apparatus that comprises a list of elements is not necessarily limited only those elements but may include other elements not expressly listed or inherent to such process, process, article, or apparatus. Further, unless expressly stated to the contrary, "or" refers to an inclusive or and not to an exclusive or. For example, a condition A or B is satisfied by any one of the following: A is true (or present) and B is false (or not present), A is false (or not present) and B is true (or present), and both A and B are true (or present).

Additionally, any examples or illustrations given herein are not to be regarded in any way as restrictions on, limits to, or express definitions of, any term or terms with which they are utilized. Instead these examples or illustrations are to be regarded as being described with respect to one particular embodiment and as illustrative only. Those of ordinary skill in the art will appreciate that any term or terms with which these examples or illustrations are utilized encompass other embodiments as well as implementations and adaptations thereof which may or may not be given therewith or elsewhere in the specification and all such embodiments are intended to be included within the scope of that term or terms. Language designating such non-limiting examples and illustrations includes, but is not limited to: “for example,” ”for instance,” “e.g.,” “in one embodiment,” and the like.

As noted above, typical LIN receiving circuits require separate circuitry for silent/active modes and sleep mode signal detection/functionality. As will be discussed in greater detail below, a LIN receiver in accordance with some embodiments includes a single, low power structure for both sleep and silent/active modes. In particular, dominant and recessive levels for the wakeup bloc are identical to those of standard LIN levels, fixed at half the battery voltage (Vbat/2). Consequently, full LIN receiving capability is available during sleep mode. That is, a single circuit is provided that meets all LIN requirements for sleep and silent/active mode operation in a compact structure.

Turning now to FIG. 1, a diagram illustrating operation of an embodiment of a LIN receiver input circuit 100 is shown. As will be explained in greater detail below, hysteresis is implemented through the mirroring ratio. A reference resistor R0 is coupled between Vbat and Ground (GND). A sense resistor R1 having half the value of the reference resistor (R0/2) is coupled to Vlin. The current in the reference resistor Vbat/R0. This current is mirrored in the sense resistor, inducing a voltage drop of Vbat/2. The voltage at the cold point of the sense resistor (Vrxd) is measured.

According to the LIN specification, when Vlin is greater than Vbat/2, the LIN bus is recessive, whereas if it is less than Vbat/2, it is dominant. Since Vrxd = Vlin – Vbat/2, when

Vrxd is positive, the LIN bus is recessive, while when Vrxd is negative, the LIN bus is dominant.

A simplified diagram of an exemplary receiver 200 in accordance with embodiments is shown in FIG. 2A. More particularly, the circuit includes a current mirror input 100a, similar to that of FIG. 1, a lowpass filter 204, and a digital output buffer 202. The current mirror circuit 100a includes a gain compensation diode-connected MOS M0 coupled between the reference resistor R0 and Vbat. Since the voltage across each of the diode-connected MOSFETs M0, M1 is Vt, the voltage across R0 is Vbat – 2 Vt, and the current is (Vbat – 2Vt)/R0. The voltage drop across the sense resistor R1 is then Vbat/2 – Vt. The sense resistor R1's cold point RX is driven through the mirror output and is connected to the input of the lowpass filter 204. The digital output buffer 202 is supplied by a digital voltage equal to 2 Vt, as will be discussed in greater detail below. Its input threshold is therefore Vt. Thus, when Vlin is greater than Vbat/2, Vrx is greater than Vt and Rxd = 1 (recessive). When Vlin is less than Vbat/2, Vrx is less than Vt, and Rxd = 0 (dominant).

An x*Vbat hysteresis can be achieved by changing the fixed mirroring ratio of the current mirror to a RX level dependent ratio as shown in FIG. 2B. The M2 transistor of FIG. 2A is split into two transistors M20 and M21 providing, respectively, a mirroring ratio of (1-x) and 2x, and a switch M22 is added in series with M21. The switch M22 is driven through an inverter 206 that is controlled by the RX output rxd.

When RX output is recessive (high) the output of inverter 206 is low and the M22 switch is off. The voltage drop on R1 is thus (1-x) of its nominal value and the threshold is changed to (1-x)*Vbat/2 + x*Vt, i.e., approximately (1-x)*Vbat/2 since Vt is small compared to Vbat. As soon as Lbus (LIN) falls below the (1-x)*Vbat/2, the RX output becomes low, the output of the inverter 206 goes high and M22 is turned "on". The threshold is thus changed to (1+x)*Vbat/2 + x*Vt, i.e., approximately (1+x)*Vbat/2 since Vt is small compared to Vbat. This creates the x*Vbat hysteresis. In order to create the typical 10% Vbat hysteresis, x is thus set to 0.1. That is, the recessive-to-dominant threshold is approximately 0.45*Vbat, while the dominant-to-recessive threshold is approximately 0.55*Vbat.

It is noted that, while a particular low pass filtering technique has been illustrated (low pass filter 204), many low pass filtering techniques may be employed. For example, active filtering as shown in FIG.2C may be employed. In the example receiver 203 illustrated, the cold point of low pass filtering capacitor C2 (FIG. 2A) is connected to the z output of buffer 202. In other embodiments, the C1 cold point could be connected to z output of buffer 202 instead. Other configurations are possible.

Another example of a receiver circuit in accordance with embodiments is shown with reference to FIG. 3. In particular, the circuit 300 illustrates digital output buffer 202 in greater detail. Generally similar to the circuit 200 of FIG. 2A, the circuit 300 includes a transistor M3 which supplies a current Ibias to supply 304, which generates the 2 Vt bias voltage Dvdd. The comparator 302 receives the output RX_LP of the lowpass filter 204 and has a threshold of Vt.

The Vdd supply and comparator is shown in greater detail in FIG. 4. As shown, the supply 304 includes transistors P0 and N1-N4 while the comparator includes transistors P5, P7, N6, and N8. The Vdd receives input current Ibias at transistor N2 and battery voltage Vbat at transistor N3. The P0 and N1 transistors generate the 2 Vt bias voltage corresponding to Vt across the M0 transistor of FIGS. 2A-2C and 3. N3 provides a buffered copy of this voltage at its source. N2 provides the gate voltage of N3, while N4 that mirrors the N1 current provides the required bias current Ibias for N3. The P5-N6 and P7-N8 transistors operate as two inverters in series operating as a comparator having a threshold of Vt (1/2 * 2 Vt). The output node of P5-N6 inverter may be used as the inverted output zn for driving the hysteresis monitoring switch M22 (FIG. 2B).

The above-described embodiments provide a simple and efficient way for detecting the bus level (recessive or dominant). However, it may additionally be necessary to consider the voltage swing at node RX. With the structure described in FIGS. 2A-2C and FIG. 3, the voltage at nodes RX and RX_LP (FIG. 3) will range from close to zero (gnd) during a dominant bus level up to close to Vbat/2 during a recessive level on the bus. This may exceed the safe input operating range of the digital buffer 202 that in many applications use low voltage (LV) devices. Therefore, some embodiments provide a clamping network at node

RX. A receiver circuit according to embodiments implementing an exemplary clamp is shown in FIG. 5. It is noted that other clamping networks may be provided.

As shown in FIG. 5, an M4 PMOS device having its drain connected to ground, its gate connected to Dvdd supply (=2Vt), and its source connected to RX, is used. With M4, the voltage on node RX is now limited to 3Vt on the positive side, and it is limited to –Uj (where Uj is a junction voltage) on the negative side. With M4, the maximum swing range of node RX is thus restricted to (+3Vt,-Uj) range. Since the Vt voltage is almost equal to Uj in many implementations, this range can be rewritten as (+3Vt,-Vt). Thus, this range is almost centered on the receiver threshold that is equal to Vt. As shown, the clamping induces a symmetrical behavior versus the receiver threshold and thus prevents strong degradation of the receiver characteristics when HF interferences are superimposed to the original bus signal. However, a slight degradation may remain. Therefore, pre-filtering may be needed. A simple way for achieving this pre-filtering is shown in the receiver 205 of FIG. 5. The resistor R1 = Rref/2 is now split into three series elements (R10, R11 and R12) of Rref/6, keeping its total value equal to Rref/2. In addition, two capacitors C3 and C4 are connected to the created intermediate points in order to implement this pre-filtering function.

It is noted that in the above descriptions, the current mirror ratio without hysteresis was set to 1 (Isense=Iref) and Rsense/Rref ratio was set to ½. That is, Rsense*Isense is equal to 0.5* Rref*Iref in order to have the voltage drop across the sense resistor equal to half the voltage across the reference resistance. Therefore, any current mirror Isense/Iref ratio may be used. The only condition to fulfill is having Rref/Rsense = 2 * Isense/Iref (or Isense/Iref = 0.5 * Rref/Rsense) , where Isense/Iref is the mirroring ratio without hysteresis..

High voltage (HV) capacitors may be required for the pre-filtering network. Usually HV capacitors have poor sheet capacitance and may require significantly larger layout area than Rsense (R10+R11+R12) area for meeting the required RC time constant of the pre-filtering network. Therefore, in some implementations, the Rsense value and HV capacitor value are determined based on which values will provide the smallest overall layout area for the pre-filtering section. The current mirror gain (G) may then be determined using the following equation: G = Isense/Iref = 0.5* Rref/Rsense (without hysteresis).

FIG. 6 shows a schematic of a simple very low power LIN receiver 600 based on various of the techniques described above.

It is noted that the high level of rxd signal available at the output of this receiver is equal to 2Vt, which may be a too low level to be processed by the rest of the whole transceiver circuitry (not shown). Therefore in many applications it will be applied to a level-shifter that will convert it up to the required level for processing by the rest of the transceiver circuitry. Techniques for level-shifting up signals are well known and thus are not described here.

In some embodiments, rather than a clamp, a dual mirror current mode approach can be used. Such a circuit is shown in FIG. 7. The sensing Vbat section based on compensating diode MP0, reference resistor R0, and reference current mirror MN0, MN1 is unchanged. However the sense resistor R1 is now connected to the input of a LIN MN3, MN2 mirror. The MN1 output reference current is mirrored in a MP1, MP2 mirror and summed with LIN current mirror output (MN2 output current), creating a current comparator. The current comparator has an inverted output. Thus inverter inv1 is provided to restore the correct polarity of the Rxd received signal. In the embodiment illustrated, all current mirror ratios are assumed to be 1 and MP1/MP2 current mirror is supplied by the digital Dvdd supply voltage, but any other supply voltage may be used.

In operation, when the LIN bus voltage is greater than Vbat/2 (recessive), the current in the sense resistor R1 is greater than the current in the reference resistor R0. The MN2 current is thus larger than the MP2 current and the Rxn node is low. Once inverted, the Rxd output is high reflecting a recessive level on the LIN bus. When the LIN bus voltage is less than Vbat/2 (dominant) the LIN sense current is lower than the reference current. The MN2 current is thus lower than the MP2 current and Rxn node is high. Once inverted, the Rxd output is high reflecting a dominant level on the bus. With this approach, battery and bus voltage info may be provided through additional MN4 and MN5 transistors (dashed).

As noted above, in the embodiment of FIG. 7, the mirrors ratios without hysteresis may be set to 1 for simplicity. In some embodiments, they can differ from 1. Without hysteresis, the rule to apply is Gain(MN2/MN3) = 2*R1/R0 * Gain(MN1/MN0) *

Gain(MP2/MP1) in order to have the voltage drop across the sense resistor R1 equal to half the voltage across the reference resistance R0 .

Although the foregoing specification describes specific embodiments, numerous changes in the details of the embodiments disclosed herein and additional embodiments will be apparent to, and may be made by, persons of ordinary skill in the art having reference to this description. In this context, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of this disclosure. Accordingly, the scope of the present disclosure should be determined by the following claims and their legal equivalents.

CLAIMS

WHAT IS CLAIMED IS:

1. A local interconnect network receiver, comprising:
a battery voltage input;
an input from a local interconnect network (LIN) bus; and
a current mirror configured to mirror a current defined by a reference resistor coupled to the battery voltage input in a sense resistance, such that a voltage at an output point of the sense resistance defines dominant and recessive states of the LIN bus in active, silent and sleep modes.

2. The local interconnect network receiver of claim 1, including a diode connected between the battery voltage input and the reference resistor.

3. The local interconnect network receiver of claim 1, wherein the sense resistance has half a value of the reference resistor.

4. The local interconnect network receiver of claim 2, including a lowpass filter coupled at the output point of the sense resistance.

5. The local interconnect network receiver of claim 3, wherein the sense resistance comprises a single resistor.

6. The local interconnect network receiver of claim 3, wherein the sense resistance comprises a plurality of resistors.

7. The local interconnect network receiver of claim 6, further including a plurality of capacitors at intermediate points between the resistors.

8. The local interconnect network receiver of claim 4, further including circuitry for compensating for voltage swing at an input of the lowpass filter.

9. The local interconnect network receiver of claim 8, wherein the circuitry for compensating for voltage swing comprises a clamping network.

10. The local interconnect network receiver of claim 8, wherein the circuitry for compensating for voltage swing comprises dual mirror common mode circuitry.

11. The local interconnect network receiver of claim 4, including an output buffer coupled to the lowpass filter and having a input threshold corresponding to a voltage drop across the diode.

12. The local interconnect network receiver of claim 11, wherein the diode is a diode-connected MOS transistor.

13. The local interconnect network receiver of claim 1, wherein power consumption is substantially similar at both sleep and silent modes.

14. The local interconnect network receiver of claim 1, the current mirror implementing hysteresis by switchably selecting differing mirroring ratios.

15. A local interconnect network (LIN) receiver, comprising:

a common circuit configured to detect dominant and recessive states of a LIN bus during active, silent and sleep modes.

16. A LIN receiver in accordance with claim 15, wherein the common circuit includes a current mirror configured to mirror a current defined by a reference resistance coupled to a battery voltage input in a sense resistor, such that a voltage at an output point of the sense resistance defines dominant and recessive states of the LIN bus.

17. The local interconnect network receiver of claim 16, including a diode connected between the battery voltage input and the reference resistance.

18. The local interconnect network receiver of claim 17, wherein the mirroring ratio and the ratio between the reference and the sense resistor are sized in such a way that the voltage drop across the sense resistance is half the voltage drop across the reference resistance.

19. The local interconnect network receiver of claim 18, including a lowpass filter coupled at the output point of the sense resistance.

20. The local interconnect network receiver of claim 18, wherein the sense resistance comprises a single resistor.

21. The local interconnect network receiver of claim 18, wherein the sense resistance comprises a plurality of resistors.

22. The local interconnect network receiver of claim 21, further including a plurality of capacitors at intermediate points between the resistors.

23. The local interconnect network receiver of claim 19, further including circuitry for compensating for voltage swing at an input of the lowpass filter.

24. The local interconnect network receiver of claim 23, wherein the circuitry for compensating for voltage swing comprises a clamping network.

25. The local interconnect network receiver of claim 23, wherein the circuitry for compensating for voltage swing comprises dual mirror common mode circuitry.

26. The local interconnect network receiver of claim 19, including an output buffer coupled to the lowpass filter and having a input threshold corresponding to a voltage drop across the diode.

27. The local interconnect network receiver of claim 26, wherein the diode is a diode-connected MOS transistor.

28. The local interconnect network receiver of claim 16, wherein power consumption is substantially similar at both sleep and silent modes.

29. The local interconnect network receiver of claim 16, wherein current consumption during sleep mode is proportional to a battery voltage.

30. The local interconnect network receiver of claim 16, the current mirror implementing hysteresis by switchably selecting differing mirroring ratios.

31. A method, comprising:

operating a local interconnect network (LIN) receiver in a sleep mode;

operating the LIN receiver in a silent mode;

operating the LIN receiver in an active mode;

wherein operating in the sleep mode and operating in the silent and active modes comprise detecting dominant and recessive states of a LIN bus using a common circuit.

32. The method of claim 31, wherein the common circuit includes a current mirror configured to mirror a current defined by a reference resistance coupled to a battery voltage input in a sense resistance, such that a voltage at an output point of the sense resistance defines dominant and recessive states of the LIN bus.

33. The method of claim 32, including a diode connected between the battery voltage input and a reference resistance.

34. The method of claim 33, wherein the mirroring ratio and the ratio between the reference and the sense resistor are sized in such a way that the voltage drop across the sense resistance is half the voltage drop across the reference resistance.

35. The method of claim 33, including a lowpass filter coupled at the output point of the sense resistance.

36. The method of claim 34, wherein the sense resistance comprises a single resistor.

37. The method of claim 34, wherein the sense resistance comprises a plurality of resistors.

38. The method of claim 37, further including a plurality of capacitors at intermediate points between the resistors.

39. The method of claim 35, further including circuitry for compensating for voltage swing at an input of the lowpass filter.

40. The method of claim 39, wherein the circuitry for compensating for voltage swing comprises a clamping network.

41. The method of claim 39, wherein the circuitry for compensating for voltage swing comprises dual mirror common mode circuitry.

42. The method of claim 35, including an output buffer coupled to the lowpass filter and having a input threshold corresponding to a voltage drop across the diode.

43. The method of claim 33, wherein the diode is a diode-connected MOS transistor.

44. The method of claim 32, wherein power consumption is substantially similar at both sleep and silent modes.

45. The method of claim 32, wherein current consumption during sleep mode is proportional to a battery voltage.

46. The method of claim 32, the current mirror implementing hysteresis by switchably selecting differing mirroring ratios.

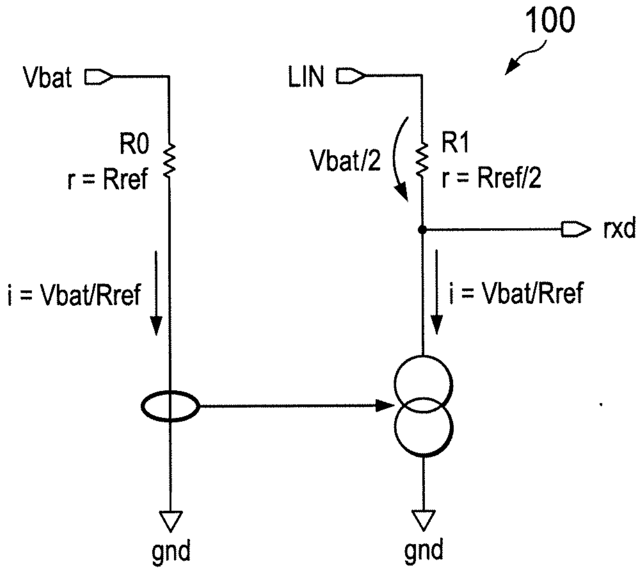

100
Vbat
LIN
R0
r = Rref
Vbat/2
R1
r = Rref/2
rxd
i = Vbat/Rref
i = Vbat/Rref
gnd
gnd

FIG. 1

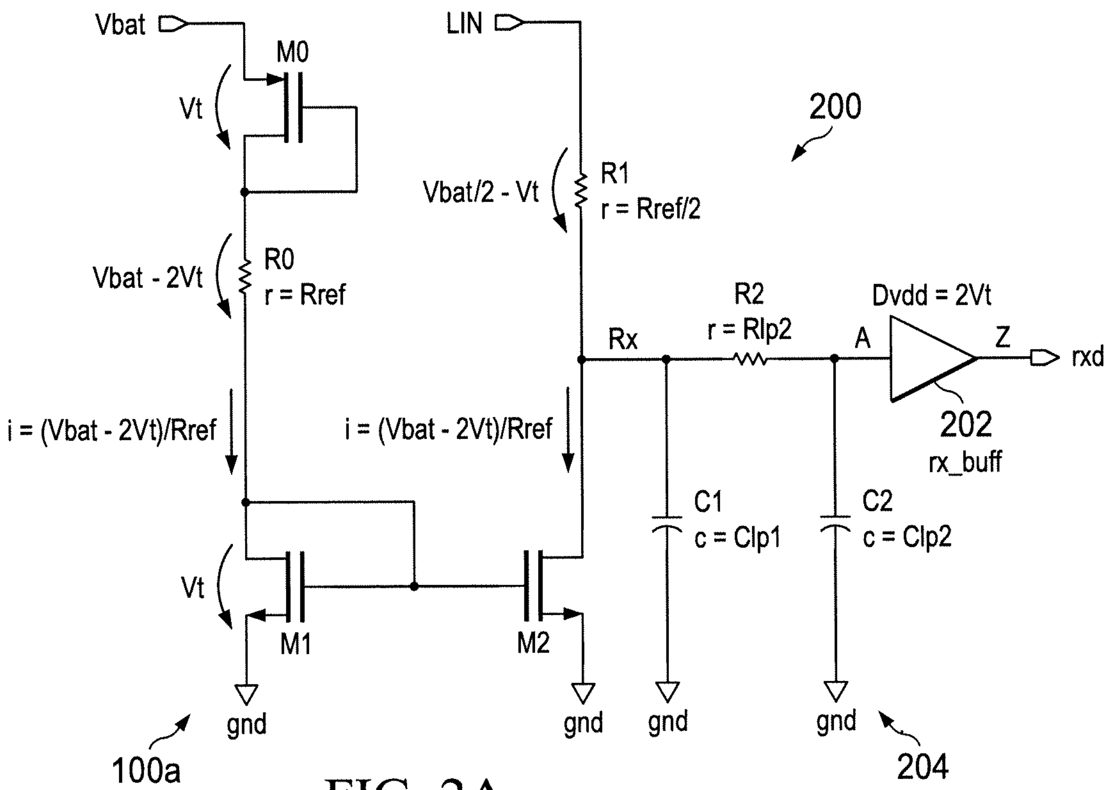

Vbat
LIN
M0
Vt
200
Vbat/2 - Vt
R1
r = Rref/2
Vbat - 2Vt
R0
r = Rref
Rx
R2
r = Rlp2
Dvdd = 2Vt
A
Z
rxd
202
rx_buff
i = (Vbat - 2Vt)/Rref
i = (Vbat - 2Vt)/Rref
C1
c = Clp1
C2
c = Clp2
Vt
M1
M2
gnd
gnd
gnd
gnd
100a
204

FIG. 2A

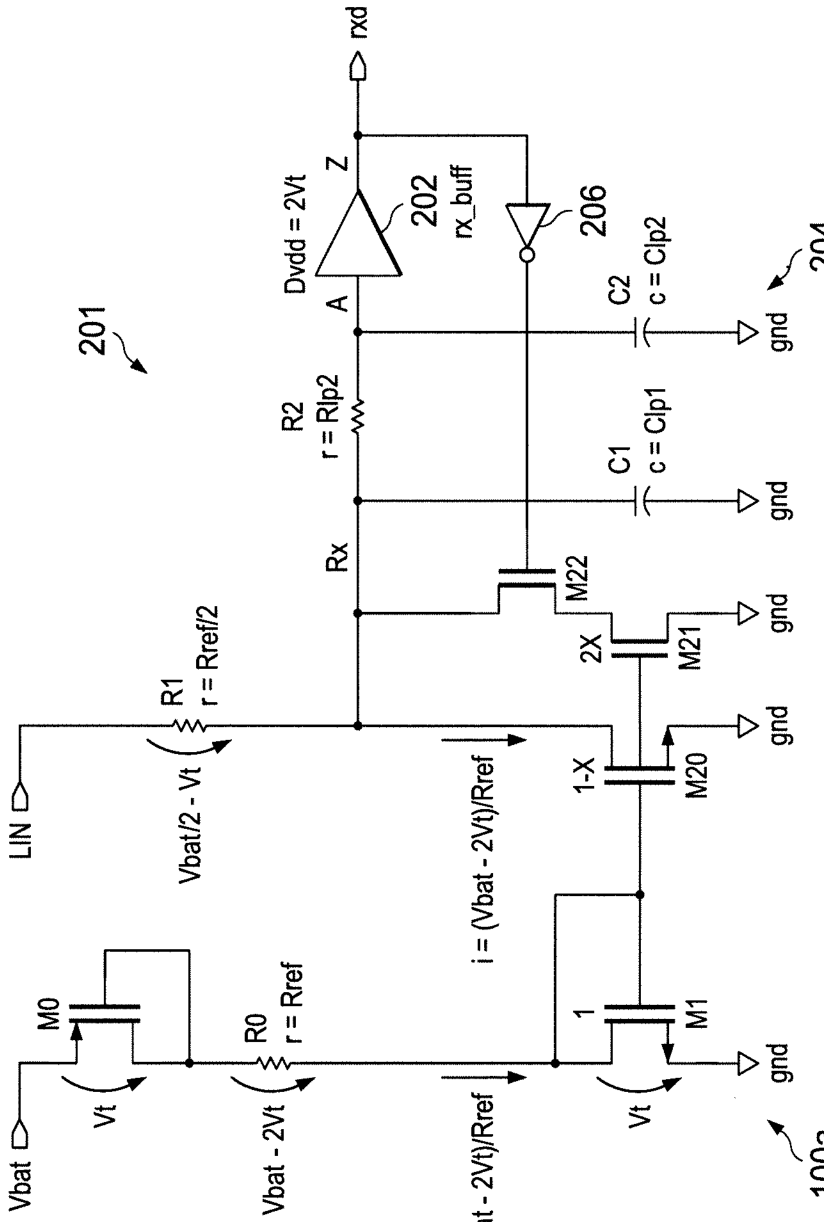

201
rxd
Z
Dvdd = 2Vt
202
rx_buff
206
A
204
C2
c = Clp2
R2
r = Rlp2
C1
c = Clp1
gnd
Rx
M22
2X
M21
R1
r = Rref/2
LIN
Vbat/2 - Vt
i = (Vbat - 2Vt)/Rref
1-X
M20
M0
R0
r = Rref
Vbat
Vt
Vbat - 2Vt
1
M1
100a

FIG. 2B

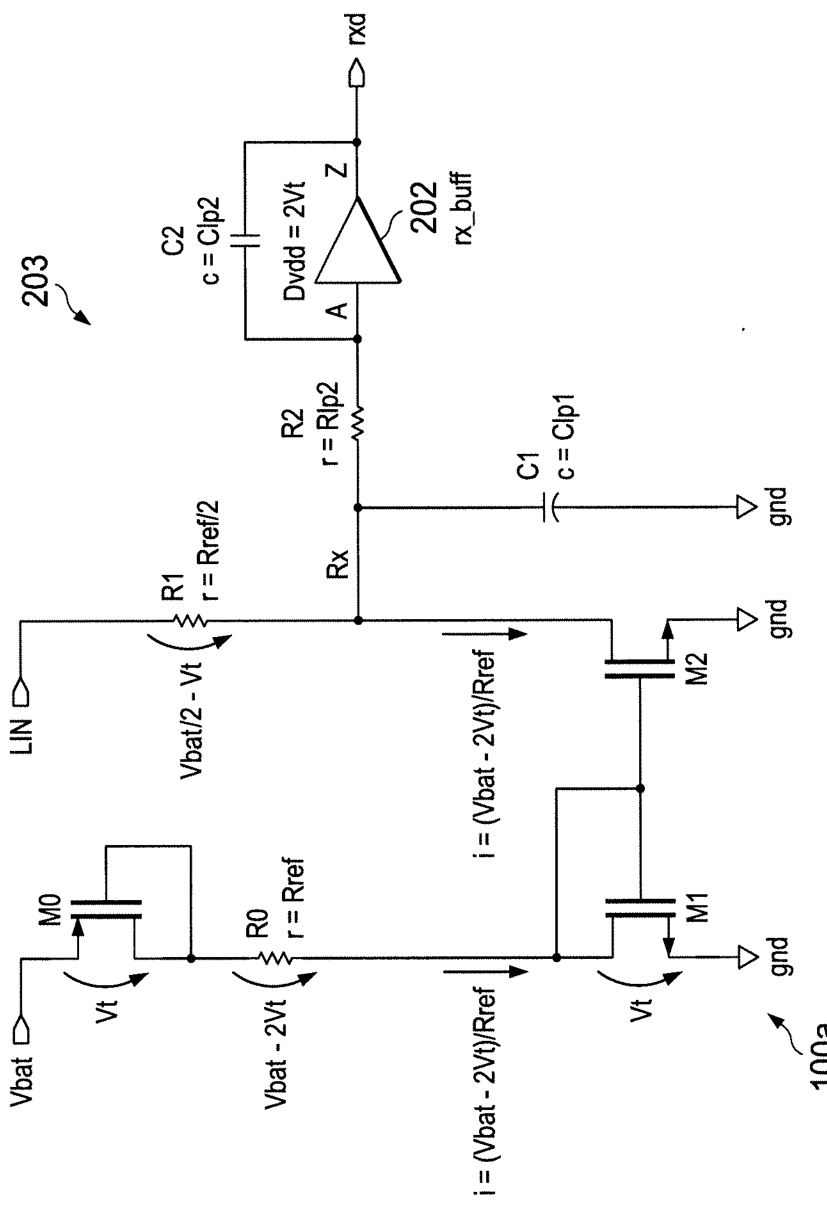

203
rxd
C2
c = Clp2
Dvdd = 2Vt
A
Z
202
rx_buff
R2
r = Rlp2
C1
c = Clp1
gnd
R1
r = Rref/2
Rx
LIN
Vbat/2 - Vt
i = (Vbat - 2Vt)/Rref
M2
gnd
M0
Vbat
Vt
R0
r = Rref
Vbat - 2Vt
i = (Vbat - 2Vt)/Rref
M1
Vt
gnd
100a

FIG. 2C

FIG. 3

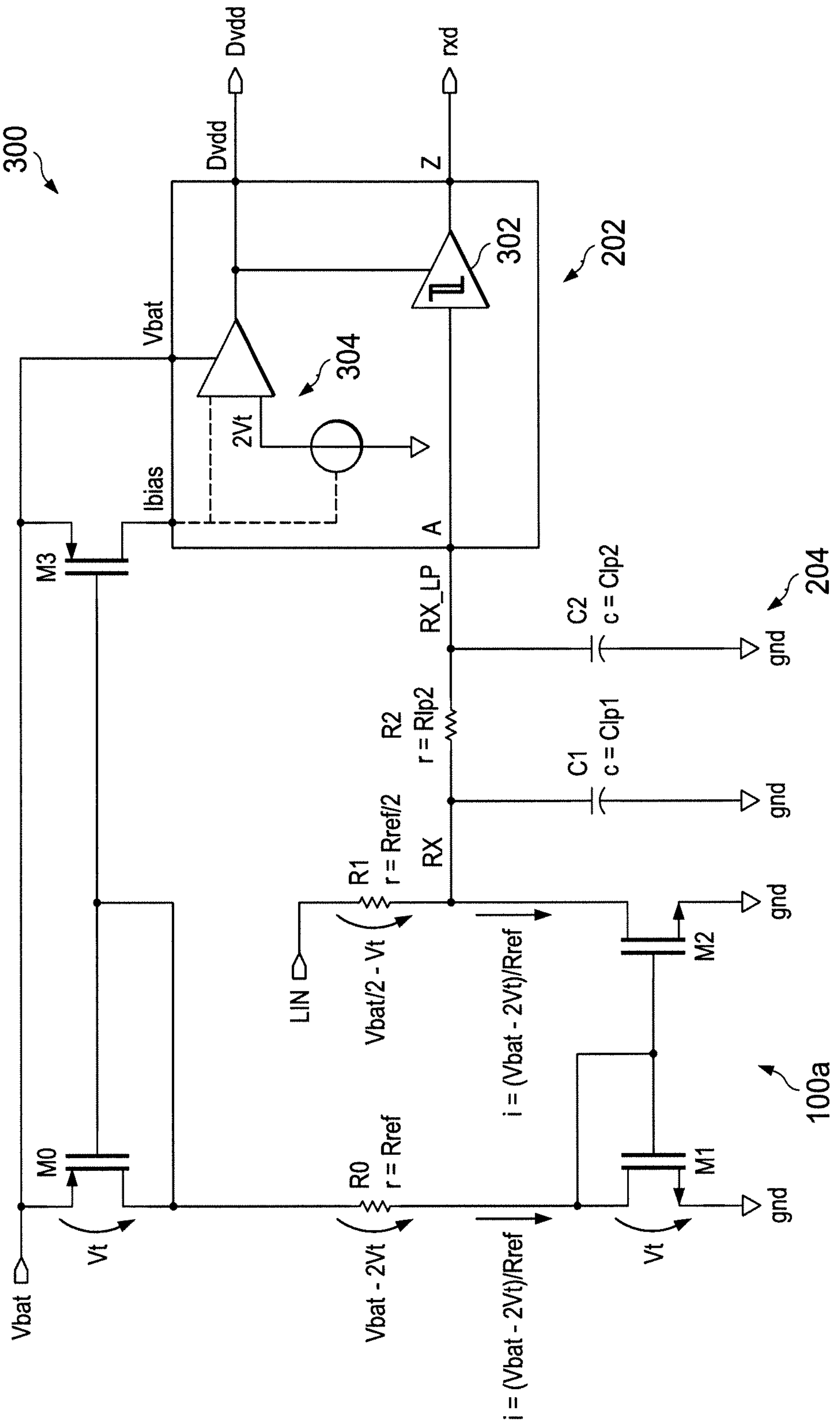
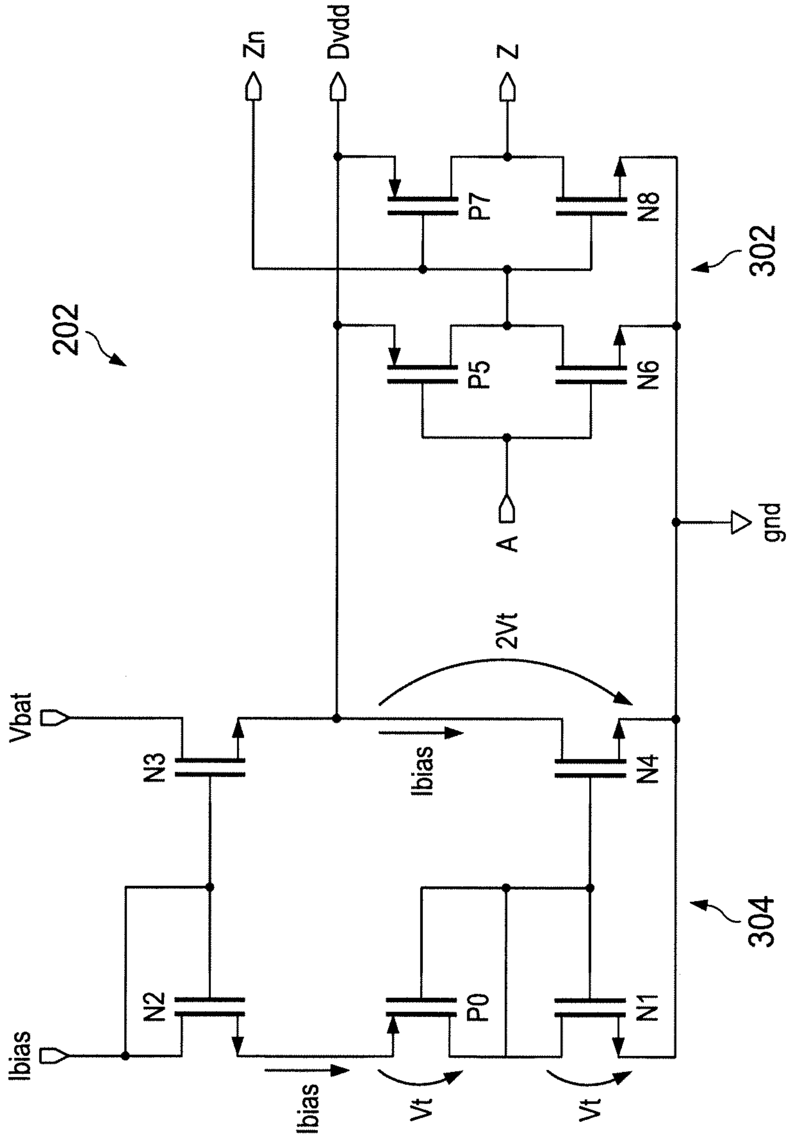

300
Dvdd
rxd
Dvdd
Z
302
202
Vbat
304
2Vt
Ibias
A
M3
RX_LP
C2
c = Clp2
204
gnd
R2
r = Rlp2
C1
c = Clp1
gnd
RX
R1
r = Rref/2
LIN
Vbat/2 - Vt
i = (Vbat - 2Vt)/Rref
gnd
M2
100a
M0
Vbat
Vt
R0
r = Rref
Vbat - 2Vt
i = (Vbat - 2Vt)/Rref
M1
Vt
gnd

FIG. 4


202
Zn
Dvdd
Z
P7
N8
302
P5
N6
A
gnd
Vbat
N3
N4
Ibias
2Vt
N2
P0
N1
304
Ibias
Ibias
Vt
Vt

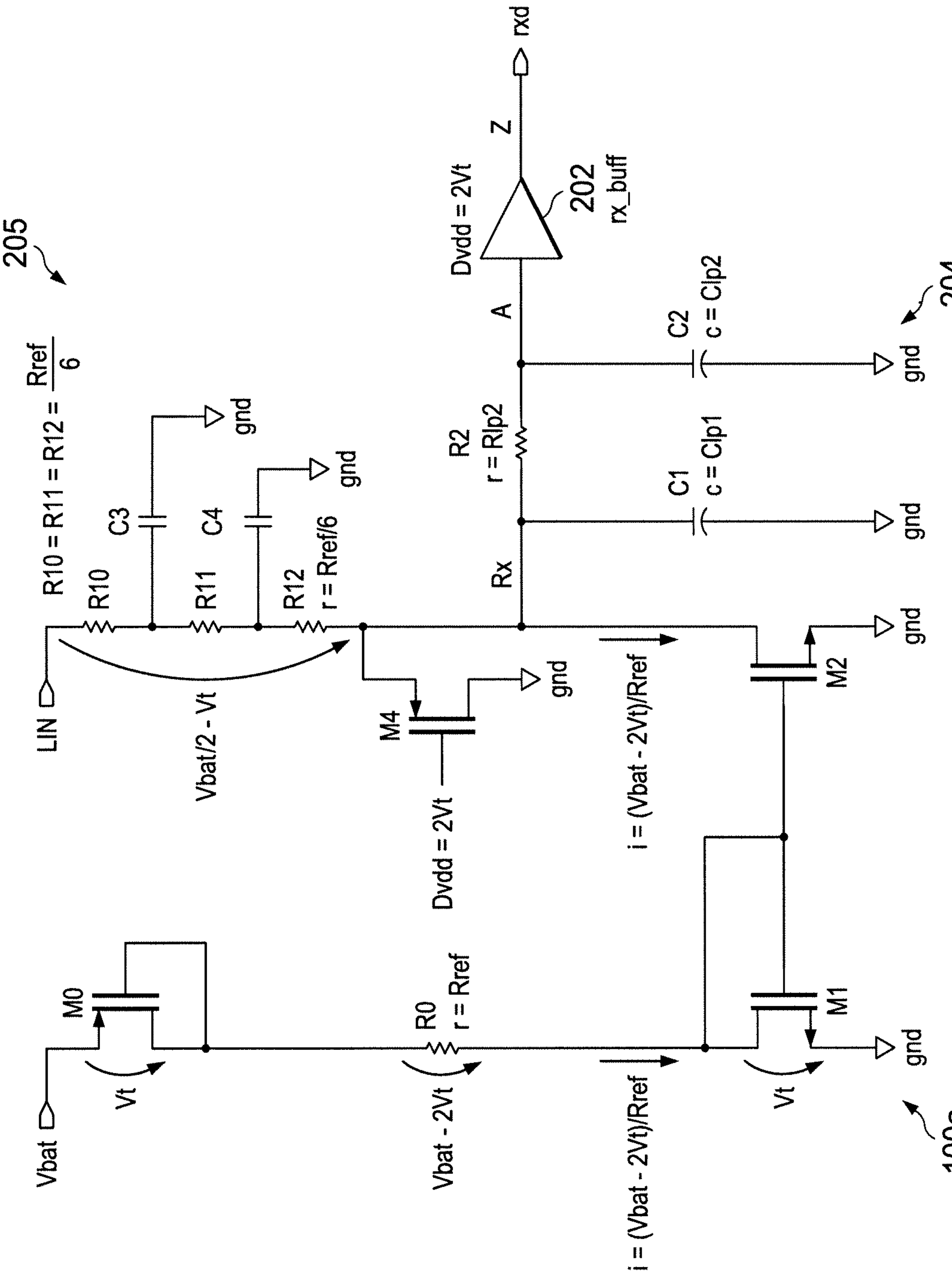
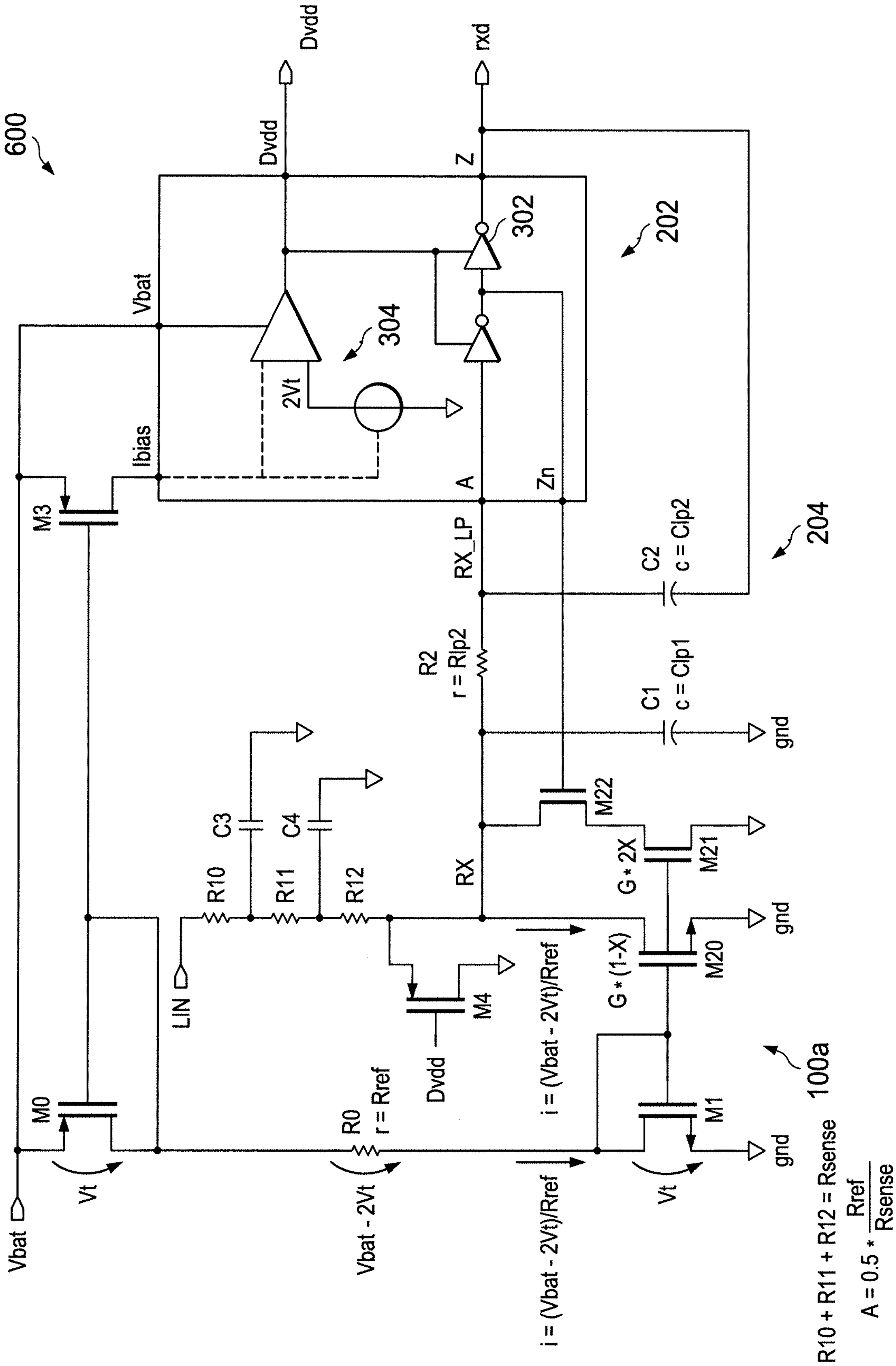

205
R10 = R11 = R12 = Rref/6
LIN
R10
C3
R11
C4
R12
r = Rref/6
gnd
gnd
Vbat/2 - Vt
M4
Dvdd = 2Vt
gnd
Rx
R2
r = Rlp2
A
Dvdd = 2Vt
202
rx_buff
Z
rxd
C1
c = Clp1
C2
c = Clp2
gnd
gnd
204
i = (Vbat - 2Vt)/Rref
M2
gnd
Vbat
M0
Vt
R0
r = Rref
Vbat - 2Vt
i = (Vbat - 2Vt)/Rref
M1
Vt
gnd
100a

FIG. 5

FIG. 6


600
Dvdd
rxd
Z
302
202
Vbat
304
2Vt
Ibias
A
Zn
M3
RX_LP
C2
c = Clp2
204
R2
r = Rlp2
C1
c = Clp1
gnd
C3
C4
M22
G * 2X
M21
RX
R10
R11
R12
LIN
M4
Dvdd
i = (Vbat - 2Vt)/Rref
G * (1-X)
M20
M0
R0
r = Rref
M1
100a
Vbat
Vt
Vbat - 2Vt
i = (Vbat - 2Vt)/Rref
R10 + R11 + R12 = Rsense
A = 0.5 * Rref/Rsense

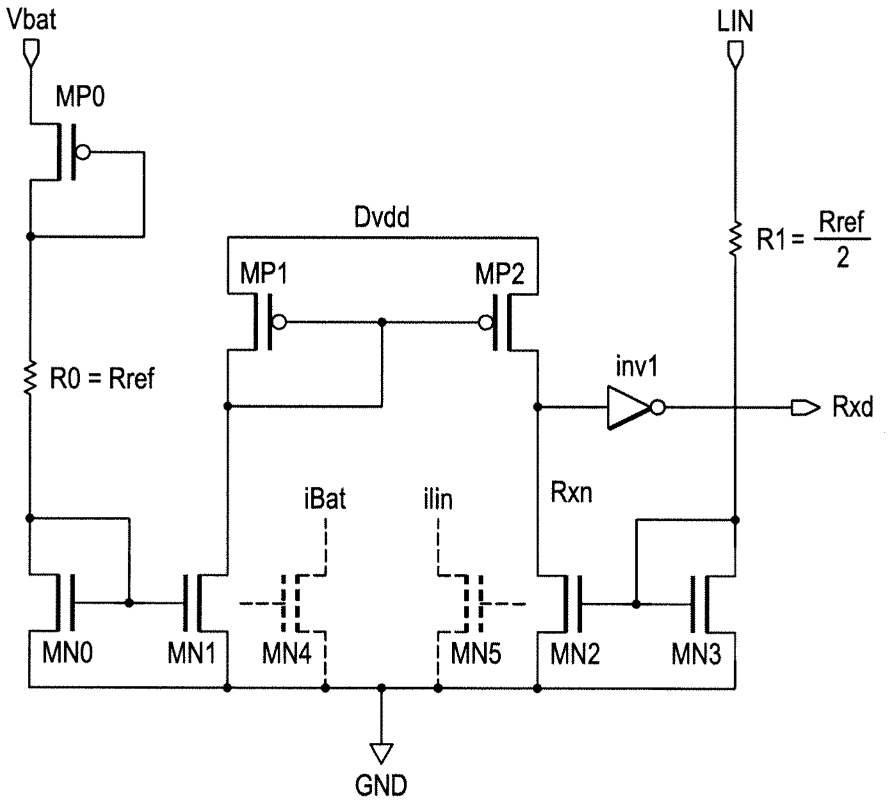

Vbat
MP0
R0 = Rref
Dvdd
MP1
MP2
LIN
R1 = Rref/2
inv1
Rxd
Rxn
iBat
ilin
MN0
MN1
MN4
MN5
MN2
MN3
GND

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/019733

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04L12/40 H04L25/02
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2010/231288 A1 (HORN WOLFGANG [AT]) 16 September 2010 (2010-09-16) paragraph [0002] - paragraph [0009] paragraph [0038] - paragraph [0041]; figure 1	15,31 1-14, 16-30, 32-46
X A	EP 1 404 078 A1 (MOTOROLA INC [US]) 31 March 2004 (2004-03-31) paragraph [0033] - paragraph [0038]; figure 7	15,31 1-14, 16-30, 32-46
Y	US 5 880 614 A (ZINKE OLAF [DE] ET AL) 9 March 1999 (1999-03-09) column 2, line 41 - column 3, line 20; figure 1	1-14, 16-30, 32-46

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 July 2014	04/08/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Tejera, Pedro

2

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/019733

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 510 943 A (FUKUNAGA MASANORI [JP]) 23 April 1996 (1996-04-23) column 16, line 10 - column 17, line 19; figure 9	1-46
A	US 2010/106991 A1 (NOLLER ARMIN [DE]) 29 April 2010 (2010-04-29) paragraph [0036] - paragraph [0058]; figure 1	1-46

2

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2014/019733

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010231288 A1	16-09-2010	DE 102007019356 A1	30-10-2008
		EP 2137914 A1	30-12-2009
		JP 5449135 B2	19-03-2014
		JP 2010525701 A	22-07-2010
		US 2010231288 A1	16-09-2010
		WO 2008128763 A1	30-10-2008
EP 1404078 A1	31-03-2004	AU 2003267415 A1	19-04-2004
		EP 1404078 A1	31-03-2004
		JP 4328295 B2	09-09-2009
		JP 2006500839 A	05-01-2006
		KR 20050071516 A	07-07-2005
		US 2006039504 A1	23-02-2006
		WO 2004030298 A1	08-04-2004
US 5880614 A	09-03-1999	DE 4434180 A1	28-03-1996
		EP 0783798 A1	16-07-1997
		JP 3495374 B2	09-02-2004
		JP H10505907 A	09-06-1998
		US 5880614 A	09-03-1999
		WO 9609691 A1	28-03-1996
US 5510943 A	23-04-1996	DE 4342082 A1	16-06-1994
		JP 2908948 B2	23-06-1999
		JP H06178552 A	24-06-1994
		US 5510943 A	23-04-1996
US 2010106991 A1	29-04-2010	DE 102008053534 B3	14-01-2010
		US 2010106991 A1	29-04-2010