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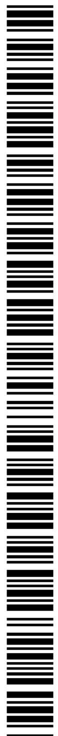
(54) **Title:** MEMORY ARRAYS AND METHODS USED IN FORMING A MEMORY ARRAY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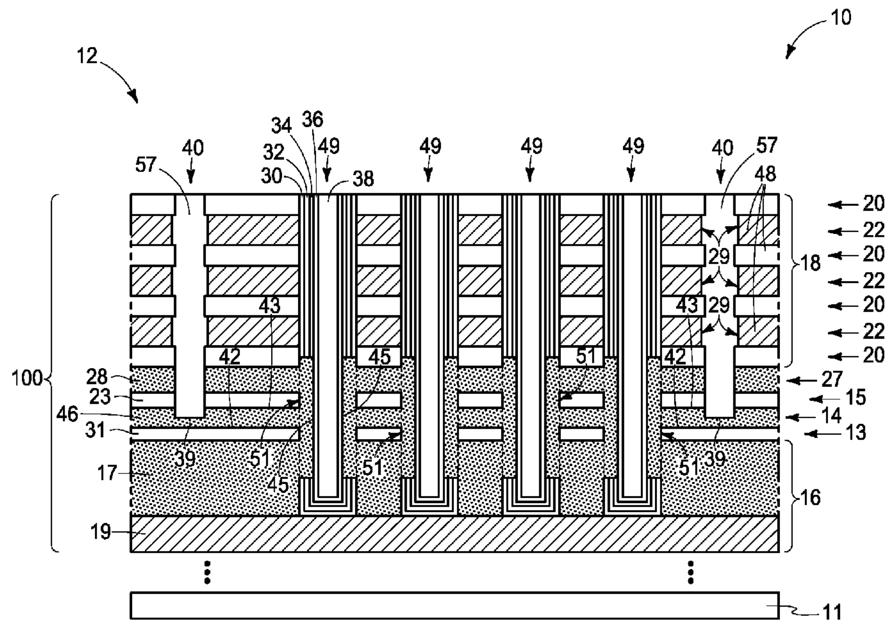

FIG. 21

(57) **Abstract:** A method used in forming a memory array comprises forming a substrate comprising a conductive tier, a first insulator tier above the conductive tier, a sacrificial material tier above the first insulator tier, and a second insulator tier above the sacrificial material tier. A stack comprising vertically-alternating insulative tiers and wordline tiers is formed above the second insulator tier. Channel material is formed through the insulative tiers and the wordline tier. Horizontally -elongated trenches are formed through the stack to the sacrificial material tier. Sacrificial material is etched through the horizontally-elongated trenches selectively relative to material of the first insulator tier and selectively relative to material of the second insulator tier. A laterally-outer sidewall of the channel material is exposed in the sacrificial material tier. A conductive structure is formed directly against the laterally-outer sidewall of the channel material in the sacrificial material tier. The conductive structure extends through the first insulator tier and directly electrically

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couples the channel material to the conductive tier. Structure embodiments are disclosed.

DESCRIPTION

MEMORY ARRAYS AND METHODS USED IN FORMING A MEMORY ARRAY

5 **TECHNICAL FIELD**

Embodiments disclosed herein pertain to memory arrays and to methods used in forming a memory array.

BACKGROUND

10 Memory is one type of integrated circuitry and is used in computer systems for storing data. Memory may be fabricated in one or more arrays of individual memory cells. Memory cells may be written to, or read from, using digit lines (which may also be referred to as bitlines, data lines, or sense lines) and access lines (which may also be referred to as wordlines).
15 The sense lines may conductively interconnect memory cells along columns of the array, and the access lines may conductively interconnect memory cells along rows of the array. Each memory cell may be uniquely addressed through the combination of a sense line and an access line.

Memory cells may be volatile, semi-volatile, or non-volatile.
20 Non-volatile memory cells can store data for extended periods of time in the absence of power. Non-volatile memory is conventionally specified to be memory having a retention time of at least about 10 years. Volatile memory dissipates and is therefore refreshed/rewritten to maintain data storage. Volatile memory may have a retention time of milliseconds or less.
25 Regardless, memory cells are configured to retain or store memory in at least two different selectable states. In a binary system, the states are considered as either a “0” or a “1”. In other systems, at least some individual memory cells may be configured to store more than two levels or states of information.

30 A field effect transistor is one type of electronic component that may be used in a memory cell. These transistors comprise a pair of conductive source/drain regions having a semiconductive channel region there-between. A conductive gate is adjacent the channel region and separated there-from by a thin gate insulator. Application of a suitable voltage to the gate allows
35 current to flow from one of the source/drain regions to the other through the

channel region. When the voltage is removed from the gate, current is largely prevented from flowing through the channel region. Field effect transistors may also include additional structure, for example a reversibly programmable charge-storage region as part of the gate construction
5 between the gate insulator and the conductive gate.

Flash memory is one type of memory and has numerous uses in modern computers and devices. For instance, modern personal computers may have BIOS stored on a flash memory chip. As another example, it is becoming increasingly common for computers and other devices to utilize
10 flash memory in solid state drives to replace conventional hard drives. As yet another example, flash memory is popular in wireless electronic devices because it enables manufacturers to support new communication protocols as they become standardized, and to provide the ability to remotely upgrade the devices for enhanced features.

15 NAND may be a basic architecture of integrated flash memory. A NAND cell unit comprises at least one selecting device coupled in series to a serial combination of memory cells (with the serial combination commonly being referred to as a NAND string). NAND architecture may be configured in a three-dimensional arrangement comprising vertically-stacked memory
20 cells individually comprising a reversibly programmable vertical transistor. Control or other circuitry may be formed below the vertically-stacked memory cells. Other volatile or non-volatile memory array architectures may also comprise vertically-stacked memory cells that individually comprise a transistor.

25

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagrammatic cross-sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

Figs. 2-21 are diagrammatic sequential sectional and/or enlarged
30 views of the construction of Fig. 1 in process in accordance with some embodiments of the invention.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Embodiments of the invention encompass methods used in forming an
35 array of transistors and/or memory cells, for example an array of NAND or

other memory cells having peripheral control circuitry under the array (e.g., CMOS under-array). Embodiments of the invention encompass so-called "gate-last" or "replacement-gate" processing, so-called "gate-first" processing, and other processing whether existing or future-developed independent of when transistor gates are formed. Embodiments of the invention also encompass an array of transistors and/or memory cells (e.g., NAND or other memory cells) independent of method of manufacture. First example method embodiments are described with reference to Figs. 1-21 which may be considered as a "gate-last" or "replacement-gate" process.

Fig. 1 shows a construction 10 in a method of forming an array 12 of elevationally-extending strings of transistors and/or memory cells (not yet shown). Construction 10 comprises a base substrate 11 having any one or more of conductive/conductor/conducting, semiconductive/semiconductor/semiconducting, or insulative/insulator/insulating (i.e., electrically herein) materials. Various materials have been formed elevationally over base substrate 11. Materials may be aside, elevationally inward, or elevationally outward of the Fig. 1-depicted materials. For example, other partially or wholly fabricated components of integrated circuitry may be provided somewhere above, about, or within base substrate 11. Control and/or other peripheral circuitry for operating components within an array (e.g., array 12) of elevationally-extending strings of memory cells may also be fabricated and may or may not be wholly or partially within an array or sub-array. Further, multiple sub-arrays may also be fabricated and operated independently, in tandem, or otherwise relative one another. In this document, a "sub-array" may also be considered as an array.

Substrate/construction 10 comprises a conductive tier 16. Example conductive tier 16 is shown as comprising a conductive material 17 (e.g., conductively-doped semiconductive material such as conductively-doped polysilicon) above a conductive material 19 (e.g., metal material such as WSi_x). Conductive tier 16 may comprise part of control circuitry (e.g., peripheral-under-array circuitry) used to control read and write access to the transistors and/or memory cells that will be formed within array 12.

Construction 10 comprises a first insulator tier 13 above conductive tier 16, a sacrificial material tier 14 above first insulator tier 13, and a

second insulator tier 15 above sacrificial material tier 14. In some embodiments, first insulator tier 13 comprises an insulative metal oxide 31 and second insulator tier 15, when present, comprises insulative metal oxide 23 which may be of the same or different composition as that of insulative metal oxide 31. In the context of this document, "metal" of an "insulative metal oxide" is any elemental metal including any of the elemental semimetals (i.e., B, Si, Ge, As, Sb, Te, Po, and At). Some examples include SiO_2, Al_2O_3, HfO_2, ZrO_2, silicates, aluminates, $Hf_xZr_yO_z$, and $Si_xAl_yO_z$. In one embodiment, the insulative metal oxide comprises multiple elemental metals and in one such embodiment wherein one of the elemental metals is Si. In one embodiment, at least a majority of the insulative metal oxide is stoichiometric, and in another embodiment at least a majority of the insulative metal oxide is non-stoichiometric. Regardless, the insulative metal oxide may contain a conductive metal oxide species (e.g., RuO_2, IrO_2, etc.) but nevertheless be overall insulative when considered as a whole (i.e., it has overall compositional intrinsic electrical conductivity of no greater than 1×10^{-10} siemen/cm at 20°C). Sacrificial material tier 14 comprises sacrificial material 21 that may be etched selectively relative to material 31 of first insulator tier 13 and selectively relative to material 23 of second insulator tier 15. One ideal example is silicon nitride, although any other suitable material may be used including metal material. A conductively-doped semiconductive material tier 27 is above sacrificial material tier 14 and comprises conductively-doped semiconductive material 28 (e.g., conductively-doped polysilicon).

Substrate construction 10 comprises a stack 18 above second insulator tier 15 (and conductively-doped semiconductive material tier 27 when present). Stack 18 comprises vertically-alternating insulative tiers 20 and wordline tiers 22, with conductively-doped semiconductive material tier 27 when present being vertically between second insulator tier 15 and a lowest of insulative tiers 20. Only a small number of tiers 20 and 22 is shown, with more likely stack 18 comprising dozens, a hundred or more, etc. of tiers 20 and 22. Other circuitry that may or may not be part of peripheral and/or control circuitry may be between conductive tier 16 and stack 18. For example, multiple vertically-alternating tiers of conductive material and insulative material of such circuitry may be below a lowest of the wordline

tiers 22 and/or above an uppermost of the wordline tiers 22. Regardless, wordline tiers 22 may not comprise conductive material and insulative tiers 20 may not comprise insulative material or be insulative at this point in processing. Example wordline tiers 22 comprise first material 26 (e.g., silicon nitride) which may be wholly or partially sacrificial. Example insulative tiers 20 comprise second material 24 (e.g., silicon dioxide) that is of different composition from that of first material 26 and which may be wholly or partially sacrificial. Collectively, stack 18 and tiers 16, 13, 14, 15, and 27 may be considered as a stack 100. Only one stack 18 and one stack 100 are shown, although more than one stack 18 and/or one stack 100 may be above or below (not shown) stack 18 and/or stack 100 above or below substrate 11.

Referring to Figs. 2 and 3, channel openings 25 have been formed (e.g., by dry anisotropic etching) into alternating tiers 20 and 22. By way of example only, channel openings 25 are shown as being arranged in groups or columns of staggered rows of four openings 25 per row. Any alternate existing or future-developed arrangement and construction may be used. Example channel openings 25 are shown as going into conductive tier 16 and in one embodiment as shown as going through material 17 and stopping on material 19.

Transistor channel material is formed in the individual channel openings to extend elevationally through the insulative tiers and the wordline tiers, and individual memory cells of the array may be formed to comprise a gate region (e.g., a control-gate region) and a memory structure laterally between the gate region and the channel material. In one such embodiment, the memory structure is formed to comprise a charge-blocking region, storage material (e.g., charge-storage material), and insulative charge-passage material. The storage material (e.g., floating gate material such as doped or undoped silicon or charge-trapping material such as silicon nitride, metal dots, etc.) of the individual memory cells is elevationally along individual of the charge-blocking regions. The insulative charge-passage material (e.g., a bandgap-engineered structure having nitrogen containing material [e.g., silicon nitride] sandwiched between two insulator oxides [e.g., silicon dioxide]) is laterally between the channel material and the storage material.

Fig. 4 shows one embodiment wherein charge-blocking material 30, storage material 32, and charge-passage material 34 have been formed in individual channel openings 25 elevationally along insulative tiers 20 and wordline tiers 22. Transistor materials 30, 32 and 34 (e.g., memory cell materials) may be formed by, for example, deposition of respective thin layers thereof over stack 18 and within individual channel openings 25 followed by planarizing such back at least to an uppermost surface of stack 18. Punch etching may be conducted (not shown) to remove materials 30, 32, and 34 from the bases of channel openings 25 to expose (not shown) conductive tier 16. Channel material 36 has been formed in channel openings 25 elevationally along insulative tiers 20 and wordline tiers 22. Example channel materials 36 include appropriately-doped crystalline semiconductor material, such as one or more silicon, germanium, and so-called III/V semiconductor materials (e.g., GaAs, InP, GaP, and GaN). Example thickness for each of materials 30, 32, 34, and 36 are 25 to 100 Angstroms. Channel openings 25 are shown as comprising a radially-central solid dielectric material 38 (e.g., spin-on-dielectric, silicon dioxide, and/or silicon nitride). Alternately, and by way of example only, the radially-central portion within channel openings 25 may include void space(s) (not shown) and/or be devoid of solid material (not shown). Regardless, and in one embodiment as shown, channel material 36 has been formed into conductive tier 16 and has a bottom 33 that is nowhere directly against any conductive material in conductive tier 16. In one embodiment, channel material 36 is formed through conductively-doped semiconductive material tier 27.

Referring to Figs. 5 and 6, horizontally-elongated trenches 40 have been formed (e.g., by anisotropic etching) through stack 18 to sacrificial material tier 14. In one embodiment, horizontally-elongated 40 trenches have respective bottoms 39 that are above a bottom 41 of first insulator tier 13. In one such embodiment, bottoms 39 of horizontally-elongated trenches 40 are above a top 42 of first insulator tier 13 and, in one such latter embodiment, bottoms 39 of horizontally-elongated trenches 40 are below a top 43 of sacrificial material tier 14.

Referring to Fig. 7, and in one embodiment, a sacrificial sidewall liner 44 (e.g., doped or undoped polysilicon) has been formed in

horizontally-elongated trenches 40. Such may be of the same composition as that of conductively-doped semiconductive material 28 of conductively-doped semiconductive material tier 27. Such a liner 44 may be provided, for example, wherein material 26 is sacrificial and comprises the same composition as that of sacrificial material 21 (e.g., silicon nitride). Such may be subjected to a punch-etch, for example as shown, to remove liner 44 from extending completely across bottoms 39 of trenches 40 to expose sacrificial material 21 of sacrificial material tier 14.

Referring to Fig. 8, sacrificial material 21 (not shown) has been etched (e.g., by wet etching, for example using H_3PO_4 where sacrificial material comprises silicon nitride) through horizontally-elongated trenches 40 selectively relative to material 31 of first insulator tier 13 and selectively relative to material 23 of second insulator tier 15. Such has formed a void space 35. Thickness of sacrificial sidewall liner 44, when present, may be reduced thereby, for example as shown.

A laterally-outer sidewall of the channel in the sacrificial material tier is ultimately exposed. Such is shown, by way of example only, with respect to enlarged Figs. 9-12. Fig. 9 is an enlarged view of a portion of Fig. 8 and Figs. 10-12 show consecutive subsequent processing relative thereto.

Referring to Fig. 10, material 30 in sacrificial material tier 14 has been etched to expose material 32 (e.g., using 100:1 [by volume] dilute HF where a material 30 comprises silicon dioxide). Such may etch material 30 upwardly and downwardly (not shown) relative to sacrificial material tier 14.

Fig. 11 shows etching of material 32 that is in sacrificial material tier 14 to expose material 34, with example upwardly and downwardly etching thereof also having resulted. Where, for example, material 32 comprises silicon nitride, such etching may occur by using H_3PO_4 or 1000:1 (by volume) ultra-dilute HF selectively relative to material 34 where at least a laterally-outermost portion thereof comprises silicon dioxide.

Fig. 12 shows example subsequent etching of exposed material 34 selectively relative to channel material 36, for example using 100:1 dilute HF if material 34 comprises silicon dioxide and/or also using, for example, H_3PO_4 if material 34 also comprises silicon nitride. Such has resulted in exposure of a laterally-outer sidewall 45 of channel material 36 in sacrificial

material tier 14. Materials 30 and/or 34 may be etched upwardly and downwardly as shown.

Referring to Figs. 13 and 14, conductive material 46 has been formed within trenches 40 and within sacrificial material tier 14, resulting in the
5 formation of a conductive structure 51 that is directly against laterally-outer sidewall 45 of channel material 36 in sacrificial material tier 14. Conductive structure 51 extends through first insulator tier 13 and directly electrically couples channel material 36 to conductive tier 16. In one embodiment, conductive material 46 is of the same composition as one or
10 both of materials 28 and 17 (e.g., conductively-doped semiconductive material such as conductively-doped polysilicon). Such may also, in one embodiment, be of the same composition as sacrificial sidewall liner 44 where such is present. Regardless, and in one embodiment as shown, conductive structure 51 comprises an annulus 47 (Fig. 13). Further and
15 regardless, and in one embodiment as shown, conductive structure 51 may be in conductively-doped semiconductive material tier 27 laterally between (a) channel material 36 that is in conductively-doped semiconductive material tier 27 and (b) conductively-doped semiconductive material 28 of conductively-doped semiconductive material tier 27. In one embodiment,
20 conductivity-increasing dopant that is in conductively-doped semiconductive material 28 is diffused laterally (e.g., by a dedicated anneal step or merely by inherent thermal processing in the process) through conductive structure 51 into channel material 36 and upwardly into channel material 36 that is above (and perhaps below) conductively-doped semiconductive
25 material tier 27. In one such embodiment, conductive structure 51 comprises conductively-doped semiconductive material (e.g., 46) comprising the conductivity-increasing dopant before and after such diffusing action.

Referring to Fig. 15, conductive material 46 (not shown) and
30 sacrificial sidewall liner 44 (not shown) when present have been removed through trenches 40 at least to below conductively-doped semiconductive material tier 27 (when present), for example as shown.

Referring to Fig. 16, first material 26 (not shown) of wordline tiers 22 has been etched selectively relative to second material 24 (e.g., using liquid

or vapor H_3PO_4 or 1000:1 [by volume] ultra-dilute HF as a primary etchant where material 26 is silicon nitride and material 24 is silicon dioxide).

Referring to Fig. 17, conductive material 48 has been formed into wordline tiers 22 through trenches 40 and which will comprise conductive
5 material of the individual wordlines to be formed. In but one example embodiment, conductive material 48 comprises a first-deposited conformal titanium nitride liner (not shown) followed by deposition of another composition metal material (e.g., elemental tungsten)

Referring to Figs. 18-20, conductive material 48 has been removed
10 from individual trenches 40. Such has resulted in formation of wordlines 29 and elevationally-extending strings 49 of individual transistors and/or memory cells 56. Approximate locations of transistors and/or memory cells 56 are indicated with a bracket in Fig. 20 and some with dashed outlines in Figs. 18 and 19, with transistors and/or memory cells 56 being essentially
15 ring-like or annular in the depicted example. Conductive material 48 may be considered as having terminal ends 50 (Fig. 20) corresponding to control-gate regions 52 of individual transistors and/or memory cells 56. Control-gate regions 52 in the depicted embodiment comprise individual portions of individual wordlines 29. Materials 30, 32, and 34 may be
20 considered as a memory structure 65 that is laterally between control-gate region 52 and channel material 36.

A charge-blocking region (e.g., charge-blocking material 30) is between storage material 32 and individual control-gate regions 52. A charge block may have the following functions in a memory cell: In a
25 program mode, the charge block may prevent charge carriers from passing out of the storage material (e.g., floating-gate material, charge-trapping material, etc.) toward the control gate, and in an erase mode the charge block may prevent charge carriers from flowing into the storage material from the control gate. Accordingly, a charge block may function to block
30 charge migration between the control-gate region and the storage material of individual memory cells. An example charge-blocking region as shown comprises insulator material 30. By way of further examples, a charge-blocking region may comprise a laterally (e.g., radially) outer portion of the storage material (e.g., material 32) where such storage
35 material is insulative (e.g., in the absence of any different-composition

material between an insulative storage material 32 and conductive material 48). Regardless, as an additional example, an interface of a storage material and conductive material of a control gate may be sufficient to function as a charge-blocking region in the absence of any separate-composition-insulator material 30. Further, an interface of conductive material 48 with material 30 (when present) in combination with insulator material 30 may together function as a charge-blocking region, and as alternately or additionally may a laterally-outer region of an insulative storage material (e.g., a silicon nitride material 32). An example material 30 is one or more of silicon hafnium oxide and silicon dioxide.

Referring to Fig. 21, a material 57 (dielectric and/or silicon-containing such as undoped polysilicon) has been formed in individual trenches 40.

In one embodiment and as described above, wordline tiers 22 comprise sacrificial material 26 and the method comprises replacing sacrificial material 26 of wordline tiers 22 with conductive wordline material 48 after forming conductive structure 51. In one such embodiment, wherein sacrificial sidewall liner 44 is formed in trenches 40, sacrificial sidewall liner 44 is removed after the etching of sacrificial material 21 in sacrificial material tier 14, and in one such embodiment is removed after forming conductive structure 51.

Any other attribute(s) or aspect(s) as shown and/or described herein with respect to other embodiments may be used with respect to the above-described embodiments.

Embodiments of the invention encompass memory arrays independent of method of manufacture. Nevertheless, such memory arrays may have any of the attributes as described herein in method embodiments. Likewise, the above-described method embodiments may incorporate and form any of the attributes described with respect to device embodiments.

In one embodiment, a memory array (e.g., 12) comprises a vertical stack (e.g., 100) comprising a conductive tier (e.g., 16), an insulator tier (e.g., 13) above the conductive tier, and a conductor tier (e.g., 14 in Fig. 21). The vertical stack comprises vertically-alternating insulative tiers (e.g., 20) and wordline tiers (e.g., 22) above the conductor tier. The wordline tiers comprise gate regions (e.g., 52) of individual memory cells (e.g., 56). The

gate lines individually comprise part of a wordline (e.g., 29) in individual of the wordline tiers. Channel material (e.g., 36) extends elevationally through the insulative tiers and the wordline tiers. The individual memory cells comprise a memory structure (e.g., 65) between the gate region and the channel material. The memory structure comprises a charge-blocking region (e.g., 30) laterally inward of the individual gate regions, a storage region (e.g., 32) laterally inward of individual of the charge-blocking regions, and insulative charge-passage material (e.g., 34) laterally inward of individual of the storage regions. A conductive structure 51 extends through the insulator tier and directly electrically couples the channel material to the conductive tier. In one embodiment, the memory array comprises horizontally-elongated insulator structures (e.g., 57) extending elevationally through the insulative tiers and the wordline tiers, with such structures laterally separating individual wordlines in individual of the wordline tiers. The horizontally-elongated insulator structures individually have a bottom (e.g., 39 in Fig. 21) that is above a bottom (e.g., 41) of the insulator tier. In one such embodiment, the bottoms of the horizontally-elongated structures are above a top (e.g., 42) of the insulator tier, and in one such latter embodiment are below a top (e.g., 43 in Fig. 21) of the conductor tier. In one embodiment, another insulator tier (e.g., 15) is above the conductor tier and below a conductively-doped semiconductive material tier (e.g., 27). In one embodiment, the memory array comprises NAND. Any other attribute(s) or aspect(s) as shown and/or described herein with respect to other embodiments may be used.

In one embodiment, a memory array (e.g., 12) comprises a vertical stack (e.g., 100) comprising a conductive tier (e.g., 16), an insulator tier (e.g., 13) above the conductive tier, and a conductor tier (e.g., 14 in Fig. 21). The vertical stack comprises vertically-alternating insulative tiers (e.g., 20) and wordline tiers (e.g., 22) above the conductor tier. The wordline tiers comprise gate regions (e.g., 52) of individual memory cells (e.g., 56). The gate lines individually comprise part of a wordline (e.g., 29) in individual of the wordline tiers. Channel material (e.g., 36) extends elevationally through the insulative tiers and the wordline tiers. The individual memory cells comprise a memory structure (e.g., 65) between the gate region and the channel material. The memory structure comprises a charge-blocking region

(e.g., 30) laterally inward of the individual gate regions, a storage region (e.g., 32) laterally inward of individual of the charge-blocking regions, and insulative charge-passage material (e.g., 34) laterally inward of individual of the storage regions. A conductive structure (e.g., 51) directly electrically
5 couples the channel material to the conductive tier. Horizontally-elongated insulator structures (e.g., 57) extend elevationally through the insulative tiers and the wordline tiers and laterally separate individual of the wordlines and individually have a bottom (e.g., 39) that is above a bottom (e.g., 41) of the insulator tier. Any other attribute(s) or aspect(s) as shown and/or
10 described herein with respect to other embodiments may be used.

An embodiment of the invention comprises a memory array (e.g., 12) comprising a vertical stack (e.g., 100) comprising a conductive tier (e.g., 16), a first insulator tier (e.g., 13) above the conductive tier, a conductor tier (e.g., 14 in Fig. 21) above the insulator tier, a second insulator tier (e.g., 15)
15 above the conductive tier, and a conductively-doped semiconductive material tier (e.g., 27) above the second insulator tier. Vertically-alternating insulative tiers (e.g., 20) and wordline tiers (e.g., 22) are above the conductively-doped semiconductive material tier. The wordline comprise gate regions (e.g., 52) of individual memory cells (e.g., 56). Individual of
20 the gate regions comprising part of a wordline (e.g., 29) in individual of the wordline tiers. Channel material (e.g., 36) extends elevationally through the insulative tiers and the wordline tiers, The individual memory cells comprising a memory structure (e.g., 65) between the individual gate regions and the channel material, The memory structure comprising a
25 charge-blocking region (e.g., 30) laterally inward of the individual gate regions, a storage region (e.g., 32) laterally inward of individual of the charge-blocking regions, and insulative charge-passage material (e.g., 34) laterally inward of individual of the storage regions. A conductive structure (e.g., 51) extends through the conductively-doped semiconductive material
30 tier, the second insulator tier, the conductor tier, and the first insulator tier. The conductive structure directly electrically couples the channel material to the conductive tier and comprises a sidewall (e.g., 45) that is directly against a sidewall of the conductive tier. Any other attribute(s) or aspect(s) as shown and/or described herein with respect to other embodiments may be
35 used.

The above processing(s) or construction(s) may be considered as being relative to an array of components formed as or within a single stack or single deck of such components above or as part of an underlying base substrate (*albeit*, the single stack/deck may have multiple tiers). Control and/or other peripheral circuitry for operating or accessing such components within an array may also be formed anywhere as part of the finished construction, and in some embodiments may be under the array (e.g., CMOS under-array). Regardless, one or more additional such stack(s)/deck(s) may be provided or fabricated above and/or below that shown in the figures or described above. Further, the array(s) of components may be the same or different relative one another in different stacks/decks. Intervening structure may be provided between immediately-vertically-adjacent stacks/decks (e.g., additional circuitry and/or dielectric layers). Also, different stacks/decks may be electrically coupled relative one another. The multiple stacks/decks may be fabricated separately and sequentially (e.g., one atop another), or two or more stacks/decks may be fabricated at essentially the same time.

The assemblies and structures discussed above may be used in integrated circuits/circuitry and may be incorporated into electronic systems. Such electronic systems may be used in, for example, memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. The electronic systems may be any of a broad range of systems, such as, for example, cameras, wireless devices, displays, chip sets, set top boxes, games, lighting, vehicles, clocks, televisions, cell phones, personal computers, automobiles, industrial control systems, aircraft, etc.

In this document unless otherwise indicated, "elevational", "higher", "upper", "lower", "top", "atop", "bottom", "above", "below", "under", "beneath", "up", and "down" are generally with reference to the vertical direction. "Horizontal" refers to a general direction (i.e., within 10 degrees) along a primary substrate surface and may be relative to which the substrate is processed during fabrication, and vertical is a direction generally orthogonal thereto. Reference to "exactly horizontal" is the direction along the primary substrate surface (i.e., no degrees there-from) and may be relative to which the substrate is processed during fabrication. Further,

"vertical" and "horizontal" as used herein are generally perpendicular directions relative one another and independent of orientation of the substrate in three-dimensional space. Additionally, "elevationally-extending" and "extend(ing) elevationally" refer to a direction that is angled away by at least 45° from exactly horizontal. Further, "extend(ing) elevationally", "elevationally-extending", "extend(ing) horizontally", "horizontally-extending" and the like with respect to a field effect transistor are with reference to orientation of the transistor's channel length along which current flows in operation between the source/drain regions. For bipolar junction transistors, "extend(ing) elevationally" "elevationally-extending", "extend(ing) horizontally", "horizontally-extending" and the like, are with reference to orientation of the base length along which current flows in operation between the emitter and collector. In some embodiments, any component, feature, and/or region that extends elevationally extends vertically or within 10° of vertical.

Further, "directly above", "directly below", and "directly under" require at least some lateral overlap (i.e., horizontally) of two stated regions/materials/components relative one another. Also, use of "above" not preceded by "directly" only requires that some portion of the stated region/material/component that is above the other be elevationally outward of the other (i.e., independent of whether there is any lateral overlap of the two stated regions/materials/components). Analogously, use of "below" and "under" not preceded by "directly" only requires that some portion of the stated region/material/component that is below/under the other be elevationally inward of the other (i.e., independent of whether there is any lateral overlap of the two stated regions/materials/components).

Any of the materials, regions, and structures described herein may be homogenous or non-homogenous, and regardless may be continuous or discontinuous over any material which such overlie. Where one or more example composition(s) is/are provided for any material, that material may comprise, consist essentially of, or consist of such one or more composition(s). Further, unless otherwise stated, each material may be formed using any suitable existing or future-developed technique, with atomic layer deposition, chemical vapor deposition, physical vapor

deposition, epitaxial growth, diffusion doping, and ion implanting being examples.

Additionally, “thickness” by itself (no preceding directional adjective) is defined as the mean straight-line distance through a given material or region perpendicularly from a closest surface of an immediately-adjacent material of different composition or of an immediately-adjacent region. Additionally, the various materials or regions described herein may be of substantially constant thickness or of variable thicknesses. If of variable thickness, thickness refers to average thickness unless otherwise indicated, and such material or region will have some minimum thickness and some maximum thickness due to the thickness being variable. As used herein, “different composition” only requires those portions of two stated materials or regions that may be directly against one another to be chemically and/or physically different, for example if such materials or regions are not homogenous. If the two stated materials or regions are not directly against one another, “different composition” only requires that those portions of the two stated materials or regions that are closest to one another be chemically and/or physically different if such materials or regions are not homogenous. In this document, a material, region, or structure is “directly against” another when there is at least some physical touching contact of the stated materials, regions, or structures relative one another. In contrast, “over”, “on”, “adjacent”, “along”, and “against” not preceded by “directly” encompass “directly against” as well as construction where intervening material(s), region(s), or structure(s) result(s) in no physical touching contact of the stated materials, regions, or structures relative one another.

Herein, regions-materials-components are “electrically coupled” relative one another if in normal operation electric current is capable of continuously flowing from one to the other and does so predominately by movement of subatomic positive and/or negative charges when such are sufficiently generated. Another electronic component may be between and electrically coupled to the regions-materials-components. In contrast, when regions-materials-components are referred to as being "directly electrically coupled”, no intervening electronic component (e.g., no diode, transistor, resistor, transducer, switch, fuse, etc.) is between the directly electrically coupled regions-materials-components.

The composition of any of the conductive/conductor/conducting materials herein may be metal material and/or conductively-doped semiconductive/semiconductor/semiconducting material. “Metal material” is any one or combination of an elemental metal, any mixture or alloy of two or more elemental metals, and any one or more conductive metal compound(s).

Herein, “selective” as to etch, etching, removing, removal, depositing, forming, and/or formation is such an act of one stated material relative to another stated material(s) so acted upon at a rate of at least 2:1 by volume. Further, selectively depositing, selectively growing, or selectively forming is depositing, growing, or forming one material relative to another stated material or materials at a rate of at least 2:1 by volume for at least the first 75 Angstroms of depositing, growing, or forming.

Unless otherwise indicated, use of “or” herein encompasses either and both.

CONCLUSION

In some embodiments, a method used in forming a memory array comprises forming a substrate comprising a conductive tier, a first insulator tier above the conductive tier, a sacrificial material tier above the first insulator tier, and a second insulator tier above the sacrificial material tier. A stack comprising vertically-alternating insulative tiers and wordline tiers is formed above the second insulator tier. Channel material is formed through the insulative tiers and the wordline tier. Horizontally-elongated trenches are formed through the stack to the sacrificial material tier. Sacrificial material is etched through the horizontally-elongated trenches selectively relative to material of the first insulator tier and selectively relative to material of the second insulator tier. A laterally-outer sidewall of the channel material is exposed in the sacrificial material tier. A conductive structure is formed directly against the laterally-outer sidewall of the channel material in the sacrificial material tier. The conductive structure extends through the first insulator tier and directly electrically couples the channel material to the conductive tier.

In some embodiments, a method used in forming a memory array comprises forming a substrate comprising a conductive tier, a first insulator

tier comprising an insulative metal oxide above the conductive tier, a silicon nitride tier above the first insulator tier, and a second insulator tier comprising the insulative metal oxide above the silicon nitride tier. A stack comprising vertically-alternating insulative tiers and wordline tiers is
5 formed above the second insulator metal oxide tier. Channel material is formed through the insulative tiers and the wordline tiers and into the conductive tier. Horizontally-elongated trenches are formed through the stack to the silicon nitride tier. The silicon nitride tier is wet etched through the horizontally-elongated trenches selectively relative to the insulative
10 metal oxide of the first insulator tier and the insulative metal oxide of the second insulator tier. A laterally-outer sidewall of the channel material is exposed in the sacrificial material tier. A conductive structure is formed directly against the laterally-outer sidewall of the channel material in the sacrificial material tier. The conductive structure extends through the first
15 insulator tier and directly electrically couples the channel material to the conductive tier.

In some embodiments, a memory array comprises a vertical stack comprising a conductive tier, an insulator tier above the conductive tier, a conductor tier above the insulator tier, and vertically-alternating insulative
20 tiers and wordline tiers above the conductor tier. The wordline tiers comprise gate regions of individual memory cells. Individual of the gate regions comprise part of a wordline in individual of the wordline tiers. Channel material extends elevationally through the insulative tiers and the wordline tiers. The individual memory cells comprise a memory structure
25 between the individual gate regions and the channel material. The memory structure comprises a charge-blocking region laterally inward of the individual gate regions, a storage region laterally inward of individual of the charge-blocking regions, and insulative charge-passage material laterally inward of individual of the storage regions. A conductive structure extends
30 through the insulator tier and directly electrically couples the channel material to the conductive tier.

In some embodiments, a memory array comprises a vertical stack comprising a conductive tier, an insulator tier above the conductive tier, a conductor tier above the insulator tier, and vertically-alternating insulative
35 tiers and wordline tiers above the conductor tier. The wordline tiers

comprise gate regions of individual memory cells. Individual of the gate regions comprise part of a wordline in individual of the wordline tiers. Channel material extends elevationally through the insulative tiers and the wordline tiers. The individual memory cells comprise a memory structure
5 between the individual gate regions and the channel material. The memory structure comprises a charge-blocking region laterally inward the individual gate regions, a storage region laterally inward of individual of the charge-blocking regions, and insulative charge-passage material laterally inward of individual of the storage regions. A conductive structure directly
10 electrically couples the channel material to the conductive tier. Horizontally-elongated insulator structures extend elevationally through the insulative tiers and the wordline tiers. The horizontally-elongated insulator structures laterally separate individual of the wordlines and individually have a bottom that is above a bottom of the insulator tier.

15 In some embodiments, a memory array comprises a vertical stack comprising a conductive tier, a first insulator tier above the conductive tier, a conductor tier above the insulator tier, a second insulator tier above the conductive tier, a conductively-doped semiconductive material tier above the second insulator tier, and vertically-alternating insulative tiers and
20 wordline tiers above the conductively-doped semiconductive material tier. The wordline tiers comprise gate regions of individual memory cells. Individual of the gate regions comprise part of a wordline in individual of the wordline tiers. Channel material extends elevationally through the insulative tiers and the wordline tiers. The individual memory cells
25 comprise a memory structure between the individual gate regions and the channel material. The memory structure comprises a charge-blocking region laterally inward of the individual gate regions, a storage region laterally inward of individual of the charge-blocking regions, and insulative charge-passage material laterally inward of individual of the storage regions.
30 A conductive structure extends through the conductively-doped semiconductive material tier, the second insulator tier, the conductor tier, and the first insulator tier. The conductive structure directly electrically couples the channel material to the conductive tier and comprises a sidewall that is directly against a sidewall of the conductive tier.

CLAIMS:

1. A method used in forming a memory array, comprising:

forming a substrate comprising a conductive tier, a first insulator tier above the conductive tier, a sacrificial material tier above the first insulator tier, a second insulator tier above the sacrificial material tier, and a stack comprising vertically-alternating insulative tiers and wordline tiers above the second insulator tier;

forming channel material through the insulative tiers and the wordline tiers;

forming horizontally-elongated trenches through the stack to the sacrificial material tier;

etching the sacrificial material through the horizontally-elongated trenches selectively relative to material of the first insulator tier and selectively relative to material of the second insulator tier, and exposing a laterally-outer sidewall of the channel material in the sacrificial material tier; and

forming a conductive structure directly against the laterally-outer sidewall of the channel material in the sacrificial material tier, the conductive structure extending through the first insulator tier and directly electrically coupling the channel material to the conductive tier.

2. The method of claim 1 wherein the material of the first insulator tier and the material of the second insulator tier are of the same composition relative one another.

3. The method of claim 1 wherein the wordline tiers comprise the sacrificial material, and further comprising replacing the sacrificial material of the wordline tiers with conductive wordline material after forming the conductive structure.

4. The method of claim 3 comprising forming a sacrificial sidewall liner in the horizontally-elongated trenches before the etching and removing the sacrificial sidewall liner after the etching.

5. The method of claim 4 wherein the sacrificial sidewall liner is removed after forming the conductive structure.

6. The method of claim 1 comprising forming the channel material into the conductive tier, the channel material having a bottom that is nowhere directly against any conductive material in the conductive tier.

7. The method of claim 1 comprising forming a conductively-
5 doped semiconductive material tier that is vertically between the second insulator tier and a lowest of the insulative tiers, the channel material being formed through the conductively-doped semiconductive material tier, the conductive structure being in the conductively-doped semiconductive material tier laterally between (a) the channel material that is in the
10 conductively-doped semiconductive material tier, and (b) conductively-doped semiconductive material of the conductively-doped semiconductive material tier.

8. The method of claim 7 comprising diffusing conductivity-increasing dopant that is in the conductively-doped
15 semiconductive material laterally through the conductive structure into the channel material and upwardly into the channel material that is above the conductively-doped semiconductive material tier.

9. The method of claim 8 wherein the conductive structure comprises conductively-doped semiconductor material comprising the
20 conductivity-increasing dopant before and after said diffusing.

10. The method of claim 7 comprising forming a sacrificial sidewall liner in the horizontally-elongated trenches before the etching and removing the sacrificial sidewall liner after the etching, the sacrificial line being of the same composition as that of the conductively-doped
25 semiconductive material of the conductively-doped semiconductive material tier.

11. The method of claim 1 wherein the horizontally-elongated trenches have respective bottoms that are above a bottom of the first insulator tier.

30 12. The method of claim 11 wherein the bottoms of the horizontally-elongated trenches are above a top of the first insulator tier.

13. The method of claim 12 wherein the bottoms of the horizontally-elongated trenches are below a top of the sacrificial material tier.

14. The method of claim 1 wherein the conductive structure
5 comprises an annulus.

15. The method of claim 1 comprising forming CMOS under array circuitry.

16. A method used in forming a memory array, comprising:

forming a substrate comprising a conductive tier, a first insulator tier
10 comprising an insulative metal oxide above the conductive tier, a silicon nitride tier above the first insulator tier, a second insulator tier comprising the insulative metal oxide above the silicon nitride tier, and a stack comprising vertically-alternating insulative tiers and wordline tiers above the second insulator metal oxide tier;

15 forming channel material through the insulative tiers and the wordline tiers and into the conductive tier;

forming horizontally-elongated trenches through the stack to the silicon nitride tier;

wet etching the silicon nitride tier through the horizontally-elongated
20 trenches selectively relative to the insulative metal oxide of the first insulator tier and the insulative metal oxide of the second insulator tier, and exposing a laterally-outer sidewall of the channel material in the sacrificial material tier; and

forming a conductive structure directly against the laterally-outer
25 sidewall of the channel material in the sacrificial material tier, the conductive structure extending through the first insulator tier and directly electrically coupling the channel material to the conductive tier.

17. The method of claim 16 wherein the insulative metal oxide comprises SiO_2.

30 18. The method of claim 16 wherein the insulative metal oxide comprises multiple elemental metals.

19. The method of claim 18 wherein one of the elemental metals is Si.

20. The method of claim 16 wherein a least a majority of the insulative metal oxide is stoichiometric.

5 21. The method of claim 16 wherein a least a majority of the insulative metal oxide is non-stoichiometric.

22. The method of claim 16 comprising forming a conductively-doped semiconductive material tier that is vertically between the second insulator tier and a lowest of the insulative tiers, the channel material being
10 formed through the conductively-doped semiconductive material tier, the conductive structure being in the conductively-doped semiconductive material tier laterally between (a) the channel material that is in the conductively-doped semiconductive material tier, and (b) conductively-doped semiconductive material of the conductively-doped semiconductive
15 material tier.

23. A memory array comprising:

a vertical stack comprising:

a conductive tier;

an insulator tier above the conductive tier;

20 a conductor tier above the insulator tier; and

vertically-alternating insulative tiers and wordline tiers above the conductor tier, the wordline tiers comprising gate regions of individual memory cells, individual of the gate regions comprising part of a wordline in individual of the
25 wordline tiers;

channel material extending elevationally through the insulative tiers and the wordline tiers;

the individual memory cells comprising a memory structure between the individual gate regions and the channel material; the memory structure
30 comprising a charge-blocking region laterally inward of the individual gate regions, a storage region laterally inward of individual of the charge-blocking regions, and insulative charge-passage material laterally inward of individual of the storage regions; and

a conductive structure that extends through the insulator tier and directly electrically couples the channel material to the conductive tier.

24. The memory array of claim 23 comprising horizontally-elongated insulator structures extending elevationally through the insulative tiers and the wordline tiers, the horizontally-elongated insulator structures laterally separating individual wordlines in individual of the wordline tiers.

25. The memory array of claim 24 wherein the horizontally-elongated insulator structures individually have a bottom that is above a bottom of the insulator tier.

26. The memory array of claim 25 wherein the bottoms of the horizontally-elongated structures are above a top of the insulator tier.

27. The memory array of claim 26 wherein the bottoms of the horizontally-elongated structures are below a top of the conductor tier.

28. The memory array of claim 23 wherein the channel material is in the conductive tier, the channel material having a bottom that is nowhere directly against any conductive material in the conductive tier.

29. The memory array of claim 23 comprising a conductively-doped semiconductive material tier that is vertically between the insulator tier and a lowest of the insulative tiers, the channel material extending through the conductively-doped semiconductive material tier, the conductive structure being in the conductively-doped semiconductive material tier laterally between (a) the channel material that is in the conductively-doped semiconductive material tier in the conductively-doped semiconductive material tier, and (b) conductively-doped semiconductive material of the conductively-doped semiconductive material tier.

30. The memory array of claim 29 wherein the conductive structure and the conductively-doped semiconductive material are of the same composition.

31. The memory array of claim 29 comprising another insulator tier above the conductor tier and below the conductively-doped semiconductive material tier.

32. The memory array of claim 23 comprising NAND.

33. The memory array of claim 23 comprising CMOS under array circuitry.

34. A memory array comprising:

5 a vertical stack comprising:

a conductive tier;

an insulator tier above the conductive tier;

a conductor tier above the insulator tier; and

vertically-alternating insulative tiers and wordline tiers

10 above the conductor tier, the wordline tiers comprising gate regions of individual memory cells, individual of the gate regions comprising part of a wordline in individual of the wordline tiers;

channel material extending elevationally through the insulative tiers

15 and the wordline tiers;

the individual memory cells comprising a memory structure between the individual gate regions and the channel material; the memory structure comprising a charge-blocking region laterally inward the individual gate regions, a storage region laterally inward of individual of the charge-

20 blocking regions, and insulative charge-passage material laterally inward of individual of the storage regions;

a conductive structure directly electrically coupling the channel material to the conductive tier; and

horizontally-elongated insulator structures extending elevationally

25 through the insulative tiers and the wordline tiers, the horizontally-elongated insulator structures laterally separating individual of the wordlines and individually having a bottom that is above a bottom of the insulator tier.

35. The memory array of claim 34 wherein the bottoms of the horizontally-elongated structures are above a top of the insulator tier.

30 36. The memory array of claim 35 wherein the bottoms of the horizontally-elongated structures are below a top of the conductor tier.

37. A memory array comprising:

a vertical stack comprising:

a conductive tier;

a first insulator tier above the conductive tier;

5 a conductor tier above the insulator tier;

a second insulator tier above the conductive tier;

a conductively-doped semiconductive material tier above the second insulator tier; and

vertically-alternating insulative tiers and wordline tiers

10 above the conductively-doped semiconductive material tier, the wordline tiers comprising gate regions of individual memory cells, individual of the gate regions comprising part of a wordline in individual of the wordline tiers;

channel material extending elevationally through the insulative tiers

15 and the wordline tiers;

the individual memory cells comprising a memory structure between the individual gate regions and the channel material; the memory structure comprising a charge-blocking region laterally inward of the individual gate regions, a storage region laterally inward of individual of the charge-

20 blocking regions, and insulative charge-passage material laterally inward of individual of the storage regions; and

a conductive structure that extends through the conductively-doped semiconductive material tier, the second insulator tier, the conductor tier, and the first insulator tier; the conductive structure directly electrically

25 coupling the channel material to the conductive tier and comprising a sidewall that is directly against a sidewall of the conductive tier.

38. The memory array of claim 37 wherein material of the first insulator tier and material of the second insulator tier are of the same composition relative one another.

30 39. The memory array of claim 37 wherein the first insulator tier comprises an insulative metal oxide and the second insulator tier comprises an insulative metal oxide.

40. The memory array of claim 39 wherein the insulative metal oxide of the first insulator tier and the insulative metal oxide of the second insulator tier are of the same composition relative one another.

41. The memory array of claim 40 wherein the insulative metal
5 oxide comprises SiO_2.

42. The memory array of claim 40 wherein the insulative metal oxide comprises multiple elemental metals.

43. The memory array of claim 42 wherein one of the elemental metals is Si.

10 44. The memory array of claim 40 wherein a least a majority of the insulative metal oxide is stoichiometric.

45. The memory array of claim 40 wherein a least a majority of the insulative metal oxide is non-stoichiometric.

FIG. 1

FIG. 2

FIG. 3

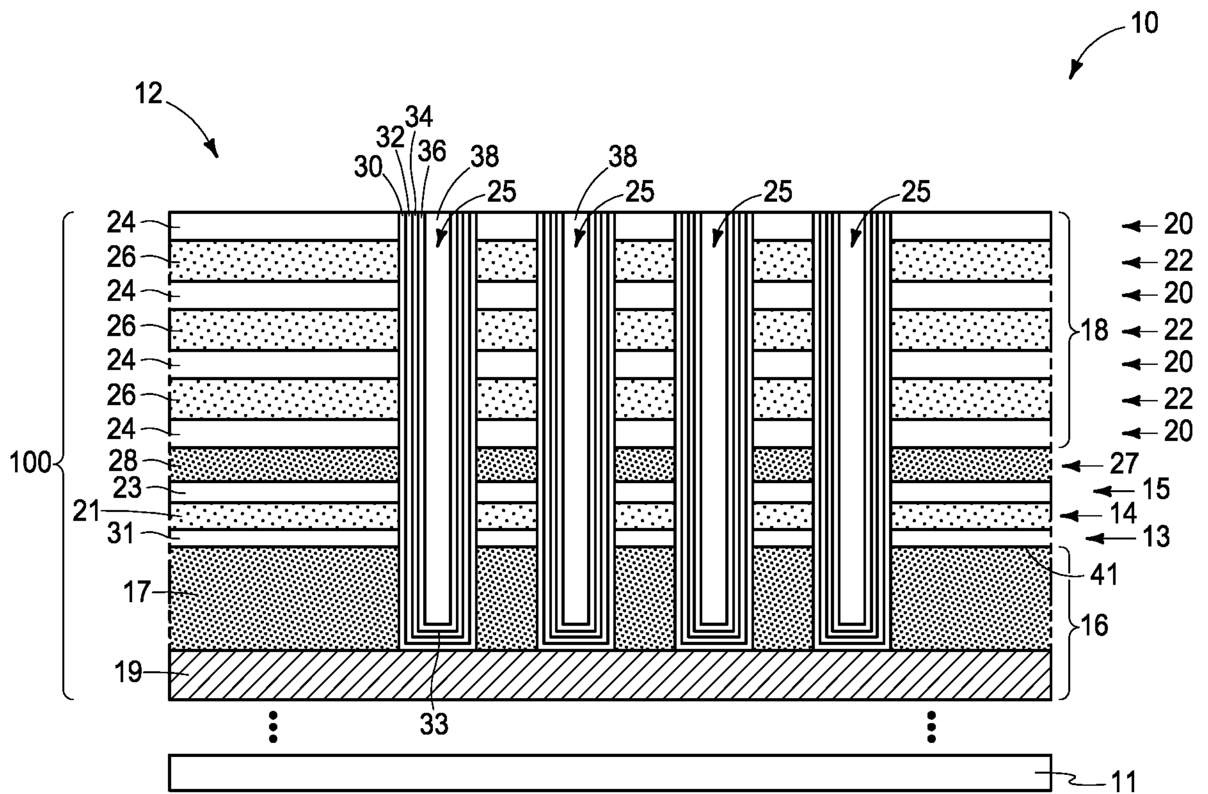

FIG. 4

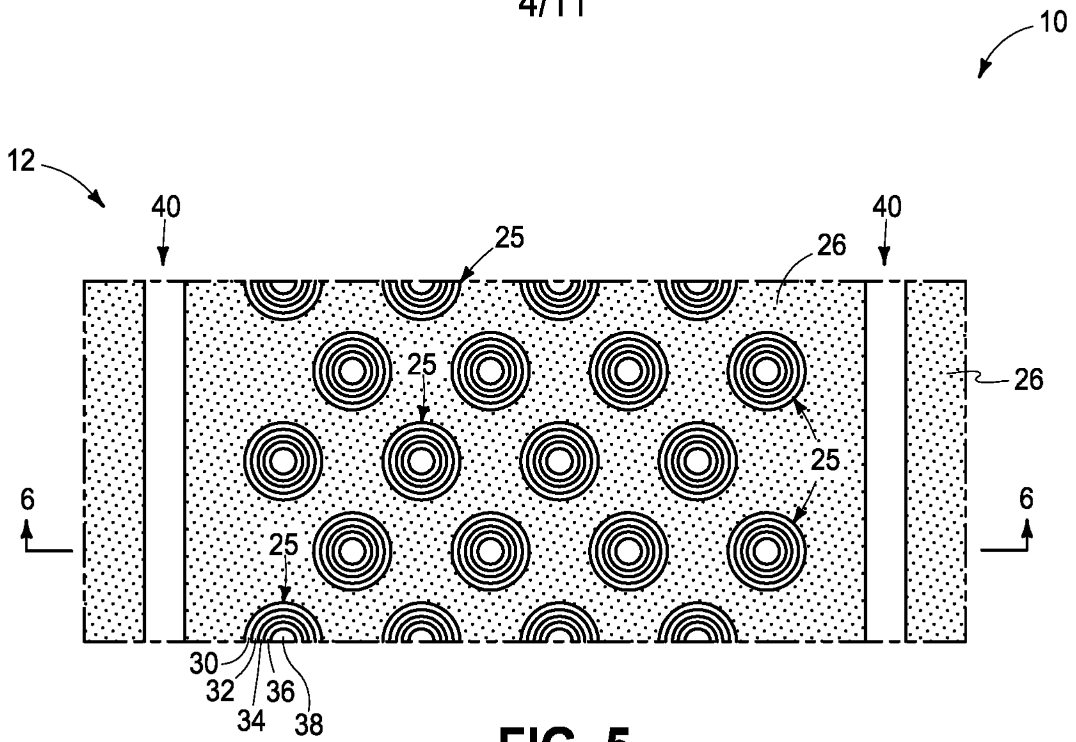

FIG. 5

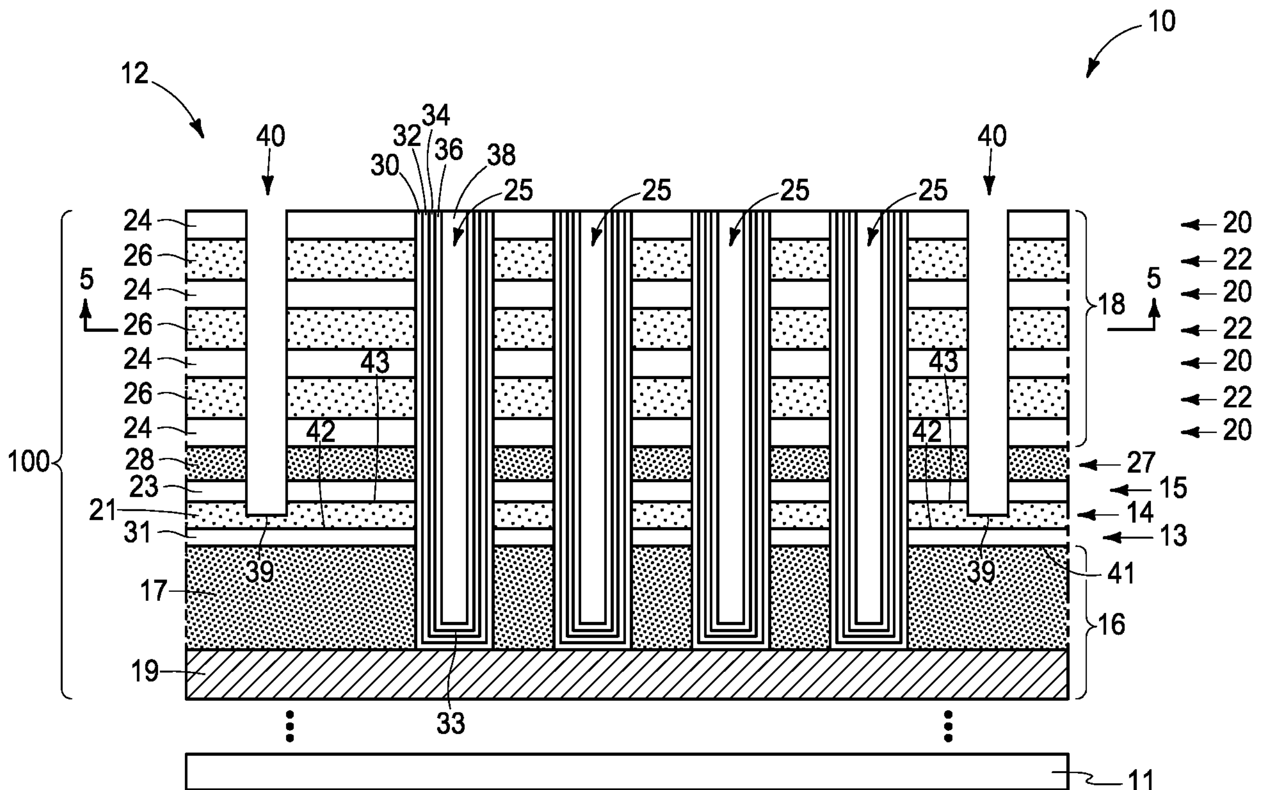

FIG. 6

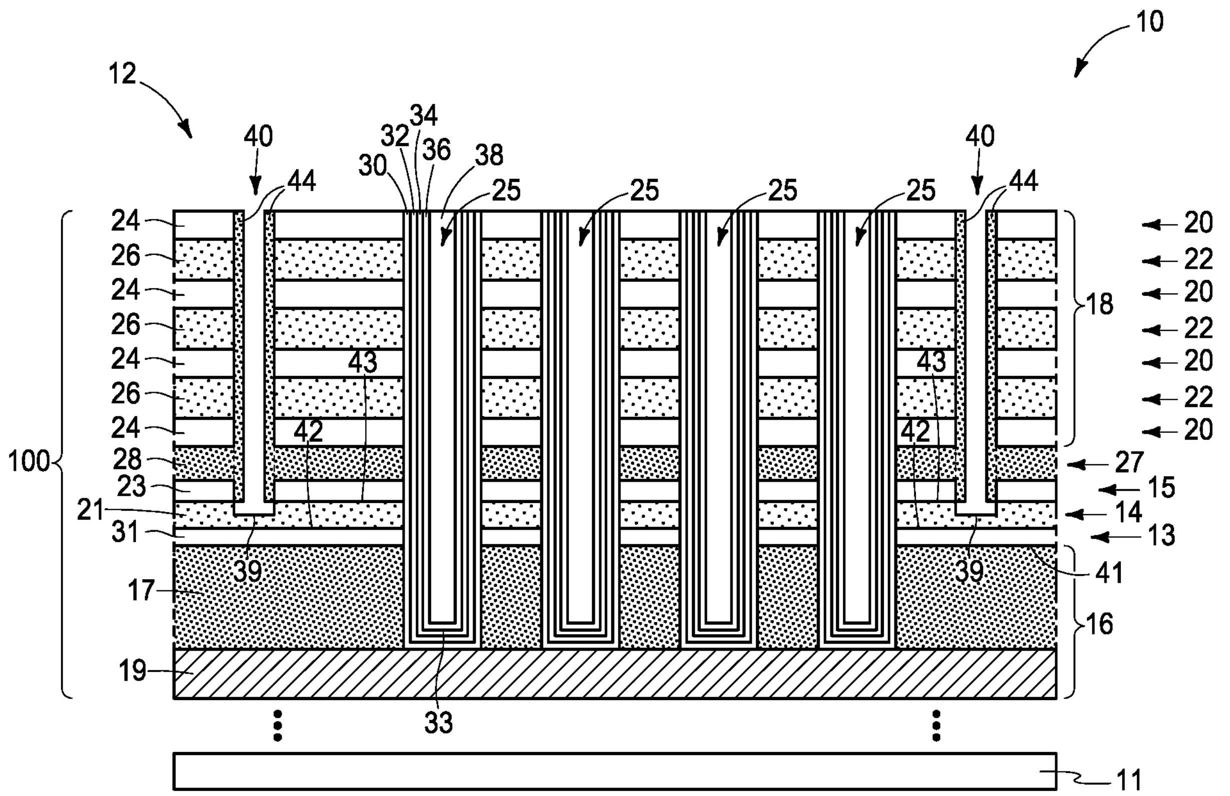

FIG. 7

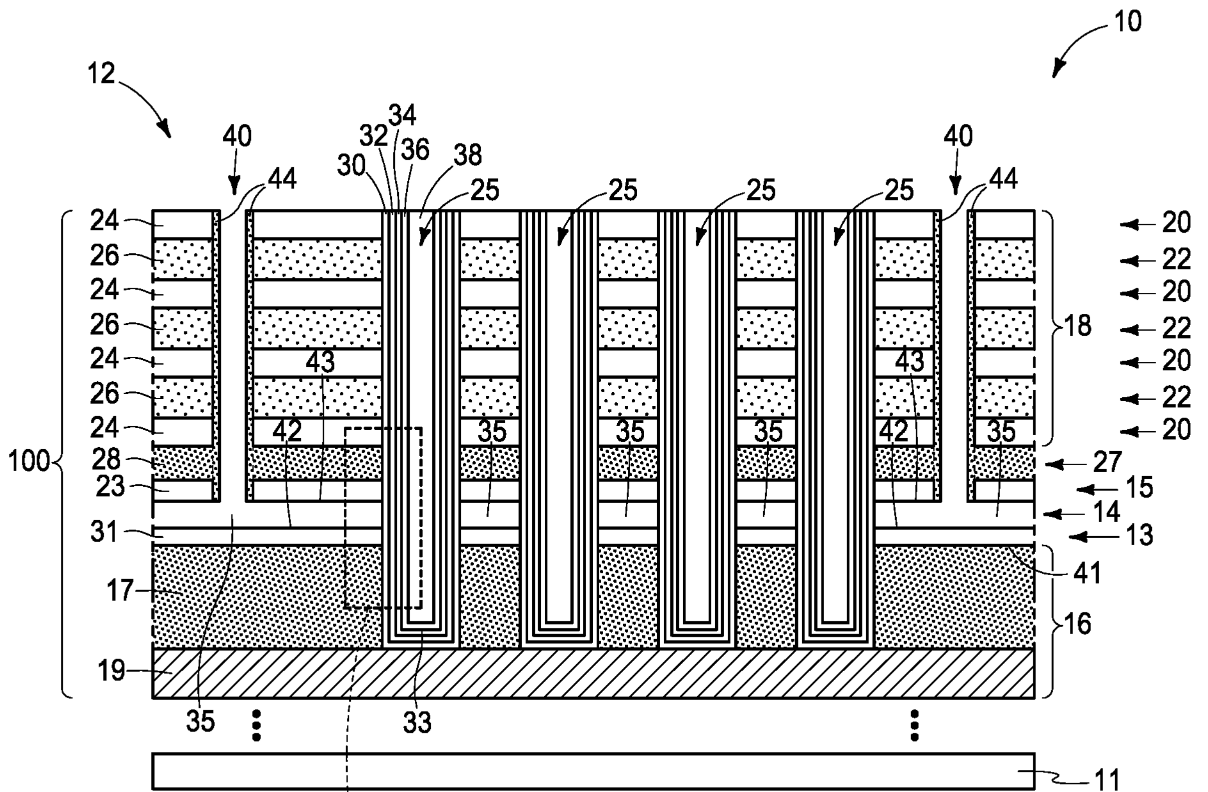

FIG. 8

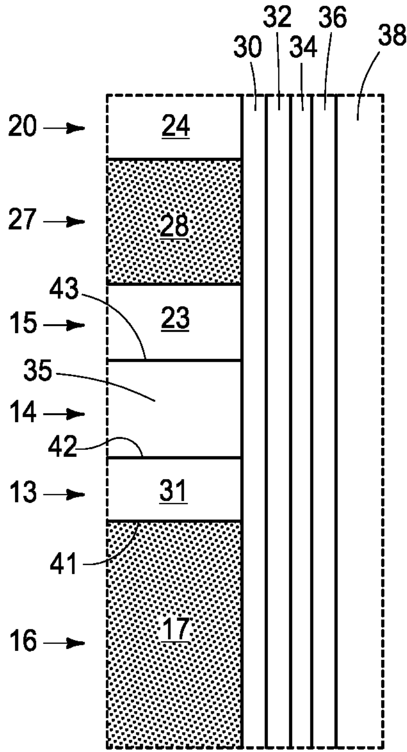

FIG. 9

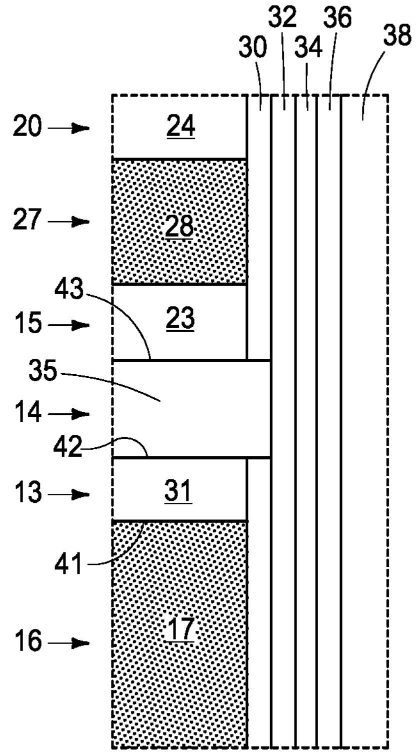

FIG. 10

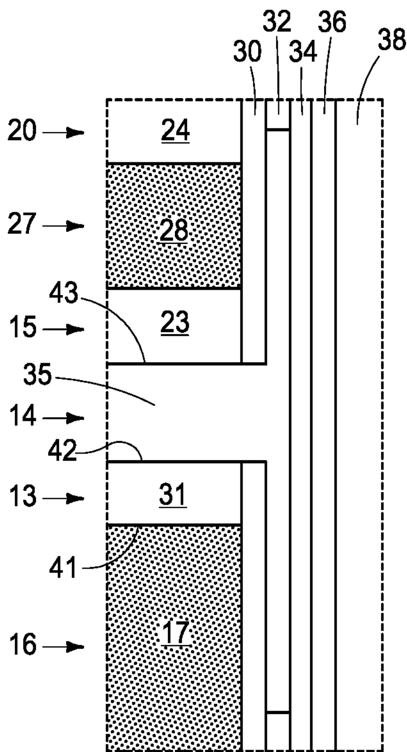

FIG. 11

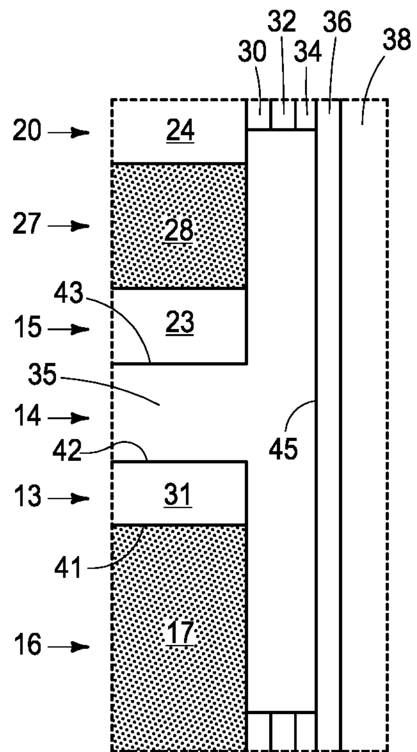

FIG. 12

FIG. 13

FIG. 14

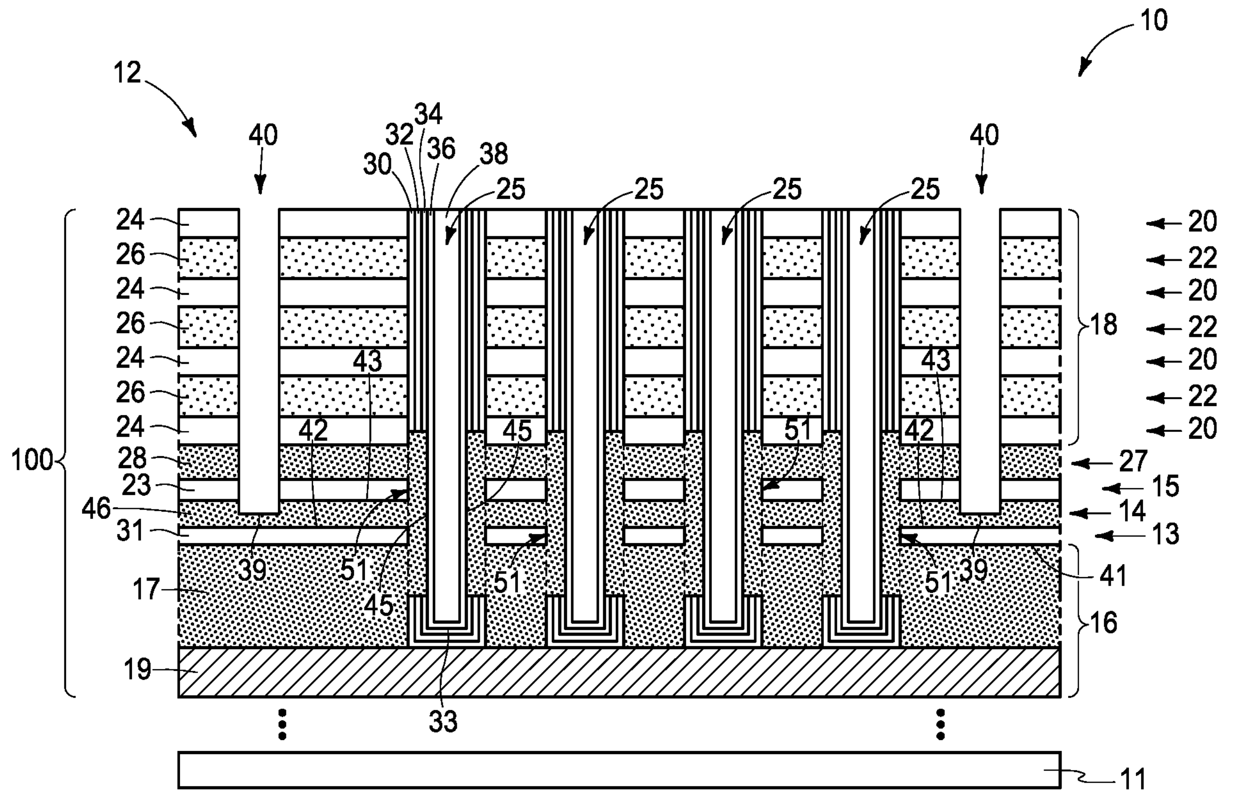

FIG. 15

FIG. 16

FIG. 17

FIG. 18

FIG. 19

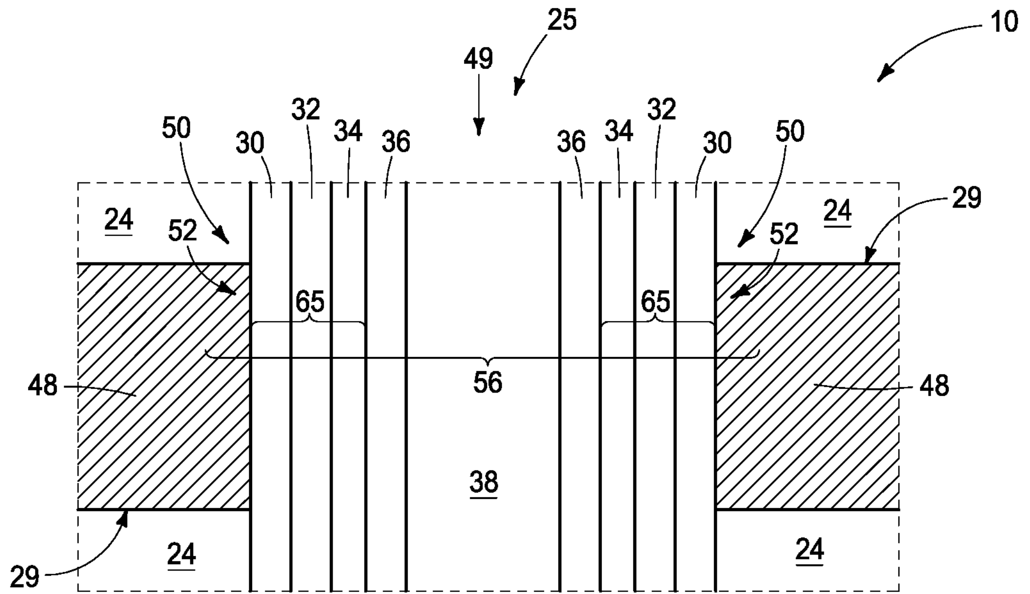

FIG. 20

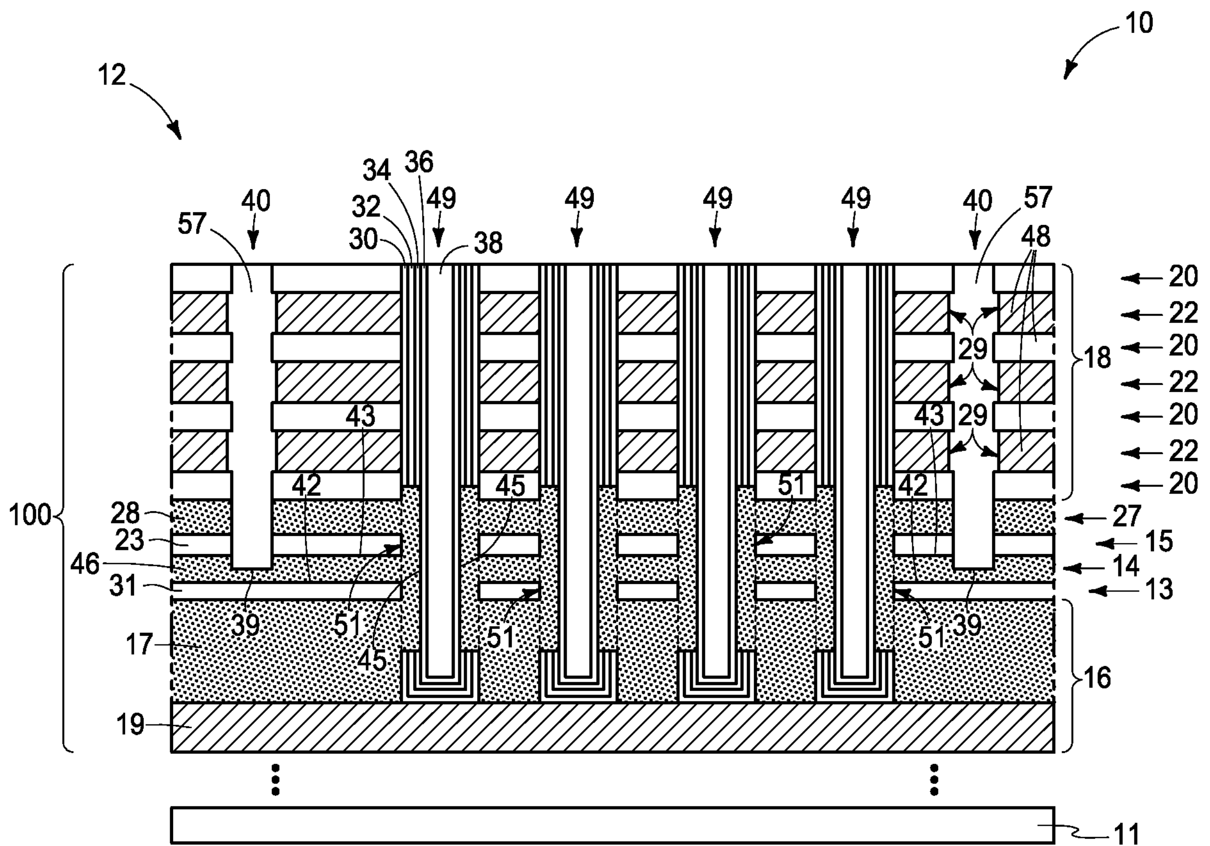

FIG. 21

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2019/057781

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/11582(2017.01)i, H01L 27/1157(2017.01)i, H01L 27/11565(2017.01)i, H01L 29/792(2006.01)i, H01L 29/66(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 27/11582; G11C 16/04; H01L 21/336; H01L 21/768; H01L 23/522; H01L 27/115; H01L 27/11556; H01L 27/1157; H01L 29/786; H01L 27/11565; H01L 29/792; H01L 29/66

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: memory, stack, substrate, insulative, conductive, sacrificial, vertical, tier

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2018-0254285 A1 (SK HYNIX INC.) 06 September 2018 See paragraphs [0021]-[0114] and figures 1A-16A.	1-6,11-19
Y		20-21,23-28,32-45
A		7-10,22,29-31
Y	US 2018-0204849 A1 (MICRON TECHNOLOGY, INC.) 19 July 2018 See paragraphs [0023]-[0037] and figure 1.	20-21,23-28,32-45
A	US 2018-0294273 A1 (MACRONIX INTERNATIONAL CO., LTD.) 11 October 2018 See paragraphs [0017]-[0046] and figures 1A-4C.	1-45
A	KR 10-2016-0094186 A (SK HYNIX INC.) 09 August 2016 See paragraphs [0013]-[0056] and figures 1-6.	1-45
A	KR 10-2016-0018921 A (SAMSUNG ELECTRONICS CO., LTD.) 18 February 2016 See paragraphs [0028]-[0076] and figures 1-10.	1-45

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 February 2020 (14.02.2020)	**17 February 2020 (17.02.2020)**

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

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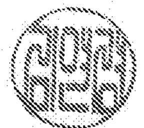

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INTERNATIONAL SEARCH REPORT
Information on patent family members

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