United States Patent

Morgan et al.

[15] **3,654,598**

[45] **Apr. 4, 1972**

[54] DIGITAL CYCLE SYSTEM COORDINATOR FOR TRAFFIC CONTROL SYSTEM

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[22] Filed: **May 20, 1969**

[21] Appl. No.: **826,167**

[52] **U.S. Cl.** **340/41**

[51] **Int. Cl.** **G08g 1/07**

[58] **Field of Search** 340/40, 37, 41, 35, 42

[56] **References Cited**

UNITED STATES PATENTS

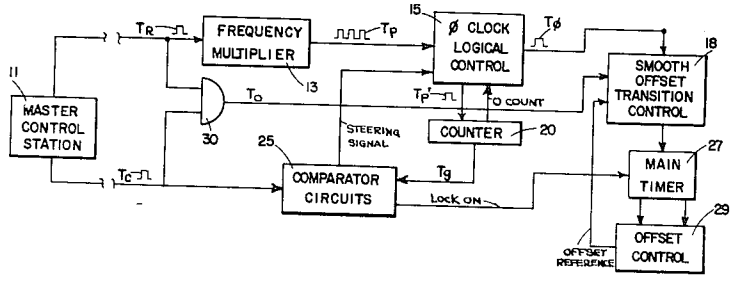
3,128,446	4/1964	Barker	340/35
3,241,104	3/1966	Du Vivier	340/35
3,544,911	12/1970	Du Vivier et al.	340/41
3,551,825	12/1970	Du Vivier et al.	340/41
2,989,728	6/1961	Barker	340/40

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[57] **ABSTRACT**

A pair of periodic pulsating signals are generated at a master control station, such signals differing in frequency by a predetermined small amount. These two frequencies are chosen so that they will periodically arrive in phase with each other at intervals equal to a desired timing cycle. The signals from the master station are transmitted to coordinated intersections in a system where the signals are received by coordinators and digitally processed to generate a plurality of clock pulses, each of said clock pulses representing a finite increment of the total timing cycle. These timing pulses as referred to the commencement of the timing cycle are utilized to synchronize the local controller with the master station and to provide various desired timing offsets.

13 Claims, 4 Drawing Figures



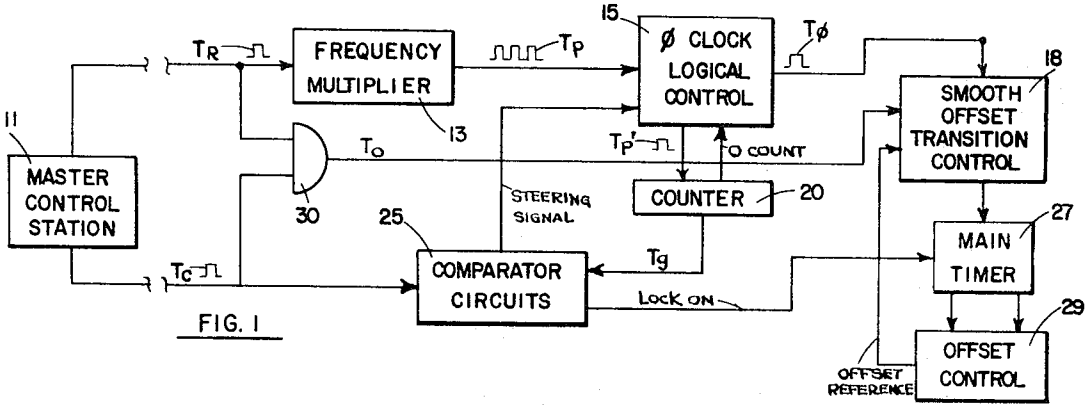


FIG. 1

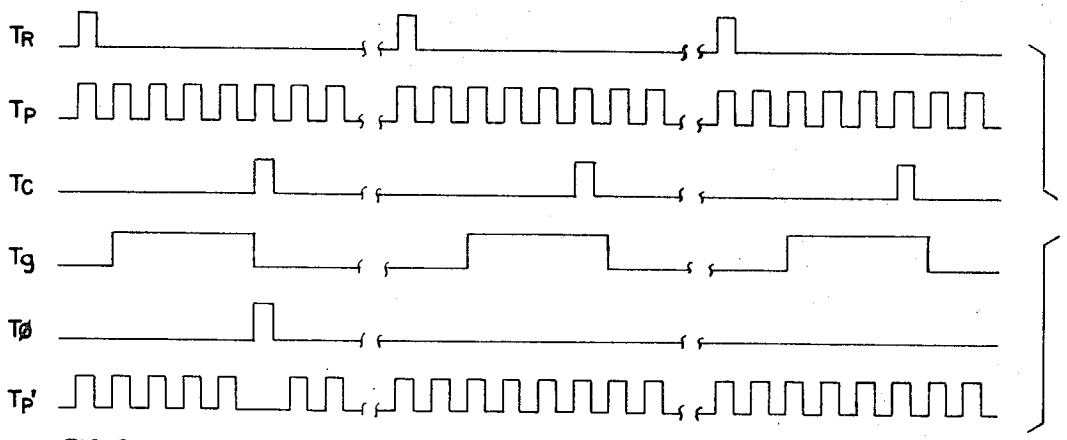


FIG. 2

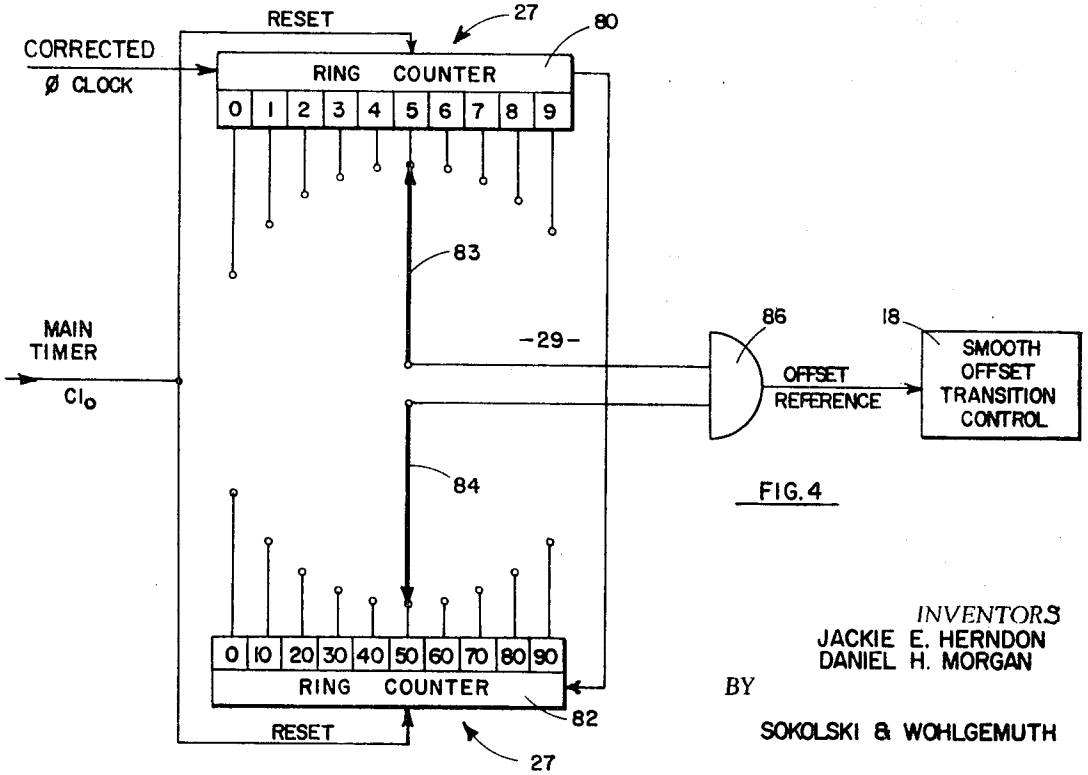


FIG. 4

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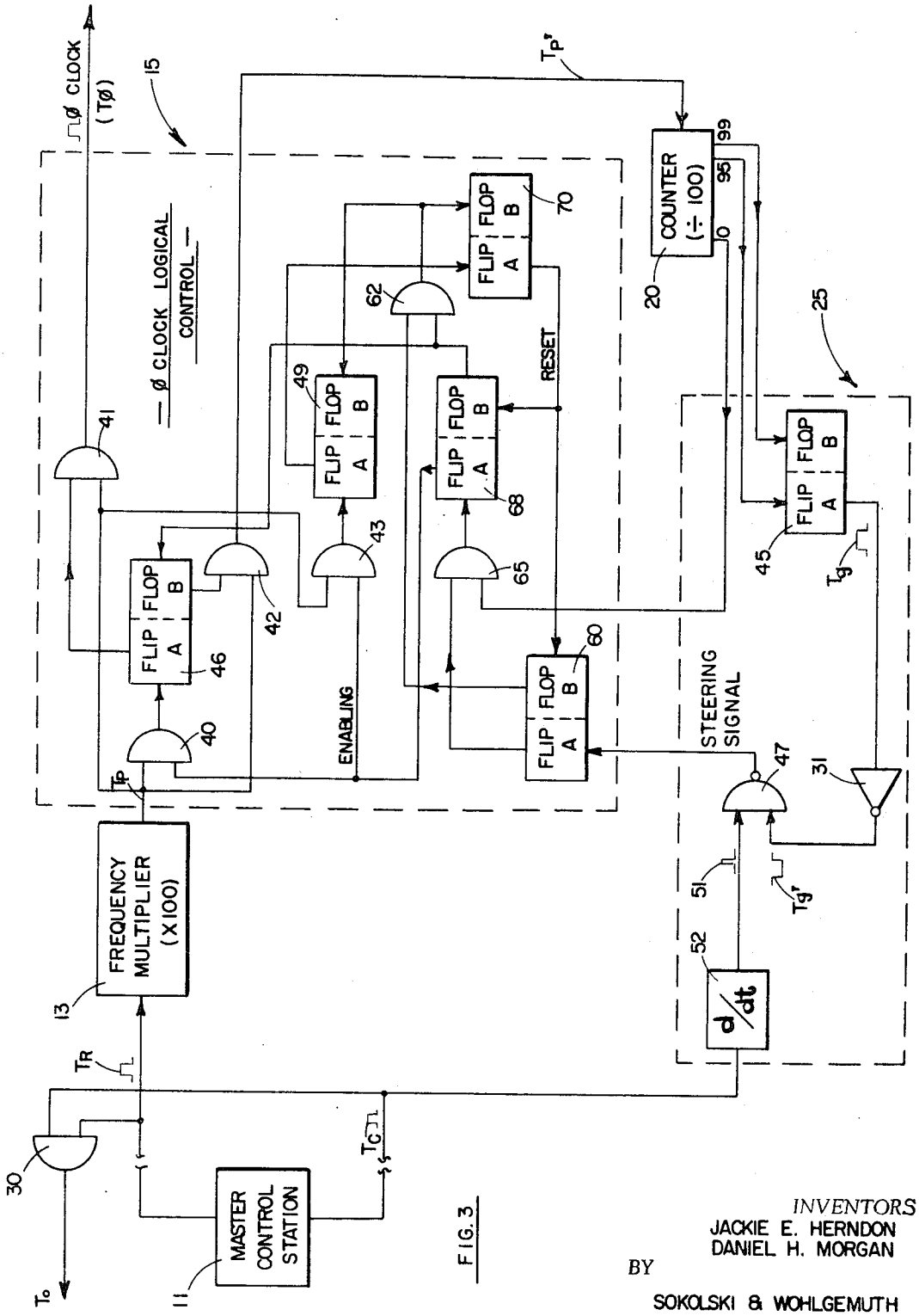


FIG. 3

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DIGITAL CYCLE SYSTEM COORDINATOR FOR TRAFFIC CONTROL SYSTEM

This invention relates to traffic controllers and more particularly to a digital system for coordinating the operation of local traffic controllers from a master control station.

Traffic controllers located at succeeding intersections along a street are generally synchronized from a master control station by means of a coordinating signal which is transmitted from the master station to each of the remote controllers to establish a timing reference. This timing reference signal is utilized to coordinate the timing of the various traffic controllers in a desired manner with offsets in the timing at each intersection being established to handle various traffic conditions.

In the prior art, such as described, for example, in U.S. Pat. No. 2,989,728 issued June 20, 1961, the timing signals are transmitted from the master station as a pair of sine waves which differ slightly in frequency thereby establishing a timing cycle in accordance with the time period between successive in phase conditions of the two sine waves.

In these prior art systems, offset operation at the local controllers is established by means of potentiometers which are utilized to introduce phase shift into one of the signals thereby changing the in phase condition time of occurrence of such signals. This type of implementation has the shortcomings inherent in potentiometers of this type such as the wear involved in the potentiometer wiper contacts which detracts from reliability of operation. Further, such potentiometers are bulky as compared with the semi-conductor type circuitry which is utilized in its stead in the instant invention. Also, it is difficult to accurately set up the offset timing on potentiometers in the phase shift type implementation of the prior art. It is even more difficult to maintain this desired phase shift once it is set, due to the effects of external influences which tend to cause erroneous phase shifts to occur.

The system of this invention overcomes the aforementioned shortcomings of the prior art by providing a fully digital implementation in which rather than using phase shift potentiometers for dividing up the timing cycle, this end result is rather achieved by dividing this cycle into equal digital timing increments, each such increment being represented by a clock pulse. It is possible with the digital implementation of this invention to obtain a very fine division of the timing cycle, the clock pulses representing these divisions being highly accurate and reliable over long periods of operation. Further, timing offsets can be set into the local controllers to a very high degree of accuracy merely by setting control switches to marked positions indicative of precisely defined percentages of the total timing cycle.

It is therefore the principle object of this invention to provide a highly accurate and reliable traffic control cycle coordinator which utilizes a digital implementation for deriving timing signals representing finite percentages of the total timing cycle available.

Other objects of this invention will become apparent from the following description as taken in connection with the accompanying drawings, of which:

FIG. 1 is a block diagram showing the general features of the invention,

FIG. 2 shows a series of waveforms illustrating the operation of one embodiment of the system of the invention,

FIG. 3 is a functional schematic drawing illustrating one embodiment of the system of the invention, and

FIG. 4 is a functional schematic drawing illustrating an offset control which may be utilized in the system of the invention.

Briefly described, the system of the invention operates as follows: Pulsating reference and control signals generated at a master station are fed to each local traffic controller. These signals differ by a frequency such that the time interval between their in phase condition defines a timing cycle. A frequency multiplier at the local traffic controller is used for multiplying the frequency of the reference pulse signal received from the master control station. The factor of this multiplication defines the number of timing increments into which the timing cycle is to be divided. The frequency multiplied signals are fed through a logical gating control to a counter which provides a "tracking gate" signal synchronized with the multiplied pulses and at the frequency of the reference signal. This tracking gate signal is compared with the control signal arriving from the master control station in a comparator circuit wherein a steering signal is generated whenever the two compared signals do not overlap each other. This steering signal is fed to the logical gating control to cause it to gate out a clock pulse representing one of the predetermined finite increments of the timing cycle.

While the logical control is gating this clock pulse, it fails to provide a pulse to the counter, thereby delaying the arrival of the tracking gate by this one pulse and restoring the overlap between the tracking gate and the reference signal. This "lock on" condition during which no clock pulses are gated out but frequency multiplied signals are continually fed to the counter, continues until the difference in frequency between the reference and control signals is again reflected by a sufficient phase shift to cause a loss of overlap between the tracking gate signal and the reference signal, at which time another clock pulse is generated and the "lock-on" is again restored by eliminating one of the pulses fed to the counter. In this manner, successive clock pulses, each of which represents a precise finite percentage of the total timing cycle, are generated with the tracking gate signal thus effectively "-tracking" the reference signal.

Referring now to FIGS. 1 and 2 the basic operation of the system of the invention is illustrated. Two pulsating signals T_R and T_C are fed from master control station **11** to the local station over telephone lines or the like. These signals may be of the order of 400 cycles and differ by a frequency which determines the desired timing cycle. The period of this cycle as already noted is a direct function of the time between the phase coincidence of the two signals. It is to be noted that T_R and T_C may originally be sine waves rather than in pulsating form, such sine waves being squared and appropriately differentiated at the local station to provide digital pulses suitable for processing by the digital circuitry involved. In an operative embodiment of the system of this invention, sine wave signals are so processed to derive digital pulses for T_R and T_C having a duration of an order of **10** microseconds. The frequency, f_c of the cycle signal, T_C for any given desired timing cycle, T can be determined by the following equation:

$$f_c = \frac{(frXT) - 1}{T} \qquad (1)$$

where

f_r is the frequency of the reference signal T_R.

It thus can be seen that the timing cycle, T can be varied as desired by changing f_c, and this parameter is thus controlled in this manner at the master control station.

The reference signal T_R is multiplied in frequency multiplier **13** to produce signals T_P which are at a multiple of the frequency of T_R, this multiplication factor being equal to the number of finite increments into which it is desired that the timing cycle be divided. It is essential that frequency multiplier **13** provide a precise multiplication of pulses T_R so that pulses T_P are phase locked with T_R at all times and are at the precise desired multiple of the reference signal. Multiplier **13** thus must be a highly accurate frequency multiplier, such as, for example, one utilizing a voltage control oscillator which operates in conjunction with a phase lock circuit.

The frequency multiplied signal T_P is fed to Φ clock logical control **15** which alternatively either feeds a single one of these pulses at a time as a phase clock pulse T_ϕ to offset transition control **18** or as a train of pulses T_P' to counter **20**. Counter **20** provides an output to comparator circuits **25** which is in synchronism with a predetermined one of the frequency multiplied pulses T_P and thus phase locked with reference signal T_R. This signal is compared for coincidence with the cycle control signal T_C in the comparator circuits **25**

and a steering signal generated which is fed to Φ clock logical control **15** in accordance with this comparison. As will be explained more fully further on in the specification, when there is coincidence between the two, the frequency multiplied signal T_P is fed through Φ clock logical control **15** to counter **20**. This represents a "lock on" condition which is maintained at all times except when each of the phase clock signals T_ϕ is being generated. A signal indicating such lock-on is fed from the comparator circuits **25** to main timer **27** to indicate operation (and non-operation) of this circuit so that when a failure in operation occurs a standby clock generator (not shown) will be placed in operation.

Due to the difference in frequency between the cycle control pulses T_C and the pulse signals received from counter **20** which are phase locked with the reference signal, T_R, and define the tracking gate signal, T_g, there is a gradual phase shift between these two signals which in the timing increment determined by the multiplication factor of frequency multiplier **13** results in a loss of "lock-on." When this occurs, a steering signal is generated by comparator circuits **25** which causes a single phase clock pulse T_ϕ to be passed from Φ clock logical control **15** to smooth offset transition control **18** and to main timer **27** to provide a clock pulse therefor. While this single phase clock pulse is being gated out, there is no pulse T_P' being gated from the logical control **15** to counter **20** thus slowing up the pulse count within this counter such as to restore lock-on, i.e., time coincidence between the signal fed from counter **20** and cycle control pulse T_C. In this manner, phase clock pulses T_ϕ are generated to represent each incremental shift in phase between signals T_R and T_C, the number of such increments in each timing cycle being determined by the multiplication factor of frequency multiplier **13**. The reference pulses T_R and the cycle control pulses T_C are fed to AND gate **30** which provides a signal indicative of phase coincidence between these two signals.

This signal, T_ϕ, which indicates the start of each "master" timing cycle, is fed to smooth offset transition control **18**. Offset transition control **18** also receives the Φ clock pulses, T_ϕ from Φ clock logical control **15** and the offset reference signals from offset control **29** and provides an adjustment in discrete steps of the timing of the local controller into synchronism with the offset master control signal. A smooth offset transition control which may be utilized with this system is described in co-pending application Ser. No. 610,510 filed Jan. 18, 1967, now U.S. Pat. No. 3,483,508 and assigned to Tamar Electronics Industries, Inc., the assignee of the instant application.

Referring now to FIG. **3**, a functional schematic of one embodiment of the system of the invention is shown. In this particular embodiment, as now to be described, the frequency of reference pulses T_R is higher than that of the cycle control pulses T_C and the frequency multiplication factor of the frequency multiplier is 100. It should be apparent, however, that the system of the invention can operate equally well with different frequency multiplication factors and with an opposite frequency relationship between T_R and T_C to that now to be described. Referring now additionally to FIG. **2** which shows the various waveforms generated in the system of the invention, reference signals T_R which originate in master control station **11** and which, as already noted, are squared and differentiated to produce short duration pulses, are fed to frequency multiplier **13** wherein they are multiplied by precisely 100 times, these multiplied signals T_P being phase locked with reference signals T_R. The multiplied signals T_P are fed to AND gates **40**, **41** and **42** of Φ clock logical control **15**.

Let us assume first that flip-flop stage "B" of flip-flop **46** is in the TRUE state, which as to be explained later on is the situation immediately following the generation of a phase clock, T_ϕ and during "lock on." Under such conditions, pulses T_P will be passed through AND gate **42** to 100 counter **20**, the input pulses to this counter being shown in FIG. **2** as pulses T_P'. Counter **20** is a recycling counter which successively repeats its counting cycle. A signal is fed on the 95th and 99th counts of the counter to flip-flop stages "A" and "B" respectively of flip-flop **45**, thus generating a gate which is provided as gating signal T_g'. Gating signal T_g is inverted by means of inverter **31** and the inverted output T_g' fed to NAND gate **47**. NAND gate **47** also receives a pulse signal **51** which corresponds to the leading edge of cycle control signal T_C this last mentioned signal being differentiated in differentiator **52**. NAND gate **47** is adapted to be responsive only to positive going signals such as pulse **51** and non-responsive to negative going signals such as gating signal T_g'. The amplitude of gating signal T_g' is such that it effectively negates pulse **51** when these two are in time coincidence, i.e., prevents pulse **51** from being passed through the gate under such conditions.

Let us assume that pulse **51** which corresponds to the leading edge of cycle control pulse T_C does not fall within the tracking gate. Under such conditions, NAND gate **47** will gate pulse **51** through to actuate stage "A" of flip-flop **60** to its TRUE state. Stage "A" of this flip-flop is connected to provide an enabling signal to AND gate **65**, and the "0" output of Counter **20** passes through this gate to actuate stage "A" of flip-flop **68**. Stage "A" of flip-flop **68** provides an enabling signal to AND gates **40** and **43**. AND gate **40** will therefore pass a pulse T_P to actuate stage "A" of flip-flop **46**. Stage "A" of flip-flop **46** in turn enables AND gate **41** which passes a Φ clock pulse, T_ϕ.

At the same time AND gate **43** passes a T_P pulse to actuate stage "A" of flip-flop **49**. This flip-flop in turn actuates stage "A" of flip-flop **70** which operates as a reset latch to reset flip-flops **68** and **60**. With the resetting of flip-flop **68**, the enabling signal is removed from AND gates **40** and **43**. Thus, no further Φ clock pulses T_ϕ can be passed through AND gate **41**. At the same time stage "B" of flip-flop **68** provides an actuating signal to stage "B" of flip-flop **46** which enables AND gate **42** to again pass T_P' pulses to counter **20**.

Assuming that pulse **51** and tracking gate, T_g do not arrive in time coincidence, succeeding pulses **51** will cause the gating of successive single Φ clock pulses in the same manner just described. It is to be noted that each time a Φ clock pulse is gated, a T_P' pulse is skipped, as shown, for example, in FIG. **2**. This produces a time delay in the tracking gate, T_g that causes it to rapidly fall into time coincidence or "lock-on" with pulse **51**. It is to be noted that normally a "search" for lock-on only occurs when the equipment is first turned on and once the pulse **51** has initially fallen within the tracking gate to manifest a "lock-on" action, the pulse **51** (leading edge of T_C) is never more than one T_P pulse width out of the gate, as for example shown in the first cycle illustrated in FIG. **2**.

As already noted, the cycle control pulses T_C are constantly shifting in phase with respect to the pulses T_P' such that finally a pulse **51**, which represents the leading edge of T_C will drift out of the tracking gate T_g. When the leading edge of this pulse T_C is no longer within the gate, i.e., has shifted so overlap is lost as shown in the first cycle illustrated in FIG. **2**, NAND gate **47** will gate a TRUE output in response to pulse **51** which will actuate flip-flop stage "A" of flip-flop **60**. The zero count of counter **20** is fed to AND gate **65**, this gate also being connected to receive the output of flip-flop stage "A" of flip-flop **60**. Therefore on the next "0" count of counter **20**, a TRUE output will be fed from AND gate **65** to actuate flip-flop stage "A" of flip-flop **68**. The TRUE output signal from flip-flop stage "A" of flip-flop **68** provides an enabling signal to AND gates **40** and **43**. Therefore, the next T_P pulse which arrives at the input to AND gate **40** will actuate flip-flop stage "A" of flip-flop **46** and also will be passed through AND gate **43** to actuate flip-flop stage "A" of flip-flop **49**. With the actuation of flip-flop stage "A" of flip-flop **46**, AND gate **41** is enabled to pass a Φ clock pulse T_ϕ in response to the next T_P pulse to arrive.

Only a single such Φ clock pulse is passed by virtue of the reset circuits now to be described. As already noted, pulse T_P is also fed through AND gate **43** which is enabled by the same signal fed to AND gate **40**, this pulse operating to actuate flip-flop stage "A" of flip-flop **49**. The signal from flip-flop stage

"A" of flip-flop 49 operates to actuate flip-flop stage "A" of flip-flop 70, which operates as a reset latch. Flip-flop 70 provides a reset signal which drives the "B" stages of flip-flops 68 and 60. The "B" stage of flip-flop 68 actuates the "B" stage of flip-flop 46, thereby restoring the circuit to a condition whereby T_P signals are passed through AND gate 42 as T_P' signals to counter 20 rather than through AND gate 41 as Φ clock signals. It is also to be noted that when the reset signal is provided to flip-flop 68 it in turn provides a gating signal to AND gate 62 which also receives a signal from flip-flop 60 as it is reset. AND gate 62 thus has an output at this time which drives the "B" stages of flip-flops 40 and 70 to reset these flip-flops for a succeeding cycle of operation.

Thus, the gating of phase clock pulses T_ϕ and pulses T_P' for counter 20 are mutually exclusive. As can be seen in FIG. 2, when a phase clock pulse, T_ϕ is present, a pulse T_P' to counter 20 is missing. Dropping of this one T_P' pulse results in a delay corresponding to one pulse in the arrival of the tracking gate T_g relative to the cycle control pulse T_C causing these pulses to fall back into coincidence as indicated in the second cycle shown in FIG. 2, thereby reestablishing lock-on. Thus, it will be apparent that each time pulse T_C shifts in phase one percent of the cycle with respect to the reference pulse T_R with which the gate T_g is synchronized, that the pulse T_C will have "drifted" out of the gate, thereby initiating the generation of a phase clock pulse and simultaneously dropping one of the pulses, T_P' fed to counter 20, thereby causing a restoration of a lock-on condition until another such one percent timing increment has been completed. This operation thus repeats itself over the entire timing cycle, generating 100 phase clock pulses during this period, each of such pulses representing a one percent increment in this timing cycle.

It is to be noted that tracking gate T_G is purposely made fairly wide, i.e., to cover several pulse counts, this to facilitate lock-on and minimize the effects of jitter on the signal which might erroneously cause a loss of the lock-on condition. It is further to be noted that it may also be desirable to place a digital filter in the comparator circuit such filter being implemented for example by means of a bidirectional counter which will only provide the gating signal through the flip-flop 60 when a predetermined number of T_C pulses have been successively received, thus minimizing the possibilities of an extraneous pulse on the line causing erroneous actuation of flip-flop 60.

Referring now to FIG. 4 an offset control 29 which may be utilized in the system of the invention is illustrated. The corrected Φ clock pulses arriving from Φ clock logical control 15 as corrected by the output of smooth offset transition control 18 are fed to ten stage ring counter 80, the output of which is connected to drive ten stage ring counter 82. These counters are the timing counters of main timer 27. Both counters are reset to zero by the Cl_0 pulse in main timer 27, indicating the initiation of main timer timing cycle. The counters may be those of a traffic control system such as described in connection with FIG. 3 of U.S. Pat. No. 3,376,546, issued Apr. 2, 1968. The Cl_0 pulse in this instance would be the reset signal arriving on line 68 or line 69. The offset control switches 83 and 84 would of course be connected to the counter outputs in parallel with the other leads connected thereto to implement the normal timing functions of the controller. Thus the ring counters will successively count up to a hundred, counter 82 producing outputs for zero and multiplies of 10 percent of this cycle while counter 80 produces outputs for zero and at 1 percent increments of the timing cycle. Switches 83 and 84 may be set to select any desired percentage of the total timing cycle. Switches 83 and 84 are connected through AND gate 86 to the smooth offset transition control 18. Thus, for example, with switches 83 and 84 set as indicated in FIG. 4, a timing signal will be fed to the smooth offset transition control 18 each time 55 percent of the timing cycle has been completed this signal being used to provide this selected offset timing. As can be seen in this manner, any percentage of the total timing cycle can be selected to provide an offset timing signal for main timer 27. The switches may, of course include relays set from a remote location.

The system of this invention thus provides highly accurate means for generating a timing signal precisely corresponding to a predetermined percentage of a timing cycle generated in a master control station. This implementation is totally digital and utilizes a unique "lock-on" technique for generating successive signals representing the timing increments.

We claim:

1. In a system for coordinating the timing operation of a local traffic controller with timing signals generated at a master control station, said timing signals comprising first and second different frequency pulsating signals, a timing cycle being defined by the interval between successive phase coincidence between said signals, the improvement comprising means in the local controller for digitally generating signals indicative of precise increments of the timing cycle, said improvement including:

frequency multiplier means for multiplying the frequency of said first signal by a multiplication factor corresponding to the number of the timing increments to be generated,

logical control means for receiving the multiplied output of said frequency multiplier means,

means responsive to the multiplied signal output of said logical control means for generating a tracking gate signal synchronized with a predetermined timing increment of said multiplied signal and at a frequency corresponding to said first signal,

comparator means for comparing said tracking gate signal for time coincidence with said second signal,

said comparator means generating a steering signal for said logical control means to cause said logical control means to generate a phase clock pulse corresponding to one of the increments of said timing cycle when the tracking and second signals are not in time coincidence and for feeding said multiplied signal to said means for generating a tracking gate signal when the tracking and second signals are in time coincidence.

2. The system of claim 1 wherein said means for generating a tracking gate signal comprises a counter for counting said multiplied signal output fed thereto from said logical control means and a flip-flop connected to receive the outputs of two predetermined stages of said counter, one of said outputs operating to set the flipflop, the other of said outputs operating to reset the flipflop, the tracking gate signal being the flip-flop output.

3. The system of claim 1 and further including offset control means for generating a signal in accordance with a selected number of said timing cycle increments, pulses corresponding to said increments being fed to said offset control means.

4. The system of claim 3 wherein the main timer of said local traffic controller includes a counter and said offset control means includes selector switch means for selecting a predetermined count output of said counter.

5. The system of claim 1 wherein said logical control means includes reset circuit means for permitting only a single incremental Φ clock pulse output for each timing increment.

6. A system for generating timing signals representing precise increments of a timing cycle comprising:

means for generating first and second pulsating signals having a predetermined difference in frequency, the period between which said signals are in phase coincidence defining said timing cycle,

means for multiplying said first pulsating signal by a factor determinative of the number of said timing cycle increments in each cycle,

counter means,

offset transition control means,

logical control means for receiving the multiplied signal and alternatively feeding said multiplied signal to said counter means or to said offset transition control means,

said counter means being adapted to successively count to a number of bits equal to said multiplying factor.

means responsive to said counter means for generating a tracking gate signal at the frequency of aid first pulsating signal and synchronized with a predetermined bit count of said counter means, and

means for comparing said tracking gate signal and said second pulsating signal for time coincidence,

said logical control means being responsive to the output of said comparing means and operating to feed said multiplied signal as a phase clock pulse (TΦ) to said offset transition control means when said second pulsating signal and said gate signal are not in coincidence and to feed said multiplied signal (T_p) to said counter means when said second pulsating signal and said tracking gate signal are in coincidence,

whereby each time one of said phase clock pulses is fed to said offset transition control means, the timing of said tracking gate signal is delayed so as to tend to restore coincidence between said tracking gate signal and said second pulsating signal.

7. The system of claim 6 and further including offset control means for selectively setting a predetermined timing offset into said system.

8. In a system for coordinating the timing operation of a local traffic controller from a master station, said master station including means for generating pulsating reference and control signals having a predetermined small difference in frequency, the period between which said signals are in phase coincidence defining a timing cycle, the improvement being means for generating digital timing signals defining precise increments of said timing cycle comprising:

frequency multiplier means for precisely multiplying said reference signal by a factor corresponding to the number of said timing increments in each cycle,

counter means for dividing the output of said multiplier means by said factor,

means responsive to said counter means for generating a tracking gate signal synchronized with a predetermined bit of said counter means,

means for comparing said gate signal and said control signal for time coincidence, and

logical control means interposed between said multiplier means and said counter means and responsive to the output of said comparing means for controlling the tracking of said control signal by said tracking gate signal, said control means alternatively feeding the output of said multiplier means to said counter means when said gate signal and said control signal are in time coincidence and providing a pulse output of said multiplier means as an incremental phase clock pulse timing signal on the arrival of each control signal whenever said gate and control signals are not in time coincidence.

9. The system of claim 8 wherein said means for generating a tracking gate signal comprises a flipflop connected to receive the output of said predetermined counter means bit as a set signal and another predetermined bit output of said counter means as a reset signal.

10. The system of claim 8 wherein said logical control means includes reset circuit means for permitting only a single incremental timing pulse output for each of the predetermined timing increments.

11. The system of claim 8 and further including AND gate means for generating a timing reference signal when the reference and control signals are in phase coincidence.

12. The system of claim 8 wherein said comparing means comprises a NAND gate for providing a signal to said logical control means in response to said control signal only when said control signal and said gate signal are not in time coincidence.

13. A method for coordinating the timing operation of a local traffic controller with a master control station comprising the steps of:

generating reference and cycle control pulsating signals at the master station, said signals differing in frequency by an amount defining a timing cycle,

transmitting said signals to said local controller,

multiplying said reference signal by a factor defining increments of said timing cycle,

generating a tracking gate signal synchronized with one of the timing increments of said multiplied signals and at the frequency of said reference signal,

comparing said tracking gate signal and said cycle control signal for time coincidence, and

logically gating out one pulse of said multiplied signal at a time, in response to a cycle control signal, as a clock signal, whenever the tracking gate signal and the cycle control signal are not in time coincidence.

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