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(54) Title: A METHOD OF FABRICATING A SEMICONDUCTOR DEVICE

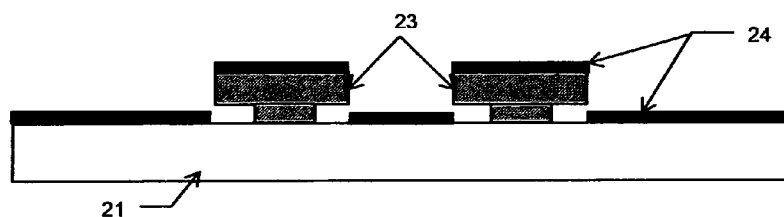


FIG. 3e

(57) Abstract: The present invention relates to a method for fabricating a semiconductor device using a lift-off method. The method comprises the steps of depositing and patterning a sacrificial layer (22) onto a substrate (21), wherein at least one portion of the substrate surface (21a) is covered by the sacrificial layer (22) and at least one portion of the substrate surface (21b) is exposed; depositing and patterning a chemical resist (23) onto the sacrificial layer (22) and the exposed substrate surface (21b); removing the sacrificial layer (22); depositing a semiconductor film (24) onto the substrate (21) and the chemical resist (23); and removing the chemical resist (23) and the semiconductor film (24) deposited on the chemical resist (23).



A METHOD OF FABRICATING A SEMICONDUCTOR DEVICE

FIELD OF INVENTION

+ The present invention relates to a method for fabricating a semiconductor
5 device and more particularly, a method of fabricating a semiconductor device using a lift-off method.

BACKGROUND OF THE INVENTION

In micro-fabrication process, patterning of thin film layers are essential to
10 create structures and features for Micro-Electro-Mechanical Systems (MEMS) and Nano-Electro-Mechanical Systems (NEMS) devices such as sensors and actuators. The conventional method for patterning of thin film layers utilises photolithography method which includes dry etching process such as Deep Reactive Ion Etching (DRIE) and Reactive Ion Etching (RIE), or wet etching process such as hydrofluoric
15 (HF) etching, potassium hydroxide (KOH) etching, Buffered Oxide Etch (BOE) etching.

However, it has been found that patterning of noble metal films or alloys such as platinum, tantalum, nickel, iron, chromium, gold and silver are hard to be
20 performed using conventional etching process due to lack of high vapour pressure compounds of the metals with common dry etching gases such as chlorine (Cl_2), bromine (Br_2) and fluorine (F_2).

In view of that, a conventional lift-off method is commonly deployed for
25 patterning of these materials. The steps to perform the conventional lift-off method are shown in FIGS. 1(a-d). Initially, a sacrificial layer (12) such as photoresist is deposited onto a substrate (11) as shown in FIG. 1a. The photoresist (12) is exposed and developed through lithography to create an inverse pattern as shown in FIG. 1b. Thereon, as shown in FIG. 1c, a target material (13) such as a thin metal layer is
30 deposited covering the photoresist (12) and the exposed substrate (11) surface. Thereafter, the photoresist (12) is washed out together with parts of the target material (13) covering it. Hence, the target material (13) on the photoresist (12) has been lifted-off and leaving only the target material (13) which was deposited directly on the substrate (11) surface as shown in FIG. 1d.

The conventional lift-off method has some drawbacks. There is a limitation on the thickness of the target material (13) that can be lifted-off when using a single resist (12) whereby the target material (13) needs to be 5 times thinner than the resist (12). Moreover, the lift-off method creates undesired effect of ears (14) forming after lift-off due to low resist aspect ratio. FIGS. 1d and 2 show the ears (14) formed after lifting-off the sacrificial layer (12). The ears (14) formed can influence device performance and its fragility is a source of contamination to downstream processes.

Hence, there is a need for a method for fabricating a semiconductor device using lift-off method that addresses thick patterning of target material layers without having the ears effect.

SUMMARY OF INVENTION

The present invention relates to a method for fabricating a semiconductor device using a lift-off method. The method is characterized by the steps of depositing and patterning a sacrificial layer (22) onto a substrate (21), wherein at least one portion of the substrate surface (21a) is covered by the sacrificial layer (22) and at least one portion of the substrate surface (21b) is exposed; depositing and patterning a chemical resist (23) onto the sacrificial layer (22) and the exposed substrate surface (21b); removing the sacrificial layer (22); depositing a semiconductor film (24) onto the substrate (21) and the chemical resist (23); and removing the chemical resist (23) and the semiconductor film (24) deposited on the chemical resist (23).

Preferably, the sacrificial layer (22) has a maximum thickness of 20μm and it is made of polycrystalline silicon, silicon dioxide, spin-on-glass (SOG), phosphosilicate glass (PSG), or boron phosphosilicate glass (BPSG).

Preferably, the chemical resist (23) has a minimum thickness of 50nm.

Preferably, the semiconductor film (24) has a thickness in a range of 5nm to 3μm and it is made of alloy, aluminium, gold, silver, platinum, titanium, tungsten, chromium, molybdenum, nickel, vanadium, palladium, metal oxides or any combination thereof.

Preferably, the chemical resist (23) forms a T-shaped structure on the exposed substrate surface (21b).

+ Preferably, the sacrificial layer (22) is removed through wet etching by using
5 wet chemical etchant such as a hydrofluoric acid based solution or a mixture solution of nitric acid and hydrofluoric acid.

Advantageously, the present invention uses thin resist material that eliminates the issue of poor lithographic resolution due to the use of thick resist which is critical
10 in producing nanostructures semiconductor.

Advantageously, the present invention does not impact lithographic resolution as it does not require thick or bi-layer chemical resist.

15 Advantageously, the present invention eliminates the ears effect after lifting-off the resist.

Advantageously, the present invention allows the fabrication of semiconductor devices having structures of high aspect ratios.
20

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1(a-d) show a conventional lift-off method used in fabricating a semiconductor device.

25 **FIG. 2** is a SEM image showing a formation of ears (14) after the lift-off method of **FIGS. 1**.

FIGS. 3(a-f) show a lift-off method used in fabricating a semiconductor device in accordance with an embodiment of the present invention.

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DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of the present invention will be described herein below with reference to the accompanying drawings. In the following description, well known functions or constructions are not described in detail since they would obscure
35 the description with unnecessary detail.

Referring now to **FIGS 3(a-f)**, a method of fabricating a semiconductor device using a lift-off method is provided. Initially, a substrate (21) is prepared for patterning
+ of semiconductor film (24) as shown in **FIG. 3a**. Preferably, the substrate (21) is a
5 silicon or glass substrate.

Thereon, in **FIG. 3b**, a sacrificial layer (22) is deposited on the surface of the substrate (21). Preferably, the sacrificial layer (22) has a thickness of up to 20µm. Moreover, the sacrificial layer (22) is preferably made of polycrystalline silicon, silicon
10 dioxide, spin-on-glass (SOG), phosphosilicate glass (PSG), boron phosphosilicate glass (BPSG) or any other material that have good adhesion to the substrate (21), able to be removed using wet chemical etchants, and able to withstand high temperature. The sacrificial layer (22) deposited on the substrate (21) is patterned
15 through etching or photolithography and thus, providing at least one portion of the substrate surface (21a) covered by the sacrificial layer (22) and at least one portion of the substrate surface exposed (21b).

In **FIG. 3c**, a chemical resist (23) is deposited and patterned on the sacrificial layer (22) through lithography and thus, covering the surface of the sacrificial layer
20 (22) and the exposed substrate surface (21b). As a result, the chemical resist (23) forms a T-shaped structure on the exposed substrate surface (21b). Preferably, the chemical resist (23) has a minimum thickness of 50nm.

Thereon, in **FIG. 3d**, the sacrificial layer (22) is removed through wet etching.
25 Preferably, hydrofluoric acid based solution or a mixture solution of nitric acid and hydrofluoric acid is used as wet chemical etchant to etch the sacrificial layer (22). The removal of the sacrificial layer (22) leaves the T-shaped structure of the chemical resist (23) on the substrate (21).

30 In **FIG. 3e**, semiconductor film (24) is deposited on the substrate (21) and the T-shaped structure of the chemical resist (23). Therefore, the top portion of the substrate (21) and the T-shaped structure of the chemical resist (23) are layered with the semiconductor film (24). Preferably, the semiconductor film (24) has a thickness in a range of 5nm to 3µm. Moreover, the semiconductor film (24) is preferably made
35 of alloy, aluminium, gold, silver, platinum, titanium, tungsten, chromium,

molybdenum, nickel, vanadium, palladium or metal oxides such as titanium dioxide (TiO_2), zinc oxide (ZnO), niobium pentoxide (Nb_2O_5), tungsten oxide (WO_3), tin dioxide (SnO_2), magnesium oxide (MgO) or any combination thereof.

+

5 In FIG. 3f, the chemical resist (23) is removed by using solvent or acid such as but not limited to acetone, NMP (1-Methyl-2-pyrrolidone), DMSO (Dimethyl sulfoxide), fuming nitric acid, sulfuric acid and chromic acid. Hence, the semiconductor film (24) deposited on top of the chemical resist (23) is lifted-off and leaving only the semiconductor film (24) which was deposited directly on the
10 substrate (21) surface.

While embodiments of the invention have been illustrated and described, it is not intended that these embodiments illustrated and describe all possible forms of the invention. Rather, the words used in the specifications are words of description
15 rather than limitation and various changes may be made without departing from the scope of the invention.

CLAIMS

1. A method for fabricating a semiconductor device using a lift-off method is characterized by the steps of:
 - 5 + a) depositing and patterning a sacrificial layer (22) onto a substrate (21), wherein at least one portion of the substrate surface (21a) is covered by the sacrificial layer (22) and at least one portion of the substrate surface (21b) is exposed;
 - 10 b) depositing and patterning a chemical resist (23) onto the sacrificial layer (22) and the exposed substrate surface (21b);
 - c) removing the sacrificial layer (22);
 - 15 d) depositing a semiconductor film (24) onto the substrate (21) and the chemical resist (23); and
 - e) removing the chemical resist (23) and the semiconductor film (24) deposited on the chemical resist (23).
- 20 2. A method as claimed in claim 1, wherein the sacrificial layer (22) has a maximum thickness of 20µm.
3. A method as claimed in claim 1, wherein the sacrificial layer (22) is made of polycrystalline silicon, silicon dioxide, spin-on-glass (SOG), phosphosilicate
25 glass (PSG), or boron phosphosilicate glass (BPSG).
4. A method as claimed in claim 1, wherein the chemical resist (23) has a minimum thickness of 50nm.
- 30 5. A method as claimed in claim 1, wherein the semiconductor film (24) has a thickness in a range of 5nm to 3µm.
6. A method as claimed in claim 1, wherein the semiconductor film (24) is made of alloy, aluminium, gold, silver, platinum, titanium, tungsten, chromium,

molybdenum, nickel, vanadium, palladium, metal oxides or any combination thereof.

- ⁺ 7. A method as claimed in step (b) of claim 1, wherein the chemical resist (23)
5 forms a T-shaped structure on the exposed substrate surface (21b).
8. A method as claimed in step (c) of claim 1, wherein the sacrificial layer (22) is removed through wet etching by using wet chemical etchant.
- 10 9. A method as claimed in claim 8, wherein the wet chemical etchant is a hydrofluoric acid based solution or a mixture solution of nitric acid and hydrofluoric acid.

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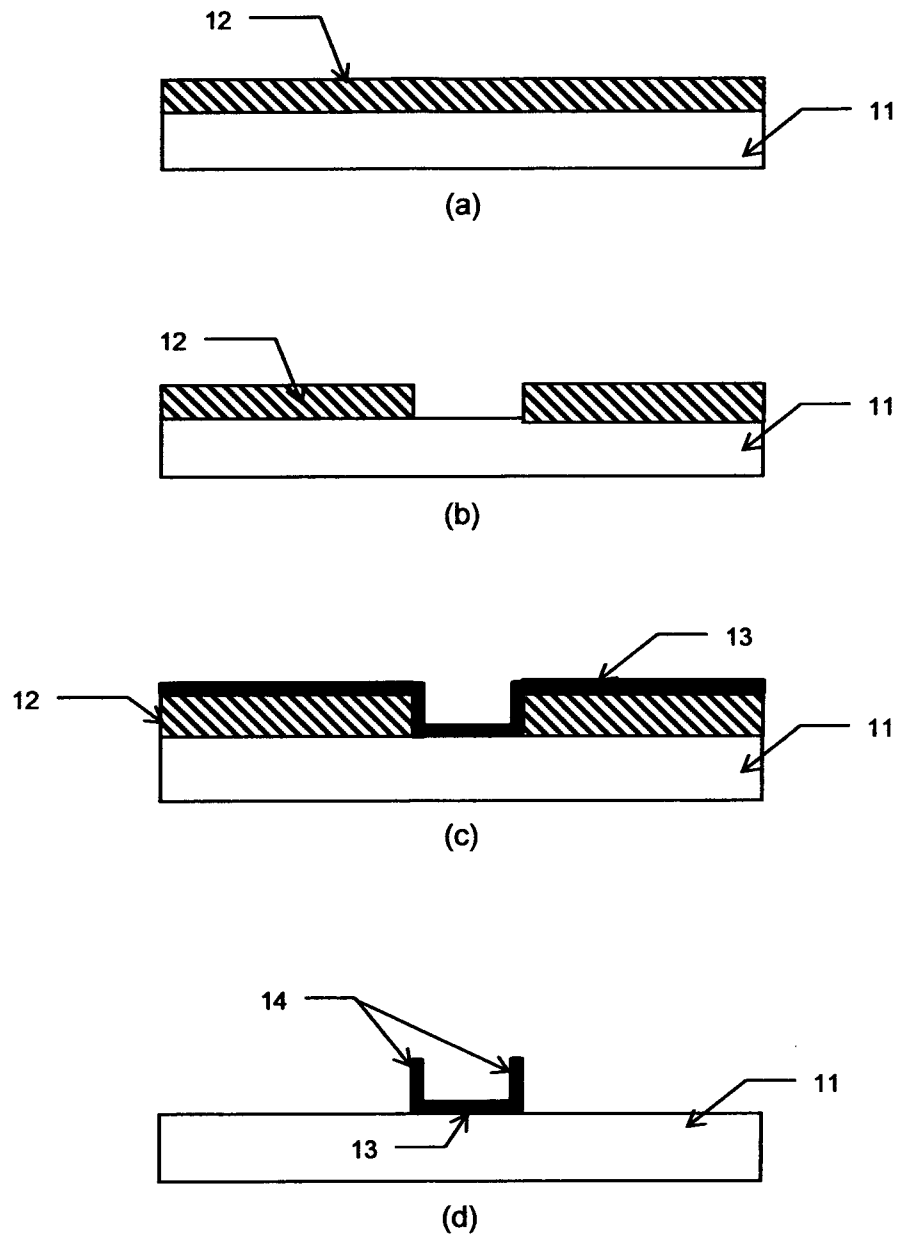


FIG. 1
PRIOR ART

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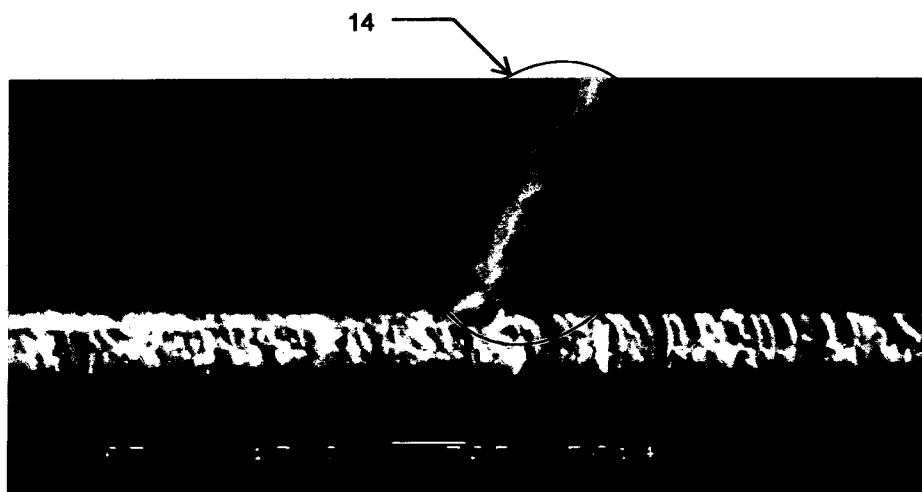


FIG. 2

PRIOR ART

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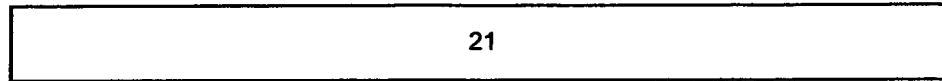


FIG. 3a

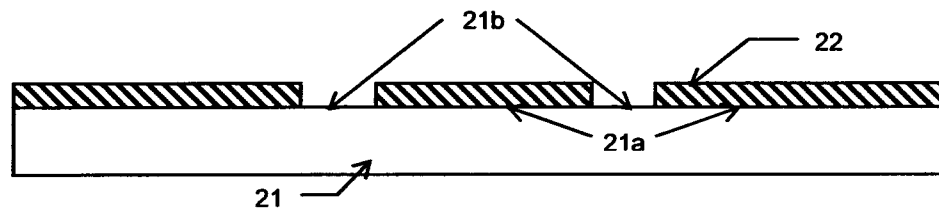


FIG. 3b

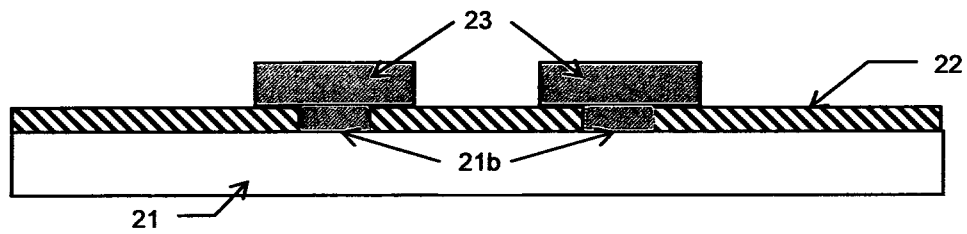


FIG. 3c

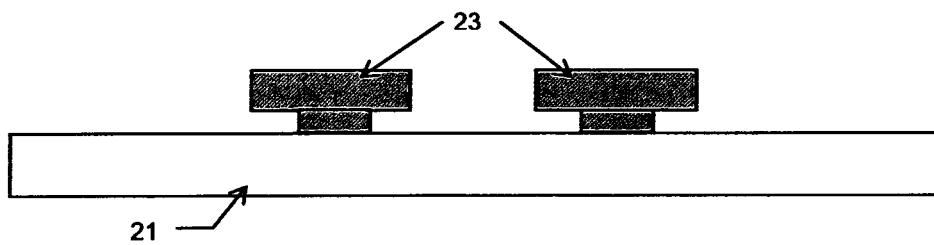


FIG. 3d

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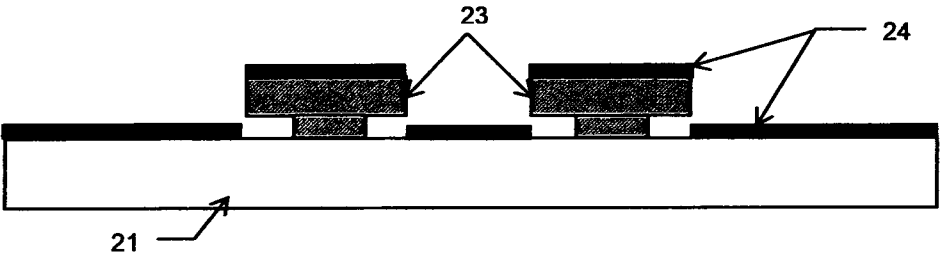


FIG. 3e

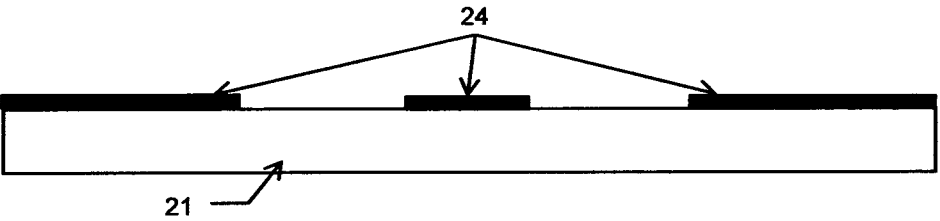


FIG. 3f

INTERNATIONAL SEARCH REPORT

International application No.
PCT/MY2011/000112

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

H01L 21/20 (2006.01)

H01L 21/311 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Google-Fabrication of semiconductors by lift-off method; Fabrication of semiconductors using chemical resist layer. E-spacenet, EPODOC and WPI- H01L21/ic and keywords-semiconductor?, lift_off, peel, exfoliate T-shape, chemical w resist, sacrificial, temporary, release, two, further, second, another, layer, film, coating.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 6,667,850 B2 (KHAN et al.) 23 December 2003 Entire document particularly fig. 1-3 and column 3-4	1, 4, 7, 8 2, 3, 5, 6, 9
Y	US 4,497,684 A (SEBESTA) 5 February 1985 Entire document particularly column 4-5	2, 3, 5, 9
Y	US 2005/0070113 A1 (HANBERG) 31 March 2005 Entire document particularly fig. 1 and paragraph 0021	9
Y	US 2010/0093176 A1 (CHANG) 15 April 2010 Entire document particularly paragraphs 0008, 0012, 0025	3, 6, 9



Further documents are listed in the continuation of Box C



See patent family annex

* "A"	Special categories of cited documents: document defining the general state of the art which is not considered to be of particular relevance	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E"	earlier application or patent but published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means	"&"	document member of the same patent family
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/MY2011/000112

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member	
US 6667850	US 6495311	US 2003036021	
US 4497684	NONE		
US 2005070113	CN 1606139	US 7319076	WO 2005031828
US 2010093176	CN 101789367		
Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.			
END OF ANNEX			