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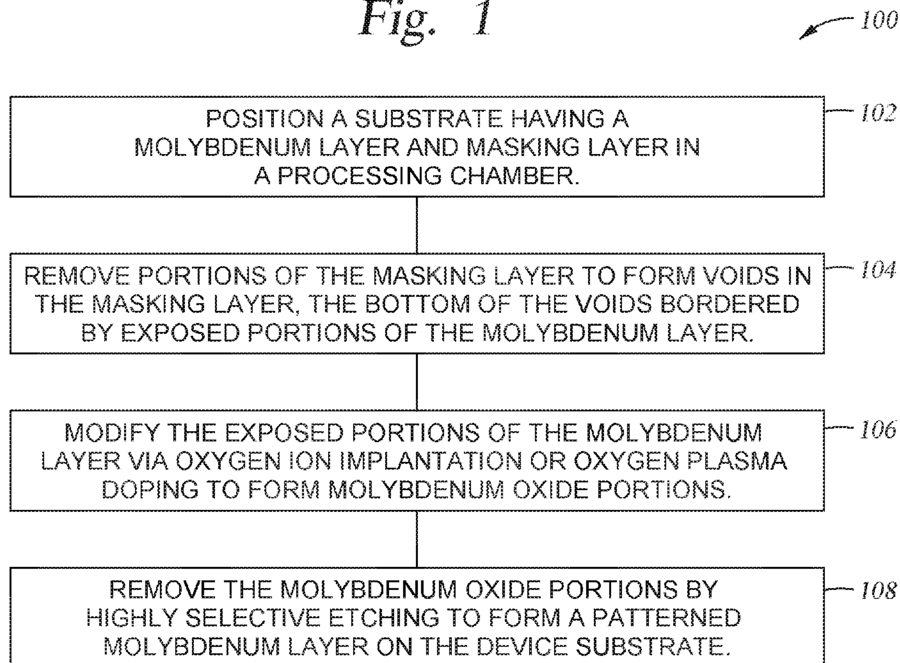
(54) **Title:** METHODS OF PATTERNING METAL LAYERS



(57) **Abstract:** The present disclosure provides methods for patterning a metal layer of a device (e.g., a semiconductor device) to form features in the interconnect layer as part of a process for manufacturing an interconnect structure of the device. The disclosed methods describe processes for patterning a molybdenum layer with improved selectivity. For example, the disclosure provides methods for modifying and removing areas of the molybdenum layer by annealing or etching without damaging other device structures or materials.

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METHODS OF PATTERNING METAL LAYERS

BACKGROUND

Field

[0001] Embodiments of the present disclosure relate to methods for forming semiconductor device structures. More specifically, embodiments of the present disclosure relate to methods of patterning metal layers on a substrate.

Description of the Related Art

[0002] Integrated circuits have evolved into complex devices that can include millions of transistors, capacitors, and resistors on a single chip. The evolution of chip design has resulted in greater circuit density to improve the process capability and speed of chips. The demands for faster processing capability with greater circuit densities impose corresponding demands on the materials used to fabricate such integrated circuits. In particular, as the dimensions of integrated circuit components are reduced to the sub-10 nm scale, low resistivity conductive materials, as well as low dielectric constant insulating materials, are used to obtain suitable electrical performance from such components.

[0003] Interconnects provide the electrical connections between the various electronic components of an integrated circuit and form the connections between these elements and the device's external contact elements (e.g. pins) for connecting the integrated circuit to other circuits. Traditionally, copper has been the material of choice for interconnect layers. However, at the sub-10 nm scale, conventional copper interconnects exhibit reduced conductivity, making copper an undesirable material for advanced nodes. Recently, alternative materials have been sought to overcome the deficiencies of copper as an interconnect material. One such material is molybdenum. Molybdenum interconnects exhibit desirable electrical properties, even at the sub-10 nm scale. Yet, because molybdenum is a high hardness metal, molybdenum interconnect layers remain difficult to pattern during semiconductor device fabrication.

[0004] Accordingly, what is needed in the art are improved methods for patterning molybdenum layers.

SUMMARY

[0005] In one embodiment, a method of patterning a molybdenum interconnect layer is provided. The method includes forming a molybdenum layer on a substrate. A masking layer is then formed over the molybdenum layer and patterned to expose areas of the molybdenum layer to an ambient. The exposed areas of the molybdenum are modified with oxygen to form molybdenum oxide portions of the molybdenum interconnect layer. After modification, the molybdenum oxide portions of the molybdenum interconnect layer are removed from the substrate via an etching process.

[0006] In one embodiment, a method of forming a metal interconnect layer on a patterned substrate is provided. The method includes forming a molybdenum layer on the patterned substrate. A masking layer is formed on the molybdenum layer, the masking layer patterned to expose undesired areas of the molybdenum layer to an ambient. The patterned substrate is then exposed to a neutral particle beam to remove the undesired areas of the molybdenum layer.

[0007] In one embodiment, a method of patterning a metal interconnect layer on a substrate is provided. The method includes forming a molybdenum interconnect layer on the substrate. A mask is formed on the molybdenum layer and patterned to expose areas of the molybdenum interconnect layer. The substrate is then placed into a substrate processing region of a substrate processing chamber and exposed to gas-phase H_2O at a partial pressure within a range of about 20 bar to about 55 bar and a temperature within a range of about 250°C to about 550°C to remove the exposed areas of the molybdenum interconnect later.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only exemplary embodiments and are therefore not to be considered limiting of its scope, and may admit to other equally effective embodiments.

[0009] Figure 1 illustrates a flow diagram of a method for patterning a molybdenum interconnect layer of a device, such as a semiconductor device, according to one embodiment of the present disclosure.

[0010] Figure 2A illustrates a schematic cross-sectional view of a portion of a semiconductor device including a molybdenum layer before portions of one or more layers on the substrate are removed, according to one embodiment of the present disclosure.

[0011] Figure 2B illustrates a schematic cross-sectional view of a portion of a semiconductor device including a molybdenum layer after portions of one or more layers on the substrate have been modified, according to one embodiment of the present disclosure.

[0012] Figure 2C illustrates a schematic cross-sectional view of a portion of a semiconductor device including a molybdenum layer after portions of one or more layers on the substrate have been modified, according to one embodiment of the present disclosure.

[0013] Figure 2D illustrates a schematic cross-sectional view of a portion of a semiconductor device including a molybdenum layer after portions of one or more layers on the substrate have been removed, according to one embodiment of the present disclosure.

[0014] Figure 3 illustrates a flow diagram of a method for patterning a molybdenum interconnect layer of a device, such as a semiconductor device, according to one embodiment of the present disclosure.

[0015] Figure 4A illustrates a schematic cross-sectional view of a portion of a semiconductor device including a molybdenum layer before portions of one or more layers on the substrate have been removed, according to one embodiment of the present disclosure.

[0016] Figure 4B illustrates a schematic cross-sectional view of a portion of a semiconductor device including a molybdenum layer after portions of one or more

layers on the substrate have been removed, according to one embodiment of the present disclosure.

[0017] Figure 4C illustrates a schematic cross-sectional view of a portion of a semiconductor device including a molybdenum layer after further portions of one or more layers on the substrate have been removed, according to one embodiment of the present disclosure.

[0018] Figure 5 illustrates a flow diagram of a method for patterning a molybdenum interconnect layer of a device, such as a semiconductor device, according to one embodiment of the present disclosure.

[0019] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. It is contemplated that elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0020] The present disclosure provides methods for patterning a metal layer of a device (e.g., a semiconductor device) to form features in the interconnect layer as part of a process for manufacturing an interconnect structure of the device. The disclosed methods describe processes for patterning a molybdenum layer with improved selectivity. For example, the disclosure provides methods for modifying and removing areas of the molybdenum layer by annealing or etching without damaging other device structures or materials.

[0021] Figure 1 is a flow diagram of a method 100 for patterning a molybdenum layer of a device, such as a semiconductor device, according to one embodiment. In some embodiments, the molybdenum layer can be disposed directly on a substrate surface. In some embodiments, the molybdenum layer can be disposed on another metal layer, such as a barrier metal layer. In other embodiments, the molybdenum layer can be disposed on a dielectric layer, such as a silicon dioxide layer. The patterning of the molybdenum layer can be used for manufacturing an interconnect structure of the device. The patterning method 100 can be performed in a process chamber, such as a plasma process chamber or other suitable process

chamber. The following describes the method 100 of Figure 1 in conjunction with views shown in Figures 2A-2C, which show the device that includes the molybdenum layer at different stages of the method 100. Furthermore, although the method 100 is described below with reference to the molybdenum layer being utilized to form an interconnect structure, the method 100 can also be advantageously used with other metal containing layers and in other semiconductor device manufacturing applications.

[0022] At operation 102, a semiconductor device 200 (see Figure 2A) including a molybdenum layer 202 is positioned in a plasma process chamber, for example, an etching process chamber (not shown). The semiconductor device 200 can include one or more semiconductor devices that are in the process of being manufactured or in various stages of fabrication. Figure 2A is a schematic cross-sectional view of a portion of the semiconductor device 200 that includes the molybdenum layer 202 before portions of one or more layers disposed on a substrate 201 are removed, according to one embodiment. The view in Figure 2A shows the semiconductor device 200 before an initial patterning process (e.g., an oxidation process) is performed to modify portions of the molybdenum layer 202.

[0023] The semiconductor device 200 includes the substrate 201 The substrate 201 can be formed of any suitable material such as silicon, crystalline silicon, silicon oxide, strained silicon, silicon germanium, doped or undoped polysilicon, silicon on insulator (SOI), carbon doped silicon oxide, silicon nitride, doped silicon, germanium, gallium arsenide, glass, or sapphire, among other materials. In some embodiments, the substrate 201 is a 200 mm, 300 mm, 450 mm, or other diameter circular substrate. In other embodiments, the substrate 201 is a rectangular substrate or a square substrate. In an embodiment in which a SOI is used for the substrate 201, the substrate 201 can further include a buried dielectric layer disposed on a silicon crystalline substrate.

[0024] The molybdenum layer 202 is disposed on the substrate 201. In one embodiment, the molybdenum layer 202 is disposed directly on and in contact with the substrate 201. In other embodiments, the molybdenum layer 202 can be disposed on an intermediate layer (not shown), such as a dielectric layer. In these

embodiments, the intermediate layer is disposed directly on and in contact with the substrate 201, and the molybdenum layer 202 is disposed on the intermediate layer. The molybdenum layer 202 is used as an interconnect layer to connect multiple elements or devices of an integrated circuit.

[0025] The semiconductor device 200 further includes a masking layer 203 during one or more stages of fabrication. The masking layer 203 can be formed directly on the molybdenum layer 202 or on an intermediate layer (not shown), such as a dielectric layer. In some embodiments, the masking layer is formed of a material that is unreactive with wet etching solutions. In some embodiments, the masking layer is formed of a low hardness material. In other embodiments, the masking layer 203 is a hard mask, such as a carbon hard mask. Alternatively or in addition to the carbon hard mask, the masking layer 203 can be formed of other high hardness materials. Examples of high hardness materials include, but are not limited to, tungsten carbide (WC), tungsten boron carbide (WBC), tungsten nitride (WN), silicon boride (SiB_x) boron carbide (BC), amorphous carbon, boron nitride (BN), boron carbon nitride (BCN), or another similar material. The masking layer 203 materials described above can comprise compounds (e.g., a chemical compound of equal parts tungsten and carbon, a stoichiometric compound, etc.) or a doped material (e.g., a tungsten layer containing a small percentage of carbon). In some embodiments, which may be combined with other embodiments described herein, the masking layer 203 is a photoresist formed of light sensitive materials, such as naphtoquinone diazide (NQD) or other suitable photoreactive materials. In other embodiments,

[0026] In some embodiments, the substrate 201 is a thermally oxidized substrate. In embodiments including a thermally oxidized substrate, the molybdenum layer 202 may be formed directly on the substrate 201. The thermally oxidized substrate includes oxygen at the surface contacting the molybdenum layer 202. When portions of the molybdenum layer 202 are removed to expose the thermally oxidized substrate as described below, the oxygen from the thermally oxidized substrate is used to form a passivation layer (not shown) on an exposed surface of the semiconductor device 200. The passivation layer stops or substantially reduces further etching when the etching process breaks through the molybdenum layer 202.

For example, the oxygen from the thermally oxidized substrate can combine with silicon atoms from a silicon-containing gas used to etch the molybdenum layer 202 to form a passivation layer of silicon oxide on exposed portions of the semiconductor device 200 to stop the etching process. Although the passivation layer is described here as being formed in part by oxygen from a thermally oxidized substrate, the oxygen can come from a layer including oxygen that directly underlies the molybdenum layer 202.

[0027] In some embodiments, the semiconductor device 200 can further include a barrier layer (not shown) and a low-k insulating dielectric layer (not shown). The low-k insulating dielectric layer is disposed over the substrate 201 between the molybdenum layer 202 and the substrate 201. The barrier layer can be disposed over the low-k insulating dielectric layer between the molybdenum layer 202 and the low-k insulating dielectric layer. The barrier layer can be fabricated from tantalum nitride (TaN), titanium nitride (TiN), aluminum nitride (AlN), tantalum silicon nitride (TaSiN), titanium silicon nitride (TiSiN), silicon nitride (SiN), silicon oxynitride (SiON), silicon carbide (SiC), (silicon isocyanide) SiNC, silicon oxycarbide (SiOC), or other suitable materials. Furthermore, the low-k insulating dielectric layer can be formed from SiO containing materials, SiN containing materials, SiOC containing materials, SiC containing materials, carbon-based materials, or other suitable materials.

[0028] At operation 104, portions of the masking layer 203 are removed to form exposed portions 222 of the molybdenum layer 202 as shown in Figure 2B. Figure 2B is a schematic cross-sectional view of a portion of the semiconductor device 200 including the molybdenum layer 202 after portions of the masking layer 203 disposed on the molybdenum layer 202 are removed, according to one embodiment. The removal of these portions of the masking layer 203 forms voids 205 in the masking layer 203, shown in Figure 2B as trenches, with the bottom of the voids 205 formed (i.e. bordered or partially defined) by the exposed portions 222 of the molybdenum layer 202. Thus, the removal of portions of the masking layer 203 exposes portions of the molybdenum layer 202.

[0029] Although the use of the materials described above for the masking layer 203 (i.e., the high hardness materials, such as WC) can improve the process of

selectively etching features above the molybdenum layer 202, eventually portions or all of the masking layer 203 are removed to form features on the device, such as transistor structures.

[0030] At operation 106, the exposed portions 222 of the molybdenum layer 202 are modified. In one embodiment, the exposed portions 222 are oxidized to form molybdenum oxide portions 223. Figure 2C is a schematic cross-sectional view of a portion of the semiconductor device 200 including the molybdenum layer 202 after exposed portions 222 of the molybdenum layer 202 are oxidized, according to one embodiment.

[0031] Exposed portions 222 may be oxidized by various methods, including but not limited to, direct oxygen ion implantation or oxygen plasma doping. For example, implanted oxygen ions may be bombarded in a substantially vertical path against the exposed portions 222 of the molybdenum layer 202 to penetrate the exposed portions 222. The implanted ions can penetrate the exposed portions 222 to various depths depending on the power and bias utilized to energize the oxygen ions. For example, the exposed portions 222 may be implanted with oxygen ions energized to an accelerating voltage of about 5 KeV to about 30 KeV, such as about 10 KeV to about 20 KeV, and at a dose ranging from about 0.5E16 ions/cm2 to about 5E17 ions/cm2, such as about 1E16 ions/cm2 to about 1E17 ions/cm2. For example, the exposed portions 222 may be implanted with oxygen ions energized at 10 KeV and dosed at 1E17 ions/cm2.

[0032] The ion implantation may be performed by beamline or plasma implantation tools. A suitable, commercially available processing platform which may be advantageously employed in accordance with the embodiments described herein is the VIISTA® PLAD™ platform available from Applied Materials, Inc., Santa Clara, CA. It is contemplated that other suitably configured implant technology platforms from other manufacturers may also be used in accordance with the embodiments herein.

[0033] In some embodiments, after oxygen ion implantation of the exposed portions 222, the semiconductor device 200 is annealed to form a polycrystalline structure of the molybdenum oxide portions 223. The semiconductor device 200 is

annealed by various methods, such as furnace annealing or rapid thermal annealing, for example, lamp based or laser annealing. In one embodiment, the device structure 200 is annealed at a temperature between about 200 ºC and about 600 ºC, a pressure between about 0.5 bar to about 75 bar water vapor, and a duration between about 15 minutes to about 2 hours. In some examples, the device structure 200 is annealed at a temperature between about 250 ºC and about 550 ºC, such as between about 300 ºC and about 500 ºC, such as between about 350 ºC and about 450 ºC. In some examples, the device structure 200 is annealed at a pressure between about 25 bar and about 55 bar, such as between about 30 bar and about 50 bar, such as between about 35 bar and about 45 bar. In some examples, the device structure 200 is annealed for a duration between about 30 minutes and about 1.5 hours, such as between 45 minutes and 75 minutes. In one example, the device structure 200 is annealed in conditions of 325 ºC and 55 bar for about 60 minutes.

[0034] In some embodiments, the thermal anneal is performed at high pressure and in the presence of a processing gas, such as hydrogen, deuterium, fluorine, chlorine, ammonium, or other suitable gases for high pressure gas annealing. Annealing the semiconductor device 200 at high pressure levels facilitates the formation the polycrystalline structure of the molybdenum oxide portions 223 even at low temperatures, for example, less than 350 ºC.

[0035] At operation 108, the molybdenum oxide portions 223 are removed from the semiconductor device 200 to form a patterned molybdenum layer 204. Figure 2D is a schematic cross-sectional view of a portion of the substrate 201 including the patterned molybdenum layer 204 after the molybdenum oxide portions 223 are removed. The removal of the molybdenum oxide portions 223 forms the voids 205 in the patterned molybdenum layer 204, shown in Figure 2D as trenches with the bottom of the voids 205 formed by a top surface 207 of the substrate 201.

[0036] Molybdenum oxide portions 223 may be removed from the substrate 201 by any suitable process of etching which is selective for molybdenum oxide, including wet etching or dry etching processes. For example, the molybdenum oxide portions 223 are removed from the substrate 201 by wet etching with an

ammonia solution. The ammonia solution is selective for the oxidized portions 223. As such, the oxidized portions 223 are removed while the patterned molybdenum layer 204, which is non-oxidized, is not removed by the ammonia solution. The ammonia solution may include ammonia hydroxide at a concentration of about 26% w/w to about 30% w/w, such as about 28% w/w. The semiconductor device 200 may be exposed to the ammonia solution for etching a desired depth of the molybdenum oxide portions 223, such as for a duration of between about 2 minutes and about 10 minutes.

[0037] In another example which may be combined with examples and embodiments described herein, the molybdenum oxide portions 223 are removed from the semiconductor device 200 by wet etching with a pH 10 buffer solution. The pH 10 buffer solution includes a sodium compound such as sodium tetraborate or sodium hydroxide. The semiconductor device 200 may be exposed to the pH 10 buffer solution for etching a desired depth of the molybdenum oxide portions 223, such as for a duration between about 2 minutes and about 10 minutes. The use of either an ammonia solution or a pH 10 buffer solution for selectively etching the molybdenum oxide portions 223 etches the molybdenum oxide portions 223 without harming the non-oxidized and patterned molybdenum layer 204 or other material layers and device structures of the semiconductor device 200.

[0038] Figure 3 is a flow diagram of a method 300 for patterning a molybdenum layer of a device, such as a semiconductor device, by neutral atom beam etching, according to one embodiment. Similar to the embodiment depicted in Figures 1 and 2, the molybdenum layer 202 can be disposed directly on the substrate 201, or on another layer, such as a metal layer or a dielectric layer. The patterning of the molybdenum layer 202 according to the current embodiment can be used for manufacturing an interconnect structure of the semiconductor device 200. The patterning method 300 is performed in a process chamber, such as a plasma process chamber or a neutral atom beam etching apparatus. The following describes the method 300 of Figure 3 in conjunction with views shown in Figures 4A-4C, which show the semiconductor device 200 of Figure 2 that includes the molybdenum layer 202 at different stages of the method 300. Furthermore, although the method 300 is described below with reference to the molybdenum layer 202

being utilized to form an interconnect structure, the method 300 can also be used to advantage with materials other than molybdenum and in other semiconductor device manufacturing applications.

[0039] At operation 302, the semiconductor device 200 (see Figure 4A) including the molybdenum layer 202 is positioned in a plasma process chamber, for example an etching process chamber (not shown). The semiconductor device 200 can include one or more semiconductor devices that are in the process of being manufactured or in various stages of fabrication. Figure 4A is a schematic cross-sectional view of a portion of the semiconductor device 200 that includes the molybdenum layer 202 before portions of one or more layers disposed on the substrate 201 are removed, according to one embodiment. The view in Figure 4A shows the semiconductor device 200 before a patterning process (e.g., a neutral beam etch) is performed to modify portions of the molybdenum layer 202.

[0040] At operation 304, portions of the masking layer 203 are removed to form exposed portions 222 of the molybdenum layer 202 as shown in Figure 4B. Figure 4B is a schematic cross-sectional view of a portion of the semiconductor device 200 including the molybdenum layer 202 after portions of the masking layer 203 disposed on the molybdenum layer 202 are removed, according to one embodiment. The removal of these portions of the masking layer 203 forms voids 205 in the masking layer 203, shown in Figure 4B as trenches with the bottom of the voids 205 formed (i.e. bordered or partially defined) by the exposed portions 222 of the molybdenum layer 202. Thus, the removal of portions of the masking layer 203 exposes portions of the molybdenum layer 202.

[0041] At operation 306, the exposed portions of the molybdenum layer 202 are removed from the semiconductor device 200 to form a patterned molybdenum layer 204. Figure 4C is a schematic cross-sectional view of a portion of the semiconductor device 200 including the patterned molybdenum layer 204 after exposed portions 222 of the molybdenum layer 202 are removed. The removal of the exposed portions 222 forms voids 205 in the patterned molybdenum layer 204, shown in figure 4C as trenches with the bottom of the voids 205 formed by a top surface of the substrate 201.

[0042] In the embodiment depicted by Figures 3 and 4, the exposed portions 222 of the molybdenum layer 202 may be removed from the semiconductor device 200 by an accelerated atom beam process. A suitable, commercially available processing platform which may be advantageously employed in accordance with the embodiments described herein is the NanoAccel™ platform available from Exogenesis Corp., Billerica, Massachusetts. It is contemplated that other suitably configured accelerated atom beam platforms from other manufacturers may also be used in accordance with the embodiments herein.

[0043] In one example, the exposed portions 222 of the molybdenum layer 202 may be removed by a gas cluster ion beam (GCIB) etch. During the GCIB etch of the molybdenum layer 202, a pressurized inert gas may be flowed, expanded, and accelerated toward the exposed portions 222 of the molybdenum layer 202 within a processing chamber, transferring energy to and causing removal of the outermost atoms of the exposed portions 222. In one embodiment, the gas cluster ion beam is formed of argon gas. In other embodiments, additional gases may be combined with an inert gas to form the gas cluster ion beam, including oxygen (O_2), nitrogen (N_2), methane (CH_4), and sulfur hexafluoride (SF_6).

[0044] The gas cluster ion beam may be directed in a substantially vertical path through the voids 205 in the masking layer 203 so as penetrate desired portions of the molybdenum layer 202 and form the patterned molybdenum layer 204. Thus, other device structures or material layers on the semiconductor device 200 are left undamaged during the gas cluster ion beam etch. The gas cluster ion beam may be accelerated to an accelerating voltage of 10 KeV to 40 KeV, such as 15 KeV to 35 KeV. For example, the gas cluster ion beam is accelerated to an accelerating voltage of 25 KeV. The semiconductor device 200 may be exposed to the gas cluster ion beam for any suitable dose time, such as between about 0 seconds and about 30 seconds, including between 2-20 seconds. For example, the semiconductor device 200 may be exposed to the gas cluster ion beam for a dose time of 6, 8, 10, 14, or 18 seconds.

[0045] In another example, which may be combined with the embodiments and examples described herein, an accelerated neutral atom beam (ANAB) etch is used

to remove the exposed portions 222 of the molybdenum layer 202 from the semiconductor device 200. Similar to GCIB etching, accelerated neutral atom beam etching utilizes a beam of accelerated gas cluster ions, but the gas cluster is dissociated and the charge is removed prior to impacting the surface of the exposed portions 222. The accelerated neutral atom beam is directed in a substantially vertical path through the voids 205 in the masking layer 203 so as to penetrate desired portions of the molybdenum layer 202. Further, each atom inside the neutral atom beam has relatively low energy, leading to limited surface modification of only a few atomic layers and thus, significantly reducing or eliminating etching damage to other materials and layers or the semiconductor device 200.

[0046] The accelerated neutral atom beam is accelerated to an accelerating voltage of 10 KeV to 40 KeV, such as 15 KeV to 35 KeV. For example, the accelerated neutral atom beam is accelerated to an accelerating voltage of 25 KeV. The semiconductor device 200 is exposed to the accelerated neutral atom beam for any suitable dose time such as between about 0 seconds and about 30 seconds, including between 2-20 seconds. For example, the semiconductor device 200 may be exposed to the accelerated neutral atom beam for a dose time of 6, 8, 10, 14, or 18 seconds. Inert gases, such as argon, may be used to form the accelerated neutral atom beam. In some embodiments, additional gases may be combined with the inert gas, including (O_2), nitrogen (N_2), methane (CH_4), and sulfur hexafluoride (SF_6). The ANAB etching may be performed at any suitable etching conditions.

[0047] Figure 5 is a flow diagram of a method 500 for patterning a molybdenum layer of a device, such as a semiconductor device, by high pressure water anneal according to one embodiment. Similar to the embodiments depicted in Figures 1-4, the molybdenum layer can be disposed directly on a substrate surface, or on another layer, such as a metal layer or a dielectric layer. The patterning of the molybdenum layer according to the current embodiment, which may be combined with other embodiments and examples described herein, can be used for manufacturing an interconnect structure of the device. The patterning method 500 is performed in a plasma process chamber, such as an etching process chamber or other suitable process apparatus. Although the method 500 is described below with reference to the molybdenum layer being utilized to form an interconnect structure,

the method 500 can also be used to advantage with materials other than molybdenum and in other semiconductor device manufacturing applications.

[0048] At operation 302, a semiconductor device including a molybdenum layer is positioned in a plasma process chamber, such as an etching process chamber (not shown). The semiconductor device can include one or more semiconductor devices that are in the process of being manufactured. The semiconductor device further includes a substrate, the molybdenum layer disposed over the substrate, and a masking layer, for example, similar to the substrate 201, the molybdenum layer 202, and the masking layer 203 described with regard to Figures 2 and 4. The semiconductor device can also include other material layers disposed on the substrate, such as a barrier layer or a low-k insulating layer.

[0049] At operation 504, portions of the masking layer are removed to form exposed portions of the molybdenum layer. The removal of these portions of the masking layer forms voids 205 in the masking layer, the bottom of the voids 205 formed by the exposed portions of the molybdenum layer. The removal of portions of the masking layer exposes portions of the molybdenum layer.

[0050] At operation 506, the semiconductor device is exposed to a high pressure water anneal (HPWA) process to remove the exposed portions of the molybdenum layer from the semiconductor device. Although method 500 describes a high pressure water anneal utilizing water vapor to anneal the semiconductor device, it is contemplated that other gases may be used to anneal the semiconductor device under high pressure. For example, the semiconductor device may be annealed at high pressure using hydrogen, deuterium, fluorine, chlorine, ammonium, or other suitable gases. In another example, the semiconductor device may be annealed using a combination of gases including hydrogen, deuterium, fluorine, chlorine, ammonium, and other suitable gases.

[0051] At operation 506, the processing chamber is pressurized by supplying water vapor from a pressure chamber to the processing chamber, followed by thermal annealing of the device and depressurization of the processing chamber by evacuation of the water vapor. The thermal annealing is performed at a temperature of between about 250 ºC and about 450 ºC, such as between about 300 ºC and

about 400 ºC. For example, the thermal annealing is performed at a temperature of between about 325 ºC and about 375 ºC. Further, the processing chamber is pressurized to a pressure of between about 10 bar and about 75 bar, such as between about 20 bar and about 60 bar. For example, the processing chamber is pressurized to a pressure of between about 30 bar and about 50 bar. The exposure of the device to high pressure water vapor annealing removes the exposed portions of the molybdenum layer, thus forming a patterned molybdenum layer without damaging other device structures or material layers.

[0052] Embodiments of the disclosure include methods for patterning a metal layer of a device to form features in the interconnect layer as part of a process for manufacturing an interconnect structure of the device. Particularly, the disclosed methods describe processes for patterning a molybdenum layer with improved selectivity. Increased selectivity in patterning molybdenum layers enables the formation of interconnect structures, as well as other metal layers, without the disadvantages associated with patterning high hardness materials, including large undercut and damage to other layers and structures stacked within a semiconductor device. Thus, methods provided herein make molybdenum, as well as other high hardness metals, more desirable and practicable materials for device structures such as interconnect structures.

[0053] While the foregoing is directed to implementations of the present disclosure, other and further implementations of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. A method of forming a metal interconnect layer, comprising:

forming a molybdenum layer on a substrate;

forming a masking layer over the molybdenum layer;

patterning the masking layer to expose portions of the molybdenum layer;

modifying the exposed portions of the molybdenum layer with oxygen to form molybdenum oxide portions of the molybdenum layer; and

removing the molybdenum oxide portions from the substrate.

2. The method of claim 1, wherein the exposed portions of the molybdenum layer are modified by oxygen plasma doping.

3. The method of claim 1, wherein the exposed portions of the molybdenum layer are modified by direct oxygen implantation.

4. The method of claim 1, wherein the molybdenum oxide portions of the molybdenum layer are removed by a dry etching process.

5. The method of claim 1, wherein the molybdenum oxide portions of the molybdenum layer are removed by a wet etching process.

6. The method of claim 5, wherein the molybdenum oxide portions of the molybdenum layer are wet etched by a pH 10 buffer solution.

7. The method of claim 5, wherein the molybdenum oxide portions of the molybdenum layer are wet etched by an ammonia solution.

8. The method of claim 1, further comprising: annealing the substrate prior to removing the molybdenum oxide portions of the molybdenum layer by etching.

9. The method of claim 8, wherein the annealing is performed at a temperature between about 250 ºC and about 550 ºC and a pressure between about 25 bar and about 55 bar.

10. A method of forming a metal interconnect layer on a patterned substrate, comprising:

forming a molybdenum layer on the patterned substrate;

forming a masking layer on the molybdenum layer, the masking layer patterned to expose portions of the molybdenum layer; and

exposing the patterned substrate to an accelerated atom beam to remove the exposed areas of the molybdenum layer.

11. The method of claim 10, wherein the accelerated atom beam is a gas cluster ion beam formed by ionizing and accelerating a gas cluster comprising argon.

12. The method of claim 11, wherein the gas cluster is accelerated at a voltage potential of about 20 KeV to 30 KeV.

13. The method of claim 11, wherein the gas cluster ion beam further comprises one or more additional gases selected from the group consisting of oxygen, nitrogen, sulfur hexafluoride, and methane.

14. The method of claim 10, wherein the accelerated atom beam is an accelerated neutral atom beam.

15. A method of patterning a metal interconnect layer on a substrate, the method comprising:

forming a molybdenum interconnect layer on the substrate;

forming a masking layer on the molybdenum interconnect layer;

patterning the masking layer to expose portions of the molybdenum interconnect layer; and

exposing the substrate to gas-phase H_2O at a partial pressure of between about 20 bar and about 55 bar and a temperature of between about 250 ºC and about 550 ºC to remove the exposed portions of the molybdenum interconnect layer.

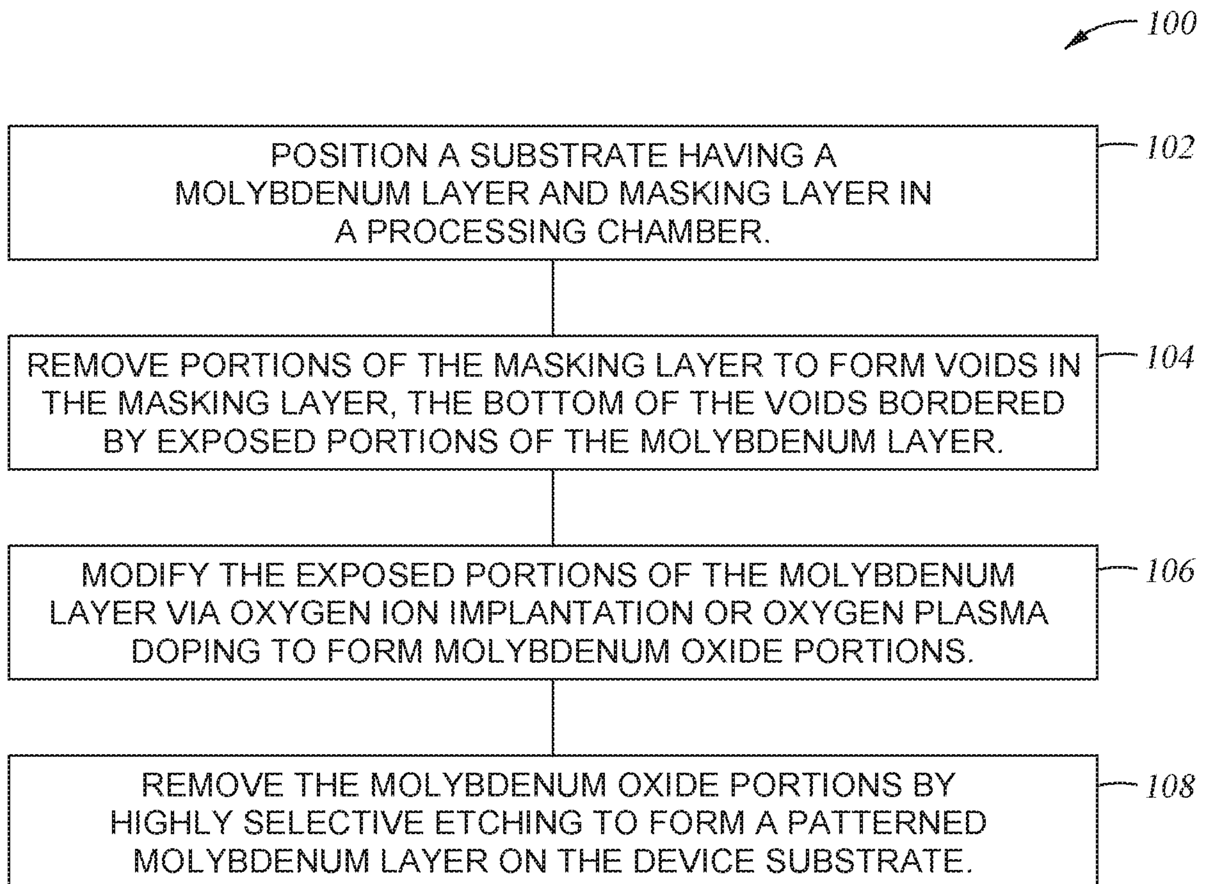

Fig. 1

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Fig. 2A

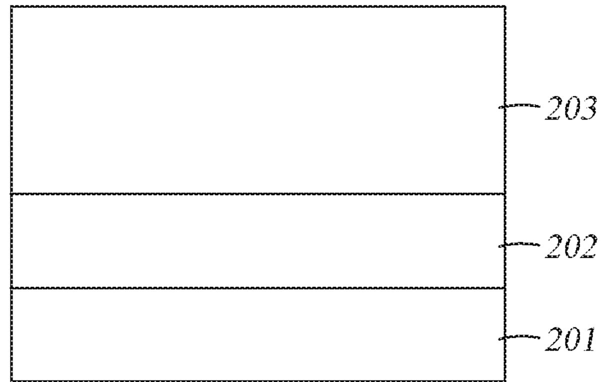

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Fig. 2B

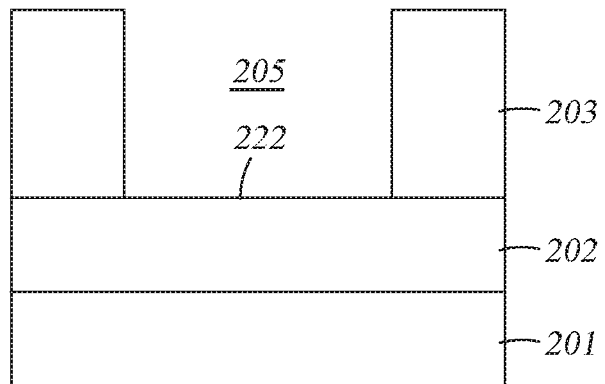

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Fig. 2C

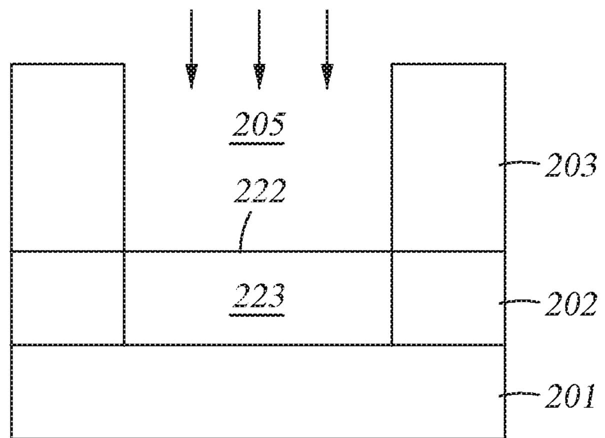

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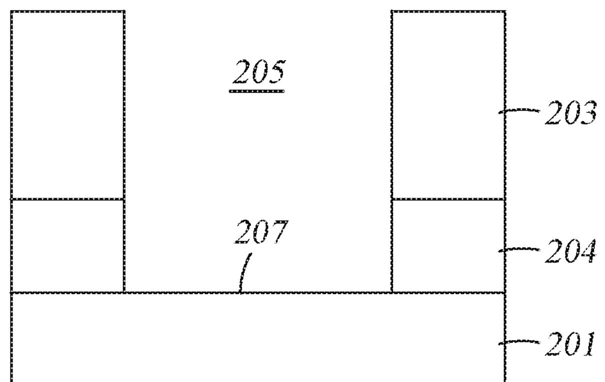
Fig. 2D



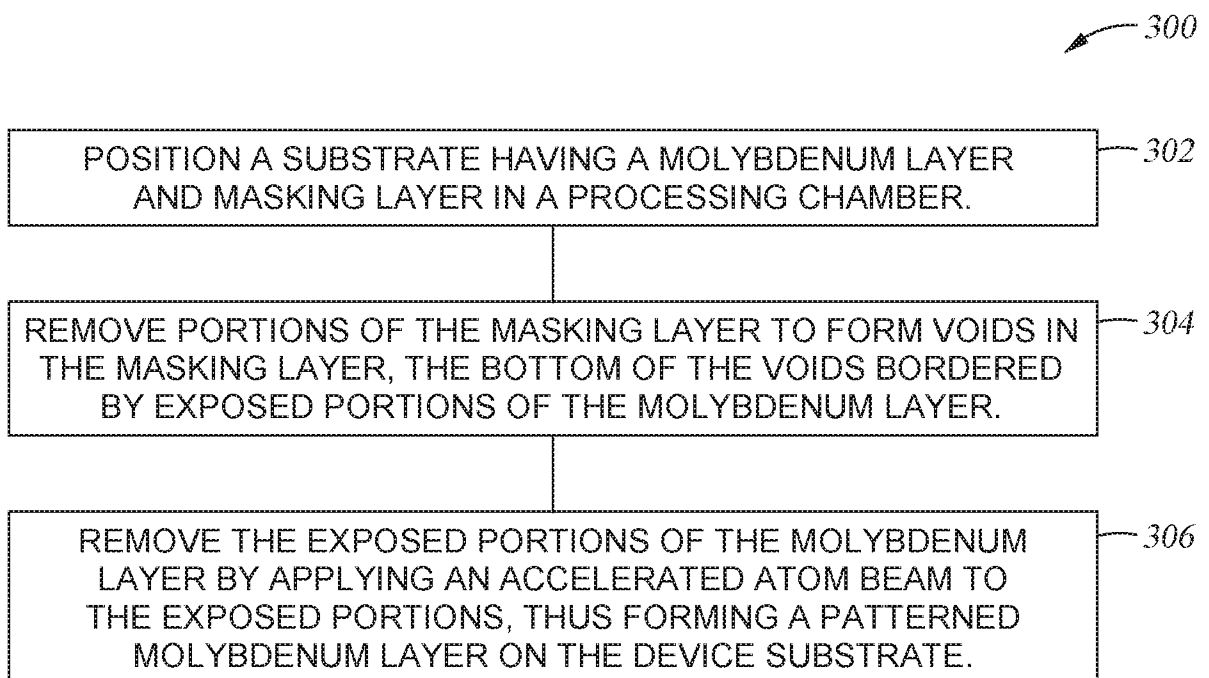


Fig. 3

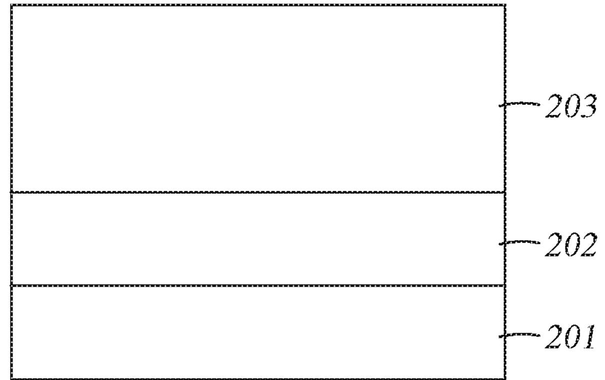


Fig. 4A

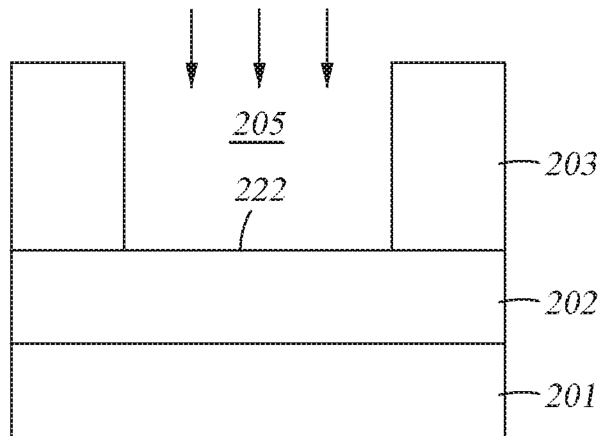


Fig. 4B

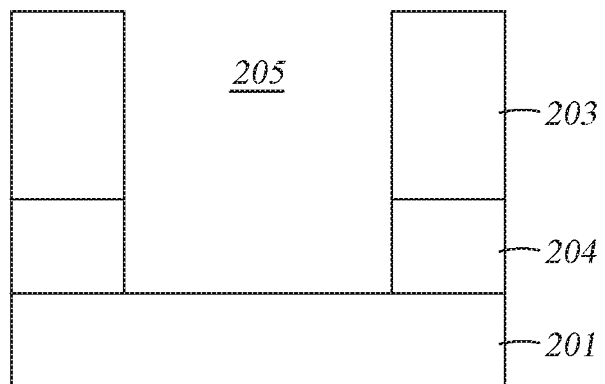


Fig. 4C

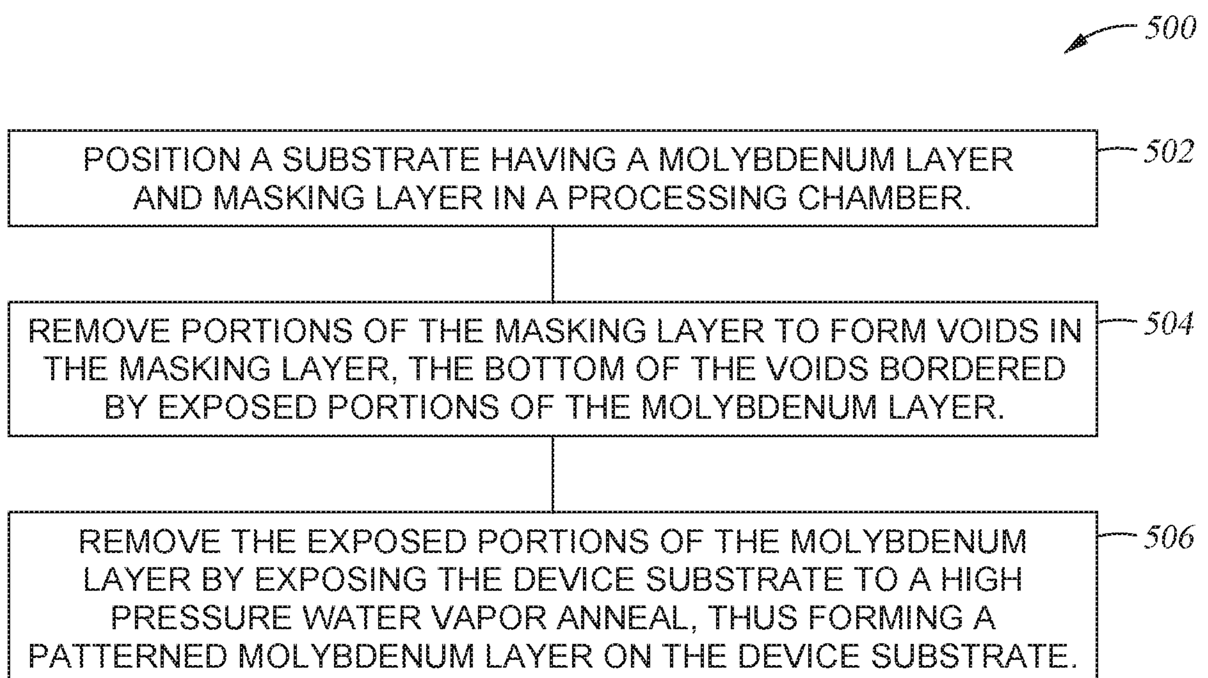


Fig. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2019/053778

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/768(2006.01)i, H01L 21/02(2006.01)i, H01L 21/3065(2006.01)i, H01L 21/306(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/768; B44C 1/22; C23F 1/02; G06F 3/038; H01J 9/02; H01L 21/00; H01L 21/033; H01L 21/306; H01L 21/02; H01L 21/3065

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: molybdenum, remove, interconnect, high pressure

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	US 2014-0273490 A1 (APPLIED MATERIALS, INC.) 18 September 2014 See paragraphs [0054]-[0062] and figures 4-5B.	1-8 9-15
Y	US 5972235 A (KRISTIN BRIGHAM et al.) 26 October 1999 See claims 1, 13.	1-8
Y	US 5350484 A (DONALD S. GARDNER et al.) 27 September 1994 See column 5, lines 17-54, column 8, lines 13-18 and figures 3A-3D.	8
A	US 2013-0059444 A1 (YAN SHAO et al.) 07 March 2013 See paragraphs [0040]-[0076], [0112]-[0113] and figures 5, 8.	1-15
A	US 2013-0335383 A1 (TERUO SASAGAWA) 19 December 2013 See claim 1 and figures 6A-7.	1-15

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 January 2020 (17.01.2020)	**17 January 2020 (17.01.2020)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2019/053778

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		KR 10-0273921 B1	15/12/2000
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US 2013-0335383 A1	19/12/2013	None	