Nov. 12, 1963 W. E. INGHAM ETAL 3,110,802

ELECTRICAL FUNCTION GENERATORS

Filed July 31, 1958 5 Sheets-Sheet 1

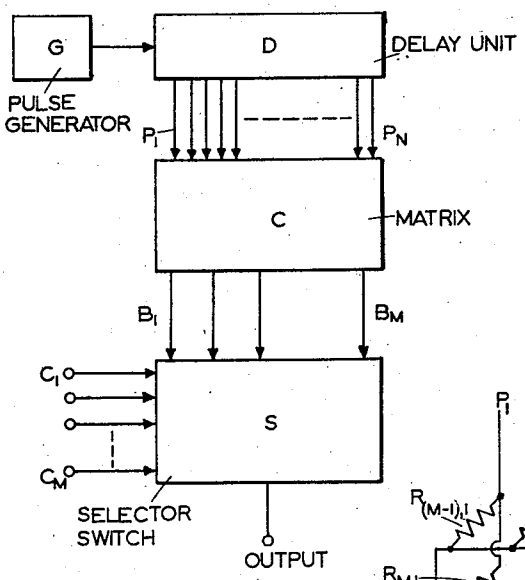

FIG.1

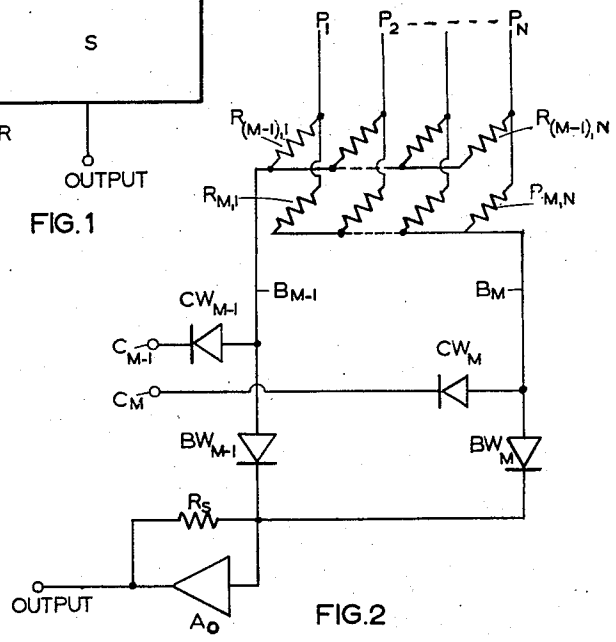

FIG.2

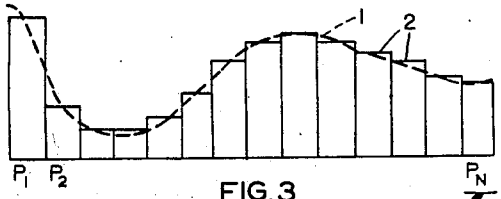

FIG.3

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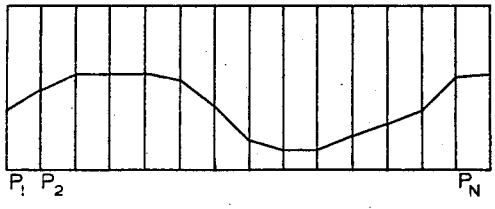

FIG.4

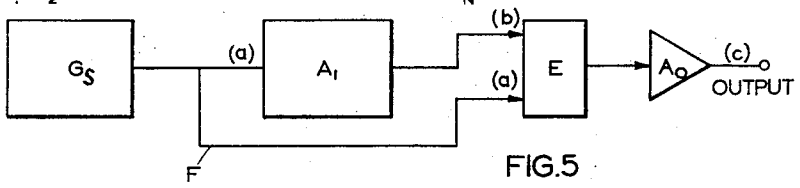

FIG.5

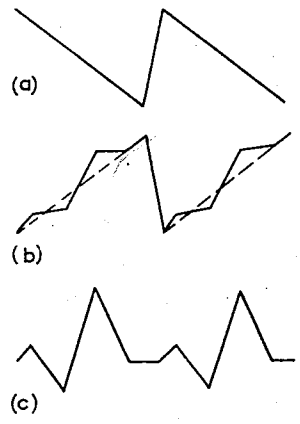

FIG.6

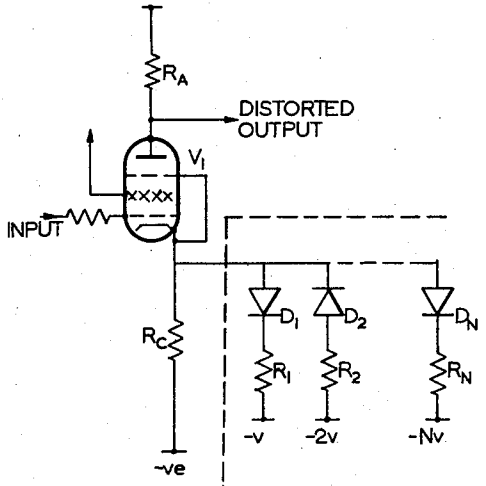

FIG. 7

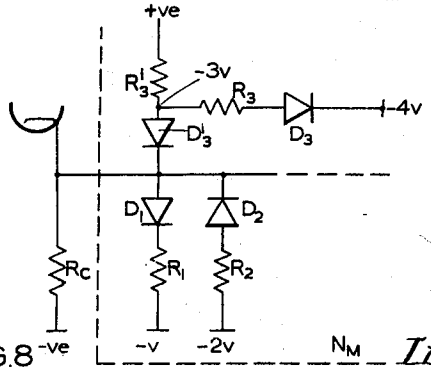

FIG.8

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ELECTRICAL FUNCTION GENERATORS

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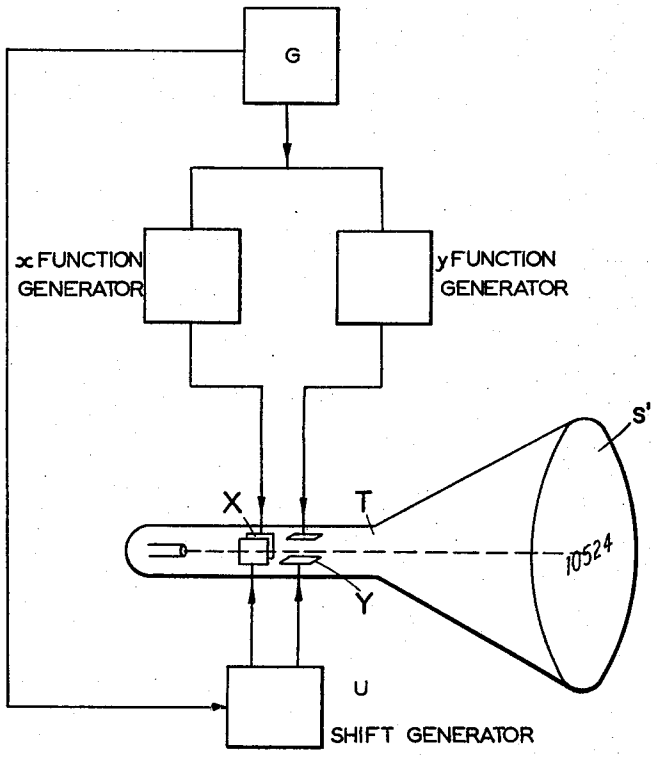

FIG. 9

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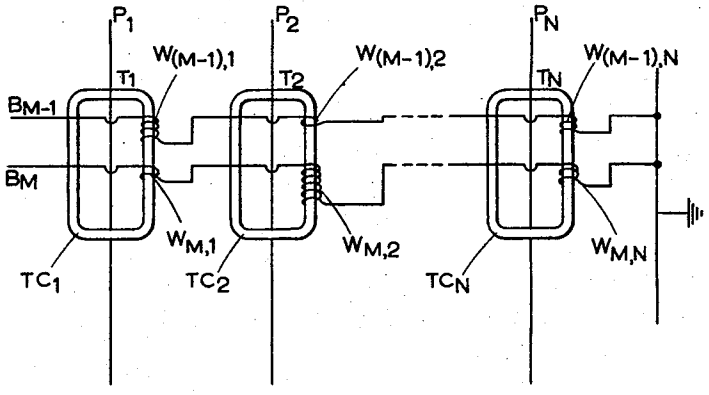

FIG. 10

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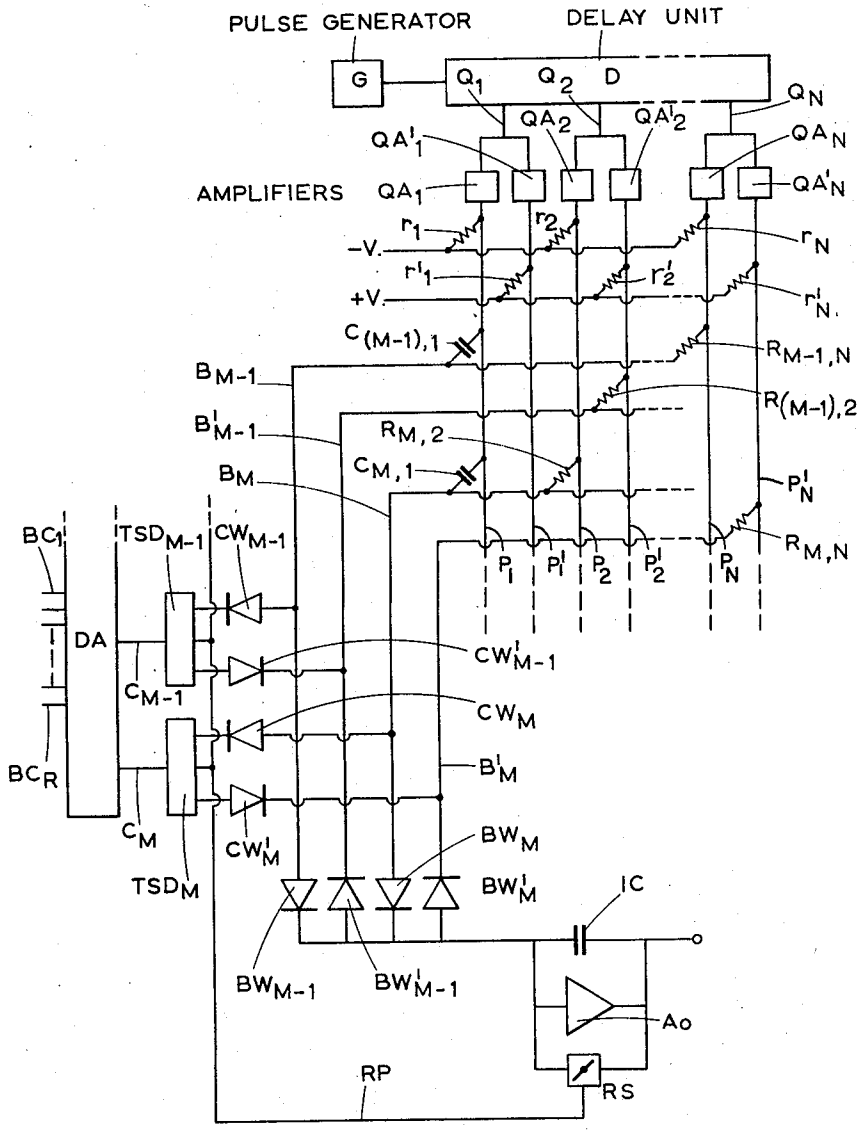

FIG. 11

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United States Patent Office 3,110,802 Patented Nov. 12, 1963

3,110,802

ELECTRICAL FUNCTION GENERATORS

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Filed July 31, 1958, Ser. No. 752,295
Claims priority, application Great Britain Aug. 3, 1957
1 Claim. (Cl. 235—197)

This invention relates to electrical function generators especially for character writing devices.

It is sometimes required to write characters electronically, usually by means of a moving beam of electrons in a cathode ray tube having a luminescent screen. The characters may be Roman letters and Arabic numerals, or other desired symbols. Such writing of characters may be used for example in the labelling of "echoes" on a radar type of display. It is also useful for presenting data by which a controller can be kept informed of the state of a process or situation. Character writing may also be required of an output device of an electrical computer, in which case advantage can be taken of the high speed of electronic writing in order to deal with information rates in excess of the capabilities of mechanical printers. In this application the character-display can be photographed or used with a xerographic printer or other dry printing means, to obtain a permanent record. In general characters can be written by generating two electrical waveforms conforming, for example, to functions representing the varations, with respect to a common parameter, of the cartesian co-ordinates of the writing spot. It has been proposed to produce such waveforms by synthesis using standard waveforms such as sine and cosine functions, but an unduly large amount of equipment is required, particularly when large numbers of characters are involved.

The object of the present invention is to provide an electrical function generator especially though not exclusively applicable to character writing devices, with a view to reducing disadvantages such as indicated and at the same time avoiding the use of cathode ray tubes or photo electrically sensitive devices in the function generation process.

According to the present invention there is provided a function generator comprising an output circuit, a plurality of groups of impedances, a source of electrical energy for said impedances, said impedances having selected magnitudes, in which each group has a common connection to which all the impedances of the group are connected, a plurality of gating means, one gating means connected from each common connection to said output circuit, means for operating the gating means connected to the common connection of a selected group, a group of gating means, connected from said energy source to the individual impedances within the selected group, and means for successively operating the gating means of said group of gating means to cause energy from said source to reach said output circuit via successive impedances in the selected group to produce an output signal conforming to the function corresponding to the selected group, the energy reaching the output circuit being responsive to the magnitude of the impedance connected to the energy source by the gating means of said group of gating means at any particular time so as to determine the respective section of the function.

Two generators, according to the invention, may be used to generate the two functions corresponding, for example, to the variations of the x and y co-ordinates of a character, so that when applied as deflecting potentials to a cathode ray tube, the beam thereof will describe the required character on the fluorescent screen.

In order that the present invention may be clearly understood and readily carried into effect, the invention will be more fully described with reference to the accompanying drawings, in which:

FIGURE 1 illustrates in block form one example of a function generator according to the present invention,

FIGURE 2 illustrates in greater detail the construction of parts of the apparatus shown in FIGURE 1,

FIGURE 3 is a diagram used in explaining FIGURE 1,

FIGURE 4 is another explanatory diagram,

FIGURE 5 illustrates in block form another example of the present invention, which operates according to the principle illustrated in FIGURE 4,

FIGURE 6 comprises waveforms which are set up at different parts of the apparatus illustrated by FIGURE 5,

FIGURES 7 and 8 show in greater detail, alternative constructions for part of the apparatus shown in FIGURE 5,

FIGURE 9 illustrates a character writing device embodying function generators such as illustrated in FIGURE 1 or FIGURE 5,

FIGURE 10 illustrates another example of a function generator according to the present invention utilising transformers, and

FIGURE 11 illustrates yet another example of a function generator according to the present invention in which the function is generated by interpolation.

The example of the invention illustrated in FIGURE 1 produces a quantized approximation to the desired function by switching the output voltage of the generator successively from one discrete level to another, the accuracy of the approximation depending on the number of switching operations. By way of example the broken line 1 in FIGURE 3 shows a desired function and the stepped waveform 2 shows the approximation which can be obtained by dividing the time taken to generate the function into fourteen intervals. The intervals are denoted by the references p_1, p_2 . . . p_N, so that N is fourteen in the example stated.

Referring to FIGURE 1, the function generator comprises a pulse generator G which generates a series of pulses, one for each function to be generated, the pulse being applied to a delay unit D. The delay unit may consist of a thermionic or transistor valve chain circuit of the construction described in United States Patent Number 2,586,409, a ring counter such as described in copending U.S. patent application Serial Number 418,195, U.S. Patent Number 2,906,870, or United States Patent Number 2,802,104, or a passive delay line. The delay unit has output leads corresponding in number to the numbers of steps in the function generated, and these outputs are denoted in the drawings by the references P_1 to P_N. As a pulse from the generator G travels along the delay unit D, the leads P_1 to P_N are energised in turn to apply a series of pulses to a matrix C. Only one pulse is allowed to be present in the delay unit at any time.

Assume that the generator has a capacity of M functions, then the matrix C comprising M rows of resistors R, and M conductors B_1 to B_M hereinafter called function conductors. In FIGURE 2, two rows of resistors and two function conductors are represented, namely for the functions $M-1$ and M, but the arrangement is general to all functions. There are N resistors in each row, one corresponding to each output lead P from the delay unit D. The resistors of row $M-1$ have one end attached to the function conductor B_{M-1} and have their other end connected respectively to the leads P_1, P_2 . . . P_N. Assume that the function shown in FIGURE 3 is the function $M-1$; the resistances of $R_{(M-1),\,1}$, $R_{(M-1),\,2}$ are then inversely proportional to the heights of the corresponding steps in that function. The resistors $R_{M,1}$, $R_{M,2}$ . . . are likewise inversely proportional to the successive steps of the function M, and so on for the other functions.

The function conductors B_1, B_2 . . . B_M lead from the matrix C to a selector switch S which has M input leads C_1 to C_M whereby a desired function can be selected, the selector input leads C being connected in the switch respectively to the function conductors B_1, B_2 . . . by way of unilaterally conductive gates in the form, say, of crystal diodes. Two of these diodes shown in FIGURE 2 are denoted by the references CW_{M-1} and CW_M. The selector switch S also includes a high gain amplifier A_0 having a negative feedback resistor R_S and the input terminal of the amplifier is connected as shown in FIGURE 2, to all the function conductors B by way of unilaterally conductive devices, also crystal diodes, say, the two such diodes shown in FIGURE 2 bearing the references BW_{M-1}, and BW_M.

In the quiescent state of the generator illustrated, the standing potentials on the output leads P_1 to P_N and in the selector leads C_1 to C_M are such that the currents are negligible in all the matrix resistors R. The selector leads C_1 to C_M are biassed below the cut-off potential of the amplifier A_0, so that the diodes BW are switched off. Assume now that the function $M-1$ has been selected. A pulse from the generator G is propagated along the delay unit and simultaneously a positive potential is applied to the selector input lead C_{M-1} lasting for the time taken by the pulse to traverse the delay unit and having sufficient amplitude to switch off the diode CW_{M-1}. When the pulse in the delay unit energises one of the leads say P_N, the potential in the lead P_N rises for the period p_N and current flows in all the resistors connected to that lead, these currents being carried by the diodes CW, except for that in the resistor $R_{(M-1),\ N}$ which is connected to the function conductor B_{M-1}, this last mentioned current being carried by the diode BW_{M-1}. That resistor together with the resistor R_S and the amplifier A_0 then act in well known see-saw manner so as to cause the potential at the output of the amplifier to assume a value determined by the current flowing in the "energised" resistor $R_{(M-1),\ N}$. Therefore during the transit of the pulse along the delay unit D, the potential at the output of the amplifier A_0 changes in a series of discrete steps determined respectively by the magnitude of the successive resistors in the row $M-1$ and thereby generates a stepped approximation to the desired function. The steps in the output can be removed by suitable filtering if desired.

The generator illustrated in FIGURE 2 can also be arranged so that the standing currents in the matrix resistors R are substantial, and that the currents in resistors connected to an energised lead fall to zero.

In a modified form of the invention illustrated in FIGURES 2 and 3, each column of resistors R is replaced by a magnetic cell transformer. This is illustrated in FIGURE 10 in which the transformers are denoted by the references T_1, T_2, . . . T_N and have cores denoted by the references TC_1, TC_2, . . . TC_N. The function conductors B are linked selectively with these transformers in series, being wound round a particular transformer core a number of times proportional to the height of the corresponding step in the appropriate function, thus forming windings on the cores such as $W_{(M-1)\ 1}$, $W_{(M-1)\ 2}$ and so on. The magnetic cell transformers may be incorporated in practice in the delay unit D in such a way that as a pulse from the generator G is propagated in the unit D the transformers are changed in succession from one limiting magnetisation state to another and back again. For example the cores TC_1, TC_2 . . . TC_N may be cores of a magnetic delay line such as described for example in United States Patent Number 2,683,819, the conductors P_1, P_2 . . . P_N being in that case the linking conductors between successive cores. The successive magnetisation changes in the cores TC_1, TC_2, . . . TC_N induce currents in the function conductors but such currents can only be transmitted through the diode BW in the function conductor selected by energisation of one selector lead C. It will be understood also that the diode BW will suppress the currents induced in any of the conductors by the reverse magnetisation changes. Other modes of connecting the cell transformers to the delay unit may be adopted. The number of turns indicated in the windings shown on the drawing is of course not intended to indicate the number which would be required in practice.

The matrix C and selector S may also employ dekatrons or other counter tubes to achieve function selection.

A generator basically similar to that shown in FIGURES 1 and 2 can also be used to produce a function by controlling the rate of change of the output voltage during successive intervals so as to produce an output of the form shown in FIGURE 4. This can be achieved for example by replacing the resistor R_S in the feedback path of the amplifier A_0 by a capacitor. A resetting or clamping device for the output is required in this case to operate between successive characters and restore the output potential to a datum level. Moreover a jump to the starting value of the next character can then be produced by replacing the resistors in column 1 (for example $R_{M-1,\ 1}$) by appropriate capacitors. Also in this case it is necessary to have a choice of two energising potentials in order to obtain both positive and negative rates of change at the output of the amplifier A_0. In this modified form of the invention the successive rates of changes required to synthesise a desired function are provided by virtue of the time constants of the matrix resistors in conjunction with the associated capacitor.

FIGURE 11 illustrates an example of the invention according to the preceding paragraph. In this figure, each conductor P has a complementary conductor P′, and they are both supplied from the same output lead of the delay unit D. The output leads are here denoted by the references Q_1, Q_2 . . . Q_N and they are connected to the input terminals of amplifiers QA_1, QA_1', QA_2, QA_2' and so on. Thus there are two amplifiers to each output lead, and one amplifier is phase reversing whilst the other is not. Assuming that the pulses applied to the leads Q_1, Q_2 . . . Q_N by the delay line are positive, then the amplifiers QA_1, QA_2, . . . QA_N are not phase reversing, whereas the amplifiers QA_1', QA_2' . . . QA_N' are phase reversing. The conductor P_1 is connected to the output terminal of the amplifier QA_1, the conductor P_1' is connected to the output lead of the amplifier QA_1' and so on. Further the conductors P_1, P_2 . . . P_N are connected to a negative bias source via resistors r_1, r_2, . . . r_N whilst the conductors P_1', P_2' . . . P_N' are connected by similar resistors r_1', r_2' . . . r_N' to a source of equal positive bias. The function conductors are also duplicated so that for each function conductor B_{M-1} say, there is a complementary function conductor B'_{M-1}. All the function conductors are connected to the input terminal of the amplifier A_0 as in FIGURE 2, via diodes BW and BW′ as indicated, the diodes BW′ corresponding to the complementary function conductors B′ and being reversed in polarity compared with the diodes BW. The feedback resistor R_S of the amplifiers is replaced by an integrating capacitor IC shunted by a resetting switch RS which may be of the construction described in United States Patent Number 2,843,736. It will be observed, moreover, that the matrix resistors are now connected either from a conductor P to the respective function conductor B, as shown in the case of the resistors $R_{(M-1),\ N}$ and $R_{M,\ 2}$, or from a conductor P′ to a function conductor B′ as in the case of the resistors $R_{(M-1),\ 2}$ and $R_{M,\ N}$. The resistors like $R_{M-1,\ N}$ and $R_{M,\ 2}$ correspond to intervals in the respective functions having negative slopes whereas resistors like $R_{M-1,\ 2}$ and $R_{M,\ N}$ correspond to intervals of positive slope, the actual slope in each instant being determined by the magnitude of the resistor in conjunction with the magnitude of the capacitor IC, and bearing in mind that the amplifier is phase reversing. Furthermore, the first resistor in each row of FIGURE 2 is replaced by a capacitor C, two such being denoted by the references $C_{M-1,\ 1}$ and $C_{M,\ 1}$. These capacitors have

magnitudes so related to the magnitude of the integrating capacitor IC as to determine the starting value of each function which can be generated. The leads C_1 to C_M of the selector switch S are connected to the input terminals of two state devices TSD_1 to TSD_M of which only two TSD_{M-1} and TSD_M are shown in the drawings. The two state devices are for example circuits of the Eccles-Jordan type and have two output terminals, connected as shown to the respective function conductors by two oppositely connected crystal diodes. Thus the diodes CW_{M-1} and CW'_{M-1} connect the output terminals of the devices TSD_{M-1} to the complementary function conductors B_{M-1} and B'_{M-1}. The leads C_1 to C_M form output leads of a decoding arrangement DA to which input signals may be applied by leads BC_1 to BC_R. In the present example, it will be assumed that input signals representing desired functions are applied in binary code, and that the decoding arrangement is of the form described in "High Speed Computing Devices" (McGraw-Hill Book Company Inc., 1950), page 42, with reference to FIGURES 4–3*a*. The leads C_1 to C_M remain unenergised except when the corresponding code appears on the leads BC_1 to BC_R and it will be assumed that to the unenergised state of each lead C_1 to C_M there corresponds an unenergised state of the devices TSD_1 to TSD_M in which negative voltage is applied to the diodes CW_1 to CW_M sufficient to maintain the diodes BW_1 to BW_M non-conducting, whilst positive voltage is applied to the diodes CW_1' to CW_M' sufficient to maintain the diodes BW_1' to BW_M' non-conducting. However, if a code signal denoting a desired character is applied to the leads BC_1 to BC_R, a signal appears in the corresponding lead C, say C_{M-1} sufficient to reverse the state of the respective two state device TSD_{M-1} so that a positive voltage is applied to the diode CW_{M-1} and a negative voltage is applied to the diode CW'_{M-1}. While these voltages are maintained a pulse is launched in the delay unit D, applying positive pulses in succession to the leads P_1 to P_N and negative pulses in succession to the leads P_1' to P_N', the positive pulses in any lead P being simultaneous with the corresponding negative pulse in the complementary lead. When the pulse from the delay line appears in the lead Q_1, the output of the amplifier A_0 jumps to the starting potential and thereafter, as the pulse appears successively on the leads Q_2 to Q_N, the pulse voltage or its negative is integrated selectively into the capacitor IC, with time constants determined by the resistors $R_{M-1,\,2} \ldots R_{M-1,\,N}$ and the capacitor IC. The current in the other resistors of the matrix is carried by the respective diodes CW and CW' and do not affect the output of the amplifier A_0. When generation of the desired function is completed the capacitor IC is reset by a clearing pulse which is arranged to momentarily close the resetting switch RS. This pulse, applied via the lead RP, is applied also to the two-state devices, to restore the energised device to the unenergised state, the pulse being applied in such a way that the other two states are unaffected.

In a modified form of FIGURE 11, the amplifier may have a feedback resistor R_S as in FIGURE 2, and a capacitor may be connected from each of conductors B_1 to B_N and B_1' to B_N to ground.

An output of the form shown in FIGURE 4 can also be obtained by means of the example of the invention shown in FIGURE 5. In this figure, the block G_s represents a sawtooth waveform generator and the sawtooth waveform is applied to an amplifier A_1 which is constructed so that its gain is a function of the value of the applied voltage. Assume that waveform (*a*) in FIGURE 6 represents the input to the amplifier then the gain of the amplifier may be such as to distort the waveform so that its output conforms to the waveform (*b*). The latter waveform is applied to a subtracting circuit E where there is subtracted from it the original sawtooth waveform applied by the path F. The output of the subtracting circuit, after amplification in the amplifier A_0, then conforms to the waveform (*c*) in FIGURE 6 and this forms the output waveform. By pre-arranging the non-linearity of the amplifier, the distortion is made to simulate a desired function, the applied voltage being utilised to select successive rates of change, or slopes. Other waveforms may be used, for this purpose, for example a sine waveform, or a staircase waveform. If the latter alternative is used the desired function will be simulated by a step function similar to that shown in FIGURE 3.

One form of non-linear amplifier, suitable for use as the amplifier A_1, is shown in FIGURE 7, and it comprises a valve V_1 having a cathode circuit comprising a resistor R_C in parallel with a plurality of uni-laterally conductive paths, one for each different slope required to generate a function. The first unilaterally conductive path comprises a diode D_1 in series with the resistor R_1, the second comprises the diode D_2 in series with the resistor R_2, and so on to the last which comprises diode D_N in series with the resistor R_N. The unilaterally conductive paths are connected from the cathode of V_1 to a series of bias sources, the potentials of which are successively more negative and are denoted in the drawing as —v, —2v, and so on. Moreover the diodes are connected so that some conduct in one sense and the others conduct in the opposite sense, but the diodes which have their cathode connected to the cathode of the valve V_1 are non-conducting and the others are conducting in the quiescent state of the generator. However when the negative sawtooth (*a*) is applied to the control electrode of the valve V_1, the diodes D_1 to D_N are switched over successively to the reverse condition in each case so that the cathode resistance of the valve V_1 is varied to discrete steps and causes the gain of the amplifier to change correspondingly. The output of the amplifier is taken from resistor R_A.

With the arrangement shown in FIGURE 7, there is the disadvantage that once a resistor has been switched in to the cathode circuit it cannot be removed and therefore the cathode resistance cannot rise above that value for the rest of the period of the sawtooth. This means that the sawtooth can be distorted by only a small percentage of its amplitude. This disadvantage is overcome by the arrangement shown in FIGURE 8 in which, for example, the diode D_3 is associated with another diode D_3' and another resistance R_3'. The value of R_3' is arranged to be large compared with R_3 to give a desired potential at the junction of R_3 and R_3'. As a result, as the sawtooth potential descends, R_3 is first included in the cathode circuit and is then cut out as the cathode potential descends past the appropriate potentials, namely —3v and —4v in the example illustrated. Moreover, development of this means of connection into a tree allows a resistor to be switched in and out more than once, if required, during one sawtooth period. The greater percentage distortion available allows a more reliable contour to be obtained from the subtracting circuit E, after the linear sawtooth component has been removed.

To enable an arrangement such as shown in FIGURE 5 to produce the several functions required for character writing, a multiplicity of non-linear amplifiers can be used, selection of the desired function being achieved by a switch of the type used in the selector S of FIGURE 1. Alternatively some economy of components can be achieved by considering the non-linear amplifier as a linear amplifier connected to a non-linear network N_M say. A common amplifier may then be used and various non-linear networks, say N_1 to N_M, may be connected selectively to the amplifier by the switch S according to which of the leads C_1 to C_M is energised. Further economy may be achieved because of identity between several portions of different functions. Thus, the net works N_1 to N_M may be subdivided into sections, or so called "bricks," arranged so that different bricks can be

connected to produce a network capable of generating the desired function. For example in FIGURE 8, the paths including R_1 and R_2 may be required for five different functions and can thus constitute a brick capable of being switched into circuit for all five functions.

In the application of the invention shown in FIGURE 9, two function generators are employed, one for generating the x function and the other the y function required to describe a particular character. These two generators have a common generator G for generating the timing pulses or the selecting waveform such as the sawtooth waveform (a). The x function generated at any particular time is applied to the x deflecting plates X of the cathode ray display tube T whilst the corresponding y function is simultaneously applied to the y deflecting plates Y. A shift generator U may also be connected to the x and y plates as indicated for applying shift voltages to locate the area on the screen S' of the cathode ray tubes in which the character is described. This shift generator may, as shown, be coupled to the generator G which times the function generation.

As aforesaid, the invention is not restricted to generating the functions required to describe alphabetical or numerical characters, even when employed to generate functions of a common parameter. In the case of functions of a common parameter, as in FIGURE 9, considerable economy can be achieved by using the same function $x(T)$ expressing x in terms of T, where T is a common parameter, or the same function $y(T)$ expressing y in terms of T, in the derivation of several functions $y(x)$ expressing y in terms of x. For example M functions $x(T)$ and N functions $y(T)$ may be used to derive P functions $y(x)$ where M and N are both less than P. This produces an economy of $2P-M-N$ rows of resistors R. Furthermore a given delay unit can, because of practical limitations, drive only a limited number of rows of resistors. If the number of x and y functions exceeds this limit, other delay units, or cathode followers, or emitter followers, are required to give sufficient power output, such for example as represented by the amplifiers QA in FIGURE 11. Thus, in addition to economy in rows of resistors, there may be other and more significant economies.

What we claim is:

A function generator comprising an output circuit, a plurality of groups of impedances of selected magnitudes in which each group has a common connection to which all the impedances of the group are connected, a group of input connections each connected to one impedance in every group, commutator means to apply a pulse to said input connections in sequence whereby energy derived from a pulse reaching the output circuit is responsive to the magnitude of the impedance of a selected group to which the pulse is applied thereby to determine the respective section of the function, an amplifier having an input terminal and an output terminal, said output terminal being connected to said output circuit, a first series of diodes connected from the respective common connections to said input terminal, a second series of diodes connected from the respective common connections, the diodes of said second series being normally conducting so as to maintain said common connections at a reference potential and the diodes of said first series non-conducting, and means for selectively rendering a diode of said second series non-conducting and consequently the diode of the first series connected to the same common connection conducting thereby to cause the amplifier to respond to the energy transmitted by the group of impedances connected to said input terminal through the conducting diode of said first series.

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