United States Patent

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[54] **QUICK RESETTING APPARATUS**
16 Claims, 5 Drawing Figs.

[52] **U.S. Cl.** ..... **317/33 SC,** 317/22, 317/28, 317/36 TD, 317/142, 320/1
[51] **Int. Cl.** **H01h 47/18,** H02h 3/08
[50] **Field of Search** ..... 317/36 TD, 33 R, 33 SC, 22; 320/1; 317/27, 28, 142

[56] **References Cited**
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3,295,019	12/1966	Altfather	317/36 TD
3,543,094	11/1970	South et al.	317/36 TD

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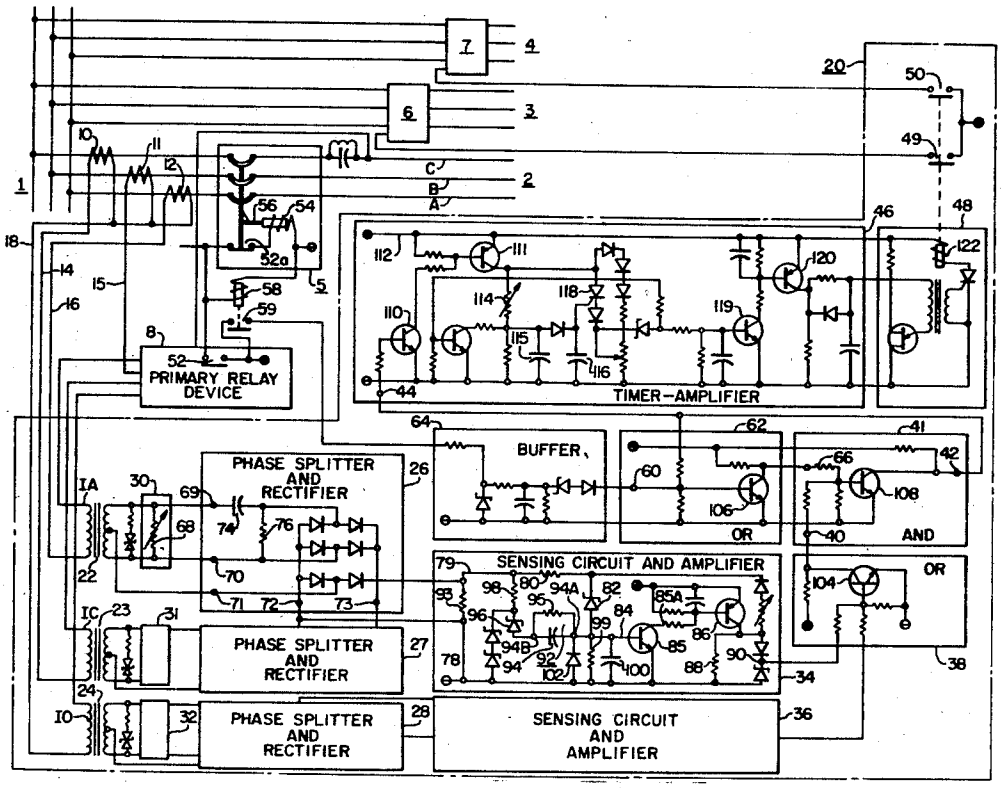
ABSTRACT: A fault current magnitude actuated resettable sensing apparatus particularly for resetting the timer of a timer actuated backup fault responsive device which sensing apparatus response to the steep slope of a decaying actuating signal resulting from the decay of the current responsive signal upon opening of the breaker to terminate the fault current whereby the time interval for the resetting of the timer by the sensing apparatus remains substantially constant irrespective of the time of the decay of the actuating signal resulting from the interruption of fault current of any expected magnitude.



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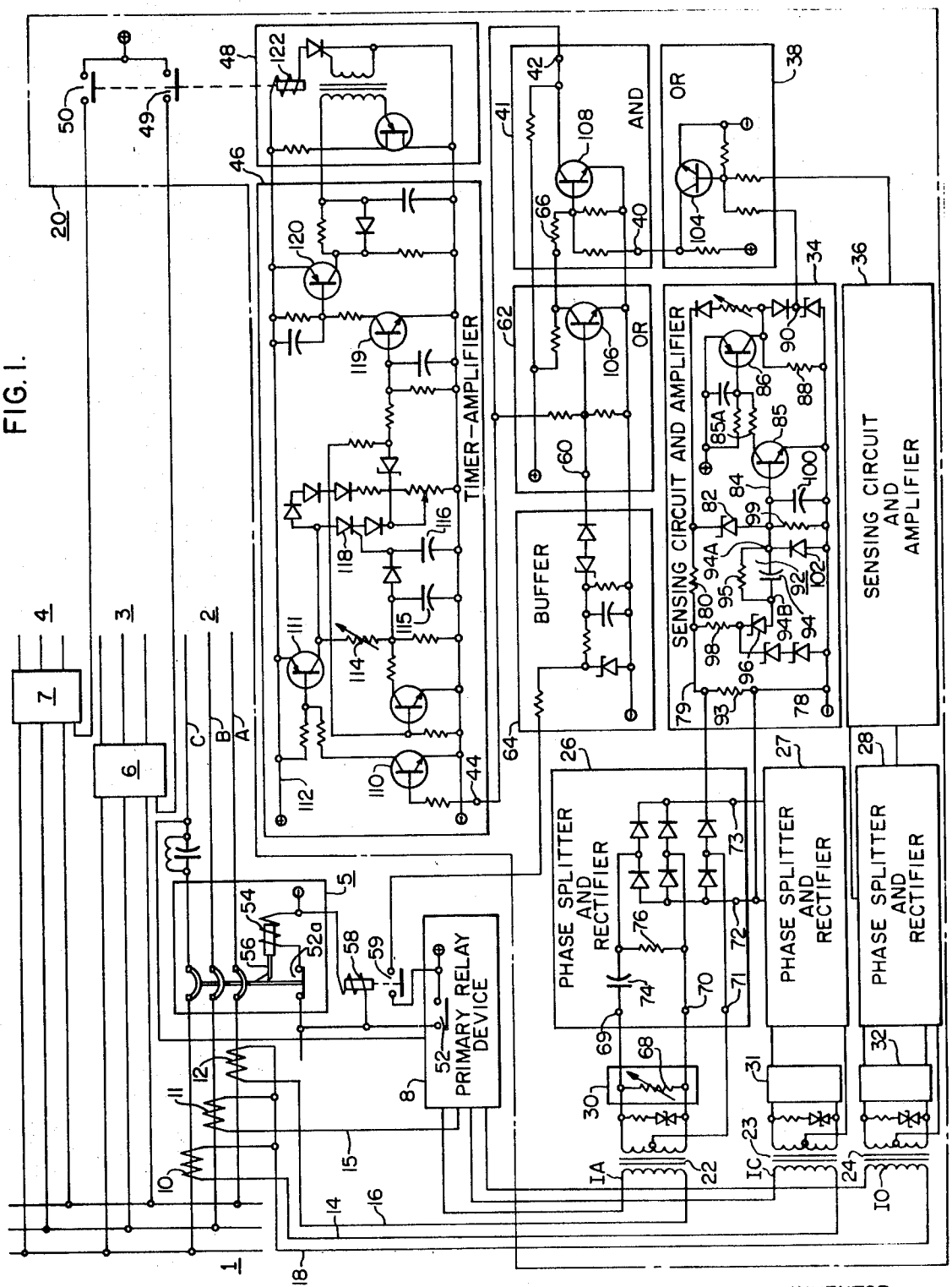

FIG. 1.

WITNESSES

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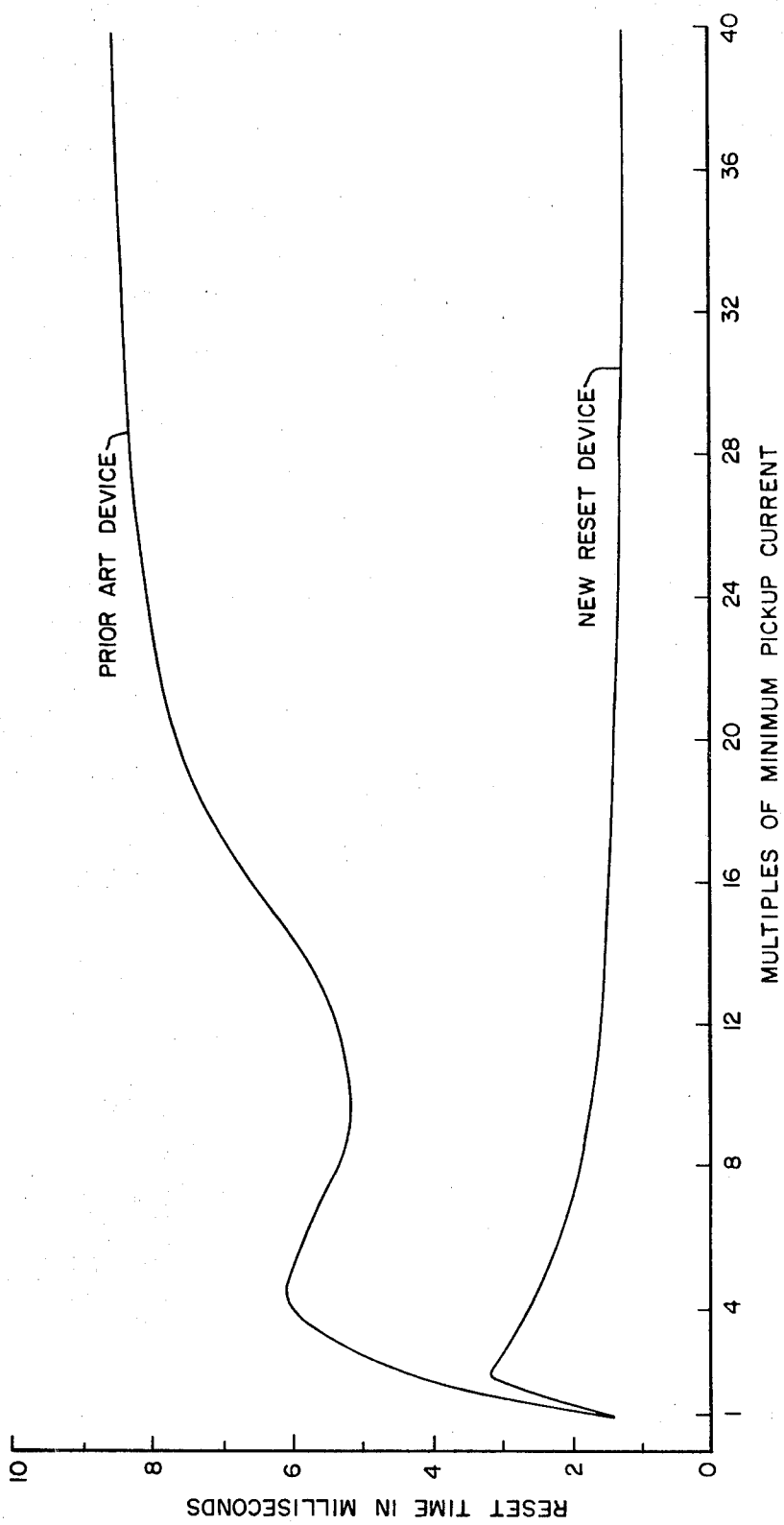
PRIOR ART DEVICE
NEW RESET DEVICE
RESET TIME IN MILLISECONDS
MULTIPLES OF MINIMUM PICKUP CURRENT
0
2
4
6
8
10
1
4
8
12
16
20
24
28
32
36
40

FIG. 2.

CURRENT REDUCED FROM 2X PICKUP TO 0 AMPERES

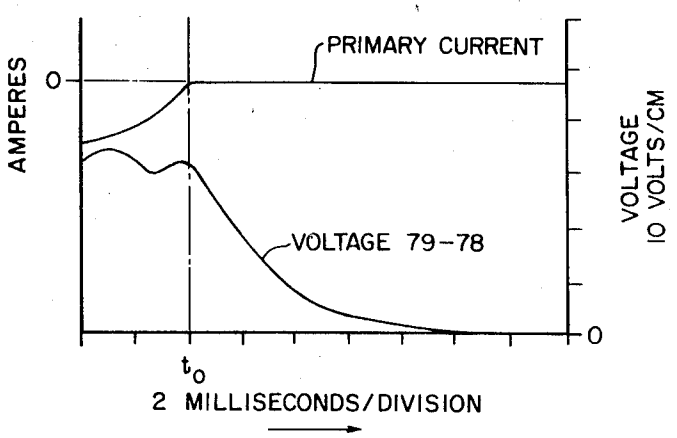

FIG.3A.

CURRENT REDUCED FROM 10X PICKUP TO 0 AMPERES

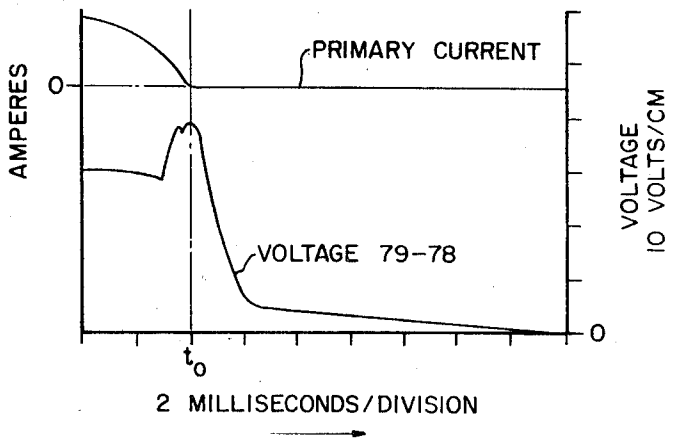

FIG.3B.

CURRENT REDUCED FROM 40X PICKUP TO 0 AMPERES

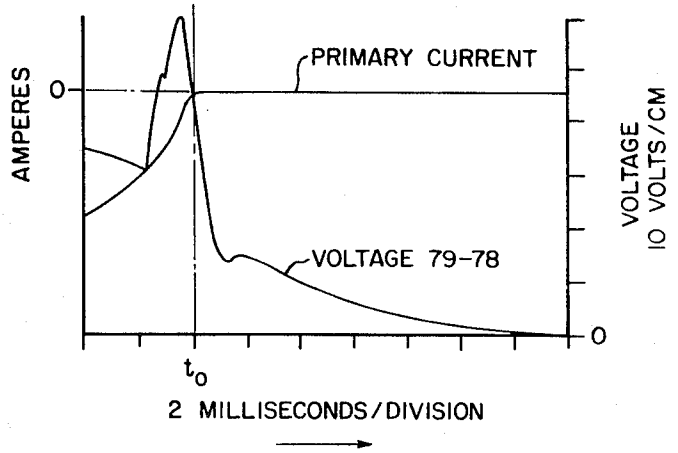

FIG.3C.

QUICK RESETTING APPARATUS

BRIEF SUMMARY OF THE INVENTION

This invention is particularly intended for use in protective relaying in which backup operation is provided for tripping backup breakers in the event that the primary breaker fails to interrupt the fault current and provides a fast and constant reset time for the backup protection timer irrespective of the magnitude of the fault current.

In the prior art, such a current actuated unit the time for resetting typically would vary from 2 to 9 milliseconds depending upon the magnitude of the primary current at the time of breaker opening. Additionally, if the current is suddenly reduced below pickup but not to zero, then the reset time would be as high as 15 milliseconds. Present reset apparatus requires the use of a backup timer which provides a time delay sufficiently longer than the longest possible expected reset time. Unless this time is provided the backup timer could provide a false actuation of the backup breakers when in reality the primary breaker has succeeded in opening the primary current.

It is desirable that the resetting circuit have a substantially constant reset time independent of the magnitude of the primary current which actuates the same. This enables a minimum time setting of the backup protection timer and permits a quicker actuation of the backup protection should the primary breaker fail to interrupt the primary current. The present invention obtains this substantially constant interval by utilizing the slope of the rapidly decaying primary current to actuate the resetting unit.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a backup protecting relaying network, partially in block form, embodying the current sensing quickly resetting circuit of the invention.

FIG. **2** is a curve comparing the times required to reset the prior art sensing circuit and to reset the sensing circuit of this invention.

FIGS. **3A**, **3B** and **3C** illustrate typical time-voltage curves showing the decrease in voltage with three different magnitudes of fault current.

DETAILED DESCRIPTION

Referring to the drawings by characters of reference, the numeral **1** designates generally a substation bus energized by three power supplying polyphase lines **2**, **3**, and **4** from suitable energy sources (not shown) through breakers **5**, **6** and **7** respectively. As illustrated in FIG. **1**, the primary fault protection from the line **2** is the breaker **5**. In the event the breaker should fail to open the circuit therethrough, the backup breakers **6** and **7** would be actuated at a time interval subsequent to attempt to actuate the breaker **5** which time interval is sufficient long to indicate a failure of the breaker **5** to open.

The primary relay device **8** for actuating the breaker **5** may be similar to that found in U.S. Pat. to C. T. Altfather No. 3,295,019 dated Dec. 27, 1966 and is shown within the dot-dash rectangle **4A** of the said Altfather patent. The fault responsive signal is applied to the primary relaying device **8** by the current transformers **10**, **11** and **12** individually associated with the conductors C, B and A respectively of the network **2**. These current transformers are connected in Y circuit arrangement. The negative and positive sequence current is carried by the conductors **14**, **15** and **16** and the zero sequence current by the conductor **18**.

The breaker failure or backup protecting apparatus **20** includes current transformers **22**, **23** and **24** which have their primary windings in series in the conductors **16**, **14** and **18** respectively. The output potential quantities of these transformers energize the phase splitter and rectifying networks **26**, **27** and **28** respectively through setting circuits **30**, **31** and **32** which comprise resistors adjustable to determine the current to voltage ratio in the usual manner. The rectified output quantities of the phase splitter and rectifying networks **26** and **27** are connected together in parallel and the resulting signal is supplied to a sensing circuit and amplifier **34**. The rectified output quantity of the phase splitter and rectifier network **28** is supplied to a sensing circuit and amplifier **36** of the same construction as the circuit and amplifier **34**.

The output quantities of the sensing and amplifying circuits **34** and **36** are supplied individually to the two inputs of an OR network **38**; the output circuit of which is connected to a first input terminal **40** of an AND network **41**. The output terminal **42** of the AND network **41** is connected to the input terminal **44** of a timer-amplifier **46**. The output of the timer-amplifier is connected to a relaying device **48** which has two sets of contacts **49** and **50**. These contacts are connected, as diagrammatically illustrated, to trip the breakers **6** and **7** respectively in the event of the actuation of the relaying device **48** and closure of the contacts **49** and **50** when the backup protection timer **46** times out.

As discussed more fully in the said Altfather patent, the occurrence of a fault in the network **2** causes the primary relay device **8** to close its contacts **52**. These contacts **52** correspond to the contacts **50***a* of the said Altfather patent. When contacts **52** close a circuit is completed from the positive power supply terminal plus through the closed contacts **52**, the contacts **52***a* of the breaker **5** and the trip coil **54** to the negative power supply terminal. Energization of the trip coil **54**, in normal operation, will disengage the latch **56** and the breaker contacts open to disconnect the network **2** from the bus **1**. Closure of the contacts **52** also completes an energizing circuit through the winding of the relay **58**, whereby this relay closes its contacts **59** and completes a circuit through the buffer **64** for energizing the first input terminal **60** of the OR network **62**. When so energized, the OR network **62** energizes the second input terminal **66** of the AND network **41**, and the AND network **41** therefore will initiate the timing function of the timer-amplifier **46**.

The timing interval of the timer-amplifier **46** is of sufficient duration so that it will not time out and actuate the relaying device **48** to trip the breakers **6** and **7** if the breaker **5** successfully terminates the current flow therethrough. If however, the breaker **5** fails to interrupt the fault current therethrough, the OR network **38** will not remove its operating signal from the input terminal **40** of the AND network **41** so that the timer will time out and energize the relaying device **48**. As set forth above, the closure of contacts **49** and **50** trip the breakers **6** and **7** to deenergize the station bus **1** and thereby prevent the flow of fault current from the station bus into the supply network **2**.

In accordance with this invention, the sensing circuits **34** and **36** remove the operating signals to the OR network **38** in a substantially constant time interval which is substantially independent of the magnitude of the fault current. Both of the sensing circuits **34** and **36** are identical and only the details of the circuit **34** are illustrated. The output winding of the current transformer **22** has its end terminals connected to the end terminals of a variable resistor **68** and to the input terminals **69** and **70** of the phase splitter and rectifier network **26**. The secondary winding of the current transformer **22** has its center tap connected to an input terminal **71** of the network **26**. In order to maintain a minimum time delay and yet provide a fairly even output the rectified alternating quantity supplied by the transformer **22**, at its output terminals **72** and **73** of the phase splitter and rectifier **26**, the single phase input supplied by the transformer **22** is split into two phase displaced quantities by the capacitor **74** and resistor **76**. Such a phase splitting is well known to the art and will not be further described. The three phase displaced quantities are rectified in a full wave three phase rectifying network connected to energize the output terminals **72** and **73**. The terminals **72** and **73** are connected across a pair of conductors in busses **78** and **79** of the sensing circuit **34**.

The conductor **79** is connected through a resistor **80**, a Zener diode **82** to the base electrode **84** of a transistor **85**. The emitter of the transistor **85** is directly connected to the conductor **78** whereby the transistor **85** is rendered conductive upon energization of the busses **78** and **79** to a potential greater than the breakover voltage of the Zener diode **82**. A second transistor **86** has its emitter connected to a source of positive potential +and its collector connected through a resistor **88** to the negative terminal −of the potential supply which −terminal is also connected to the conductor **78**. The base of the transistor **86** is connected to the collector of the transistor **85** through a resistor **85A**. Therefore, upon energization of the busses **78** and **79** to the breakover voltage of the Zener diode **82**, the transistor **85** will conduct and base current will flow through the transistor **86** which thereupon conducts to raise the potential of the output terminal **90** which is connected to one input terminal of the OR network **38**. When the transistor **86** is not conducting the potential of the output terminal **90** is that of the negative power supply.

The conductor **79** is also connected to the base **84** through a timing device or network **92**. This network includes a capacitor **94** shunted by a resistor **95** with one terminal **94A** of the capacitor **94** and resistor **95** connected to the base **84** of transistor **85**. The other terminal **94B** of the capacitor **94** and resistor **95** is connected through a Zener diode **96** and a resistor **98** to the conductor **79**. The common terminal **94A** is connected to the conductor **78** through a resistor **99** shunted by a capacitor **100** and by a solid state rectifying diode **102** all in parallel with the base-emitter circuit of the transistor **85**. The diode **102** is connected to limit the reverse voltage which can appear between the emitter and base of the transistor **85**. The maximum voltage to which the capacitor **94** may be charged is limited by a pair of Zener diodes which are connected between the conductor **78** and the common connection of the Zener diode **96** and the resistor **98**.

It is believed that the remainder of the description may best be set forth by a description of operation of the apparatus which is as follows:

In the event of the occurrence of a fault in the network **2** which causes current IA of fault magnitude to flow in the conductor A associated with the current transformer **12**, the current transformer **22** will be energized and provide an alternating potential between the terminals **69**, **70** and **71** of a magnitude with respect to the magnitude of the current flowing through the conductor A as determined by the setting of the variable resistor **68**. This alternating quantity is rectified by the three-phase full wave rectifying network of the phase splitter and rectifier circuit **26**. Assuming that the current IA in the A conductor is a number of multiplier of the normal rated or pickup current and greater than the current IC in the C conductor, the rectified potential of a magnitude proportional to the IA current will appear between the output terminals **72** and **73** and between the conductors **78** and **79**. The variable resistor **68** is set so that when the current flowing through the conductor A rises to approximately 1¼ times the pickup or normal maximum value of current in the line A, the voltage between conductors **79** and **78** will be sufficiently high to cause the Zener diode **82** to break over. Therefore with a value of current greater than the set pickup, the Zener diode **82** will conduct base current from the bus **79** through the transistor **85**. This will allow base current of transistor **86** to flow through a resistor **85A** and the collector emitter circuit of transistor **85** to −, conductor **78**. The conducting transistor **86** raises the potential of the output terminal **90** to substantially that of the positive bus. This potential supplies a base drive current to the transistor **104** of the OR network **38**. When transistor **104** conducts, the potential of the input terminal **40** of the AND network **41** is reduced to substantially the negative source potential and one actuating signal is applied to the AND network.

The fault also actuates the primary relay device **8** to close its contacts **52** to energize the relay **58**, thereby closing contacts **59** to supply a positive potential to the buffer circuit **64** which will actuate input terminal **60** of the OR network **62**. This positive potential causes base current for transistor **106** to flow and make it conduct whereby the potential of the second input terminal **66** of the AND network **41** is substantially that of the negative supply. This is the remaining actuating signal for the AND network **41**. With both terminals **40** and **66** at negative potential, transistor **108** will stop conducting and cause the potential of the output terminal **42** of the AND network **41** and of the input terminal **44** of the timer amplifier **46** to increase sufficiently to provide base current for the transistor **110** which conducts to cause base current in the transistor **111**. Charging current flows through the transistor **111** and the variable timing resistor **114** and the main timing capacitors **115** and **116** charge at a rate determined by the resistance value of the timing resistor **114**.

Assuming that the breaker **5** did not terminate fault current, the primary relay device **8** will maintain the relay **58** energized. Under these conditions both of the input terminals of the AND network **41** will remain energized by the actuating signals and a positive potential will be held at its terminal **42** to maintain the timer in its timing condition with the capacitors **115** and **116** charging. At the end of the timing interval, the critical potential necessary to fire the thyristor **118** will be reached and the thyristor **118** thereupon conducts to render the transistors **119** and **120** conducting. Conduction of the transistor **120** energizes the relaying device **48** which actuates its output relay **122** and the contacts **49** and **50** close, to open the breakers **6** and **7** to interrupt the current flowing in the line **2**. This opening of the breakers also deenergizes the substation busses and the loads (not shown) supplied thereby.

The timing interval of the timer amplifier **46** should be as short a time as possible in the event of the failure of the breaker **5** in order to alleviate damage to the power systems and yet at the same time the delay must be large enough so that the timer will not time out until the breaker **5** is given time enough to interrupt the fault current therethrough. Under the prior art resetting or timing terminating network, the interval required to do this increased as the magnitude of the fault current increased. Therefore, the timer was adjusted to provide a delay sufficient to accommodate the longest expected resetting or terminating time which as indicated in FIG. **2** could exceed 8 milliseconds and as explained above could under the circumstances where the current did not decrease to zero be as long as upwards of 15 milliseconds. With the resetting network operating as described herein, the resetting or terminating time is rendered from a practical viewpoint independent of the pickup or fault current magnitude which initiated the timing operation. In the instance shown and with the values to be given below this interval will remain between 1 and 2 milliseconds for a multiple of pickup current between 8 and 40 with a maximum time of only 3.2 milliseconds at a fault current two times pickup. This permits a great reduction of the timing interval which must be provided by the timer-amplifier **46** and thereby greatly lessens the danger of substantial damage to the power systems.

Assume an interruption of the fault current by the breaker **5** for current IA through the line A. The output voltage of the phase splitter and rectifier **26** will decrease and eventually reach a zero potential. However because of the reactance in the circuits for energizing the conductors **78** and **79**, the time required for this voltage to reach a zero magnitude will be dependent upon the magnitude of the current flowing through the conductor A at the time that the breaker **5** terminated this current flow. This is illustrated in FIGS. **3A**, **3B** and **3C** which show the time for the voltage between the conductors **78** and **79** to reach zero potential for multiples of pickup current FIG. **3A**, **10** multiples of pickup current, FIG. **3B**, and **30** multiples of pickup current, FIG. **3C**. The zero point of time being of course when the primary current reached its zero value time t_0 in each of the FIGS. **3A**, **3B** and **3C**. The sensing circuit of this invention does not, upon the potential between the conductors **78** and **79** reaching a value less than the breakover of Zener diode **82** remove the positive output potential applied

by the output terminal **90** to the OR network **38** and thereby reset or terminate further timing of the timer **46**, but rather utilizes the initial rapidly decaying portion of the voltage curve to terminate the conduction of the transistors **85** and **86** and the removal of the positive output potential to the OR network **38**.

During the interval in which the conductors **78** and **79** were energized, the capacitor **94** was charged through the resistor **98**, Zener diode **96** and base to emitter of the transistor **85**. The magnitude of the resistance of the resistor **98** is small and the capacitor **94** therefore assumes, with a minimum time delay, a charged condition in which the potential thereacross is substantially equal to the potential between the conductors **78** and **79** minus the drop across the Zener diode **96** (which may for example be 9.1 volts as compared to the 6.8 volt drop across the Zener diode **82**). Any small decreases in the potential between the busses **78** and **79** will be followed by a comparable discharge of the capacitor **94** through the shunt connected resistor **95**. Small increases will, or course, be taken care of in the same manner in which the capacitor **94** is originally charged.

Assume now an opening of the breaker **5** and an interruption in the current therethrough. The potential between the busses **78** and **79** will decrease sharply (see FIGS. **3A**, **3B** and **3C**). The Zener diode **96** has a small forward drop as for example six-tenths of a volt so that as soon as the potential of the conductor **79** drops to six-tenths of a volt below the potential of the terminal **94B**, the capacitor **64** commences to discharge through the Zener diode **96**, the resistor **98**, a resistor **93** connected across the busses **78** and **79** and the resistor **99** and/or the diode **102** to the other terminal **94A** of the capacitor **94**. This current flow through the resistor **99** and/or the diode **102** results in the reversal of the potential between the base and emitter and the transistor **86** and a termination of the conduction thereof. It will now be apparent that the OR network **38** will be actuated to remove its signal to the AND network **41** to terminate further timing of and reset the timer **46** without the necessity of the quantity supplied to the busses **78** and **79** returning to zero or even substantially zero.

If the current through the line A reduced slightly rather than terminated, then the capacitor **94** would discharge through the resistor **95** at a similar rate to that of the rectified voltage and the sensing circuit and amplifier **34** would not terminate its signal to the OR network **38** and no resetting of the timer **46** would result. The timer **48** would continue to time out its interval and trip the breakers **6** and **7**.

Assuming that the circuit constants are so taken that a voltage of approximately 5 volts represents a single multiple of pickup current flow in the line A until limited by a Zener clipper across the secondary of **22**, suitable circuit constants for the sensing circuit would be as follows:

Resistor **80**=10K ohms
Resistor **93**=82K ohms
Resistor **95**=33K ohms
Resistor **98**=2.2K ohms
Resistor **99**=10K ohms
Zener diode **82**=6.8 breakover voltage
Zener diode **97**=9.1 breakover voltage
Capacitor **94**=0.5 microfarads
Capacitor **100**=0.5 microfarads.

When the values as indicated are utilized, the time required for the sensing circuit to reset subsequent to opening of the breaker would, as indicated in FIG. **2**, vary from a maximum of 3.2 milliseconds at two multiples of pickup current to a minimum of 1.2 milliseconds at 40 multiples of pickup current.

What is claimed and is desired to be secured by United States Letters Patent is as follows:

1. A sensing apparatus comprising a pair of input terminals adapted to be energized with a variable magnitude electrical quantity, a pair of output terminals, a first energizing network for said output terminals and including switching means having a control circuit connected to said input terminals and operable in response to the occurrence of a predetermined minimum magnitude of said quantity to render said energizing network effective to energize said output terminals at a first relative polarity, a chargeable device, a charging circuit for said chargeable device, said charging circuit being effective to charge said chargeable device when the magnitude of said quantity applied to said input terminals is not less than said predetermined minimum magnitude, a first discharge circuit connected to discharge said chargeable device, and means connecting said discharge circuit to said output terminals for energization thereof at a second relative polarity as a consequence of the discharging of said chargeable device.

2. The combination of claim **1** in which said quantity is of unidirectional potential, said discharge circuit includes an impedance energized by said quantity in a polarity to oppose the discharge of said chargeable device, and in which there is provided a second discharge circuit for said chargeable device, said second discharge circuit discharging said chargeable device at a rate which is independent of the rate of reduction of the magnitude of said quantity.

3. The combination of claim **1** in which said energizing network is connected across said input terminals and includes an asymmetric current conducting device connected to conduct current between said output terminals in a first direction, said network further including a potential dropping device which limits the current flow through said asymmetric device, said asymmetric device having a less impedance to current flow in said first direction than in a second direction opposite to said first direction, said impedance to current flow in said second direction being effective to establish said second relative polarity.

4. The combination to claim **3** in which said asymmetric device includes the control element of a current actuated switch device.

5. The combination of claim **4** in which said switch device is a semiconductor solid state triode device having a control element and a pair of electrodes and which conducts between its electrodes as a consequence of the current flow through said control element.

6. The combination of claim **5** in which said triode device is a transistor having a base and collector and an emitter, said control element is said base and in which said base is connected to one of said output terminals and said emitter is connected to the other of said output terminals.

7. The combination of claim **6** in which said switching means is a Zener diode, said potential dropping device is a resistor, and an asymmetrically conducting diode is connected in shunt with said base and said emitter in a polarity to conduct through its lesser impedance in a direction opposite to the lesser impedance to conduction between said base and emitter of said transistor.

8. The combination of claim **7** in which said chargeable device is a capacitor, and said second discharge circuit includes a resistor connected in shunt with said capacitor.

9. The combination of claim **1** in which said charging circuit includes an asymmetric conducting device connected to charge said chargeable device through its greater impedance, said first discharge circuit also including said asymmetric device connected to discharge said chargeable device through its lesser impedance.

10. The combination of claim **9** in which said first discharge circuit includes a first impedance element connected to be energized with a potential proportional to the magnitude of said quantity and polarized to oppose the discharge of said chargeable device and further includes a second impedance element connected in shunt with said output terminals.

11. The combination of claim **10** including a triode semiconductor switch having a pair of main electrodes and a control electrode, said control electrode being connected to a first of said output terminals, one of said main electrodes being connected to the second of said output terminals, said first energizing network including current control means to limit the current flow between said control electrode and said

one main electrode, and a third impedance element connected in shunt with said chargeable device.

12. The combination of claim 11 in which said switching means comprises a first Zener diode, said asymmetric conducting device comprises a second Zener diode, said current control means comprises a fourth impedance element, said triode switch includes a junction permitting substantially unimpeded flow of current through said energizing network and a high impedance to the flow of current through said first charge circuit.

13. The combination of claim 12 in which said first Zener diode breaks over at said minimum magnitude of said quantity and said second Zener diode breaks over at a magnitude substantially greater than said predetermined magnitude.

14. A quick resetting circuit comprising first and second conductors, a plurality of resistors, a plurality of Zener diodes, a transistor having a base and a collector and an emitter, a first control circuit connected between said first conductor and said base and including in series circuit a first of said resistors and a first of said Zener diodes, means connecting said emitter to said second conductor, a capacitor, a charging circuit connecting said capacitor between said conductors and including in series circuit a second of said resistors and a second of said Zener diodes, means connecting a third of said resistors between said conductors, means connecting a fourth of said resistors between said base and said emitter, a first discharge circuit connected across said capacitor and including in series circuit said second Zener diode and said second resistor and said third resistor and said fourth resistor, and means connecting a fifth of said resistors in shunt with said capacitor.

15. The combination of claim 14 including an alternating current network connected to energize said conductors through a rectifying device whereby said conductors are energized with a rectified electrical quantity proportional to the alternating electrical quantity flowing in said network, said network including reactance which delays the collapse of said quantity upon deenergization of said network, the magnitude of said rectified quantity normally being not greater than a first predetermined magnitude but being subject to excursions which are many times said first magnitude, said first Zener diode being effective to break over at magnitudes of said rectified quantity not less than said first predetermined magnitude, said second Zener diode being effective to break over only at magnitudes which exceed a second predetermined magnitude of said rectified quantity, said second predetermined magnitude being greater than said first predetermined magnitude, the magnitude of said fifth resistor being less than the magnitude of said third resistor and greater than the magnitude of said second resistor, first potential limiting means connected in said charging circuit for limiting the maximum potential to which said capacitor may be charged, and second potential limiting means connected between said emitter and said base and effective to limit the potential therebetween due to current flow in said first discharge circuit.

16. The combination of claim 15 in which said first predetermined magnitude is about 6.8 volts, said second predetermined magnitude is about 9.1 volts, the magnitude of the resistance of said first resistor is about 10K ohms and of said second resistor is about 2.2K ohms and of said third resistor is about 82K ohms and of said fourth resistor is about 10K ohms and of said fifth resistor is about 33K ohms, the capacitance of said capacitor is about 0.5 mfd., the potential limit of said first limiting means is about 40 volts and of second limiting means is about 1 volt.