

[54] **CIRCUMFERENTIAL AND LATERAL WEB REGISTRATION CONTROL SYSTEM**

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226/16, 226/31

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[58] Field of Search 101/181, 248; 226/16, 30, 31,
226/2, 3

[56] **References Cited**

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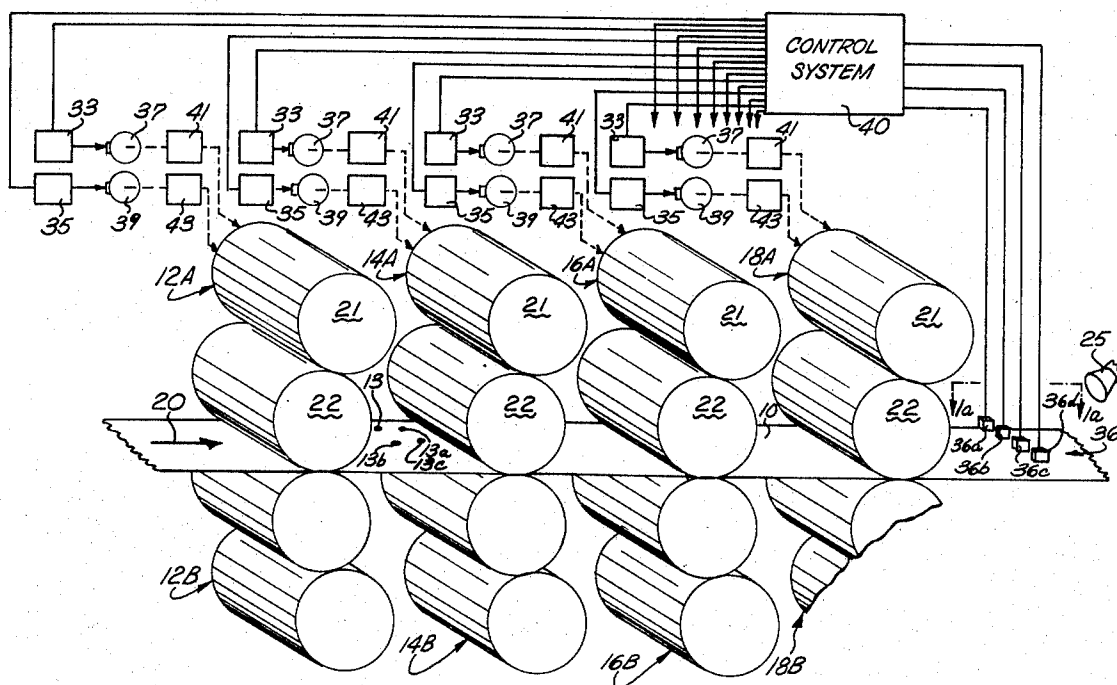
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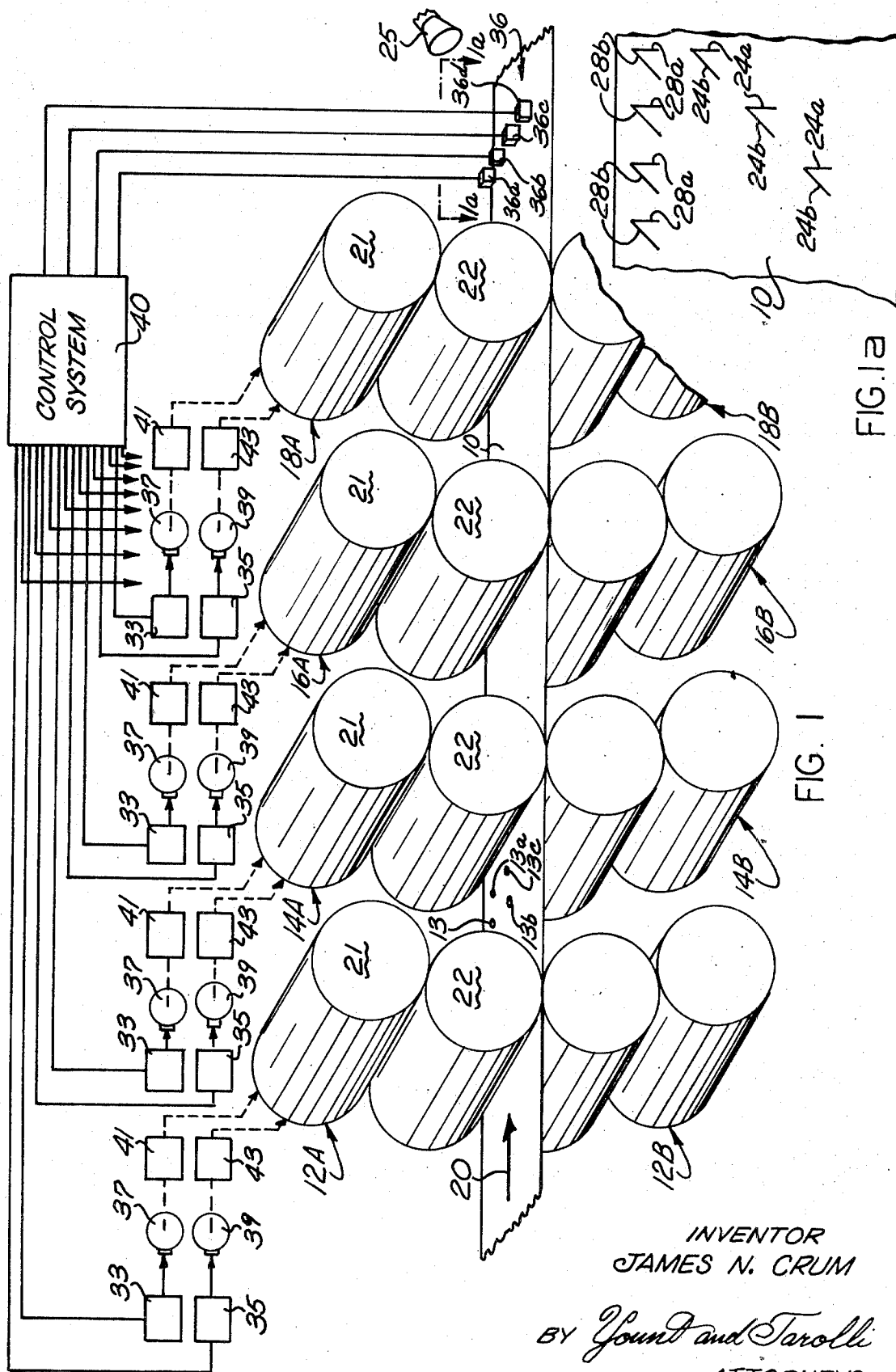
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[57] **ABSTRACT**

A control system for controlling registration in a multi-color web-fed printing press system senses register marks which are printed on the web. Any circumferential registration error which is detected by sensors that sense the register marks is translated into a count in a circumferential counter which is coupled to a circumferential motor control circuit. The circumferential motor control circuit drives a stepping motor which in turn drives appropriate gearing to correct for the circumferential misregistration of the web as directed by the count in the circumferential counter. The apparent lateral registration error is then measured in a similar manner and is stored as a count in a lateral counter which corrects for lateral misregistration through a stepping motor and appropriate gearing. The error previously determined in the circumferential register is employed to correct the apparent error in the lateral register so that it represents the true lateral registration error instead of the apparent lateral registration error.

17 Claims, 8 Drawing Figures





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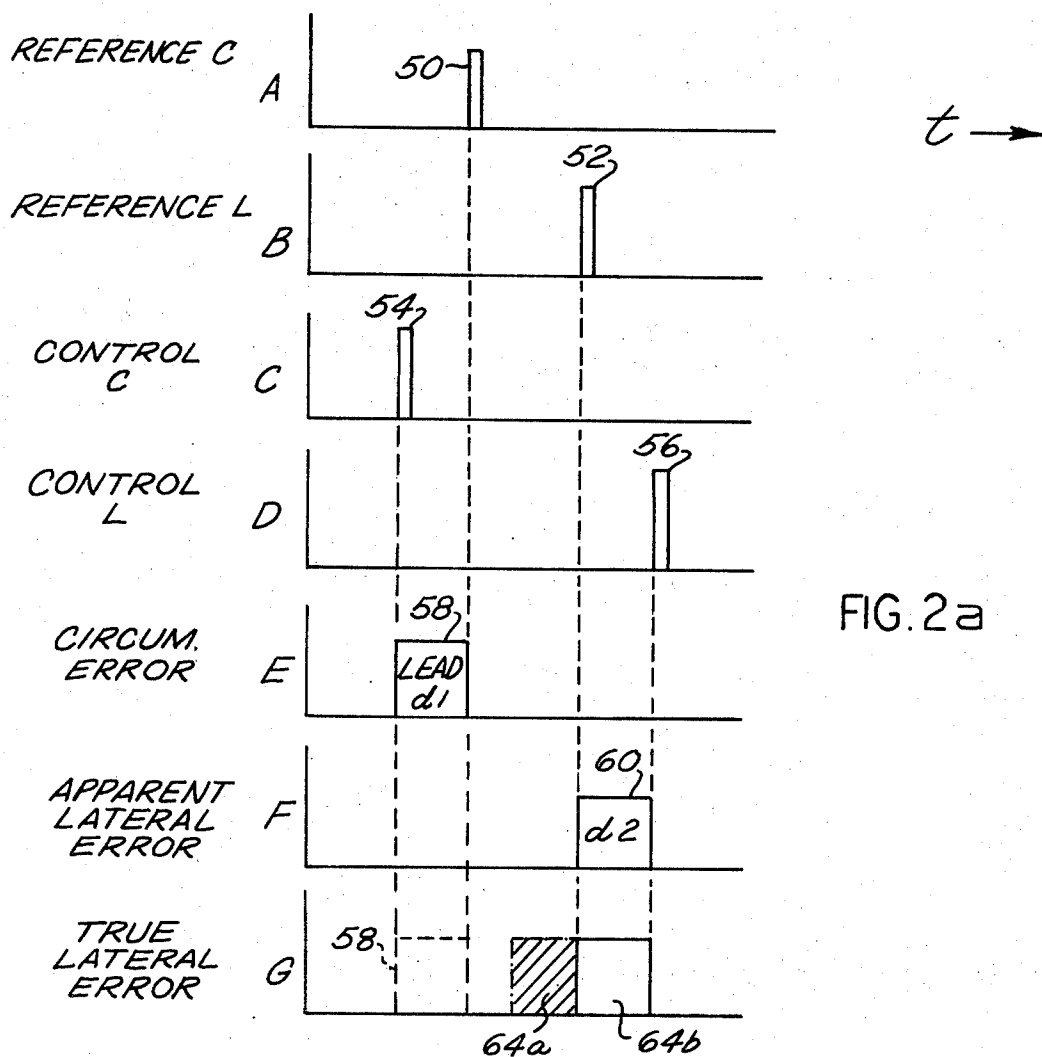
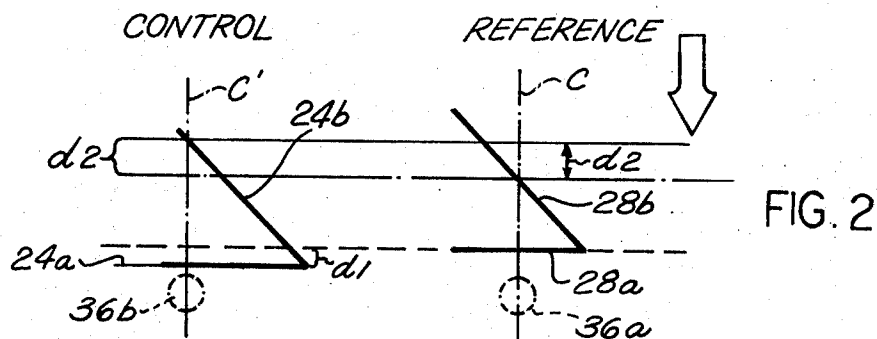


FIG. 2a

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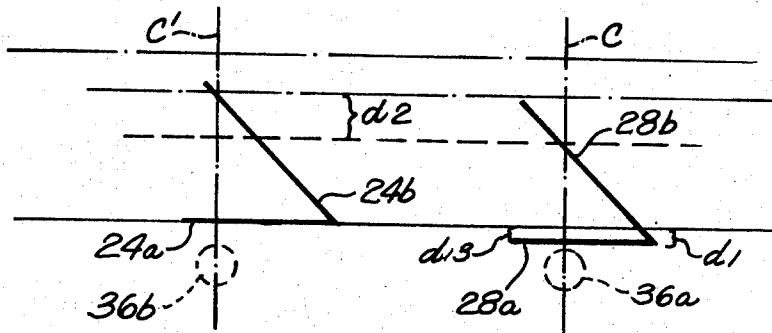


FIG. 3

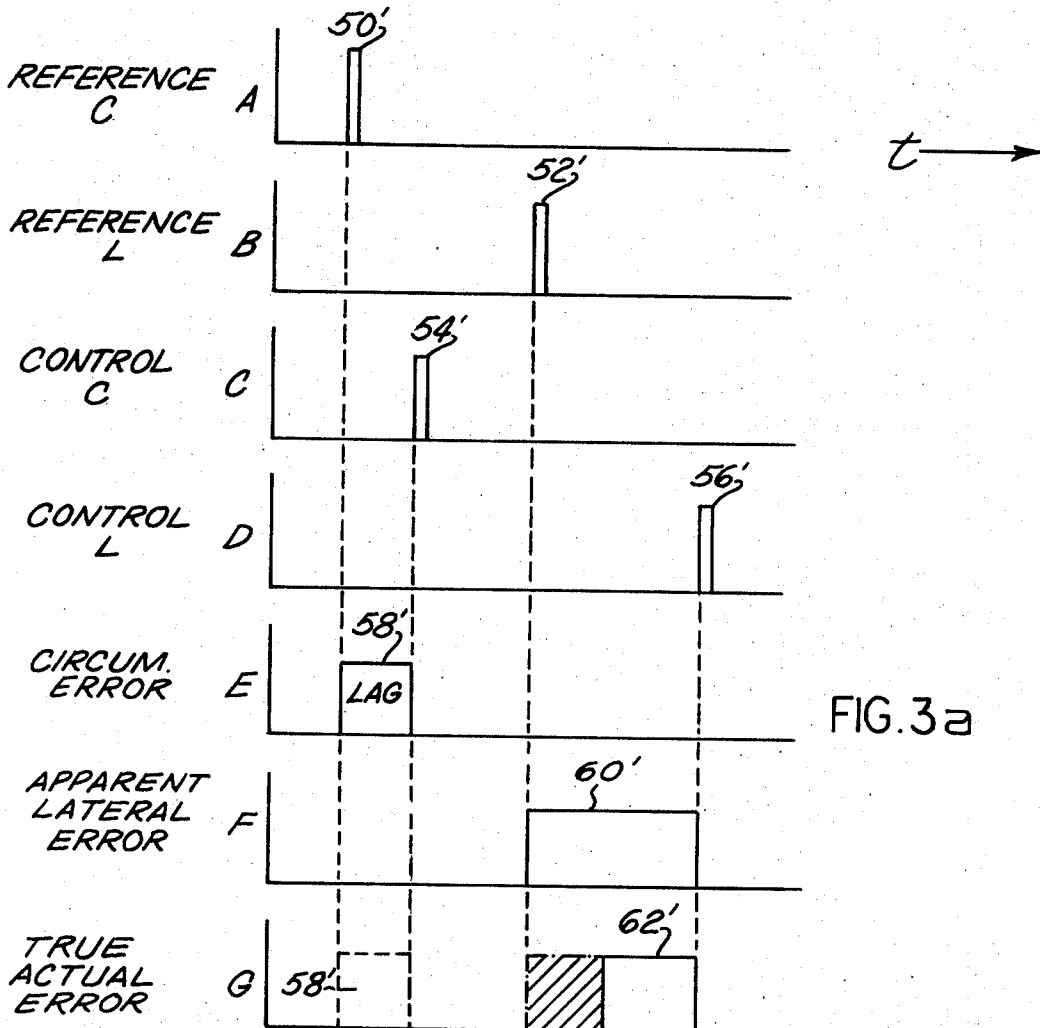


FIG. 3a

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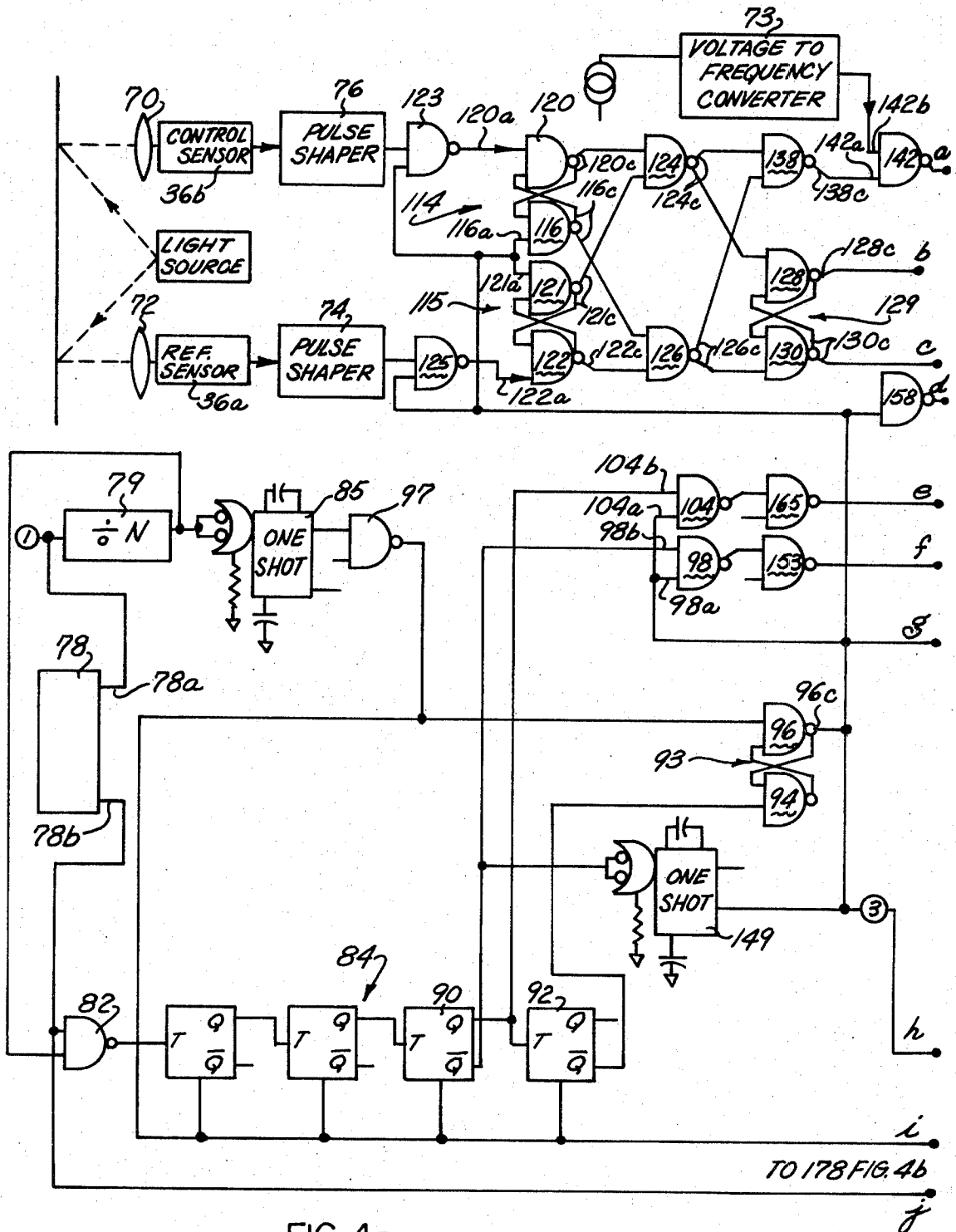


FIG. 4a

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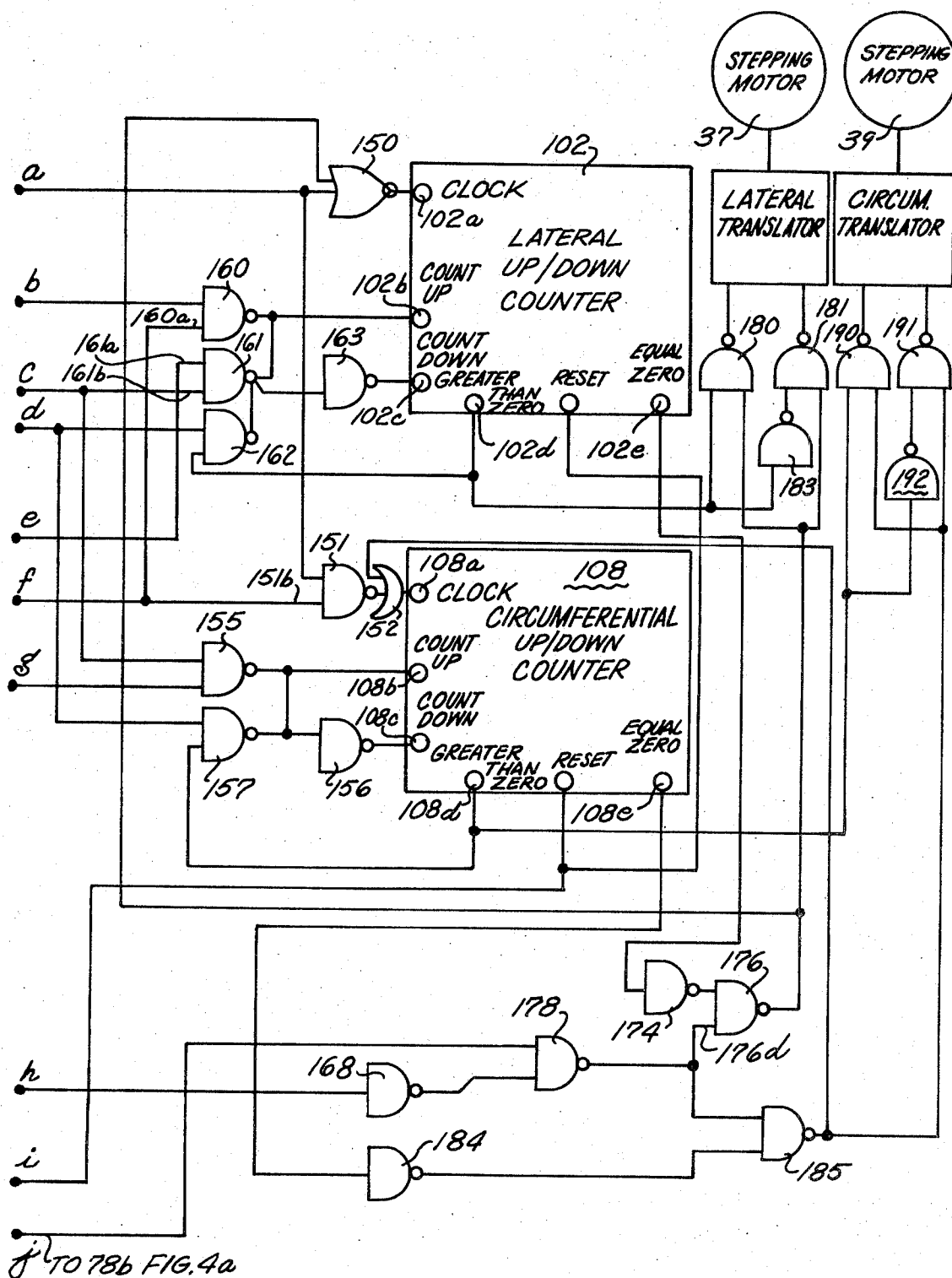


FIG. 4b

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CIRCUMFERENTIAL AND LATERAL WEB REGISTRATION CONTROL SYSTEM

In a rotary web-fed printing press, the printing cylinder is adjustable circumferentially to adjust the position of the image longitudinally of the web and axially to adjust the image laterally of the web. During printing in a multi-unit press, it is essential that the various colors printed onto a web by the units of the press be in proper registration both in a longitudinal direction and in a lateral direction if satisfactory color printing is to be achieved. Various systems have been devised for sensing longitudinal (circumferential) and lateral registration errors in a multi-color printing press to determine the circumferential and the lateral adjustments which must be made.

When the lateral and the circumferential registration errors are determined, the true circumferential or the true lateral error may not be correctly measured whenever there is an error in the other direction. The present invention provides a control system for a multi-color web-fed printing press in which the measured apparent error in one of the registrations due to an error in the other is corrected.

It is an object of the present invention to provide a web registration control system in which a first registration error of a web which is associated with a first coordinate direction is determined and combined with a second registration error of the web which is associated with a second coordinate direction in order to obtain an accurate registration indication.

It is also an object of the present invention to provide a multi-color web-fed digitally controlled registration system in which a first registration error which is associated with a first coordinate direction is determined by scanning register marks on a moving web and this error is digitally stored in a first counter and a second registration error which is associated with a second coordinate direction is measured by scanning second register marks and this error is digitally stored in a second counter with the count in the second counter being corrected by a factor corresponding to the count in the first counter in order to obtain a more accurate registration indication.

It is a further object of the present invention to provide a web registration control system in which the control mechanism for circumferential registration is controlled by pulsing a first counter which contains a circumferential count representing the circumferential registration error in which the pulses to the first counter are also applied to a second counter to establish a correction in the second counter which is used to indicate lateral registration error for apparent error in the lateral representation introduced by the circumferential misregistration.

It is an additional object of the present invention to provide a multi-color web registration control system in which a single sensor is utilized to sense circumferential and lateral registration marks and a gating and control circuit is employed to gate both circumferential and lateral registration error information to a circumferential and to a lateral storage means, respectively.

By way of illustration, a specific embodiment of the present invention is disclosed in the following specification and the accompanying drawings in which:

FIG. 1 is a diagrammatic view which shows a web passing through a multi-color web-fed printing system

which has individual lateral and circumferential correction means for each color printing press of the system;

FIG. 1a is an enlarged portion of the web of FIG. 1 which shows the register marks which are employed for registration compensation;

FIG. 2 is a diagram showing the relative position of a reference and a control register mark when the diagram of FIG. 2a applies;

FIG. 2a is a diagram showing wave forms for a leading circumferential registration error;

FIG. 3 is a diagram showing the relative position of a reference and a control register mark when the diagram of FIG. 3a applies;

FIG. 3a is a diagram showing wave forms for a lagging circumferential registration error; and

FIGS. 4a and 4b are block diagrams of a portion of the control system.

A perfecting multi-color web-fed printing press is shown diagrammatically in FIG. 1 in which lithographic perfecting press units 12, 14, 16 and 18 are employed to successively print different colors on the web 10 which moves through the printing press in the direction indicated by the arrow 20. The press units each comprise upper and lower printing units designated by A and B appended to the reference character for the press unit and each printing unit has a plate cylinder 21 and a blanket cylinder 22 which prints onto the web. The conventional dampeners and inkers are not shown.

A perfecting multi-color web-fed printing press is shown diagrammatically in FIG. 1. The press includes a plurality of lithographic perfecting press units 12, 14, 16 and 18 which print different colors onto a web 10 as the web moves through the press in the direction indicated by the arrow 20. The press units each comprise upper and lower printing units designated by the reference character for the press unit with the letters A and B appended thereto for the upper and lower units, respectively. Each printing unit has a plate cylinder 21 and a blanket cylinder 22. The conventional dampeners and inkers have not been illustrated in the drawings.

As is well known to those skilled in the art, it is necessary for the images printed by the units which print on one side of the web to be in accurate registration with each other. Also, it is often desirable to have the images printed on the opposite sides of the web registered with each other so that the images will appear in the proper location when the web is cut and folded. Conventionally, to adjust the registration of images, each printing unit of the press is provided with some type of mechanism for advancing or retarding the angular phase of the printing cylinders relative to the web (circumferential registration) and a mechanism for shifting the cylinders axially (lateral registration).

In the practice of the present invention, register marks are printed by each of the printing units for use in determining the accuracy of registration of the images and making the adjustments necessary to maintain registration. The register marks printed by the units include circumferential and lateral register marks and for all the units, except unit 18A, the circumferential marks are designated by the reference character 24a and the lateral registration marks are designated by the reference character 24b. The register

marks printed by the upper unit 18A are used as reference registration marks and have been designated by the reference character 28a for the circumferential register mark and 28b for the lateral registration mark. The registration marks of the different units are printed along a line which extends transversely of the web and the marks printed by each unit are sensed by a corresponding photoelectric sensor. The sensors for the upper units are designated by the reference characters 36a, 36b, 36c, 36d, while those for the lower printing units have not been shown. It will be understood, however, that they are located on the underside of the web and that they operate in a manner similar to the sensors shown for controlling the registration of the lower printing units.

As the register marks printed by the printing units pass beneath the corresponding photoelectric sensor, electric pulse signals are generated and applied to a control system 40. The pulse signals are generated by the register mark when it passes the photoelectric sensor and changes the amount of reflected light received by the sensor from a light source 25. The control system 40 determines whether or not the reference marks printed by the printing unit 18A pass the sensor 36a ahead, behind or at the same time that the registration marks printed by the other printing units pass the corresponding sensor for those units. If a register mark from one of the other units leads or lags the reference mark from the printing unit 18A, a registration error exists and the control circuitry 40 determines the magnitude and direction of the registration error as well as whether the error is circumferential, lateral, or both.

Following the determination of the magnitude and direction of the circumferential and lateral registration errors by the control system 40, circumferential and lateral control signals are provided to correct the error in registration. Each printing unit has motor control circuits 33 and 35 which control stepping motors 37 and 39, respectively. The stepping motors 37 are circumferential correction stepping motors while the stepping motors 39 are lateral misregistration correction stepping motors. The stepping motors 37 and 39 for each unit respectively drive gearing systems 41 and 43 for correcting for circumferential and lateral misregistration, respectively. The gearing systems 41 and 43 are shown diagrammatically in FIG. 1 and a detailed description of these gearing systems will not be undertaken since they are well known to those skilled in the art. Moreover, only the stepping motors and gearing for the upper printing unit have been schematically shown but it is to be understood that the lower units have corresponding motors and gearing units.

The manner in which the circumferential and lateral registration errors is measured is described below with reference to FIGS. 2, 2a, 3 and 3a. FIGS. 2 and 2a illustrate the technique by which the circumferential and the lateral registration error for a printing unit is determined when the circumferential register mark 24a of printing unit 12A leads the circumferential reference register mark 28a and the lateral register mark 24b of the unit 12A lags the lateral reference register mark 28b. The pulse wave forms of FIG. 2a correspond to the positions of the reference and unit register marks of FIG. 2 for this condition with voltage extending in the vertical direction and time extending in the horizontal direction in the figure.

When the type of error illustrated in FIGS. 2 and 2a occurs, the photoelectric sensing device 36b, which senses along the line C of FIG. 2, will first sense the presence of the circumferential register mark 24a and, following the sensing of the register mark 24a, the sensing device 36a, which senses along the line C, will sense the presence of the circumferential reference register mark 28a. Since the unit register mark 24a was sensed prior to the sensing of the reference register mark 28a, the control system 40 of FIG. 1 will determine that a leading circumferential error has occurred. The time that elapses between the sensing of the control register mark 24a and the sensing of the reference register mark 28a indicates the circumferential registration error which corresponds to the distance $d1$ of FIG. 2. The pulses from the sensor 36a in response to the reference marks 28a, 28b are illustrated in displays A and B of FIG. 2a and designated by the reference numerals 50 and 52, respectively. Similarly, the pulses from the sensor 36b are shown in displays C and D of FIG. 2a and designated by the reference numerals 54 and 56, respectively. The time period which elapses between the leading edges of the circumferential pulse 54 from the sensor 36b and the reference circumferential pulse 50 from the sensor 36a is illustrated by a "pulse" 58 shown in display E of FIG. 2a, the duration of which is proportional to the distance of FIG. 2.

This pulse is utilized to open a pulse gate to pulse a counter in the control system 40 to establish the circumferential error therein prior to the sensing of the lateral reference register mark 24b.

Following the sensing of the circumferential register marks 24a, 28a, the sensors 36a, 36b will then operate to sense the lateral register marks 28b, 24b, respectively. If as in the assumed case, there is a leading circumferential error, the control register mark 24a would lead the reference mark 28a and this would give a false indication of lateral misregister since the lateral registration mark 24b will pass the sensor 36b before the lateral reference register mark 28b passes the sensor 36a. Accordingly, even if there is no lateral registration error, the sensors will see an apparent error caused by the circumferential error. If in fact there is a lateral error, for example, a lateral error which would shift the marks 24a, 24b for the unit 12A to the solid line position shown in FIG. 2, the reference mark for lateral registration 28b will produce pulse 52 (see display B in FIG. 2a) which occurs in time ahead of the pulse 56 (see display D in FIG. 2a) which occurs when the mark 24b printed by the unit 12A reaches the sensor 36b. Accordingly, the apparent lateral error will be decreased and will be as shown by pulse 60 in display F in FIG. 2a. To obtain the true lateral error in this case, the circumferential error must be added to the apparent lateral error as represented by the pulses 64a and 64b in display G in FIG. 2a.

The control system 40 algebraically adds the circumferential error, which is represented by the "pulse" 58, to the apparent lateral error, which is represented by the "pulse" 60 to obtain the true lateral error, which is represented by the combined "pulses" 64a, 64b. In other words, the true lateral error is represented by the sum of the distances $d1$ and $d2$ of FIG. 2, and not merely by the distance $d2$, and this distance is measured by the control system 40.

In FIGS. 3 and 3a, a lagging circumferential misregistration error and a lagging lateral misregistration error are illustrated. In this instance, the sensing device 36a will sense the reference register mark 28a and produce pulse 50' (see display A in FIG. 3a) prior to the sensing of the control register mark 24a by the sensing device 36b and the occurrence of pulse 54' in display C in FIG. 3a. The time between pulses 50' and 54' is represented by the "pulse" 58' which extends between the leading edge of the pulse 50' and the leading edge of the pulse 54' and the width of the pulse 58' represents the lagging circumferential error that corresponds to the distance d1 of FIG. 3.

The lateral reference register mark 28b is sensed along the subtract line C by the sensing device 36a to produce the pulse 52' and the lateral control register mark 24b is sensed along the line C' by the sensing device 36b to produce the pulse 56' at a time subsequent to pulse 52'. The duration of the "pulse" 60' of FIG. 3a which extends between the leading edge of the pulse 52' and the leading edge of the pulse 56' represents the apparent lateral registration error. Since the true lateral error in FIG. 3 is the distance d2 minus the distance d1, the control system 40 must subtract the circumferential registration error, as represented by the "pulse" 58' from the apparent lateral error, as represented by the "pulse" 60', in order to obtain the true lateral registration error which is represented by the "pulse" 62'.

The control circuitry 40 includes a lateral error counter 102 and a circumferential error counter 108 for each of the upper and each of the lower printing units. The counters for the printing unit 12A are shown in FIG. 4b. It will be understood that there are no counters for the last printing unit since it is the printing unit which prints the reference register marks 28a, 28b.

When the circumferential reference mark 28a arrives at its sensor 36a before or after the circumferential mark 24a printed by the printing unit 12A, pulses will be applied to the circumferential counter 108 to indicate the magnitude of the circumferential error. These pulses will also be applied to the lateral counter 102 to correct for the apparent error which will occur in the lateral register as described above. Similarly, when the lateral register reference mark 28b arrives at the sensor 36a before or after the lateral register mark printed by a particular unit, pulses will be applied to the lateral register counter 102 for that unit to indicate the magnitude of the apparent lateral error.

The counters 102, 108 shown in FIG. 4b are for the printing unit 12A and the description will proceed with reference to that unit. When the reference register mark 28a arrives at the sensor 36a before the register mark 24a printed by the printing unit 12A, the reference circumferential register mark 28a will activate gating to allow pulses from a pulse generator 73 to be applied to the circumferential counter and to the lateral counter. The pulses from the pulse generator 73 will be applied to the counters until the circumferential register mark 24a printed by the printing unit 12A arrives at the sensor 36b. At this time the pulses to the counter 108 and to the lateral counter 102 will be terminated in response to the sensing of the circumferential register mark. If the circumferential register mark printed by the printing unit 12A arrives at the

sensor 36b before the reference circumferential register mark arrives at the sensor 36a, the register mark 24a will initiate the pulses to the counters and the reference mark 28a will terminate the pulses. Consequently, it can be seen that the number of pulses supplied to the counting means 108 and the counting means 102 will be indicative of the magnitude of the circumferential error.

Similarly, when the lateral register mark 28b arrives at the reference sensor 36a before or after the time that the lateral register mark printed by the printing unit 12A arrives at the sensor 36b, the pulses from the sensor are utilized to initiate and stop pulses to the lateral error counter 102. The pulses will be applied to the error counter 102 to effect counting in one direction if the reference pulse arrives first and to effect counting in the opposite direction if the lateral register mark 24b printed by the printing unit 12A arrives first.

In accordance with the preferred embodiment of the present invention, the registration of the units are not checked every cycle but are periodically checked every Nth cycle, for example every eight cycles. In the illustrated embodiment, the press has a second pulse generator 78 which generates one pulse for every press revolution with this pulse appearing on output 78a. The pulse generator 78 also generates a much higher number of pulses each revolution, for example 240 pulses, and these pulses appear on an output terminal 78b.

The revolution output 78a is connected to a dividing circuit 79 which provides a signal on an output connection 79a every Nth revolution. It is during the revolution when this output signal is present that the control circuitry 40 may respond to signals from the sensor for the register marks. When there is an output signal on the output 79a from the counter 79, the output pulses 78b are applied through a gate 82 to a counter 84 for selecting the period during the revolution when the circuitry is capable of responding to the sensors. The counter 84 is a multi-stage binary counter and the third stage of the counter has been designated by the reference numeral 90 and the fourth stage by the reference numeral 92. The counterstages each have Q and $\bar{Q}$ outputs which respectively have a logic 1 signal thereon when the stage is set and reset, respectively.

After the counter 79 has received N pulses a signal appears during the Nth revolution on its output 79a and this activates a one-shot multivibrator 85 to provide a signal to a flip-flop circuit 93 provided by two cross-connected NAND gates 94, 96. The reset input of the flip flop is provided by one of the inputs of the NAND gate 94 and this input normally has a logic 1 input supplied by the $\bar{Q}$ signal from the binary stage 92. As will be appreciated by those skilled in the art, the binary stage 92 normally has a logic 1 output on its Q output unless it has been set in response to pulses applied to the counter. It requires six pulses to set the binary stage 92 when the counter starts counting from 0 where all stages are in their reset states. The output from the one-shot multivibrator 85 is applied to the 1 input of the NAND gate 96 through an inverter 97 so that there is normally a logic 1 input from the divide by N circuit 79 to the NAND gate 96. This input coupled with the logic 1 input to the NAND gate 94 from the binary stage 92 normally maintains a 0 logic level on the output 96c from the NAND gate 96 which is the output of flip flop

93. When the signal appears on the output of the divide by N circuit 79 and triggers the one-shot multivibrator 85, the input to the NAND gate 96 becomes a logic 0 and the output from the NAND gate becomes a logic 1.

A logic 1 on the output of the NAND gate 96 of window flip flop 93 conditions inputs 98a, 104a of circumferential and lateral cycle gates 98 and 104, respectively, to be activated in response to logic 1 inputs on their second terminals 98b, 104b, respectively. The gates 98, 104 direct the application pulses to the counters 102, 108 during the portions of the cycle for sensing circumferential and lateral errors, respectively, and when the gate 98 is activated pulses are applied in response to the sensing of an error to both the circumferential counter 108 and the lateral counter 102. When the gate 104 is activated, pulses are only applied to the lateral counter. The gate 98 for conditioning both counters 102, 108 to receive pulses has its second input 98b conditioned by the Q by the third stage 90 of the binary counter 84. Consequently, the gate 98 is conditioned while the counter has a count of 0 to 3 since the third stage of the counter is set in response to the fourth pulse applied to the counter input when the counter starts counting from 0. When the third stage 90 is set in response to the fourth pulse, the logic 1 is lost on the input 98b and established on the input 104b of the gate 104 which is connected to the Q output of the binary stage 90. The conditioning of the gate 104 with the logic 1 conditions the gating for the lateral counter so that it may receive pulses if an error is sensed by the sensors 36a, 36b.

The logic 1 output of the window flip flop 93 formed by the gates 94, 96 is also applied to the reset terminals of a pair of direction flip flops 114, 115 formed by NAND gates 116, 120 and 121, 122, respectively, for determining the sense of the error, i.e., whether the error is leading or lagging. As long as the inputs to the NAND gates 116, 121 from the window flip flop 93 is at a 0, the flip flops 120, 121 will set and reset with a change in signal on inputs 120a, 122a to the gates 120, 122, respectively. However, the inputs to the gates 120, 122 on the inputs 120a, 122a are clamped at a high level except during the window period by the output of gates 123, 125 between the circuits 74, 76. The gates 123, 125 are NAND gates so that the gates have a high output as long as one of the inputs is low. One of the inputs of each gate 123, 125 is connected to one of the pulse shaping circuits 74, 76 for the sensors 36a, 36b, respectively, while the other input is connected to the output 96a of the window flip flop 93 so that a high level output is maintained to the NAND gates 120, 122 as long as a logic 0 appears on the output 96a. Consequently, the output from the flip flop 93 renders the flip flops 114, 115 nonresponsive to signals from the sensors 36a, 36b except during the window period and the flip flops are held in a condition where there is a logic 0 on the outputs 122c, 120c of the flip flops 115, 114, respectively, and a logic 1 on the outputs 116c and 121c of the flip flops 114, 115, respectively.

When the logic 1 appears on the output 96a from the flip flop 93 to inputs 116a, 121a of the NAND gates 116, 121, there will be no change in the NAND gates of either of the flip flops 114, 115 until the logic 1 from a sensor changes to a logic 0. This is true because the gates 116, 121, each have a logic 0 on an input from the

associated NAND gate which holds the output of gates 121, 116 at a logic 1 regardless of the logic levels on inputs 116a, 121a from the window flip flop. However, when there is a logic 1 on the inputs 116a, 121a and the signal from one of the sensors 36a, 36b changes to a logic 0, the corresponding flip flop 114 or 115 will switch states. If the input to NAND gate 122 from sensor 36a changes to a logic 0, the output 122c of NAND gate 122, and of the flip flop 115, changes to a logic 0 which in turn will apply a logic 1 to one input of the NAND gate 121 to change the flip flop output 121c from a logic 1 to a logic 0. Since the NAND gate 121 now has two logic 1 inputs, the second input to the NAND gate 122 is a logic 0. Consequently, any change in the change in level on the input 122a to the signal on input 122a to the flip flop 115 will not change the state of the gate 122 or the flip and the flip flop remains set for the entire window period, i.e., as long as a logic 1 is maintained to the gate 121 from the flip flop 93. Consequently, if the sensor 36a first senses the mark printed by the printing unit 18A, the flip flop 115 will change its state so that a logic 1 appears on its output 122c and a logic 0 appears on its output 121c. The control flip flop 114 will remain in the same state that it was at the beginning of the window period and will have a logic 0 on its output 120c and a logic 1 on its output 116c. In this condition the logic 1's on the output 116c and the output 122c from the flip flops 114, 115, respectively, are utilized to activate a NAND gate 126 of a pair of direction sensing NAND gates 124, 126 to change the output of the NAND gate 126 from a 1 to 0. Normally, the NAND gates 124, 126 have a 1 output since the NAND gates 124 have respective inputs connected to the outputs 120c, 122c of the flip flops 114, 115 which normally have logic 0 thereon and respective inputs connected to the outputs 121c, 116c, respectively, which normally have logic 1's thereon. Consequently, when one of the flip flops 114, 115 changes states, for example flip flop 115, the input therefrom to gate 126 changes to a logic 1 to change the output 126c from the gate to a logic 0. The input to gate 124 from flip flop 115 also changes from a logic 1 to a logic 0 but this does not activate the gate since its input from the gate 120 of flip flop 114 is a logic 0.

The direction NAND gates 124, 126 have their outputs 124c, 126c connected to inputs of a direction sensing flip flop 129 made up of NAND gates 128, 130. The output 130c of the NAND gate 130 is used to signal whether the error is leading or lagging, that is whether the reference control mark or the reference register mark was first sensed by its respective sensor. In the illustrated embodiment if there is a logic 0 on the output 130c it signifies that the mark printed by the printing unit preceded the mark printed by the reference sensor and that the error is therefore leading while if a logic 1 appears it indicates the contrary.

The outputs of the direction sensing gates 124, 126 are also used to gate pulses to the counters when an error is sensed. The outputs 124c, 126c of the direction sensing gates 124, 126 are applied to the inputs of the NAND gate 138. Normally, the NAND gates 124, 126 supply logic 1 signals to the NAND gate 138 and this normally provides a logic 0 on the output 138c from the NAND gate 138. The logic 0 on the output of NAND gate 138c is applied to one input 142a of a NAND gate

142 which has its second input 142b connected to the output of the pulse generator 73. Since the input from the NAND gate 138 to the pulse gate 142 is normally a logic 0 because both NAND gates 124, 126 have a logic 1 on their outputs, when one of the flip flops 114, 115 is activated by a signal from its sensor, the change in input from the gate 124, or the gate 126 depending on which of the flip flops is first activated from a logic 1 to a logic 0 causes the output 138c from the gate 138 to change to a logic 1 to supply a logic 1 to one input of the pulse gate 142. Consequently, as the input of the pulse gate 142 which is connected to the pulse generator 73 changes level, the output of the gate 142 will also change level and the pulses will be transmitted by the gate until the output of the gate 138 is again a logic 0. The output of the gate 138c will return to a logic 0 when the second register mark passes its sensor.

In the assumed case where the register mark from the printing unit 12A passes its sensor 36b after the reference register mark passes its sensor 36a, the arrival of the register mark from unit 12A at the sensor 36b will cause the activation of the flip flop 114 to change the logic 0 on its output 120c and the logic 1 on its output 116c to logic 1 and logic 0, respectively. This changes the input from the flip flop 114 to the NAND gate 126 from a 1 to a 0 to return its output 126c to its 1 condition. Also, the inputs to the NAND gate 124 now have a logic 1 and a logic 0 on its inputs since the flip flop 115 which was initially switched in response to the pulse from the sensor 36b to a state where there was a logic 0 on the output 121c to provide two logic 0's to NAND gate 124. When the flip flop 114 is triggered to change its output from gate 120c to gate 124 from a 0 to a 1, the NAND gate 124 now has a logic 1 input and a logic 0 which still provides a logic 1 output which is the same as the output for a normal condition. This logic 1 with the logic 1 output of the NAND gate 126 because of the logic 0 from the flip flop 114 and the logic 1 input from the flip flop 115 provides two logic 1 inputs to the gate 138 and causes a logic 0 to appear on the output of the NAND gate 138 closing the pulse gate 142. Consequently, it can be seen from the above description that for the described situation, pulses will be passed by the pulse gate 142 only during the time period between the pulses from the sensors 36b, 36a.

It will also be readily appreciated that if the mark from the printing unit 12A arrives at its sensor 36b before the reference mark arrives at sensor 36a to indicate a leading error, the flip flop 114 will be first activated to change the input to the NAND gate 124 so that both of its inputs are a logic 1 and its input to gate 126 so that both of its inputs are logic 0. When this happens, the output of the NAND gate 138 will change from a 0 to a 1 and open the pulse gate. Also, the connection from the NAND gate 124 to one input of the NAND gate 128 of the direction sensing flip flop 129 will change from a 1 to a 0. A changing of the input 128 from a normally 1 to a 0 will cause a switching of the flip flop if the flip is in a state where there is a logic 0 on the output from gate 128 and logic 1 from gate 130. With the NAND gate 128 of the flip flop in a state with a 1 input from the NAND gate 130 and from the gate 124, when the NAND gate 124 changes its output from a 1 to a 0, the output of NAND gate 128 of flip flop 129 changes to a 1 and this changes the output 130c from

the gate 130 from a 1 to a 0. Consequently, if the direction sensing gate 124a is changed to have a logic 0 on its output to indicate a leading error, the direction sensing flip flop changes from its state to have a 1 on its output 128c and a 0 on its output 130c. If once set in this state, it will so remain until the gate 126c is activated to establish a logic 1 to gate 130 and a logic 1 on output 130c of the gate.

In the assumed case, when the mark 24a of unit 12A passes the sensor 36b, the output from the sensor changes the flip flop 114 to provide a logic 1 on its output 120c and a logic 0 on its output 116c. When the output from the NAND gate 116c of flip flop 114 changes from a 1 to a 0, it switches the output of the NAND gate 126 to a 1. Since the NAND gate 124 also has a logic 1 output at this time, the pulse gate 138 will be switched to a logic 0 to close the pulse gate 142.

From the foregoing description it can be seen that the NAND gate 124 has one input connected to the flip flop 114 which normally receives a logic 0 from the flip flop. A second input of the NAND gate 124 is connected to the flip flop 115 and normally has a logic 1. Similarly, the NAND gate 126 has an input connected to the flip flop 114 to have a normal logic 1 input and an input connected to the flip flop 115 to normally have a logic 0. Consequently, if one of the flip flops changes state, one of the NAND gates 124 will have a logic 1 applied to both inputs and the other NAND gate will have logic 0 applied to both inputs. If the flip flop 114 changes state, the NAND gate 124 will have both inputs at a logic 1 level while if the flip flop 115 first changes state the NAND gate 126 will have both inputs at a logic 1 level. The output of a NAND gate is not changed when a logic 0 is maintained on one of the inputs even though the other input changes from a logic 1 to a logic 0. Consequently, if the flip flop 114 is first activated in response to a register mark, the NAND gate 124 will be activated to change its output from a logic 1 to a logic 0 while the NAND gate 126 will not be activated in response to the change of its input from the flip flop 114 from a 1 to a 0. Conversely, if the flip flop 115 is activated before the flip flop 114, the NAND gate 126 will have logic 1's on both of its inputs and will be activated to change its output from a logic 1 to a logic 0 while the NAND gate 124 will not be activated. However, when the other flip flop is activated in either case, the NAND gate 124 or 126 which had been activated will lose the logic 1 from the flip flop which is activated second to return its output to a logic 1. The other NAND gate will not be activated because when only one of the flip flops 114, 115 is switched in response to a signal, the nonactivated one of the gates 124, 126 has two logic 0 inputs and the changing of one of the logic 0 to a 1 does not alter the output of the gate.

It will be noted that once one of the flip flops 114, 115 is switched to change its state, the inputs from the sensor to the flip flop loses control since the gate receiving a signal from the flip flop 95 has two logic 1 signals applied to its inputs to maintain its output at a logic 0. In the case of the flip flop 114, this maintains one input to the NAND gate 120 at a logic 0 regardless of the level on the input from the sensor 36a. Similarly, when the flip flop is switched, the NAND gate 121 has two logic 1 signals on its inputs and its output is a logic

0 so that the level on the input 122a to the gate 122 has no effect on the output of the gate.

After the flip flops 114, 115 have been set it is necessary to reset the flip flops before a next sensing operation. This is done by changing the level from the direction flip flop 93 to the inputs 116a, 121a of the flip flops 114, 115 to a logic 0. When these inputs are changed to a logic 0 with logic 1 signals on their inputs 120a, 122a, the flip flops reset with the gates 122, 120 having two logic 1 signals applied thereto to provide logic 0 signals from the NAND gates 120, 122 to the direction sensing gates 124, 126.

Since the circumferential register marks are to be sensed first and then the lateral register marks, it is necessary to reset the flip flops and the circuitry after the sensing of the circumferential register mark and the measurement of any error by opening the pulse gate 142 for a time corresponding to the error. The circuitry is reset by a one-shot multivibrator 149 which is connected to the Q output of the third stage 90 of the binary counter 84. Consequently, when this output changes from a logic 1 to a logic 0, the one shot is activated to change its output from a logic 1 to a logic 0. The Q output of the one shot is connected to the output 96c of the window flip flop 93 and when it changes to a logic 0 it changes the signal from the flip flop 93 to a logic 0 to reset the flip flops 114, 115. After the resetting, the circuit is then in condition to sense the lateral register marks and will do so until the fourth stage flip flop 92 is activated to lose the logic 1 signal on its Q output. At this time, the window flip flop 93 is reset and the window signal is lost to the flip flops 114, 115 and the gates 123, 125 are clamped in a condition where they will not respond to the sensors 36a, 36b.

As explained hereinbefore, it is necessary to correct the apparent lateral error for any circumferential error. Consequently, pulses which indicate the circumferential error are applied to the lateral up-down counter as well as to the circumferential up-down counter. To this end, the pulse gate 142 is connected directly to the clock terminal 102a (FIG. 4b) of the lateral up-down counter 102 through an OR gate 150 so that any pulses which are passed by the pulse gate will be applied to the lateral up-down counter. These pulses are also applied to the clock terminal 108a of the circumferential up-down counter 108 through a NAND gate 151 and an OR gate 152. The NAND gate 151 normally has a logic 0 on an input 151b whose logic level is controlled by the output of the circumferential cycle gate 98 (FIG. 4a). The output of the gate 98 is applied to the input 151b through an inverter gate 153 and this gate will have a logic 1 thereon for the period during which the binary counter 84 counts from 0 to 4. On the fourth count, the third binary stage 90 is triggered from its $\bar{Q}$ condition to its Q condition so that the output from the circumferential gate 98 becomes a logic 1 to change the output of the inverter gate 153 to a logic 0 which renders the circumferential gate 151 for counter 108 nonresponsive to pulses from the pulse generator 142. Consequently, the circumferential register 108 can only be stepped from the pulse gate 142 during the period that the counter is counting from 0 to 4 and on the occurrence of the fourth pulse, the circumferential gate is closed. The timing is set so that the register marks will normally be passing the sensors during this sensing period.

The direction of counting in the counters 102, 108 in response to an error pulse is determined by a condition of the flip flop 129. If the reference sensor arrives at the sensor 36a in advance of the register mark printed by the unit 16A, the flip flop 129 will have a logic 1 on its output 130c to indicate that the printing unit is lagging the reference mark. This logic 1 is applied to the input of a NAND gate 155 (FIG. 4b) to change its output from a logic 1 to a logic 0 since the other input of the NAND gate 155 is connected to the window flip flop 93. The output of the NAND gate 155 is connected to the count-up terminal 108b of the circumferential counter 108 and to the countdown terminal 108c of the up-down counter through an inverter gate 156. Consequently, when the gate 155 has a logic 1 on its output the counter counts in an up direction and when it has a logic 0 on its output the counter counts in the down direction.

A second NAND gate 157 has its output wired to the output of the NAND gate 155 so that these NAND gates constitute a wired OR arrangement. In a wired OR arrangement, one of the gates is maintained with a logic 1 on its output and the other gate then assumes control and the output from the two gates is either a logic 1 or a logic 0 depending on the output of the other gate. The gate 157 at this time will have a logic 0 on one input since the output 96c of the window flip flop 93 is connected to one input of the NAND gate 157 through an inverter NAND gate 158 (FIG. 4a) so that a logic 0 is applied to the NAND gate 157 during the window period. This assures a logic 1 on the output of the gate. The NAND gate has its other input connected to a greater than 0 terminal 108d to receive a 1 on the other input when the count in the counter is greater than 0. The purposes of gate 157 will be explained hereinafter.

As explained above, the output 130c of the flip flop 129 is used to control the direction of counting of the circumferential up-down counter 108. The output 128c of the flip flop 129 is similarly utilized to control the direction of counting of the lateral up-down counter and is connected to one input of a NAND gate 160 which has its output connected in a wired OR relationship with NAND gates 161, 162. The outputs of these NAND gates are connected directly to the count-up terminal 102b of the up-down counter 102 and to the countdown terminal 102c through an inverter 163. Consequently, the logic 1 or a 0 condition at the output of these gates causes the counter to count in different directions.

During the circumferential register mark sensing period, the NAND gates 161, 162 will have logic 1 outputs so that the NAND gate 160 controls the signal level to the count-up and countdown terminals 102b, 102c. The NAND gate 160 has an input 160a controlled by the output of the circumferential gate 98 so that when there is a logic 1 on the output of inverter 153 to signify the circumferential register mark sensing period, the input to NAND gate 160 is a 1 level so that the input to input 160b of NAND gate 160, which is from the direction sensing flip flop 129, controls the output of the NAND gate 160. The output of the NAND gate 160 will have a logic 1 if the direction sensing flip flop indicates a lagging circumferential error and a logic 0 if a leading error is indicated since the gate 128c of flip flop 129 has a 0 output for a lagging error and a 1 output for a leading error.

As will be understood from the foregoing, the pulses which are added to the circumferential counter when error occurs are also added to the lateral updown counter to count the counter in the proper direction to correct the apparent error which will occur in the counter because of the circumferential error. For example, since the lateral up-down counter 102 is normally counted in an up direction when there is a lateral error caused by the mark printed by the printing unit 16A lagging the reference mark printed by the last unit 18A, the signal from the NAND gate 160 conditioned by the circumferential gate will cause the pulses added during the circumferential gate sensing period to count the counter in a down direction in a situation where the circumferential mark printed by the printing unit 16A is lagging the reference mark and the input to the direction count gate 160 from the direction flip flop 129 is a logic 0. Then when the apparent error of lateral register caused by circumferential misregistration is sensed during the lateral sensing period, the direction count gate 161, as is further explained hereinafter, will cause the counter to count in an up direction to subtract the same error from the counter and to arrive at a zero error in the absence of any actual lateral misregistration.

When the third binary stage 90 is triggered to its Q condition on the fourth pulse applied to the counter after the start of the counter period, the logic 1 on the Q output of the stage is applied to the cycle NAND gate 104 to render the lateral error circuitry effective during a lateral error sensing period. The output of the NAND gate 104 is connected through an inverter 165 to one input 161a of the NAND gate 161, the NAND gate having its input 161b connected to the output 130c of the direction sensing flip flop 129. At this time, the NAND gates 160, 162 will have a logic 1 output because of the logic 0 on the output of the inverter 153 from the circumferential gate 98 and the logic 0 on the output of NAND gate 158 whose input is connected to the window flip flop 93. Accordingly, the logic level on the output of the NAND gate 161 controls the direction of counting on the up-down counter during the lateral error sensing period and this level is controlled by the signal level on the output 130c of the direction sensing flip flop 129. Consequently, during the error sensing period, any pulses which are passed by the pulse gate 142 and applied to the clock terminal 102a of the up-down counter 102 will count the counter in a direction determined by the direction sensing flip flop 129. If the error is a lagging error, the output of gate 161 is a logic 0 and the counter counts down while if a leading error, the counter counts up. These pulses are not applied to the circumferential up-down counter because the NAND gate 151 now has a logic 0 on the input controlled by output of the circumferential cycle gate 98.

The lateral error sensing period will continue from count 4 of the counter 84 until the binary stage 90 of the counter is reset which will occur on the eighth count after the start of the counting period. The resetting of the binary stage 90 effects a setting of the binary stage 92 to cause the logic level on the Q binary output stage 92 to change from a logic 1 level to a logic 0 level. When this output changes to a logic 0 level, a logic 1 signal therefrom to the NAND gate 94 of the

window flip flop 93 changes to a logic 0 to reset the flip flop and change the output of the NAND gate 94 to a logic 0 which in turn changes the output 96c from the NAND gate 96 to a logic 0 to provide a logic 0 output to the control circuitry from the window flip flop 93. This logic 0 prevents the circuitry from responding to the sensors as hereinbefore described and since the pulse gate 142 has been closed, no pulses can be applied to the up-down counters until the next window period is initiated by the divide by N circuit 79.

Following the completion of the 16th count the logic 1 signal to the NAND gate 94 of flip flop 93 from the Q terminal of the binary stage 92 of the counter 84 will be re-established but this will not effect the window flip flop 93 since at that time the NAND gate 96 of the flip flop will have a logic 0 on its input to the gate 94 so that the signal level on the input of the NAND gate 94 connected to the Q terminal of the binary stage 92 of the counter 84 has no effect on the flip flop so long as the level of signal to gate 96 from the one-shot multivibrator remains at a logic one.

After the window period, the up-down counters for the unit 16A are to control the corresponding stepping motors 37, 39 to correct for any misregister. When a count is registered in one or both of the counters after the window period, pulses are supplied to the corresponding stepping motor and for each pulse applied to the stepping motor, a corresponding pulse is applied to the counter to count the counter toward its zero or middle count. When the counter is at 0, gates are closed to stop the application of pulses to the stepping motor and correction has been effected.

To this end, the lateral up-down counter has an equal zero terminal 102e and the circumferential updown counter 108 has an equal zero terminal 108e. The equal zero terminal 102e is connected through an inverter 174 to one input of a NAND gate 176 whose output is connected to the OR gate 150 for the clock terminal 102a of the lateral up-down counter. When the count in the lateral up-down counter is equal to 0, a logic 1 appears on the terminal 102e and when it is different from 0, a logic 0 appears on the terminal. When a logic 0 is on the terminal 102e, the NAND gate 176 is conditioned to pass pulses applied to its input 176b. The pulses are applied to the input 176b from the pulse generating terminal 78b of the pulse generator 78 through a NAND gate 178. One input of the NAND gate 178 is connected to the terminal 78b while the second input of the NAND gate 178 is controlled by the window flip flop 93 which has its output 96c connected to input of the gate 178 through an inverter 168. Consequently, the input of the NAND gate 178 controlled by the window flip flop has a logic 1 thereon when the window is closed and a logic 0 thereon when the window is opened. This prevents pulses from being applied to the stepping motor 37 during the window period. When the window period is over and there is a count in the counter, pulses will be applied to the NAND gate 176 and in turn to the OR gate 150 and the clock terminal of the lateral up-down counter 102 if there is a count in the counter so that the logic level on the equal to zero terminal 102e is a logic 0.

The pulses from the NAND gate 176 are also applied to stepping motor gates 180, 181 for operating the stepping motor in a clockwise and a counterclockwise

direction, respectively. If the count in the up-down counter is greater than 0, a logic level 1 appears on its greater than 0 terminal 102d, and this terminal is connected to one input of the NAND gate 180 so that pulses from the NAND gate 176 will be applied to the stepping motor circuitry to step the motor in a clockwise direction if the count in the counter is greater than 0. The greater than 0 terminal 102d is also connected to one input of the NAND gate 181 through an inverter 183 so that if the count is not greater than 0 and a logic 0 appears on the terminal 102d, a logic 1 is applied to one input of the NAND gate 181 from the gate 183 and pulses from the pulse gate 176 will be passed from the pulse gate to the motor control circuitry to step the motor in a counterclockwise direction. Consequently, it can be seen that if, after the window period, there is a count in the lateral counter, the pulse gate 176 is opened by the signal on the equal zero terminal, and the pulses are applied through either the clockwise gate 180 or the counterclockwise gate 181, depending on the logic signal on the greater than zero terminal, to step the motor to correct the error and simultaneously the pulses from the gate are applied to the clock terminal 102a of the lateral up-down counter to step the counter to zero. When the counter is stepped to zero, the logic level 1 on the equal zero terminal 102e shuts the pulse gate 176 to pulses and the correction stops.

Similarly the equal zero terminal 108e on the circumferential up-down counter is connected through a NAND inverter gate 184 to one input of a NAND gate 185 for supplying pulses to the circumferential up-down counter and to the stepping motor 39 for effecting the circumferential correction when there is a count in the counter. The pulse gate 185 has its second input connected to the output of the gate 178 and its output connected through the OR gate 152 to the clock terminal 108a of the up-down counter and to clockwise gate 190 and counterclockwise gate 191 for transmitting pulses to the control circuitry for the stepping motor 39 to operate the stepping motor in a clockwise direction and counterclockwise direction, respectively. The greater than zero terminal 108d is connected to one input of the clockwise gate 190 to condition that gate to pass pulses when the count is greater than 0 and through an inverter 192 to an input of the NAND gate 180 for operating the motor in a counterclockwise direction to condition that gate to pass pulses when the count is less than 0. It can be seen that the circumferential up-down counter supplies pulses to the stepping motor to effect the correction in the same manner as was the case with the lateral up-down counter after the window period is over and an error has been registered. As in the case of the lateral up-down counter, when the circumferential counter is counted to 0, the logic 1 level on the equal zero terminal closes the pulse gate 185 to terminate the correction.

It will be noted that the greater than 0 terminal controls the direction of counting of the counter for the pulses from the gate 174 in the case of the up-down counter 102 and from the gate 185 in the case of the up-down counter 108. In the case of the lateral up-down counter, the greater than 0 terminal 102d is connected to one input of the NAND gate 162 which has a

logic 1 on its other input at the end of the window period. Since the NAND gates 160, 161 for controlling the direction of counting of the terminal have, at this time, a logic 1 on their outputs, the NAND gate 162 controls the direction of counting and its output has a logic 0 or a logic 1 thereon depending upon the signal on the greater than zero terminal. If a logic 1 appears on the terminal, the output of the NAND gate 162 is a logic 0 to cause the counter to count down. If the count in the counter is less than zero, the counter will count up since the greater than 0 terminal will have a logic 0 thereon to provide a logic 1 on the output of NAND gate 162 to effect a counting up of the counter.

It will be noted that the window period is initiated every N revolutions of the press by the one-shot multivibrator 85. This pulse is a pulse of short duration and is applied to reset all the counters except the divide by N counter as well as to set the window flip 93 to condition the control circuitry to respond to the sensor marks during the window period. The resetting of all of the counters at the start of the period assures a zero setting in all counters and, in the case of counter 84, proper cycling of the sensing periods. It will be further noted that the window flip flop is reset on the eighth count of the counter 84 and when reset to terminate the window period, the logic 1 input to the gate 96 of the flip flop 93 prevents changes in logic levels on the Q terminal of stage 92 of the counter from changing the flip flop 93 and the counter may be allowed to count continuously since it is reset at the beginning of each window period.

Changes in the cycle flip gating 98, 104 will have no effect if the counter operates outside of the window period.

From the foregoing, it can be seen that the lateral register mark has been compensated for the error introduced by circumferential misregister. It will be appreciated that the illustrated embodiment has added or subtracted pulses from the lateral counter from the time the pulses are applied to the circumferential counter, the circumferential pulses could be counted, the lateral pulses and an algebraic operation performed to obtain the true lateral error before the correction is made. Also, the circumferential error could be inserted into the counter by parallel techniques after it has been established in the circumferential counter or the circumferential correction could first be made and the feedback pulses for the circumferential correction applied to the lateral error counter to correct the lateral error of the counter at that time and a lateral correction made only if there is a count in the counter after the circumferential misregistration has been corrected.

From the foregoing, it will also be appreciated that if the marks are in registry, the flip flops 114, 115 will be switched simultaneously and when this happens the condition of the circuit will be the same as that for the circuit after both flip flops have been triggered in sequence when there is a misregister. It will be recalled that when both flip flops have been switched, the NAND gates 124, 126 each have a logic 1 on their output which closes the pulse gate 142.

Although the present invention has been described with reference to an embodiment thereof, it is to be understood that other embodiments and variations of the

present invention will be apparent to those skilled in the art and it is intended that these be included within the scope of the appended claims.

Moreover, in accordance with the preferred embodiment, the frequency of the pulses is dependent on the speed of the press so that the pulses to the counters for a given error will be constant. In the illustrated embodiment, an analogue signal representative of pulse speed is converted to a pulse train having a frequency dependent on the magnitude of the signal.

What is claimed is:

1. In a machine for operating on stock moving through the machine including first adjusting means for making a first adjustment of said stock relative to the operation performed by said machine on said stock with respect to a first degree of freedom, second adjustment means for making a second adjustment of said stock relative to the operation of said machine on said stock with respect to a second degree of freedom, sensor means for sensing a first register mark on said stock which indicates the relationship of said stock to the operation of said machine performed thereon with respect to said first degree of freedom and for sensing a second register mark on said stock to indicate the relationship of the stock to the operation of the machine with respect to said second degree of freedom, changes in the relationship of said stock to the operation of said machine with respect to the second degree of freedom effecting a change in the sensed relationship of said first mark independently of a change in the relationship of the machine and stock with respect to said first degree of freedom, and means responsive to said sensor means for ascertaining errors in the adjustment of said first and second adjusting means and providing first and second error signals for use in correcting said first and second adjusting means in dependency on the sensing of said first and second marks including means responsive to the sensing of said second mark for compensating said first error signal for error introduced by changes with respect to said second degree of freedom.

2. In a machine as defined in claim 1 wherein said means responsive to said sensor means comprises means responsive to said first and second marks for providing first and second control signals having a time duration in accordance with the magnitudes of error to be corrected by said first and second adjusting means, respectively, and integrating means responsive to the time duration of said first control signal to provide an error indication for said first adjusting means and responsive to the time duration of said second signal to compensate the said error indication to derive said first error signal in dependency on said first and second marks.

3. In a machine as defined in claim 2 wherein said integrating means comprises a pulse counter and means for transmitting pulses to said counter during said first control signal to register an error therein in dependency on said first mark and means for transmitting pulses during said second control signal to establish a count for compensating the count which is established during said first signal.

4. In a machine as defined in claim 3 wherein said counter is incrementally pulsed during said first and second control signals to establish a compensated error count therein.

5. In a machine as defined in claim 2 wherein said means responsive to said sensor means includes reference means providing reference signals for indicating the time said first and second marks are to be sensed when adjustment is proper, means for providing first and second pulse signals indicating the time difference between said reference pulse and said first and second marks and direction signals for indicating the lead-lag relationship of the marks and the reference pulses, and a counter for counting pulses in a direction depending upon said direction signals during the time duration of said first and second pulse signals to provide said first error signal.

6. In a machine as defined in claim 5 wherein said reference means comprises means for providing first and second reference signals to be compared respectively with said first and second registration marks and said means responsive to said marks for providing said first and second control signals comprises circuit means actuated to two conditions by one of said reference signals and the corresponding one of said marks.

7. In a machine according to claim 6 wherein said circuit means is actuated to first and second conditions to provide one of said first and second control signals in response to one of said registration signals and the corresponding reference signal and includes means for resetting said circuit means to a third condition for actuation to said first and second conditions in response to the other mark and corresponding reference signal to provide the other of said first and second signals.

8. In a machine according to claim 7 wherein said circuit means comprises first and second two-stage circuits, one of said circuits being set in response to the registration mark and the other of said circuits being set in response to the reference mark and said means for resetting said circuit comprising means for resetting said first and second two-stage circuits.

9. In a machine according to claim 8 wherein said circuit means responsive to said sensor means includes means responsive to the actuation of said first and second two-stage circuits to determine which of the circuits is first actuated to determine the lead-lag relationship of the reference mark and its corresponding registration mark.

10. In a machine according to claim 9 in which said means responsive to said sensor means comprises means for inhibiting the response of said circuit means to said sensor means except for a predetermined period in the operation of said machine in which a register mark is to be passing said sensor means.

11. A method of correcting a false error indicated by the sensing of a registration mark for indicating the location of machine operation on the work with respect to an adjustment in one direction when the position of the mark on the work varies with the position of the stock relative to the machine in a degree of freedom controlled by a second adjustment, the relationship of the stock to the machine in the degree of freedom controlled by the second adjustment being indicated by the position of a second registration mark, comprising the steps of sensing the registration marks as they pass a fixed location, comparing the registration marks with a reference to determine time intervals that the marks are late or early in passing the location to ascertain the error in the adjustment in accordance with the time in-

terval and modifying the error derived in dependency on the first mark before making the adjustment as a function of the error derived in dependency on said second mark.

12. A method of registering images printed by a press onto sheet material comprising the steps of printing first and second register marks indicating the position of the image on the sheet material transversely of and in the direction of movement of the sheet material through the press, the first mark being inclined relative to the line of movement of the sheet material through the press and the second mark being transverse to the line of movement, sensing the marks at a fixed location to determine the time that the marks pass the location with respect to a reference to determine registration errors transversely of and in the direction of sheet movement and electrically combining the error sensed in the adjustment transversely of and in the direction of the movement of the sheet to provide a corrected transverse error signal when errors are introduced into the error signal because of misregistration in the direction of sheet movement.

13. A method as defined in claim 12 in which a signal is derived from each of said registration marks as it passes said sensing means and is compared with reference signals for each mark indicating the time that the registration marks should be at the sensing means, the error in time being measured by pulsing a counter for registering the error in the direction transversely of the sheet movement both during the time interval between the arrive of the first and second registration marks at the sensing means and their respective reference signals.

14. In a printing press for printing an image on sheet stock moving through the machine including first adjusting means for making a first adjustment of said stock relative to the printing operation performed by said machine on said stock, second adjustment means for making a second adjustment of said stock relative to the printing operation of said machine on said stock, sensor means for sensing a first register mark on said stock which indicates the relationship of the printed image on said stock with respect to a first degree of freedom controlled by said first adjustment and for sensing a second register mark on said machine to indicate the relationship of the printed image on said stock with respect to a second degree of freedom con-

trolled by said second adjustment means, changes in the position of the image on said stock with respect to the second degree of freedom effecting a change in the sensed relationship derived from said first mark independently of a change in the relationship of the image on the stock with respect to said first degree of freedom, means responsive to said sensor means for ascertaining errors in the adjustment of said first and second adjusting means and providing first and second error signals for correcting said first and second adjusting means including means responsive to the sensing of said second mark for compensating said first error signal for false errors introduced by errors in said second adjusting means.

15. In a method of operating a machine in which a cyclical work operation is performed on stock moving in one direction through a machine with the work operation being controlled with respect to a first degree of freedom, applying first register marks to said stock whose times of arrival at a sensing station as compared to a reference indicate the adjustment of the machine with respect to a first degree of freedom, the times of arrival of said first register marks at said first station varying in accordance with the adjustment of the machine with respect to a second degree of freedom, applying register marks said stock whose time of arrival at said station with respect to a reference indicates the adjustment of said machine with respect to said second degree of freedom, and sensing the times of arrival of said first and second marks at said station to provide error signals for controlling the adjustment of the machine with respect to said first degree of freedom including compensating the error signal derived in dependency on the arrival of said first register marks in accordance with the time of arrival of said second register marks at said station to render the error signal for adjusting the machine with respect to said first degree of freedom independent of the adjustment of said machine with respect to said second degree of freedom.

16. In a method as defined in claim 15 wherein said first degree of freedom is transversely of the line of movement of the stock through the machine and the first register mark comprises a line which is inclined with respect to the line of movement.

17. In a method as defined in claim 16 wherein said second degree of freedom is along the line of movement of the said material through the machine.

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