United States Patent [19]

Christiansen et al.

[11] **3,812,475**

[45] **May 21, 1974**

[54] **DATA SYNCHRONIZER**

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[73] Assignee: **International Business Machines Corporation,** New York, N.Y.

[22] Filed: **Dec. 26, 1957**

[21] Appl. No.: **705,447**

[52] **U.S. Cl.** **340/172.5**

[51] **Int. Cl.** **G06f 9/18**

[58] **Field of Search** ..... 235/61 PB, 61 MS, 157, 235/165, 166, 167

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Primary Examiner—Raulfe B. Zache
Attorney, Agent, or Firm—Hanifin & Jancin

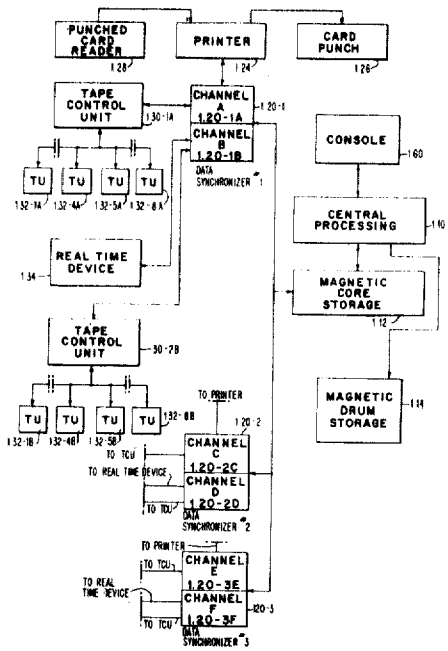
[57] **ABSTRACT**

A data processing system in which a plurality of data channels control the simultaneous exchange of data between many input/output devices, and a common shared storage. The channels automatically extract control instructions from storage and interpret them to independently carry out data transfers.

Each data channel is initialized by the central processing unit (CPU) which causes a control word to be transferred from storage to the data channel where it is stored. The data channel utilizes the control word to start an input/output operation. The input/output operation is continued automatically by the channel which has means for retrieving subsequent control words from storage independent of the CPU. Data transfers between a data channel and the storage over a common storage bus are performed by a "cycle stealing" capability wherein execution of the CPU program may be delayed for one storage cycle, which cycle is utilized by the channel to store a word of data in the storage. Competing requests among data channels and the CPU are resolved by a priority circuit which grants storage access to the highest priority channel demanding access. The CPU is given the lowest priority.

Since the channels direct the flow of information between I/O devices and main storage, they relieve the CPU of the task of communicating directly with the devices and permit data processing to proceed concurrently with I/O operations.

91 Claims, 506 Drawing Figures



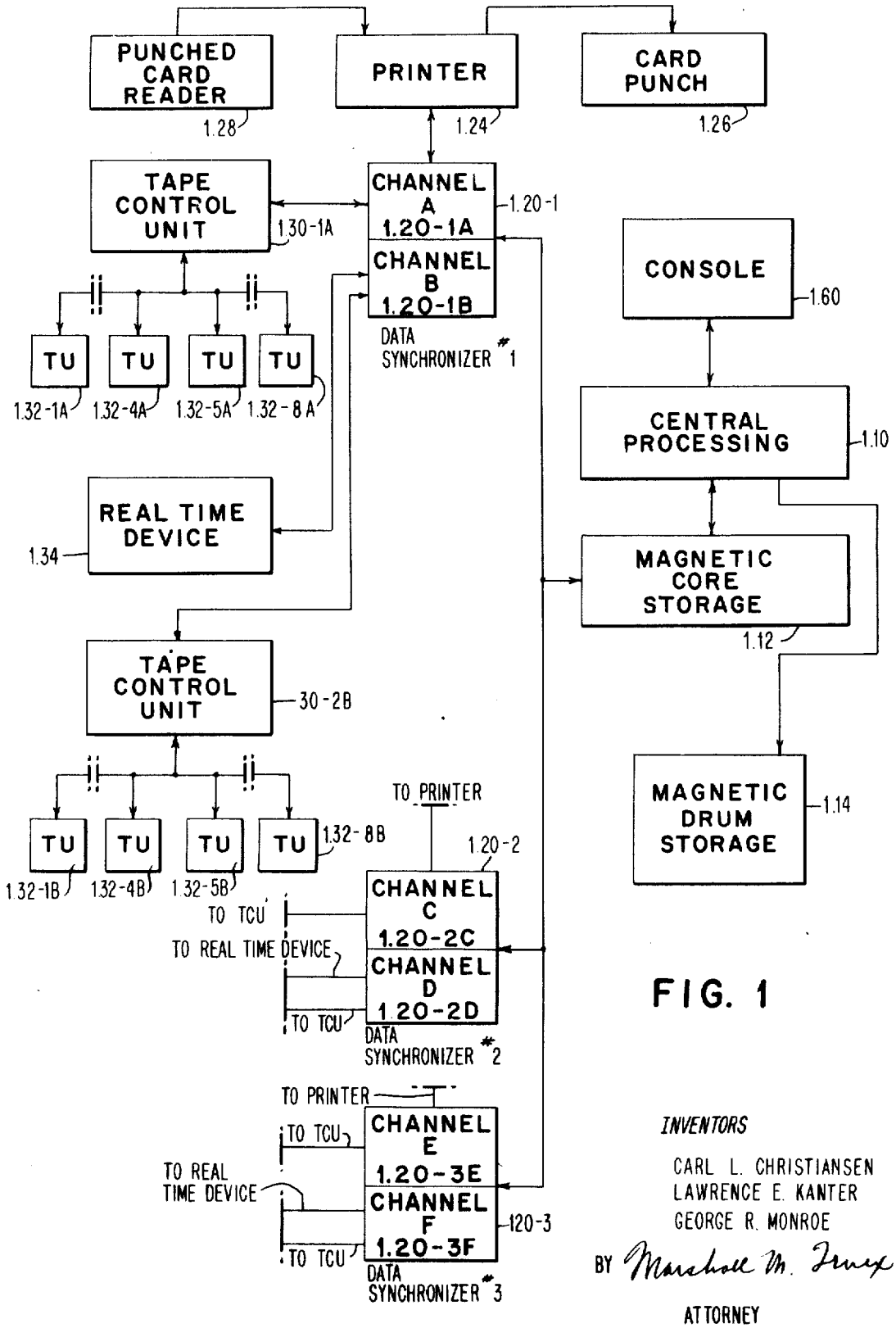


FIG. 1

INVENTORS

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GEORGE R. MONROE

BY Marshall M. Truex

ATTORNEY

FIG. 2a

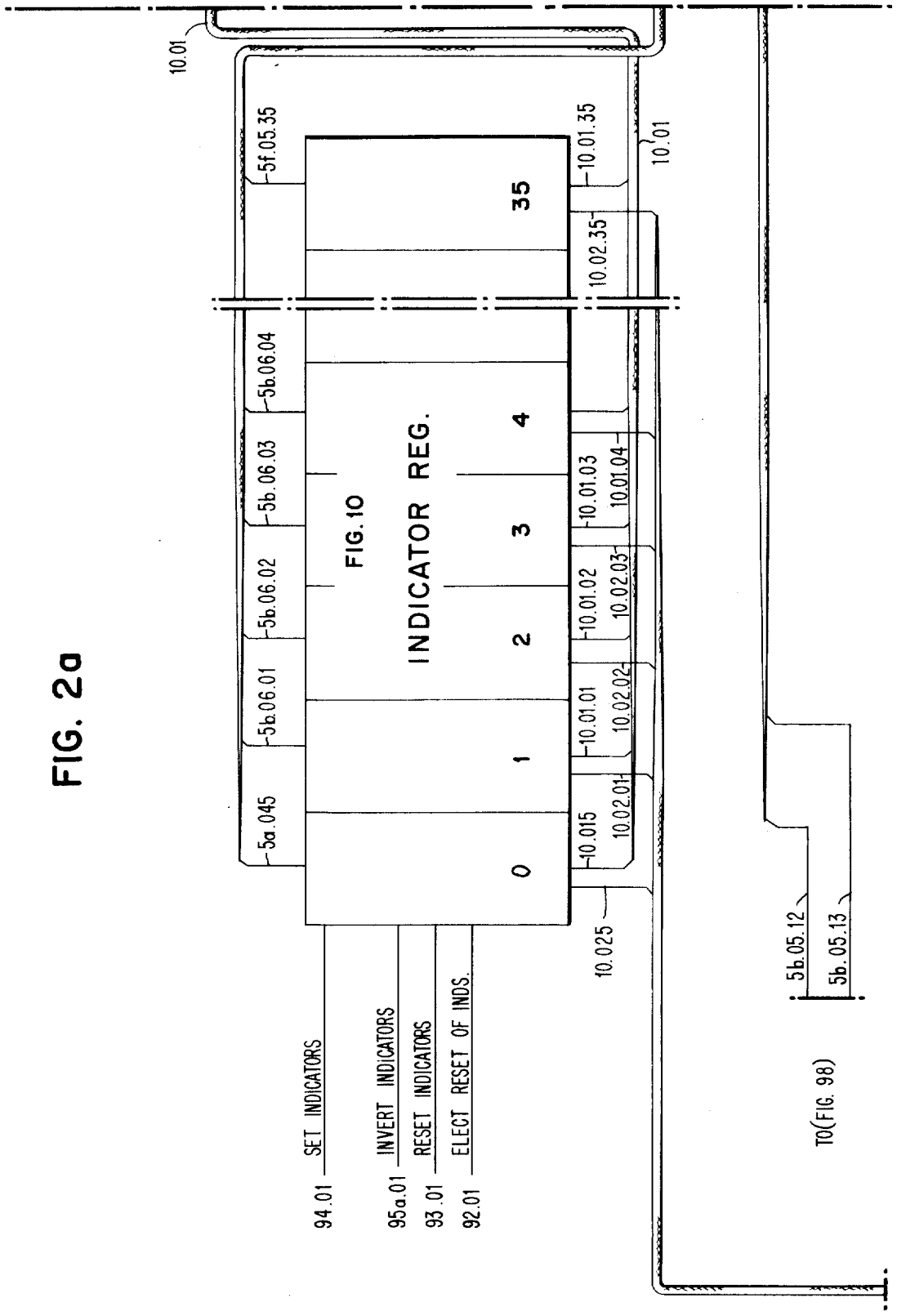

10.01
5f.05.35
10.01.35
10.01
10.02.35
35
5b.06.04
5b.06.03
5b.06.02
5b.06.01
5a.045
INDICATOR REG.
4
3
2
1
0
10.01.03
10.01.04
10.01.02
10.02.03
10.01.01
10.02.02
10.015
10.02.01
10.025
5b.05.12
5b.05.13
TO(FIG. 98)
94.01 SET INDICATORS
95a.01 INVERT INDICATORS
93.01 RESET INDICATORS
92.01 ELECT RESET OF INDS.

FIG. 10

FIG. 2b

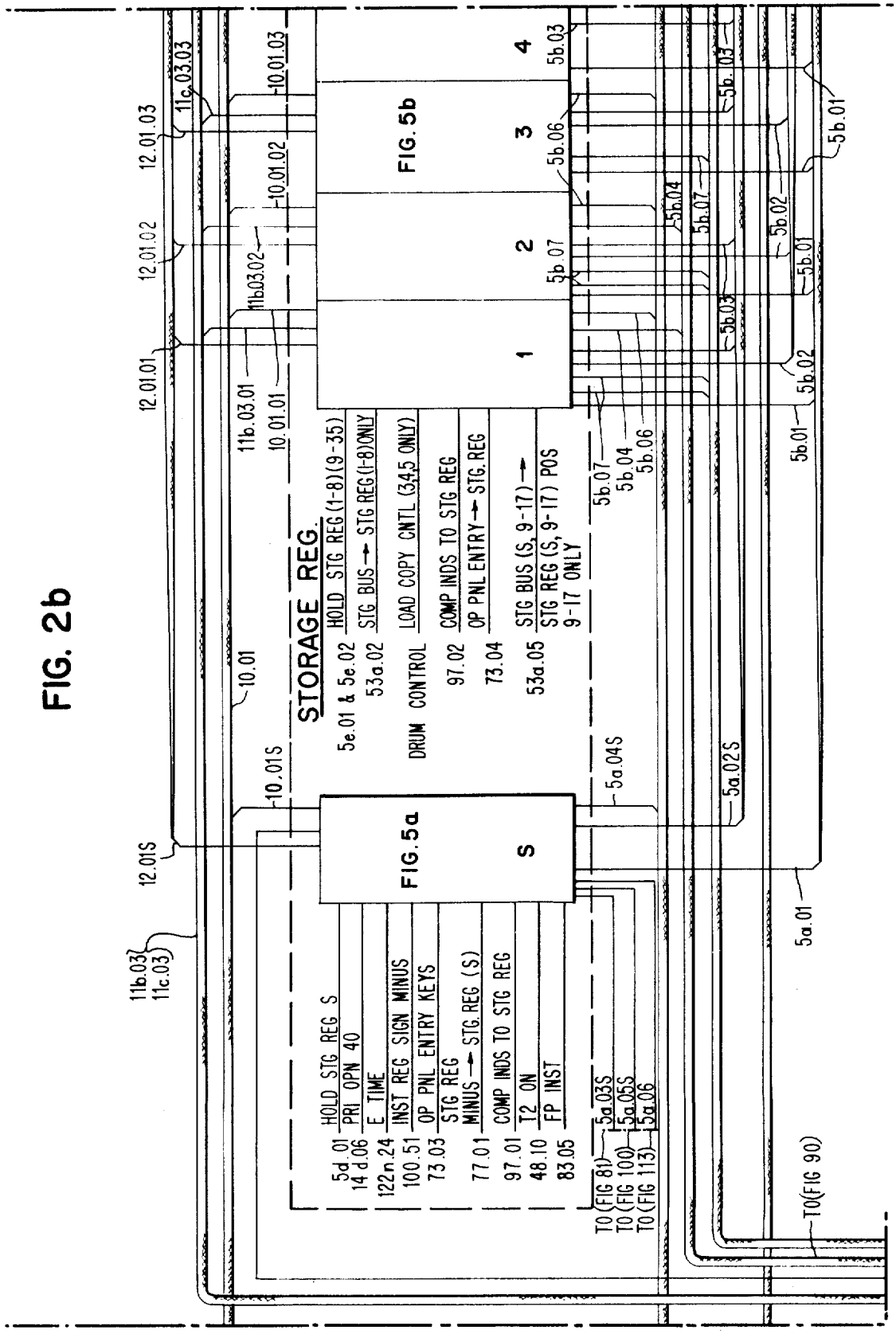

STORAGE REG.
DRUM CONTROL
HOLD STG REG (1-8)(9-35)
STG BUS → STG REG (1-8) ONLY
LOAD COPY CNTL (34,5 ONLY)
COMP INDS TO STG REG
OP PNL ENTRY → STG. REG
STG BUS (S, 9-17) →
STG REG (S, 9-17) POS 9-17 ONLY
HOLD STG REG S
PRI OPN 40
E TIME
INST REG SIGN MINUS
OP PNL ENTRY KEYS
STG REG MINUS → STG. REG (S)
COMP INDS TO STG REG
T2 ON
FP INST
FIG. 5a
FIG. 5b
TO (FIG 81)
TO (FIG 100)
TO (FIG 113)
TO (FIG 90)

FIG. 2c

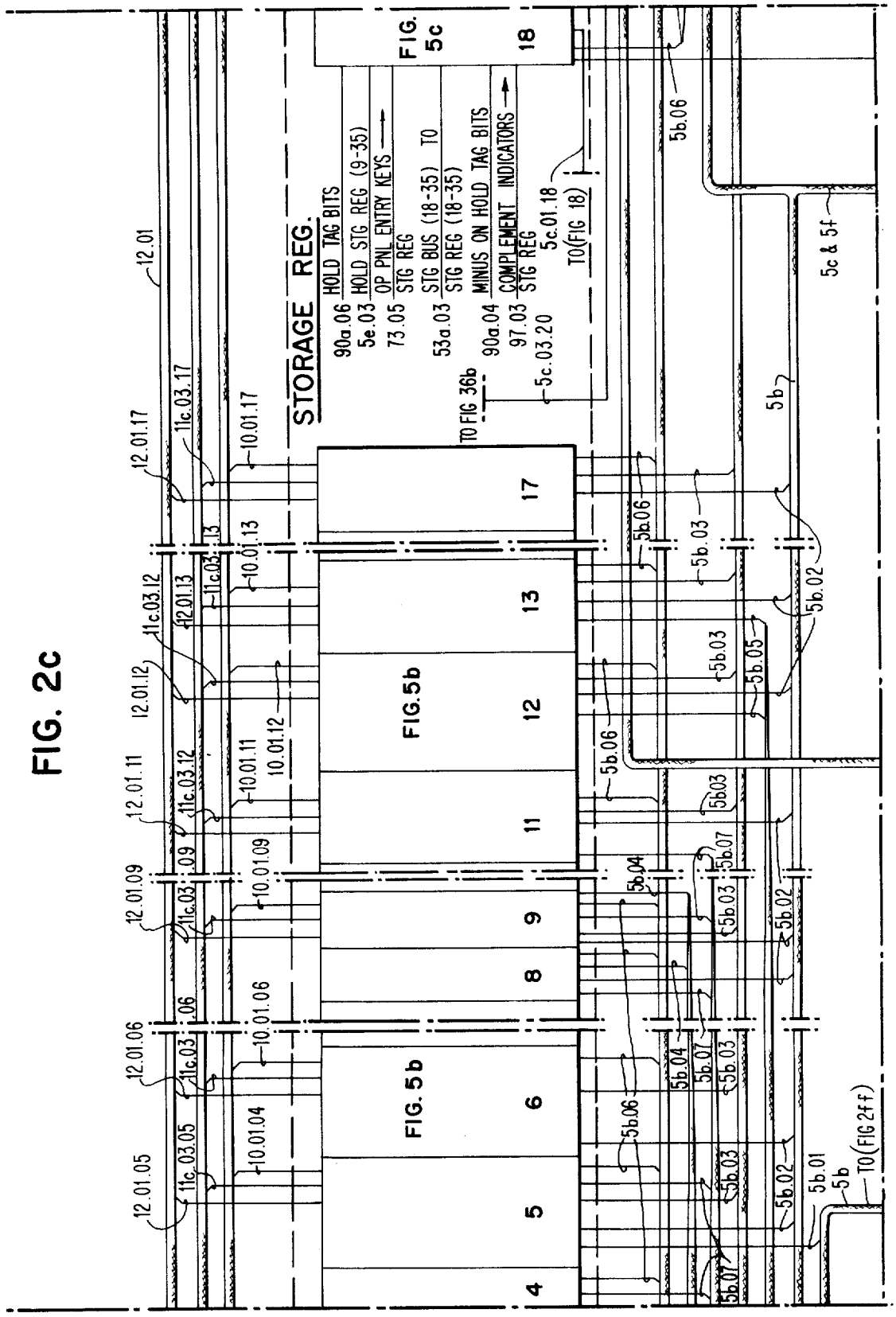
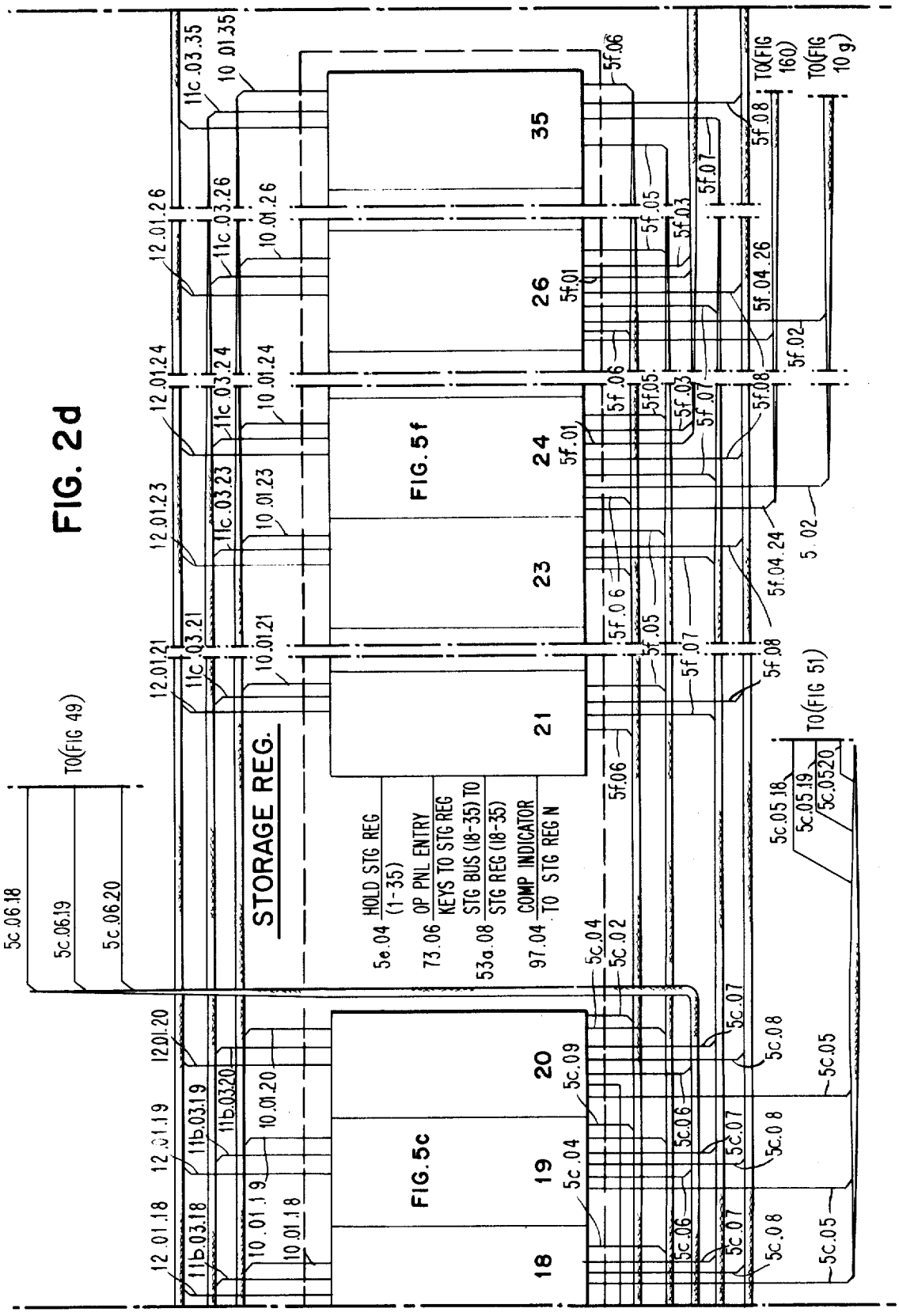
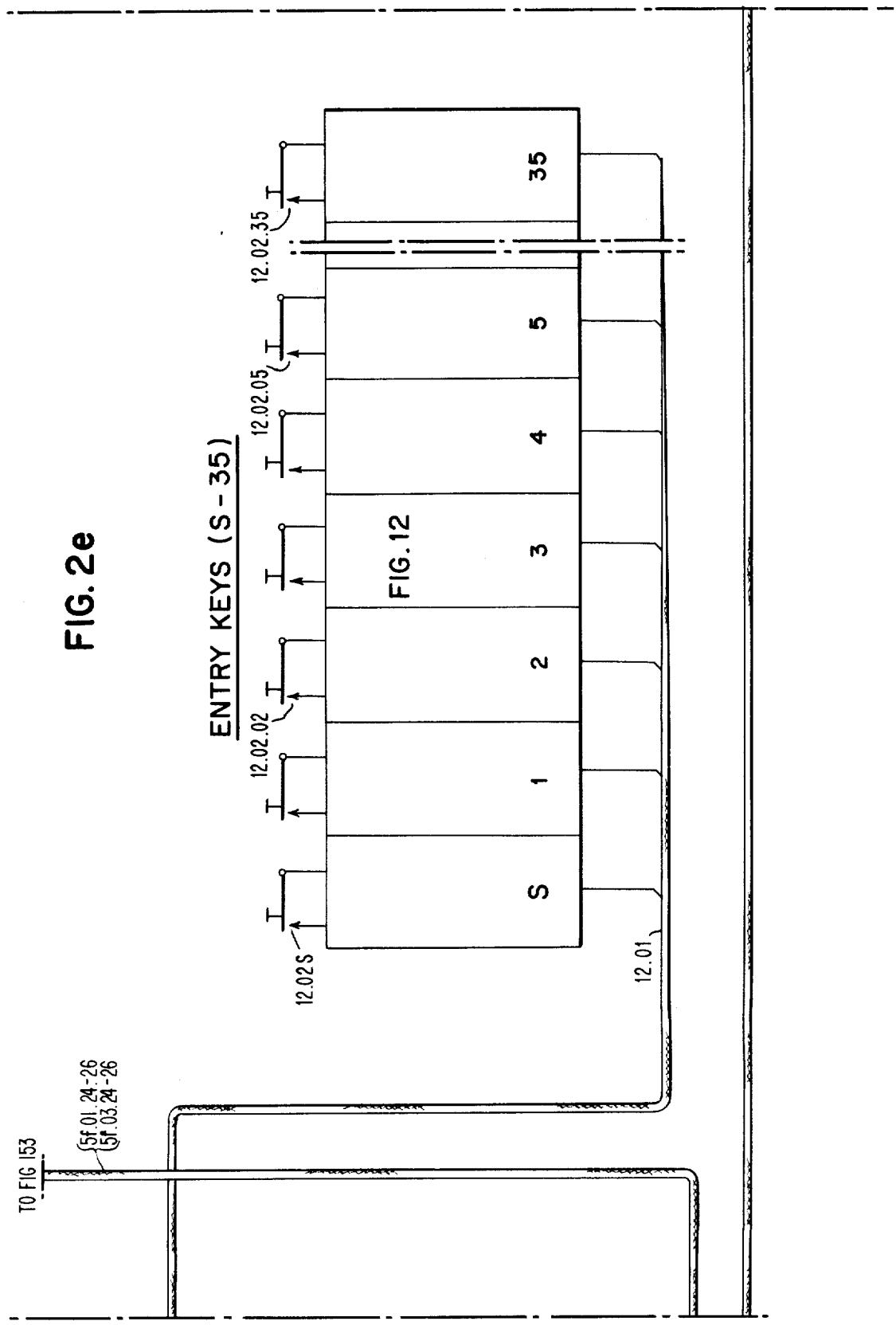

STORAGE REG.
HOLD TAG BITS
90a.06
HOLD STG REG (9-35)
5e.03
OP PNL ENTRY KEYS
73.05
STG REG
STG BUS (18-35) TO
53a.03
STG REG (18-35)
MINUS ON HOLD TAG BITS
90a.04
COMPLEMENT INDICATORS
97.03
STG REG
5c.03.20
5c.01.18
TO(FIG 18)
TO FIG 36b
FIG. 5c
FIG. 5b
FIG. 5b
5c & 5f
5b
5b.06
5b.03
5b.02
5b.05
5b.04
5b.07
5b.01
TO(FIG 2f f)
12.01
12.01.17
12.01.13
12.01.12
12.01.11
12.01.09
12.01.06
12.01.05
11c.03.17
11c.03.12
11c.03.05
10.01.17
10.01.13
10.01.12
10.01.11
10.01.09
10.01.06
10.01.04
18
17
13
12
11
9
8
6
5
4

FIG. 2d


STORAGE REG.
FIG. 5f
FIG. 5c
HOLD STG REG (1-35)
OP PNL ENTRY KEYS TO STG REG
STG BUS (18-35) TO STG REG (18-35)
COMP INDICATOR TO STG REG N
TO(FIG 49)
TO(FIG 51)
TO(FIG 16D)
TO(FIG 10 g)


FIG. 2e
ENTRY KEYS (S - 35)
12.02.35
12.02.05
12.02.02
12.02S
12.01
35
5
4
3
2
1
S
FIG. 12
TO FIG 153
5f.01.24-26
5f.03.24-26

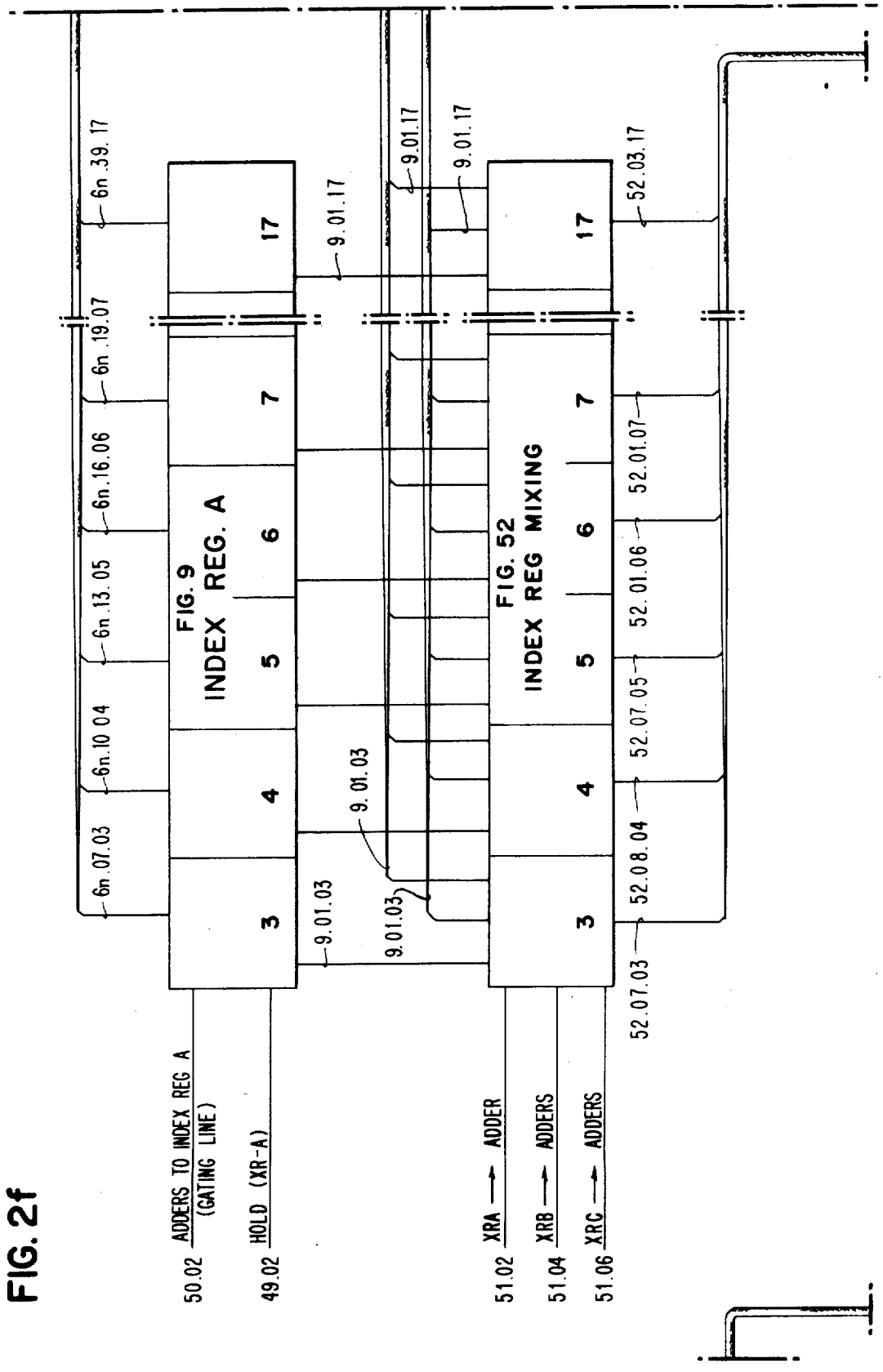
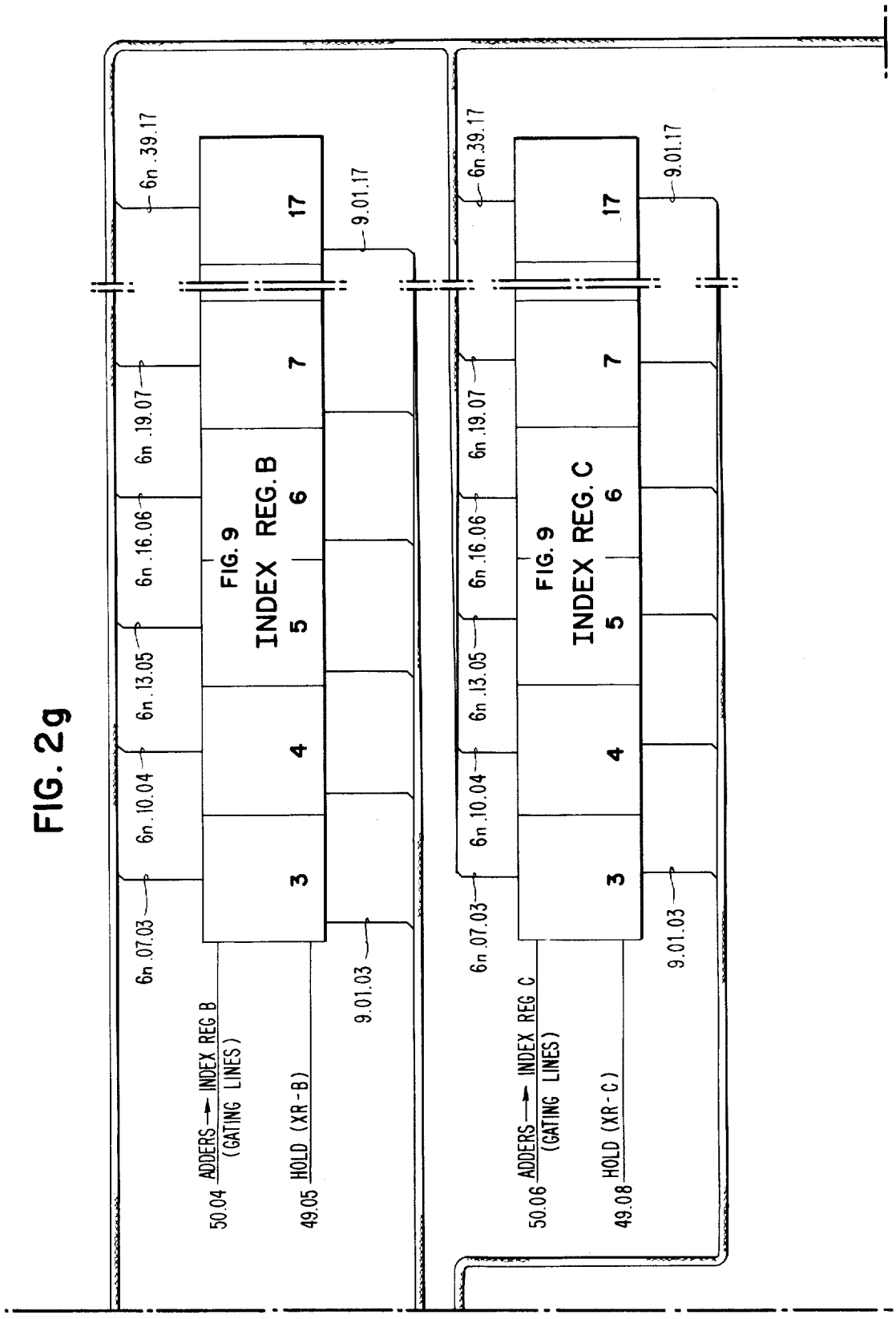

FIG. 9
INDEX REG. A
FIG. 52
INDEX REG MIXING
6n.39.17
6n.19.07
6n.16.06
6n.13.05
6n.10.04
6n.07.03
9.01.17
9.01.03
52.03.17
52.01.07
52.01.06
52.07.05
52.08.04
52.07.03
17
7
6
5
4
3
50.02 ADDERS TO INDEX REG A (GATING LINE)
49.02 HOLD (XR-A)
51.02 XRA → ADDER
51.04 XRB → ADDERS
51.06 XRC → ADDERS

FIG. 2f

FIG. 2g


FIG. 9
INDEX REG. B
FIG. 9
INDEX REG. C
6n.39.17
9.01.17
6n.19.07
6n.16.06
6n.13.05
6n.10.04
6n.07.03
9.01.03
17
7
6
5
4
3
50.04 ADDERS → INDEX REG B (GATING LINES)
49.05 HOLD (XR-B)
50.06 ADDERS → INDEX REG C (GATING LINES)
49.08 HOLD (XR-C)

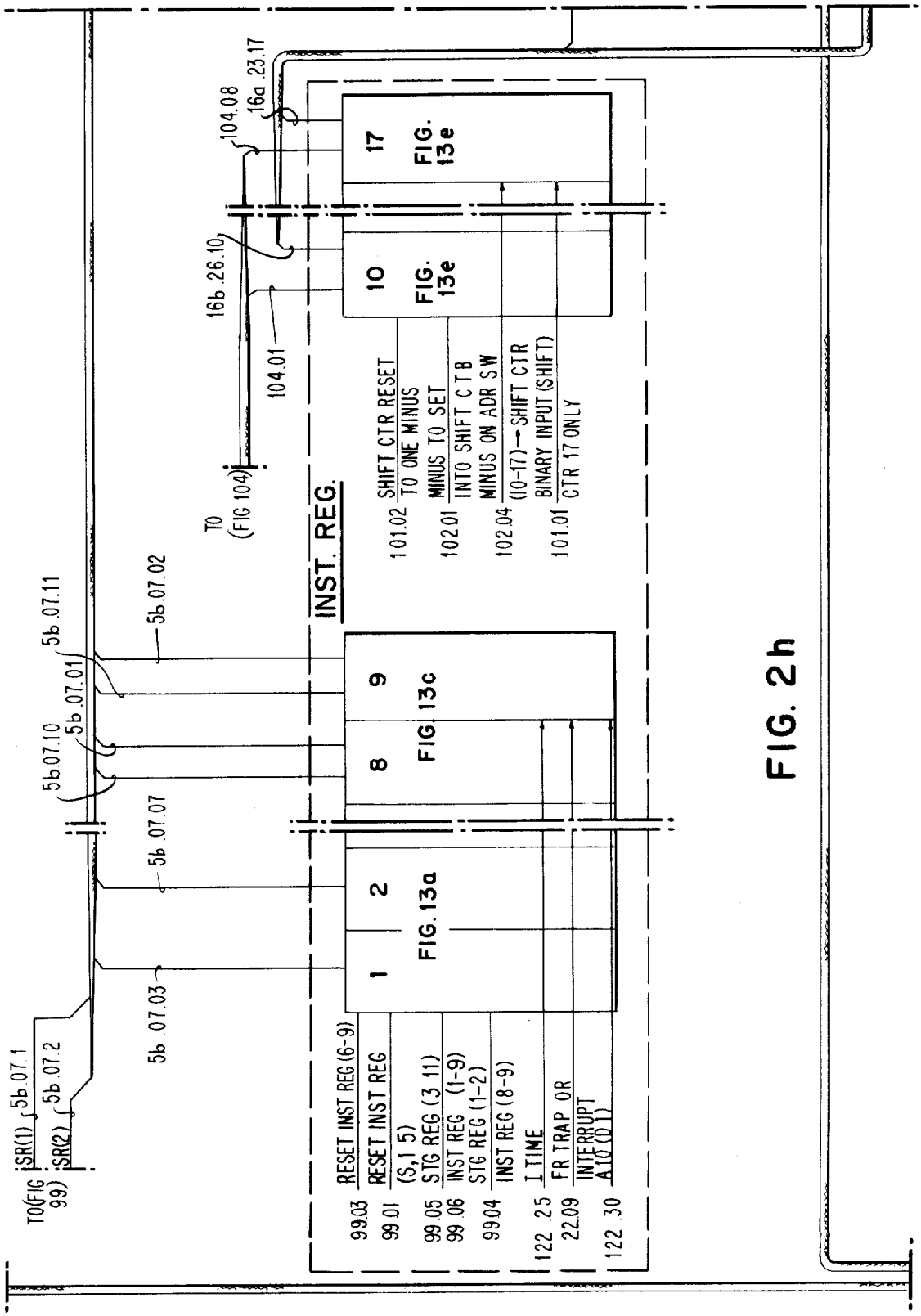
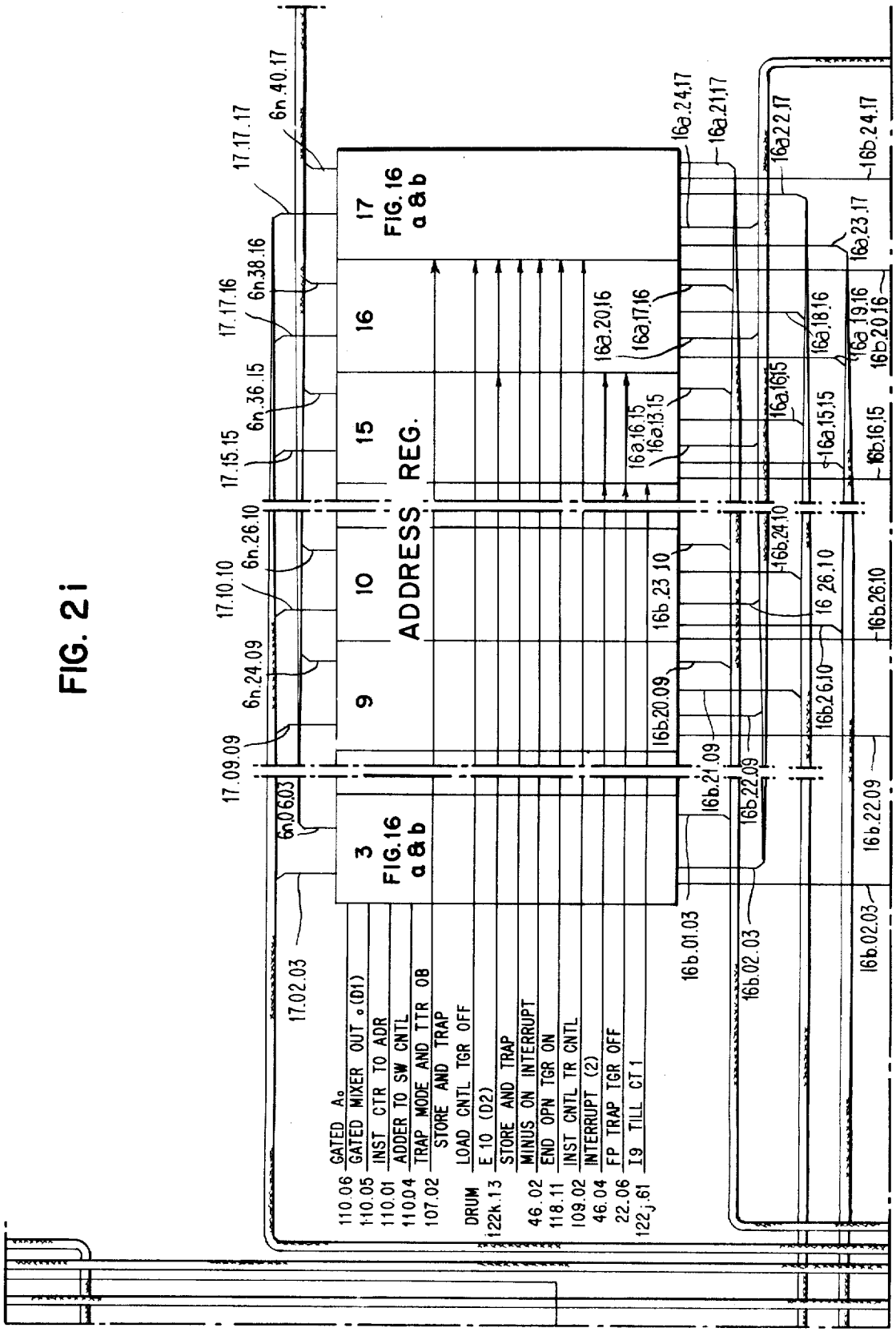
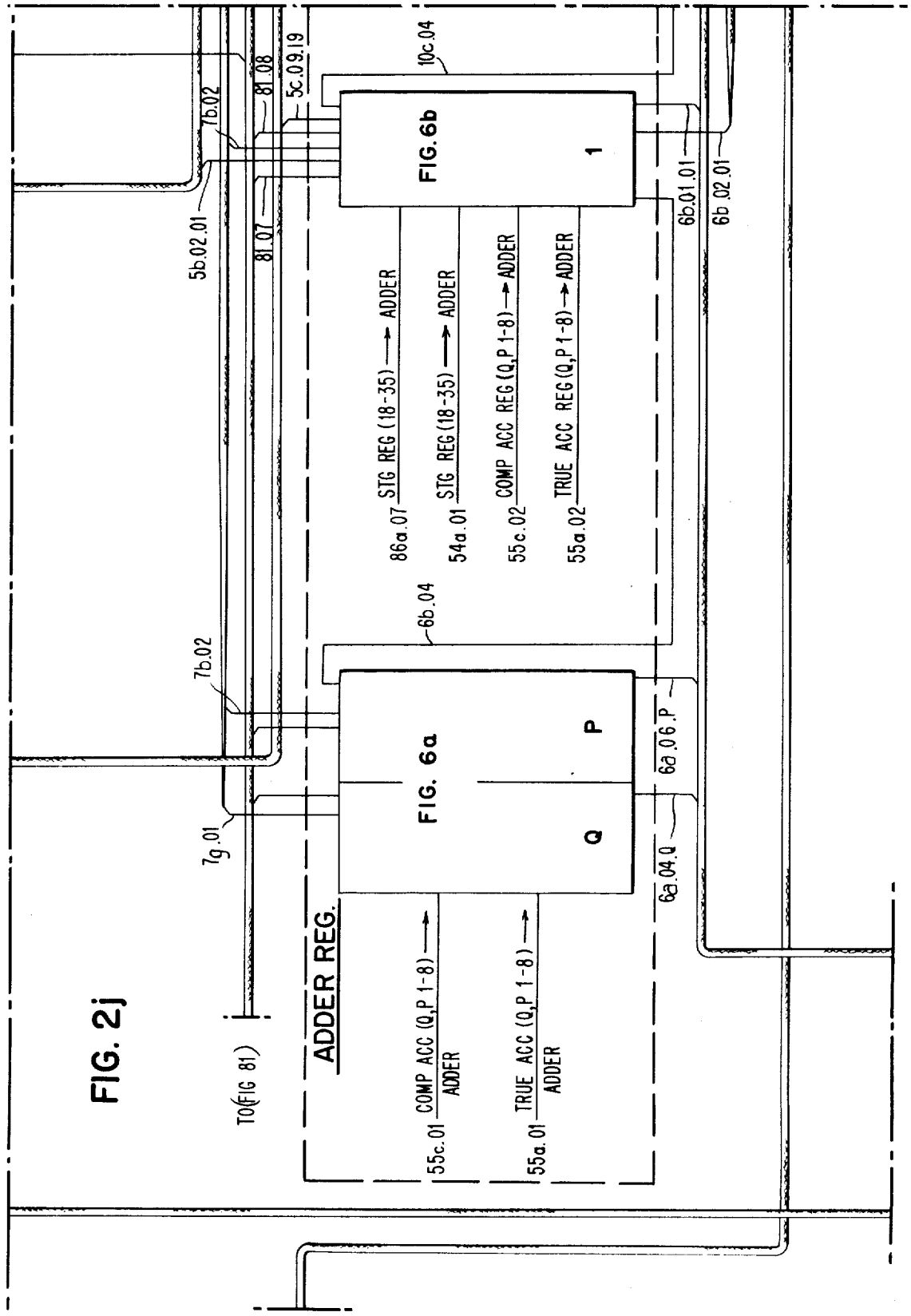

INST. REG.
TO (FIG 104)
104.01
16b .26.10
104.08
16a .23.17
17
FIG. 13e
10
FIG. 13e
101.02 SHIFT CTR RESET TO ONE MINUS
102.01 MINUS TO SET INTO SHIFT CTR
102.04 MINUS ON ADR SW (10-17) → SHIFT CTR
101.01 BINARY INPUT (SHIFT) CTR 17 ONLY
5b .07.11
5b .07.01
5b.07.10
5b .07.02
5b .07.07
5b .07.03
9
8
FIG. 13c
2
1
FIG. 13a
99.03 RESET INST REG (6-9)
99 01 RESET INST REG (S,1 5)
99 05 STG REG (3 11)
99 06 INST REG (1-9) STG REG (1-2)
99 04 INST REG (8-9)
122 25 I TIME FR TRAP OR
22.09 INTERRUPT A10 (0 1)
122 30
TO (FIG 99) SR(1) 5b .07 1
SR(2) 5b .07.2

FIG. 2h

FIG. 2i


ADDRESS REG.
3 FIG. 16 a & b
9
10
15
16
17 FIG. 16 a & b
GATED A₀
110.06 GATED MIXER OUT ₀ (D1)
110.05 INST CTR TO ADR
110.01 ADDER TO SW CNTL
110.04 TRAP MODE AND TTR 08
107.02 STORE AND TRAP
DRUM LOAD CNTL TGR OFF
122k.13 E.10 (D2)
STORE AND TRAP
46.02 MINUS ON INTERRUPT
118.11 END OPN TGR ON
109.02 INST CNTL TR CNTL
46.04 INTERRUPT (2)
22.06 FP TRAP TGR OFF
122j.61 I9 TILL CT 1
17.02.03
6n.06.03
17.09.09
6n.24.09
17.10.10
6n.26.10
17.15.15
6n.36.15
17.16.16
6n.38.16
17.17.17
6n.40.17
16b.01.03
16b.02.03
16b.21.09
16b.22.09
16b.20.09
16b.23.10
16b.24.10
16b.26.10
16a.20.16
16a.16.15
16a.13.15
16a.17.16
16a.16.15
16a.13.15
16a.24.17
16a.21.17
16a.22.17
16a.23.17
16a.19.16
16a.18.16
16a.15.15
16a.16.15
16b.24.17
16b.20.16
16b.16.15
16b.26.10
16 26.10
16b.26.10
16b.22.09
16b.02.03


FIG. 2j
FIG. 6b
FIG. 6a
ADDER REG.
1
P
Q
10c.04
5c.09.19
81.08
7b.02
5b.02.01
81.07
6b.01.01
6b.02.01
86a.07 STG REG (18-35) → ADDER
54a.01 STG REG (18-35) → ADDER
55c.02 COMP ACC REG (Q,P 1-8) → ADDER
55a.02 TRUE ACC REG (Q,P 1-8) → ADDER
6b.04
7b.02
6a.06.P
7g.01
6a.04.Q
TO (FIG 81)
55c.01 COMP ACC (Q,P 1-8) → ADDER
55a.01 TRUE ACC (Q,P 1-8) → ADDER

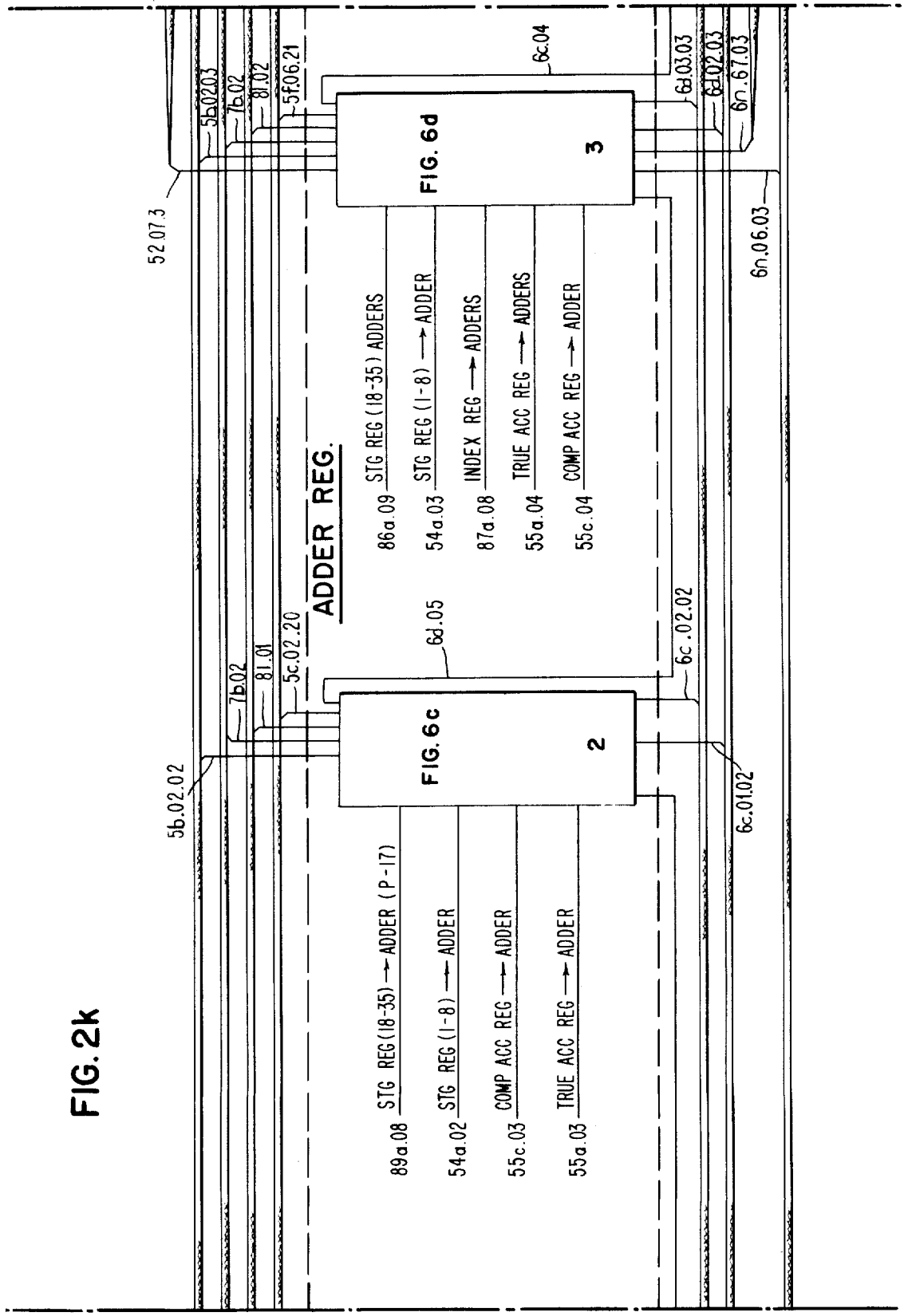
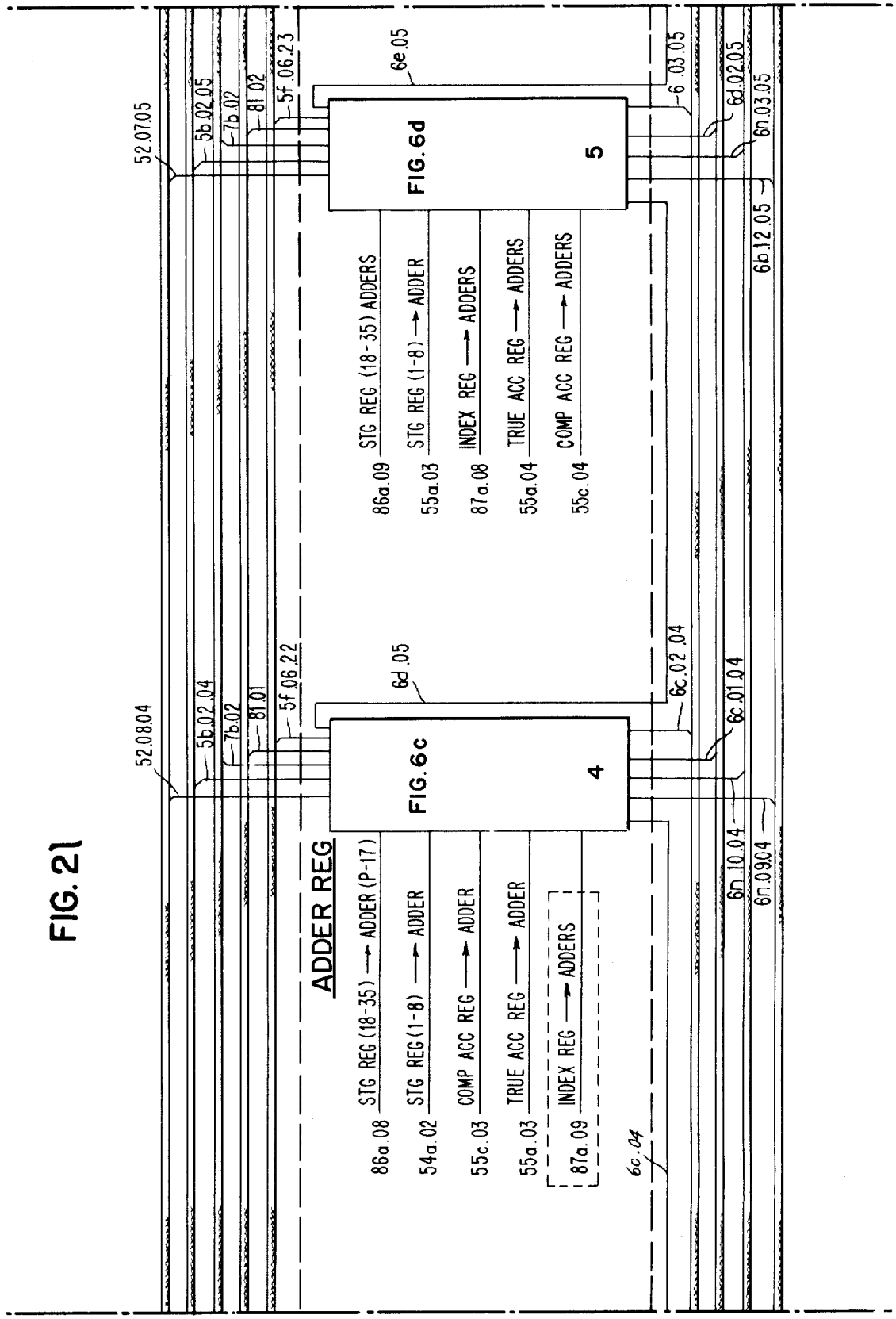

FIG. 2k
52.07.3
5b.02.03
7b.02
81.02
5f06.21
6c.04
6d.03.03
6d.02.03
6n.67.03
6n.06.03
FIG. 6d
3
86a.09 STG REG (18-35) ADDERS
54a.03 STG REG (1-8) → ADDER
87a.08 INDEX REG → ADDERS
55a.04 TRUE ACC REG → ADDERS
55c.04 COMP ACC REG → ADDER
ADDER REG.
6d.05
6c.02.02
5b.02.02
7b.02
81.01
5c.02.20
FIG. 6c
2
89a.08 STG REG (18-35) → ADDER (P-17)
54a.02 STG REG (1-8) → ADDER
55c.03 COMP ACC REG → ADDER
55a.03 TRUE ACC REG → ADDER
6c.01.02

FIG. 21


52.07.05
52.08.04
5b.02.05
5b.02.04
7b.02
8l.02
8l.01
5f.06.23
5f.06.22
6e.05
6d.05
6.03.05
6d.02.05
6n.03.05
6b12.05
6c.02.04
6c.01.04
6n.10.04
6n.09.04
FIG. 6d
FIG. 6c
5
4
ADDER REG
86a.09 STG REG (18-35) ADDERS
55a.03 STG REG (1-8) → ADDER
87a.08 INDEX REG → ADDERS
55a.04 TRUE ACC REG → ADDERS
55c.04 COMP ACC REG → ADDERS
86a.08 STG REG (18-35) → ADDER (P-17)
54a.02 STG REG (1-8) → ADDER
55c.03 COMP ACC REG → ADDER
55a.03 TRUE ACC REG → ADDER
87a.09 INDEX REG → ADDERS
6c.04

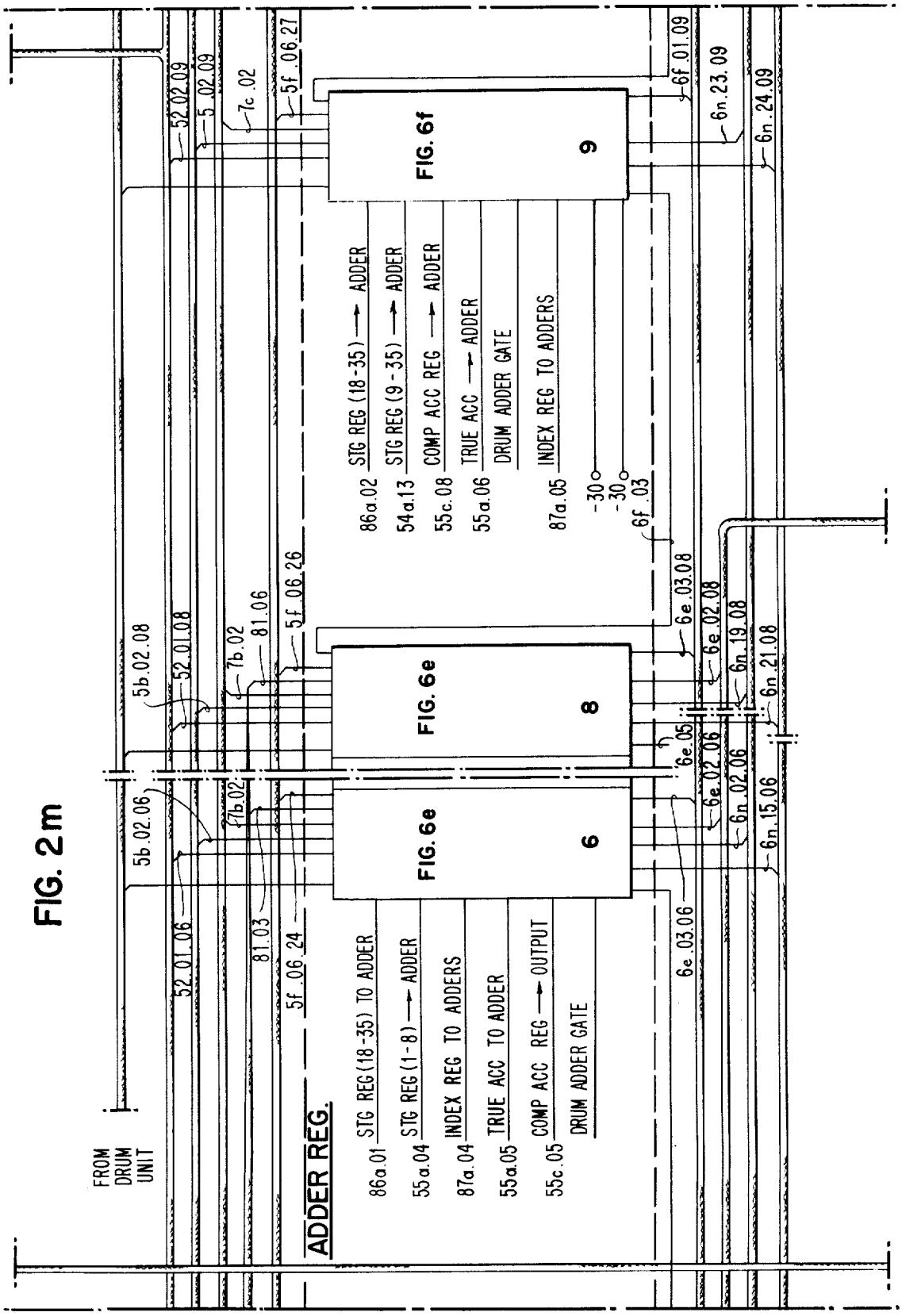
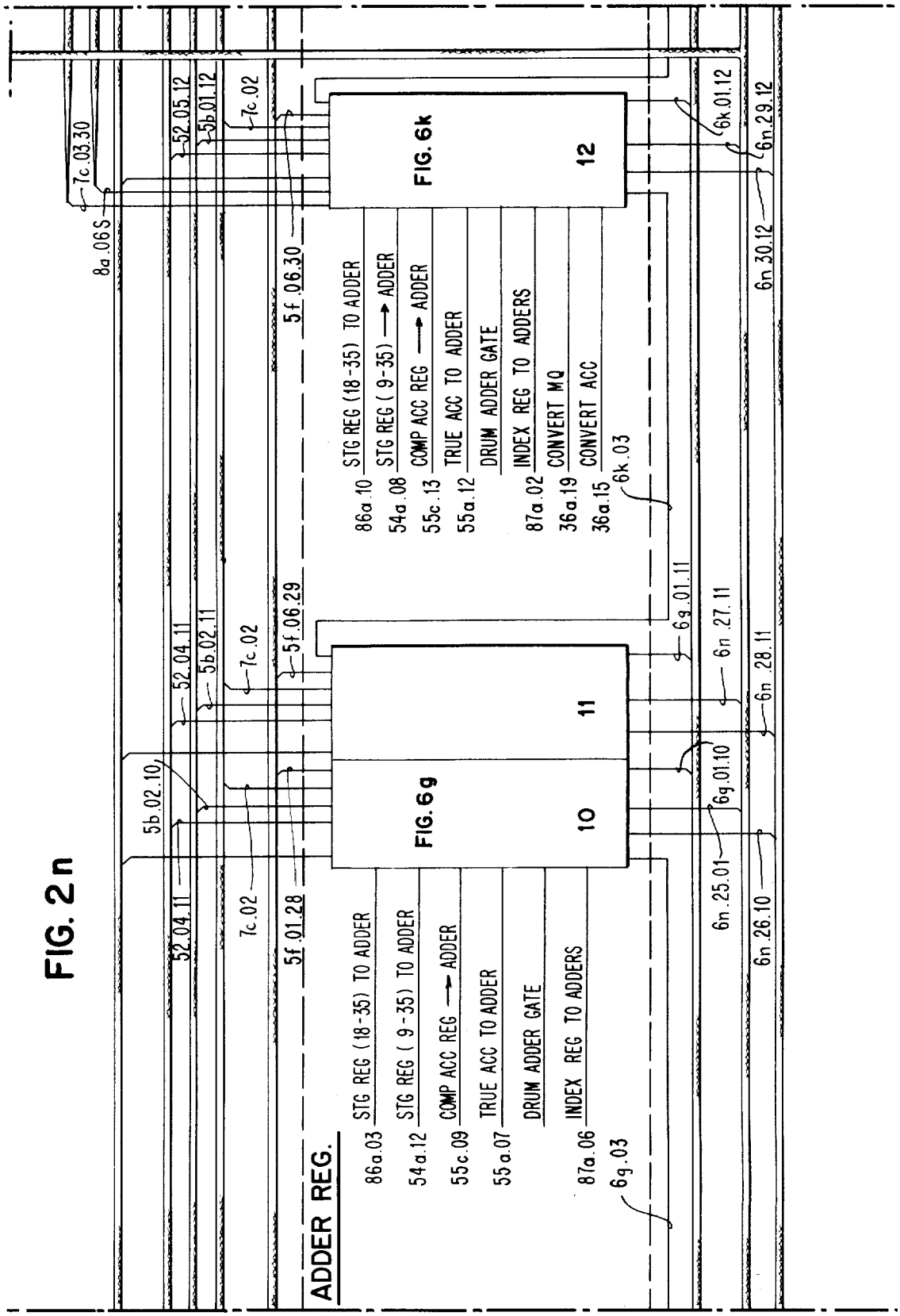

FIG. 2m
FROM DRUM UNIT
ADDER REG.
86a.01 STG REG (18-35) TO ADDER
55a.04 STG REG (1-8) → ADDER
87a.04 INDEX REG TO ADDERS
55a.05 TRUE ACC TO ADDER
55c.05 COMP ACC REG → OUTPUT
DRUM ADDER GATE
FIG. 6e
6
FIG. 6e
8
FIG. 6f
9
86a.02 STG REG (18-35) → ADDER
54a.13 STG REG (9-35) → ADDER
55c.08 COMP ACC REG → ADDER
55a.06 TRUE ACC → ADDER
DRUM ADDER GATE
87a.05 INDEX REG TO ADDERS
5b.02.06
5b.02.08
52.01.06
52.01.08
52.02.09
5.02.09
7b.02
7c.02
81.03
81.06
5f.06.24
5f.06.26
5f.06.27
6e.03.06
6e.03.08
6e.05
6e.02.06
6e.02.08
6n.02.06
6n.19.08
6n.15.06
6n.21.08
6f.01.09
6n.23.09
6n.24.09
-30
-30
6f.03

FIG. 2n


ADDER REG.
86a.03 STG REG (18-35) TO ADDER
54a.12 STG REG (9-35) TO ADDER
55c.09 COMP ACC REG → ADDER
55a.07 TRUE ACC TO ADDER
DRUM ADDER GATE
87a.06 INDEX REG TO ADDERS
6g.03
FIG. 6g
10
11
86a.10 STG REG (18-35) TO ADDER
54a.08 STG REG (9-35) → ADDER
55c.13 COMP ACC REG → ADDER
55a.12 TRUE ACC TO ADDER
DRUM ADDER GATE
87a.02 INDEX REG TO ADDERS
36a.19 CONVERT MQ
36a.15 CONVERT ACC
6k.03
FIG. 6k
12
7c.03.30
8a.06S
52.05.12
5b.01.12
7c.02
6k.01.12
6n.29.12
6n.30.12
5f.06.30
52.04.11
5b.02.11
7c.02
5f.06.29
6g.01.11
6n.27.11
6n.28.11
5b.02.10
52.04.11
7c.02
5f.01.28
6g.01.10
6n.25.01
6n.26.10

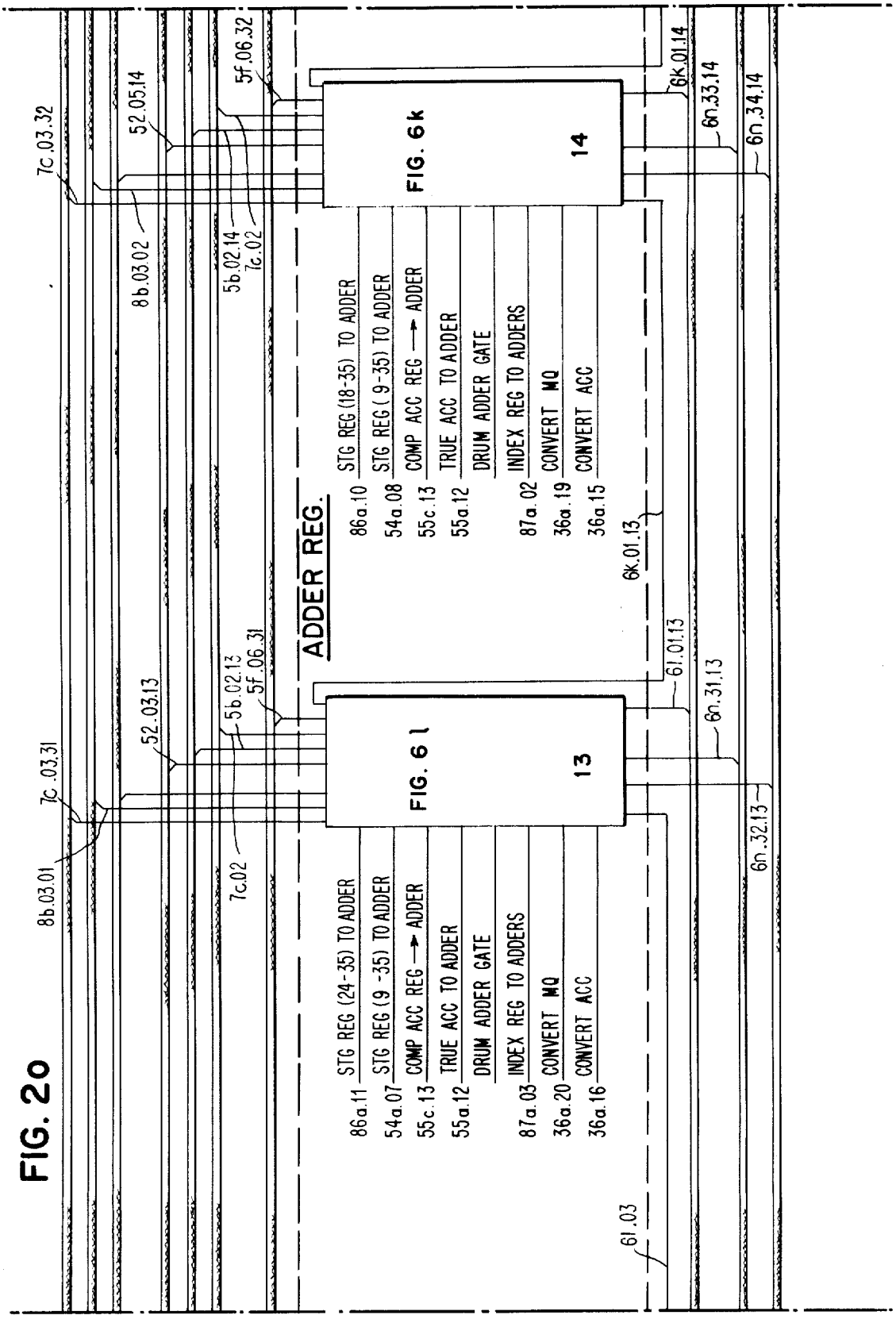

FIG. 20
ADDER REG.
FIG. 6 l
FIG. 6 k
13
14
STG REG (24-35) TO ADDER
STG REG (9 -35) TO ADDER
COMP ACC REG → ADDER
TRUE ACC TO ADDER
DRUM ADDER GATE
INDEX REG TO ADDERS
CONVERT MQ
CONVERT ACC
STG REG (18-35) TO ADDER
STG REG (9-35) TO ADDER
COMP ACC REG → ADDER
TRUE ACC TO ADDER
DRUM ADDER GATE
INDEX REG TO ADDERS
CONVERT MQ
CONVERT ACC
86a.11
54a.07
55c.13
55a.12
87a.03
36a.20
36a.16
86a.10
54a.08
55c.13
55a.12
87a.02
36a.19
36a.15
8b.03.01
7c .03.31
7c.03.32
52.03.13
52.05.14
8b.03.02
5b.02.13
5f.06.31
5b.02.14
7c.02
5f.06.32
7c.02
6K.01.13
6K.01.14
61.01.13
6n.31.13
6n.32.13
6n.33.14
6n.34.14
61.03

FIG. 2p

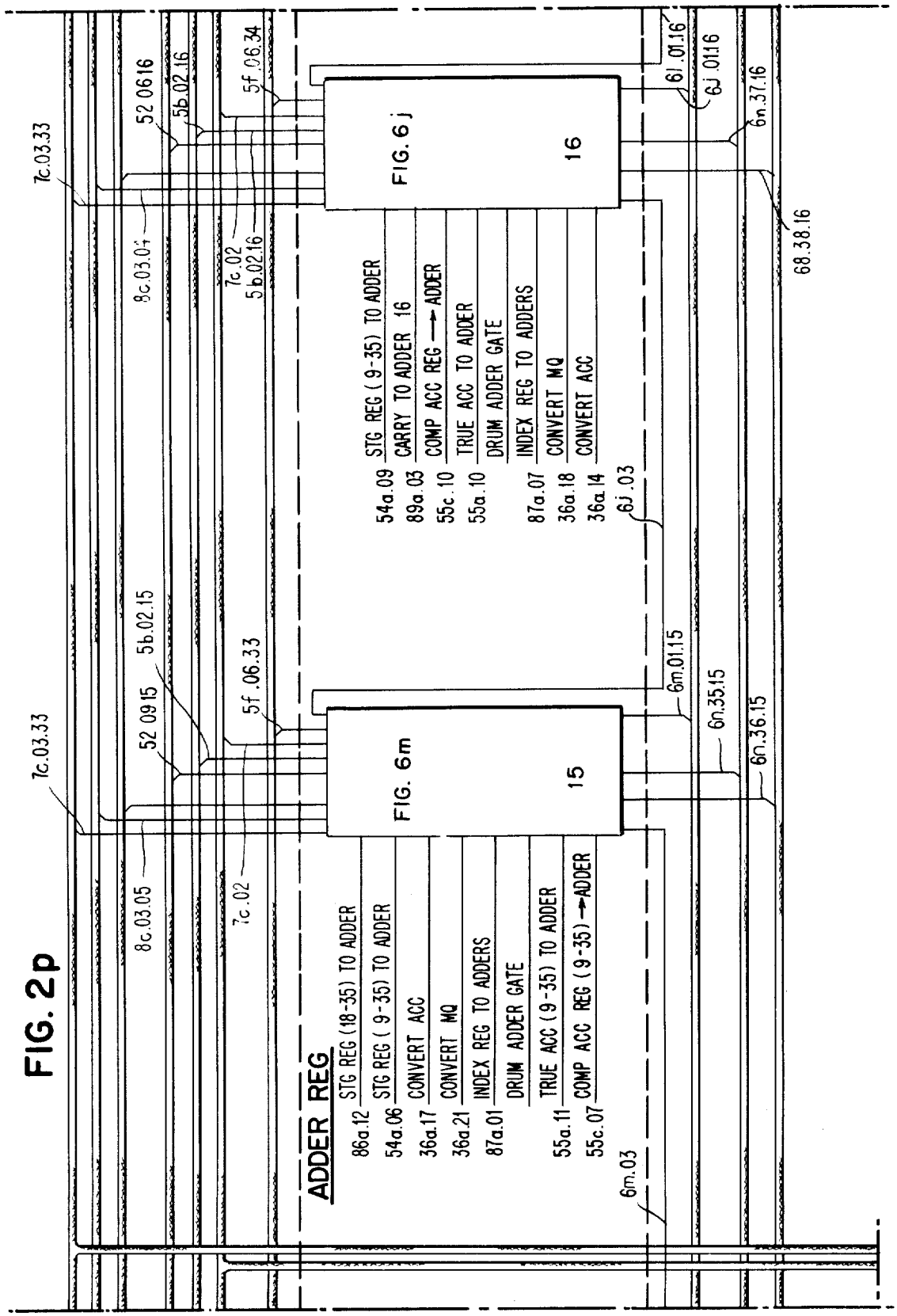
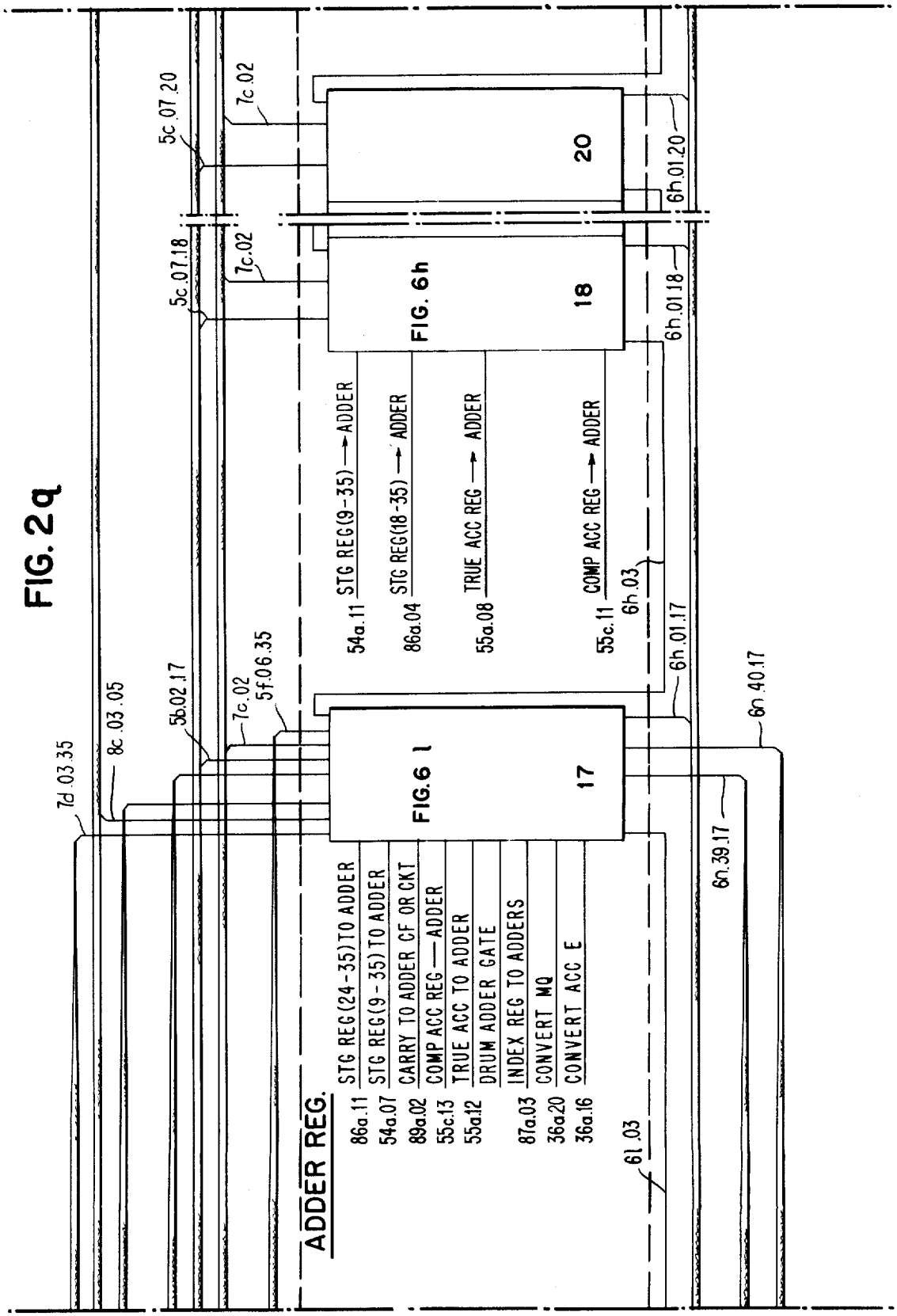

7c.03.33
52 0616
5b.02.16
5f .06.34
8c.03.04
7c.02
5b.02.16
FIG. 6 j
16
61 .01.16
6j .0116
6n.37.16
68.38.16
54a.09 STG REG (9-35) TO ADDER
89a.03 CARRY TO ADDER 16
55c.10 COMP ACC REG → ADDER
55a.10 TRUE ACC TO ADDER
DRUM ADDER GATE
87a.07 INDEX REG TO ADDERS
36a.18 CONVERT MQ
36a.14 CONVERT ACC
6j .03
6m.01.15
6n.35.15
6n.36.15
7c.03.33
52 0915
5b.02.15
5f .06.33
8c.03.05
7c .02
FIG. 6m
15
ADDER REG
86a.12 STG REG (18-35) TO ADDER
54a.06 STG REG (9-35) TO ADDER
36a.17 CONVERT ACC
36a.21 CONVERT MQ
87a.01 INDEX REG TO ADDERS
DRUM ADDER GATE
55a.11 TRUE ACC (9-35) TO ADDER
55c.07 COMP ACC REG (9-35) → ADDER
6m.03

FIG. 2q


ADDER REG.
86a.11 STG REG(24-35)TO ADDER
54a.07 STG REG(9-35)TO ADDER
89a.02 CARRY TO ADDER CF OR CKT
55c.13 COMP ACC REG — ADDER
55a12 TRUE ACC TO ADDER
DRUM ADDER GATE
87a.03 INDEX REG TO ADDERS
36a.20 CONVERT MQ
36a.16 CONVERT ACC E
FIG. 6 l
17
54a.11 STG REG(9-35) → ADDER
86a.04 STG REG(18-35) → ADDER
55a.08 TRUE ACC REG → ADDER
55c.11 COMP ACC REG → ADDER
FIG. 6h
18
20
7d.03.35
8c.03.05
5b.02.17
7c.02
5f.06.35
5c.07.18
5c.07.20
6h.01.17
6h.03
6h.01.18
6h.01.20
6n.40.17
6n.39.17
61.03

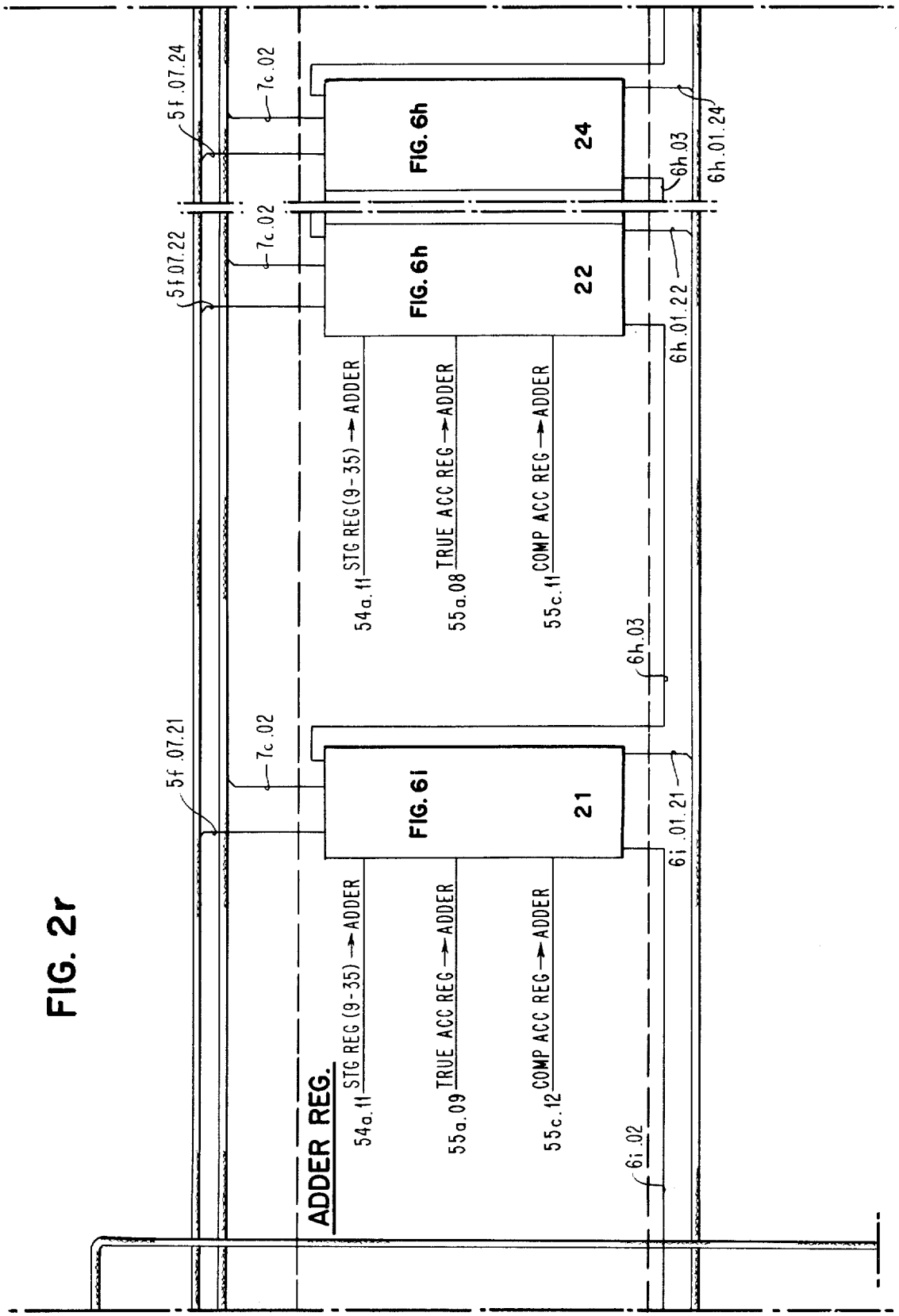

5f.07.24
7c.02
FIG. 6h
24
6h.03
6h.01.24
5f.07.22
7c.02
FIG. 6h
22
6h.01.22
54a.11 STG REG(9-35) → ADDER
55a.08 TRUE ACC REG → ADDER
55c.11 COMP ACC REG → ADDER
6h.03
5f.07.21
7c.02
FIG. 6i
21
6i.01.21
ADDER REG.
54a.11 STG REG (9-35) → ADDER
55a.09 TRUE ACC REG → ADDER
55c.12 COMP ACC REG → ADDER
6i.02

FIG. 2r

FIG. 2s

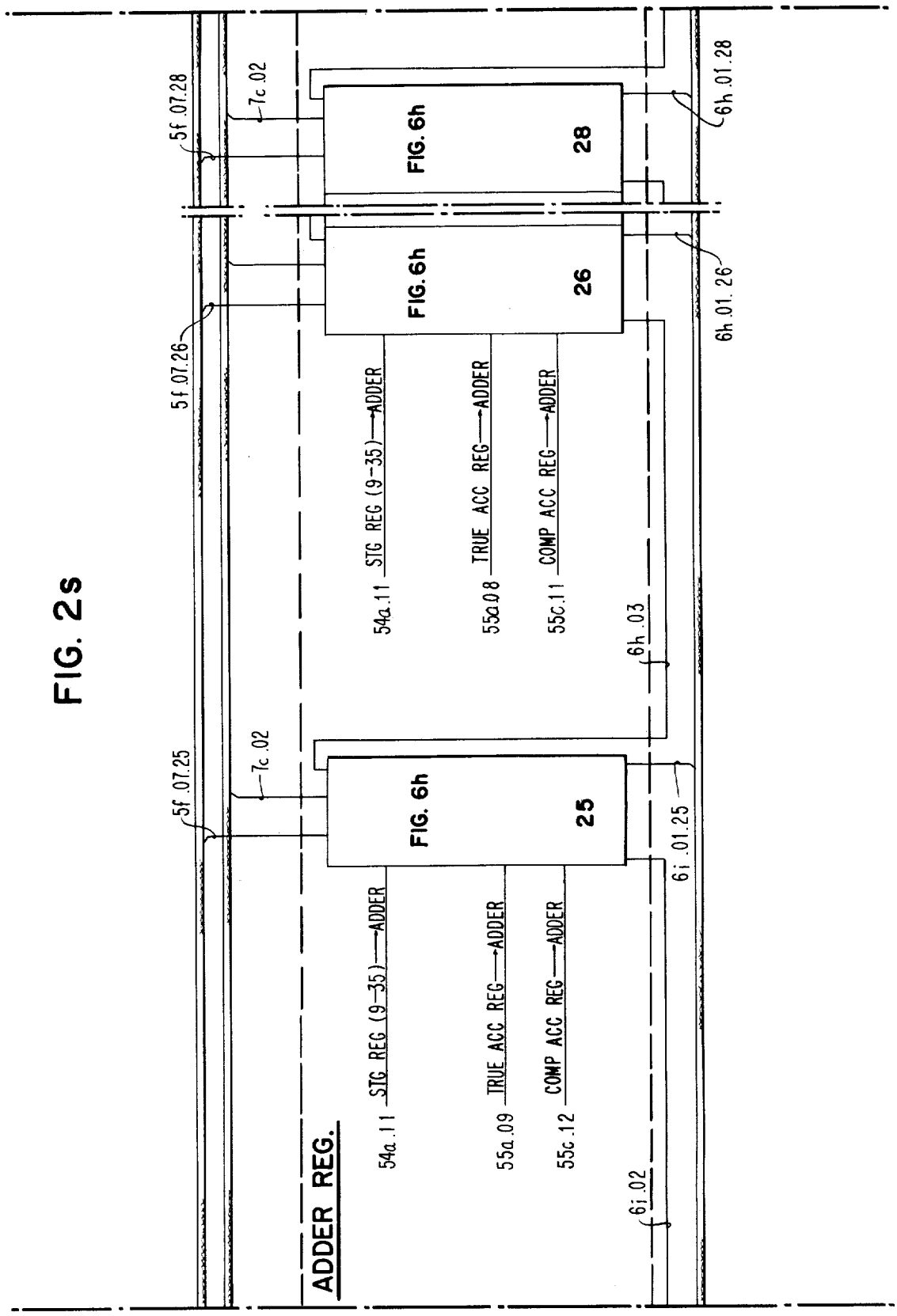

5f .07.28
7c .02
FIG. 6h
28
6h .01.28
FIG. 6h
26
6h .01. 26
5f .07.26
54a.11 STG REG (9-35)→ADDER
55a 08 TRUE ACC REG→ADDER
55c.11 COMP ACC REG→ADDER
6h .03
5f .07.25
7c .02
FIG. 6h
25
6i .01.25
ADDER REG.
54a .11 STG REG (9-35)→ADDER
55a .09 TRUE ACC REG→ADDER
55c .12 COMP ACC REG→ADDER
6i .02

FIG. 2t

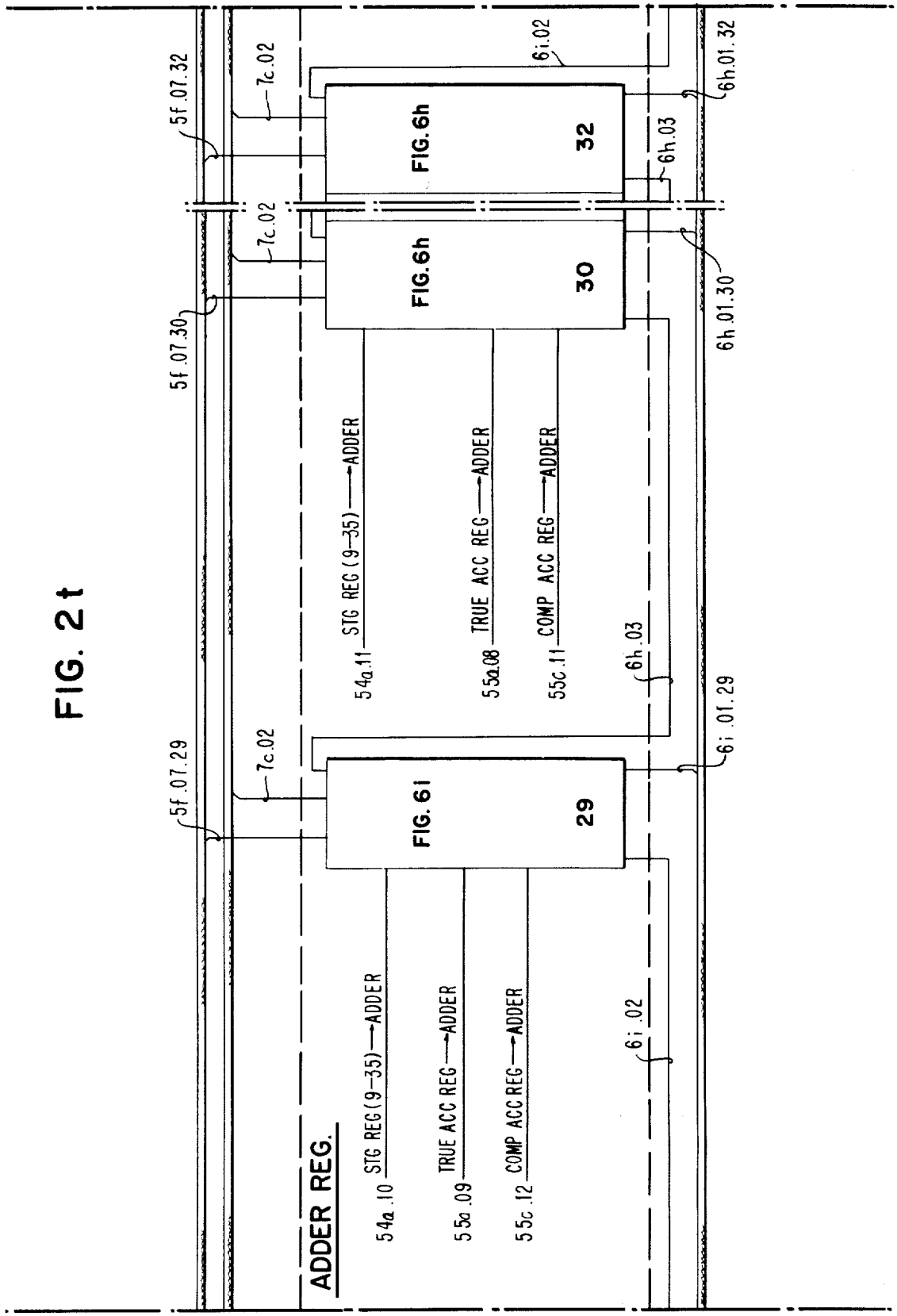
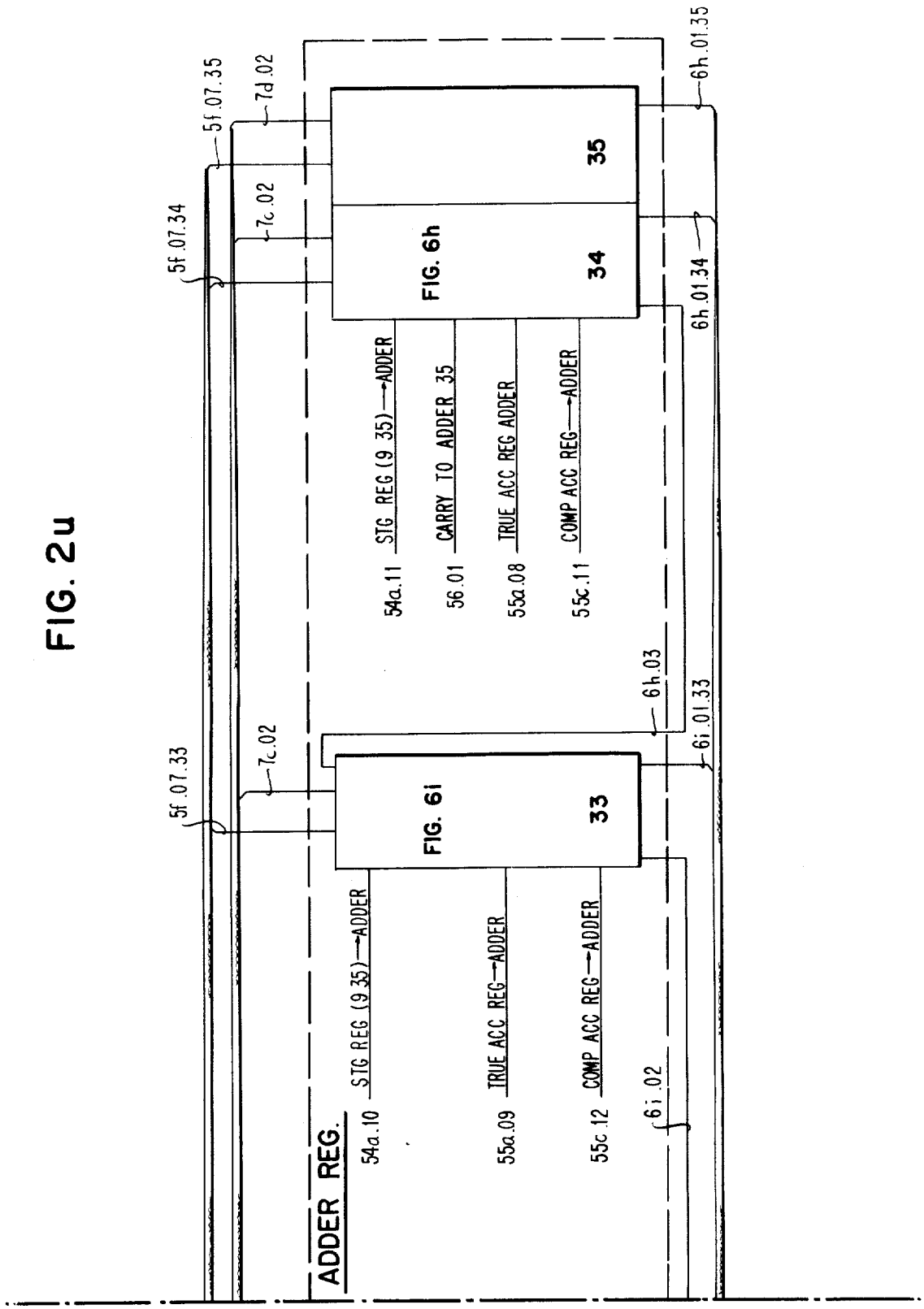

5f .07.32
7c.02
6i.02
6h.01.32
FIG.6h
32
6h.03
5f .07.30
7c.02
FIG.6h
30
6h.01.30
54a.11 STG REG (9-35) → ADDER
55a.08 TRUE ACC REG → ADDER
55c.11 COMP ACC REG → ADDER
6h.03
5f .07.29
7c.02
FIG. 6I
29
6i .01.29
ADDER REG.
54a .10 STG REG (9-35) → ADDER
55a .09 TRUE ACC REG → ADDER
55c .12 COMP ACC REG → ADDER
6i .02

FIG. 2u


5f.07.35
7d.02
6h.01.35
5f.07.34
7c.02
FIG. 6h
35
34
6h.01.34
54a.11 STG REG (9 35)→ADDER
56.01 CARRY TO ADDER 35
55a.08 TRUE ACC REG ADDER
55c.11 COMP ACC REG→ADDER
6h.03
6i.01.33
5f.07.33
7c.02
FIG. 6i
33
ADDER REG.
54a.10 STG REG (9 35)→ADDER
55a.09 TRUE ACC REG→ADDER
55c.12 COMP ACC REG→ADDER
6i.02

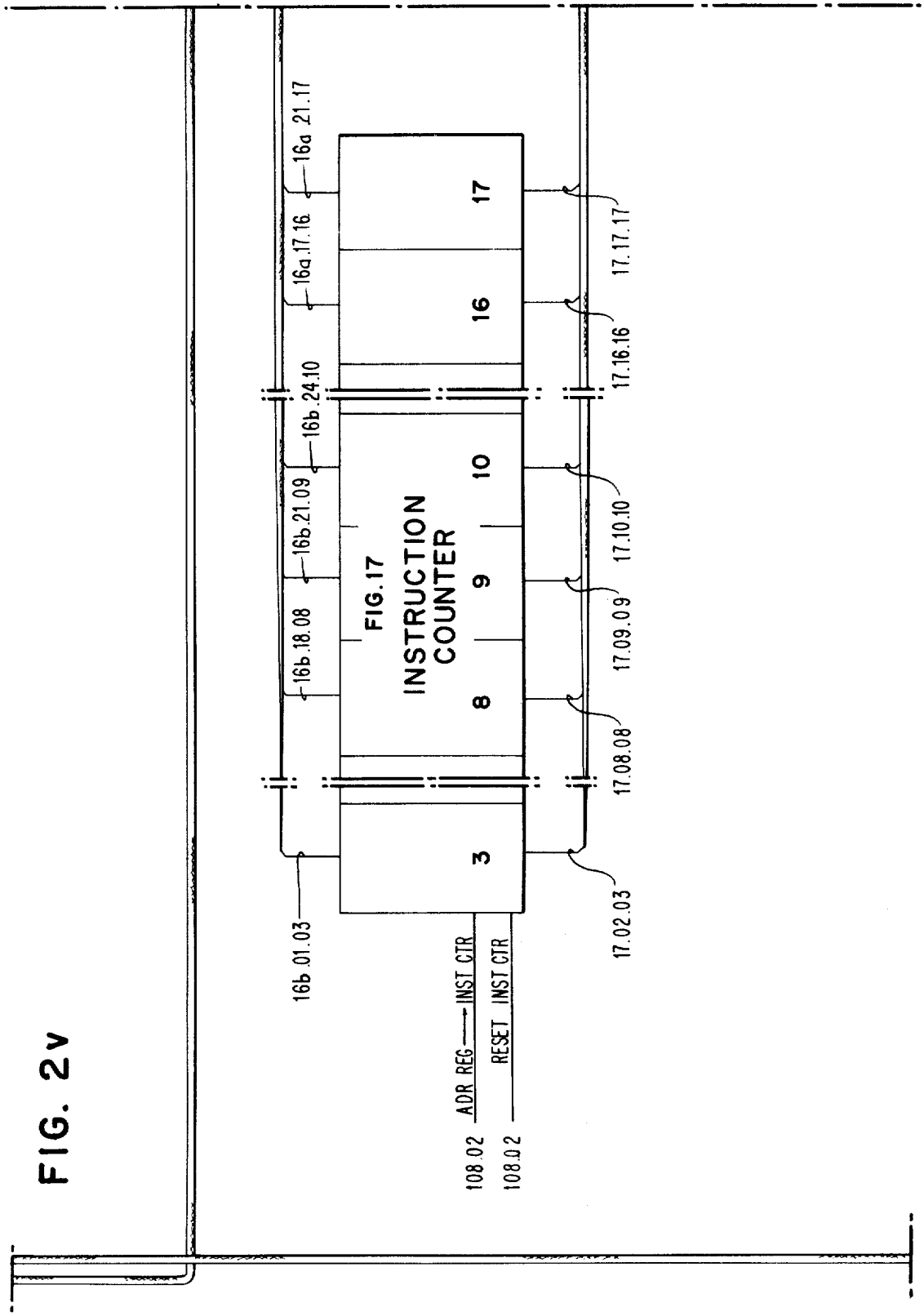
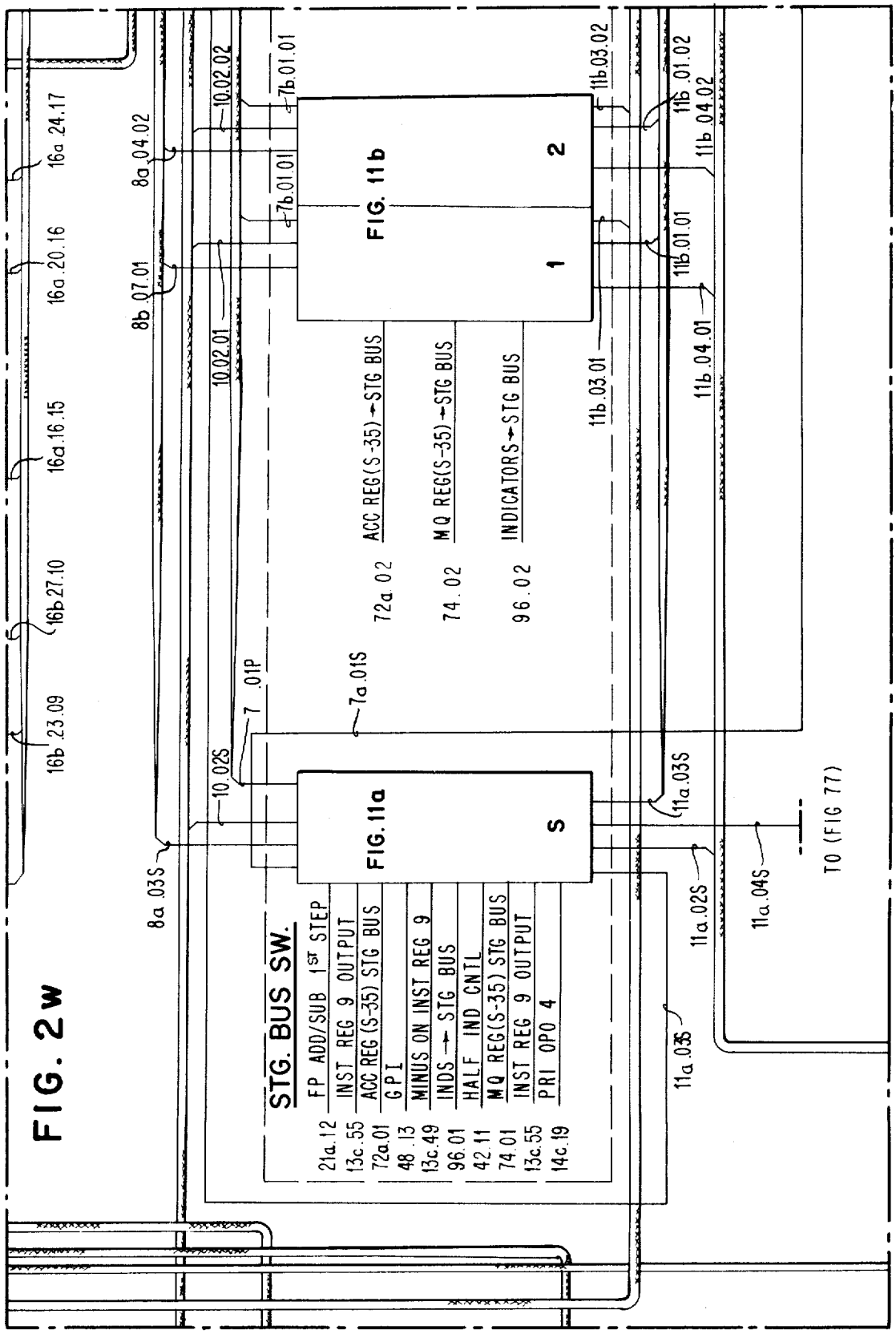
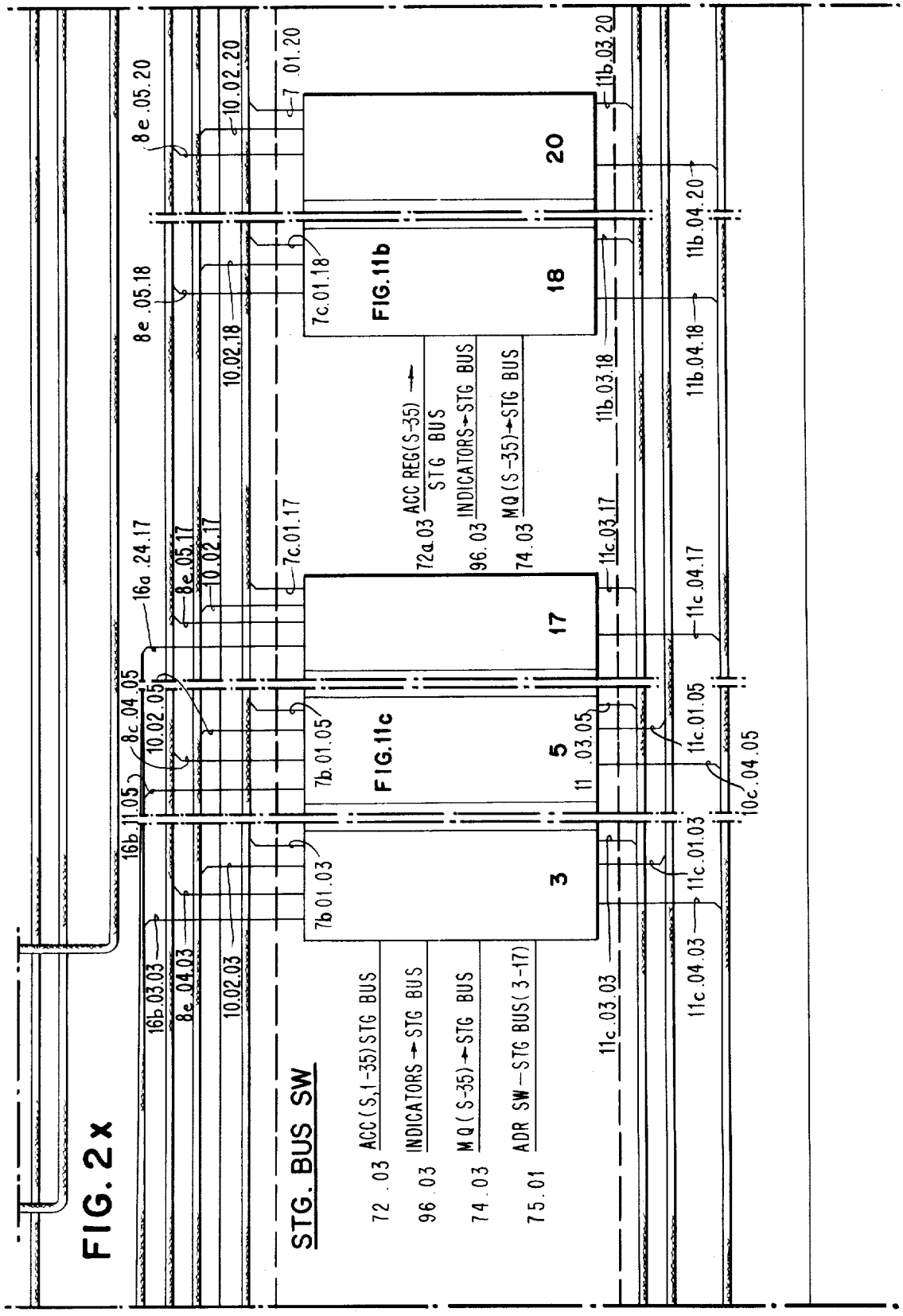

16a 21.17
16a.17.16
16b .24.10
16b.21.09
16b.18.08
16b .01.03
FIG.17
INSTRUCTION COUNTER
17
16
10
9
8
3
17.17.17
17.16.16
17.10.10
17.09.09
17.08.08
17.02.03
108.02 ADR REG INST CTR
108.02 RESET INST CTR

FIG. 2v


FIG. 2w
16b 23.09
16b 27.10
16a.16.15
16a.20.16
16a 24.17
8a .03S
8b 07.01
8a .04.02
10.02S
7 .01P
10.02.01
10.02.02
7a .01S
7b.01.01
7b.01.01
FIG. 11a
FIG. 11b
S
1
2
72a. 02
74. 02
96. 02
ACC REG(S-35)→STG BUS
MQ REG(S-35)→STG BUS
INDICATORS→STG BUS
11b.03.01
11b.03.02
11b.01.01
11b .01.02
11b .04.02
11b .04.01
11a.03S
11a.02S
11a.04S
11a.03S
TO (FIG 77)
STG. BUS SW.
21a.12 FP ADD/SUB 1ST STEP
13c.55 INST REG 9 OUTPUT
72a.01 ACC REG (S-35) STG BUS
48 .13 GPI
13c.49 MINUS ON INST REG 9
96.01 INDS → STG BUS
42.11 HALF IND CNTL
74.01 MQ REG(S-35) STG BUS
13c.55 INST REG 9 OUTPUT
14c.19 PRI OPO 4


FIG. 2x
STG. BUS SW
72 .03 ACC(S,1-35)STG BUS
96 .03 INDICATORS→STG BUS
74 .03 MQ(S-35)→STG BUS
75 .01 ADR SW→STG BUS(3-17)
16b .11 .05
16b.03.03
8e .04.03
10.02.03
8c .04.05
10.02.05
16a .24.17
8e .05.17
10.02.17
8e .05.18
10.02.18
8e .05.20
10.02.20
7b.01.03
7b.01.05
7c.01.17
7c.01.18
7 .01.20
11b.03.20
3
5
17
18
20
FIG.11c
FIG.11b
72a.03 ACC REG(S-35) → STG BUS
96. 03 INDICATORS→STG BUS
74. 03 MQ(S-35)→STG BUS
11 .03.05
11c.03.03
11c.03.17
11b.03.18
11c.01.03
11c.01.05
11c.04.03
11c.04.17
11b.04.18
11b.04.20
10c.04.05

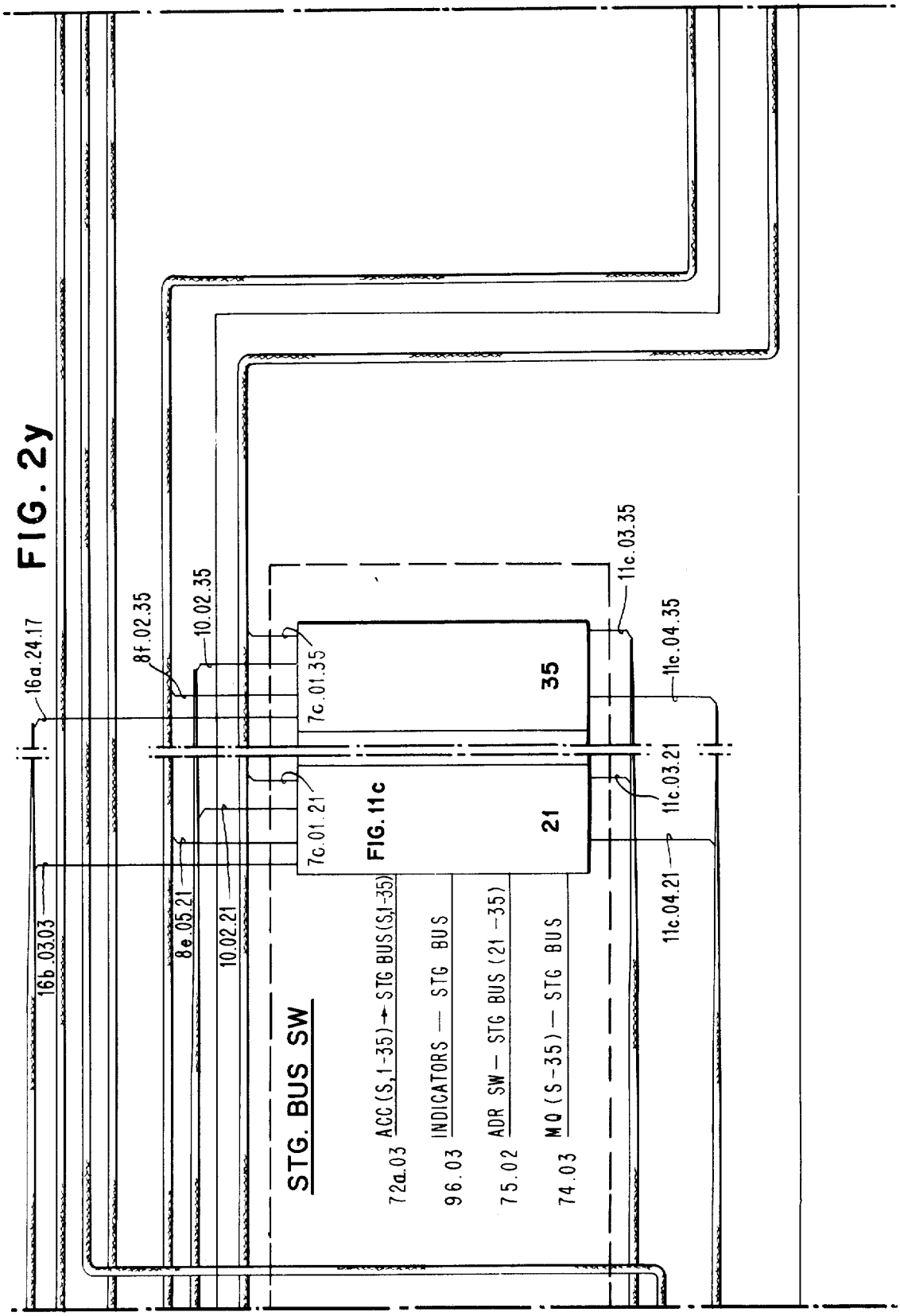
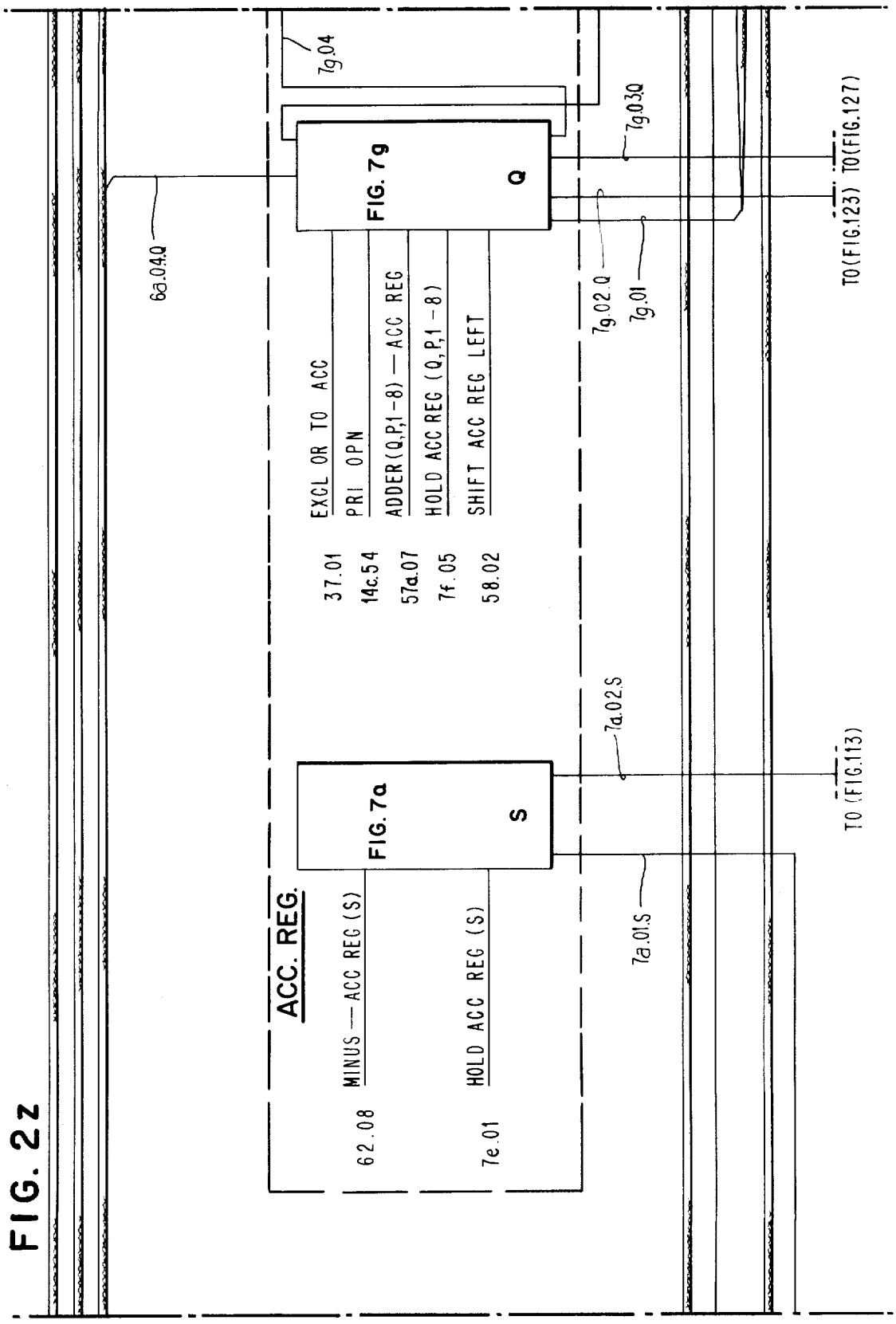
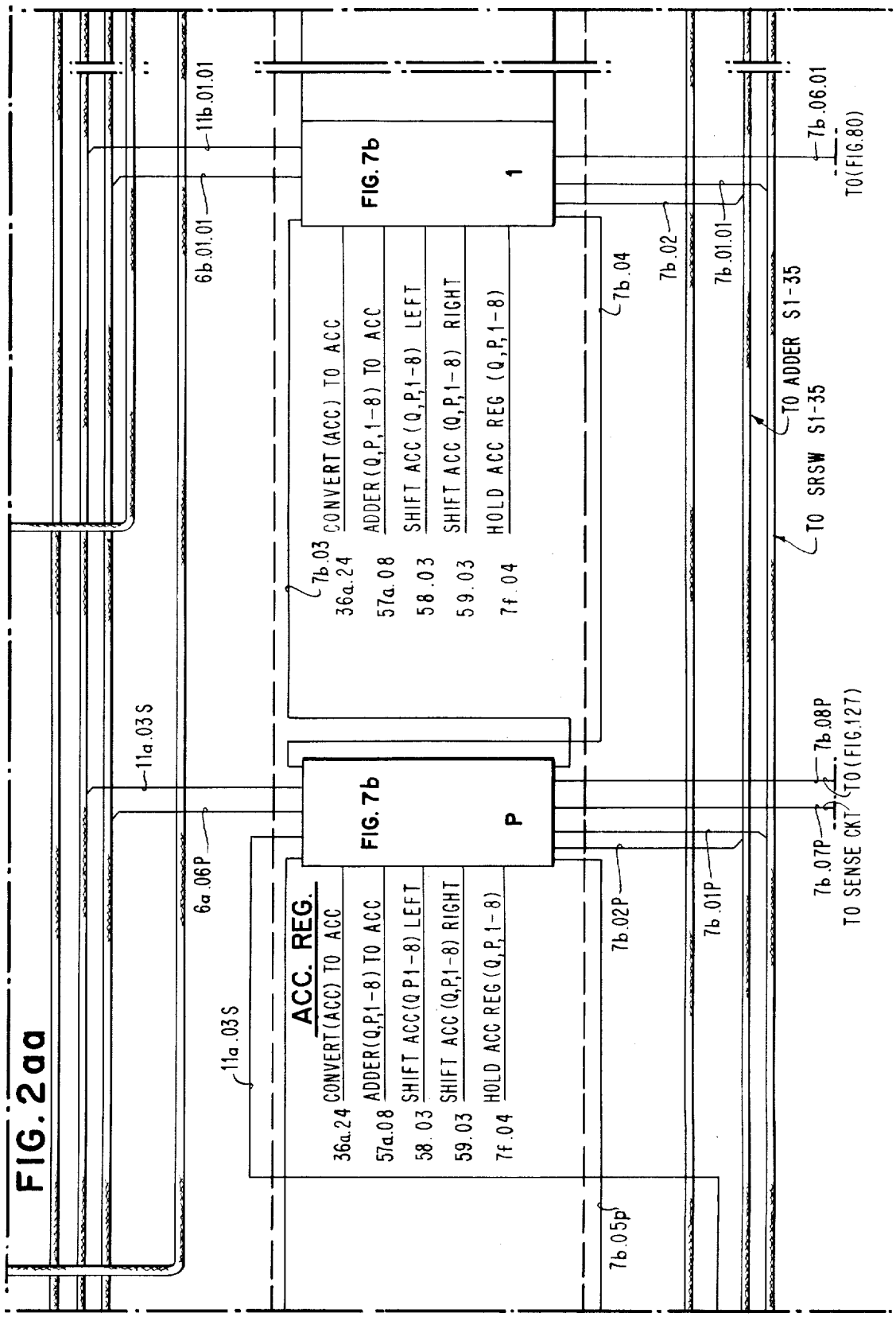
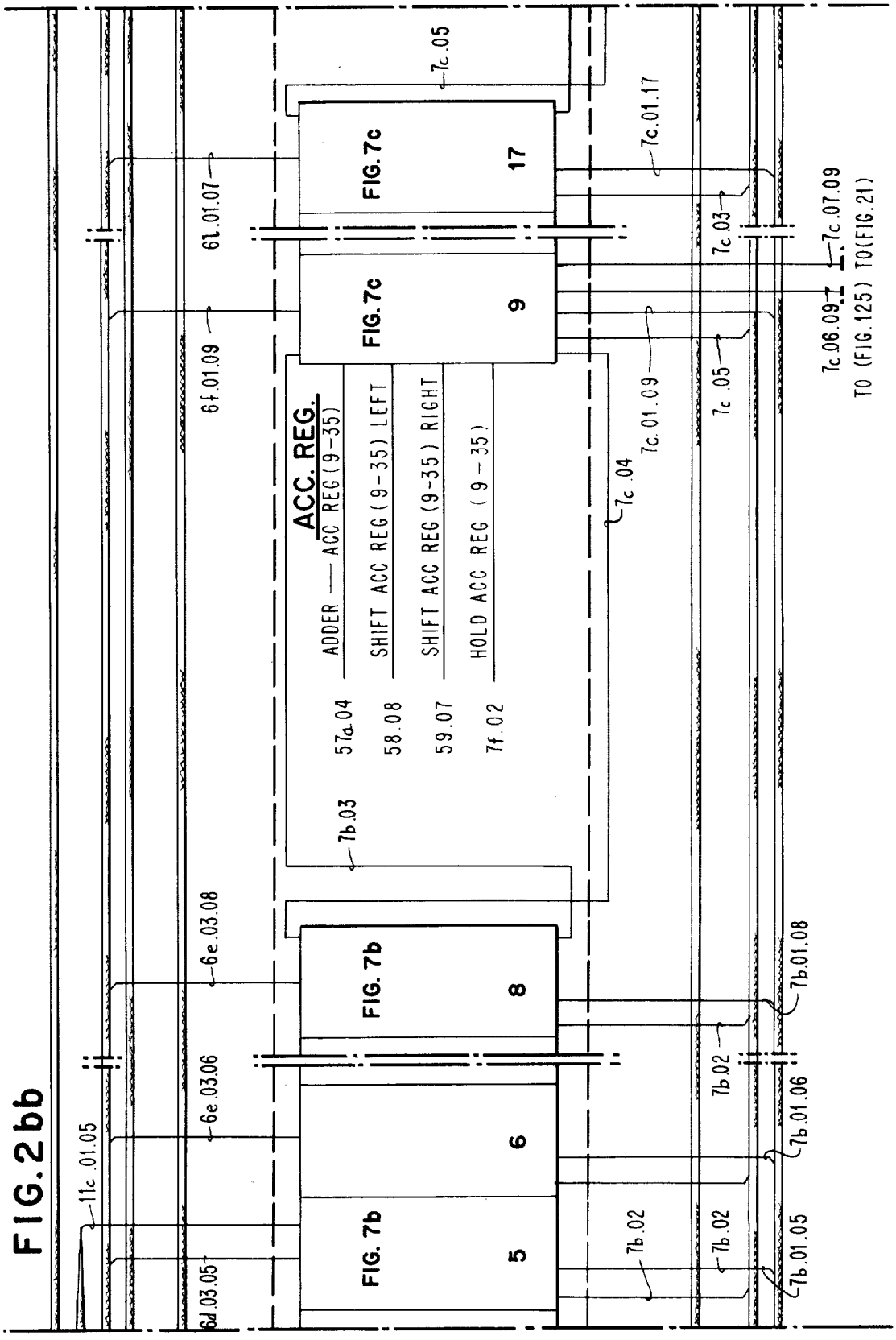
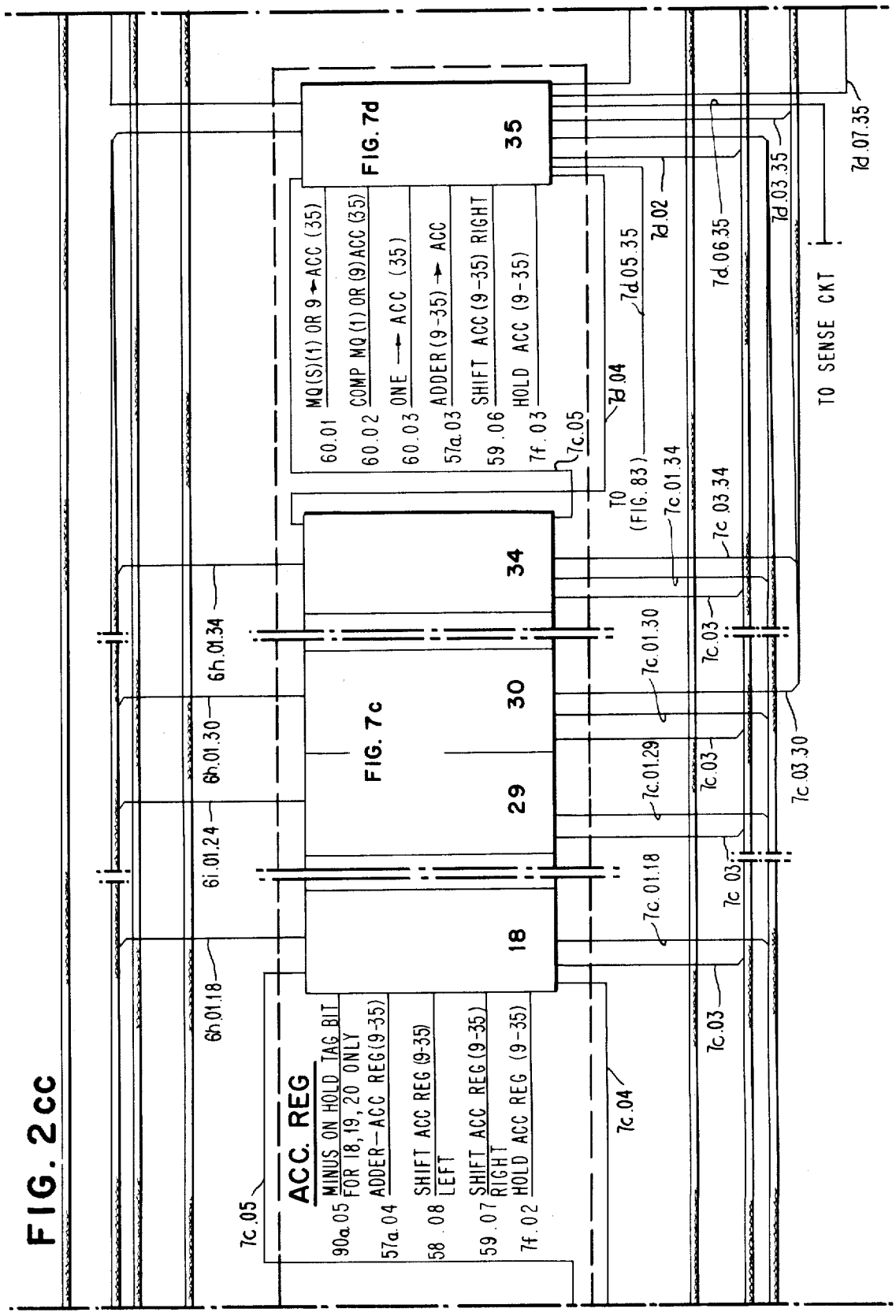

16a.24.17
8f.02.35
10.02.35
11c.03.35
11c.04.35
7c.01.35
35
7c.01.21
FIG. 11c
21
11c.03.21
16b.03.03
8e.05.21
10.02.21
11c.04.21
STG. BUS SW
72a.03 ACC (S,1-35) → STG BUS (S1-35)
96.03 INDICATORS — STG BUS
75.02 ADR SW — STG BUS (21-35)
74.03 MQ (S-35) — STG BUS

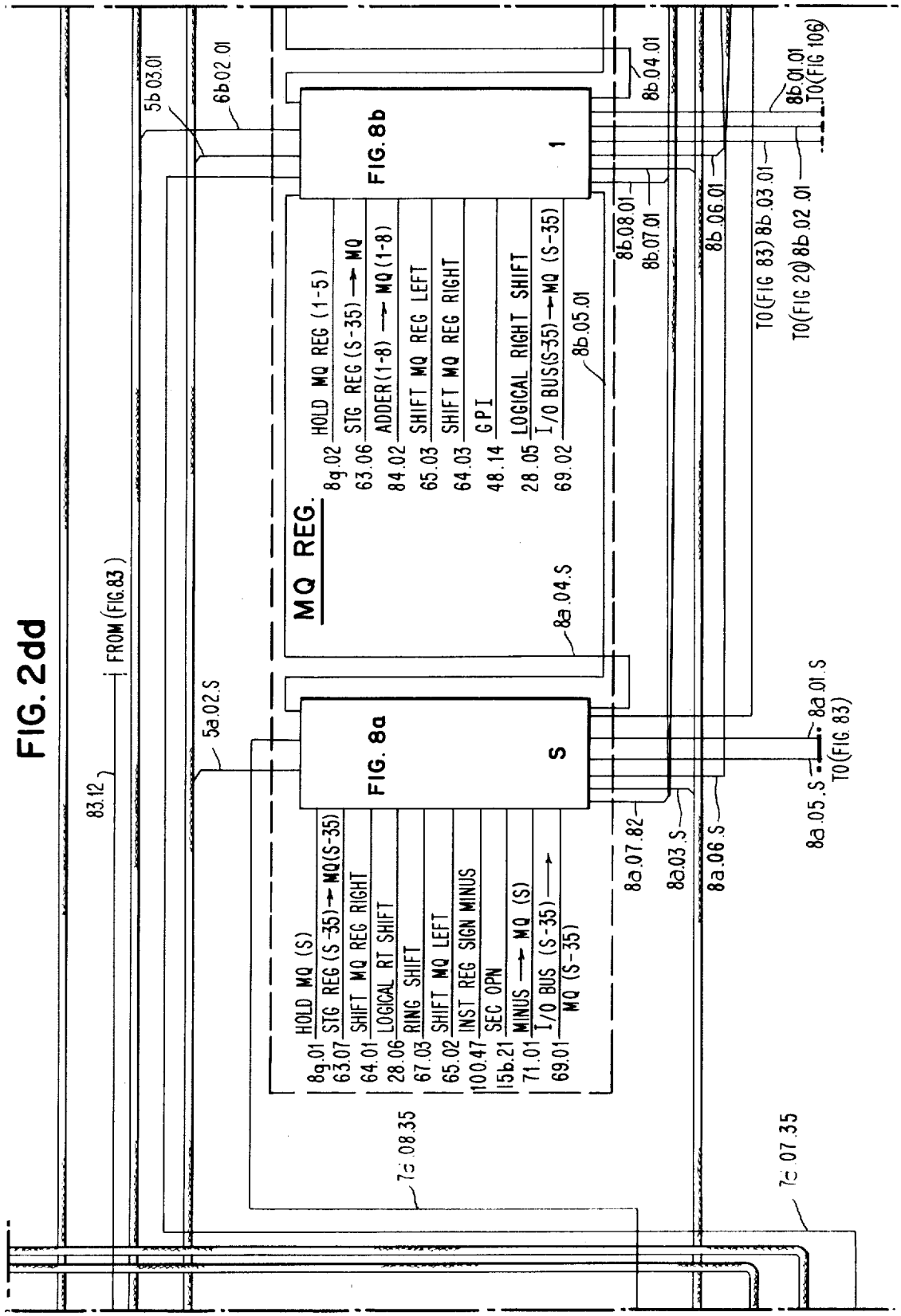
FIG. 2y


FIG. 2z
ACC. REG.
FIG. 7a
S
62.08
MINUS — ACC REG (S)
7e.01
HOLD ACC REG (S)
7a.01.S
7a.02.S
TO (FIG.113)
FIG. 7g
Q
37.01
EXCL OR TO ACC
14c.54
PRI OPN
57a.07
ADDER (Q,P,1-8) — ACC REG
7f.05
HOLD ACC REG (Q,P,1-8)
58.02
SHIFT ACC REG LEFT
6a.04.Q
7g.04
7g.03.Q
7g.02.Q
7g.01
TO (FIG.123) TO (FIG.127)


FIG. 2aa
11b.01.01
6b.01.01
11a.03S
6a.06P
11a.03S
ACC. REG.
36a.24 CONVERT (ACC) TO ACC
57a.08 ADDER (Q,P,1-8) TO ACC
58.03 SHIFT ACC (Q P1-8) LEFT
59.03 SHIFT ACC (Q,P,1-8) RIGHT
7f.04 HOLD ACC REG (Q,P,1-8)
FIG. 7b
P
7b.05P
7b.02P
7b.01P
7b.07P
TO SENSE CKT
7b.08P
TO (FIG.127)
7b.03
36a.24 CONVERT (ACC) TO ACC
57a.08 ADDER (Q,P,1-8) TO ACC
58.03 SHIFT ACC (Q,P,1-8) LEFT
59.03 SHIFT ACC (Q,P,1-8) RIGHT
7f.04 HOLD ACC REG (Q,P,1-8)
FIG. 7b
1
7b.04
7b.02
7b.01.01
TO ADDER S1-35
TO SRSW S1-35
7b.06.01
TO (FIG.80)


FIG. 2bb
FIG. 7b
5
FIG. 7b
6
FIG. 7b
8
FIG. 7c
9
FIG. 7c
17
ACC. REG.
ADDER — ACC REG (9-35)
SHIFT ACC REG (9-35) LEFT
SHIFT ACC REG (9-35) RIGHT
HOLD ACC REG (9-35)
57a.04
58.08
59.07
7f.02
7b.03
7c.04
7c.05
7c.01.09
7c.01.17
7c.03
7c.07.09
7c.06.09
TO (FIG.125) TO(FIG.21)
6f.01.09
6l.01.07
6e.03.08
6e.03.06
6d.03.05
11c.01.05
7b.02
7b.01.08
7b.01.06
7b.01.05


FIG. 2cc
ACC. REG
90a.05 MINUS ON HOLD TAG BIT FOR 18, 19, 20 ONLY
57a.04 ADDER—ACC REG (9-35)
58 .08 SHIFT ACC REG (9-35) LEFT
59 .07 SHIFT ACC REG (9-35) RIGHT
7f .02 HOLD ACC REG (9-35)
7c.05
6h.01.18
6i.01.24
6h.01.30
6h.01.34
18
29
30
34
FIG. 7c
60.01 MQ(S)(1) OR 9 → ACC (35)
60.02 COMP MQ (1) OR (9) ACC (35)
60.03 ONE → ACC (35)
57a.03 ADDER (9-35) → ACC
59 .06 SHIFT ACC (9-35) RIGHT
7f .03 HOLD ACC (9-35)
35
FIG. 7d
7c.05
7d.04
TO (FIG. 83)
7c.01.34
7c.01.30
7c.01.29
7c.01.18
7c.04
7d.05 35
7d.02
7c.03.34
7c.03
7d.06.35
7d.03.35
7c.03.30
7d.07.35
TO SENSE CKT


FIG. 2dd
FROM (FIG. 83)
83.12
5a.02.S
5b.03.01
6b.02.01
MQ REG.
FIG. 8a
S
FIG. 8b
1
8g.02 HOLD MQ REG (1-5)
63.06 STG REG (S-35) → MQ
84.02 ADDER (1-8) → MQ (1-8)
65.03 SHIFT MQ REG LEFT
64.03 SHIFT MQ REG RIGHT
48.14 GPI
28.05 LOGICAL RIGHT SHIFT
69.02 I/O BUS (S-35) → MQ (S-35)
8a.04.S
8b.05.01
8b.04.01
8b.08.01
8b.07.01
8b.06.01
8b.01.01
TO (FIG 106)
TO (FIG 83) 8b.03.01
TO (FIG 20) 8b.02.01
8g.01 HOLD MQ (S)
63.07 STG REG (S-35) → MQ (S-35)
64.01 SHIFT MQ REG RIGHT
28.06 LOGICAL RT SHIFT
67.03 RING SHIFT
65.02 SHIFT MQ LEFT
100.47 INST REG SIGN MINUS
15b.21 SEC OPN
71.01 MINUS → MQ (S)
69.01 I/O BUS (S-35) → MQ (S-35)
8a.07.82
8a.03.S
8a.06.S
8a.05.S
8a.01.S
TO (FIG 83)
To 08.35
To 07.35

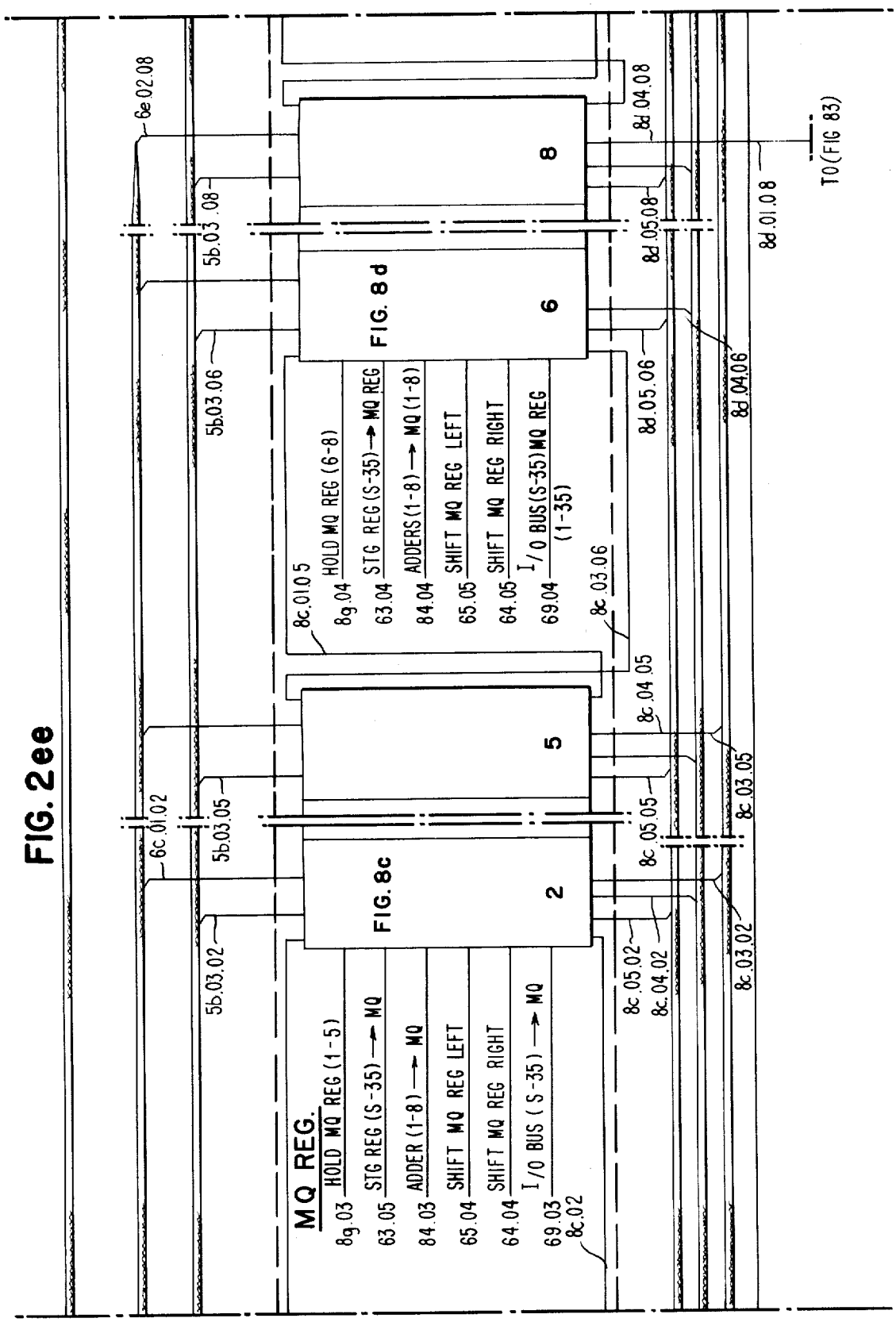
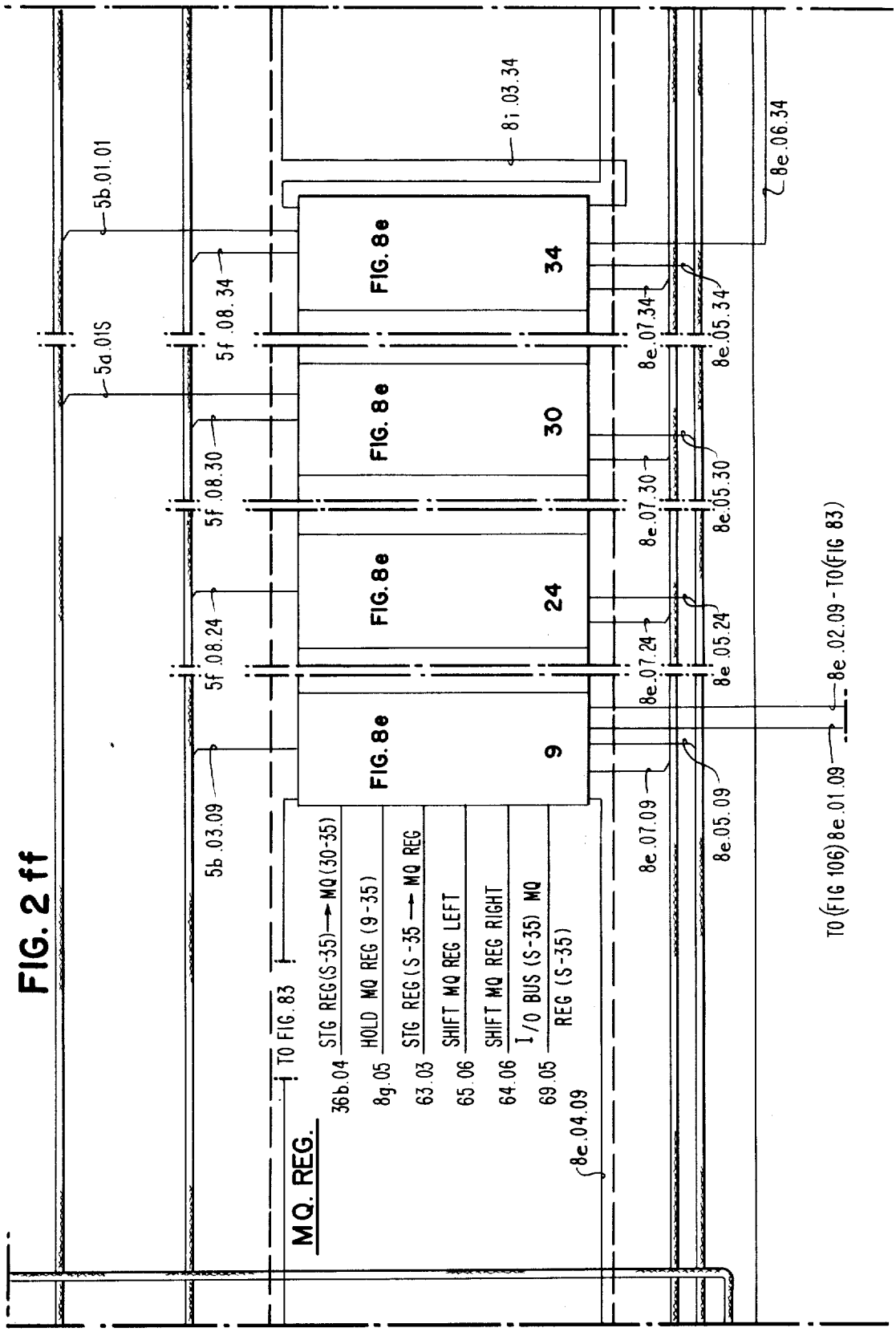

MQ REG.
8g.03 HOLD MQ REG (1-5)
63.05 STG REG (S-35) → MQ
84.03 ADDER (1-8) → MQ
65.04 SHIFT MQ REG LEFT
64.04 SHIFT MQ REG RIGHT
69.03 I/O BUS (S-35) → MQ
8c.02
FIG. 8c
2
5
FIG. 8d
6
8
8g.04 HOLD MQ REG (6-8)
63.04 STG REG (S-35) → MQ REG
84.04 ADDERS (1-8) → MQ (1-8)
65.05 SHIFT MQ REG LEFT
64.05 SHIFT MQ REG RIGHT
69.04 I/O BUS (S-35) MQ REG (1-35)
8c.01.05
8c.03.06
8c.04.05
8c.05.05
8c.03.05
8c.03.02
8c.04.02
8c.05.02
8d.05.06
8d.04.06
8d.05.08
8d.04.08
8d.01.08
TO (FIG 83)
6c.01.02
5b.03.05
5b.03.02
6e.02.08
5b.03.08
5b.03.06

FIG. 2ee


FIG. 2ff
MQ. REG.
TO FIG. 83
36b.04 STG REG(S-35)→MQ(30-35)
8g.05 HOLD MQ REG (9-35)
63.03 STG REG(S-35→MQ REG
65.06 SHIFT MQ REG LEFT
64.06 SHIFT MQ REG RIGHT
69.05 I/O BUS (S-35) MQ REG (S-35)
8e.04.09
5b.03.09
5f.08.24
5f.08.30
5a.01S
5b.01.01
5f.08.34
8i.03.34
8e.06.34
FIG. 8e
9
24
30
34
8e.07.09
8e.07.24
8e.07.30
8e.07.34
8e.05.09
8e.05.24
8e.05.30
8e.05.34
8e.01.09
8e.02.09
TO (FIG 106)
TO (FIG 83)

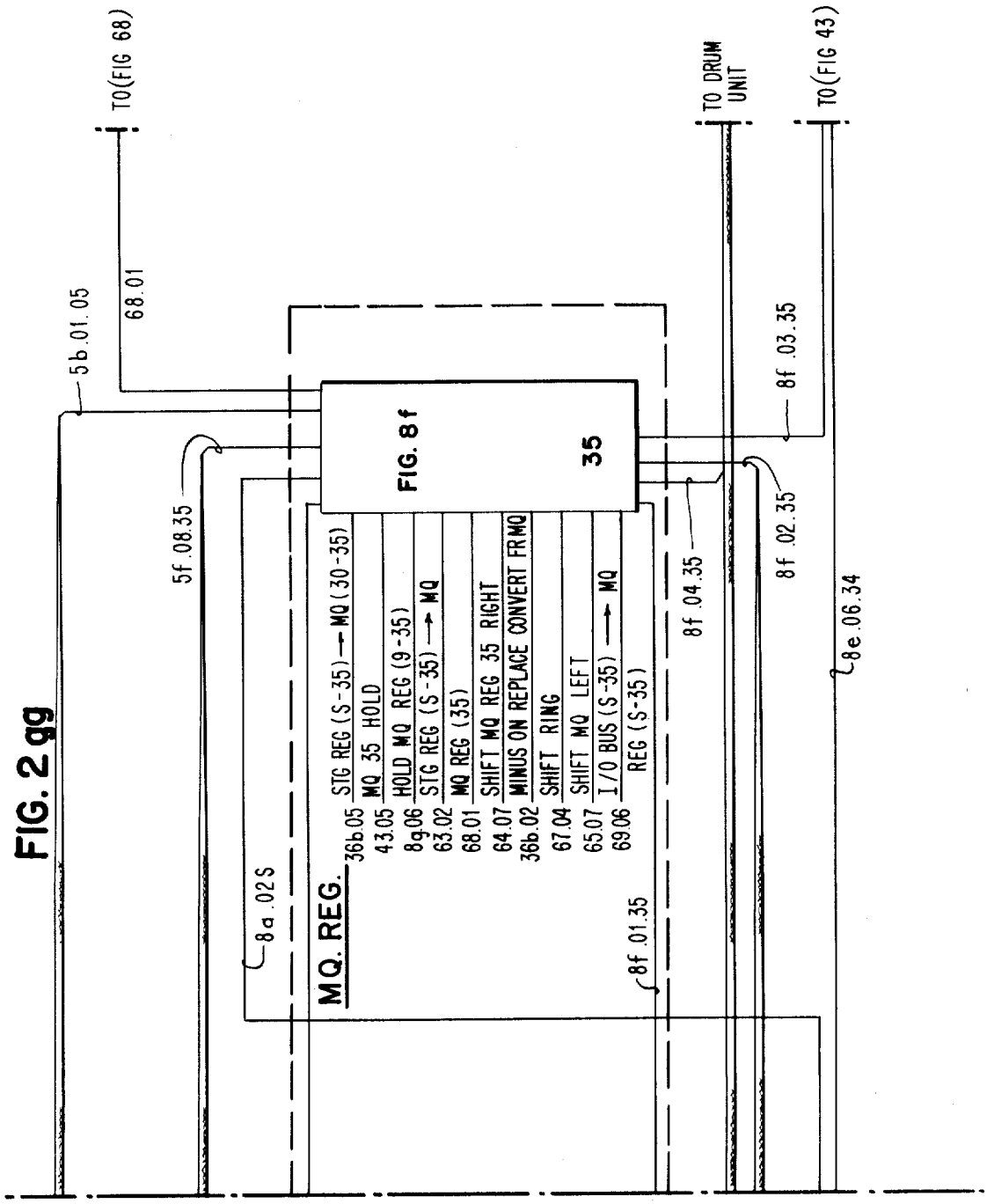

TO(FIG 68)
68.01
5b.01.05
5f.08.35
8a.02S
MQ. REG.
36b.05 STG REG (S-35) → MQ (30-35)
43.05 MQ 35 HOLD
8q.06 HOLD MQ REG (9-35)
63.02 STG REG (S-35) → MQ
68.01 MQ REG (35)
64.07 SHIFT MQ REG 35 RIGHT
36b.02 MINUS ON REPLACE CONVERT FR MQ
67.04 SHIFT RING
65.07 SHIFT MQ LEFT
69.06 I/O BUS (S-35) → MQ
REG (S-35)
8f.01.35
FIG. 8f
35
8f.04.35
TO DRUM UNIT
8f.03.35
8f.02.35
TO(FIG 43)
8e.06.34

FIG. 2gg

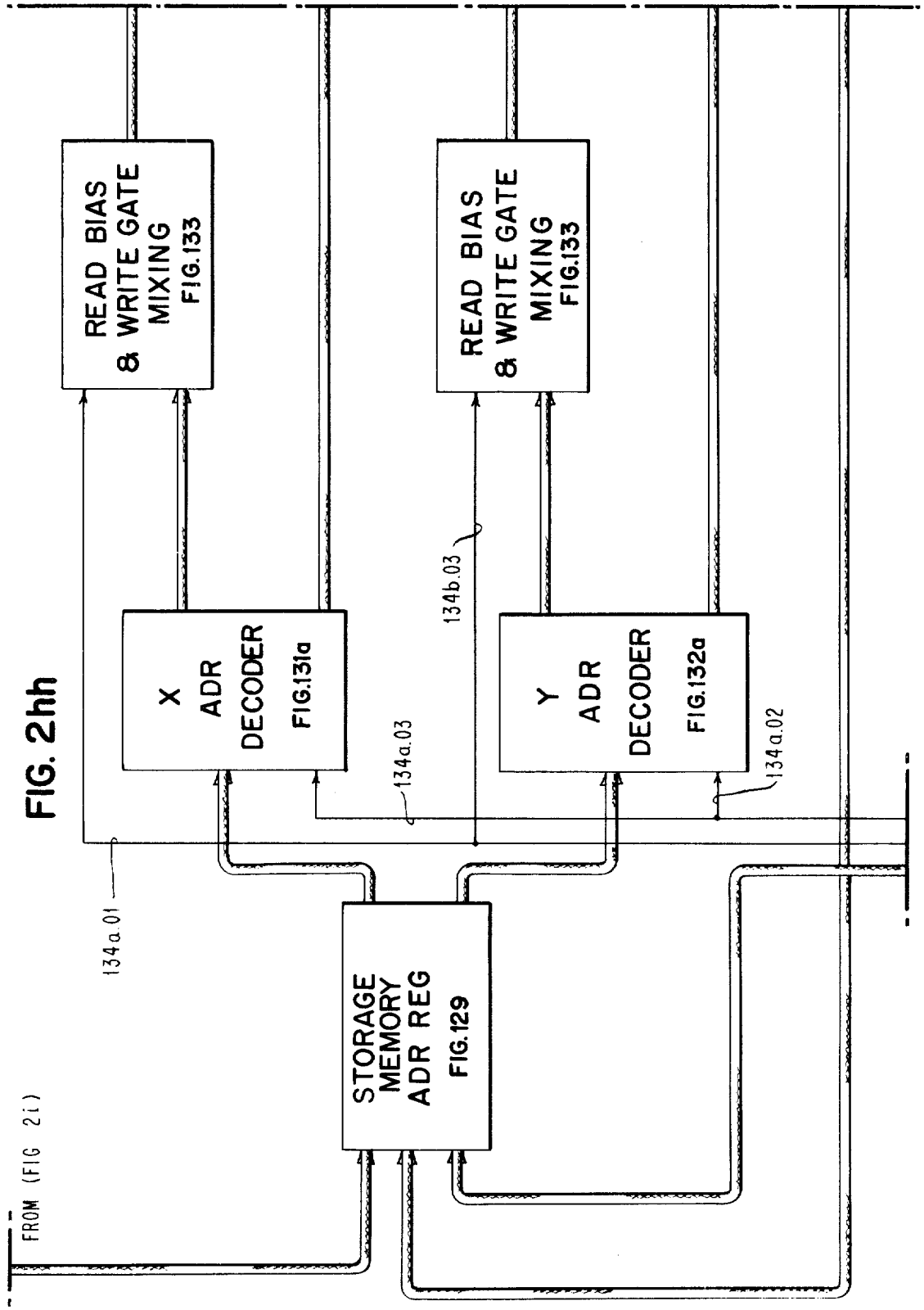

READ BIAS & WRITE GATE MIXING FIG.133
READ BIAS & WRITE GATE MIXING FIG.133
X ADR DECODER FIG.131a
Y ADR DECODER FIG.132a
134b.03
134a.03
134a.02
134a.01
STORAGE MEMORY ADR REG FIG.129
FROM (FIG 2i)

FIG. 2hh

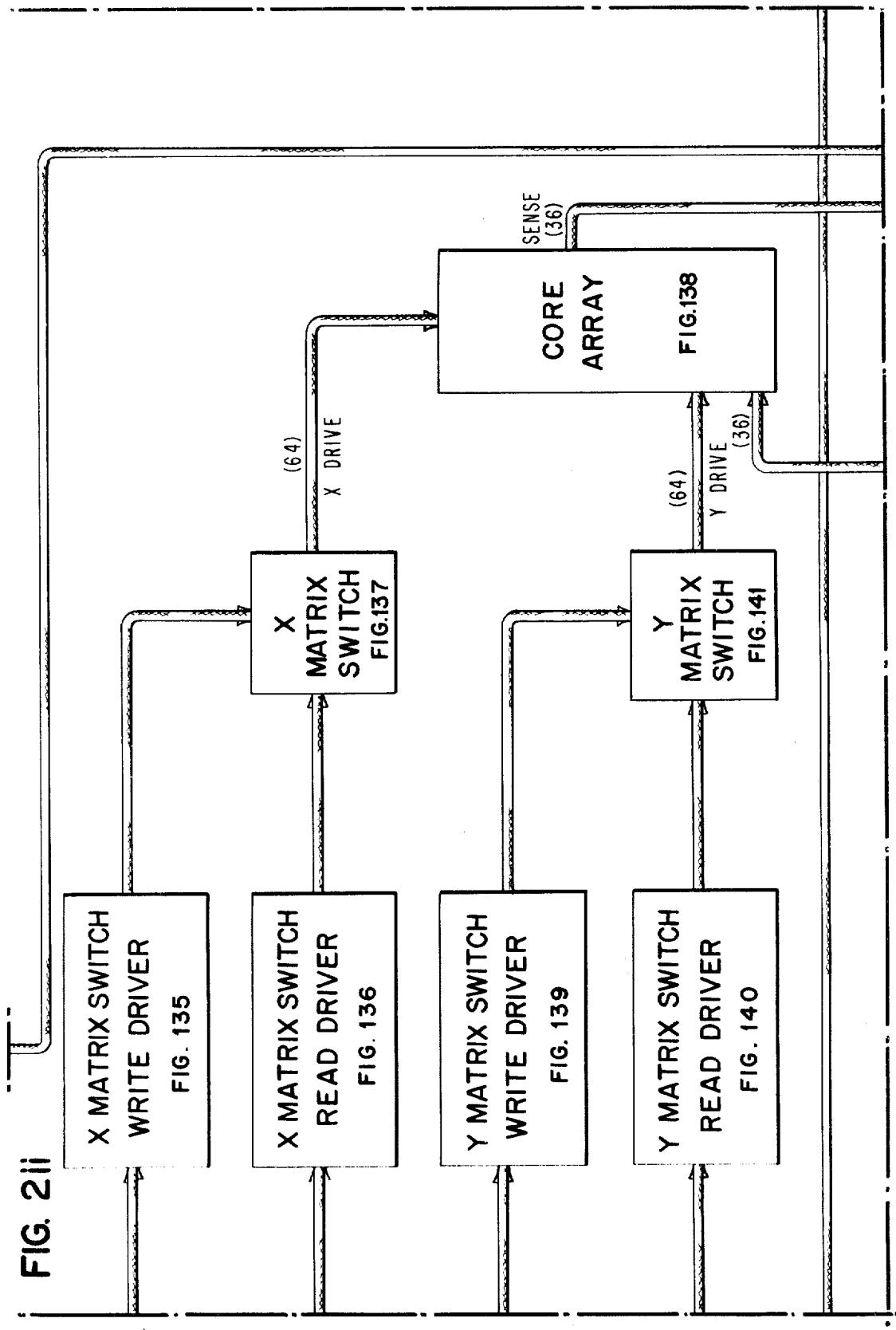

X MATRIX SWITCH WRITE DRIVER FIG. 135
X MATRIX SWITCH READ DRIVER FIG. 136
Y MATRIX SWITCH WRITE DRIVER FIG. 139
Y MATRIX SWITCH READ DRIVER FIG. 140
X MATRIX SWITCH FIG. 137
Y MATRIX SWITCH FIG. 141
(64) X DRIVE
(64) Y DRIVE
(36)
SENSE (36)
CORE ARRAY FIG. 138

FIG. 2ii

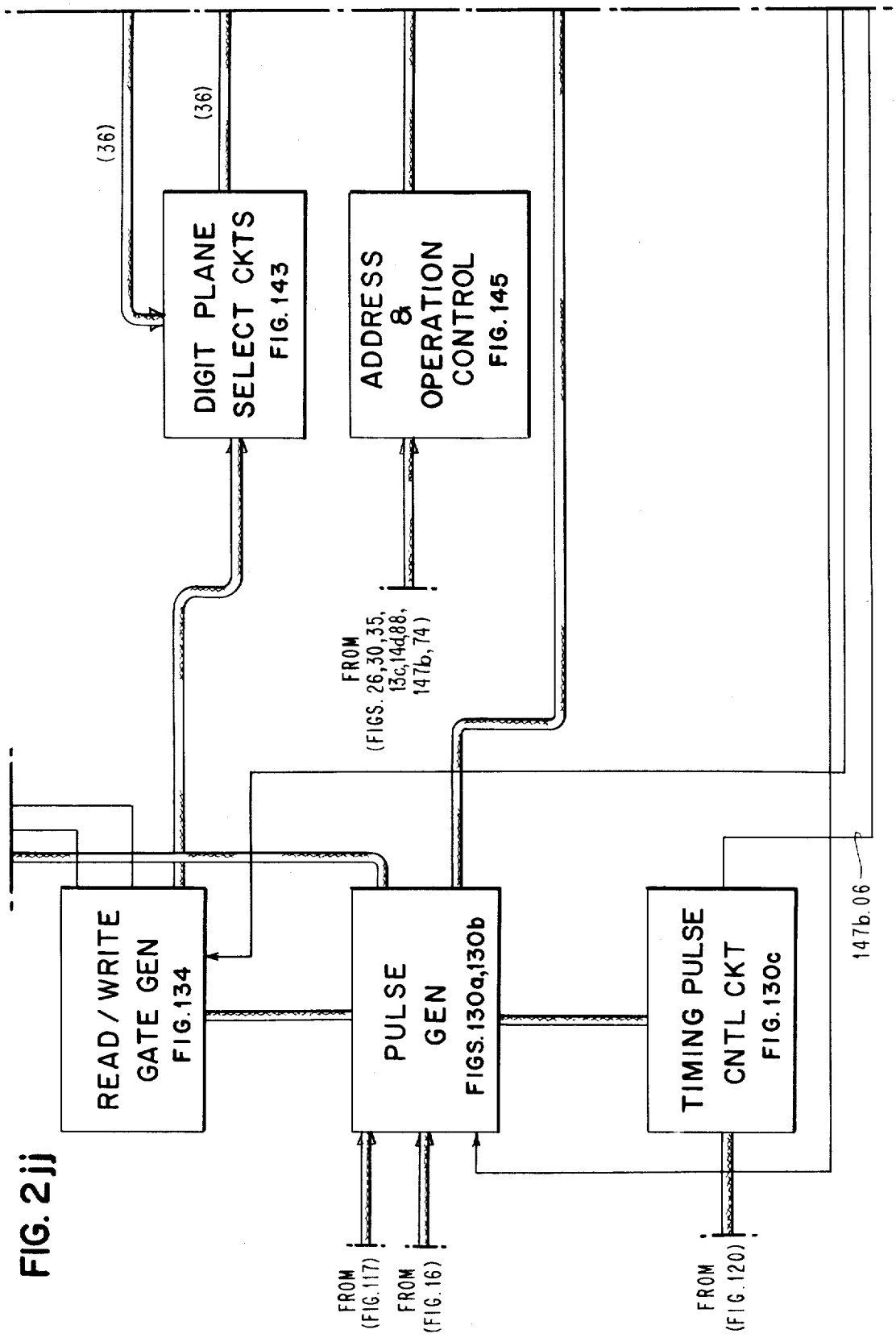

(36)
(36)
DIGIT PLANE SELECT CKTS FIG. 143
ADDRESS & OPERATION CONTROL FIG. 145
FROM (FIGS. 26,30,35, 13c,14d,88, 147b,74)
READ / WRITE GATE GEN FIG. 134
PULSE GEN FIGS. 130a,130b
TIMING PULSE CNTL CKT FIG. 130c
147b.06
FROM (FIG. 117)
FROM (FIG. 16)
FROM (FIG. 120)

FIG. 2jj

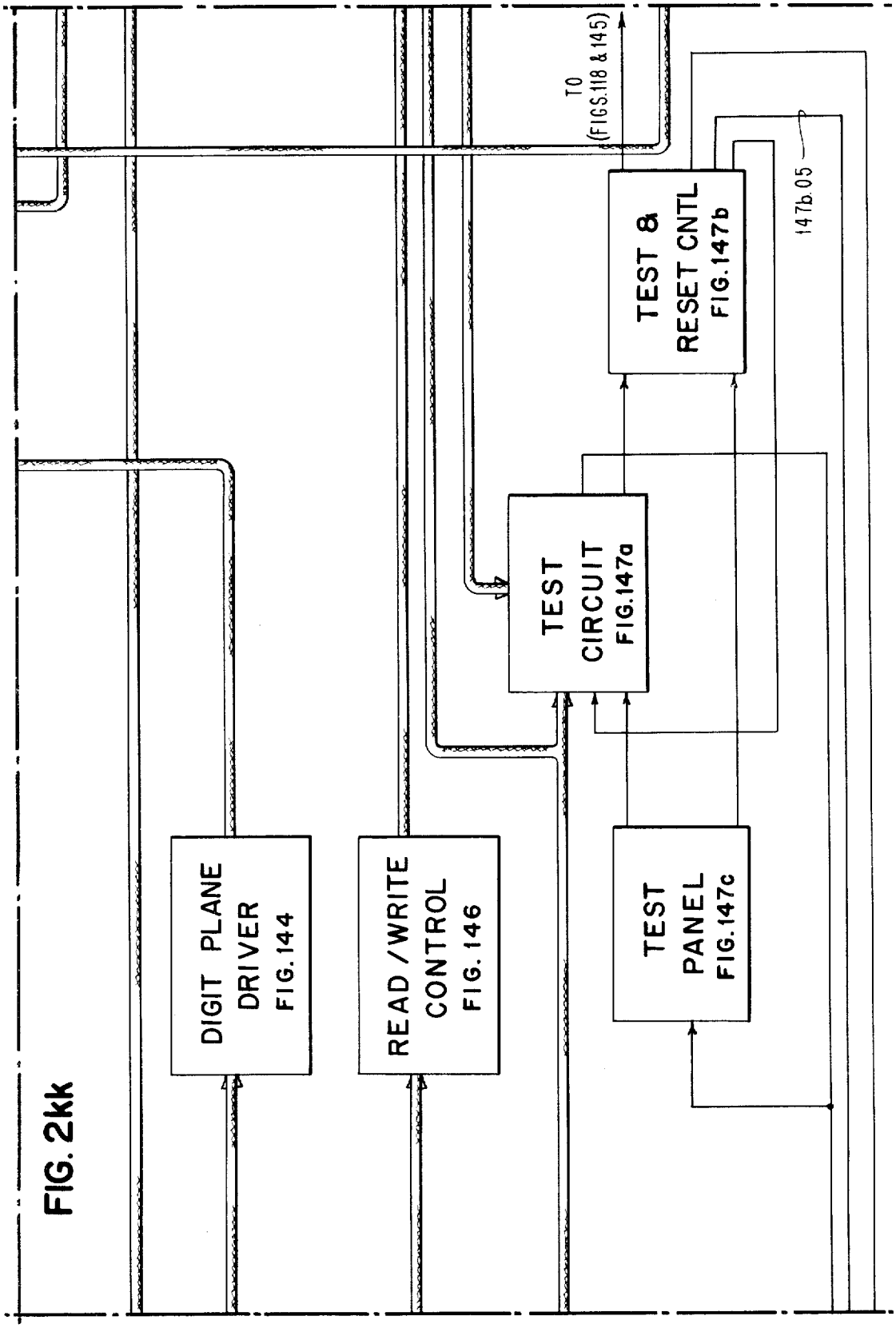

TO (FIGS.118 & 145)
147b.05
TEST & RESET CNTL FIG.147b
TEST CIRCUIT FIG.147a
TEST PANEL FIG.147c
DIGIT PLANE DRIVER FIG.144
READ/WRITE CONTROL FIG.146

FIG. 2kk

FIG. 211

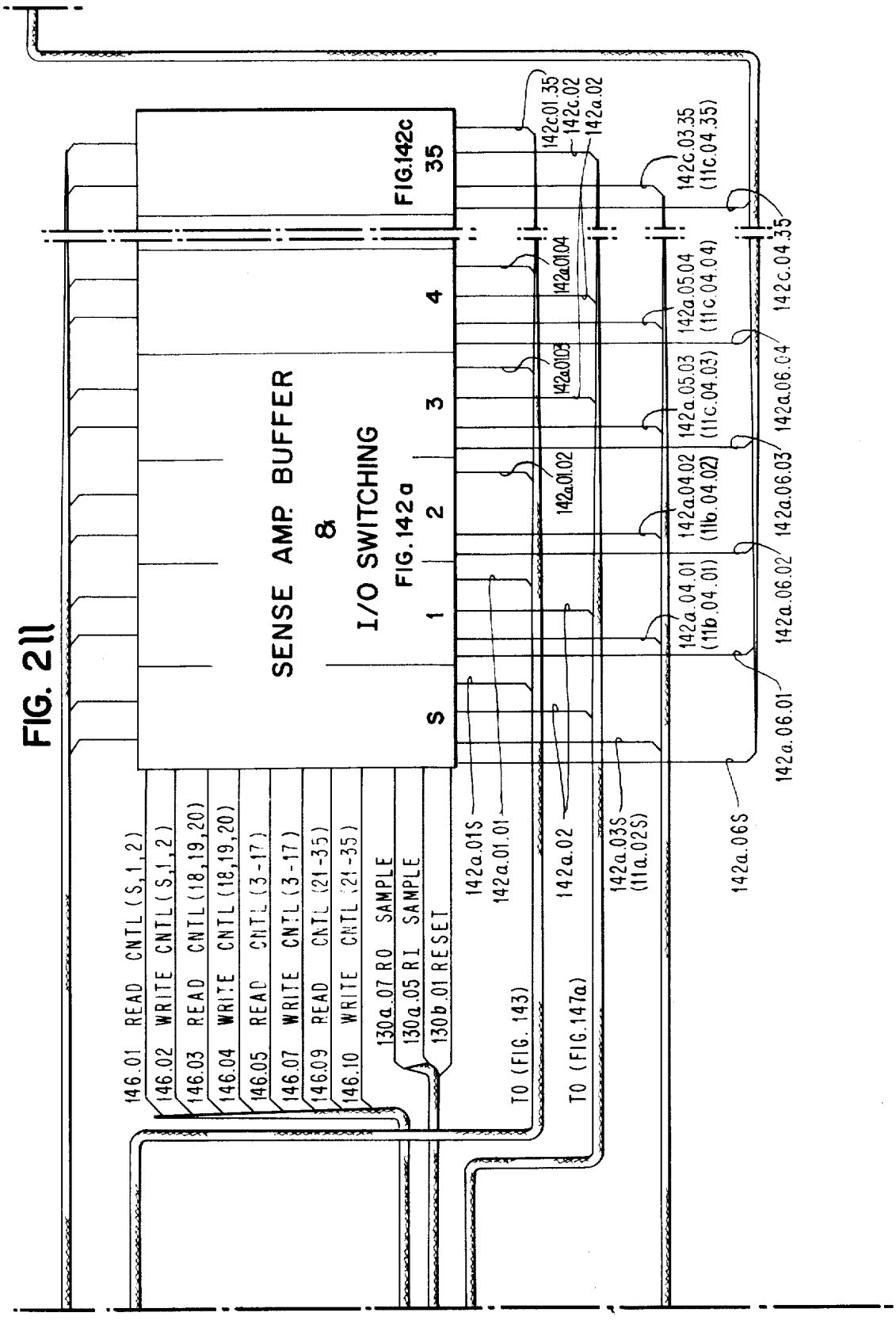

SENSE AMP BUFFER
&
I/O SWITCHING
FIG. 142a
FIG. 142c
35
4
3
2
1
S
146.01 READ CNTL (S,1,2)
146.02 WRITE CNTL (S,1,2)
146.03 READ CNTL (18,19,20)
146.04 WRITE CNTL (18,19,20)
146.05 READ CNTL (3-17)
146.07 WRITE CNTL (3-17)
146.09 READ CNTL (21-35)
146.10 WRITE CNTL (21-35)
130a.07 RO SAMPLE
130a.05 RI SAMPLE
130b.01 RESET
TO (FIG. 143)
TO (FIG. 147a)
142a.01S
142a.01.01
142a.02
142a.03S
(11a.02S)
142a.06S
142a.01.02
142a.0103
142a.0104
142c.01.35
142c.02
142a.02
142c.03.35
(11c.04.35)
142a.05.04
(11c.04.04)
142a.05.03
(11c.04.03)
142a.04.02
(11b.04.02)
142a.04.01
(11b.04.01)
142a.06.01
142a.06.02
142a.06.03
142a.06.04
142c.04.35

FIG. 2mm

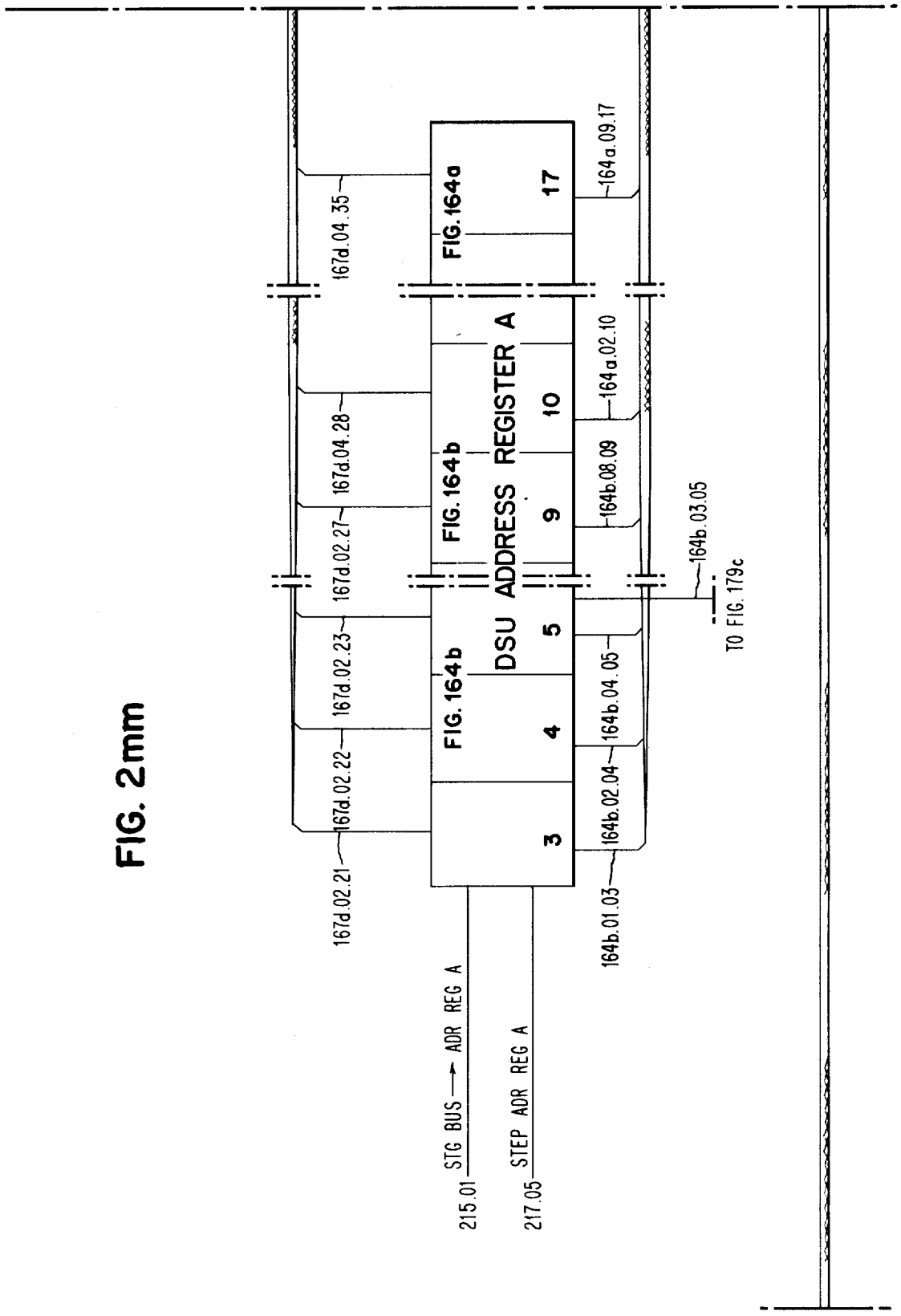
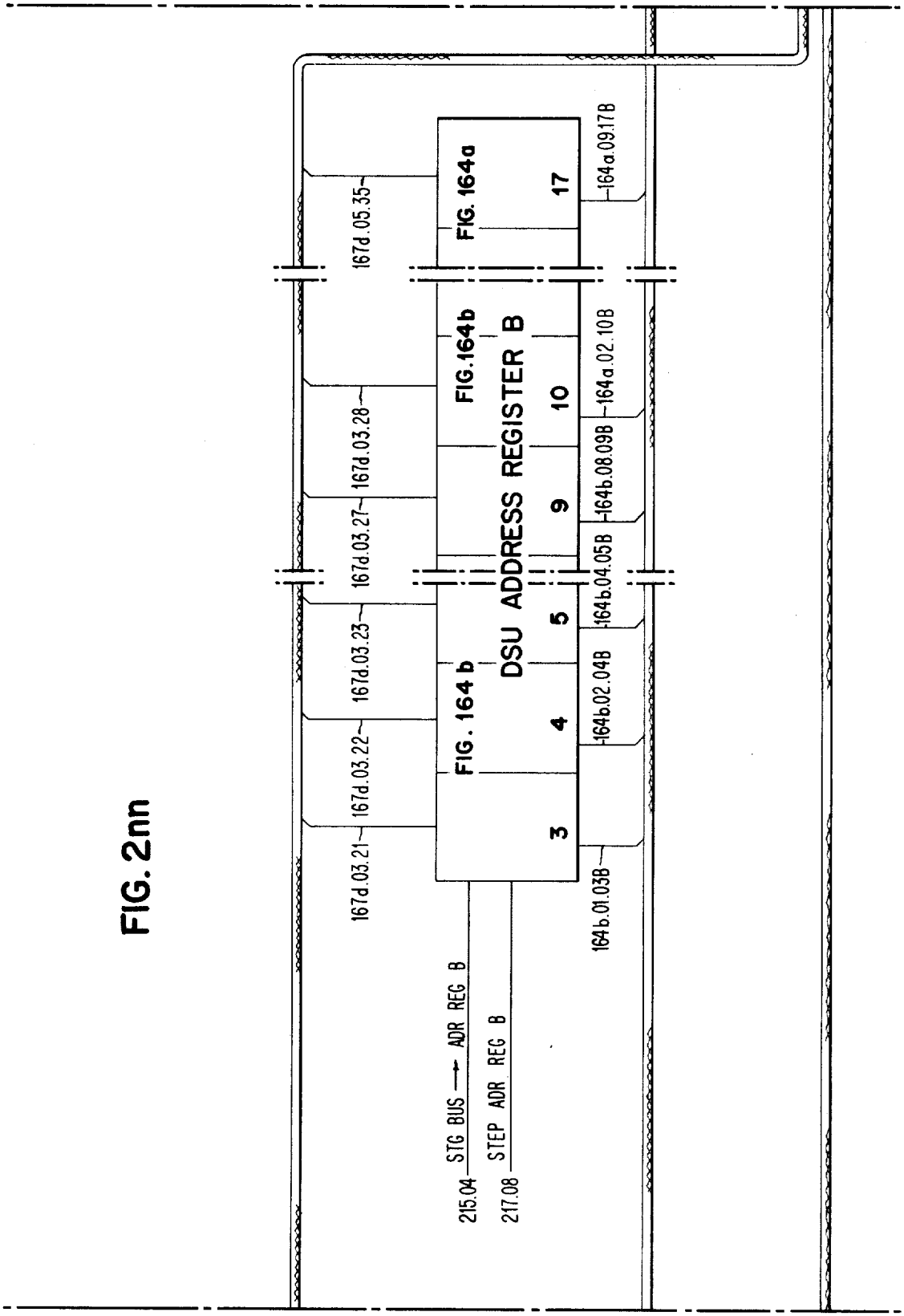

DSU ADDRESS REGISTER A
FIG. 164a
FIG. 164b
FIG. 164b
17
10
9
5
4
3
167d.04.35
167d.04.28
167d.02.27
167d.02.23
167d.02.22
167d.02.21
164a.09.17
164a.02.10
164b.08.09
164b.03.05
164b.04.05
164b.02.04
164b.01.03
TO FIG. 179c
215.01 STG BUS → ADR REG A
217.05 STEP ADR REG A

FIG. 2nn


DSU ADDRESS REGISTER B
FIG. 164a
FIG. 164b
FIG. 164 b
17
10
9
5
4
3
167d.05.35
167d.03.28
167d.03.27
167d.03.23
167d.03.22
167d.03.21
164a.09.17B
164a.02.10B
164b.08.09B
164b.04.05B
164b.02.04B
164b.01.03B
215.04 STG BUS → ADR REG B
217.08 STEP ADR REG B

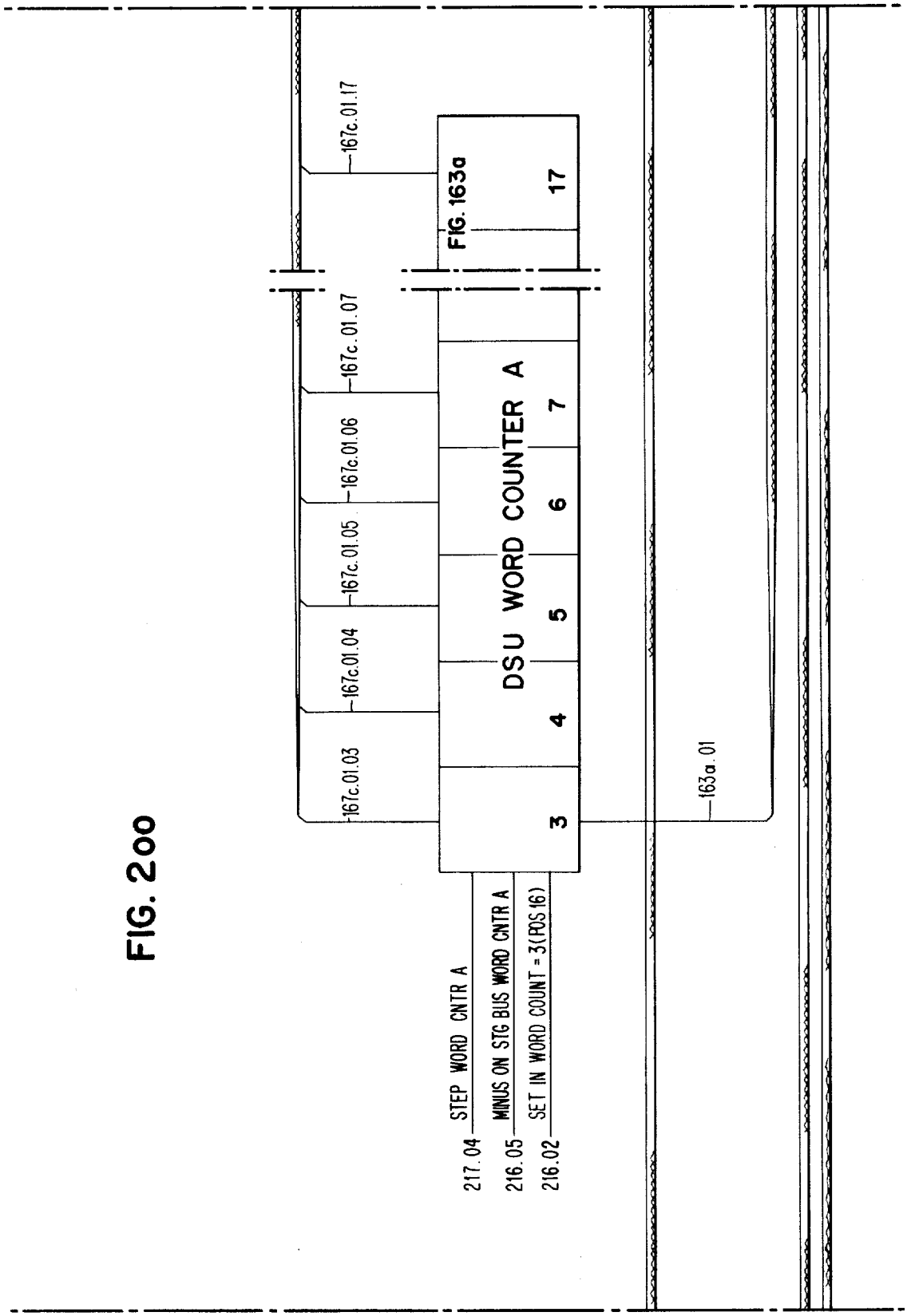

167c.01.17
FIG. 163a
17
167c.01.07
167c.01.06
167c.01.05
167c.01.04
167c.01.03
DSU WORD COUNTER A
7
6
5
4
3
163a.01
217.04 STEP WORD CNTR A
216.05 MINUS ON STG BUS WORD CNTR A
216.02 SET IN WORD COUNT = 3 (POS 16)

FIG. 200

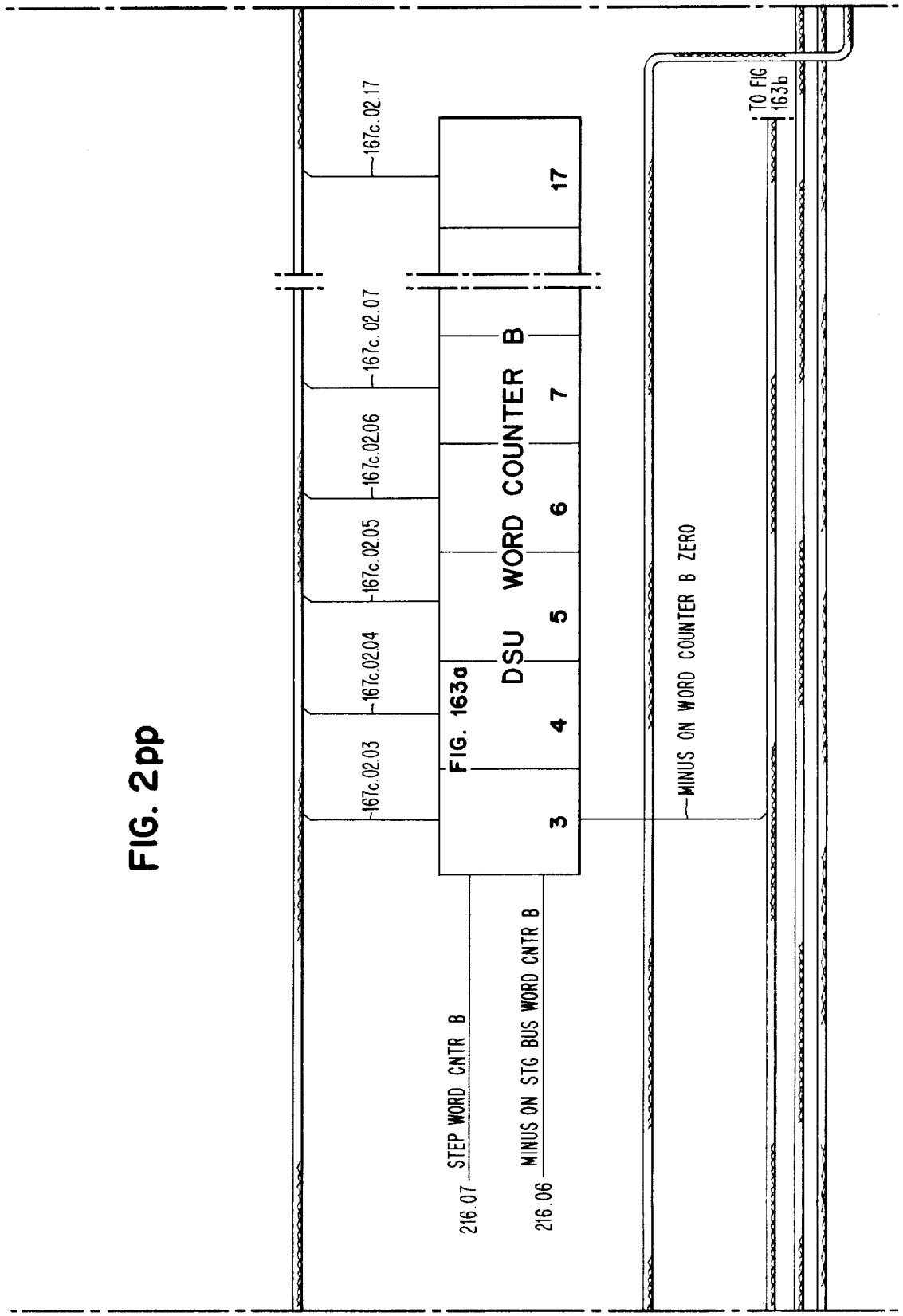

TO FIG 163b
167c.02.17
17
167c.02.07
7
167c.02.06
6
167c.02.05
5
167c.02.04
4
167c.02.03
3
DSU WORD COUNTER B
FIG. 163a
MINUS ON WORD COUNTER B ZERO
216.07 STEP WORD CNTR B
216.06 MINUS ON STG BUS WORD CNTR B

FIG. 2pp

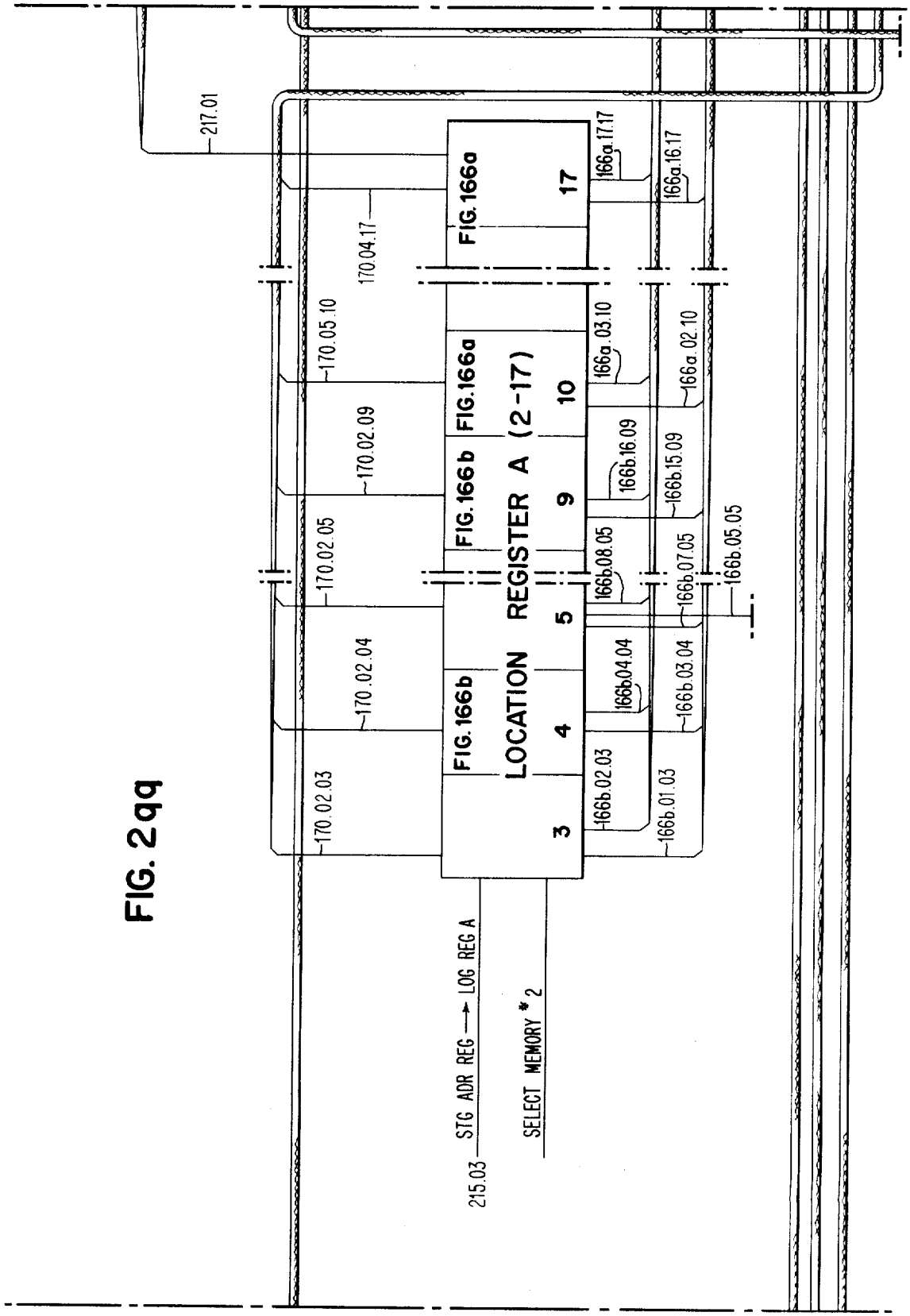

217.01
FIG. 166a
17
166a.17.17
166a.16.17
170.04.17
170.05.10
FIG. 166a
10
166a.03.10
166a.02.10
170.02.09
FIG. 166b
9
166b.16.09
166b.15.09
170.02.05
166b.08.05
166b.07.05
166b.05.05
LOCATION REGISTER A (2-17)
5
170.02.04
FIG. 166b
4
166b.04.04
166b.03.04
170.02.03
3
166b.02.03
166b.01.03
215.03
STG ADR REG → LOG REG A
SELECT MEMORY * 2

FIG. 2qq

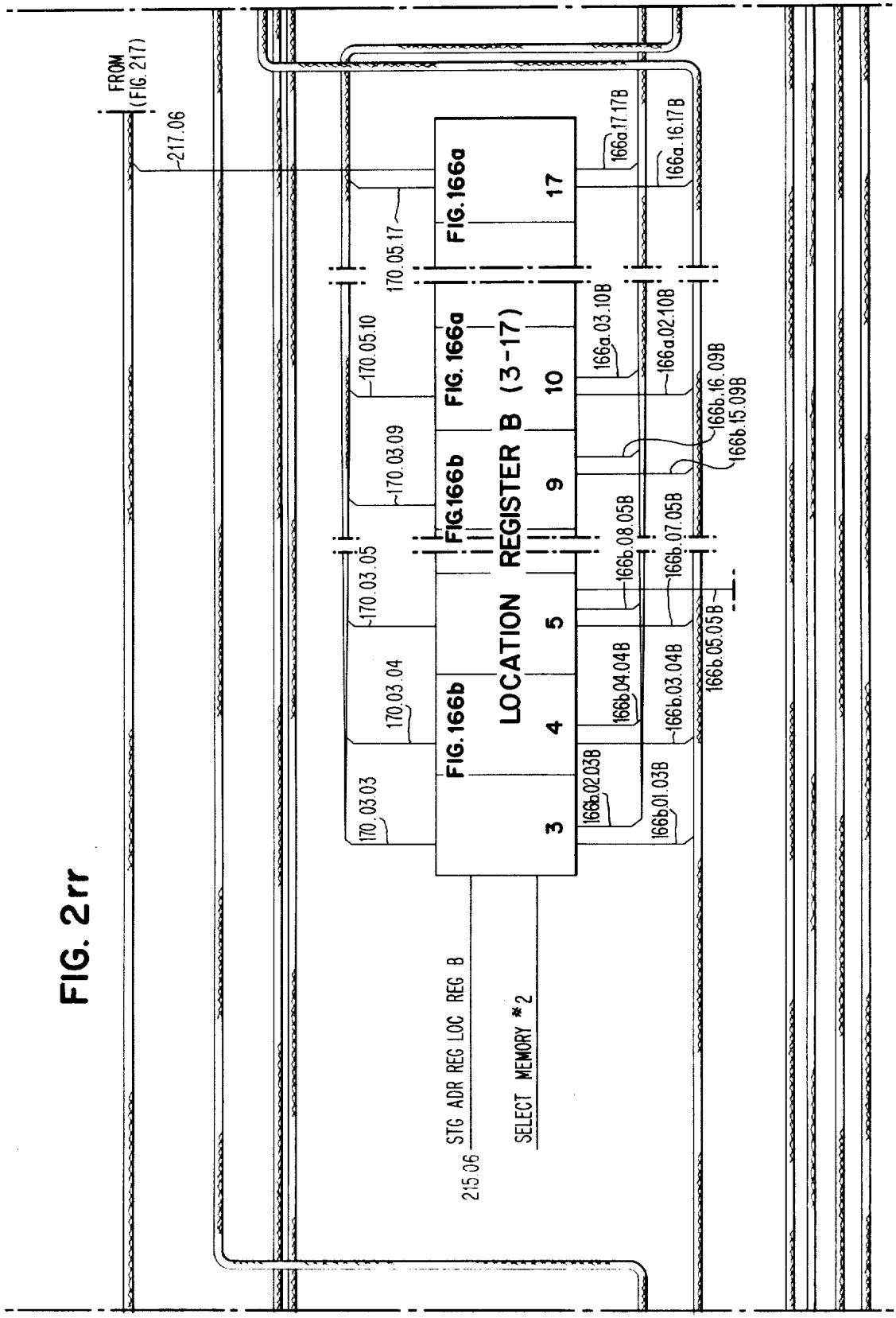

FROM (FIG. 217)
217.06
FIG. 166a
17
166a.17.17B
166a.16.17B
170.05.17
170.05.10
FIG. 166a
10
166a.03.10B
166a.02.10B
166b.16.09B
166b.15.09B
170.03.09
FIG.166b
9
166b.08.05B
166b.07.05B
LOCATION REGISTER B (3-17)
170.03.05
5
166b.05.05B
170.03.04
FIG. 166b
4
166b.04.04B
166b.03.04B
166b.02.03B
166b.01.03B
170.03.03
3
215.06 STG ADR REG LOC REG B
SELECT MEMORY *2

FIG. 2rr

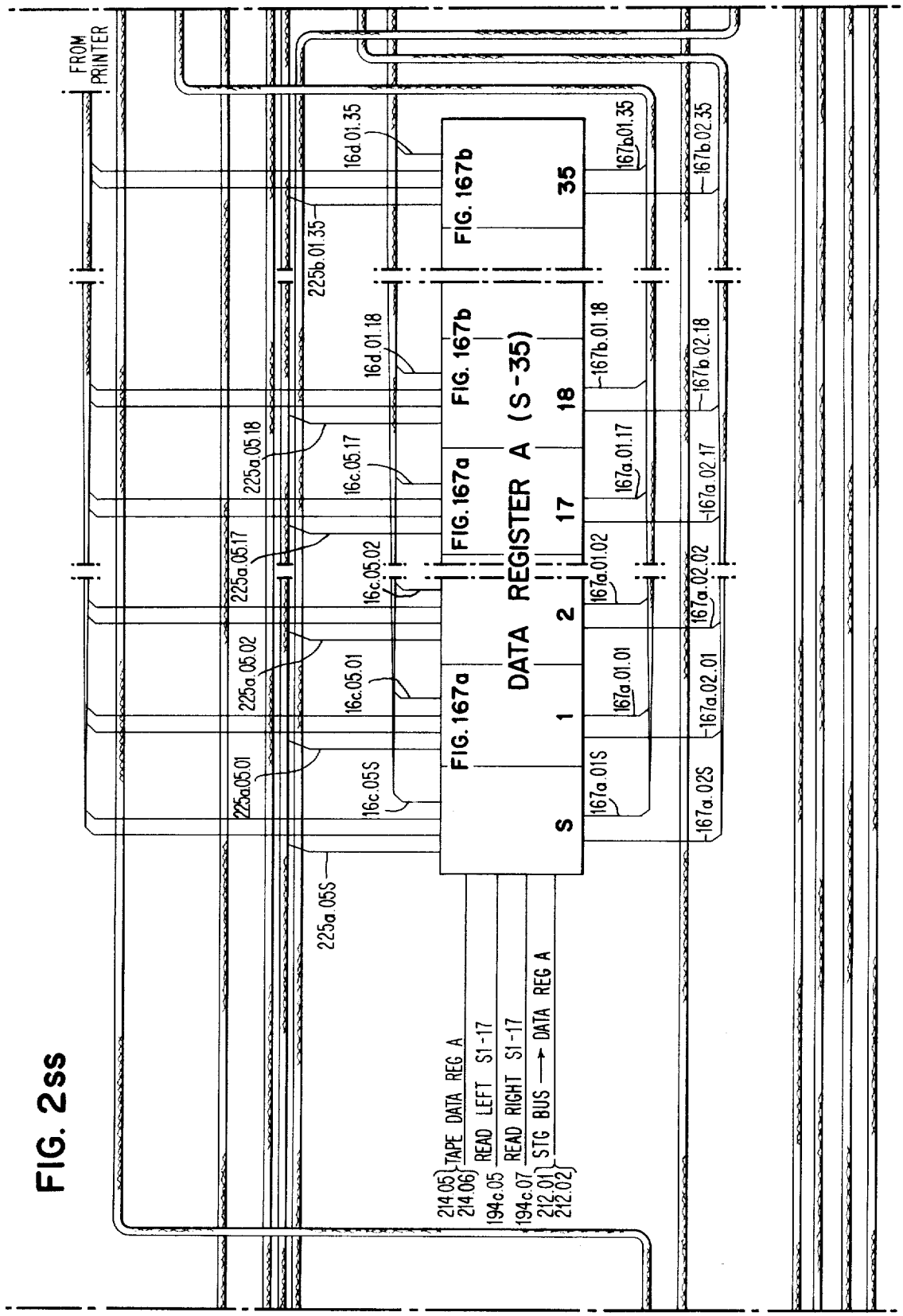
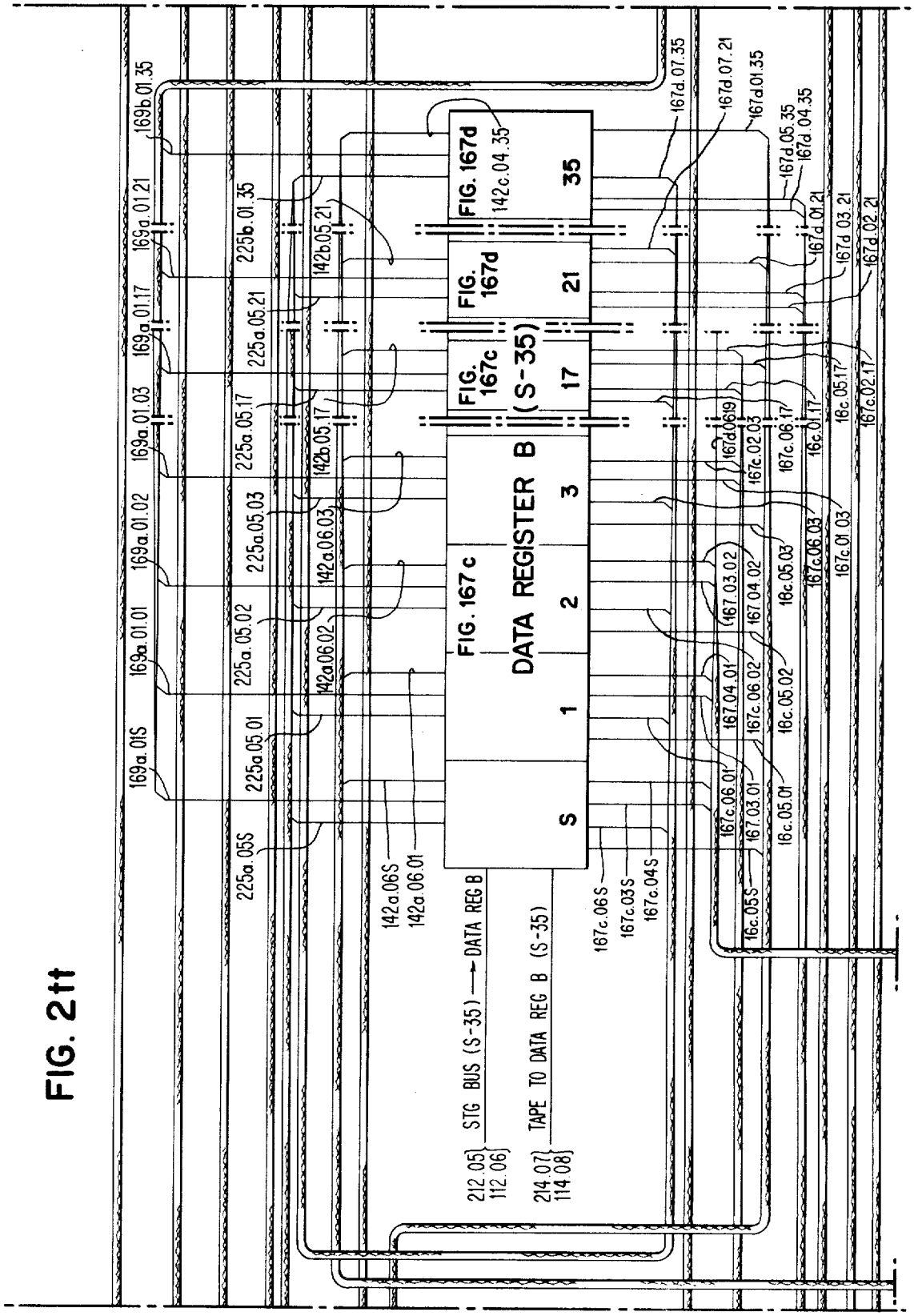

FROM PRINTER
FIG. 167b
35
18
FIG. 167a
17
DATA REGISTER A (S-35)
2
1
S
FIG. 167a
16d.01.35
225b.01.35
167b.01.35
167b.02.35
16d.01.18
167b.01.18
167b.02.18
225a.05.18
16c.05.17
167a.01.17
167a.02.17
225a.05.17
16c.05.02
167a.01.02
167a.02.02
225a.05.02
16c.05.01
167a.01.01
167a.02.01
225a.05.01
16c.05S
167a.01S
167a.02S
225a.05S
214.05 TAPE DATA REG A
214.06
194c.05 READ LEFT S1-17
194c.07 READ RIGHT S1-17
212.01 STG BUS → DATA REG A
212.02

FIG. 2ss

FIG. 21t


DATA REGISTER B
FIG. 167c
FIG. 167c (S-35)
FIG. 167d
FIG. 167d
S
1
2
3
17
21
35
STG BUS (S-35) → DATA REG B
TAPE TO DATA REG B (S-35)
212.05
112.06
214.07
114.08
169a.01S
169a.01.01
169a.01.02
169a.01.03
169a.01.17
169a.01.21
169b.01.35
225a.05S
225a.05.01
225a.05.02
225a.05.03
225a.05.17
225a.05.21
225b.01.35
142a.06S
142a.06.01
142a.06.02
142a.06.03
142b.05.17
142b.05.21
142c.04.35
167c.06S
167c.03S
167c.04S
167c.06.01
167.03.01
16c.05S
167.04.01
167c.06.02
167.03.02
167.04.02
16c.05.01
16c.05.02
16c.05.03
167c.06.03
167d.06.19
167c.02.03
167c.06.17
16c.01.17
16c.05.17
167c.02.17
167c.01.03
167d.07.35
167d.07.21
167d.01.35
167d.05.35
167d.04.35
167d.01.21
167d.03.21
167d.02.21

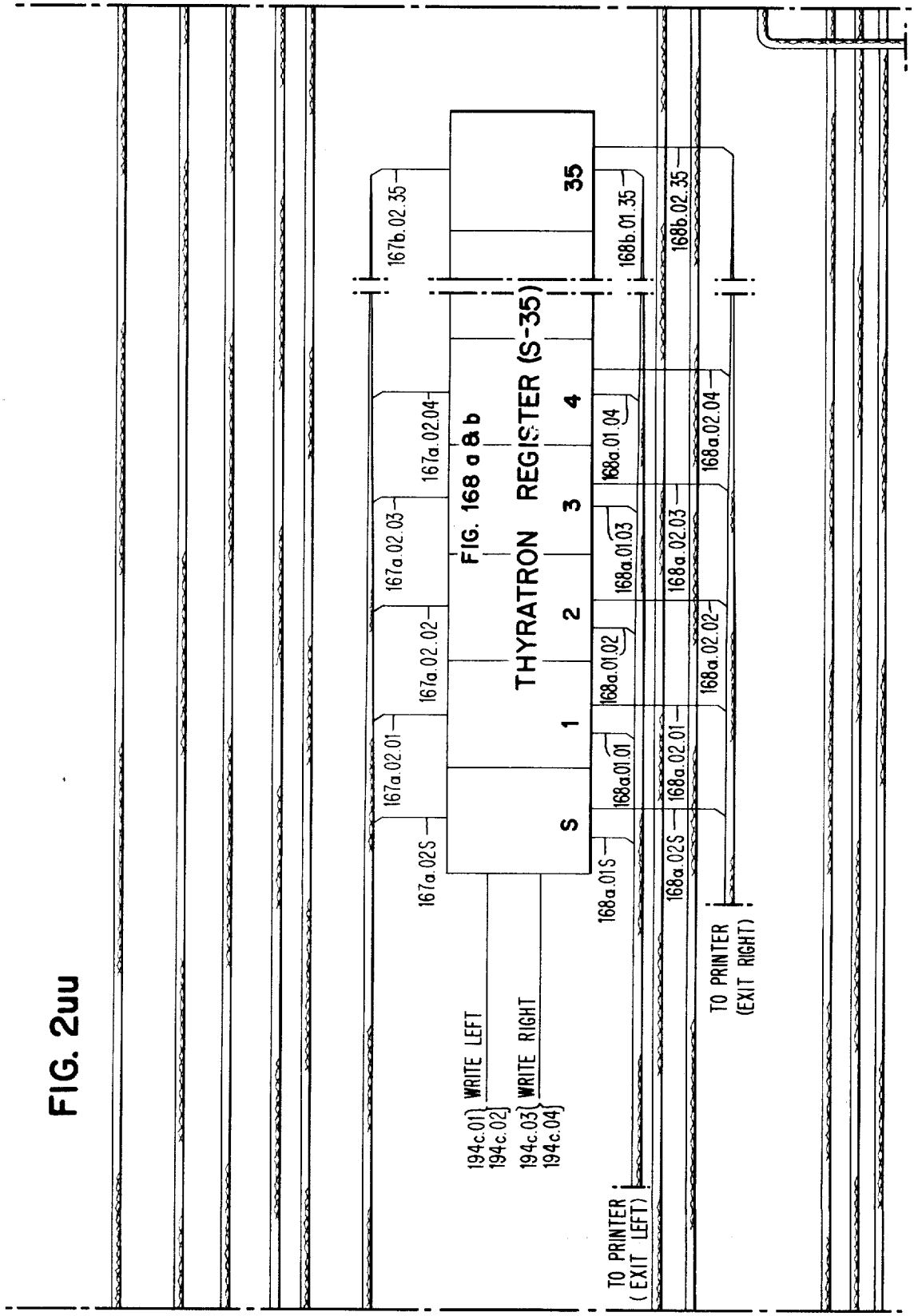
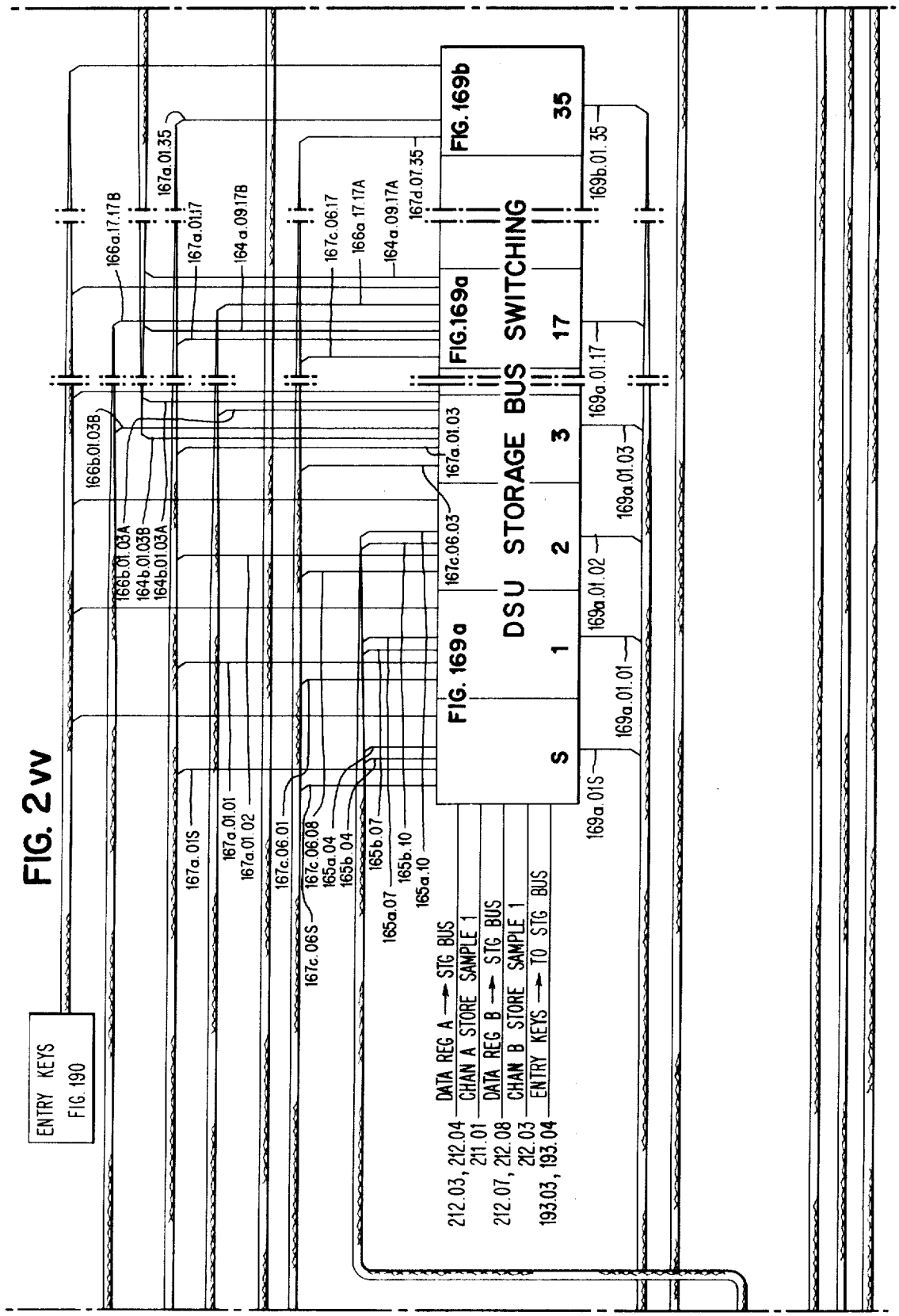

FIG. 168 a & b
THYRATRON REGISTER (S-35)
S
1
2
3
4
35
167a.02S
167a.02.01
167a.02.02
167a.02.03
167a.02.04
167b.02.35
168a.01S
168a.01.01
168a.01.02
168a.01.03
168a.01.04
168b.01.35
168a.02S
168a.02.01
168a.02.02
168a.02.03
168a.02.04
168b.02.35
194c.01 WRITE LEFT
194c.02
194c.03 WRITE RIGHT
194c.04
TO PRINTER (EXIT LEFT)
TO PRINTER (EXIT RIGHT)

FIG. 2uu


FIG. 2vv
ENTRY KEYS FIG. 190
FIG. 169a
DSU STORAGE BUS SWITCHING
S
1
2
3
FIG. 169a
17
FIG. 169b
35
166a.17.17B
167a.01.35
167a.01.17
164a.09.17B
167c.06.17
166a.17.17A
164a.09.17A
167d.07.35
166b.01.03B
166b.01.03A
164b.01.03B
164b.01.03A
167a.01S
167a.01.01
167a.01.02
167c.06.01
167c.06S
167c.06.08
165a.04
165b.04
165b.07
165a.07
165b.10
165a.10
167a.01.03
167c.06.03
169a.01.17
169a.01.03
169a.01.02
169a.01.01
169a.01S
169b.01.35
212.03, 212.04 DATA REG A → STG BUS
211.01 CHAN A STORE SAMPLE 1
212.07, 212.08 DATA REG B → STG BUS
212.03 CHAN B STORE SAMPLE 1
193.03, 193.04 ENTRY KEYS → TO STG BUS

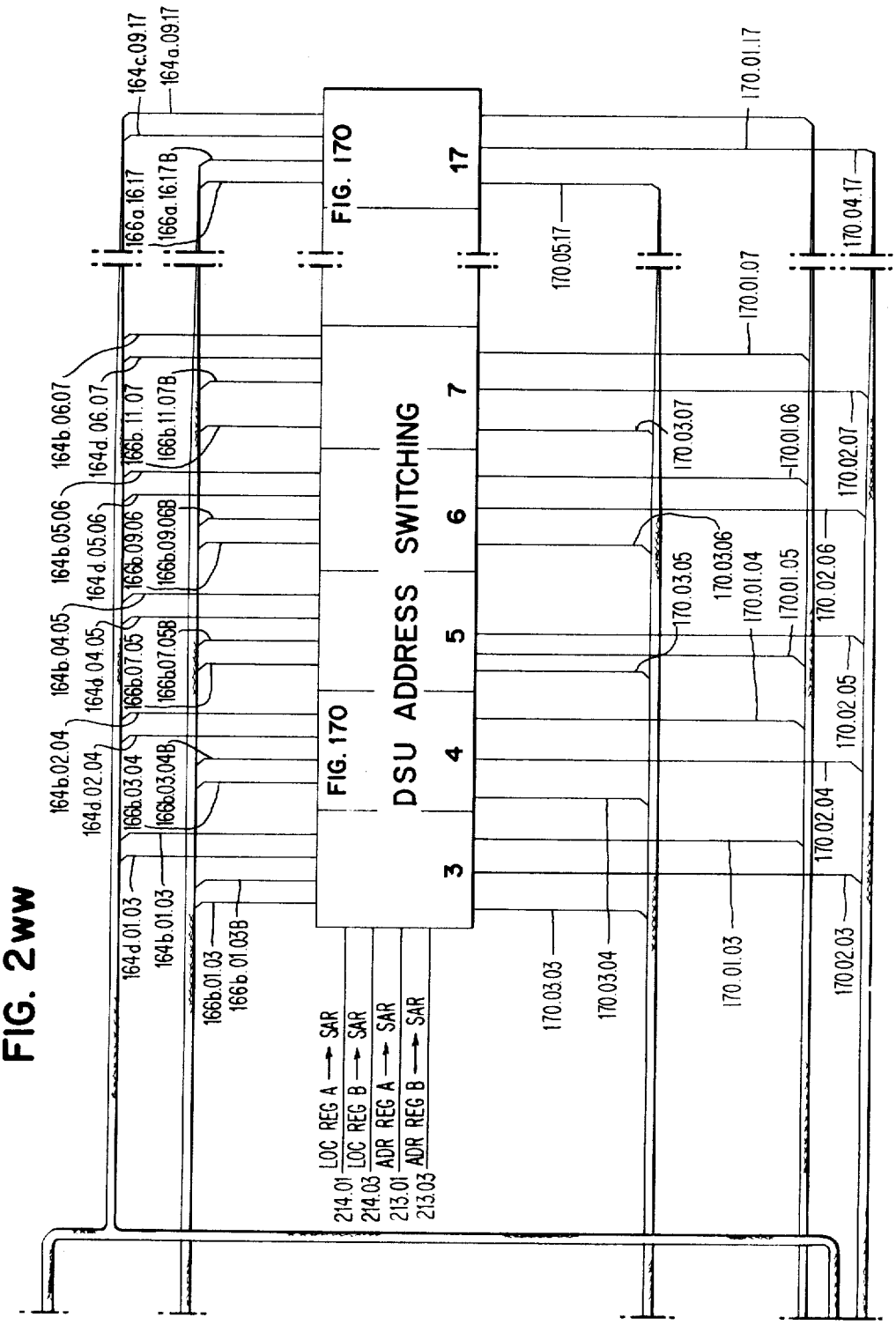

DSU ADDRESS SWITCHING
FIG. 170
FIG. 170
3
4
5
6
7
17
164c.09.17
164a.09.17
166a.16.17
166a.16.17B
164b.06.07
164d.06.07
166b.11.07
166b.11.07B
164b.05.06
164d.05.06
166b.09.06
166b.09.06B
164b.04.05
164d.04.05
166b.07.05
166b.07.05B
164b.02.04
164d.02.04
166b.03.04
166b.03.04B
164d.01.03
164b.01.03
166b.01.03
166b.01.03B
214.01 LOC REG A → SAR
214.03 LOC REG B → SAR
213.01 ADR REG A → SAR
213.03 ADR REG B → SAR
170.01.17
170.05.17
170.01.07
170.04.17
170.03.07
170.01.06
170.02.07
170.03.05
170.03.06
170.01.04
170.01.05
170.02.06
170.02.05
170.02.04
170.03.03
170.03.04
170.01.03
170.02.03

FIG. 2ww

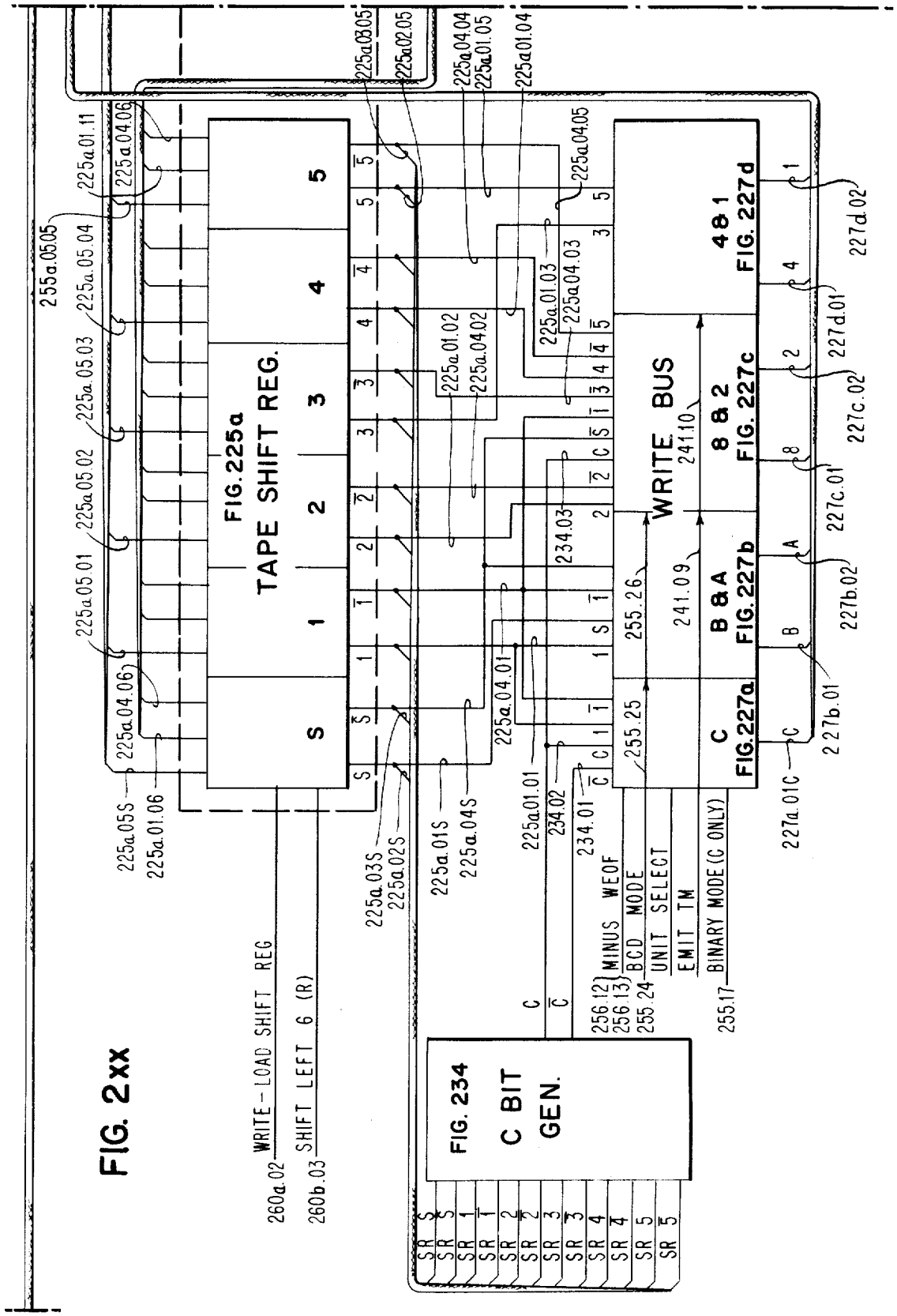

FIG. 225a
TAPE SHIFT REG.
FIG. 234
C BIT GEN.
WRITE BUS
241.10
241.09
FIG. 227a
FIG. 227b
FIG. 227c
FIG. 227d
WRITE-LOAD SHIFT REG
SHIFT LEFT 6 (R)
MINUS WEOF
BCD MODE
UNIT SELECT
EMIT TM
BINARY MODE (C ONLY)

FIG. 2xx

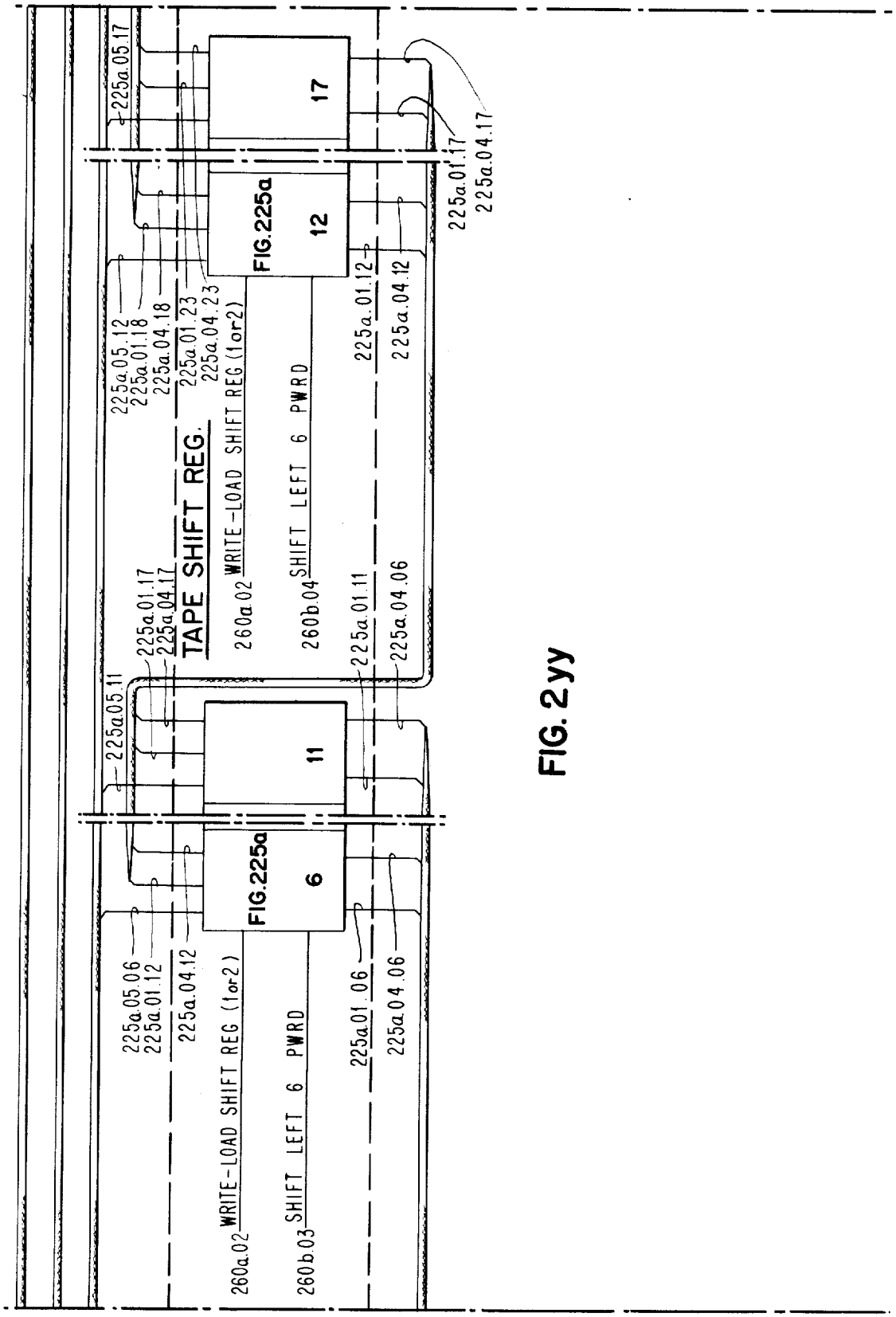

TAPE SHIFT REG.
FIG.225a
17
12
11
6
225a.05.17
225a.05.12
225a.01.18
225a.04.18
225a.01.23
225a.04.23
225a.01.17
225a.04.17
225a.05.11
225a.01.17
225a.04.17
225a.01.12
225a.04.12
225a.01.11
225a.04.06
260a.02 WRITE-LOAD SHIFT REG (1or2)
260b.04 SHIFT LEFT 6 PWRD
225a.05.06
225a.01.12
225a.04.12
225a.01.06
225a.04.06
260a.02 WRITE-LOAD SHIFT REG (1or2)
260b.03 SHIFT LEFT 6 PWRD

FIG. 2yy

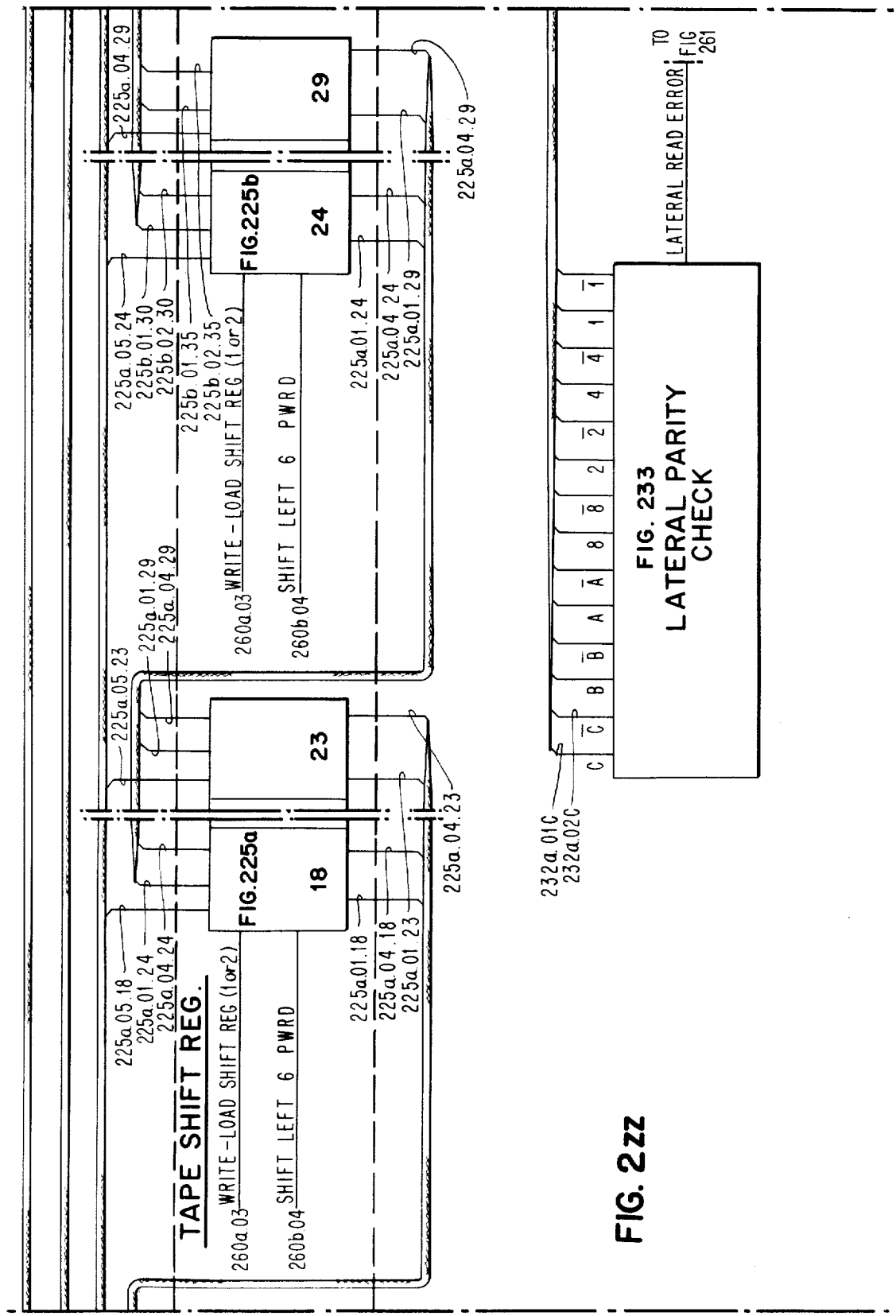

TAPE SHIFT REG.
WRITE-LOAD SHIFT REG (1 or 2)
260a 03
SHIFT LEFT 6 PWRD
260b 04
225a.05.18
225a.01.24
225a.04.24
225a.05.23
225a.01.29
225a.04.29
225a.01.18
225a.04.18
225a.01.23
225a.04.23
FIG.225a
18
23
WRITE-LOAD SHIFT REG (1 or 2)
260a 03
SHIFT LEFT 6 PWRD
260b 04
225a.05.24
225b.01.30
225b.02.30
225b 01.35
225b 02.35
225a.01.24
225a.04 24
225a.01.29
225a.04.29
FIG.225b
24
29
LATERAL READ ERROR
TO FIG 261
FIG. 233
LATERAL PARITY CHECK
C C̄ B B̄ A Ā 8 8̄ 2 2̄ 4 4̄ 1 1̄
232a.01C
232a.02C

FIG. 2zz

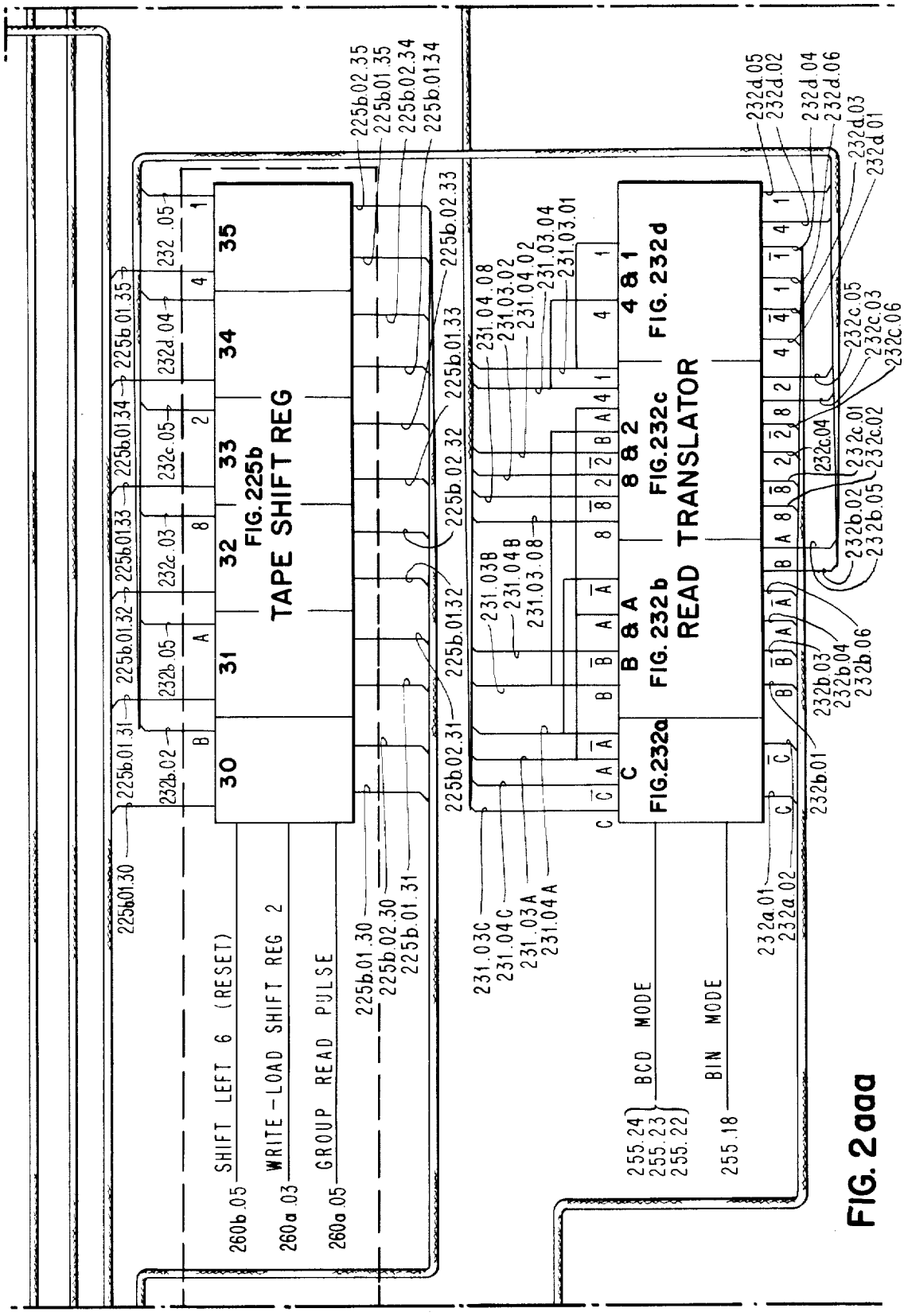

FIG. 225b
TAPE SHIFT REG
FIG. 232a
B & A
FIG. 232b
8 & 2
FIG. 232c
4 & 1
FIG. 232d
READ TRANSLATOR
SHIFT LEFT 6 (RESET)
WRITE-LOAD SHIFT REG 2
GROUP READ PULSE
BCD MODE
BIN MODE

FIG. 2aa

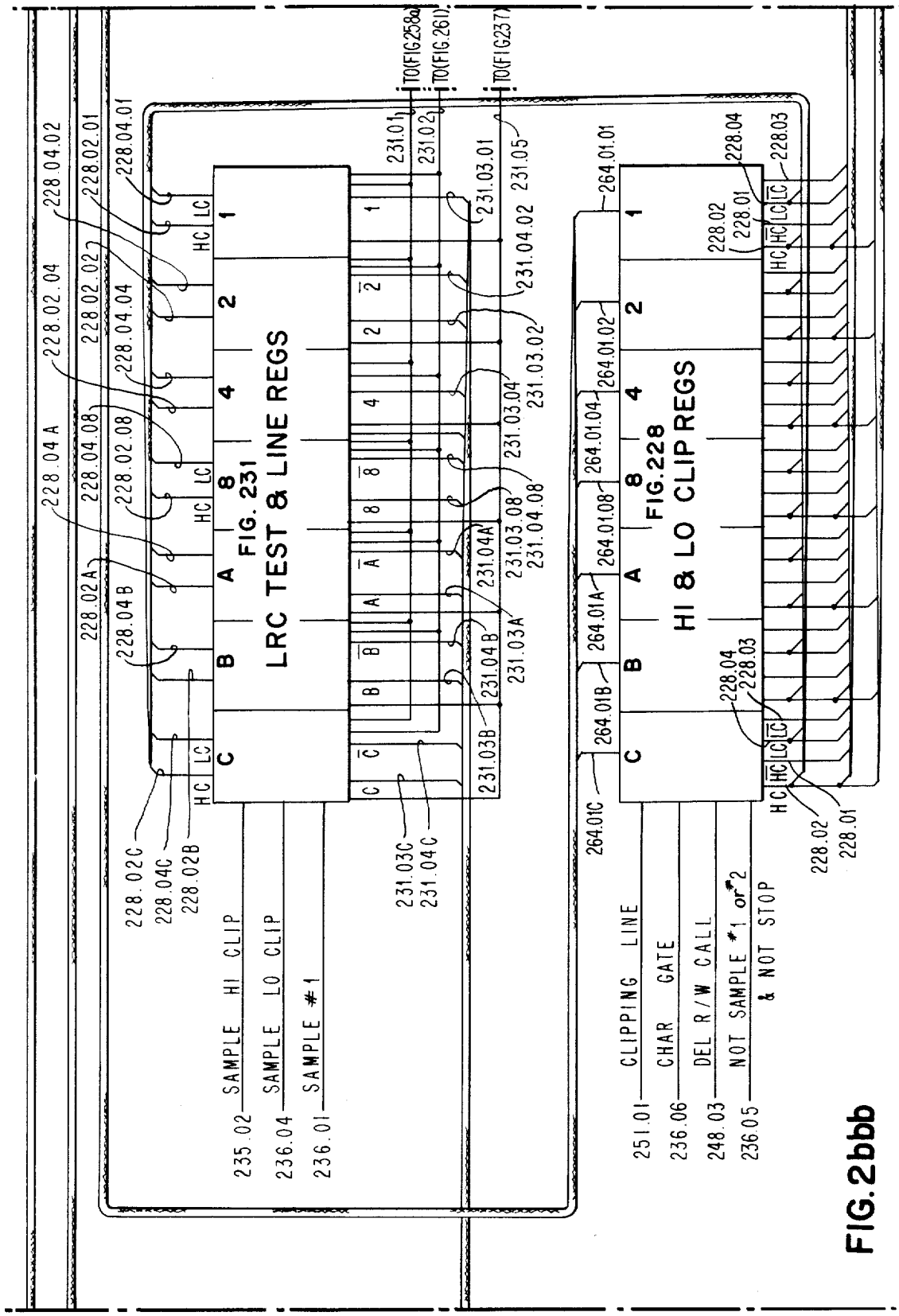

FIG. 231
LRC TEST & LINE REGS
FIG. 228
HI & LO CLIP REGS
SAMPLE HI CLIP
SAMPLE LO CLIP
SAMPLE #1
CLIPPING LINE
CHAR GATE
DEL R/W CALL
NOT SAMPLE #1 or #2 & NOT STOP
TO(FIG.258)
TO(FIG.261)
TO(FIG.237)

FIG.2bb

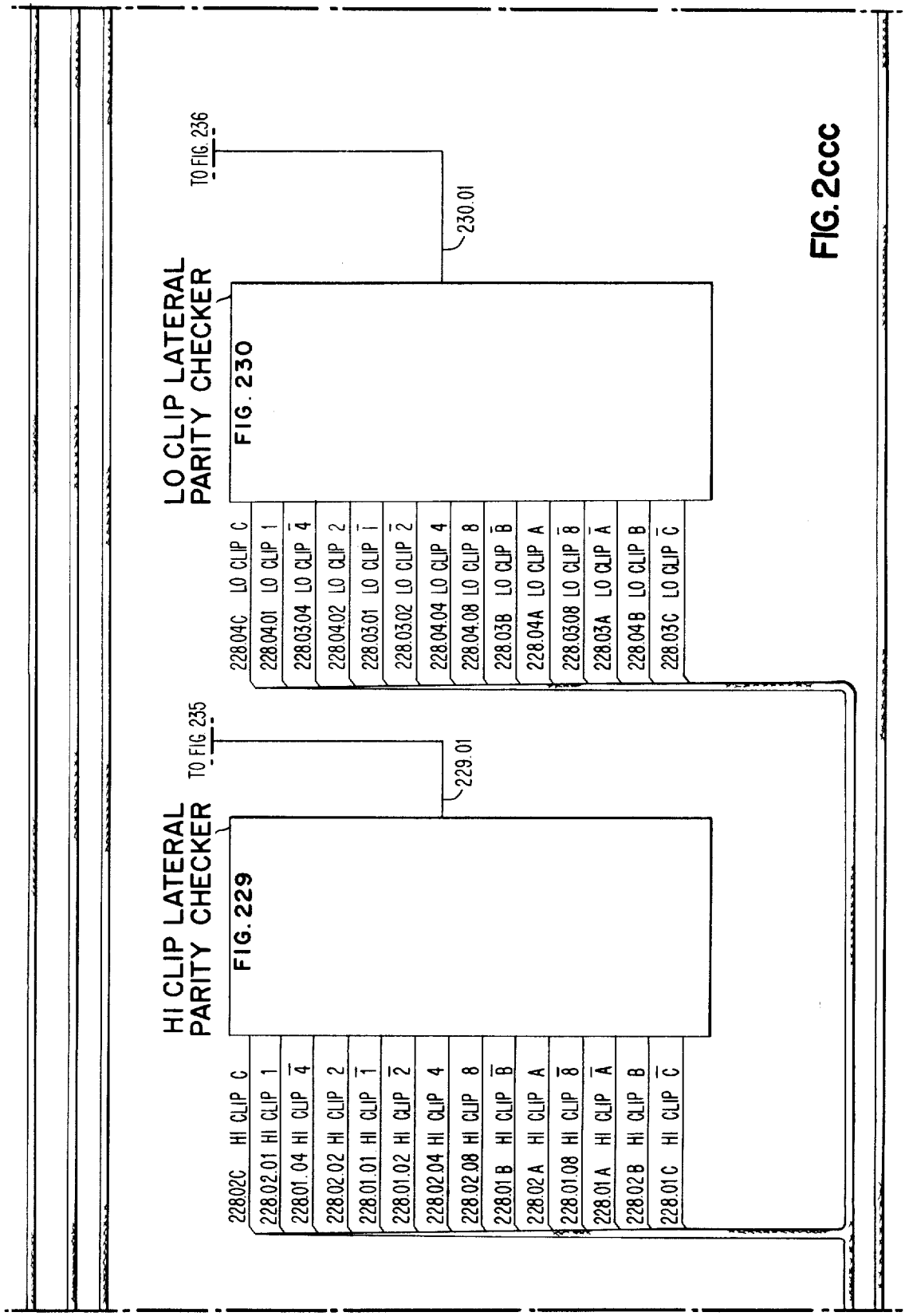
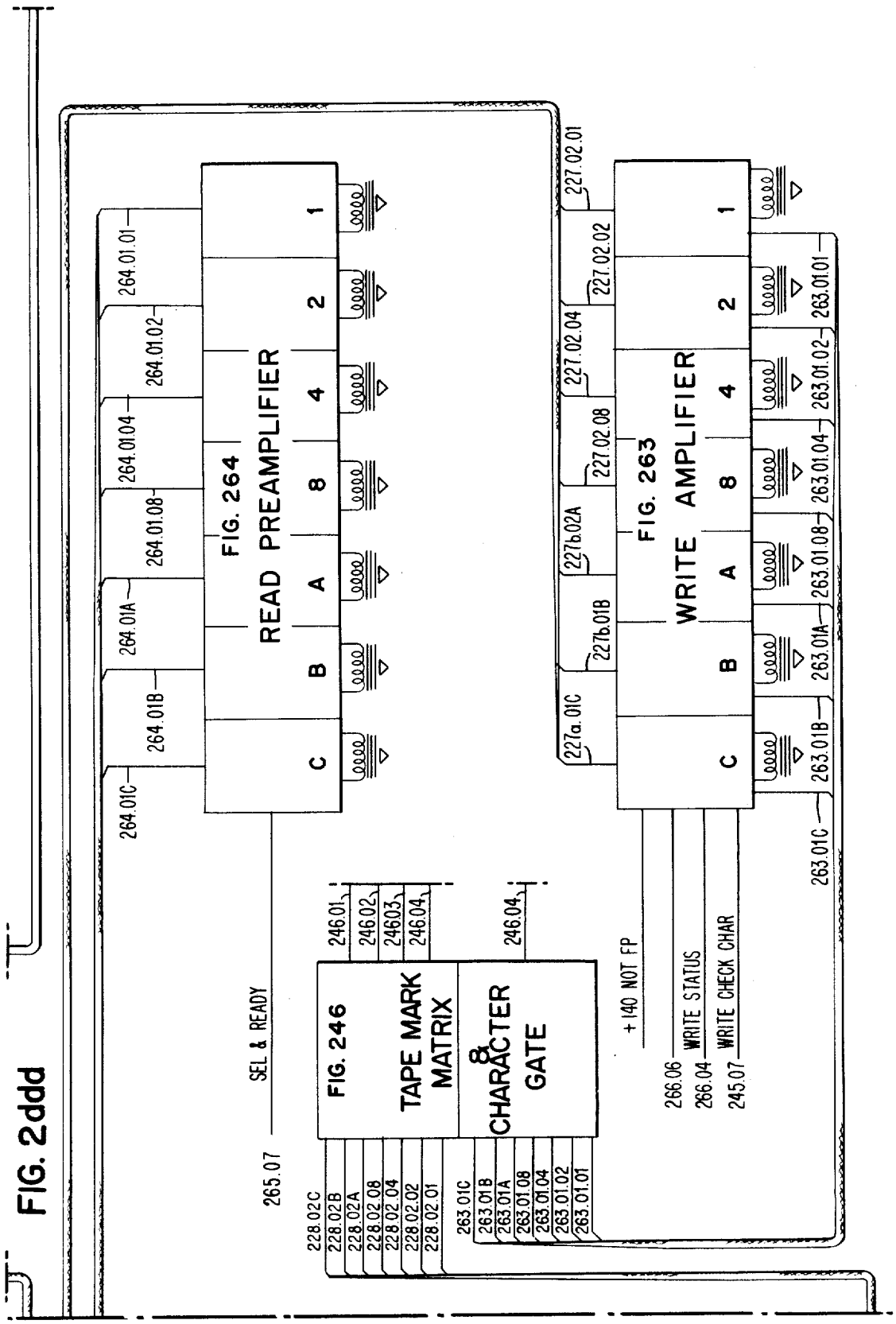

HI CLIP LATERAL PARITY CHECKER
FIG. 229
TO FIG. 235
229.01
228.02C HI CLIP C
228.02.01 HI CLIP 1
228.01.04 HI CLIP $\overline{4}$
228.02.02 HI CLIP 2
228.01.01 HI CLIP $\overline{1}$
228.01.02 HI CLIP $\overline{2}$
228.02.04 HI CLIP 4
228.02.08 HI CLIP 8
228.01B HI CLIP $\overline{B}$
228.02A HI CLIP A
228.01.08 HI CLIP $\overline{8}$
228.01A HI CLIP $\overline{A}$
228.02B HI CLIP B
228.01C HI CLIP $\overline{C}$
LO CLIP LATERAL PARITY CHECKER
FIG. 230
TO FIG. 236
230.01
228.04C LO CLIP C
228.04.01 LO CLIP 1
228.03.04 LO CLIP $\overline{4}$
228.04.02 LO CLIP 2
228.03.01 LO CLIP $\overline{1}$
228.03.02 LO CLIP $\overline{2}$
228.04.04 LO CLIP 4
228.04.08 LO CLIP 8
228.03B LO CLIP $\overline{B}$
228.04A LO CLIP A
228.03.08 LO CLIP $\overline{8}$
228.03A LO CLIP $\overline{A}$
228.04B LO CLIP B
228.03C LO CLIP $\overline{C}$

FIG. 2ccc


FIG. 2dd
FIG. 264
READ PREAMPLIFIER
C
B
A
8
4
2
1
264.01C
264.01B
264.01A
264.01.08
264.01.04
264.01.02
264.01.01
FIG. 263
WRITE AMPLIFIER
227a.01C
227b.01B
227b.02A
227.02.08
227.02.04
227.02.02
227.02.01
263.01C
263.01B
263.01A
263.01.08
263.01.04
263.01.02
263.01.01
FIG. 246
TAPE MARK MATRIX
& CHARACTER GATE
246.01
246.02
246.03
246.04
246.04
SEL & READY
265.07
+140 NOT FP
WRITE STATUS
266.06
266.04
WRITE CHECK CHAR
245.07
228.02C
228.02B
228.02A
228.02.08
228.02.04
228.02.02
228.02.01
263.01C
263.01B
263.01A
263.01.08
263.01.04
263.01.02
263.01.01

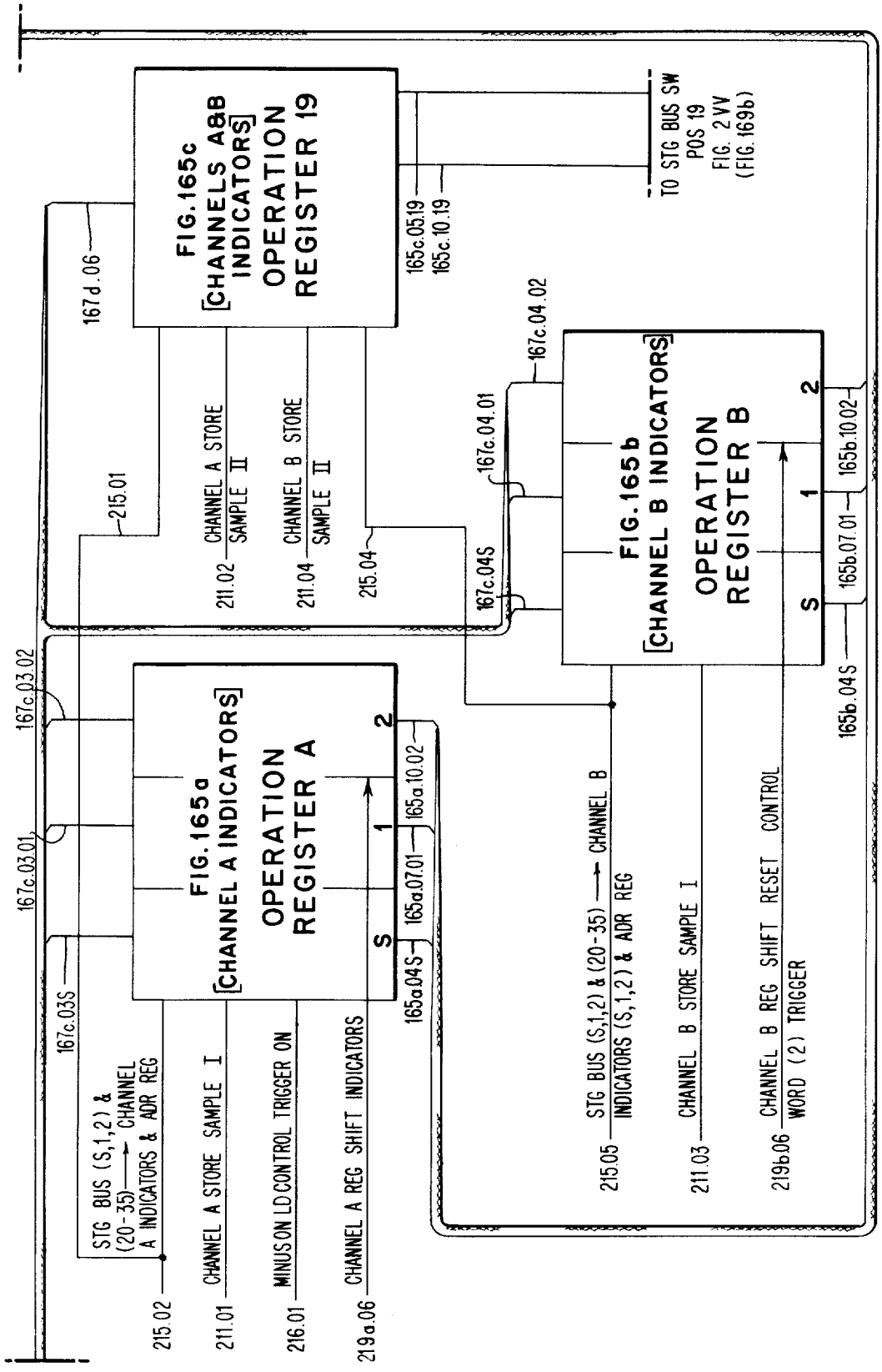
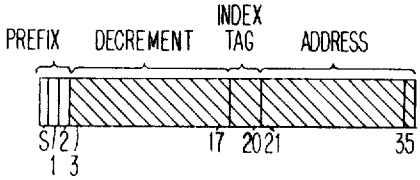

FIG. 165c
[CHANNELS A&B INDICATORS]
OPERATION REGISTER 19
FIG. 165a
[CHANNEL A INDICATORS]
OPERATION REGISTER A
FIG. 165b
[CHANNEL B INDICATORS]
OPERATION REGISTER B
TO STG BUS SW POS 19 FIG. 2VV (FIG. 169b)
STG BUS (S,1,2) & (20-35) → CHANNEL A INDICATORS & ADR REG
CHANNEL A STORE SAMPLE I
MINUS ON LD CONTROL TRIGGER ON
CHANNEL A REG SHIFT INDICATORS
CHANNEL A STORE SAMPLE II
CHANNEL B STORE SAMPLE II
STG BUS (S,1,2) & (20-35) → CHANNEL B INDICATORS (S,1,2) & ADR REG
CHANNEL B STORE SAMPLE I
CHANNEL B REG SHIFT RESET CONTROL WORD (2) TRIGGER
215.02
211.01
216.01
219a.06
211.02
211.04
215.04
215.01
215.05
211.03
219b.06
167c.03.01
167c.03.02
167c.03S
167d.06
165c.05.19
165c.10.19
167c.04.02
167c.04.01
167c.04S
165a.04S
165a.07.01
165a.10.02
165b.04S
165b.07.01
165b.10.02

FIG. 2eee

FIG. 2fff

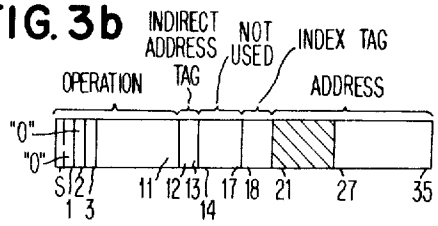
FIG.2a	FIG.2b	FIG.2c	FIG.2d	FIG.2e	FIG.2f	FIG.2g												
FIG.2h	FIG.2i	FIG.2j	FIG.2k	FIG.2l	FIG.2m	FIG.2n	FIG.2o	FIG.2p	FIG.2q	FIG.2r	FIG.2s	FIG.2t	FIG.2u					
FIG.2v	FIG.2w	FIG.2x	FIG.2y	FIG.2z	FIG.2aa	FIG.2bb	FIG.2cc	FIG.2dd	FIG.2ee	FIG.2ff	FIG.2gg							
FIG.2hh	FIG.2ii	FIG.2mm	FIG.2nn	FIG.2oo	FIG.2pp	FIG.2qq	FIG.2rr	FIG.2ss	FIG.2tt	FIG.2uu	FIG.2vv	FIG.2ww						
FIG.2jj	FIG.2kk	FIG.2ll	FIG.2xx	FIG.2yy	FIG.2zz	FIG.2aaa	FIG2bbb	FIG.2ccc	FIG.2ddd	FIG.2eee								

FIG. 3a



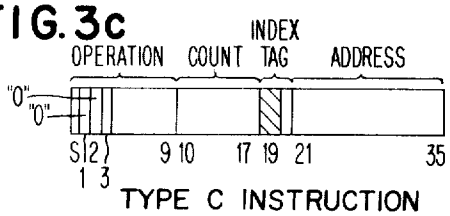
TYPE A INSTRUCTION

FIG. 3b



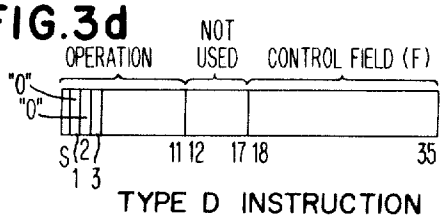
TYPE B INSTRUCTION

FIG. 3c



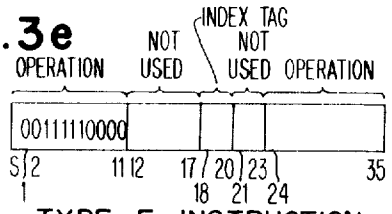
TYPE C INSTRUCTION

FIG. 3d



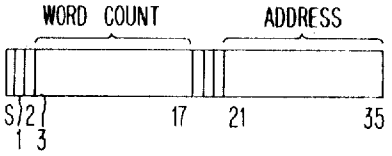
TYPE D INSTRUCTION

FIG. 3e



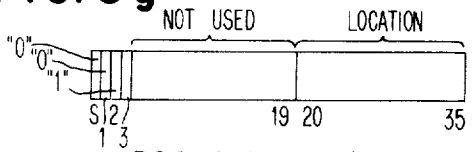
TYPE E INSTRUCTION

FIG. 3f



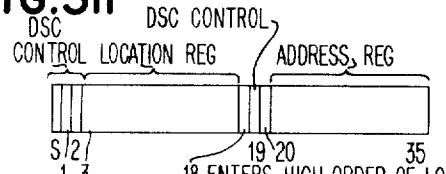
DSC CONTROL (NORMAL)

FIG. 3g



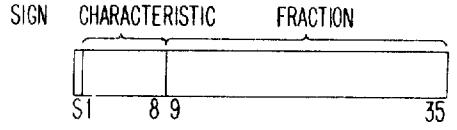
DSC CONTROL (SPECIAL)

FIG. 3h



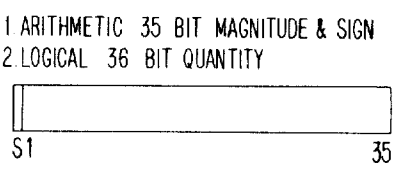
EXECUTION OF STORE DSC

FIG. 3i



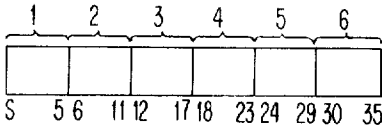
FLOATING POINT NUMBER

FIG. 3j



FIXED POINT WORD

FIG. 3k



BCD 6 - CHARACTER WORD

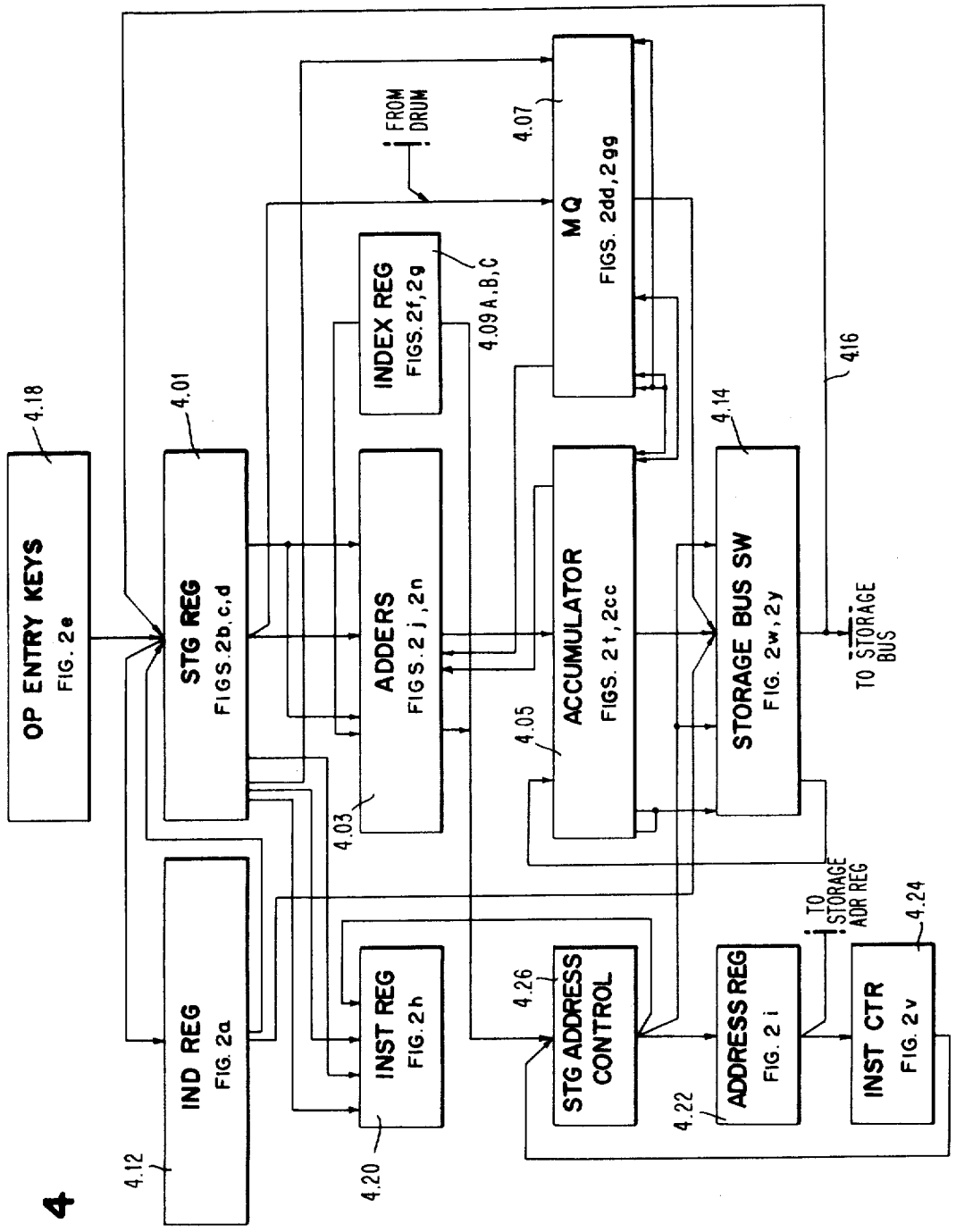

OP ENTRY KEYS
FIG. 2e
4.18
STG REG
FIGS. 2b, c, d
4.01
ADDERS
FIGS. 2j, 2n
4.03
INDEX REG
FIGS. 2f, 2g
4.09 A, B, C
FROM DRUM
MQ
FIGS. 2dd, 2gg
4.07
ACCUMULATOR
FIGS. 2t, 2cc
4.05
STORAGE BUS SW
FIG. 2w, 2y
4.14
416
TO STORAGE BUS
IND REG
FIG. 2a
4.12
INST REG
FIG. 2h
4.20
STG ADDRESS CONTROL
4.26
ADDRESS REG
FIG. 2i
4.22
TO STORAGE ADR REG
INST CTR
FIG. 2v
4.24

FIG. 4

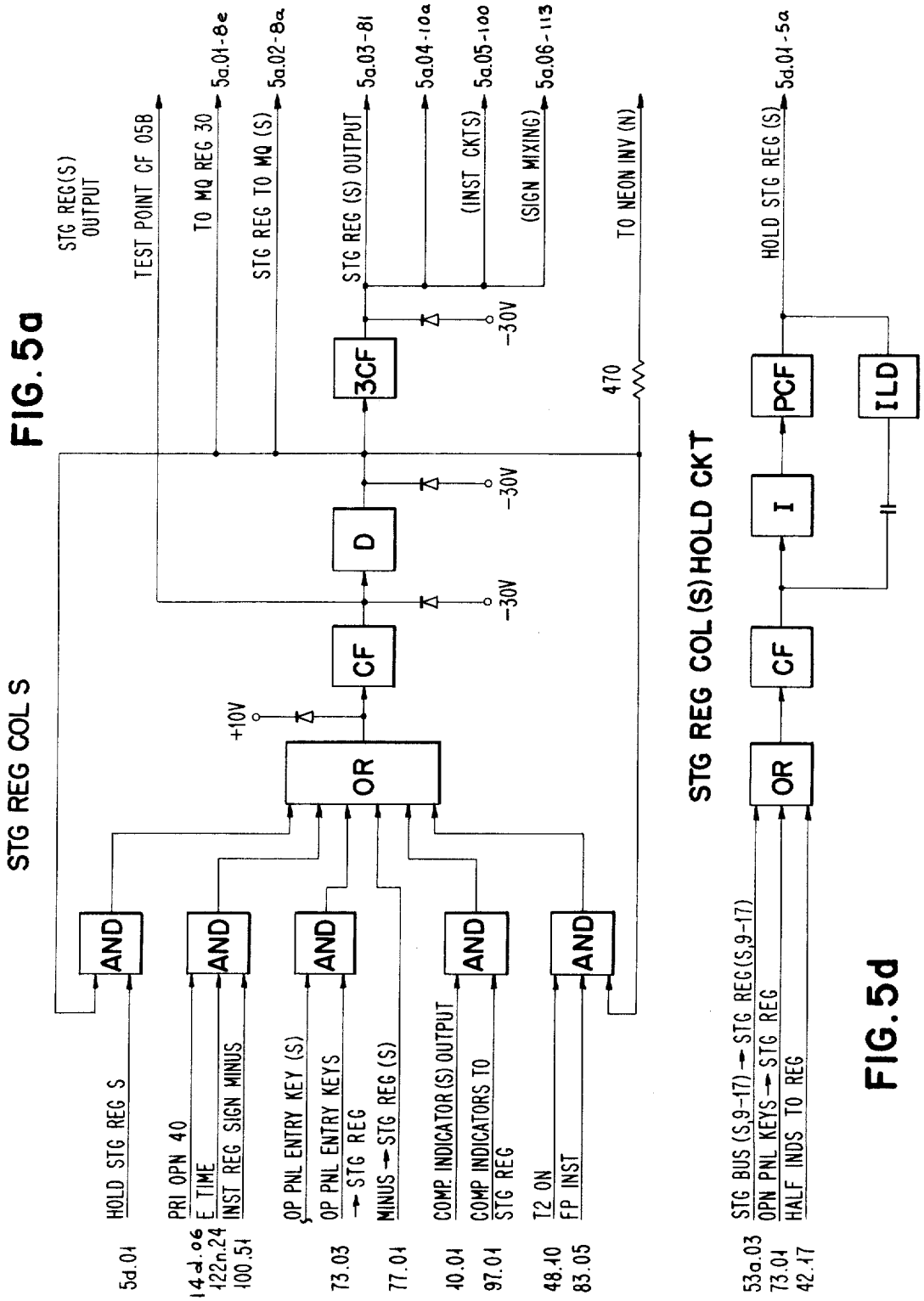
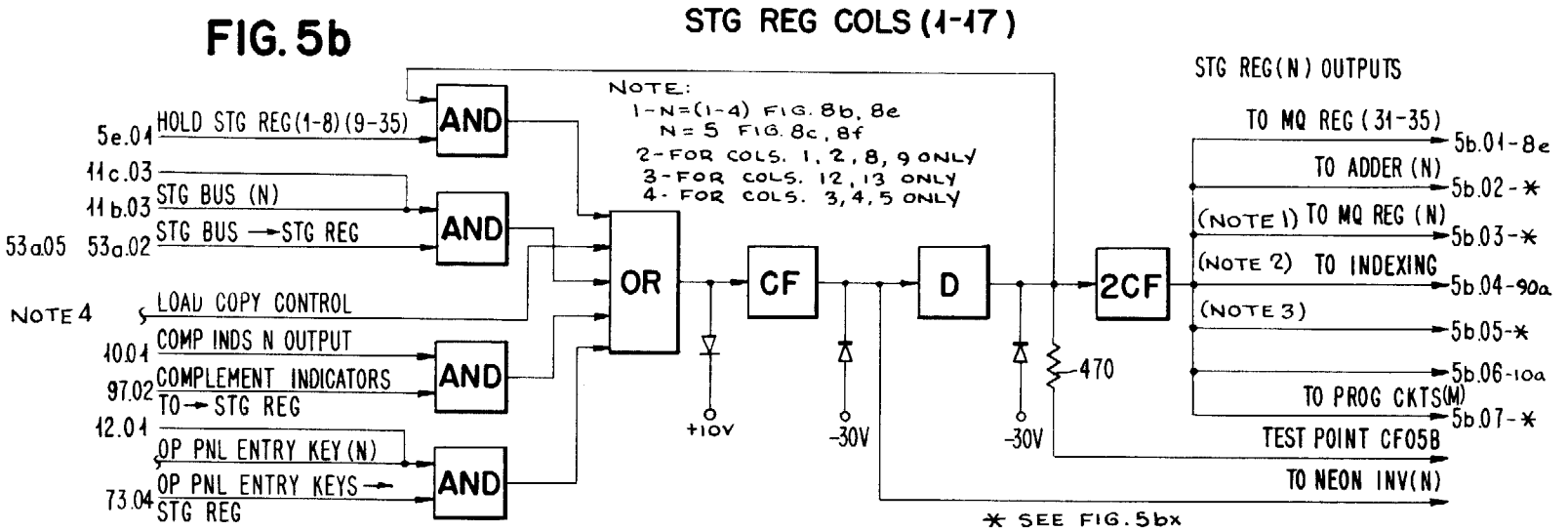

STG REG COL S
STG REG(S) OUTPUT
TEST POINT OF 05B
TO MQ REG 30
5a.01-8e
STG REG TO MQ (S)
5a.02-8a
STG REG (S) OUTPUT
5a.03-81
5a.04-10a
(INST CKTS)
5a.05-100
(SIGN MIXING)
5a.06-113
TO NEON INV (N)
470
-30V
-30V
-30V
+10V
3CF
D
CF
OR
AND
AND
AND
AND
AND
5d.04 HOLD STG REG S
14d.06 PRI OPN 40
122n.24 E TIME
100.51 INST REG SIGN MINUS
OP PNL ENTRY KEY (S)
73.03 OP PNL ENTRY KEYS → STG REG
77.04 MINUS → STG REG (S)
40.04 COMP. INDICATOR (S) OUTPUT
97.04 COMP INDICATORS TO STG REG
48.10 T2 ON
83.05 FP INST

FIG. 5a

STG REG COL (S) HOLD CKT
HOLD STG REG (S)
5d.01-5a
PCF
I
ILD
CF
OR
53a.03 STG BUS (S,9-17) → STG REG(S,9-17)
73.04 OPN PNL KEYS → STG REG
42.17 HALF INDS TO REG

FIG. 5d

FIG. 5b


STG REG COLS (1-17)
NOTE:
1-N=(1-4) FIG. 8b, 8e
N=5 FIG. 8c, 8f
2-FOR COLS. 1, 2, 8, 9 ONLY
3-FOR COLS. 12, 13 ONLY
4-FOR COLS. 3, 4, 5 ONLY
STG REG(N) OUTPUTS
5e.01 HOLD STG REG(1-8)(9-35)
11c.03
11b.03 STG BUS (N)
53a.05 53a.02 STG BUS → STG REG
NOTE 4 LOAD COPY CONTROL
10.01 COMP INDS N OUTPUT
97.02 COMPLEMENT INDICATORS TO → STG REG
12.01 OP PNL ENTRY KEY (N)
73.04 OP PNL ENTRY KEYS → STG REG
AND
AND
AND
OR
CF
D
2CF
+10V
-30V
-30V
470
TO MQ REG (31-35) 5b.01-8e
TO ADDER (N) 5b.02-*
(NOTE 1) TO MQ REG (N) 5b.03-*
(NOTE 2) TO INDEXING 5b.04-90a
(NOTE 3) 5b.05-*
5b.06-10a
TO PROG CKTS(M) 5b.07-*
TEST POINT CF05B
TO NEON INV(N)
* SEE FIG. 5bx

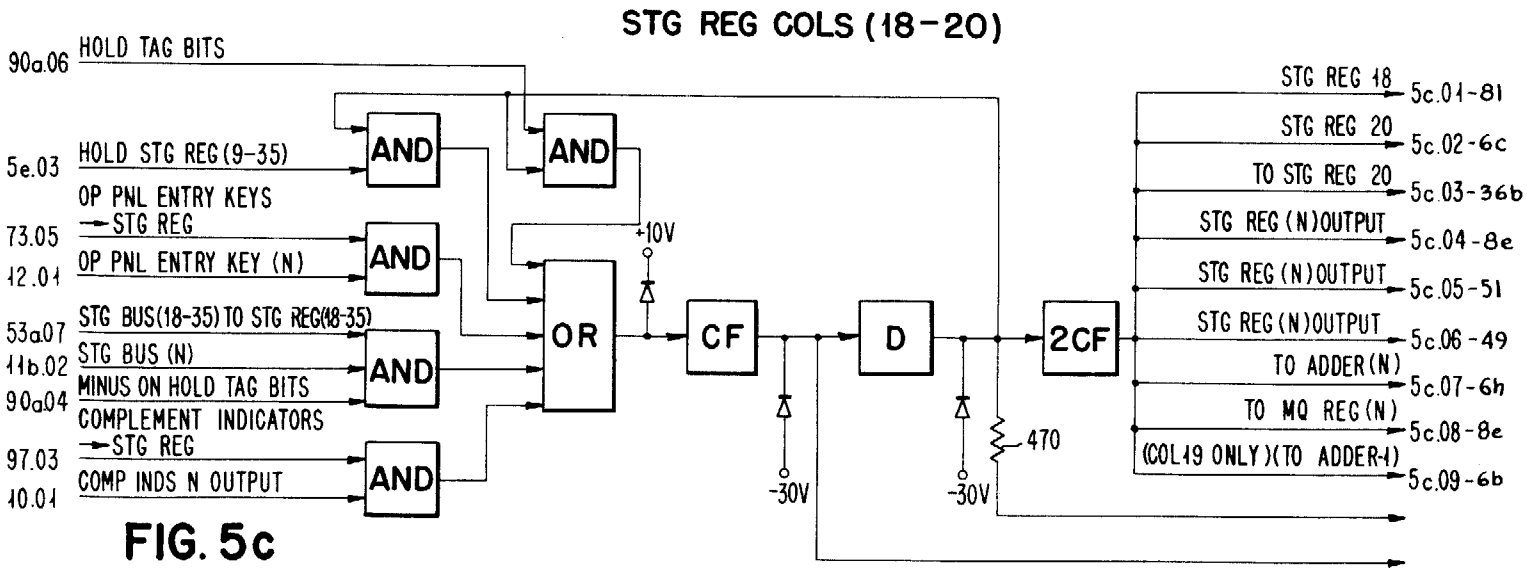

STG REG COLS (18-20)
90a.06 HOLD TAG BITS
5e.03 HOLD STG REG (9-35)
73.05 OP PNL ENTRY KEYS → STG REG
12.01 OP PNL ENTRY KEY (N)
53a.07 STG BUS(18-35) TO STG REG(18-35)
11b.02 STG BUS (N)
90a.04 MINUS ON HOLD TAG BITS
97.03 COMPLEMENT INDICATORS → STG REG
10.01 COMP INDS N OUTPUT
AND
AND
AND
AND
AND
OR
+10V
CF
D
2CF
-30V
-30V
470
STG REG 18 5c.01-81
STG REG 20 5c.02-6c
TO STG REG 20 5c.03-36b
STG REG (N) OUTPUT 5c.04-8e
STG REG (N) OUTPUT 5c.05-51
STG REG (N) OUTPUT 5c.06-49
TO ADDER (N) 5c.07-6h
TO MQ REG (N) 5c.08-8e
(COL 19 ONLY) (TO ADDER-1) 5c.09-6b

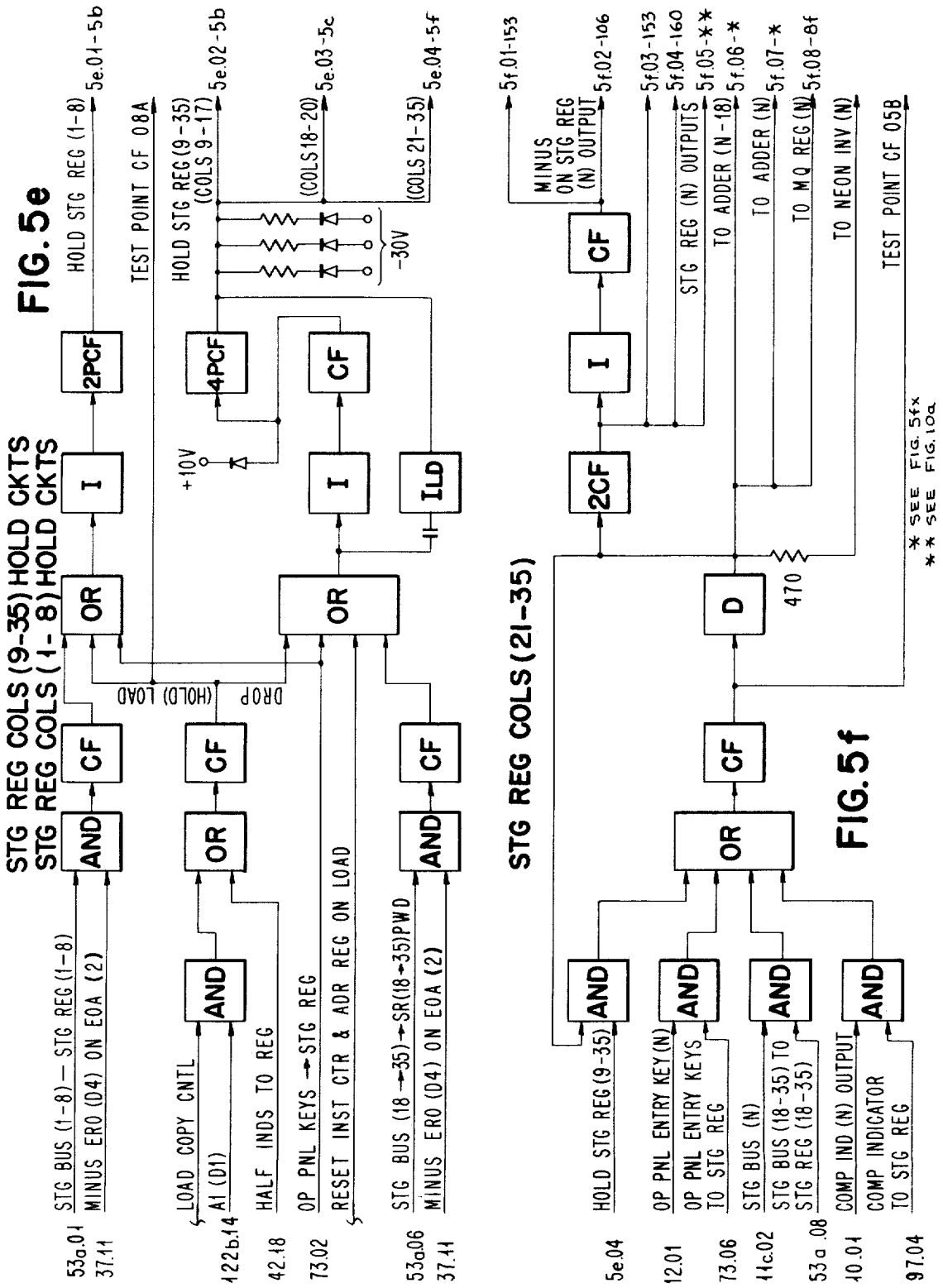
FIG. 5c

FIG. 5bx

STG BUS → STG REG	ARITH COL NO. (N)	STG REG (N) OUTPUTS		
		TO ADDER (N) FIG. NO.	TO MQ REG (N) FIG. NO.	TO PROGRAM CKTS FIG. NO.
1-8	1	6b	8b	99,13c
1-8	2	6c	8c	99,13c
1-8	3	6d	8c	13a
1-8	4	6c	8c	13a
1-8	5	6d	8c	13a
1-8	6	6e	8d	13a
1-8	7	6e	8d	13a
1-8	8	6e	8d	13b
S, 9-17	9	6f	8e	13b
S, 9-17	10	6g	8e	13c
S, 9-17	11	6g	8e	13c
S, 9-17	12	6k	8e	
S, 9-17	13	6l	8e	
S, 9-17	14	6k	8e	
S, 9-17	15	6m	8e	
S, 9-17	16	6j	8e	
S, 9-17	17	6l	8e	

FIG. 5fx

ARITH COL NO. (N)	STG REG (N) OUTPUTS		
	TO ADDER (N) FIG. NO.	TO ADDER (N-18) FIG. NO.	TO DSU INST. DECODER FIG. NO.
21	6i	6d	
22	6h	6c	
23	6h	6d	
24	6h	6e	160
25	6i	6e	160
26	6h	6e	160
27	6h	6f	
28	6h	6g	
29	6i	6g	
30	6h	6k	
31	6h	6l	
32	6h	6k	
33	6i	6m	
34	6h	6j	
35	6h	6l	


FIG. 5e
STG REG COLS (9-35) HOLD CKTS
STG REG COLS (1-8) HOLD CKTS
STG BUS (1-8) — STG REG (1-8)
MINUS ERO (D4) ON EOA (2)
LOAD COPY CNTL
A1 (D1)
HALF INDS TO REG
OP PNL KEYS → STG REG
RESET INST CTR & ADR REG ON LOAD
STG BUS (18→35) → SR (18→35) PWD
MINUS ERO (D4) ON EOA (2)
AND
OR
CF
I
2PCF
4PCF
ILD
+10V
-30V
DROP
(HOLD) LOAD
HOLD STG REG (1-8)
TEST POINT CF 08A
HOLD STG REG (9-35)
(COLS 9-17)
(COLS 18-20)
(COLS 21-35)
5e.01-5b
5e.02-5b
5e.03-5c
5e.04-5f
53a.01
37.11
122b.14
42.18
73.02
53a.06
37.11
STG REG COLS (21-35)
MINUS ON STG REG (N) OUTPUT
STG REG (N) OUTPUTS
TO ADDER (N-18)
TO ADDER (N)
TO MQ REG (N)
TO NEON INV (N)
TEST POINT CF 05B
2CF
D
470
5f.01-153
5f.02-106
5f.03-153
5f.04-160
5f.05-**
5f.06-*
5f.07-*
5f.08-8f
* SEE FIG. 5fx
** SEE FIG. 10a
HOLD STG REG (9-35)
OP PNL ENTRY KEY (N)
OP PNL ENTRY KEYS TO STG REG
STG BUS (N)
STG BUS (18-35) TO STG REG (18-35)
COMP IND (N) OUTPUT
COMP INDICATOR TO STG REG
5e.04
12.01
73.06
11c.02
53a.08
10.01
97.04
FIG. 5f

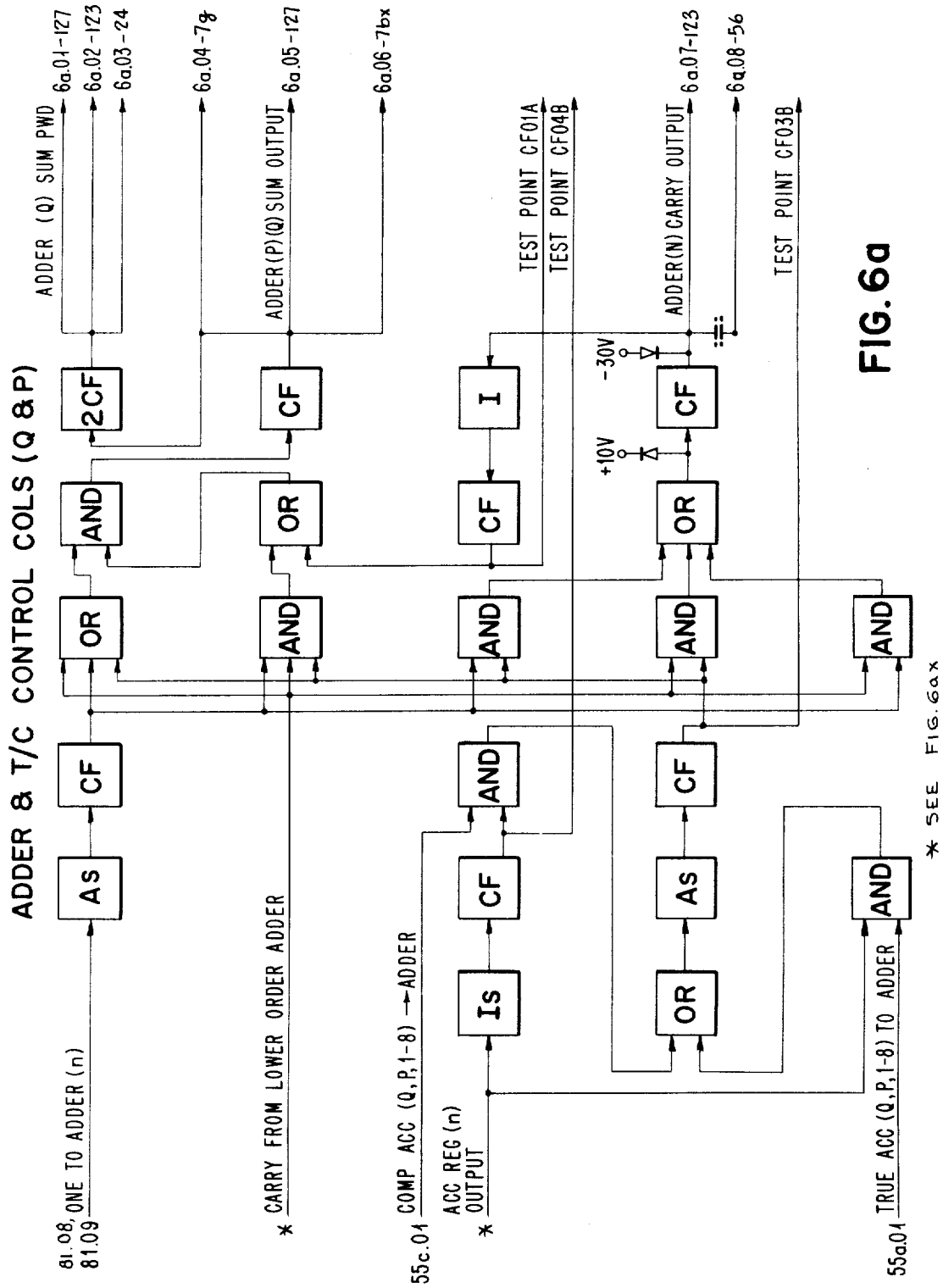

ADDER & T/C CONTROL COLS (Q & P)
ADDER (Q) SUM PWD
6a.01-127
6a.02-123
6a.03-24
6a.04-79
ADDER (P) (Q) SUM OUTPUT
6a.05-127
6a.06-7bx
TEST POINT CF01A
TEST POINT CF04B
ADDER (N) CARRY OUTPUT
6a.07-123
6a.08-56
TEST POINT CF03B
-30V
+10V
2CF
CF
I
AND
OR
As
Is
81.08, 81.09 ONE TO ADDER (n)
CARRY FROM LOWER ORDER ADDER
55c.01 COMP ACC (Q,P,1-8) → ADDER
ACC REG (n) OUTPUT
55a.01 TRUE ACC (Q,P,1-8) TO ADDER
* SEE FIG. 6ax

FIG. 6a

FIG. 6ax

ARITH COL NO.	ACC REG(N) OUTPUT FIG. NO.	ADDER (N) CARRY OUTPUT FIG. NO.	CARRY FROM LOWER ORDER FIG. NO.
Q	7g	123	6a
P	7b	6a	6b

FIG. 6cx

ARITH COL NO. (N)	ADDER CARRY OUTPUT FIG. NO.
2	6b
4	6d

FIG. 6dx

ARITH COL NO. (N)	CARRY INPUT FIG. NO.
3	6c
5	6e

FIG. 6ex

ARITH COL NO. (N)	ADDER CARRY OUTPUT FIG. NO.	CARRY INPUT FIG. NO.
6	6d	6e
7	6e	6e
8	6e	82

FIG. 6gx

ARITH COL NO. (N)	ADDER (N) CARRY OUTPUT FIG. NO.	CARRY INPUT FIG. NO.
10	6f	6g
11	6g	6k

FIG. 12a

OPERATOR PANEL ENTRY KEY (N)	FIG. NO.
S	5b
1	5b
2	5b
3	5b
4	5b
5	5b
6	5b
7	5b
8	5b
9	5b
10	5b
11	5b
12	5b
13	5b
14	5b
15	5b
16	5b
17	5b
18	5c
19	5c
20	5c
21	5f
22	5f
23	5f
24	5f
25	5f
26	5f
27	5f
28	5f
29	5f
30	5f
31	5f
32	5f
33	5f
34	5f
35	5f

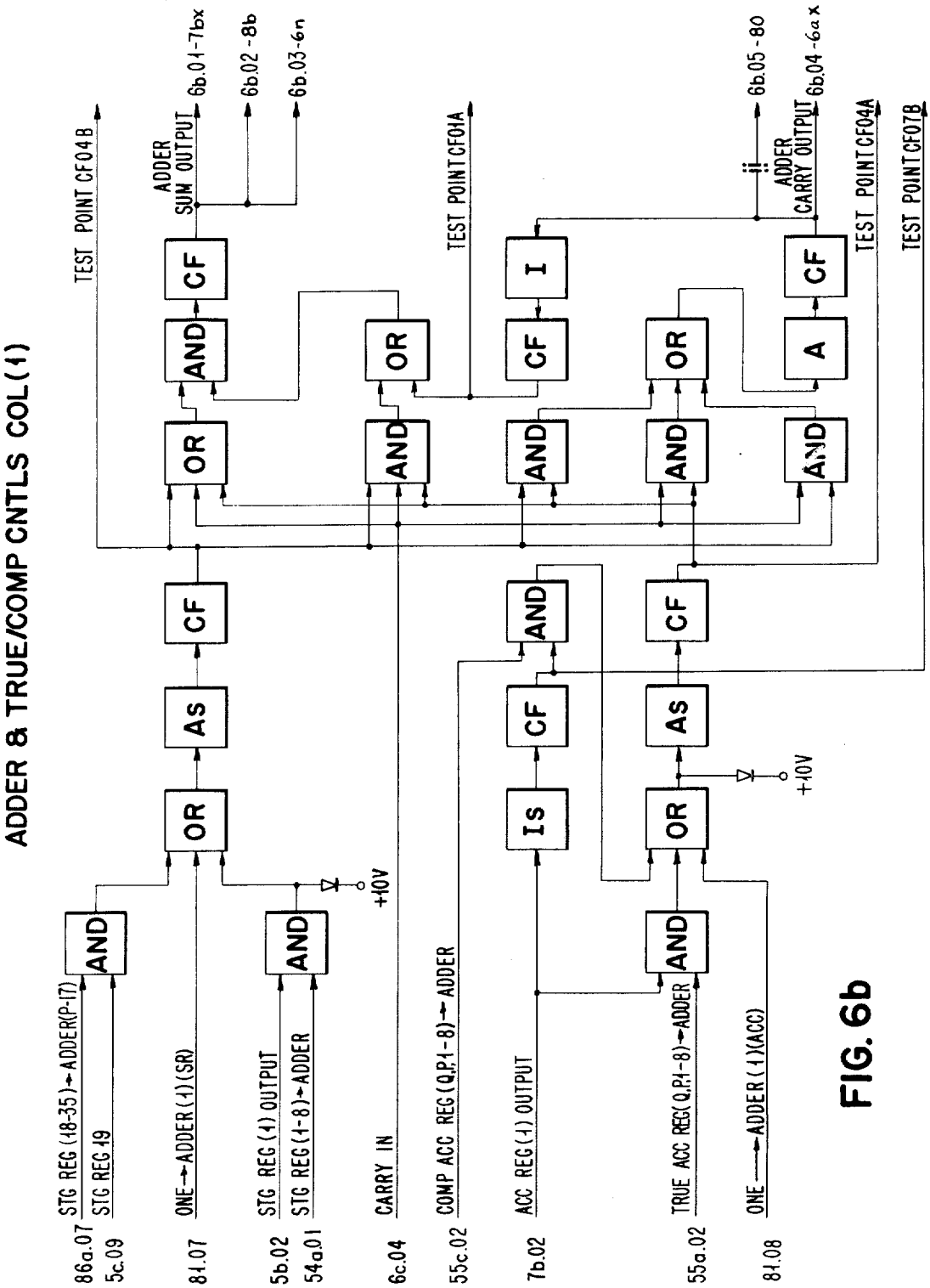
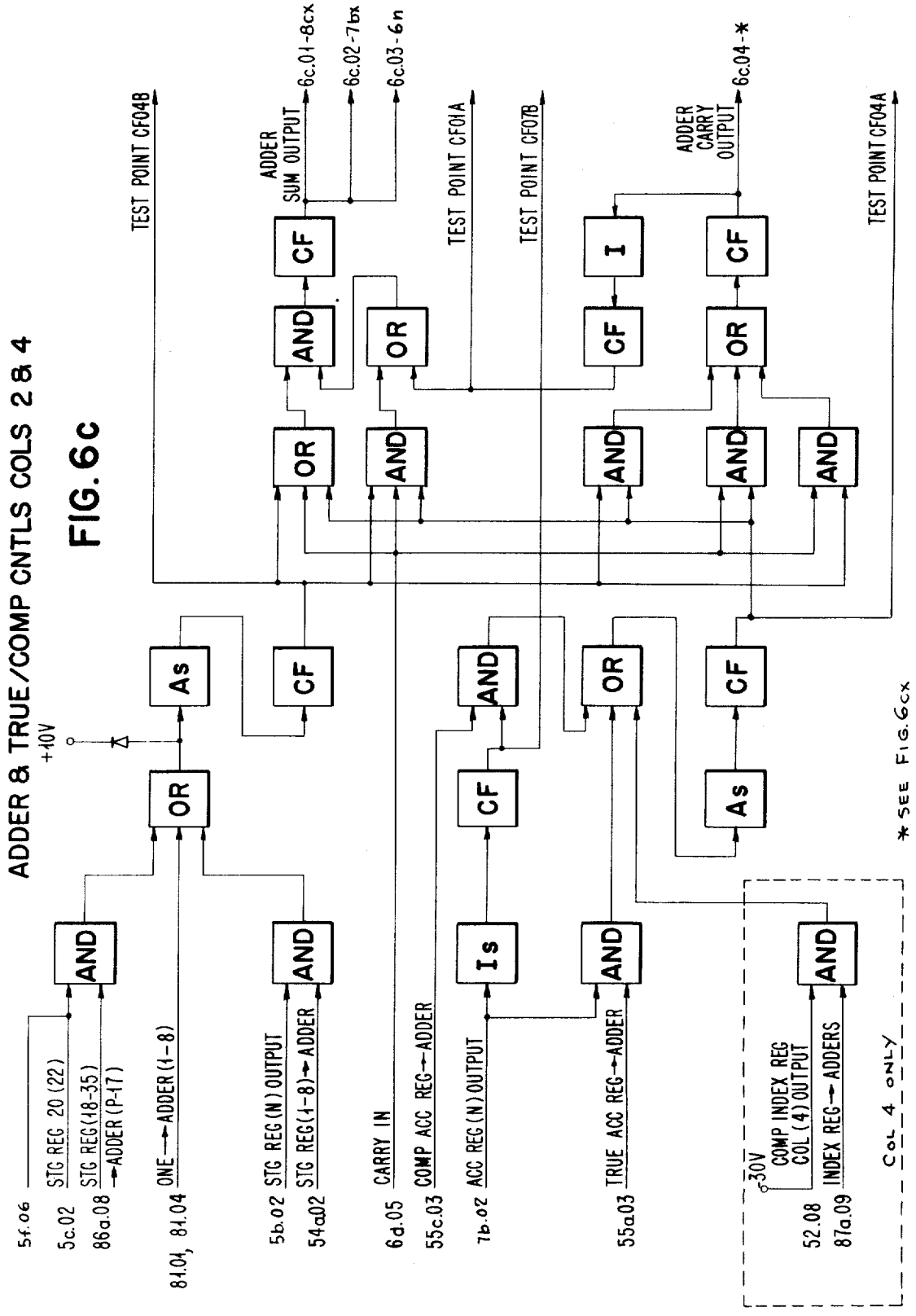

ADDER & TRUE/COMP CNTLS COL (1)
STG REG (18-35) → ADDER(P-17)
STG REG 19
86a.07
5c.09
ONE → ADDER (1) (SR)
81.07
STG REG (1) OUTPUT
STG REG (1-8) → ADDER
5b.02
54a.01
CARRY IN
6c.04
COMP ACC REG (Q,P,1-8) → ADDER
55c.02
ACC REG (1) OUTPUT
7b.02
TRUE ACC REG (Q,P,1-8) → ADDER
55a.02
ONE → ADDER (1) (ACC)
81.08
AND
OR
As
Is
CF
I
A
+10V
TEST POINT CF04B
TEST POINT CF01A
TEST POINT CF04A
TEST POINT CF07B
ADDER SUM OUTPUT
6b.01-7bx
6b.02-8b
6b.03-6n
ADDER CARRY OUTPUT
6b.04-6ax
6b.05-80

FIG. 6b


ADDER & TRUE/COMP CNTLS COLS 2 & 4
FIG. 6c
+10V
TEST POINT CF04B
TEST POINT CF01A
TEST POINT CF07B
TEST POINT CF04A
ADDER SUM OUTPUT
6c.01-8cx
6c.02-7bx
6c.03-6n
ADDER CARRY OUTPUT
6c.04-*
AND
OR
CF
As
Is
I
5f.06
5c.02 STG REG 20 (22)
86a.08 STG REG(18-35) → ADDER (P-17)
81.04, 81.04 ONE → ADDER (1-8)
5b.02 STG REG (N) OUTPUT
54a02 STG REG(1-8) → ADDER
6d.05 CARRY IN
55c.03 COMP ACC REG → ADDER
7b.02 ACC REG (N) OUTPUT
55a03 TRUE ACC REG → ADDER
-30V
52.08 COMP INDEX REG COL (4) OUTPUT
87a.09 INDEX REG → ADDERS
COL 4 ONLY
* SEE FIG. 6cx

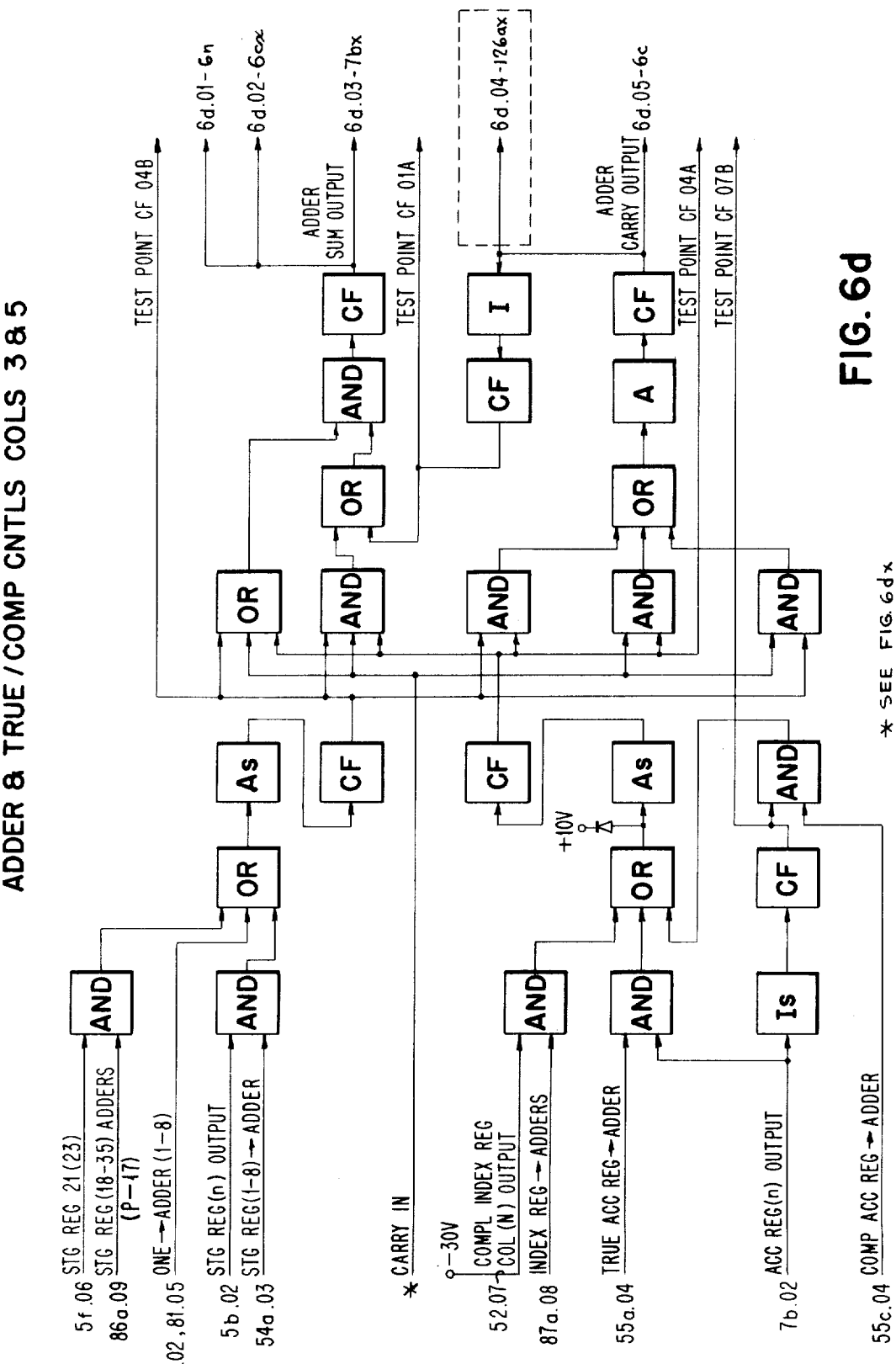

ADDER & TRUE / COMP CNTLS COLS 3 & 5
TEST POINT CF 04B
6d.01-6n
6d.02-6cx
ADDER SUM OUTPUT
6d.03-7bx
TEST POINT CF 01A
6d.04-126ax
ADDER CARRY OUTPUT
6d.05-6c
TEST POINT CF 04A
TEST POINT CF 07B
5f.06 STG REG 21(23)
86a.09 STG REG(18-35) ADDERS (P-17)
81.02, 81.05 ONE → ADDER (1-8)
5b.02 STG REG(n) OUTPUT
54a.03 STG REG(1-8) → ADDER
* CARRY IN
-30V
52.07 COMPL INDEX REG COL (N) OUTPUT
87a.08 INDEX REG → ADDERS
+10V
55a.04 TRUE ACC REG → ADDER
7b.02 ACC REG(n) OUTPUT
55c.04 COMP ACC REG → ADDER
AND
OR
As
CF
I
A
Is
* SEE FIG. 6dx

FIG. 6d

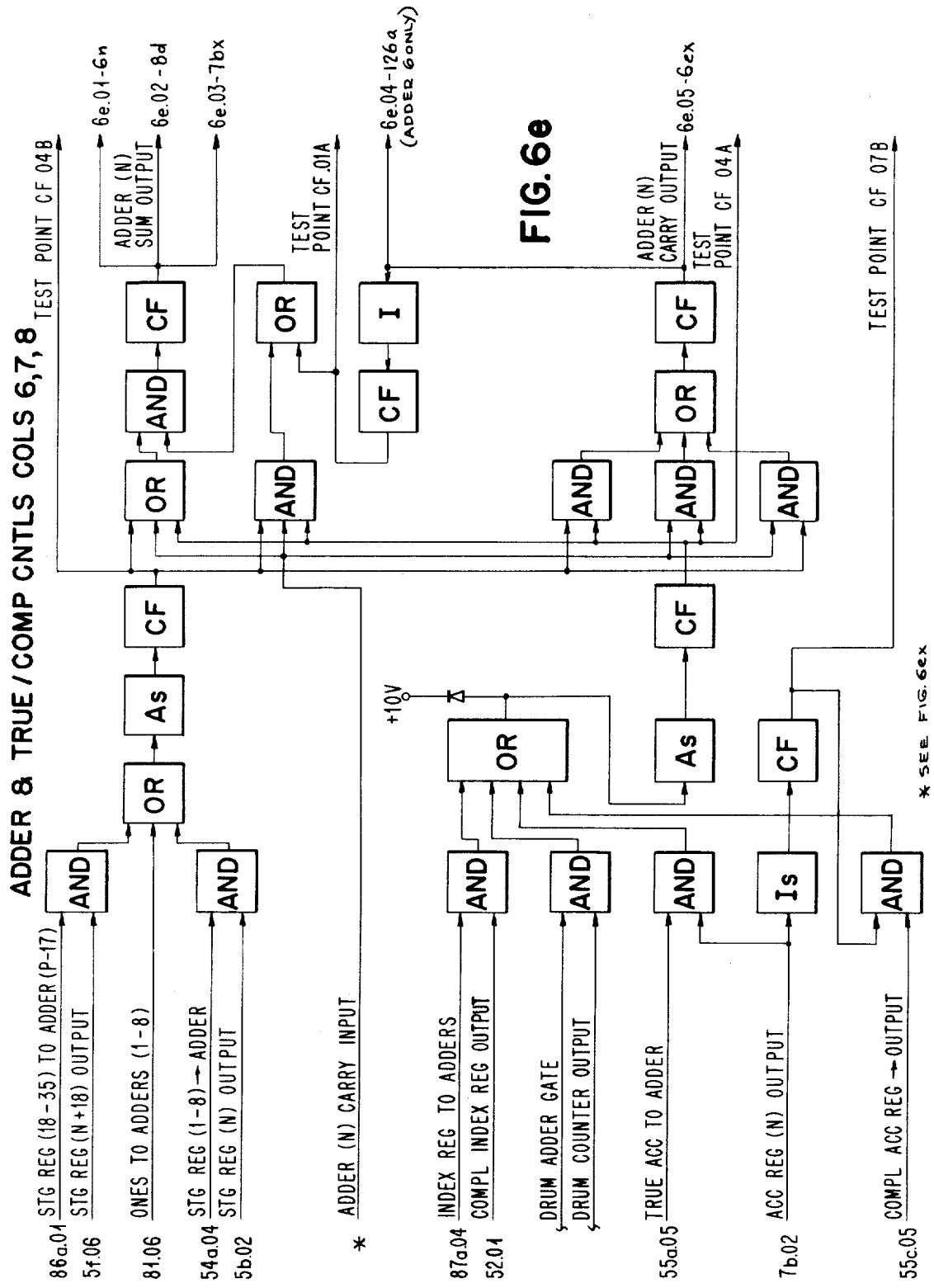

ADDER & TRUE/COMP CNTLS COLS 6,7,8
TEST POINT CF 04B
6e.01-6n
ADDER (N) SUM OUTPUT
6e.02-8d
6e.03-7bx
TEST POINT CF.01A
6e.04-126a (ADDER 6 ONLY)
ADDER (N) CARRY OUTPUT
6e.05-6ex
TEST POINT CF 04A
TEST POINT CF 07B
AND
OR
As
CF
I
Is
+10V
86a.01 STG REG (18-35) TO ADDER (P-17)
5f.06 STG REG (N+18) OUTPUT
81.03, 81.06 ONES TO ADDERS (1-8)
54a.04 STG REG (1-8) → ADDER
5b.02 STG REG (N) OUTPUT
* ADDER (N) CARRY INPUT
87a.04 INDEX REG TO ADDERS
52.01 COMPL INDEX REG OUTPUT
DRUM ADDER GATE
DRUM COUNTER OUTPUT
55a.05 TRUE ACC TO ADDER
7b.02 ACC REG (N) OUTPUT
55c.05 COMPL ACC REG → OUTPUT
* SEE FIG. 6ex

FIG. 6e

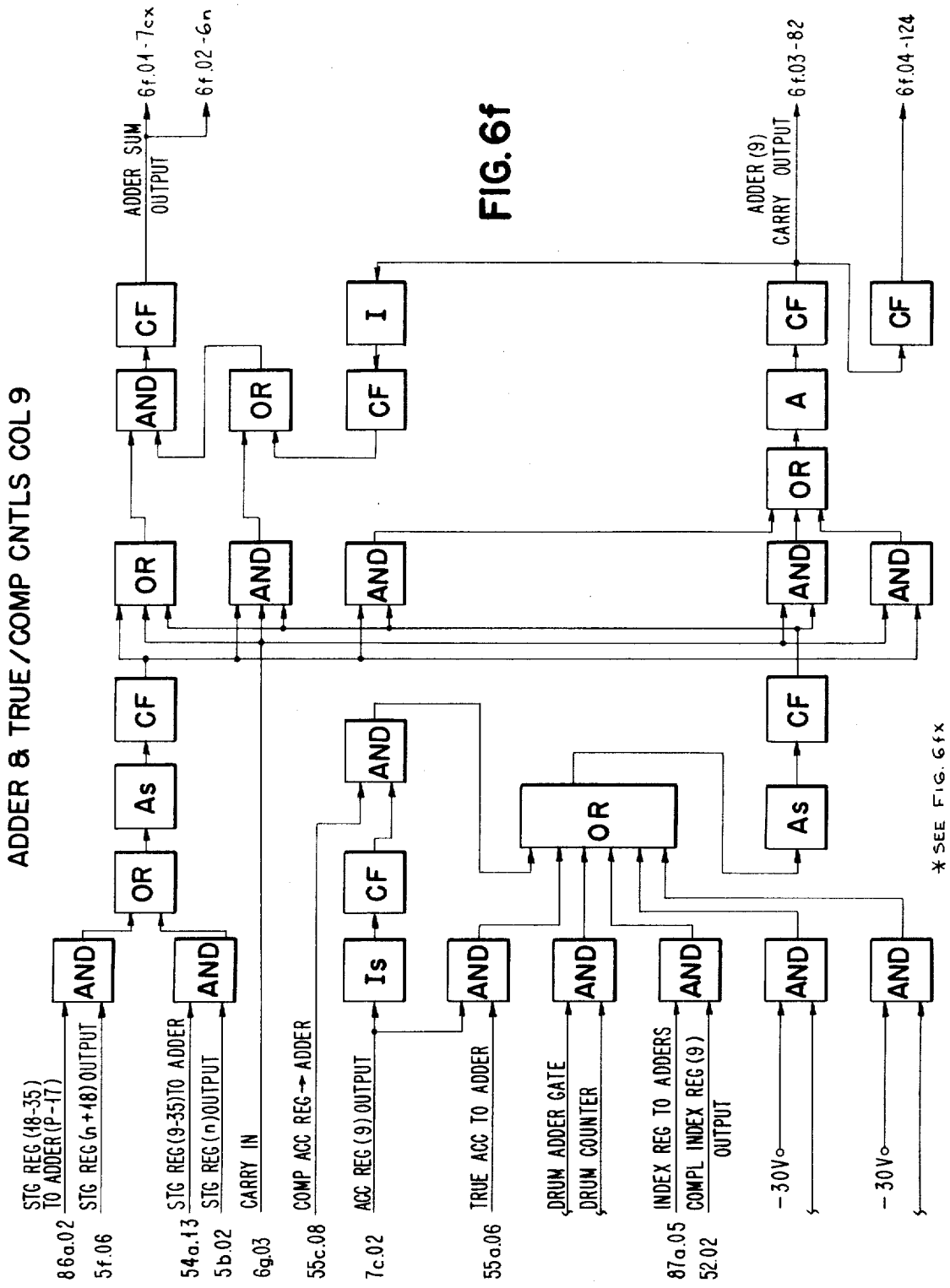
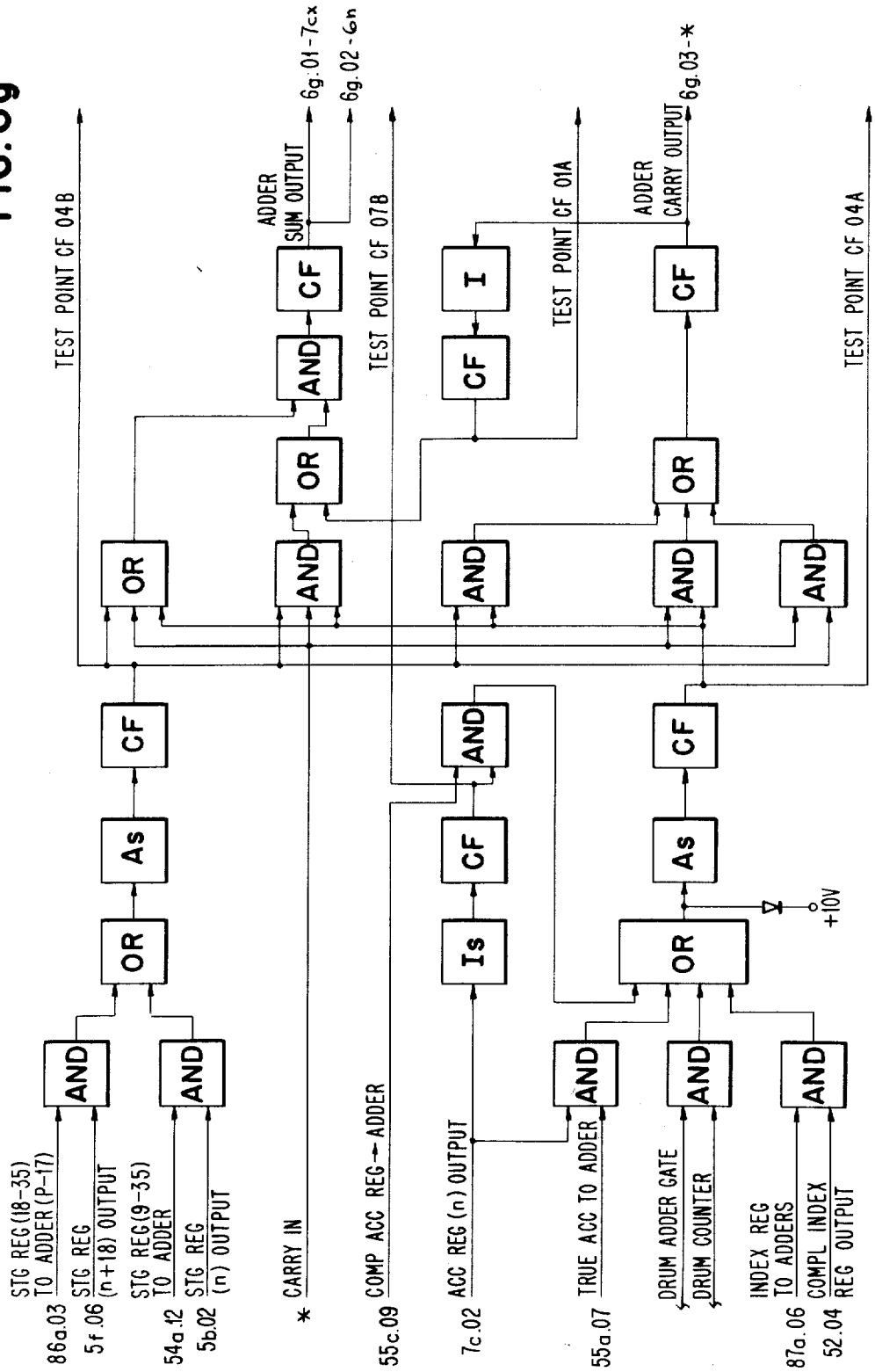

ADDER & TRUE/COMP CNTLS COL 9
STG REG (18-35) TO ADDER (P-17)
86a.02
STG REG (n+18) OUTPUT
5f.06
STG REG (9-35) TO ADDER
54a.13
STG REG (n) OUTPUT
5b.02
CARRY IN
6g.03
COMP ACC REG → ADDER
55c.08
ACC REG (9) OUTPUT
7c.02
TRUE ACC TO ADDER
55a.06
DRUM ADDER GATE
DRUM COUNTER
INDEX REG TO ADDERS
87a.05
COMPL INDEX REG (9) OUTPUT
52.02
-30V
-30V
AND
OR
As
CF
Is
I
A
ADDER SUM OUTPUT
6f.04-7cx
6f.02-6n
ADDER (9) CARRY OUTPUT
6f.03-82
6f.04-124
* SEE FIG. 6fx

FIG. 6f

FIG. 6g

ADDER & TRUE/COMP CNTLS COLS 10, 11



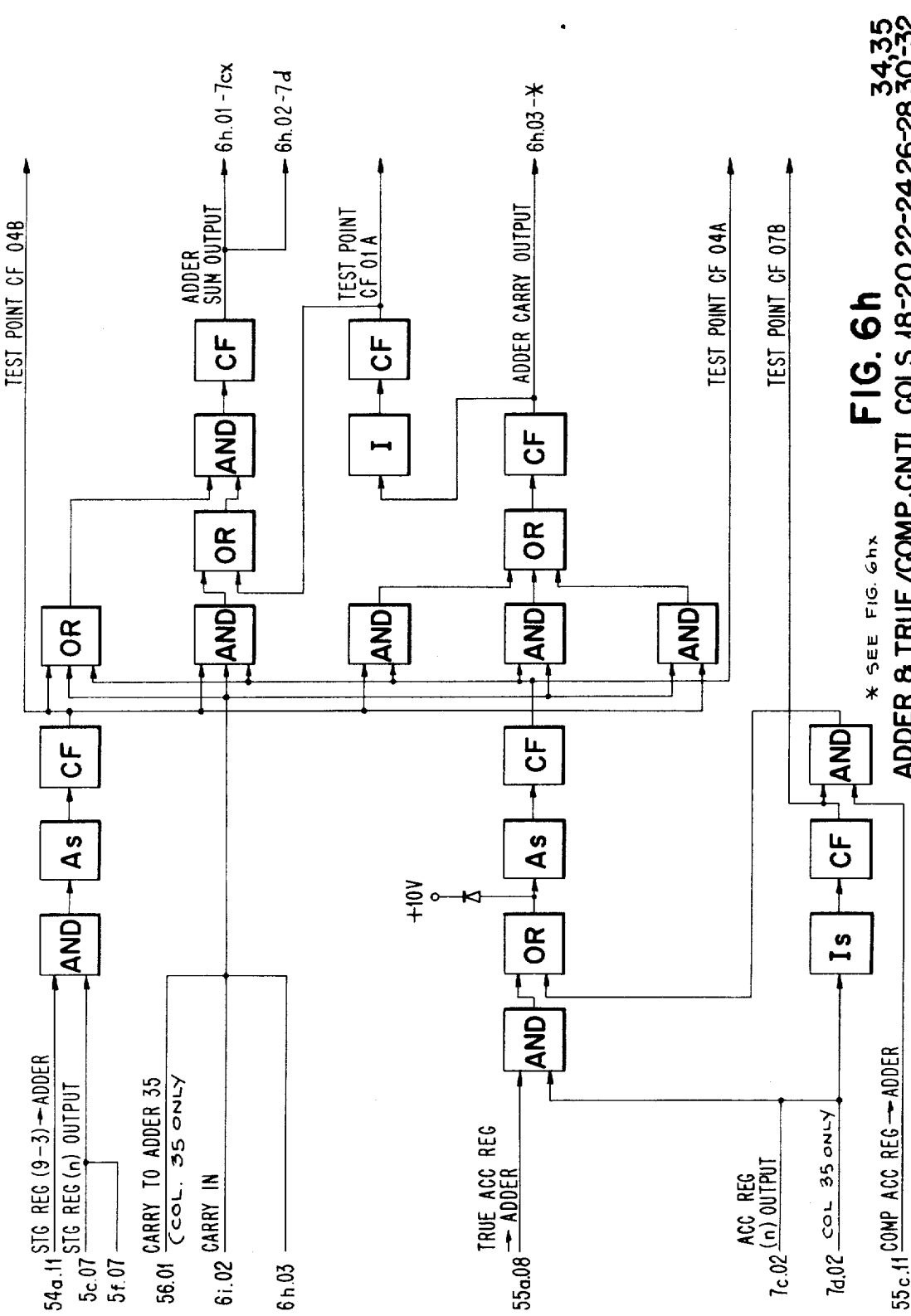


FIG. 6h

ADDER & TRUE/COMP. CNTL COLS 18-20, 22-24, 26-28, 30-32, 34, 35

FIG. 6hx

ARITH COL NO. (N)	ADDER (N) CARRY OUTPUT FIG. NO.
18	6l
19	6h
20	6h
22	6i
23	6h
24	6h
26	6i
27	6h
28	6h
30	6i
31	6h
32	6h
34	6i
35	6h

FIG. 6kx

ARITH COL NO. (N)	ADDER (N) CARRY OUTPUT FIG. NO.	CARRY INPUT FIG. NO.
12	6g	6l
14	6l	6m

FIG. 6lx

ARITH COL NO. (N)	ADDER (N) CARRY OUTPUT FIG. NO.	CARRY INPUT FIG. NO.
13	6k	6k
17	6j	6h

COL (N)	OUTPUT	
	SRN FIG. NO.	$\overline{\text{SRN}}$ FIG. NO.
S	227b	227b
1	227a,b	227a,b,c
2	227c	227c
3	227d	227c
4	227c	227c
5	227d	227c
6-29	225a	225a

FIG. 225ax

FIG. 10a

STG REG (N)	STG REG(N) FIG. NO.	STG BUS(N) FIG. NO.
S	5a	11a
1	5b	11b
2	5b	11b
3	5b	11c
4	5b	11c
5	5b	11c
6	5b	11c
7	5b	11c
8	5b	11c
9	5b	11c
10	5b	11c
11	5b	11c
12	5b	11c
13	5b	11c
14	5b	11c
15	5b	11c
16	5b	11c
17	5b	11c
18	5c	11b
19	5c	11b
20	5c	11b
21	5f	11c
22	5f	11c
23	5f	11c
24	5f	11c
25	5f	11c
26	5f	11c
27	5f	11c
28	5f	11c
29	5f	11c
30	5f	11c
31	5f	11c
32	5f	11c
33	5f	11c
34	5f	11c
35	5f	11c

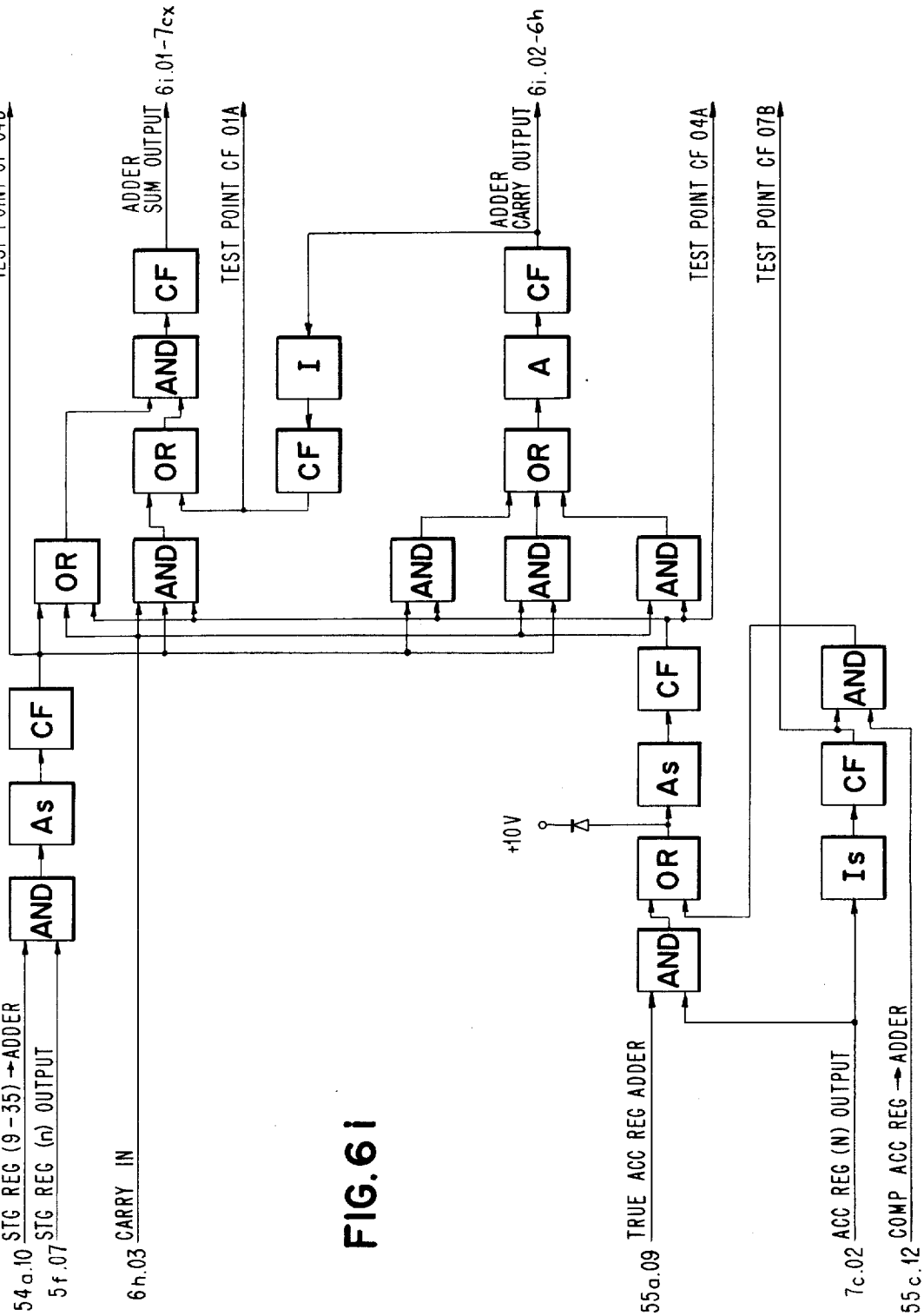

ADDER & TRUE / COMP CNTLS - COLS 21, 25, 29, 33
TEST POINT CF 04B
ADDER SUM OUTPUT
6i.01-7cx
TEST POINT CF 01A
ADDER CARRY OUTPUT
6i.02-6h
TEST POINT CF 04A
TEST POINT CF 07B
54a.10 STG REG (9-35) → ADDER
5f.07 STG REG (n) OUTPUT
6h.03 CARRY IN
55a.09 TRUE ACC REG ADDER
7c.02 ACC REG (N) OUTPUT
55c.12 COMP ACC REG → ADDER
+10V
AND
As
CF
OR
I
A
Is

FIG. 6i

ADDER & TRUE / COMP CNTLS COL 16

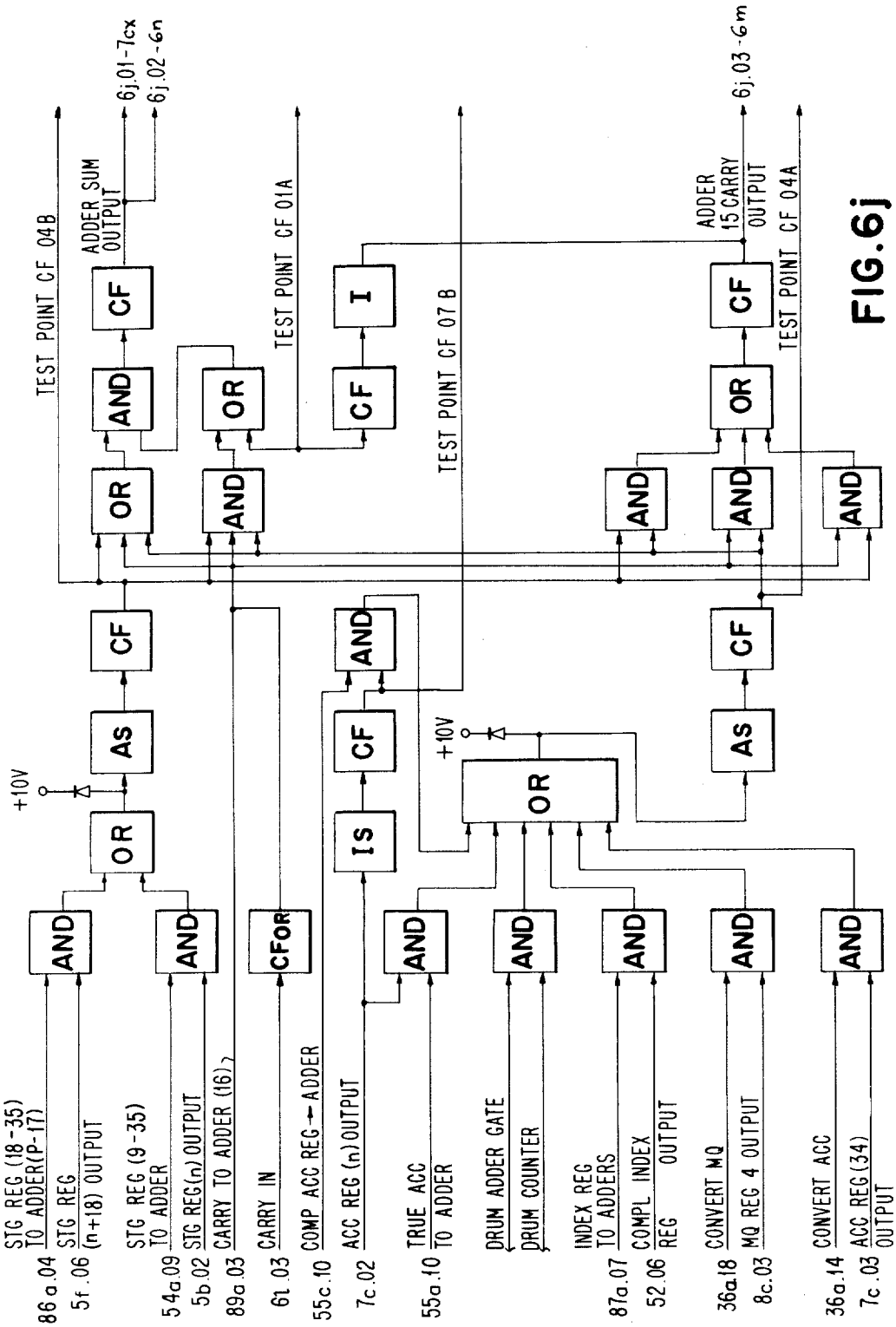
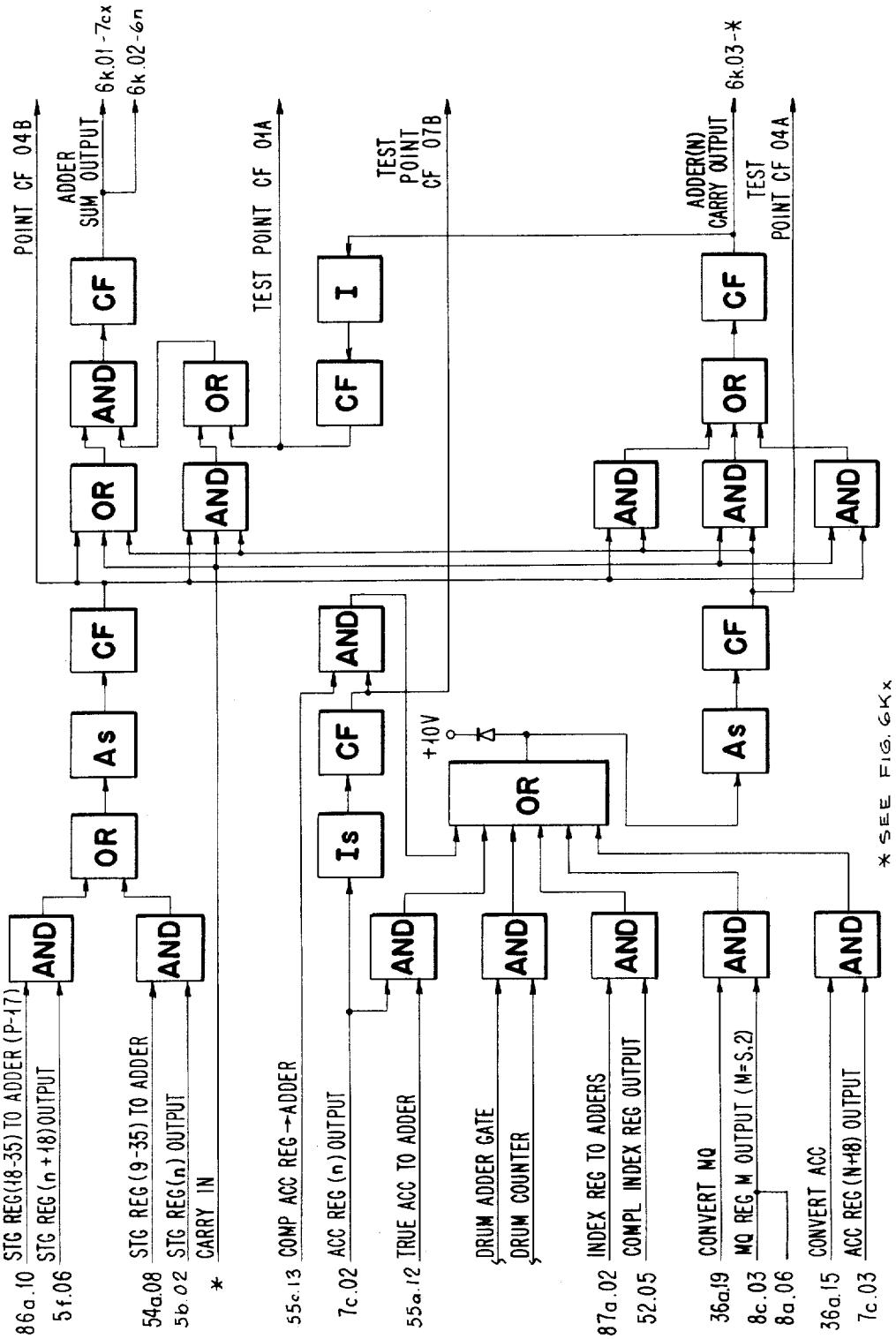


FIG.6j

FIG. 6k

ADDER & TRUE/COMP CNTLS COLS 12, 14



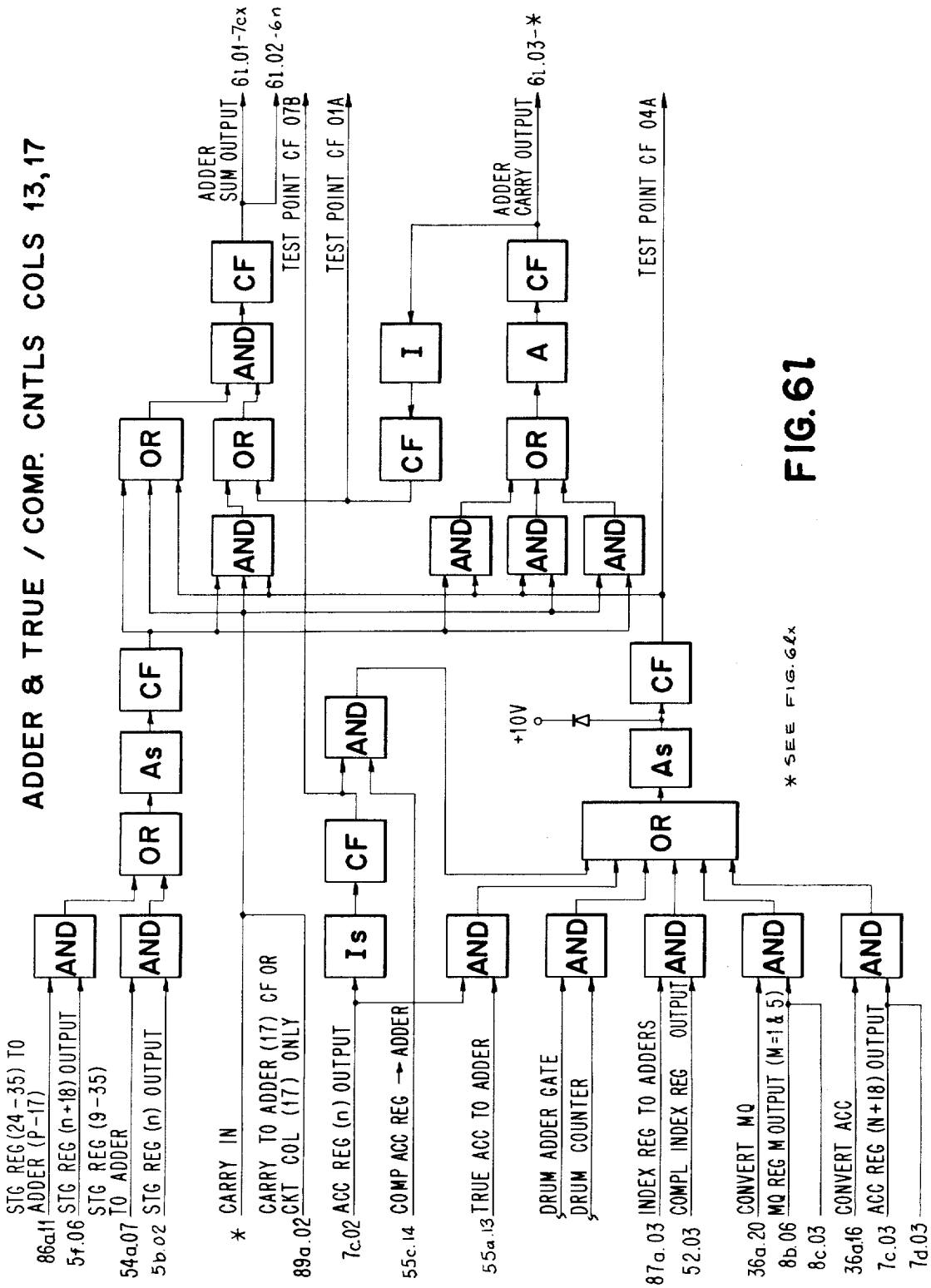

ADDER & TRUE / COMP. CNTLS COLS 13,17
STG REG (24-35) TO ADDER (P-17)
86a.11
STG REG (n+18) OUTPUT
5f.06
STG REG (9-35) TO ADDER
54a.07
STG REG (n) OUTPUT
5b.02
CARRY IN
CARRY TO ADDER (17) CF OR CKT COL (17) ONLY
89a.02
ACC REG (n) OUTPUT
7c.02
COMP ACC REG → ADDER
55c.14
TRUE ACC TO ADDER
55a.13
DRUM ADDER GATE
DRUM COUNTER
INDEX REG TO ADDERS
87a.03
COMPL INDEX REG OUTPUT
52.03
CONVERT MQ
36a.20
MQ REG M OUTPUT (M=1 & 5)
8b.06
8c.03
CONVERT ACC
36a.16
ACC REG (N+18) OUTPUT
7c.03
7d.03
AND
OR
As
CF
Is
I
A
+10V
ADDER SUM OUTPUT
61.01-7cx
TEST POINT CF 07B
61.02-6n
TEST POINT CF 01A
ADDER CARRY OUTPUT
61.03-*
TEST POINT CF 04A
* SEE FIG. 62x

FIG. 61

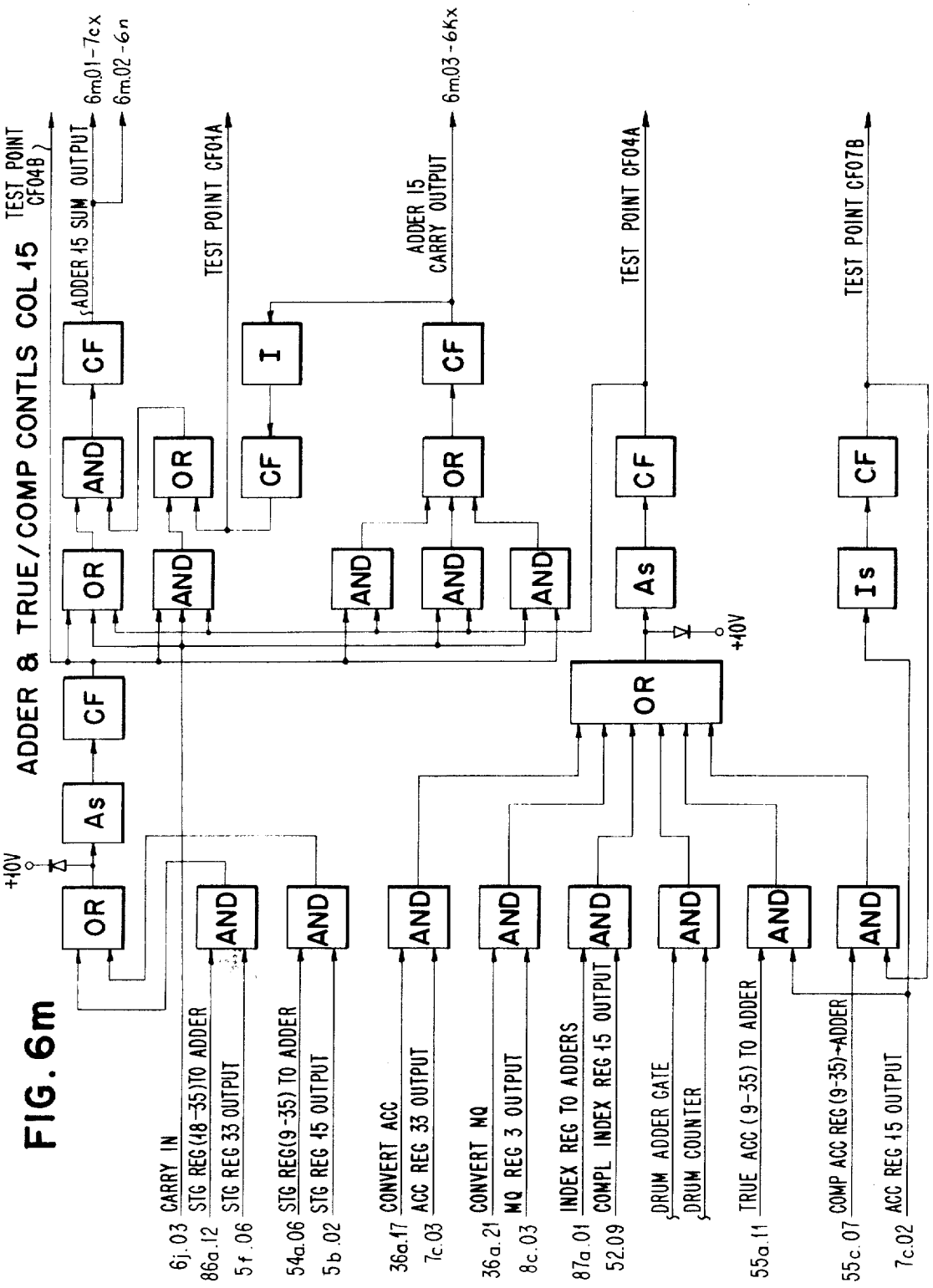

ADDER & TRUE/COMP CONTLS COL 15
TEST POINT CF04B
ADDER 15 SUM OUTPUT
6m.01-7cx
6m.02-6n
TEST POINT CF01A
ADDER 15 CARRY OUTPUT
6m.03-6kx
TEST POINT CF04A
TEST POINT CF07B
+10V
+10V
OR
AS
CF
AND
OR
CF
I
CF
AND
OR
AND
AND
AND
AND
OR
AS
CF
IS
CF
AND
AND
AND
AND
AND
AND
AND
AND
6j.03 CARRY IN
86a.12 STG REG(18-35)TO ADDER
5f.06 STG REG 33 OUTPUT
54a.06 STG REG(9-35) TO ADDER
5b.02 STG REG 15 OUTPUT
36a.17 CONVERT ACC
7c.03 ACC REG 33 OUTPUT
36a.21 CONVERT MQ
8c.03 MQ REG 3 OUTPUT
87a.01 INDEX REG TO ADDERS
52.09 COMPL INDEX REG 15 OUTPUT
DRUM ADDER GATE
DRUM COUNTER
55a.11 TRUE ACC (9-35) TO ADDER
55c.07 COMP ACC REG (9-35)→ADDER
7c.02 ACC REG 15 OUTPUT

FIG. 6m

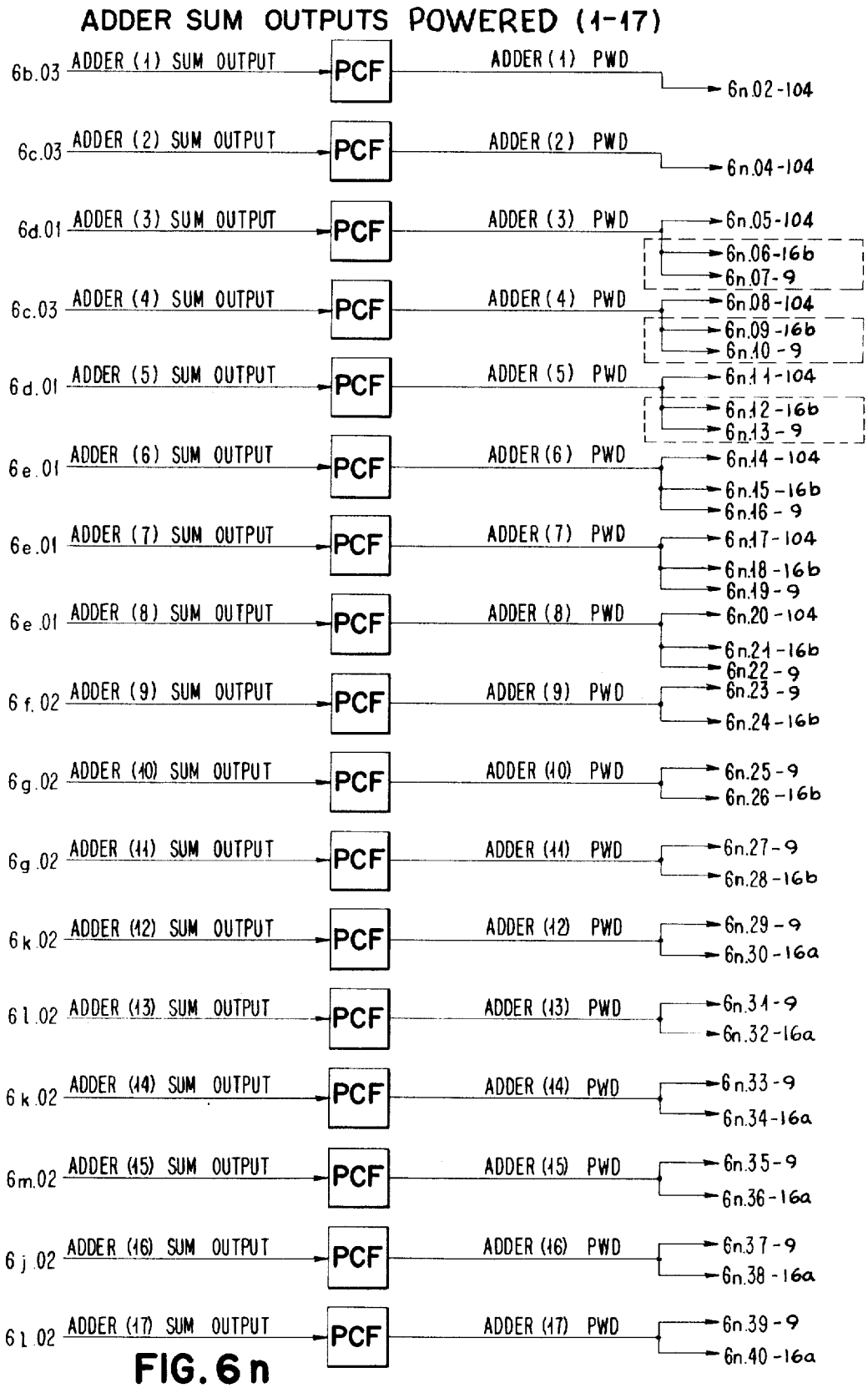

ADDER SUM OUTPUTS POWERED (1-17)
6b.03 ADDER (1) SUM OUTPUT
PCF
ADDER (1) PWD
6n.02-104
6c.03 ADDER (2) SUM OUTPUT
PCF
ADDER (2) PWD
6n.04-104
6d.01 ADDER (3) SUM OUTPUT
PCF
ADDER (3) PWD
6n.05-104
6n.06-16b
6n.07-9
6c.03 ADDER (4) SUM OUTPUT
PCF
ADDER (4) PWD
6n.08-104
6n.09-16b
6n.10-9
6d.01 ADDER (5) SUM OUTPUT
PCF
ADDER (5) PWD
6n.11-104
6n.12-16b
6n.13-9
6e.01 ADDER (6) SUM OUTPUT
PCF
ADDER (6) PWD
6n.14-104
6n.15-16b
6n.16-9
6e.01 ADDER (7) SUM OUTPUT
PCF
ADDER (7) PWD
6n.17-104
6n.18-16b
6n.19-9
6e.01 ADDER (8) SUM OUTPUT
PCF
ADDER (8) PWD
6n.20-104
6n.21-16b
6n.22-9
6f.02 ADDER (9) SUM OUTPUT
PCF
ADDER (9) PWD
6n.23-9
6n.24-16b
6g.02 ADDER (10) SUM OUTPUT
PCF
ADDER (10) PWD
6n.25-9
6n.26-16b
6g.02 ADDER (11) SUM OUTPUT
PCF
ADDER (11) PWD
6n.27-9
6n.28-16b
6k.02 ADDER (12) SUM OUTPUT
PCF
ADDER (12) PWD
6n.29-9
6n.30-16a
6l.02 ADDER (13) SUM OUTPUT
PCF
ADDER (13) PWD
6n.31-9
6n.32-16a
6k.02 ADDER (14) SUM OUTPUT
PCF
ADDER (14) PWD
6n.33-9
6n.34-16a
6m.02 ADDER (15) SUM OUTPUT
PCF
ADDER (15) PWD
6n.35-9
6n.36-16a
6j.02 ADDER (16) SUM OUTPUT
PCF
ADDER (16) PWD
6n.37-9
6n.38-16a
6l.02 ADDER (17) SUM OUTPUT
PCF
ADDER (17) PWD
6n.39-9
6n.40-16a

FIG. 6n

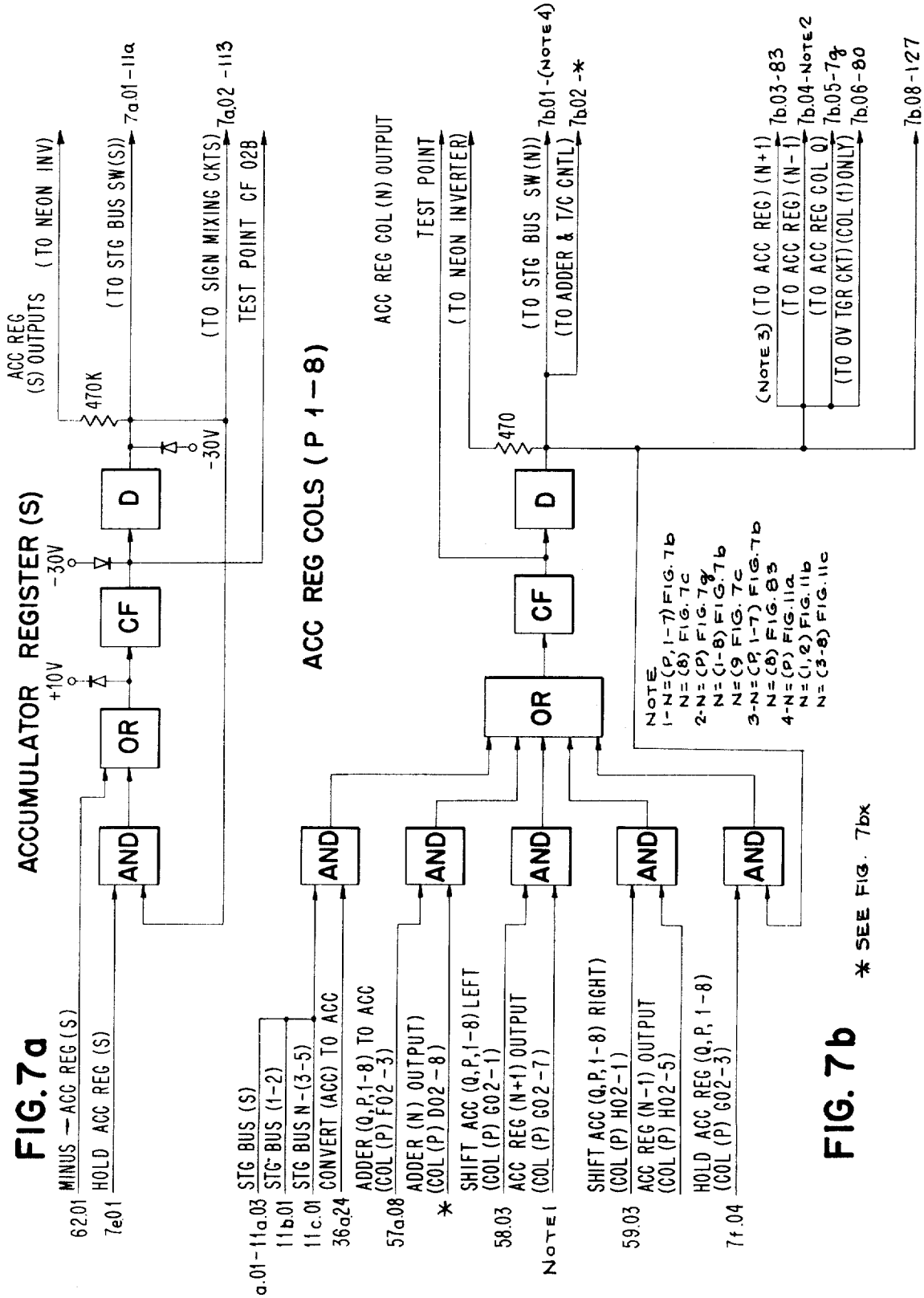

ACCUMULATOR REGISTER (S)
MINUS — ACC REG (S)
HOLD ACC REG (S)
62.01
7e01
+10V
-30V
AND
OR
CF
D
470K
-30V
ACC REG (S) OUTPUTS
(TO NEON INV)
(TO STG BUS SW(S))
7a.01-11a
(TO SIGN MIXING CKTS)
TEST POINT CF 02B
7a.02-113
ACC REG COLS (P 1-8)
11a.01-11a.03 STG BUS (S)
11b.01 STG BUS (1-2)
11c.01 STG BUS N-(3-5)
36a.24 CONVERT (ACC) TO ACC
57a.08 ADDER (Q,P,1-8) TO ACC (COL (P) F02-3)
* ADDER (N) OUTPUT (COL (P) D02-8)
58.03 SHIFT ACC (Q,P,1-8) LEFT (COL (P) G02-1)
NOTE1 ACC REG (N+1) OUTPUT (COL (P) G02-7)
59.03 SHIFT ACC (Q,P,1-8) RIGHT (COL (P) H02-1)
ACC REG (N-1) OUTPUT (COL (P) H02-5)
7f.04 HOLD ACC REG (Q,P,1-8) (COL (P) G02-3)
ACC REG COL (N) OUTPUT
TEST POINT
(TO NEON INVERTER)
470
(TO STG BUS SW (N))
(TO ADDER & T/C CNTL)
7b.01-(NOTE 4)
7b.02-*
(NOTE 3) (TO ACC REG) (N+1)
(TO ACC REG) (N-1)
(TO ACC REG COL Q)
(TO OV TGR CKT) (COL (1) ONLY)
7b.03-83
7b.04-NOTE 2
7b.05-79
7b.06-80
7b.08-127
NOTE
1-N=(P, 1-7) FIG. 7b
N=(8) FIG. 7c
2-N=(P) FIG. 79
N=(1-8) FIG. 7b
N=(9 FIG. 7c
3-N=(P, 1-7) FIG. 7b
N=(8) FIG. 83
4-N=(P) FIG. 11a
N=(1,2) FIG. 11b
N=(3-8) FIG. 11c
* SEE FIG. 7bx

FIG. 7a

FIG. 7b

FIG. 7bx

ARITH COL NO. (N)	ADDER & T/C CNTL FIG. NO.
P	6a
1	6b
2	6c
3	6d
4	6c
5	6d
6	6e
7	6e
8	6e

FIG. 7cx

ARITH COL NO. (N)	TO ADDER & T/C CNTLS FIG. NO.	TO TRUE COMP & ADD (N-18) FIG. NO.
9	6f	
10	6g	
11	6g	
12	6k	
13	6f	
14	6k	
15	6m	
16	6j	
17	6l	
18	6h	
19	6h	
20	6h	
21	6i	
22	6h	
23	6h	
24	6h	
25	6i	
26	6h	
27	6h	
28	6h	
29	6i	
30	6h	6k
31	6h	6l
32	6h	6k
33	6i	6m
34	6h	6j

FIG. 8cx

ARITH COL NO. (N)	ADDER(N) SUM OUTPUT FIG. NO.	OUTPUT TO STG BUS SW(N) FIG. NO.	ADDER & T/C CNTLS COL (N) FIG. NO.
2	6c	11b	6k
3	6d	11c	6m
4	6c	11c	6j
5	6d	11c	6l

FIG. 126ax

ADDER COL (N)	ADDER (N) CARRY OUTPUT FIG. NO.
3	6d
5	6d
6	6e

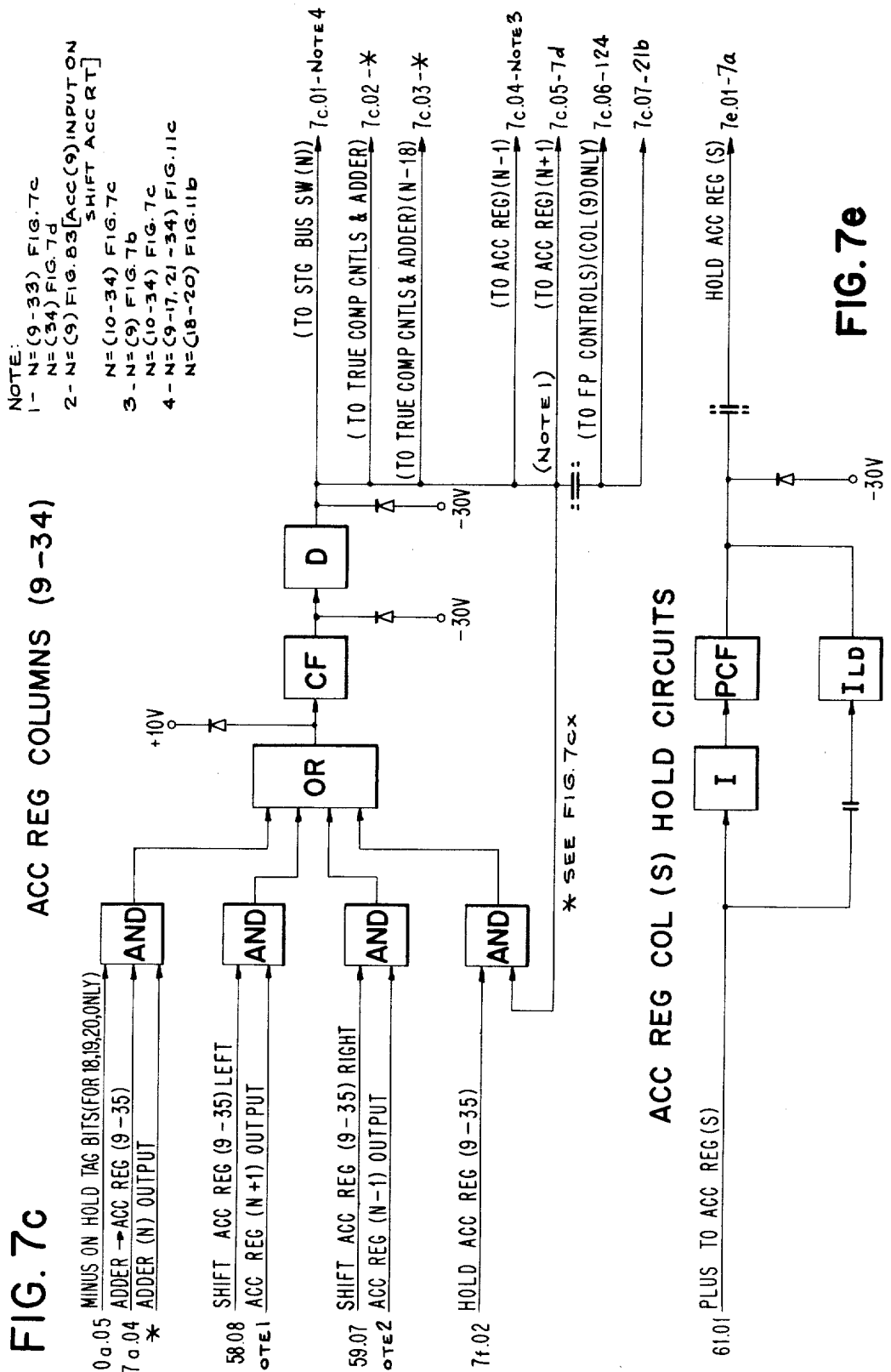

NOTE:
1- N=(9-33) FIG.7c
N=(34) FIG.7d
2- N=(9) FIG.83 [ACC(9) INPUT ON SHIFT ACC RT]
N=(10-34) FIG.7c
3- N=(9) FIG.7b
N=(10-34) FIG.7c
4- N=(9-17, 21-34) FIG.11c
N=(18-20) FIG.11b
ACC REG COLUMNS (9-34)
90a.05 MINUS ON HOLD TAG BITS (FOR 18,19,20, ONLY)
57a.04 ADDER → ACC REG (9-35)
* ADDER (N) OUTPUT
58.08 SHIFT ACC REG (9-35) LEFT
NOTE 1 ACC REG (N+1) OUTPUT
59.07 SHIFT ACC REG (9-35) RIGHT
NOTE 2 ACC REG (N-1) OUTPUT
7f.02 HOLD ACC REG (9-35)
AND
OR
+10V
CF
D
-30V
-30V
-30V
(TO STG BUS SW (N)) 7c.01-NOTE 4
(TO TRUE COMP CNTLS & ADDER) 7c.02-*
(TO TRUE COMP CNTLS & ADDER) (N-18) 7c.03-*
(TO ACC REG) (N-1) 7c.04-NOTE 3
(NOTE 1) (TO ACC REG) (N+1) 7c.05-7d
(TO FP CONTROLS) (COL (9) ONLY) 7c.06-124
7c.07-21b
* SEE FIG. 7cx
ACC REG COL (S) HOLD CIRCUITS
61.01 PLUS TO ACC REG (S)
I
PCF
ILD
HOLD ACC REG (S) 7e.01-7a
-30V

FIG. 7c

FIG. 7e

FIG. 7d

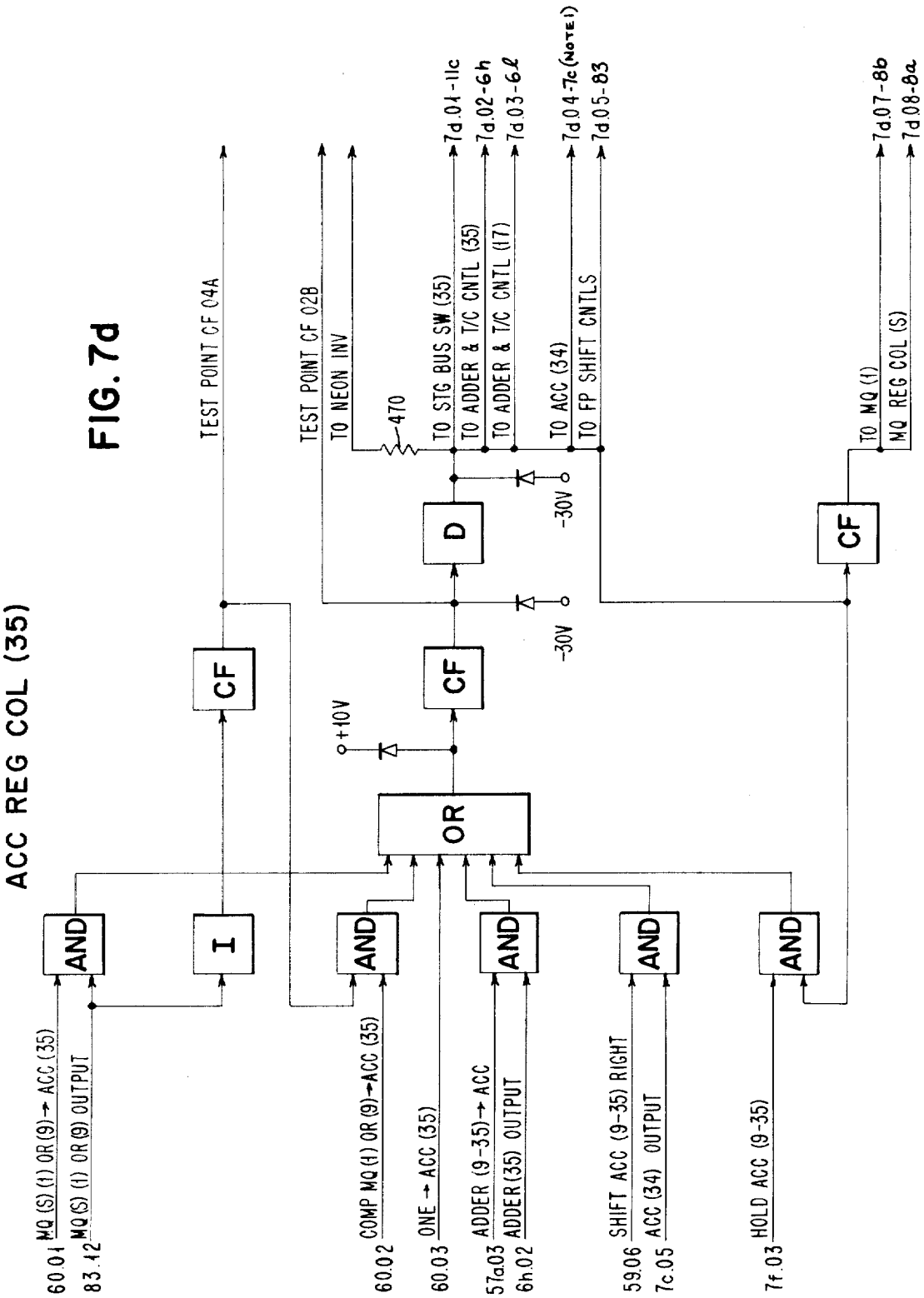

ACC REG COL (35)
60.01 MQ (S) (1) OR (9) → ACC (35)
83.12 MQ (S) (1) OR (9) OUTPUT
AND
I
CF
TEST POINT CF 04A
60.02 COMP MQ (1) OR (9) → ACC (35)
AND
60.03 ONE → ACC (35)
+10V
CF
OR
57a.03 ADDER (9-35) → ACC
6h.02 ADDER (35) OUTPUT
AND
59.06 SHIFT ACC (9-35) RIGHT
7c.05 ACC (34) OUTPUT
AND
7f.03 HOLD ACC (9-35)
AND
TEST POINT CF 02B
TO NEON INV
470
-30V
D
-30V
7d.01-11c TO STG BUS SW (35)
7d.02-6h TO ADDER & T/C CNTL (35)
7d.03-6l TO ADDER & T/C CNTL (17)
7d.04-7c (NOTE 1) TO ACC (34)
7d.05-8B TO FP SHIFT CNTLS
CF
7d.07-8b TO MQ (1)
7d.08-8a MQ REG COL (S)

FIG. 7f

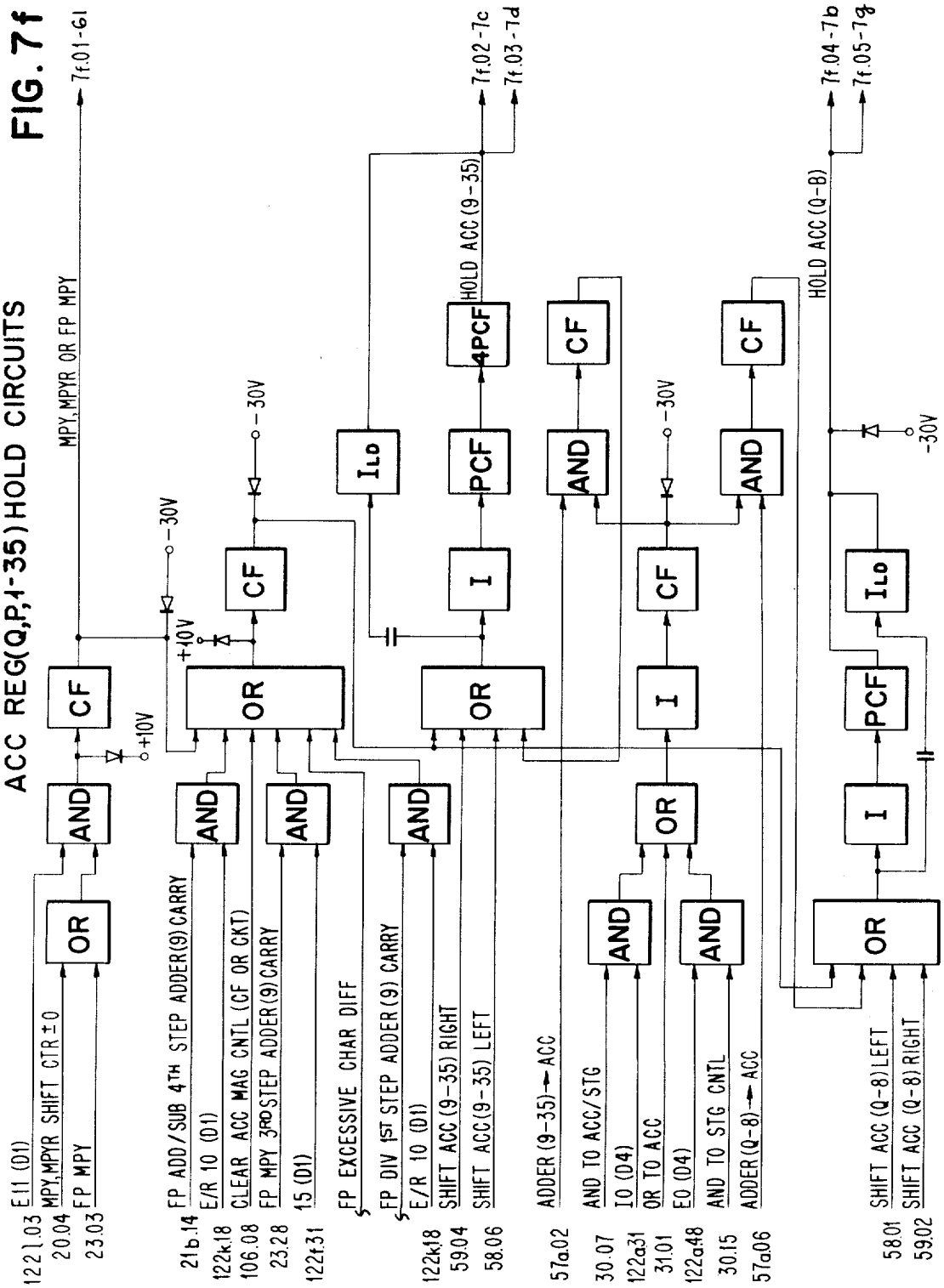

ACC REG(Q,P,1-35) HOLD CIRCUITS
MPY,MPYR OR FP MPY
7f.01-61
7f.02-7c
7f.03-7d
7f.04-7b
7f.05-7a
HOLD ACC (9-35)
HOLD ACC (Q-8)
+10V
-30V
AND
OR
CF
I
PCF
4PCF
ILO
1221.03 E11 (D1)
20.04 MPY,MPYR SHIFT CTR ± 0
23.03 FP MPY
21b.14 FP ADD/SUB 4TH STEP ADDER(9) CARRY
122k18 E/R 10 (D1)
106.08 CLEAR ACC MAG CNTL (CF OR GKT)
23.28 FP MPY 3RD STEP ADDER(9) CARRY
122f.31 15 (D1)
FP EXCESSIVE CHAR DIFF
FP DIV 1ST STEP ADDER(9) CARRY
122k18 E/R 10 (D1)
59.04 SHIFT ACC (9-35) RIGHT
58.06 SHIFT ACC(9-35) LEFT
57a.02 ADDER (9-35) → ACC
30.07 AND TO ACC/STG
122a31 IO (D4)
31.01 OR TO ACC
122a48 EO (D4)
30.15 AND TO STG CNTL
57a.06 ADDER(Q-8) → ACC
58.01 SHIFT ACC (Q-8) LEFT
59.02 SHIFT ACC (Q-8) RIGHT

FIG. 7g

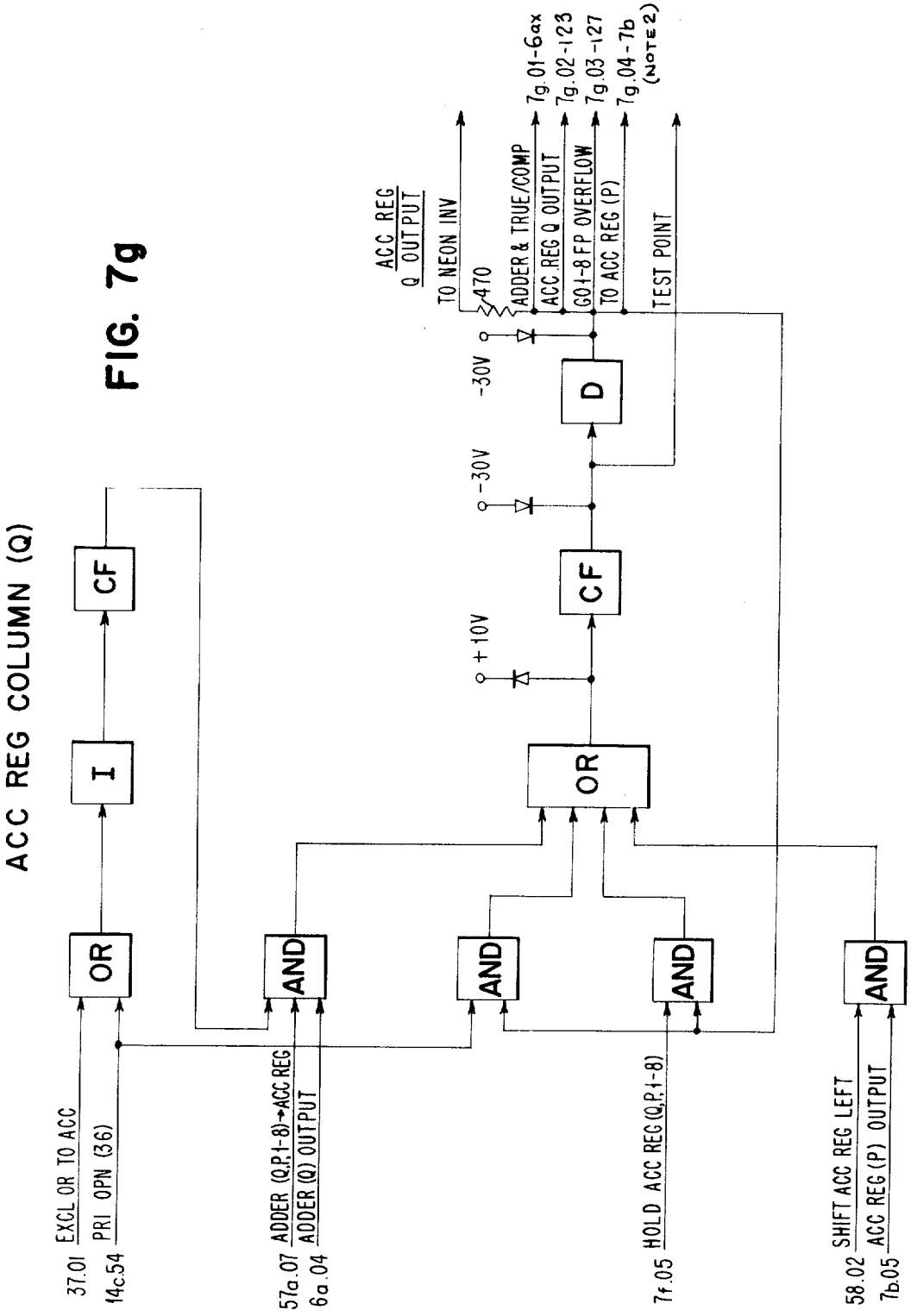

ACC REG COLUMN (Q)
37.01 EXCL OR TO ACC
14c.54 PRI OPN (36)
OR
I
CF
57a.07 ADDER (Q,P,1-8)→ACC REG
6a.04 ADDER (Q) OUTPUT
AND
AND
AND
AND
OR
+10V
-30V
CF
-30V
D
-30V
7f.05 HOLD ACC REG (Q,P,1-8)
58.02 SHIFT ACC REG LEFT
7b.05 ACC REG (P) OUTPUT
ACC REG Q OUTPUT
TO NEON INV
470
ADDER & TRUE/COMP
ACC.REG Q OUTPUT
G01-8 FP OVERFLOW
TO ACC REG (P)
TEST POINT
7g.01-6ax
7g.02-123
7g.03-127
7g.04-7b (NOTE 2)

FIG. 8a

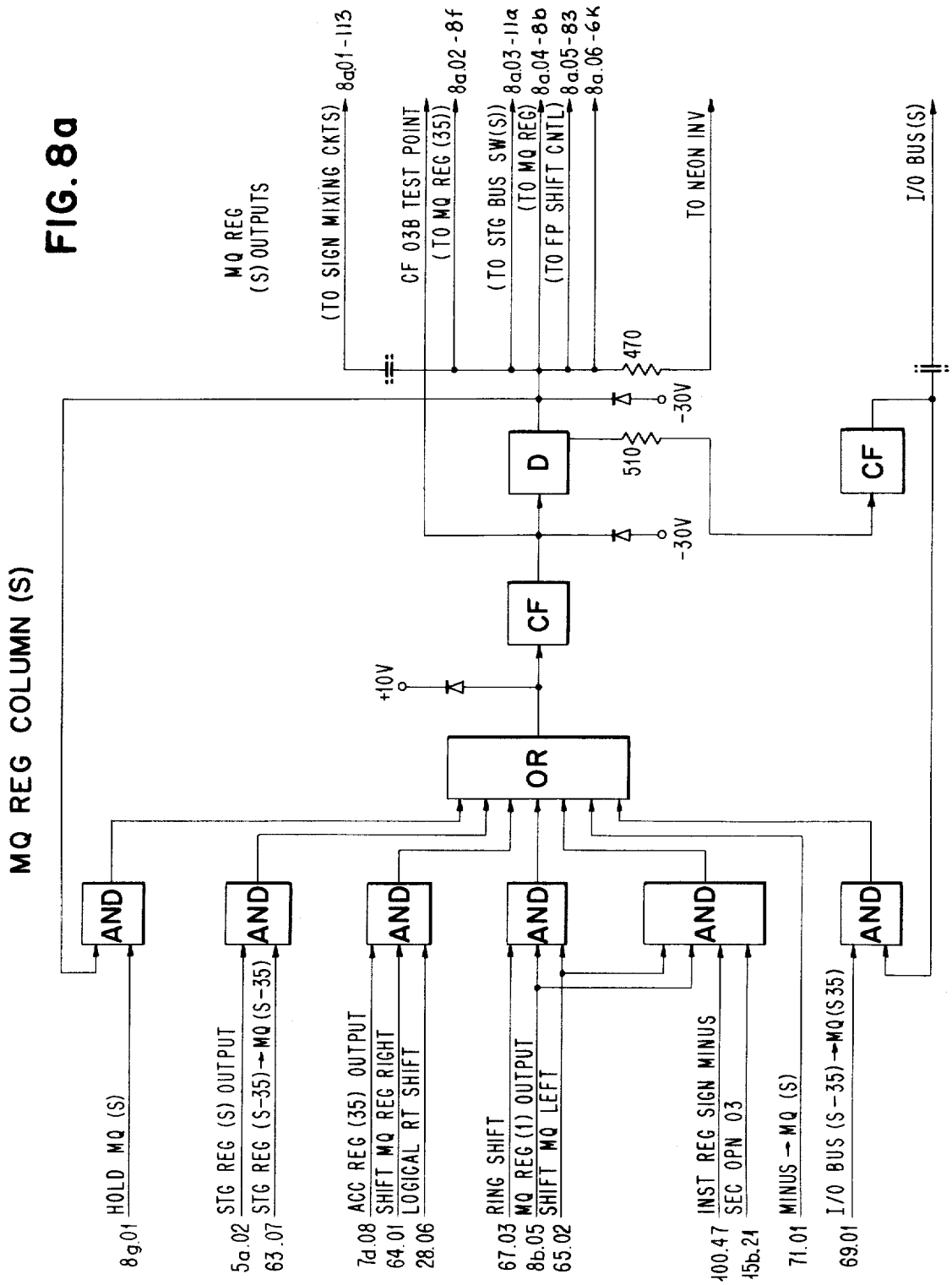
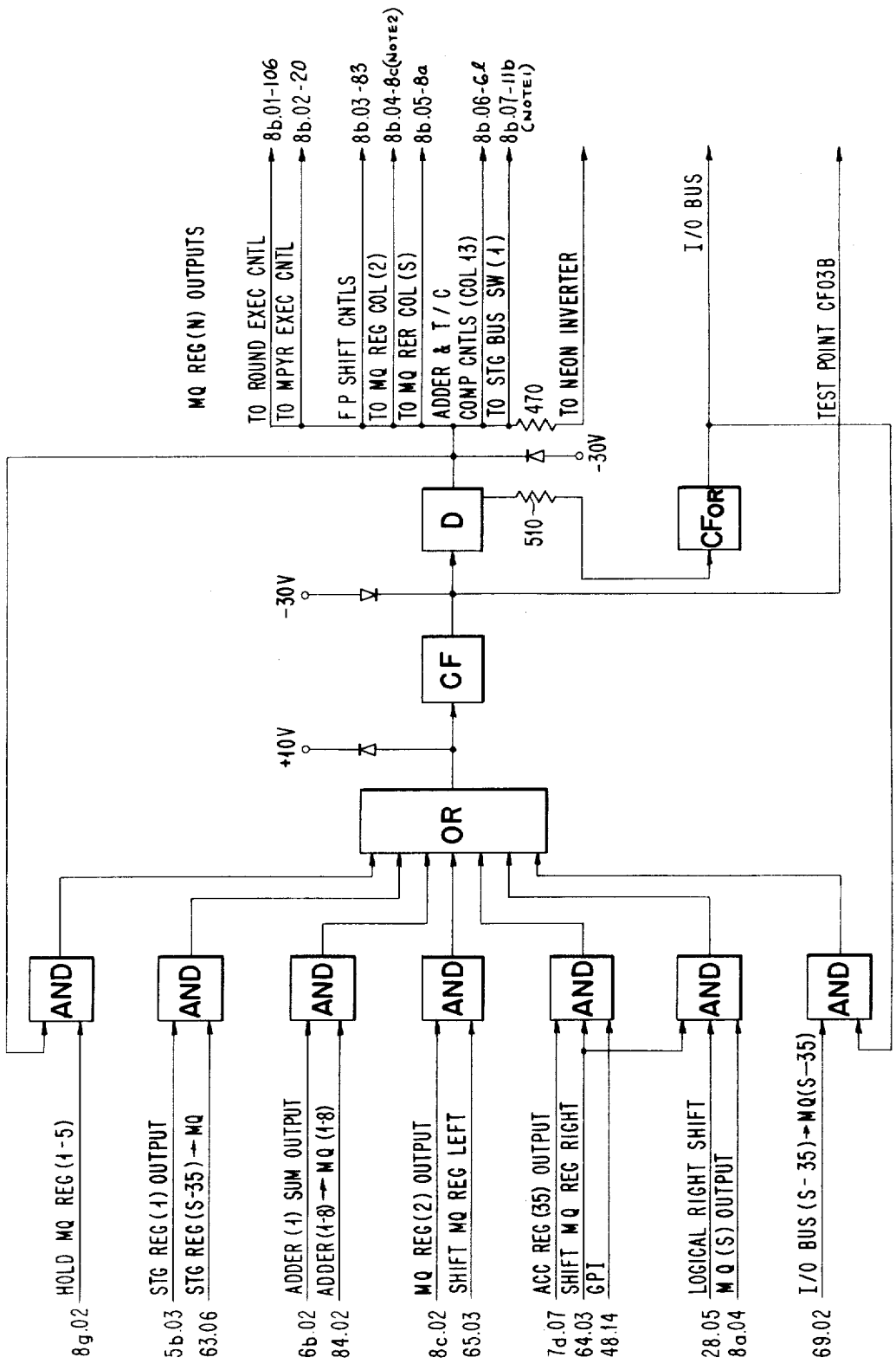

MQ REG COLUMN (S)
MQ REG (S) OUTPUTS
(TO SIGN MIXING CKTS) 8a.01-113
CF 03B TEST POINT (TO MQ REG (35)) 8a.02-8f
(TO STG BUS SW(S)) 8a.03-11a
(TO MQ REG) 8a.04-8b
(TO FP SHIFT CNTL) 8a.05-83
8a.06-6K
TO NEON INV
I/O BUS(S)
470
-30V
D
510
-30V
CF
CF
+10V
OR
AND
AND
AND
AND
AND
AND
8g.01 HOLD MQ (S)
5a.02 STG REG (S) OUTPUT
63.07 STG REG (S-35)→MQ (S-35)
7d.08 ACC REG (35) OUTPUT
64.01 SHIFT MQ REG RIGHT
28.06 LOGICAL RT SHIFT
67.03 RING SHIFT
8b.05 MQ REG (1) OUTPUT
65.02 SHIFT MQ LEFT
100.47 INST REG SIGN MINUS
15b.24 SEC OPN 03
71.01 MINUS→MQ (S)
69.01 I/O BUS (S-35)→MQ(S35)

FIG. 8b


MQ REG COLUMN (1)
MQ REG(N) OUTPUTS
TO ROUND EXEC CNTL
TO MPYR EXEC CNTL
F P SHIFT CNTLS
TO MQ REG COL(2)
TO MQ RER COL(S)
ADDER & T/C COMP CNTLS (COL 13)
TO STG BUS SW(1)
470
TO NEON INVERTER
8b.01-106
8b.02-20
8b.03-83
8b.04-8c(NOTE2)
8b.05-8a
8b.06-6L
8b.07-11b (NOTE1)
-30V
510
D
CF
OR
AND
+10V
-30V
I/O BUS
TEST POINT CF03B
HOLD MQ REG(1-5)
8g.02
STG REG(1) OUTPUT
STG REG(S-35)→MQ
5b.03
63.06
ADDER(1) SUM OUTPUT
ADDER(1-8)→MQ(1-8)
6b.02
84.02
MQ REG(2) OUTPUT
SHIFT MQ REG LEFT
8c.02
65.03
ACC REG(35) OUTPUT
SHIFT MQ REG RIGHT
GPI
7d.07
64.03
48.14
LOGICAL RIGHT SHIFT
MQ(S) OUTPUT
28.05
8a.04
I/O BUS(S-35)→MQ(S-35)
69.02

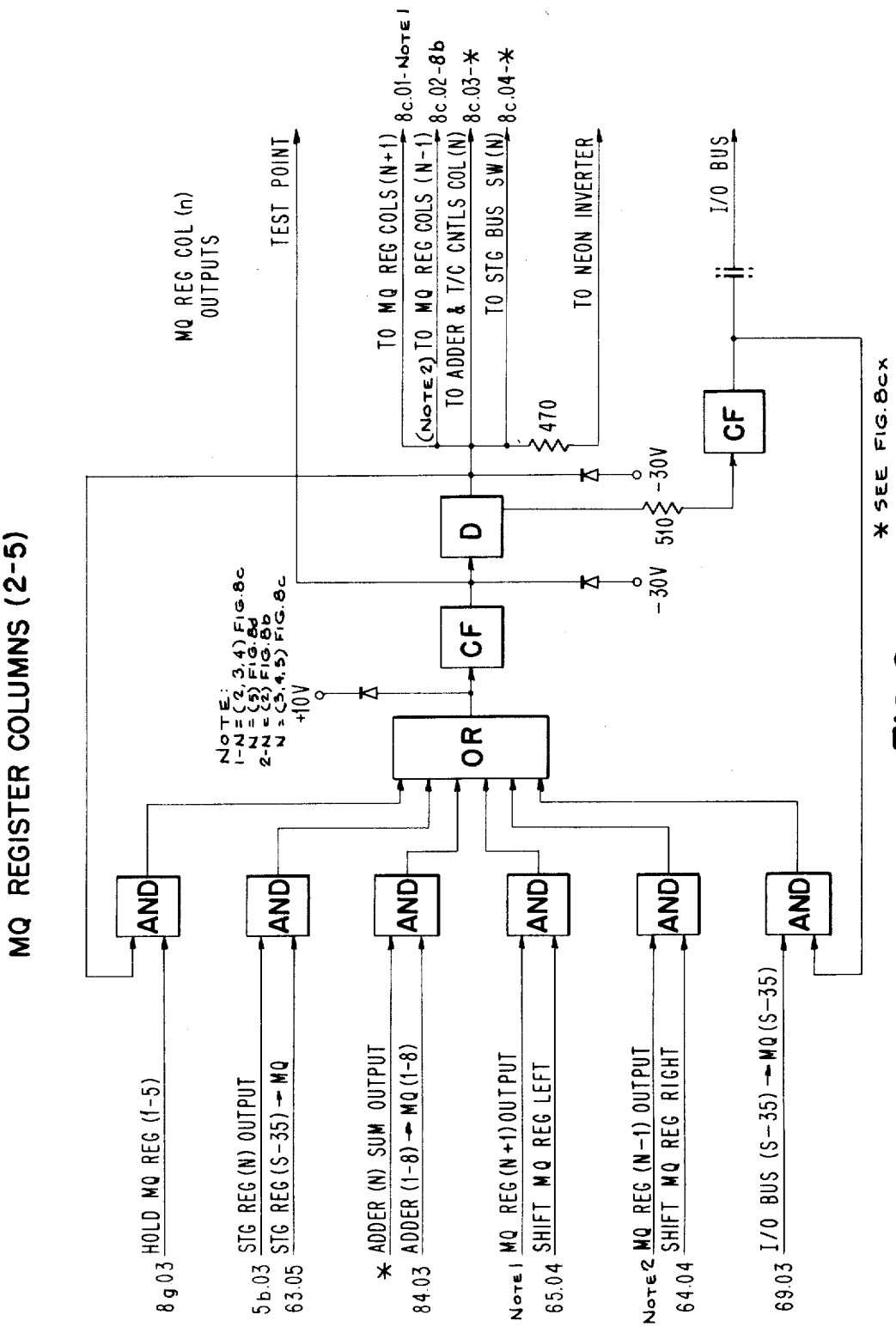
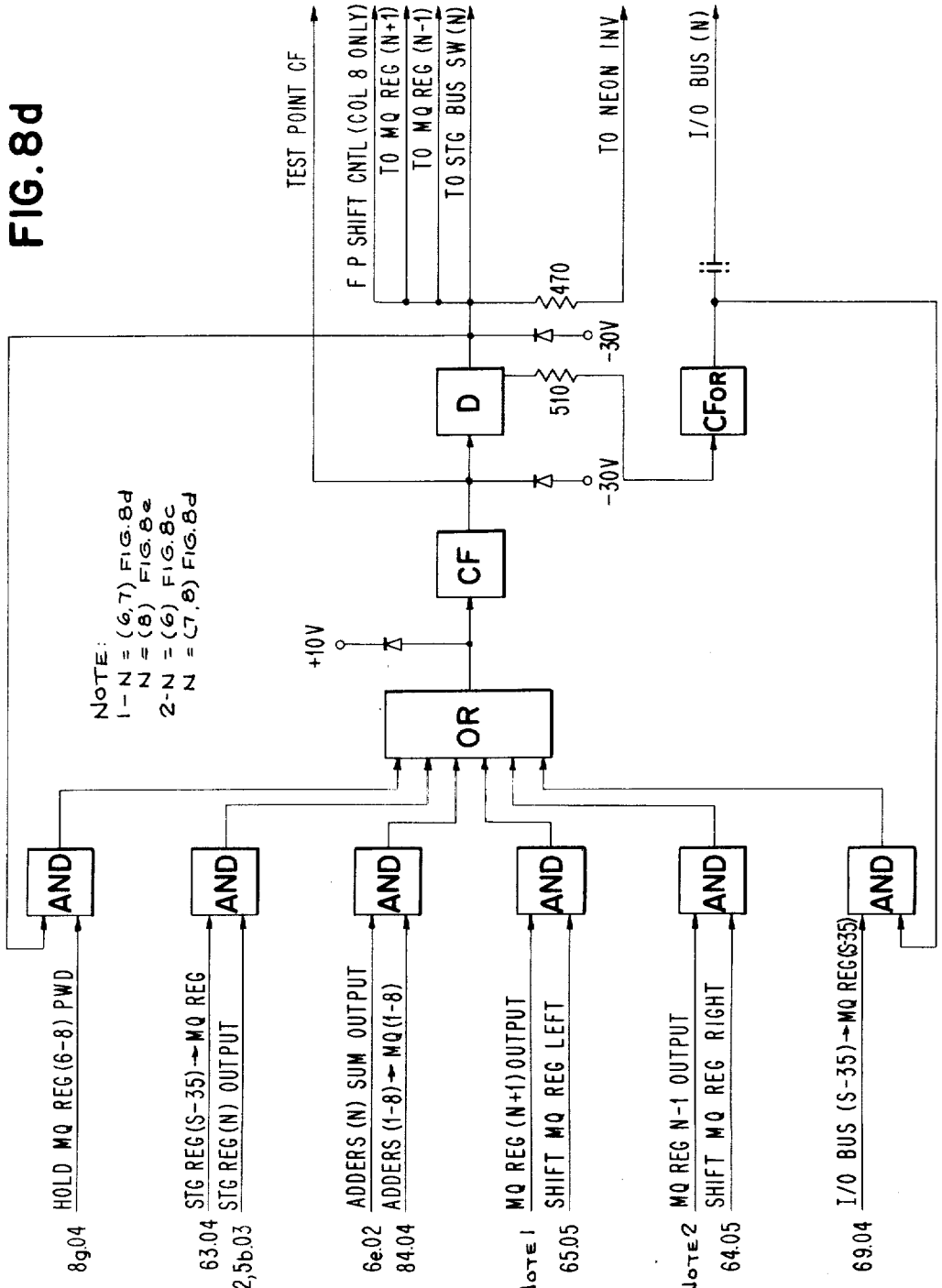

MQ REGISTER COLUMNS (2-5)
MQ REG COL (n) OUTPUTS
TEST POINT
TO MQ REG COLS (N+1) 8c.01-NOTE 1
(NOTE 2) TO MQ REG COLS (N-1) 8c.02-8b
TO ADDER & T/C CNTLS COL (N) 8c.03-*
TO STG BUS SW (N) 8c.04-*
TO NEON INVERTER
I/O BUS
470
-30V
510
-30V
+10V
NOTE:
1-N = (2, 3, 4) FIG. 8c
N = (5) FIG. 8d
2-N = (2) FIG. 8b
N = (3, 4, 5) FIG. 8c
D
CF
OR
CF
AND
AND
AND
AND
AND
AND
8g.03 HOLD MQ REG (1-5)
5b.03 STG REG (N) OUTPUT
63.05 STG REG (S-35) → MQ
* ADDER (N) SUM OUTPUT
84.03 ADDER (1-8) → MQ (1-8)
NOTE 1 MQ REG (N+1) OUTPUT
65.04 SHIFT MQ REG LEFT
NOTE 2 MQ REG (N-1) OUTPUT
64.04 SHIFT MQ REG RIGHT
69.03 I/O BUS (S-35) → MQ (S-35)
* SEE FIG. 8cx

FIG. 8c

FIG.8d

MQ REG COL 6-8



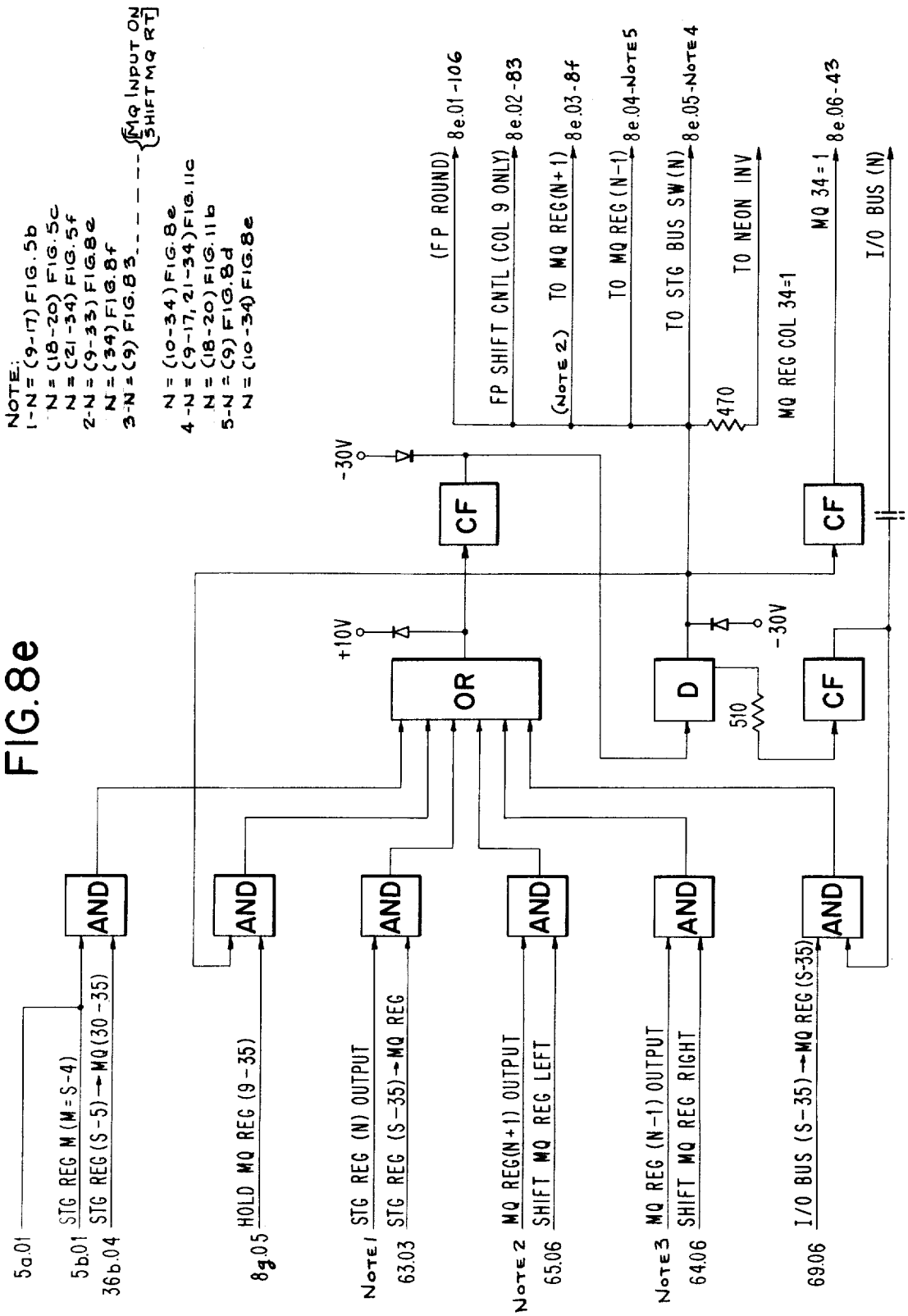

NOTE:
1-N = (9-17) FIG. 5b
N = (18-20) FIG. 5c
N = (21-34) FIG. 5f
2-N = (9-33) FIG. 8a
N = (34) FIG. 8f
3-N = (9) FIG. 83
N = (10-34) FIG. 8e
4-N = (9-17, 21-34) FIG. 11c
N = (18-20) FIG. 11b
5-N = (9) FIG. 8d
N = (10-34) FIG. 8e
MQ INPUT ON SHIFT MQ RT
(FP ROUND) 8e.01-106
FP SHIFT CNTL (COL 9 ONLY) 8e.02-83
(NOTE 2) TO MQ REG(N+1) 8e.03-8f
TO MQ REG (N-1) 8e.04-NOTE 5
TO STG BUS SW (N) 8e.05-NOTE 4
TO NEON INV
MQ REG COL 34=1
MQ 34=1 8e.06-43
I/O BUS (N)
-30V
+10V
CF
OR
D
AND
470
510
5a.01
5b.01 STG REG M (M=S-4)
36b.04 STG REG (S-5)→MQ (30-35)
8g.05 HOLD MQ REG (9-35)
NOTE 1 STG REG (N) OUTPUT
63.03 STG REG (S-35)→MQ REG
NOTE 2 MQ REG(N+1) OUTPUT
65.06 SHIFT MQ REG LEFT
NOTE 3 MQ REG (N-1) OUTPUT
64.06 SHIFT MQ REG RIGHT
69.06 I/O BUS (S-35)→MQ REG (S-35)

FIG. 8e

FIG. 8f

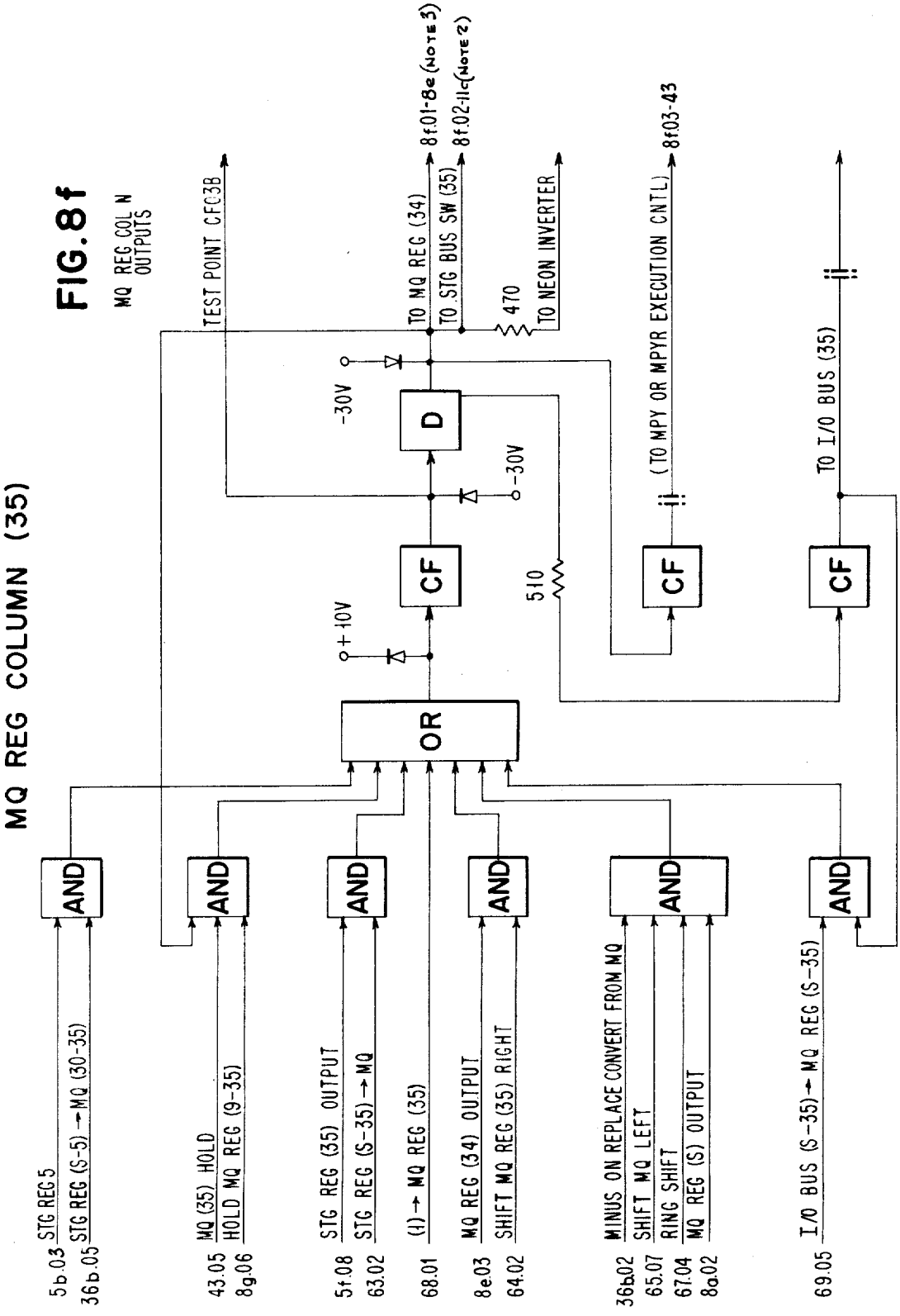
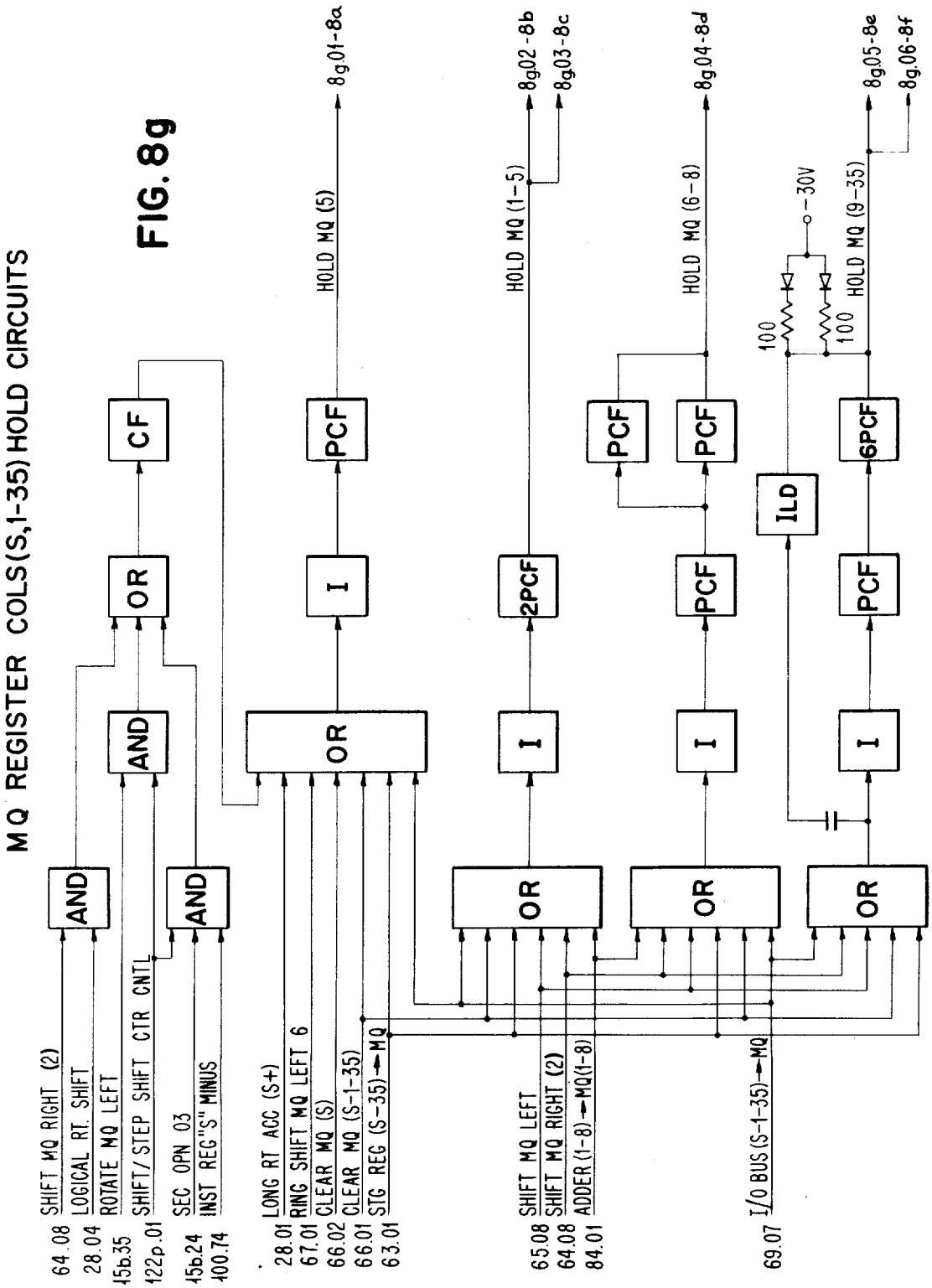

MQ REG COLUMN (35)
MQ REG COL N OUTPUTS
TEST POINT CFC3B
TO MQ REG (34)
8f.01-8e (NOTE 3)
TO STG BUS SW (35)
8f.02-11c (NOTE 2)
470
TO NEON INVERTER
-30V
D
-30V
+10V
CF
510
CF
(TO MPY OR MPYR EXECUTION CNTL)
8f.03-43
CF
TO I/O BUS (35)
OR
AND
5b.03 STG REC 5
36b.05 STG REG (S-5) → MQ (30-35)
AND
43.05 MQ (35) HOLD
8g.06 HOLD MQ REG (9-35)
AND
5f.08 STG REG (35) OUTPUT
63.02 STG REG (S-35) → MQ
68.01 (1) → MQ REG (35)
AND
8e.03 MQ REG (34) OUTPUT
64.02 SHIFT MQ REG (35) RIGHT
AND
36b.02 MINUS ON REPLACE CONVERT FROM MQ
65.07 SHIFT MQ LEFT
67.04 RING SHIFT
8a.02 MQ REG (S) OUTPUT
AND
69.05 I/O BUS (S-35) → MQ REG (S-35)

FIG. 8g


MQ REGISTER COLS(S,1-35) HOLD CIRCUITS
64.08 SHIFT MQ RIGHT (2)
28.04 LOGICAL RT. SHIFT
15b.35 ROTATE MQ LEFT
122p.01 SHIFT/STEP SHIFT CTR CNTL
15b.24 SEC OPN 03
400.74 INST REG"S" MINUS
28.01 LONG RT ACC (S+)
67.01 RING SHIFT MQ LEFT 6
66.02 CLEAR MQ (S)
66.01 CLEAR MQ (S-1-35)
63.01 STG REG (S-35)→MQ
65.08 SHIFT MQ LEFT
64.08 SHIFT MQ RIGHT (2)
84.01 ADDER (1-8)→MQ(1-8)
69.07 I/O BUS (S-1-35)→MQ
AND
AND
AND
OR
OR
OR
OR
CF
I
I
I
I
PCF
2PCF
PCF
PCF
ILD
6PCF
HOLD MQ (5)
HOLD MQ (1-5)
HOLD MQ (6-8)
HOLD MQ (9-35)
8g.01-8a
8g.02-8b
8g.03-8c
8g.04-8d
8g.05-8e
8g.06-8f
100
100
-30V

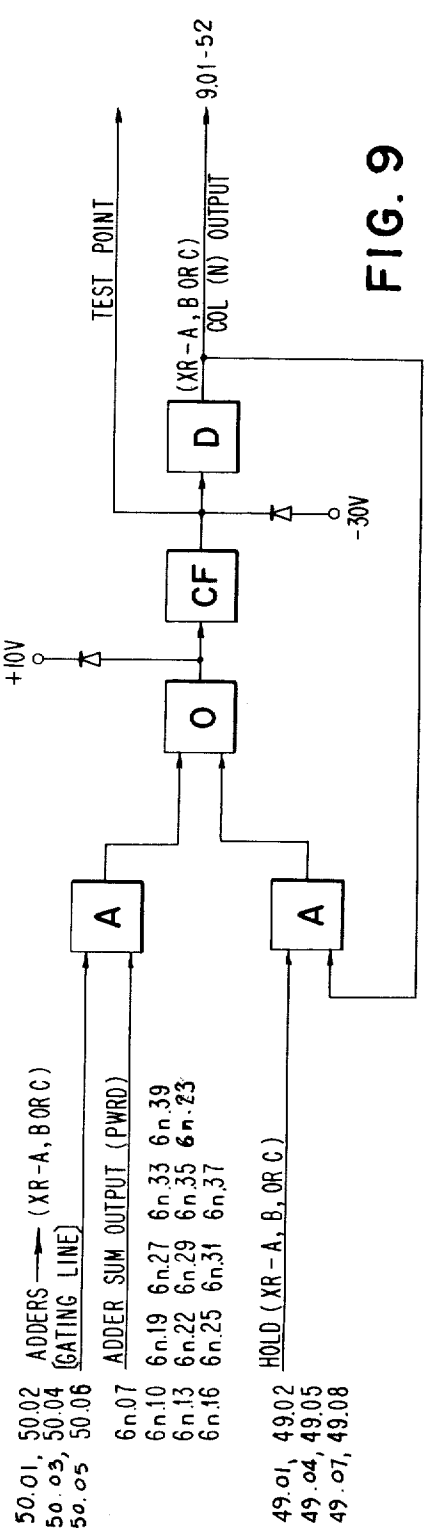

INDEX REGISTER (3-17) A, B or C
50.01, 50.02
50.03, 50.04
50.05 50.06
ADDERS → (XR-A, B OR C)
GATING LINE
ADDER SUM OUTPUT (PWRD)
6n.07 6n.19 6n.27 6n.33 6n.39
6n.10 6n.22 6n.29 6n.35 6n.23
6n.13 6n.25 6n.31 6n.37
6n.16
HOLD (XR-A, B, OR C)
49.01, 49.02
49.04, 49.05
49.07, 49.08
A
O
CF
D
+10V
-30V
TEST POINT
(XR-A, B OR C) COL (N) OUTPUT
9.01-52

FIG. 9

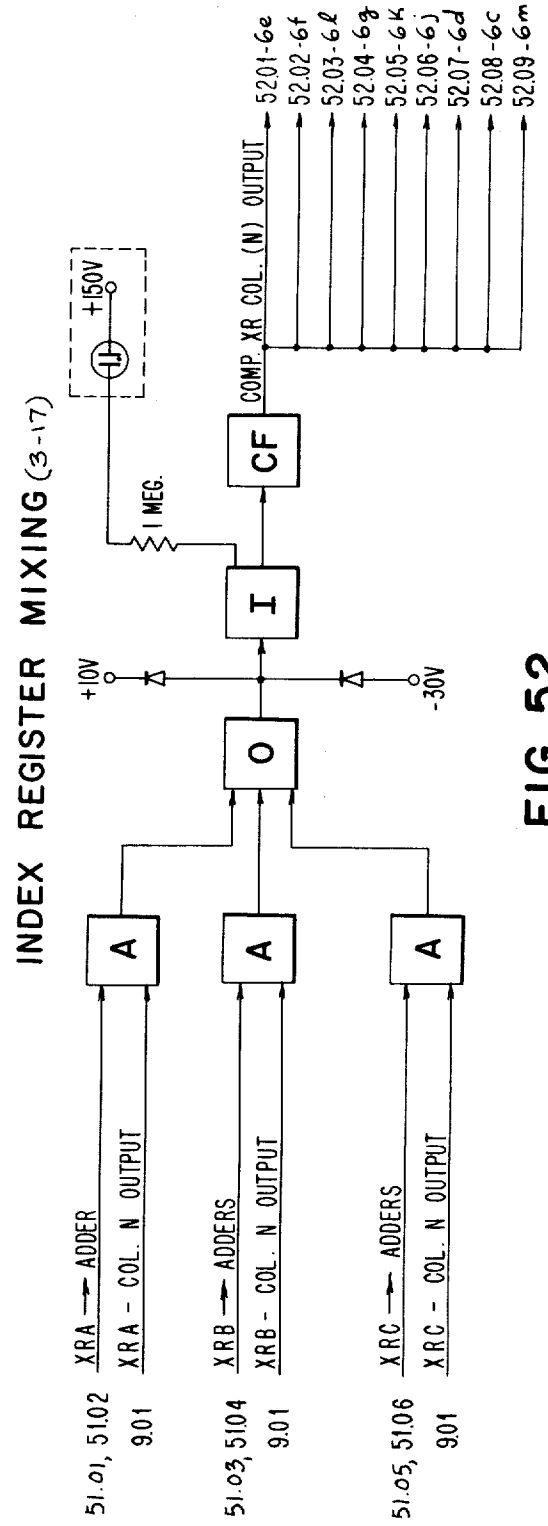

INDEX REGISTER MIXING (3-17)
51.01, 51.02
9.01
XRA → ADDER
XRA - COL. N OUTPUT
51.03, 51.04
9.01
XRB → ADDERS
XRB - COL. N OUTPUT
51.05, 51.06
9.01
XRC → ADDERS
XRC - COL. N OUTPUT
A
O
I
CF
+10V
-30V
+150V
1 MEG.
COMP. XR COL. (N) OUTPUT
52.01-6e
52.02-6f
52.03-6l
52.04-6g
52.05-6k
52.06-6j
52.07-6d
52.08-6c
52.09-6m

FIG. 52

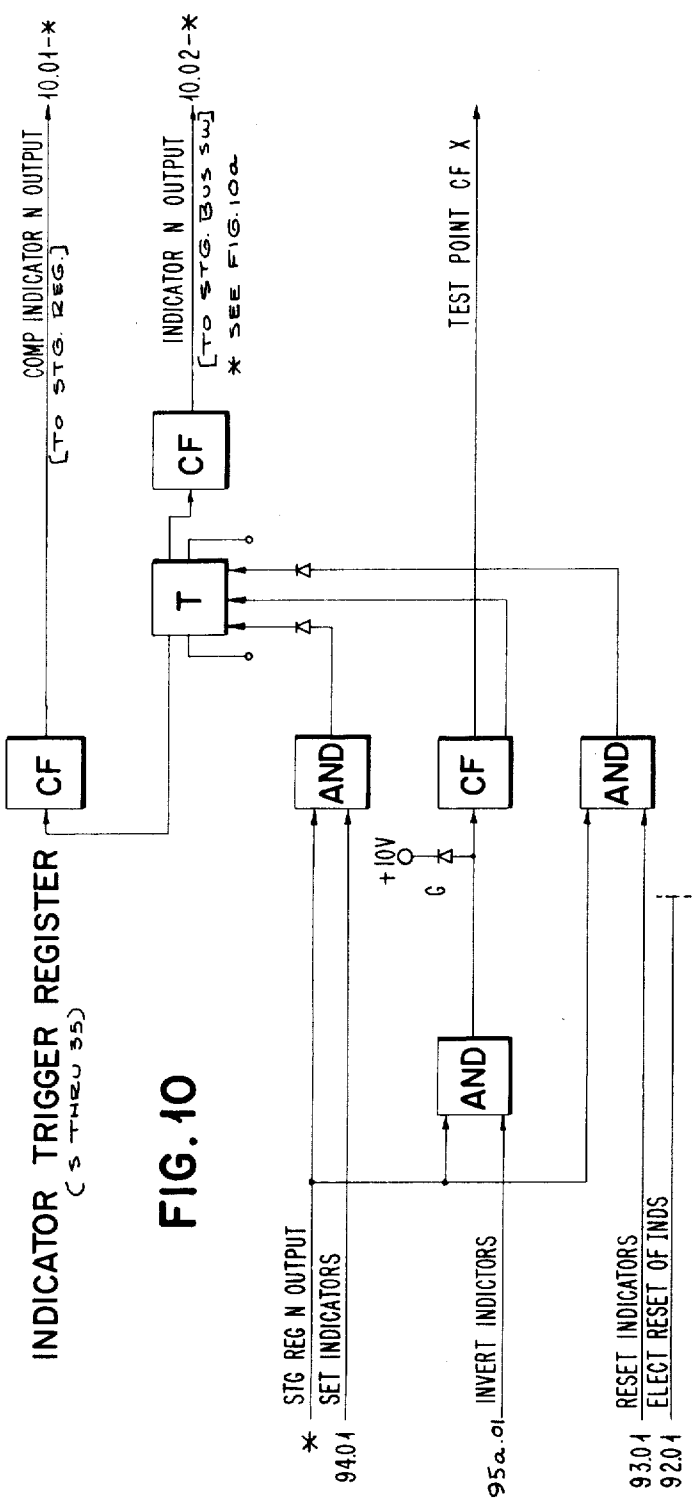

INDICATOR TRIGGER REGISTER
(5 THRU 35)
CF
COMP INDICATOR N OUTPUT
10.01-*
[TO STG. REG.]
T
CF
INDICATOR N OUTPUT
10.02-*
[TO STG. BUS SW]
* SEE FIG. 10a
TEST POINT CF X
AND
CF
AND
+10V
G
AND
* STG REG N OUTPUT
94.04 SET INDICATORS
95a.01 INVERT INDICTORS
93.04 RESET INDICATORS
92.04 ELECT RESET OF INDS

FIG. 10

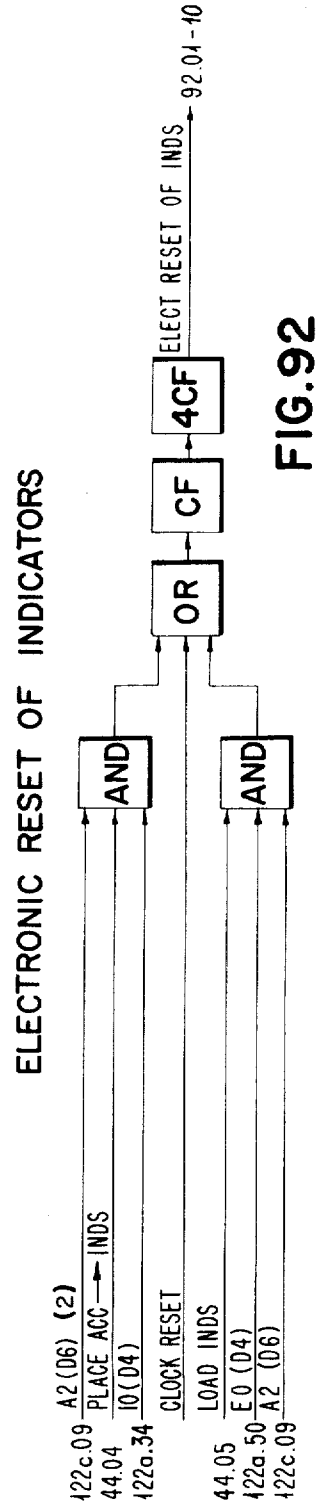
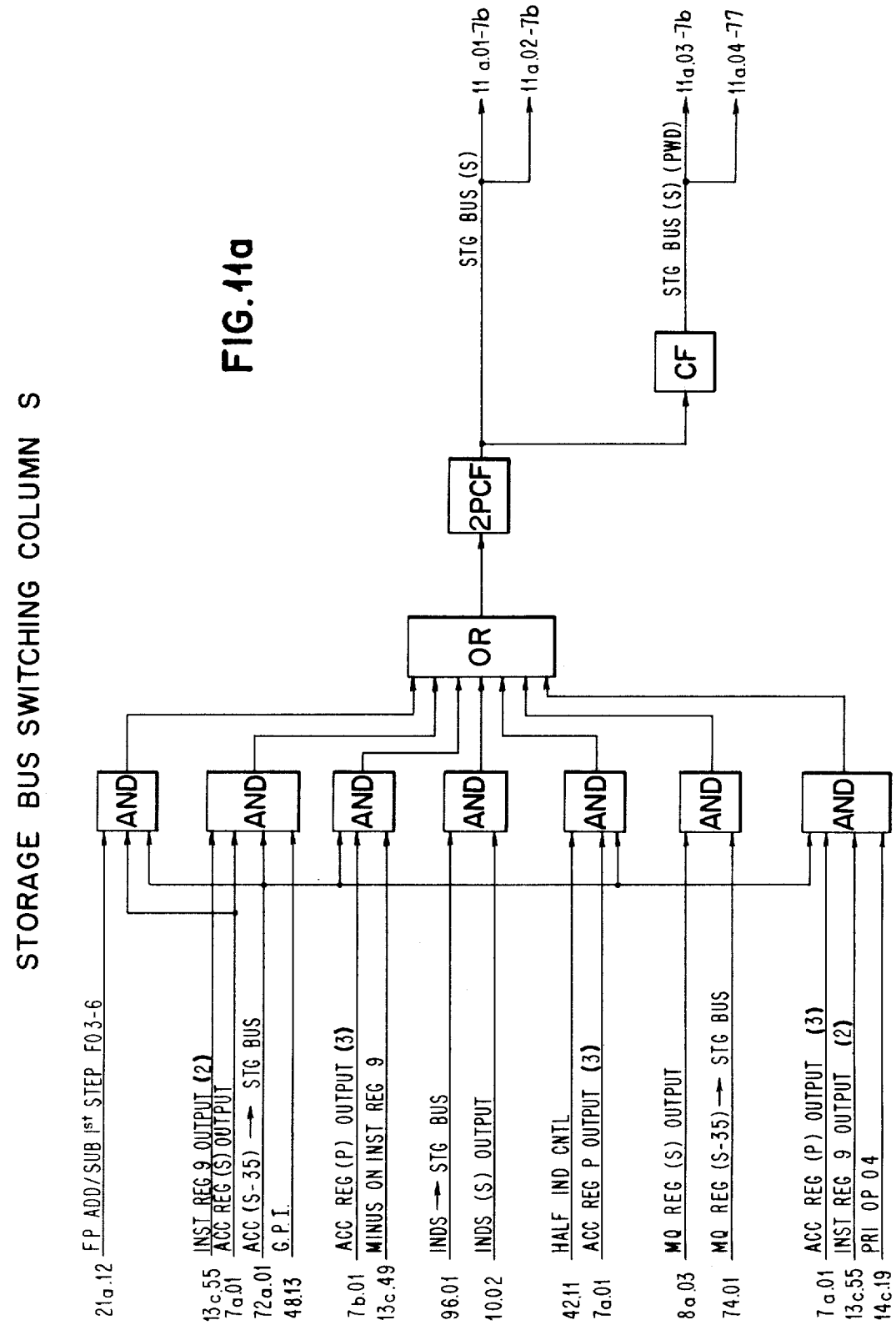

ELECTRONIC RESET OF INDICATORS
AND
AND
AND
OR
CF
4CF
ELECT RESET OF INDS
92.04-10
122c.09 A2 (D6) (2)
44.04 PLACE ACC → INDS
122a.34 10 (04)
CLOCK RESET
44.05 LOAD INDS
122a.50 E0 (04)
122c.09 A2 (D6)

FIG. 92

FIG. 11a


STORAGE BUS SWITCHING COLUMN S
21a.12 F.P. ADD/SUB 1st STEP F03-6
13c.55 INST REG 9 OUTPUT (2)
7a.01 ACC REG (S) OUTPUT
72a.01 ACC (S-35) → STG BUS
48.13 G.P.I.
7b.01 ACC REG (P) OUTPUT (3)
13c.49 MINUS ON INST REG 9
96.01 INDS → STG BUS
10.02 INDS (S) OUTPUT
42.11 HALF IND CNTL
7a.01 ACC REG P OUTPUT (3)
8a.03 MQ REG (S) OUTPUT
74.01 MQ REG (S-35) → STG BUS
7a.01 ACC REG (P) OUTPUT (3)
13c.55 INST REG 9 OUTPUT (2)
14c.19 PRI OP 04
AND
OR
2PCF
CF
STG BUS (S)
11a.01-7b
11a.02-7b
STG BUS (S) (PWD)
11a.03-7b
11a.04-77

STORAGE BUS SWITCHING COLUMNS (1,2,18,19,20)

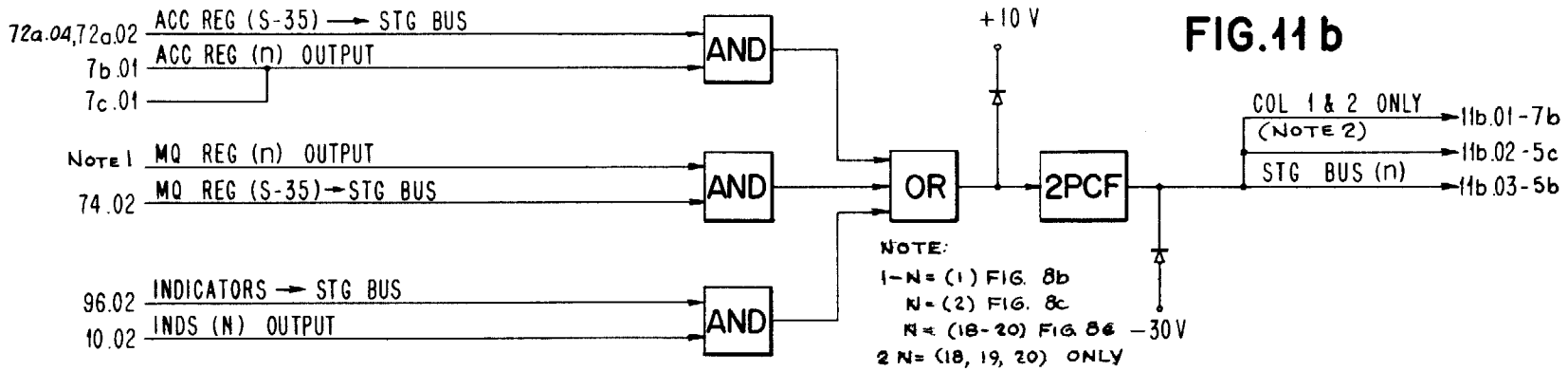


FIG. 11b

STORAGE BUS SWITCHING COLUMNS (21-35),(3-17)

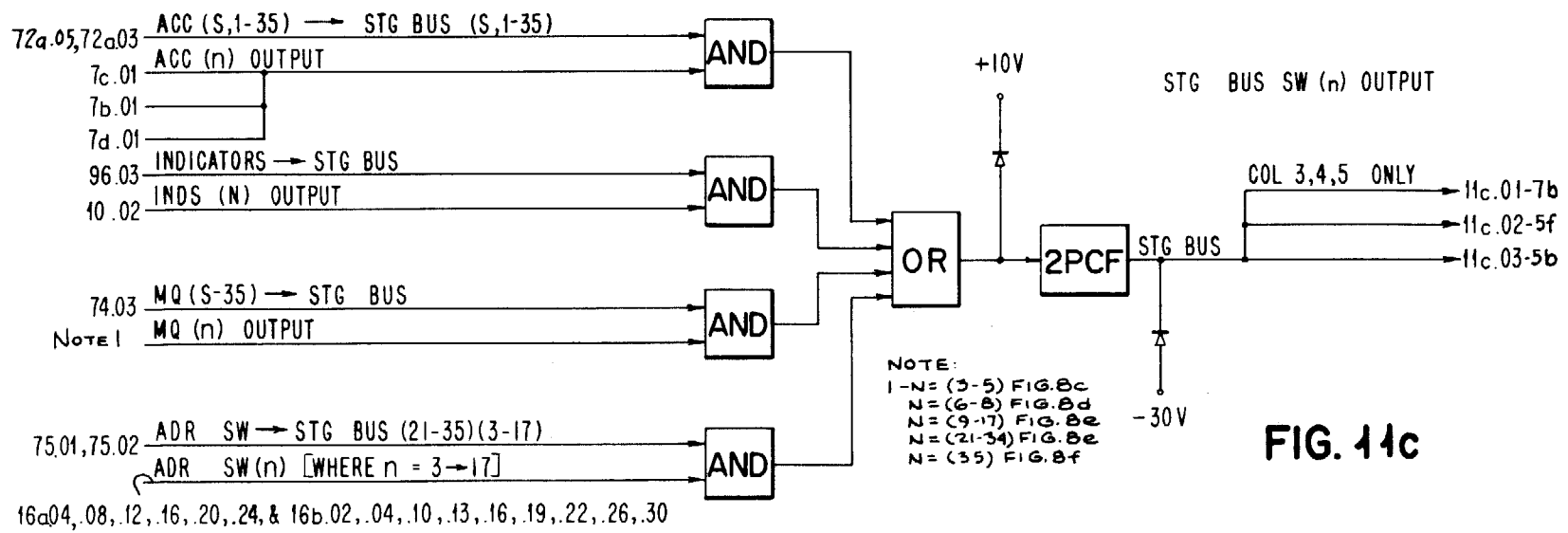


FIG. 11c

FIG. 12

OPERATORS PANEL ENTRY KEYS (S THRU 35)

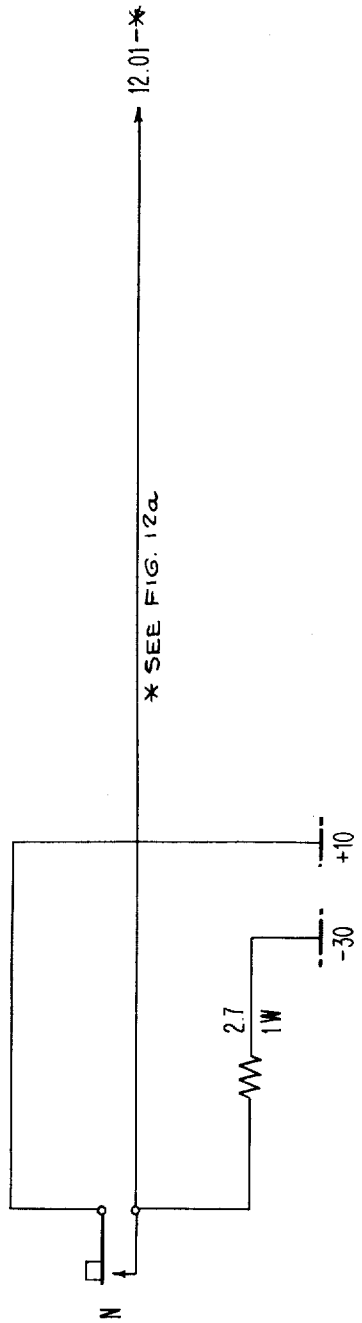


FIG. 126b

DIVIDE CHECK TRIGGER

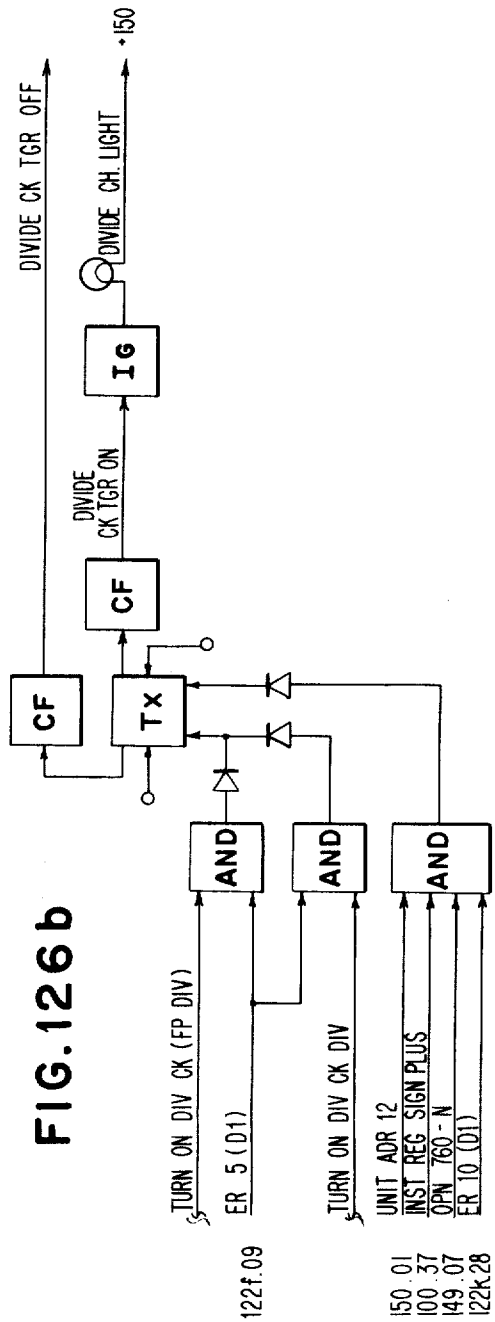
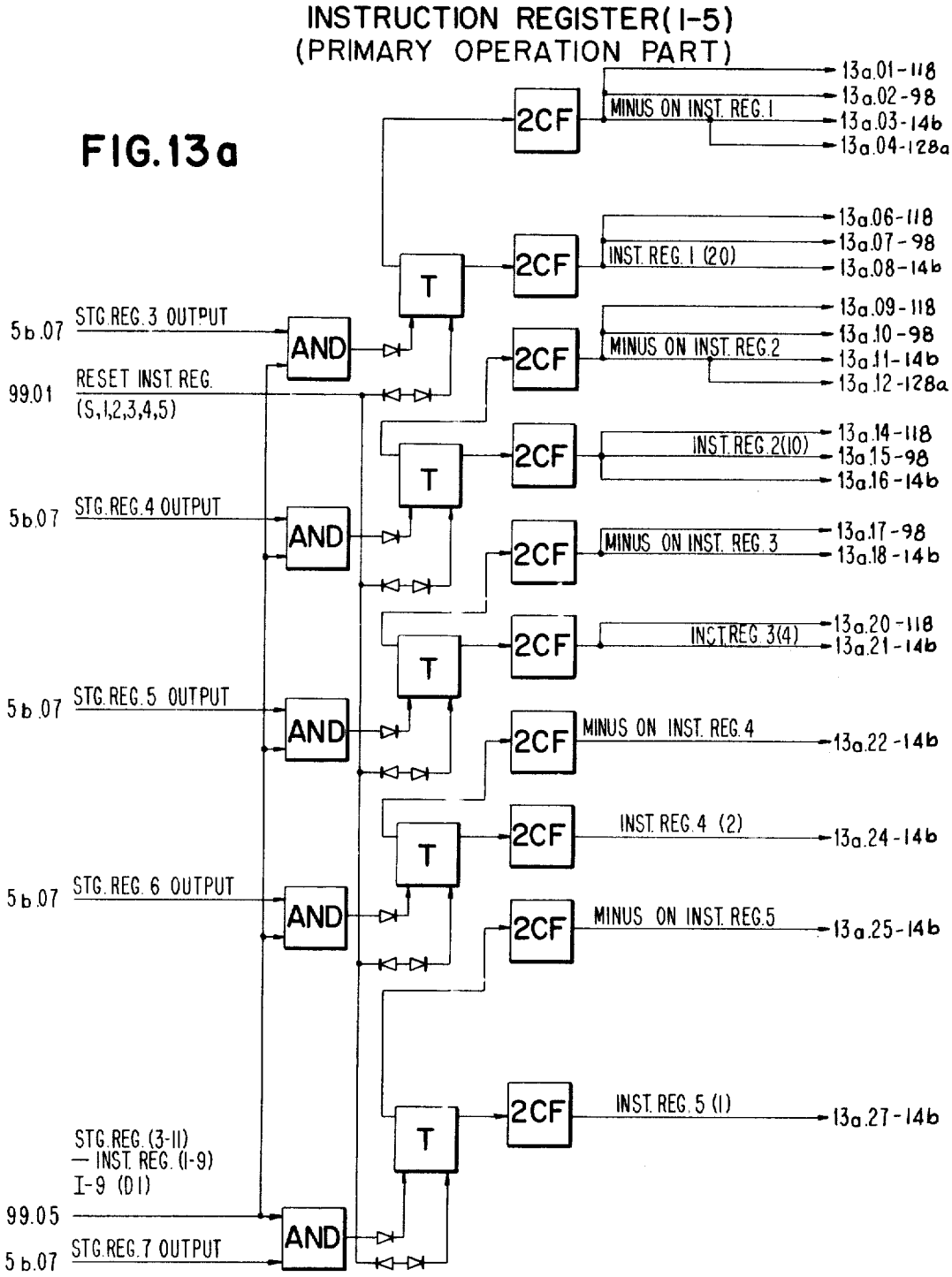


FIG. 13a


INSTRUCTION REGISTER(I-5)
(PRIMARY OPERATION PART)
2CF
MINUS ON INST. REG.1
13a.01-118
13a.02-98
13a.03-14b
13a.04-128a
T
2CF
INST. REG. 1 (20)
13a.06-118
13a.07-98
13a.08-14b
5b.07 STG.REG.3 OUTPUT
AND
99.01 RESET INST. REG. (S,1,2,3,4,5)
2CF
MINUS ON INST. REG.2
13a.09-118
13a.10-98
13a.11-14b
13a.12-128a
T
2CF
INST. REG.2(10)
13a.14-118
13a.15-98
13a.16-14b
5b.07 STG.REG.4 OUTPUT
AND
2CF
MINUS ON INST. REG. 3
13a.17-98
13a.18-14b
T
2CF
INST.REG. 3(4)
13a.20-118
13a.21-14b
5b.07 STG.REG.5 OUTPUT
AND
2CF
MINUS ON INST. REG. 4
13a.22-14b
T
2CF
INST. REG. 4 (2)
13a.24-14b
5b.07 STG. REG. 6 OUTPUT
AND
2CF
MINUS ON INST. REG.5
13a.25-14b
T
2CF
INST. REG. 5 (1)
13a.27-14b
STG.REG.(3-11) — INST. REG.(1-9) I-9 (D1)
99.05
5b.07 STG.REG.7 OUTPUT
AND

INSTRUCTION REGISTER (6-7)

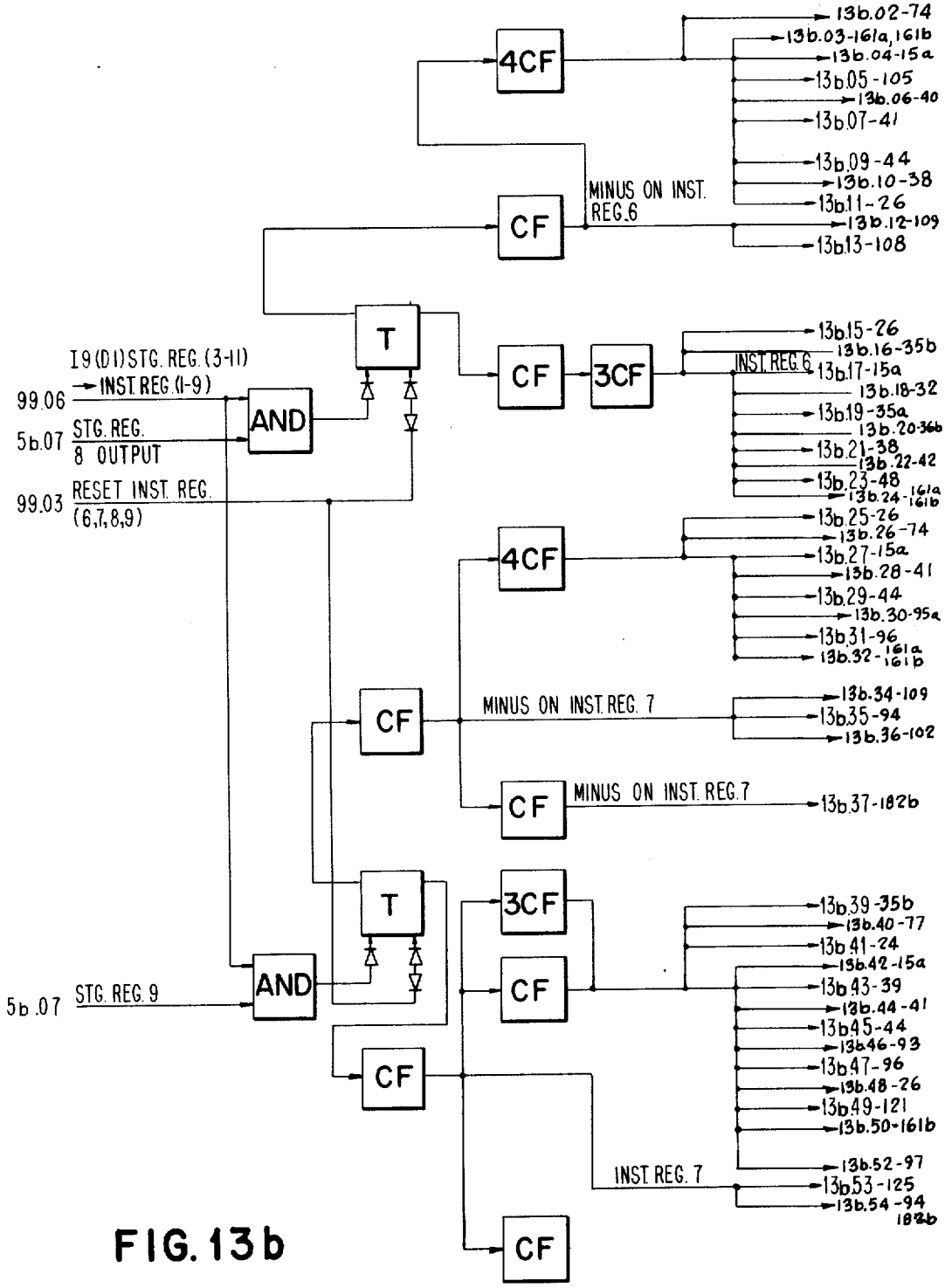


FIG. 13b

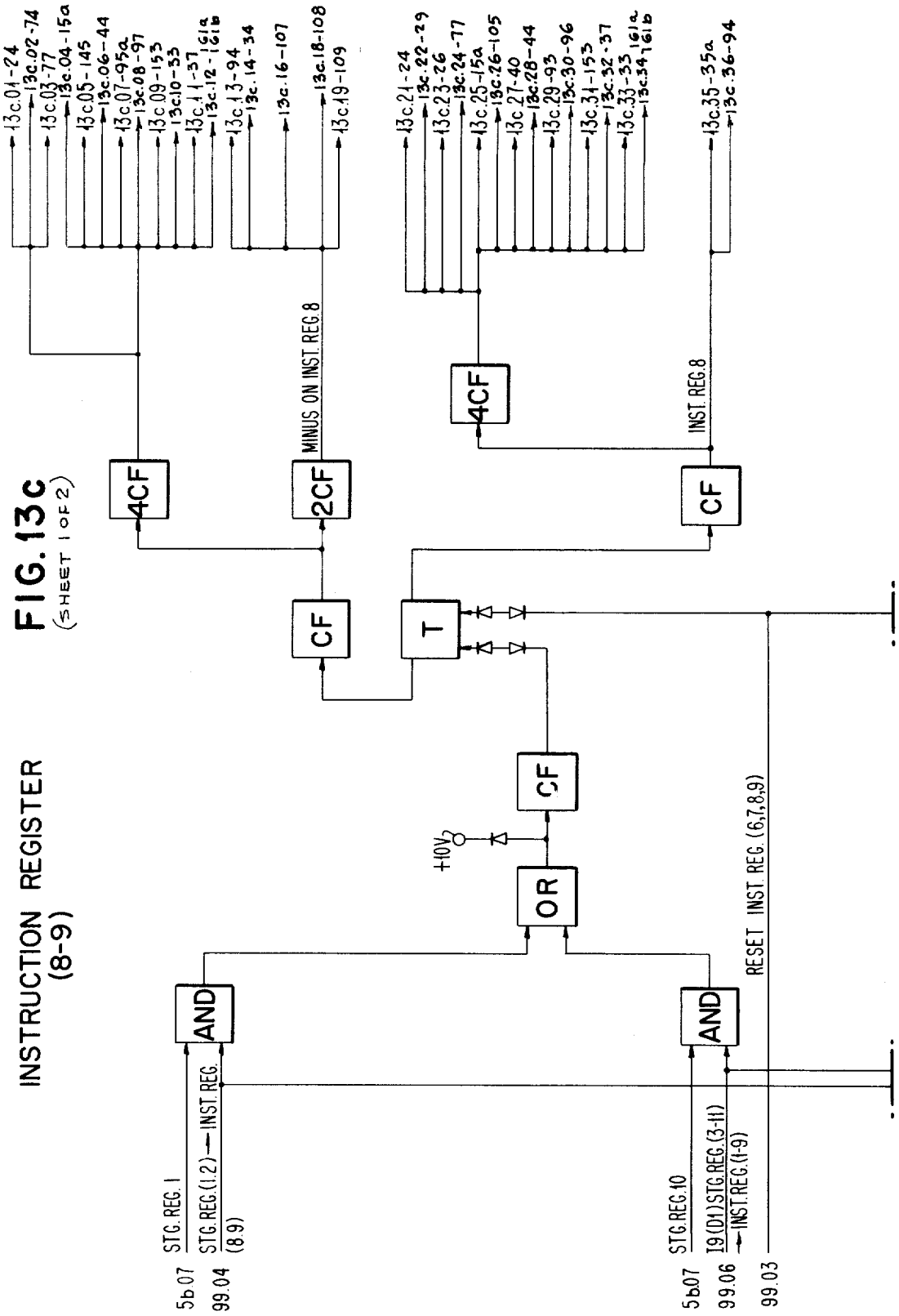


FIG. 13c
(SHEET 1 OF 2)

INSTRUCTION REGISTER
(8-9)

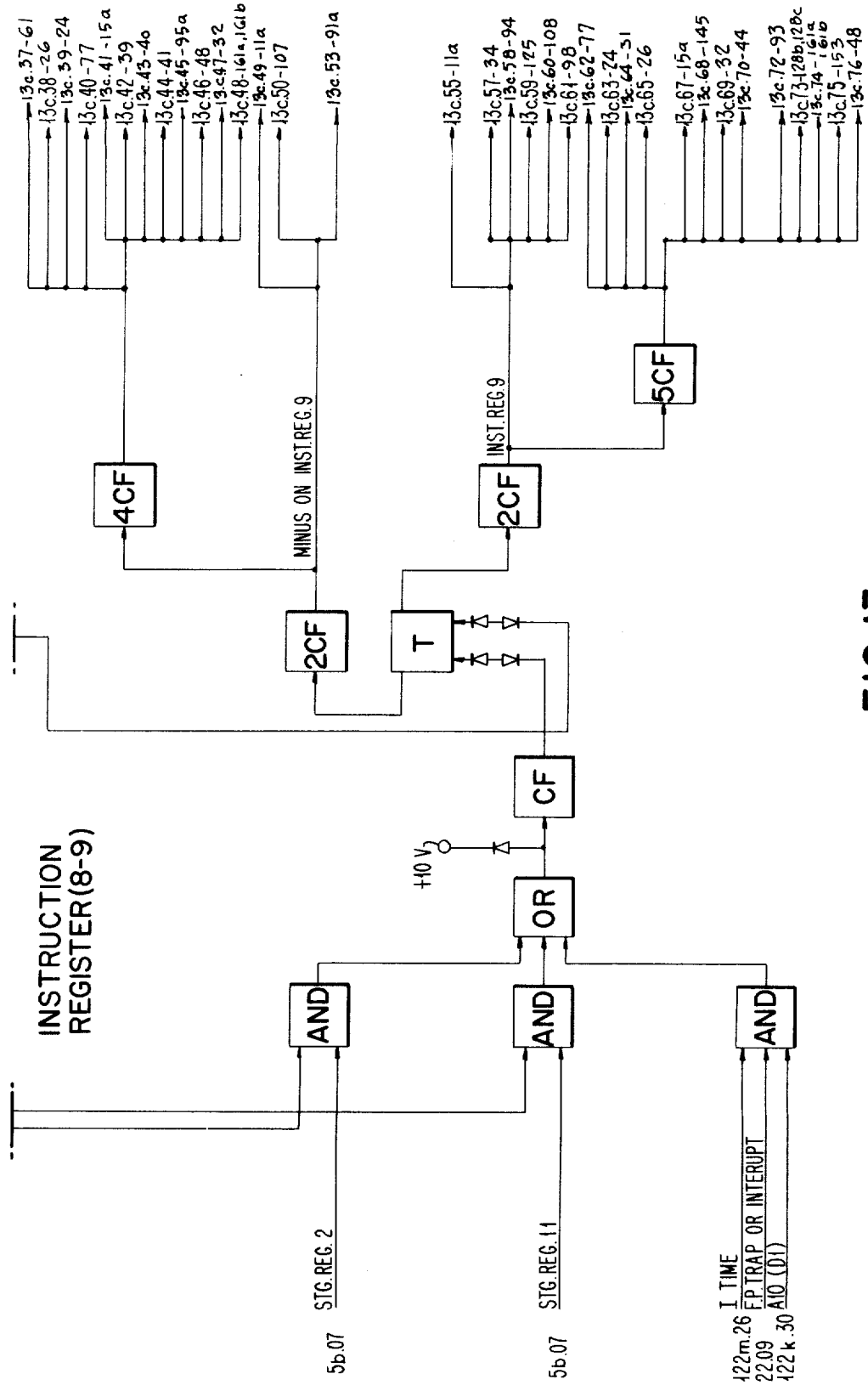


FIG.13c
(SHEET 2 OF 2)

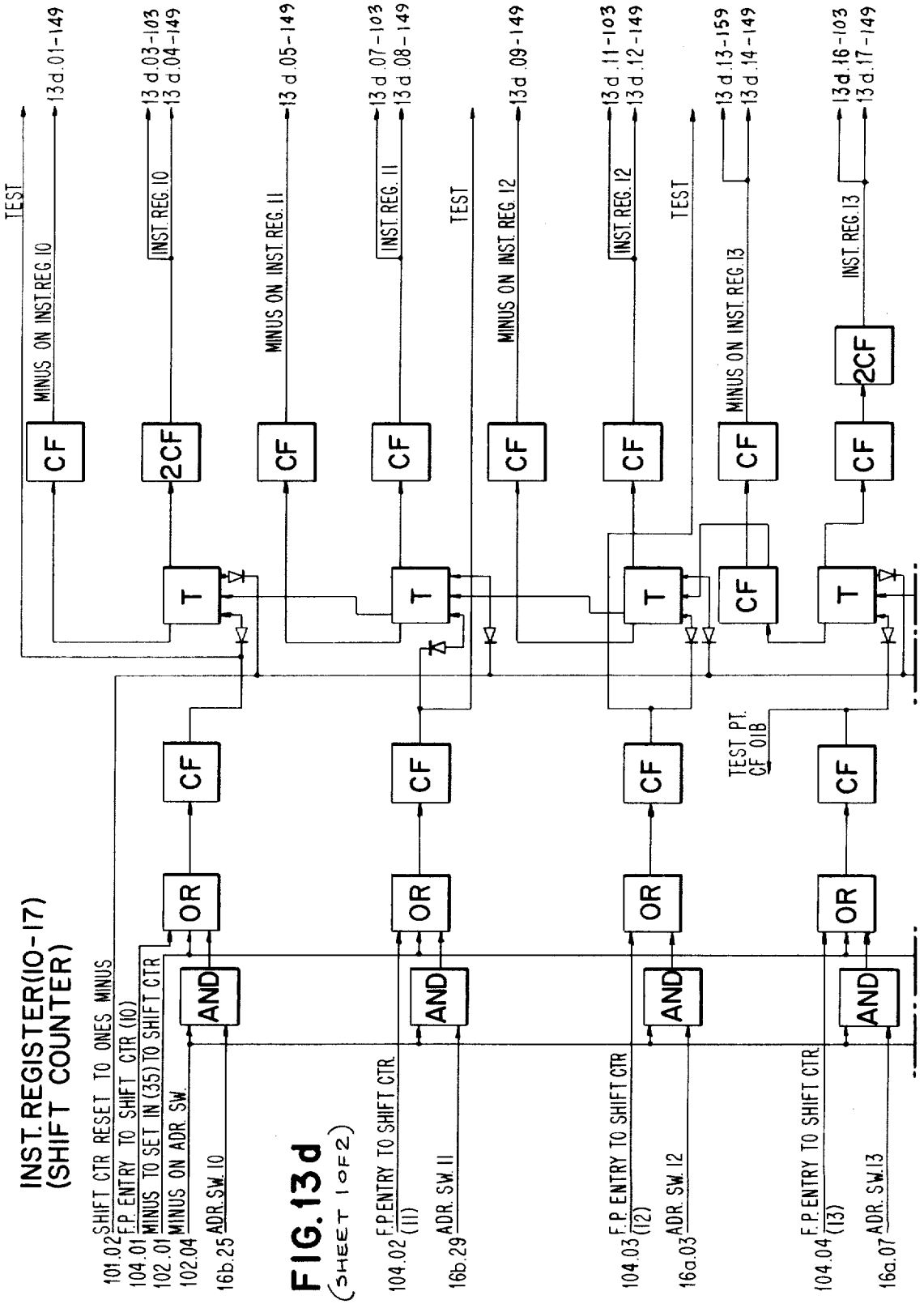


FIG. 13d
(SHEET 1 OF 2)

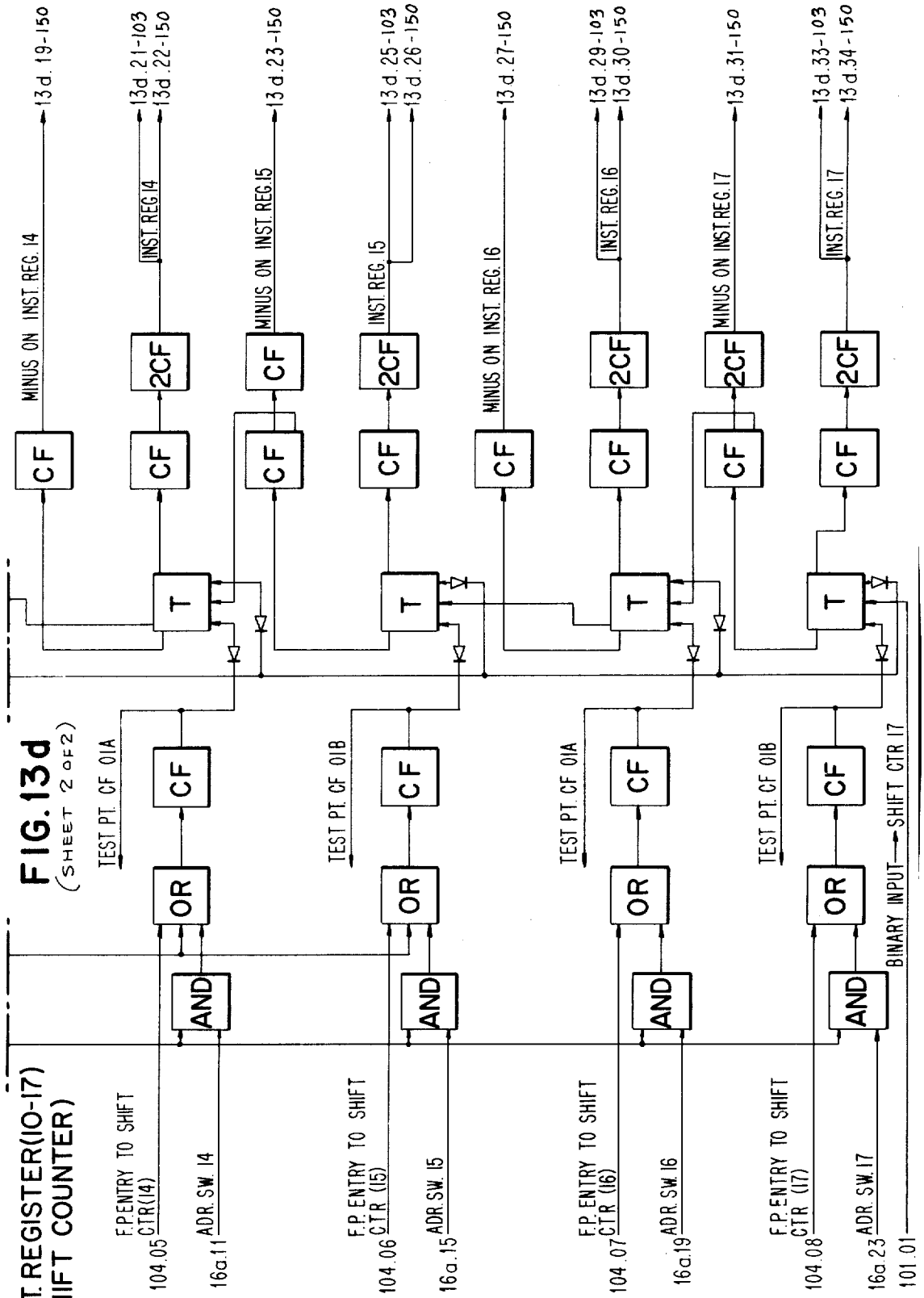


FIG. 13d
(SHEET 2 OF 2)

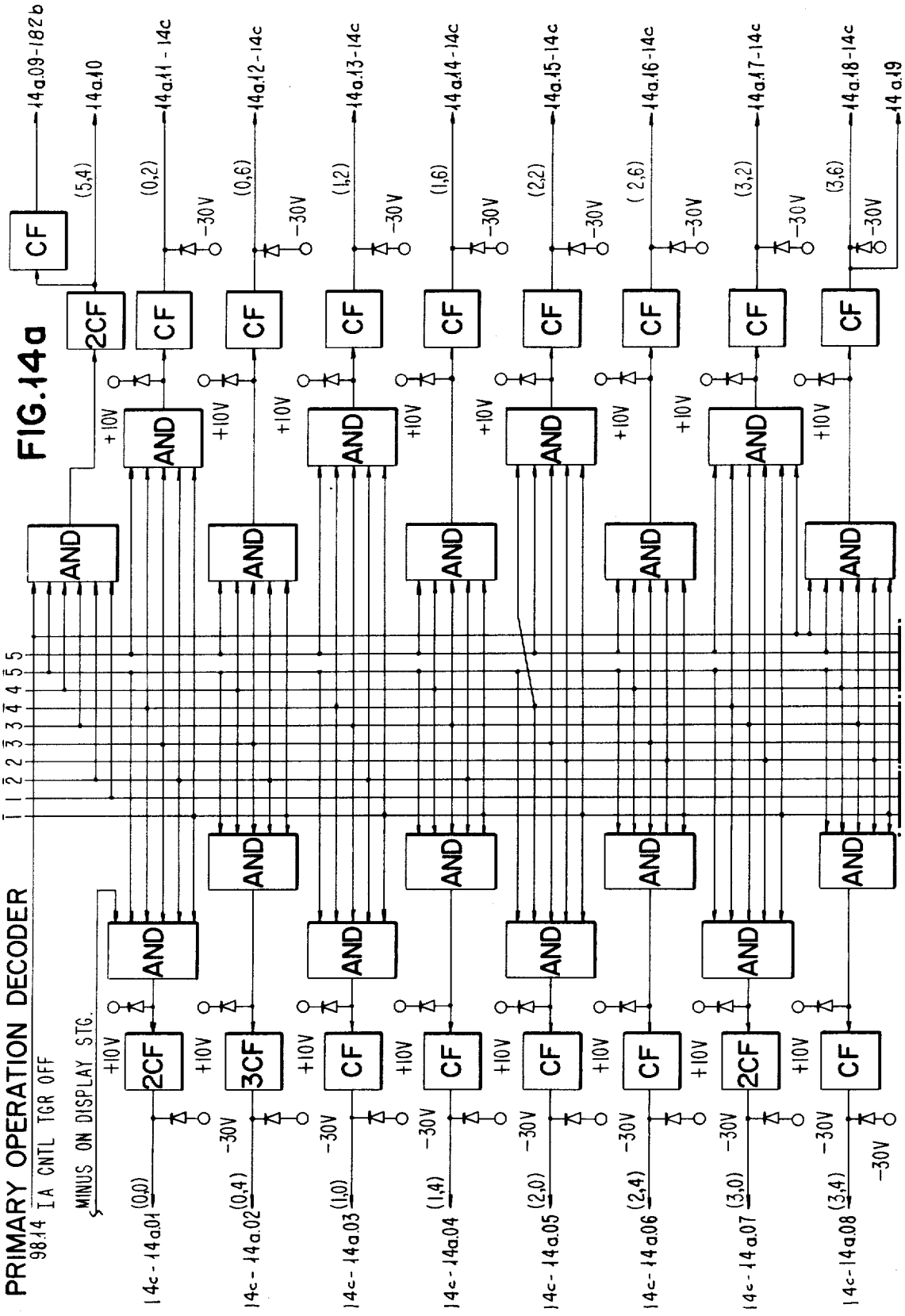
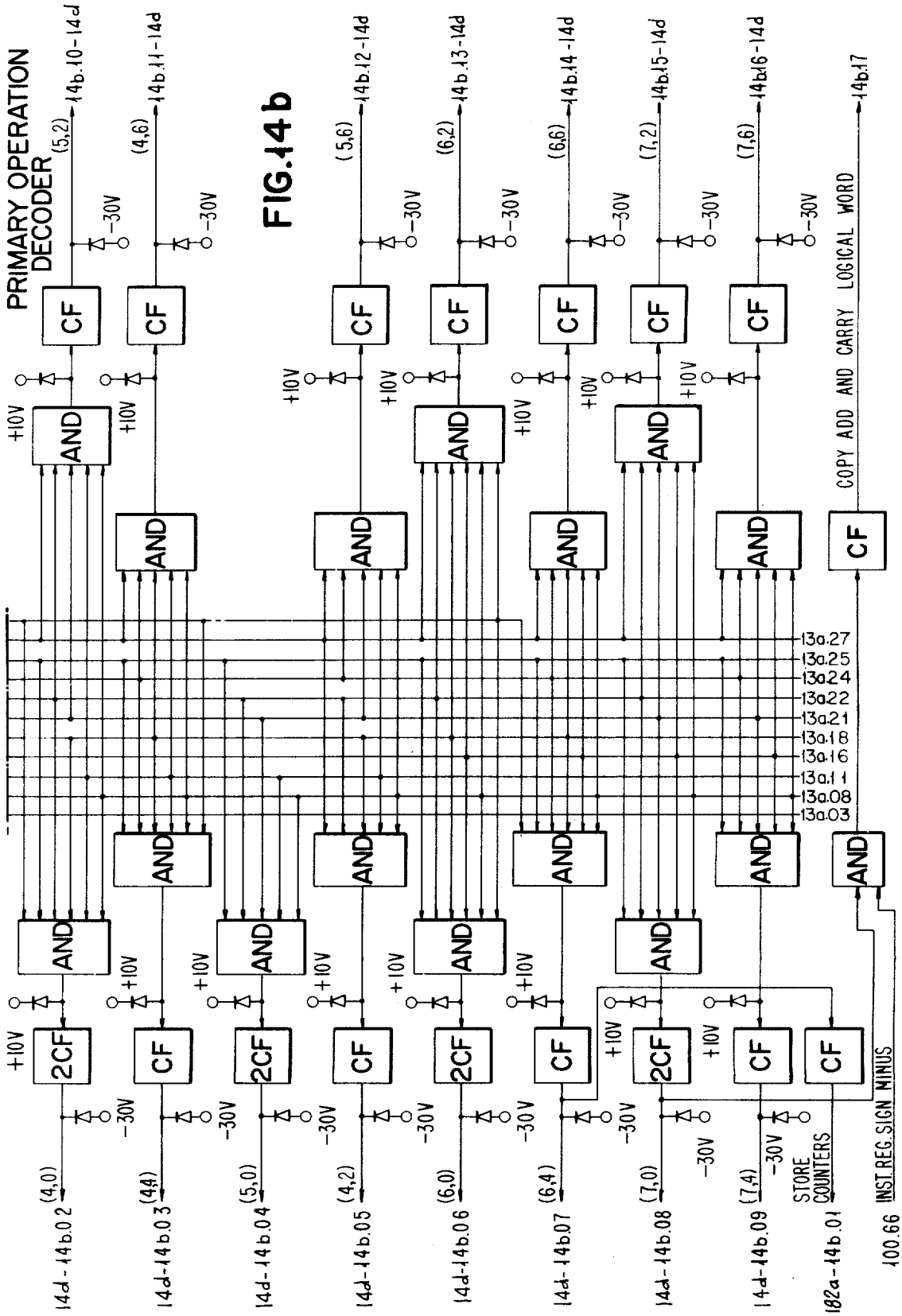

FIG.14a
PRIMARY OPERATION DECODER
98.14 IA CNTL TGR OFF
MINUS ON DISPLAY STG.
1 2 3 4 5
AND
CF
2CF
3CF
+10V
-30V
14a.09-182b
14a.10
14a.11 - 14c
14a.12-14c
14a.13-14c
14a.14-14c
14a.15-14c
14a.16-14c
14a.17-14c
14a.18-14c
14a.19
(5,4)
(0,2)
(0,6)
(1,2)
(1,6)
(2,2)
(2,6)
(3,2)
(3,6)
14c-14a.01 (0,0)
14c-14a.02 (0,4)
14c-14a.03 (1,0)
14c-14a.04 (1,4)
14c-14a.05 (2,0)
14c-14a.06 (2,4)
14c-14a.07 (3,0)
14c-14a.08 (3,4)

FIG.14b


PRIMARY OPERATION DECODER
14b.10-14d
14b.11-14d
14b.12-14d
14b.13-14d
14b.14-14d
14b.15-14d
14b.16-14d
14b.17
(5,2)
(4,6)
(5,6)
(6,2)
(6,6)
(7,2)
(7,6)
-30V
+10V
CF
2CF
AND
13a.27
13a.25
13a.24
13a.22
13a.21
13a.18
13a.16
13a.11
13a.08
13a.03
COPY ADD AND CARRY LOGICAL WORD
14d-14b.02 (4,0)
14d-14b.03 (4,4)
14d-14b.04 (5,0)
14d-14b.05 (4,2)
14d-14b.06 (6,0)
14d-14b.07 (6,4)
14d-14b.08 (7,0)
14d-14b.09 (7,4)
182a-14b.01 STORE COUNTERS
100.66 INST.REG.SIGN MINUS

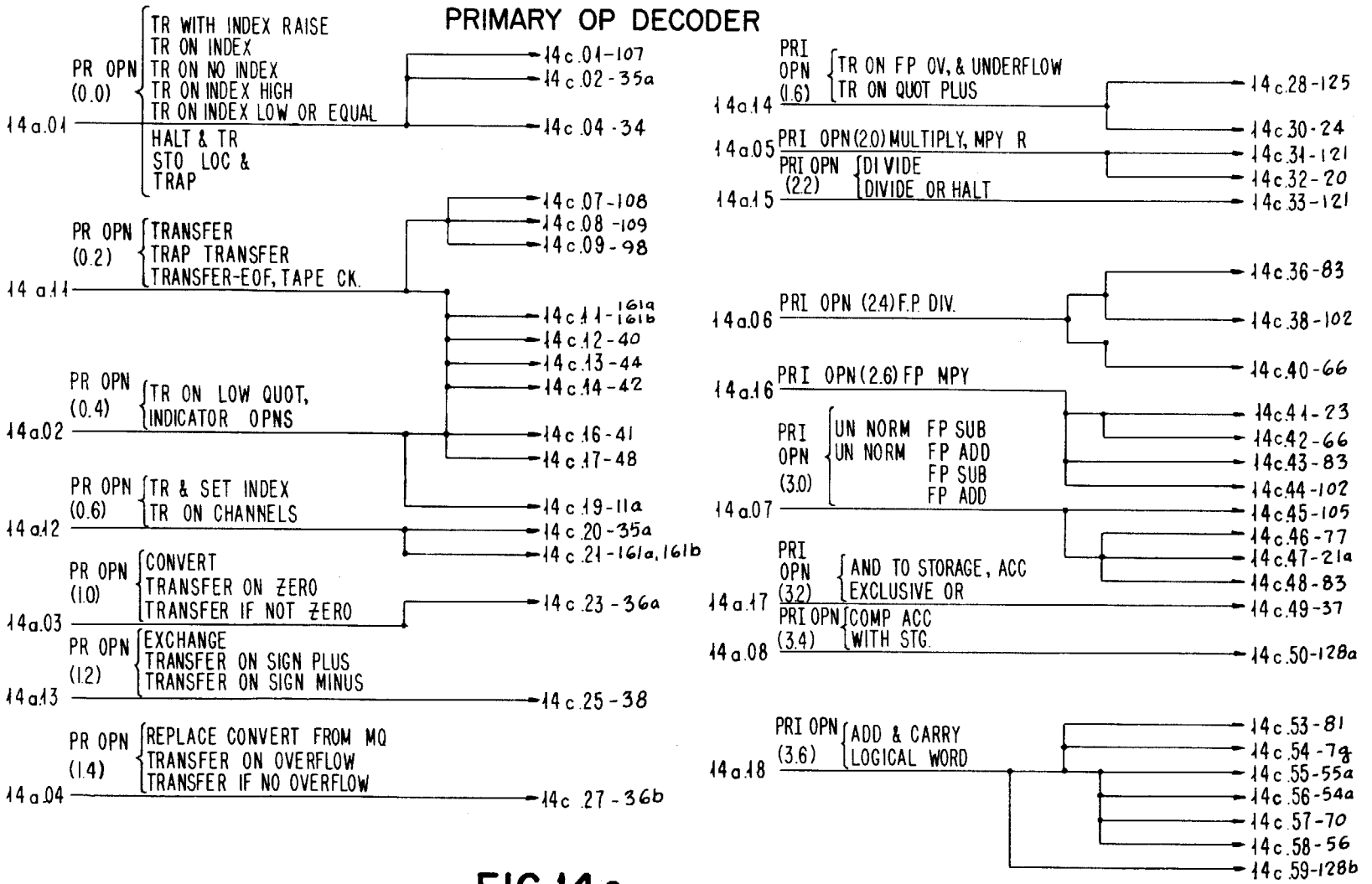

PRIMARY OP DECODER
PR OPN (0.0)
TR WITH INDEX RAISE
TR ON INDEX
TR ON NO INDEX
TR ON INDEX HIGH
TR ON INDEX LOW OR EQUAL
HALT & TR
STO LOC &
TRAP
14a.01
14c.01-107
14c.02-35a
14c.04-34
PR OPN (0.2)
TRANSFER
TRAP TRANSFER
TRANSFER-EOF, TAPE CK.
14a.11
14c.07-108
14c.08-109
14c.09-98
14c.11-161a
14c.11-161b
14c.12-40
14c.13-44
14c.14-42
PR OPN (0.4)
TR ON LOW QUOT, INDICATOR OPNS
14a.02
14c.16-41
14c.17-48
PR OPN (0.6)
TR & SET INDEX
TR ON CHANNELS
14a.12
14c.19-11a
14c.20-35a
14c.21-161a, 161b
PR OPN (1.0)
CONVERT
TRANSFER ON ZERO
TRANSFER IF NOT ZERO
14a.03
14c.23-36a
PR OPN (1.2)
EXCHANGE
TRANSFER ON SIGN PLUS
TRANSFER ON SIGN MINUS
14a.13
14c.25-38
PR OPN (1.4)
REPLACE CONVERT FROM MQ
TRANSFER ON OVERFLOW
TRANSFER IF NO OVERFLOW
14a.04
14c.27-36b
PRI OPN (1.6)
TR ON FP OV, & UNDERFLOW
TR ON QUOT PLUS
14a.14
14c.28-125
14c.30-24
PRI OPN (2.0) MULTIPLY, MPY R
14a.05
14c.31-121
PRI OPN (2.2)
DIVIDE
DIVIDE OR HALT
14a.15
14c.32-20
14c.33-121
PRI OPN (2.4) F.P. DIV.
14a.06
14c.36-83
14c.38-102
14c.40-66
PRI OPN (2.6) FP MPY
14a.16
14c.41-23
14c.42-66
14c.43-83
14c.44-102
PRI OPN (3.0)
UN NORM FP SUB
UN NORM FP ADD
FP SUB
FP ADD
14a.07
14c.45-105
PRI OPN (3.2)
AND TO STORAGE, ACC
EXCLUSIVE OR
14a.17
14c.46-77
14c.47-21a
14c.48-83
14c.49-37
PRI OPN (3.4)
COMP ACC WITH STG
14a.08
14c.50-128a
PRI OPN (3.6)
ADD & CARRY
LOGICAL WORD
14a.18
14c.53-81
14c.54-7g
14c.55-55a
14c.56-54a
14c.57-70
14c.58-56
14c.59-128b

FIG. 14c

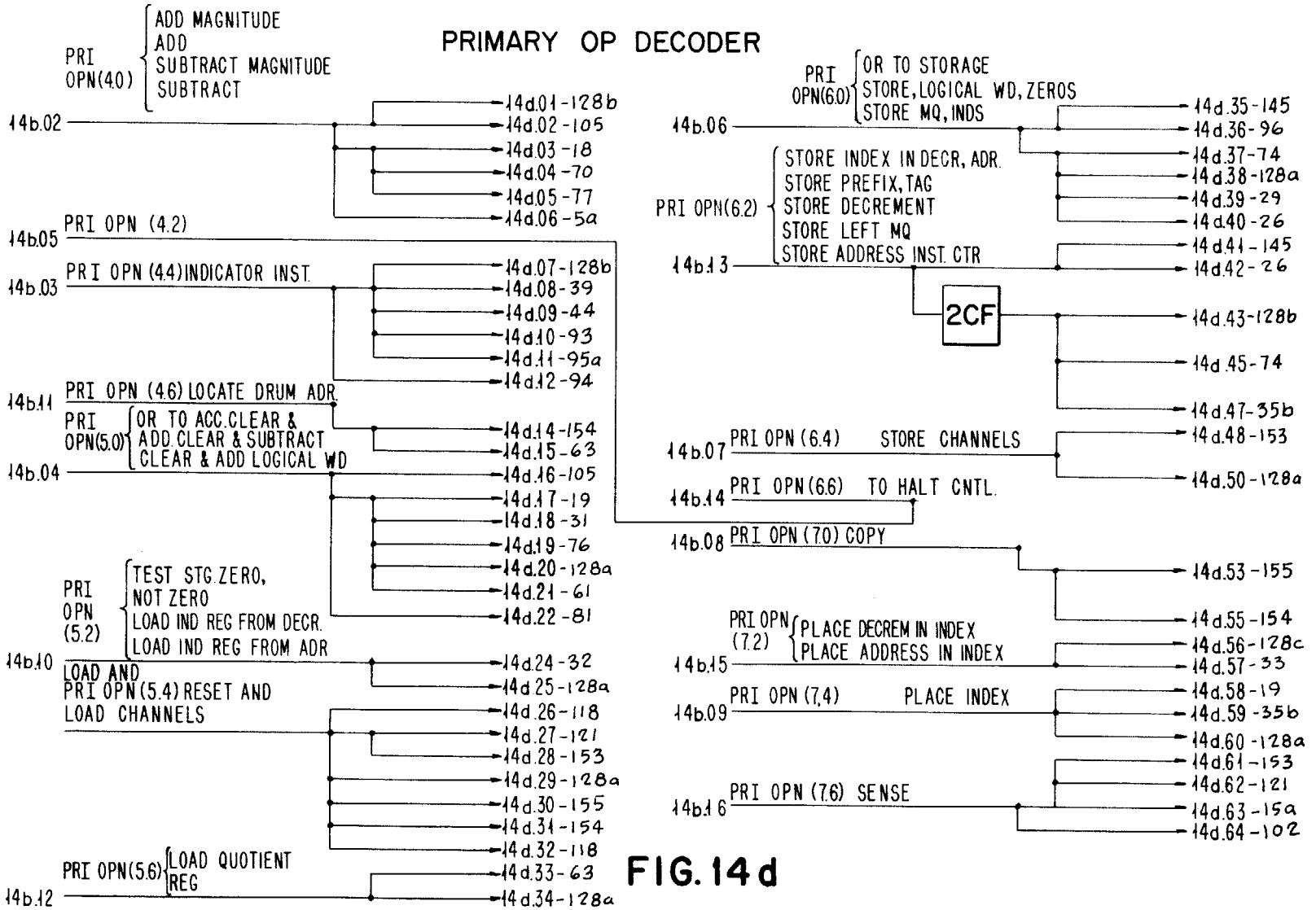

PRIMARY OP DECODER
PRI OPN(4.0) { ADD MAGNITUDE, ADD, SUBTRACT MAGNITUDE, SUBTRACT
14b.02
14d.01-128b
14d.02-105
14d.03-18
14d.04-70
14d.05-77
14d.06-5a
14b.05 PRI OPN (4.2)
14b.03 PRI OPN (4.4) INDICATOR INST.
14d.07-128b
14d.08-39
14d.09-44
14d.10-93
14d.11-95a
14d.12-94
14b.11 PRI OPN (4.6) LOCATE DRUM ADR.
PRI OPN(5.0) { OR TO ACC. CLEAR & ADD, CLEAR & SUBTRACT, CLEAR & ADD LOGICAL WD
14b.04
14d.14-154
14d.15-63
14d.16-105
14d.17-19
14d.18-31
14d.19-76
14d.20-128a
14d.21-61
14d.22-81
PRI OPN (5.2) { TEST STG. ZERO, NOT ZERO, LOAD IND REG FROM DECR., LOAD IND REG FROM ADR
14b.10
14d.24-32
14d.25-128a
LOAD AND PRI OPN (5.4) RESET AND LOAD CHANNELS
14d.26-118
14d.27-121
14d.28-153
14d.29-128a
14d.30-155
14d.31-154
14d.32-118
PRI OPN(5.6) { LOAD QUOTIENT REG
14b.12
14d.33-63
14d.34-128a
PRI OPN(6.0) { OR TO STORAGE, STORE, LOGICAL WD, ZEROS, STORE MQ, INDS
14b.06
14d.35-145
14d.36-96
14d.37-74
14d.38-128a
14d.39-29
14d.40-26
PRI OPN(6.2) { STORE INDEX IN DECR. ADR., STORE PREFIX, TAG, STORE DECREMENT, STORE LEFT MQ, STORE ADDRESS INST. CTR
14b.13
14d.41-145
14d.42-26
2CF
14d.43-128b
14d.45-74
14d.47-35b
14b.07 PRI OPN (6.4) STORE CHANNELS
14d.48-153
14d.50-128a
14b.14 PRI OPN(6.6) TO HALT CNTL.
14b.08 PRI OPN (7.0) COPY
14d.53-155
14d.55-154
PRI OPN (7.2) { PLACE DECREM IN INDEX, PLACE ADDRESS IN INDEX
14b.15
14d.56-128c
14d.57-33
14b.09 PRI OPN (7.4) PLACE INDEX
14d.58-19
14d.59-35b
14d.60-128a
14d.61-153
14d.62-121
14b.16 PRI OPN (7.6) SENSE
14d.63-15a
14d.64-102

FIG. 14d

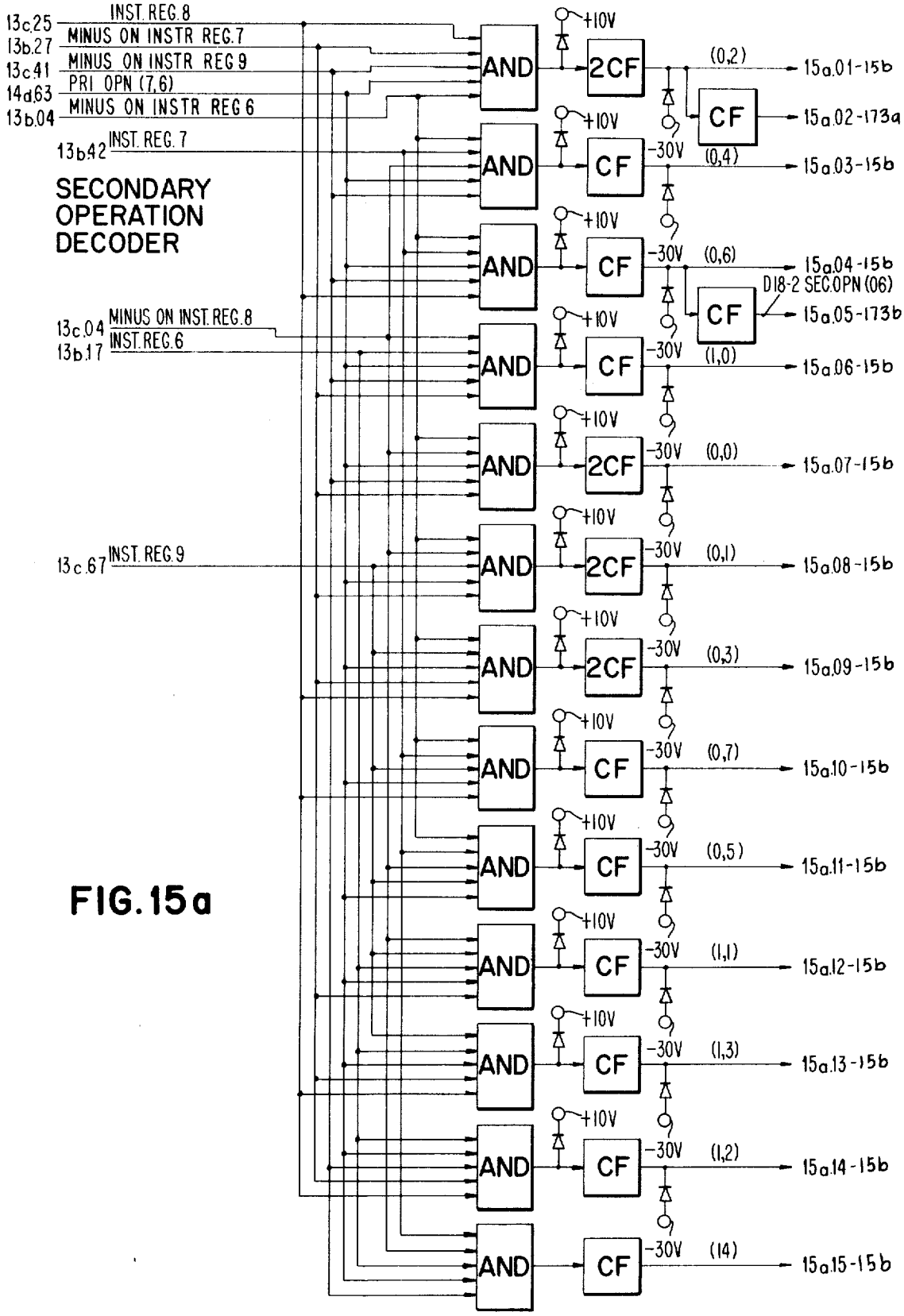

13c.25 INST. REG. 8
13b.27 MINUS ON INSTR REG. 7
13c.41 MINUS ON INSTR REG 9
14d.63 PRI OPN (7,6)
13b.04 MINUS ON INSTR REG 6
13b.42 INST. REG. 7
SECONDARY OPERATION DECODER
13c.04 MINUS ON INST. REG. 8
13b.17 INST. REG. 6
13c.67 INST. REG. 9
AND
+10V
2CF
CF
-30V
(0,2)
(0,4)
(0,6)
(1,0)
(0,0)
(0,1)
(0,3)
(0,7)
(0,5)
(1,1)
(1,3)
(1,2)
(14)
15a.01-15b
15a.02-173a
15a.03-15b
15a.04-15b
D18-2 SEC.OPN (06)
15a.05-173b
15a.06-15b
15a.07-15b
15a.08-15b
15a.09-15b
15a.10-15b
15a.11-15b
15a.12-15b
15a.13-15b
15a.14-15b
15a.15-15b

FIG. 15a

SECONDARY OPERATION DECODER

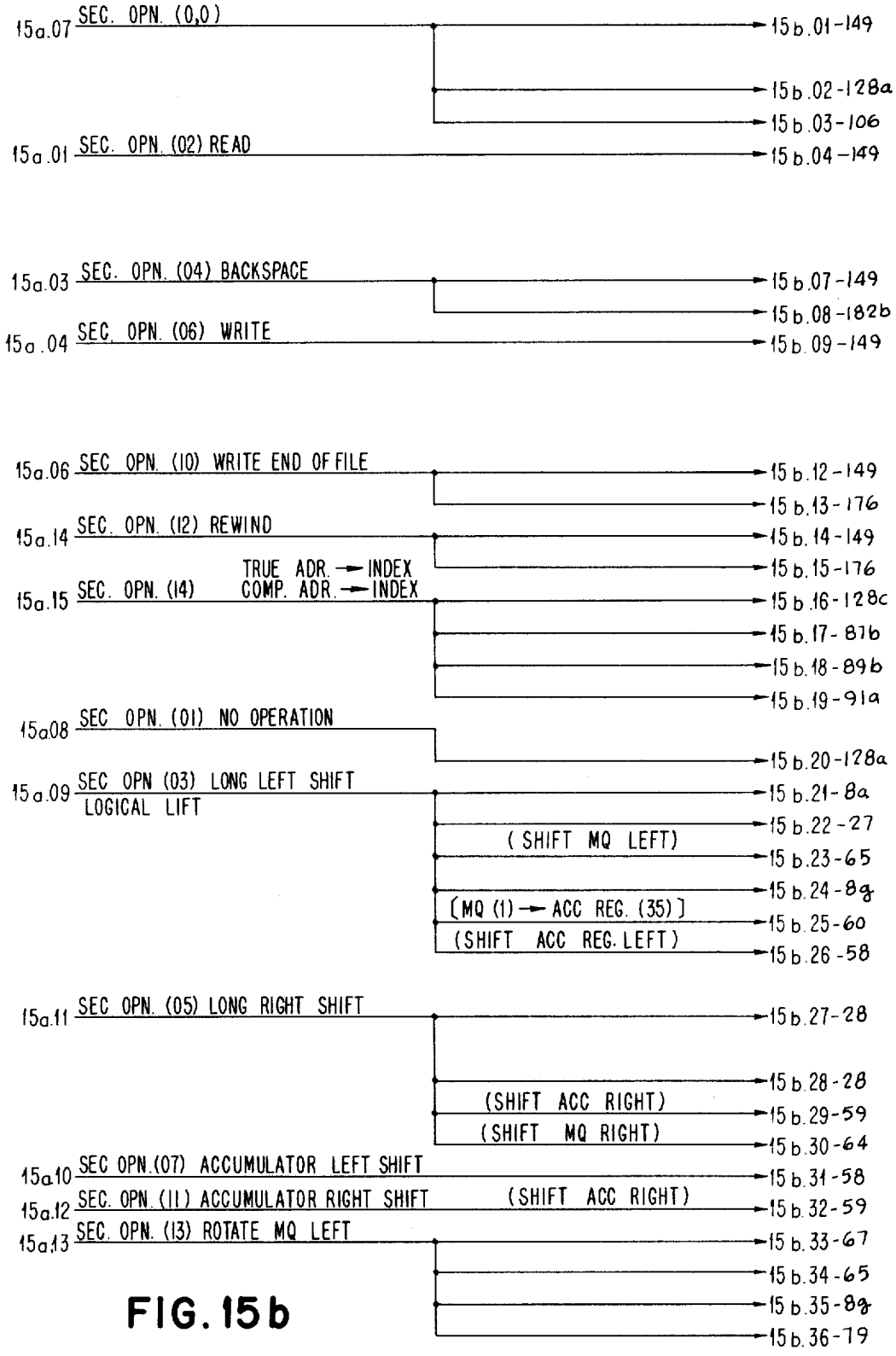


FIG. 15b

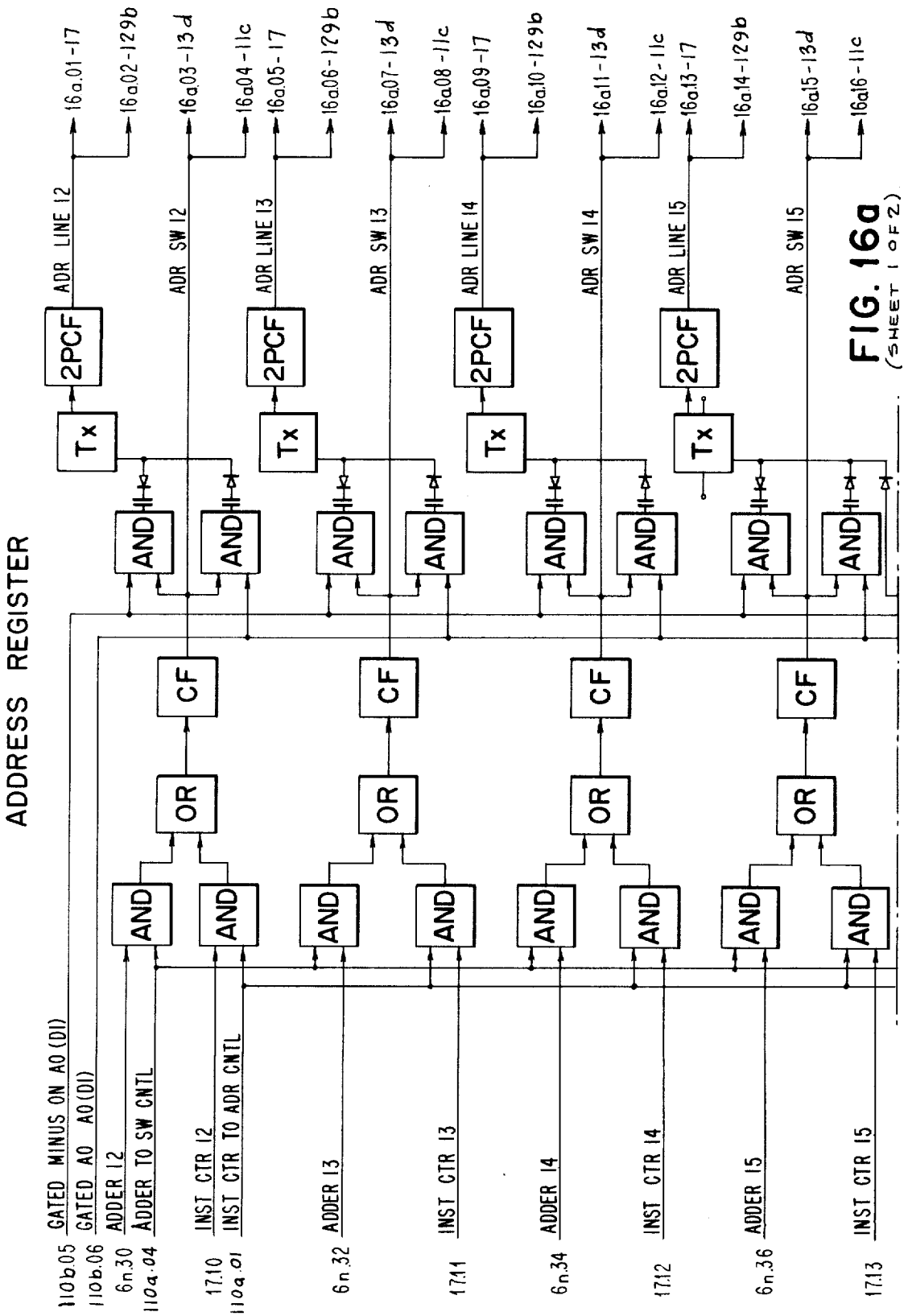


FIG. 16a
(SHEET 1 OF 2)

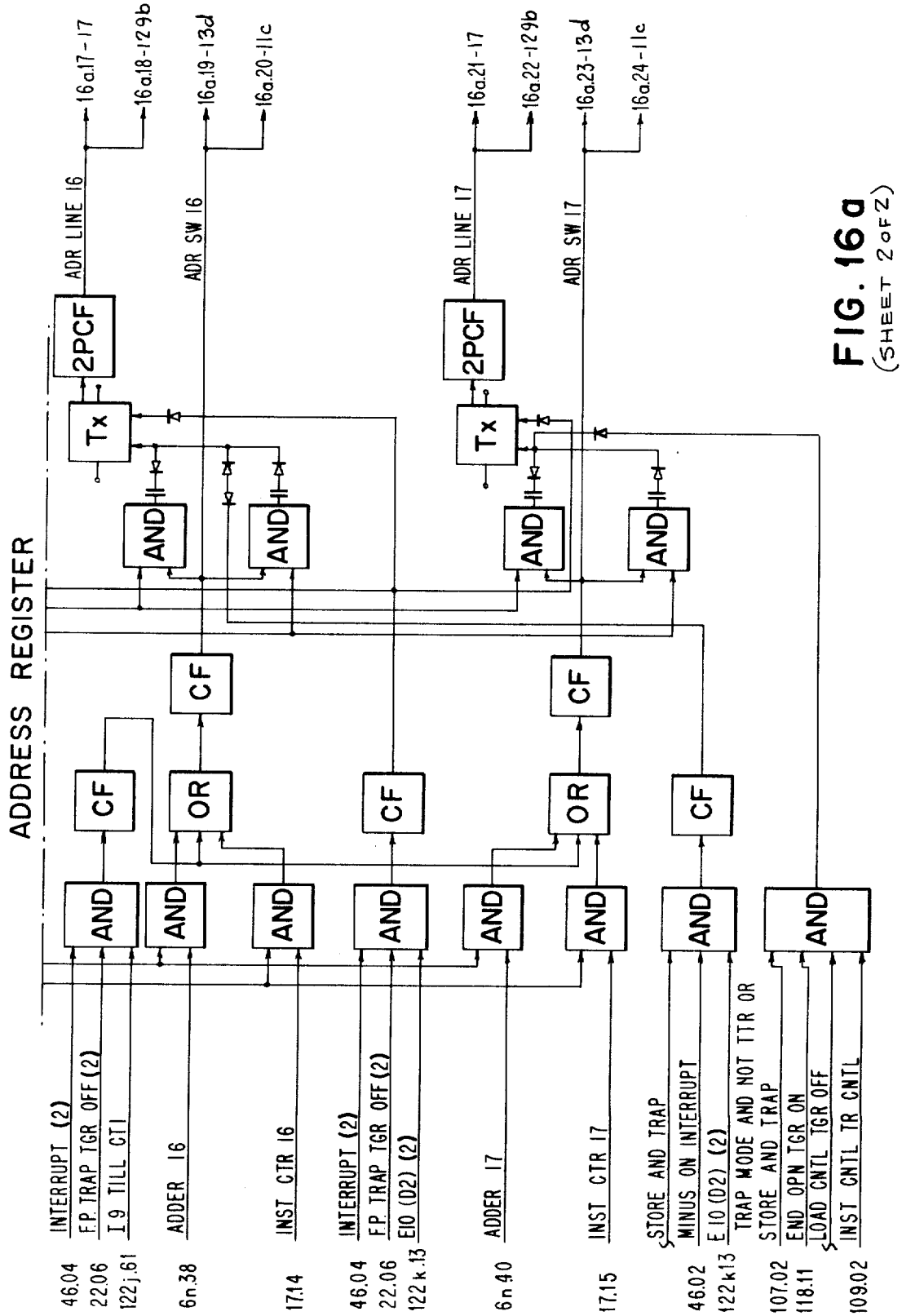


FIG. 16a
(SHEET 2 OF 2)

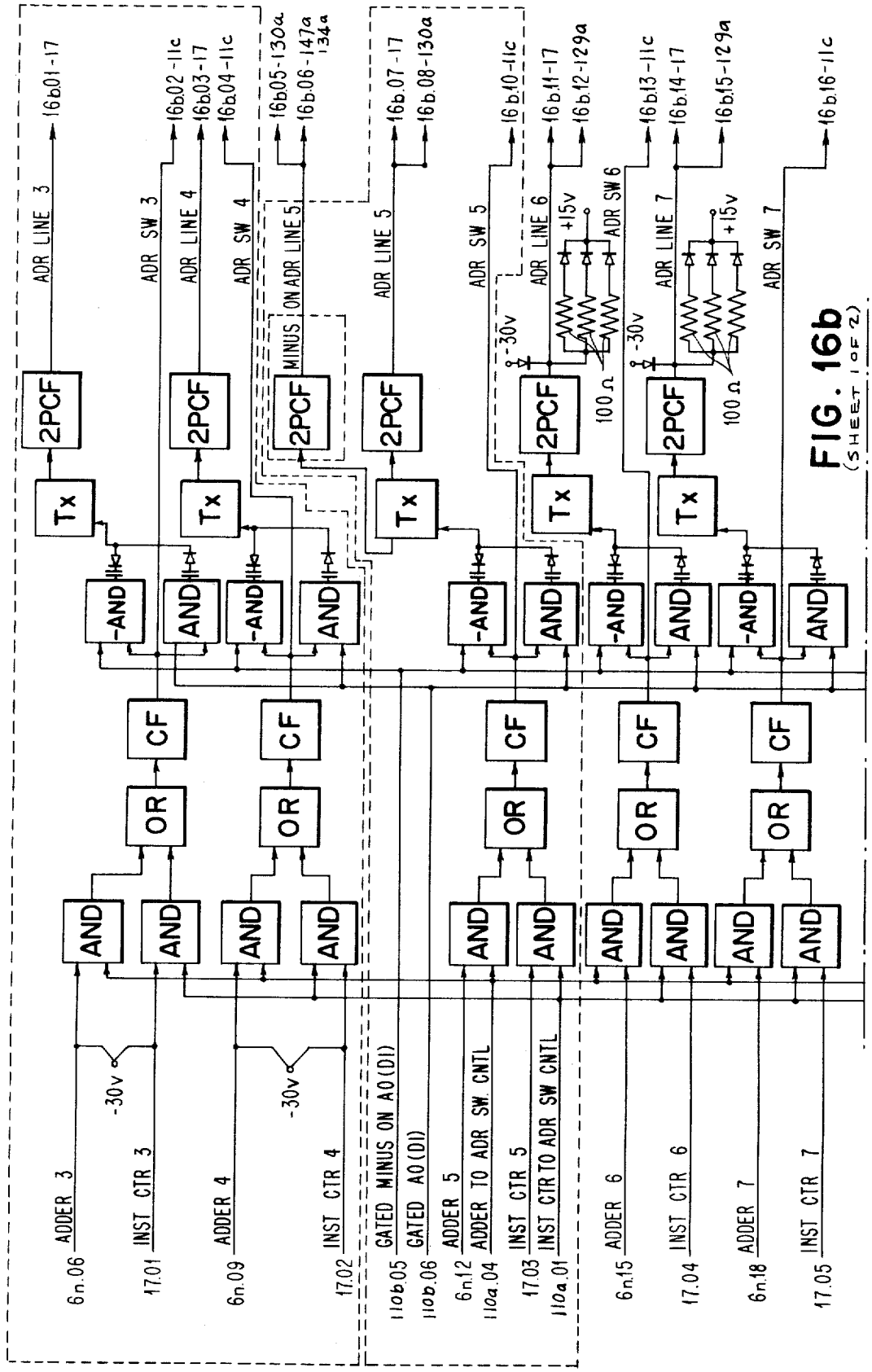


FIG. 16b
(SHEET 1 OF 2)

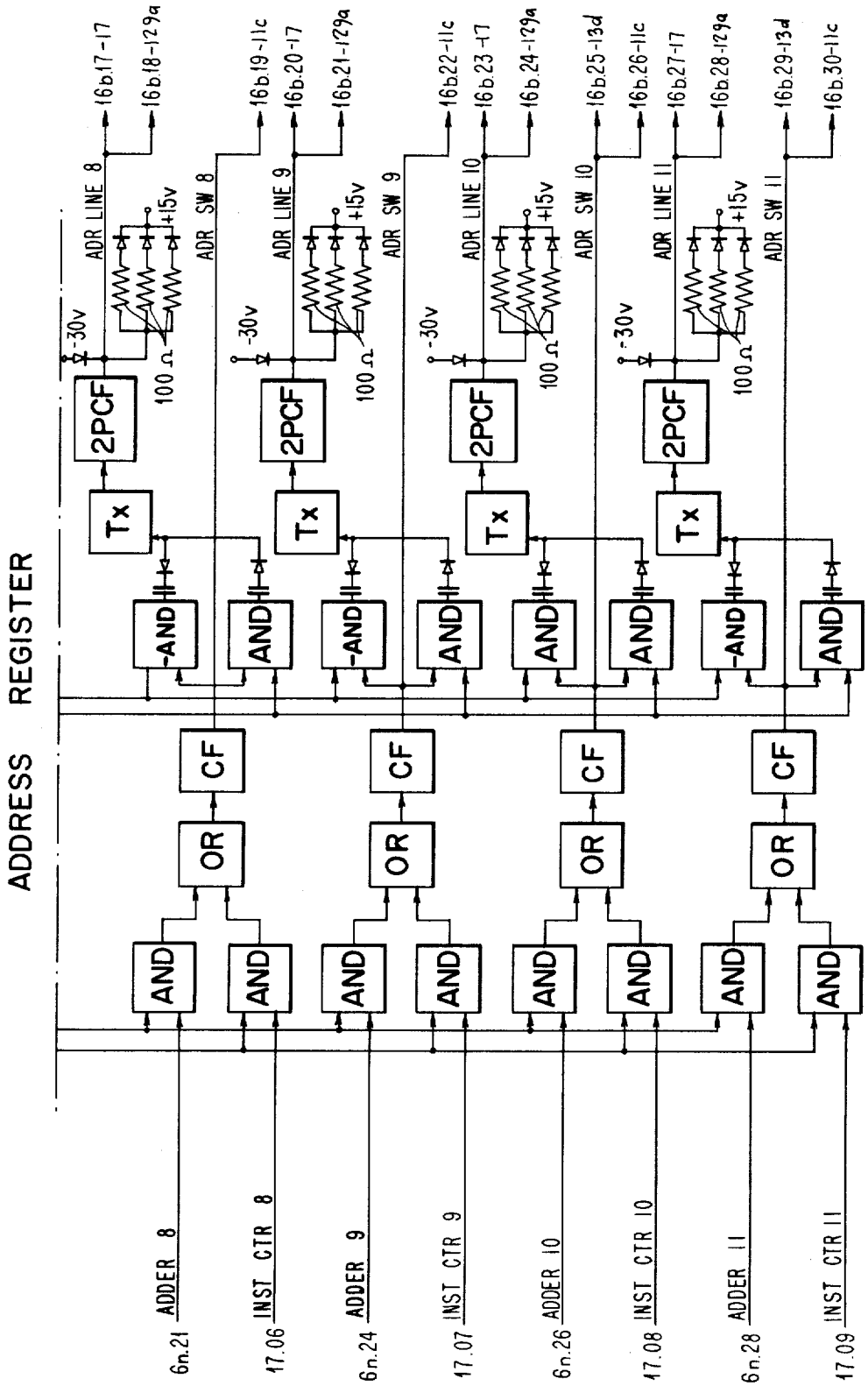


FIG. 16b
(SHEET 2 OF 2)

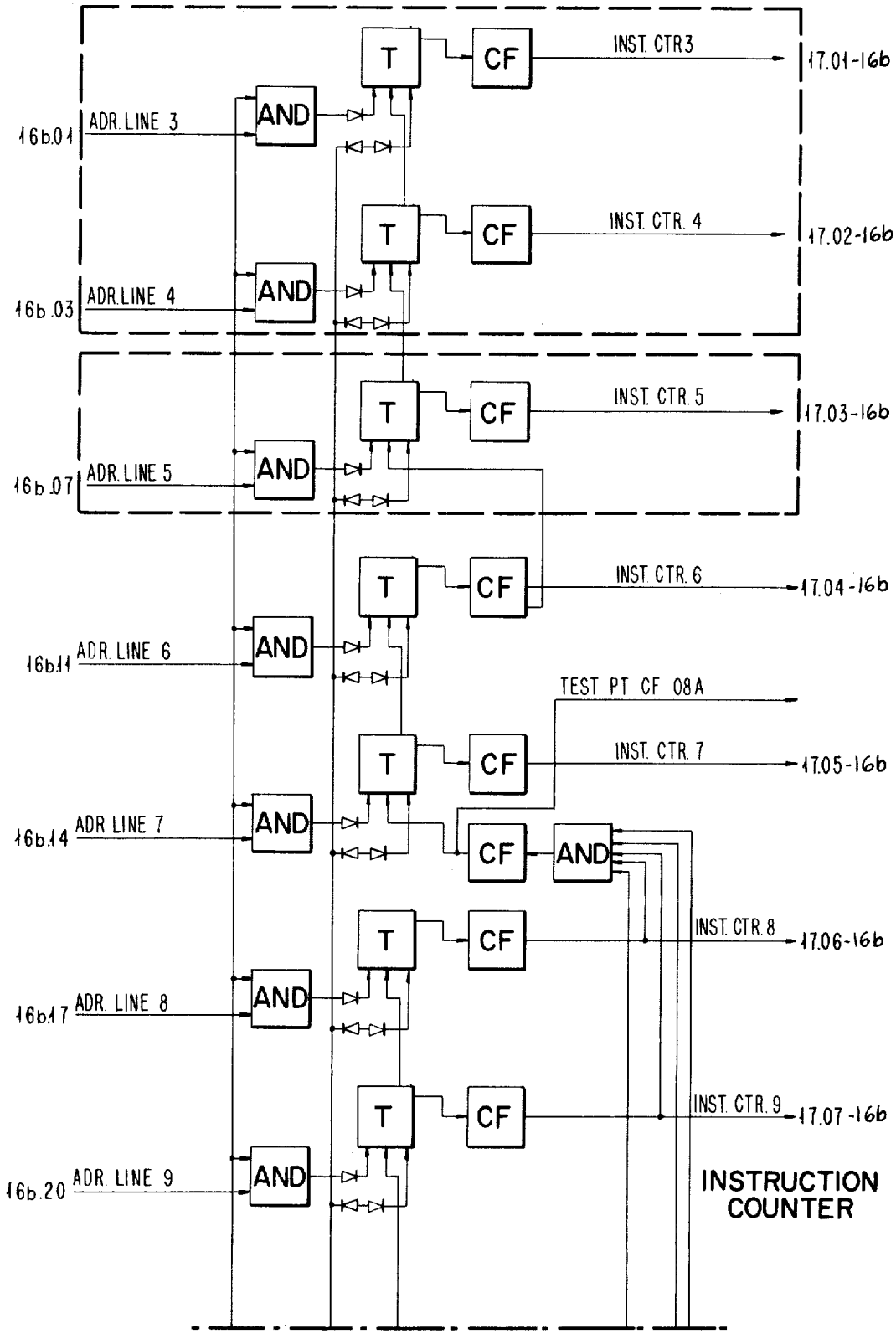


FIG.17
(SHEET 1 OF 2)

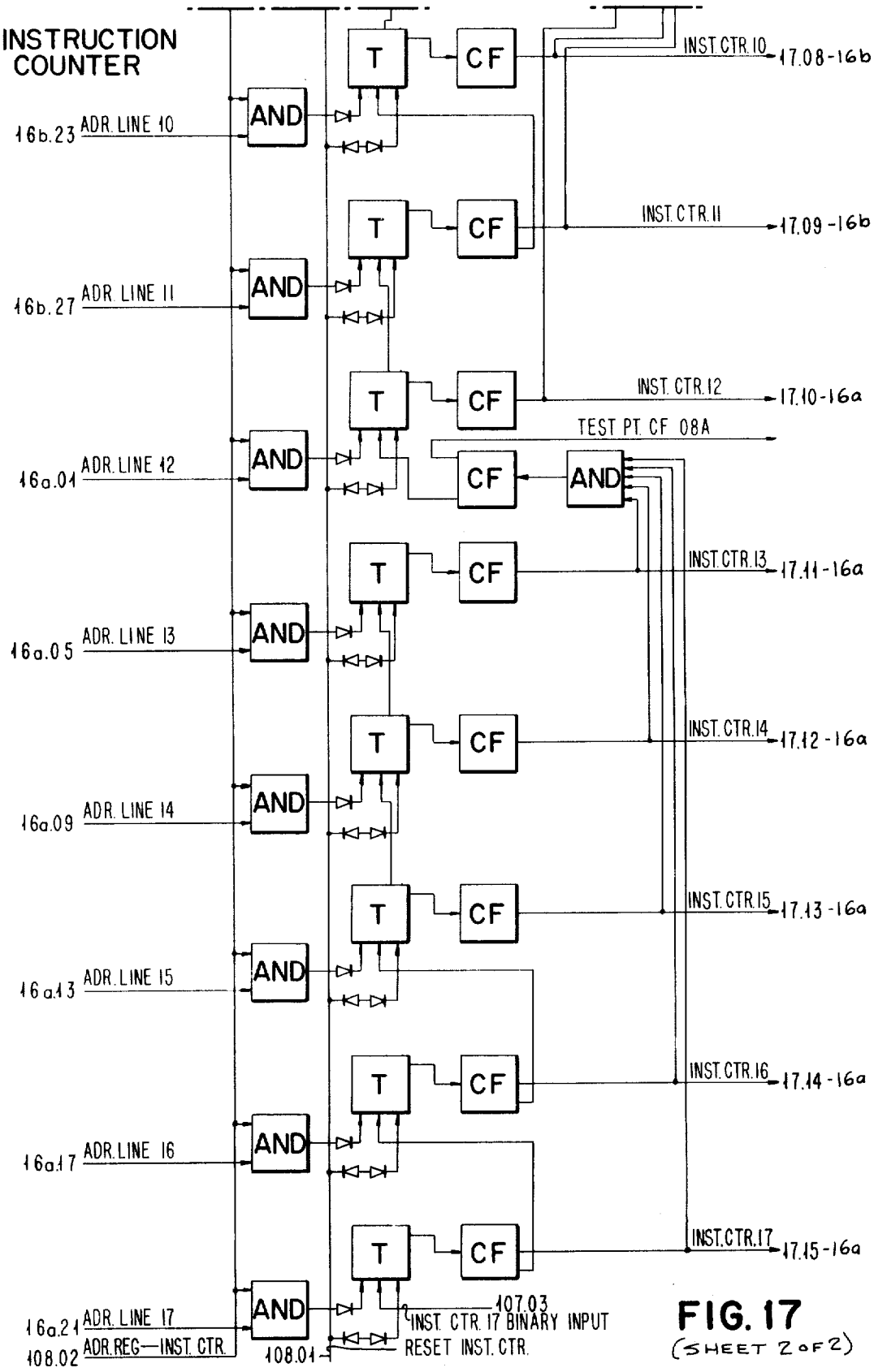


FIG. 17
(SHEET 2 OF 2)

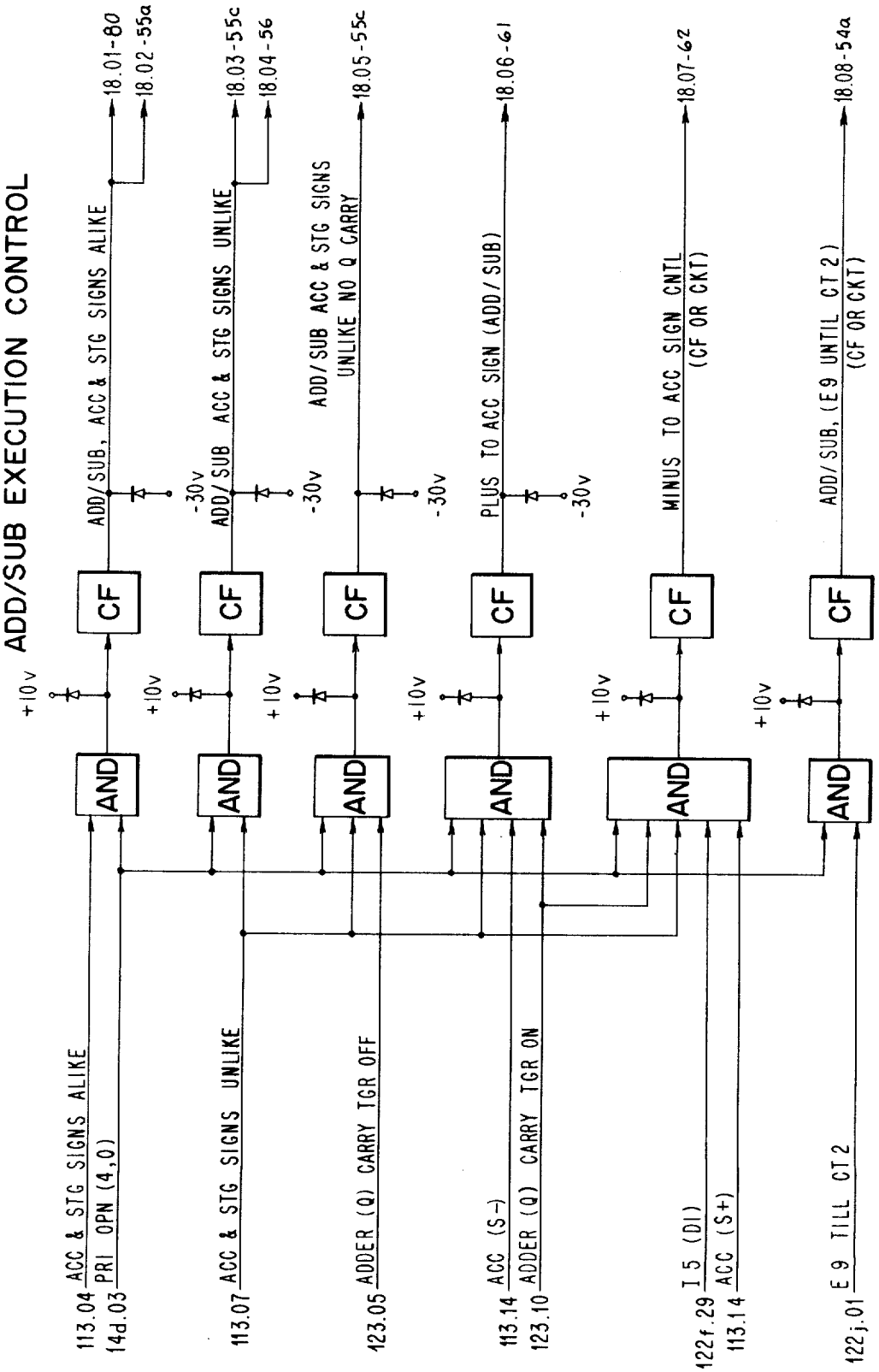

ADD/SUB EXECUTION CONTROL
113.04 ACC & STG SIGNS ALIKE
14d.03 PRI OPN (4,0)
113.07 ACC & STG SIGNS UNLIKE
123.05 ADDER (Q) CARRY TGR OFF
113.14 ACC (S-)
123.10 ADDER (Q) CARRY TGR ON
122f.29 I 5 (DI)
113.14 ACC (S+)
122j.01 E 9 TILL CT 2
+10v
AND
CF
-30v
ADD/SUB, ACC & STG SIGNS ALIKE
ADD/SUB ACC & STG SIGNS UNLIKE
ADD/SUB ACC & STG SIGNS UNLIKE NO Q CARRY
PLUS TO ACC SIGN (ADD/SUB)
MINUS TO ACC SIGN CNTL (CF OR CKT)
ADD/SUB, (E9 UNTIL CT 2) (CF OR CKT)
18.01-80
18.02-55a
18.03-55c
18.04-56
18.05-55c
18.06-61
18.07-62
18.08-54a

FIG.18

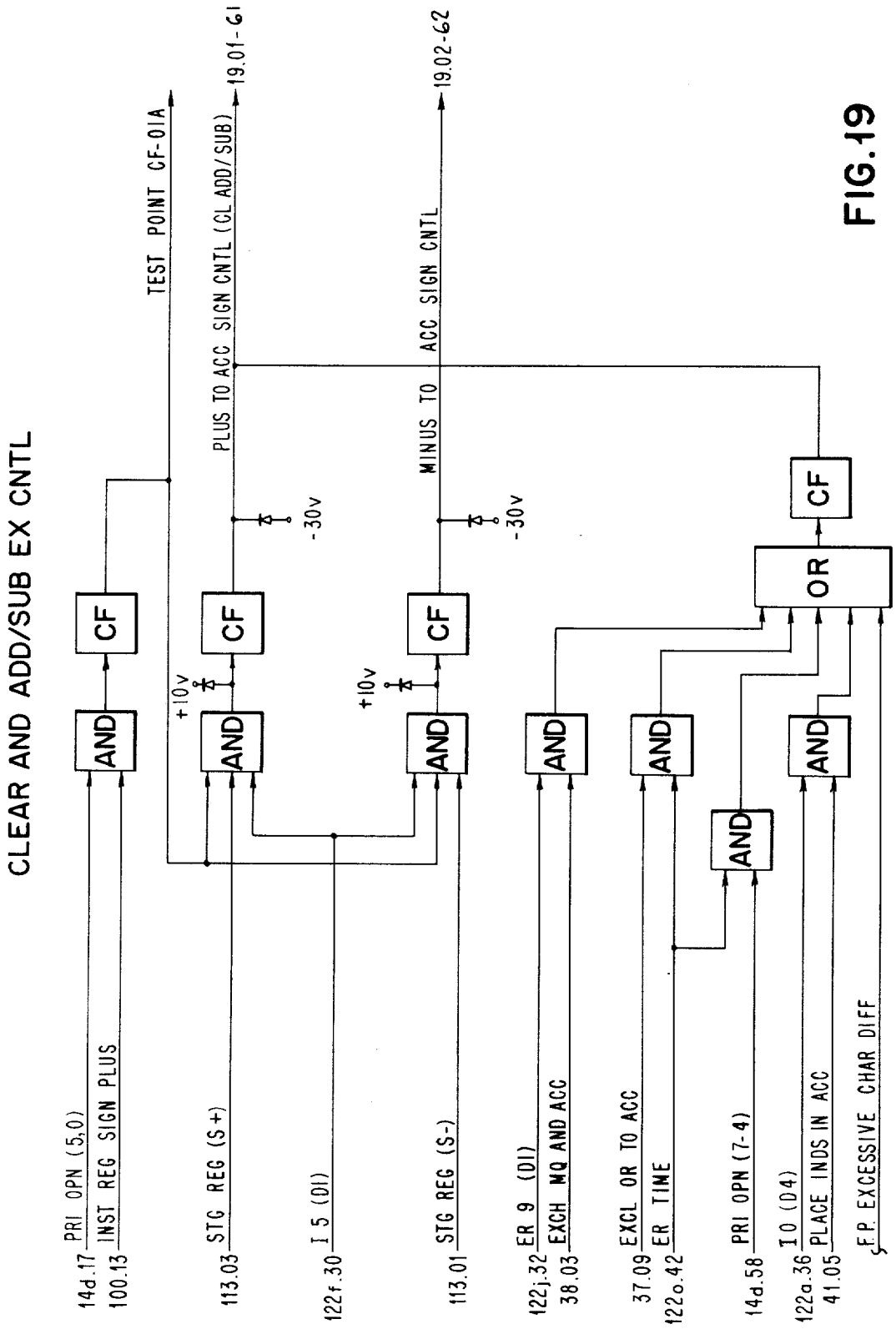
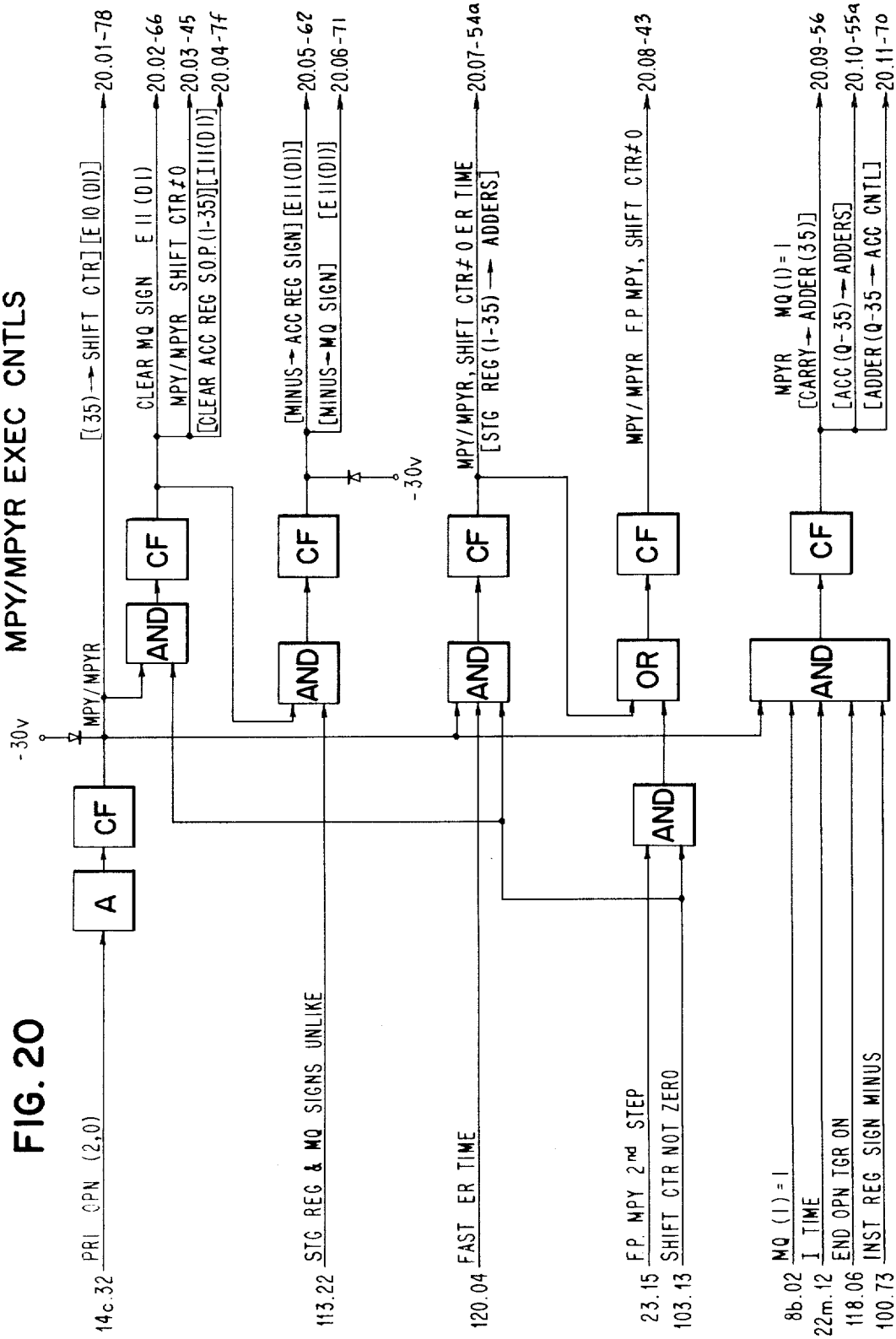

CLEAR AND ADD/SUB EX CNTL
TEST POINT CF-01A
PLUS TO ACC SIGN CNTL (CL ADD/SUB)
19.01-61
MINUS TO ACC SIGN CNTL
19.02-62
+10v
-30v
CF
AND
OR
14d.17 PRI OPN (5,0)
100.13 INST REG SIGN PLUS
113.03 STG REG (S+)
122f.30 I 5 (01)
113.01 STG REG (S-)
122j.32 ER 9 (01)
38.03 EXCH MQ AND ACC
37.09 EXCL OR TO ACC
122o.42 ER TIME
14d.58 PRI OPN (7-4)
122a.36 I 0 (04)
41.05 PLACE INDS IN ACC
E.P. EXCESSIVE CHAR DIFF

FIG.19

FIG. 20

MPY/MPYR EXEC CNTLS



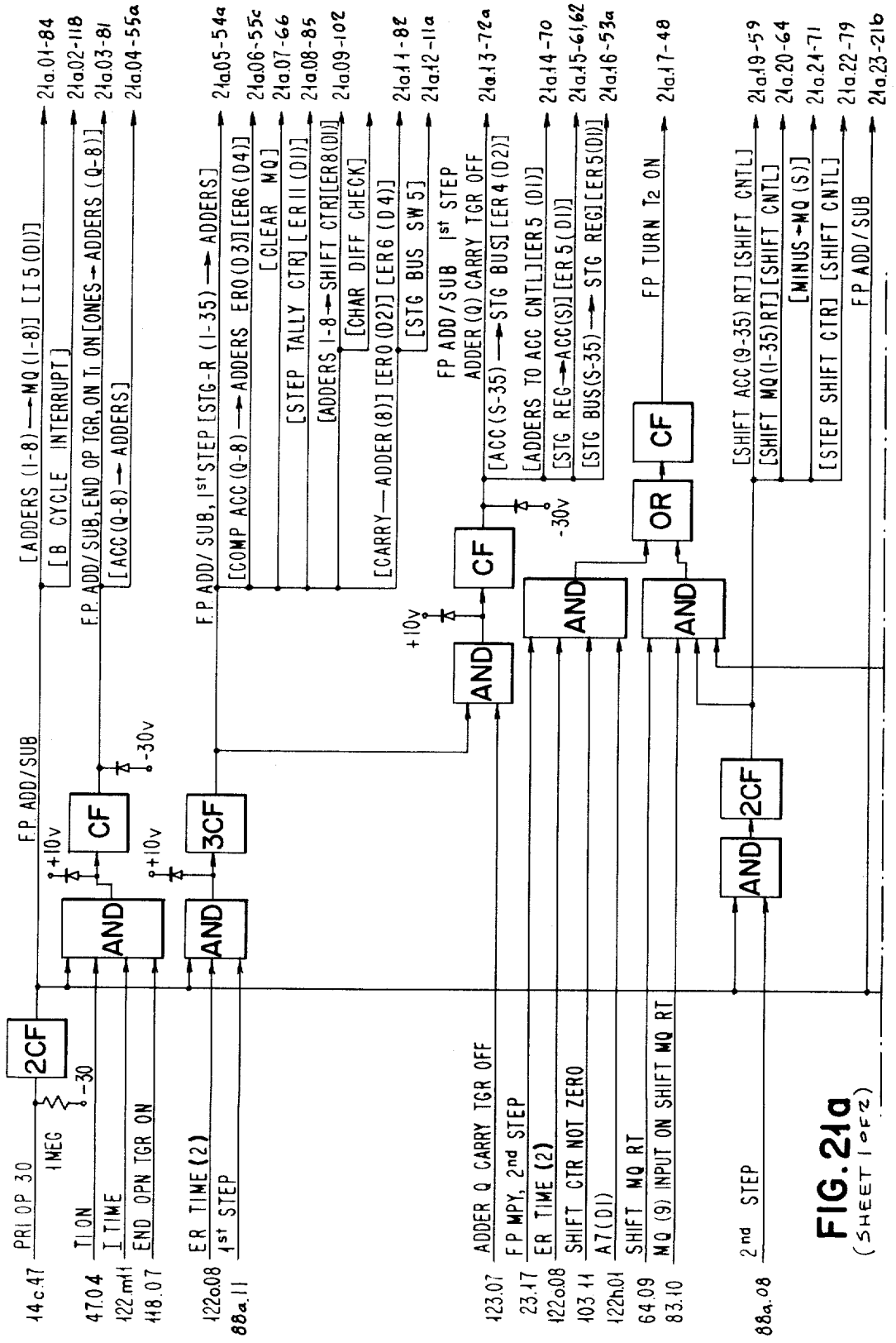
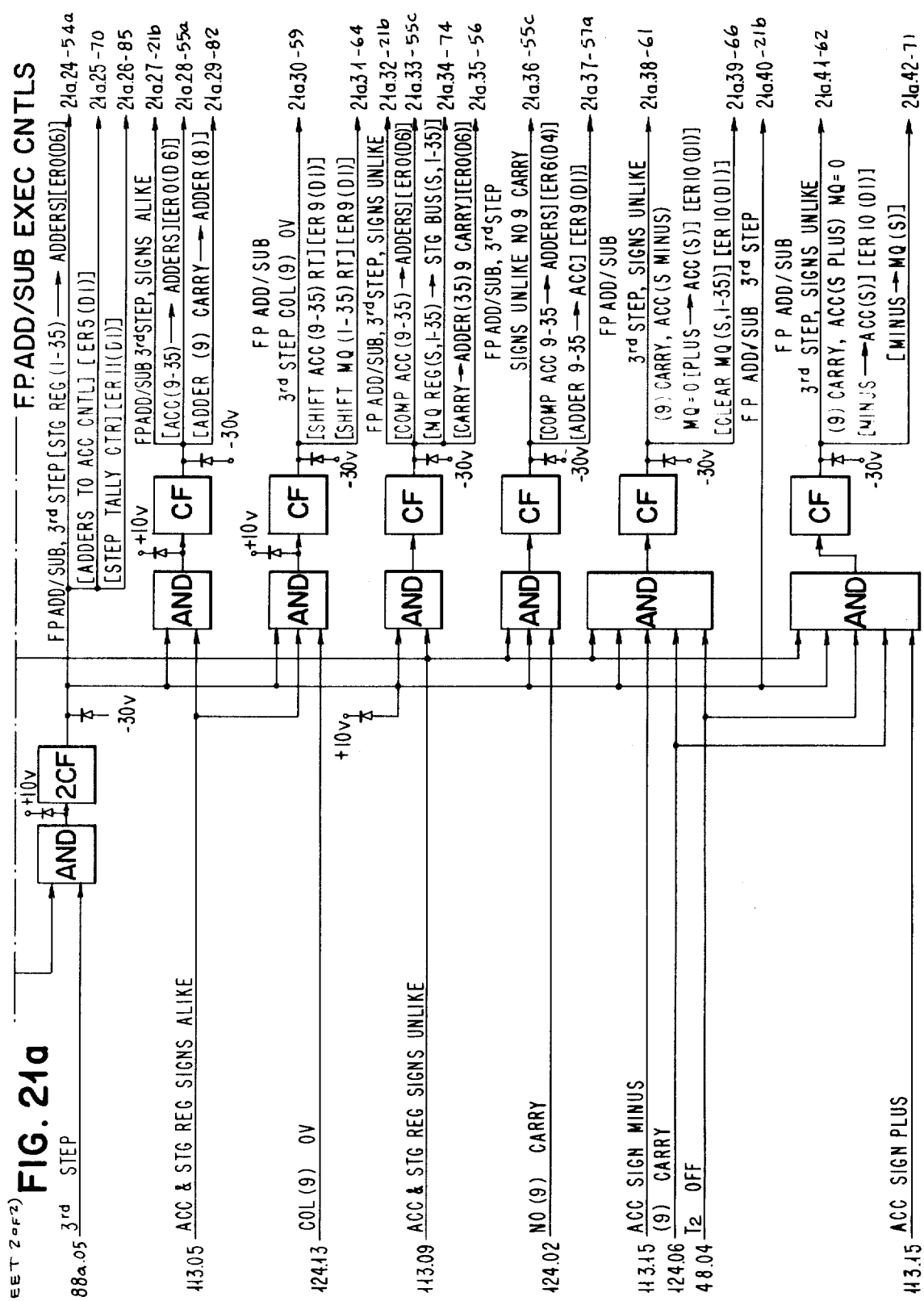


FIG. 21a
(SHEET 1 OF 2)


F.P. ADD/SUB EXEC CNTLS
FIG. 21a
(SHEET 2 of 2)
88a.05 3rd STEP
AND
+10v
2CF
-30v
F P ADD/SUB, 3rd STEP [STG REG (1-35) → ADDERS][ER0(D6)] 21a.24-54a
[ADDERS TO ACC CNTL] [ER5(D1)] 21a.25-70
[STEP TALLY CTR][ER11(D1)] 21a.26-85
113.05 ACC & STG REG SIGNS ALIKE
AND
+10v
CF
FPADD/SUB 3rdSTEP, SIGNS ALIKE
[ACC(9-35) → ADDERS][ER0(D6)] 21a.27-21b
[ADDER (9) CARRY → ADDER(8)] 21a.28-55a
-30v
21a.29-82
424.13 COL (9) 0V
AND
+10v
CF
F P ADD/SUB
3rd STEP COL(9) 0V 21a.30-59
[SHIFT ACC (9-35) RT][ER9(D1)]
[SHIFT MQ (1-35) RT][ER9(D1)] 21a.31-64
-30v
113.09 ACC & STG REG SIGNS UNLIKE
AND
+10v
CF
F P ADD/SUB, 3rdSTEP, SIGNS UNLIKE
[COMP ACC (9-35) → ADDERS][ER0(D6)] 21a.32-21b
[MQ REG(S,1-35) → STG BUS(S,1-35)] 21a.33-55c
[CARRY → ADDER(35) 9 CARRY][ER0(D6)] 21a.34-74
-30v
21a.35-56
424.02 NO (9) CARRY
AND
CF
F P ADD/SUB, 3rdSTEP
SIGNS UNLIKE NO 9 CARRY
[COMP ACC 9-35 → ADDERS][ER6(D4)] 21a.36-55c
[ADDER 9-35 → ACC][ER9(D1)] 21a.37-57a
-30v
113.15 ACC SIGN MINUS
124.06 (9) CARRY
48.04 I2 OFF
AND
CF
F P ADD/SUB
3rd STEP, SIGNS UNLIKE 21a.38-61
(9) CARRY, ACC(S MINUS)
MQ=0 [PLUS → ACC(S)][ER10(D1)]
[CLEAR MQ(S,1-35)][ER10(D1)] 21a.39-66
-30v
F P ADD/SUB 3rd STEP 21a.40-21b
113.15 ACC SIGN PLUS
AND
CF
F P ADD/SUB
3rd STEP, SIGNS UNLIKE 21a.41-62
(9) CARRY, ACC(S PLUS) MQ=0
[MINUS → ACC(S)][ER10(D1)]
[MINUS → MQ(S)] 21a.42-71
-30v

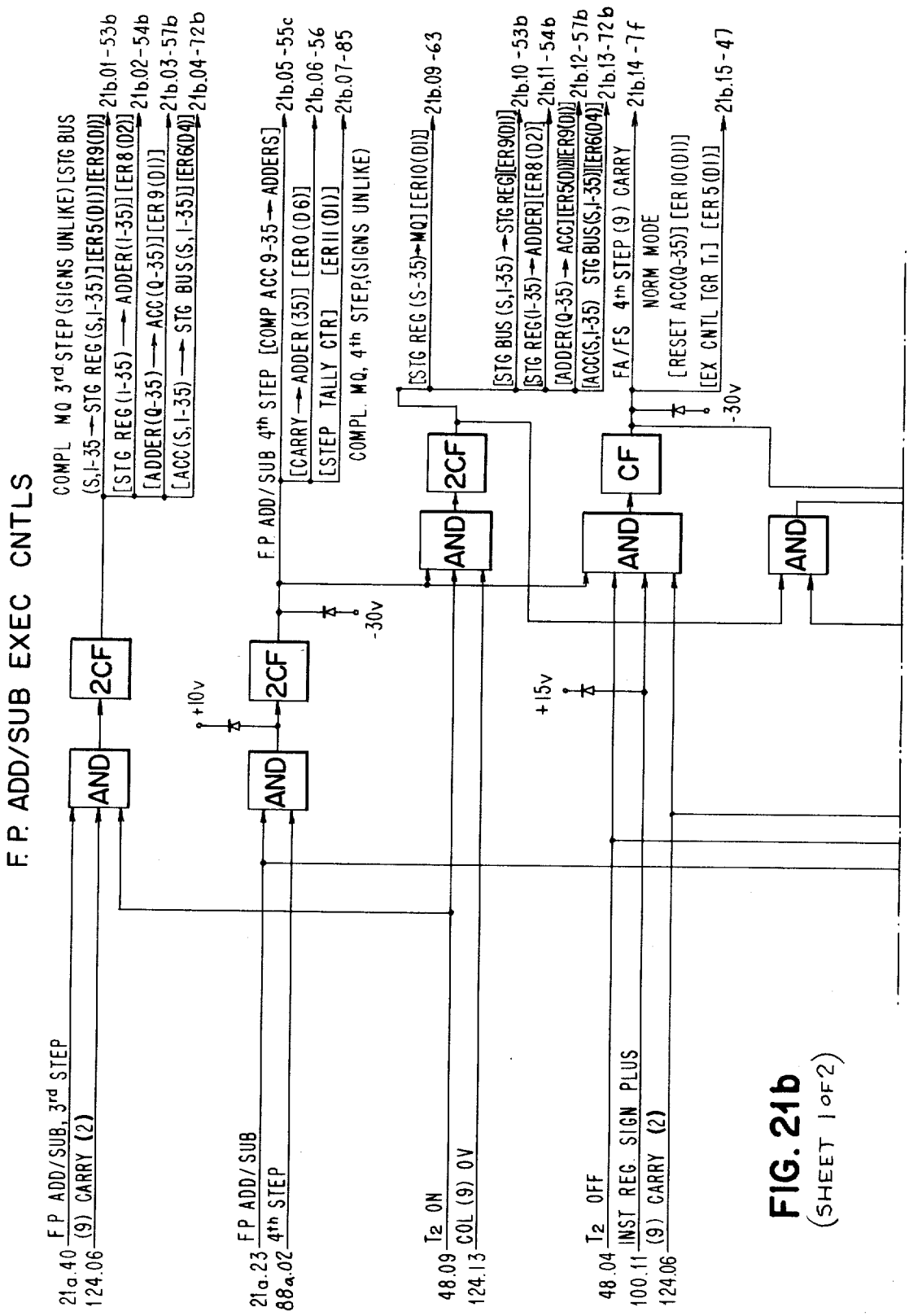


FIG. 21b
(SHEET 1 OF 2)

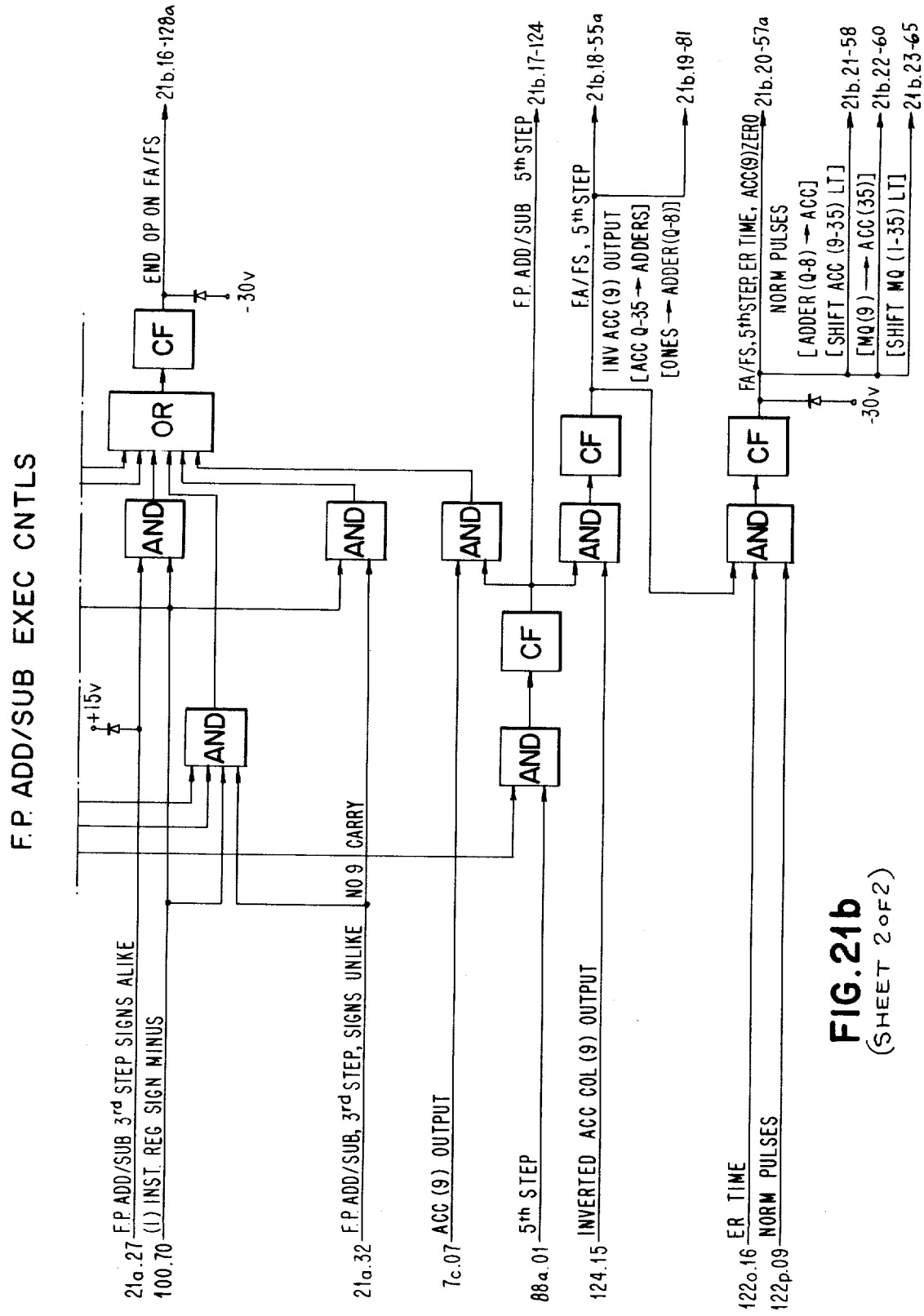


FIG. 21b
(SHEET 2 OF 2)

F P TRAP TGR

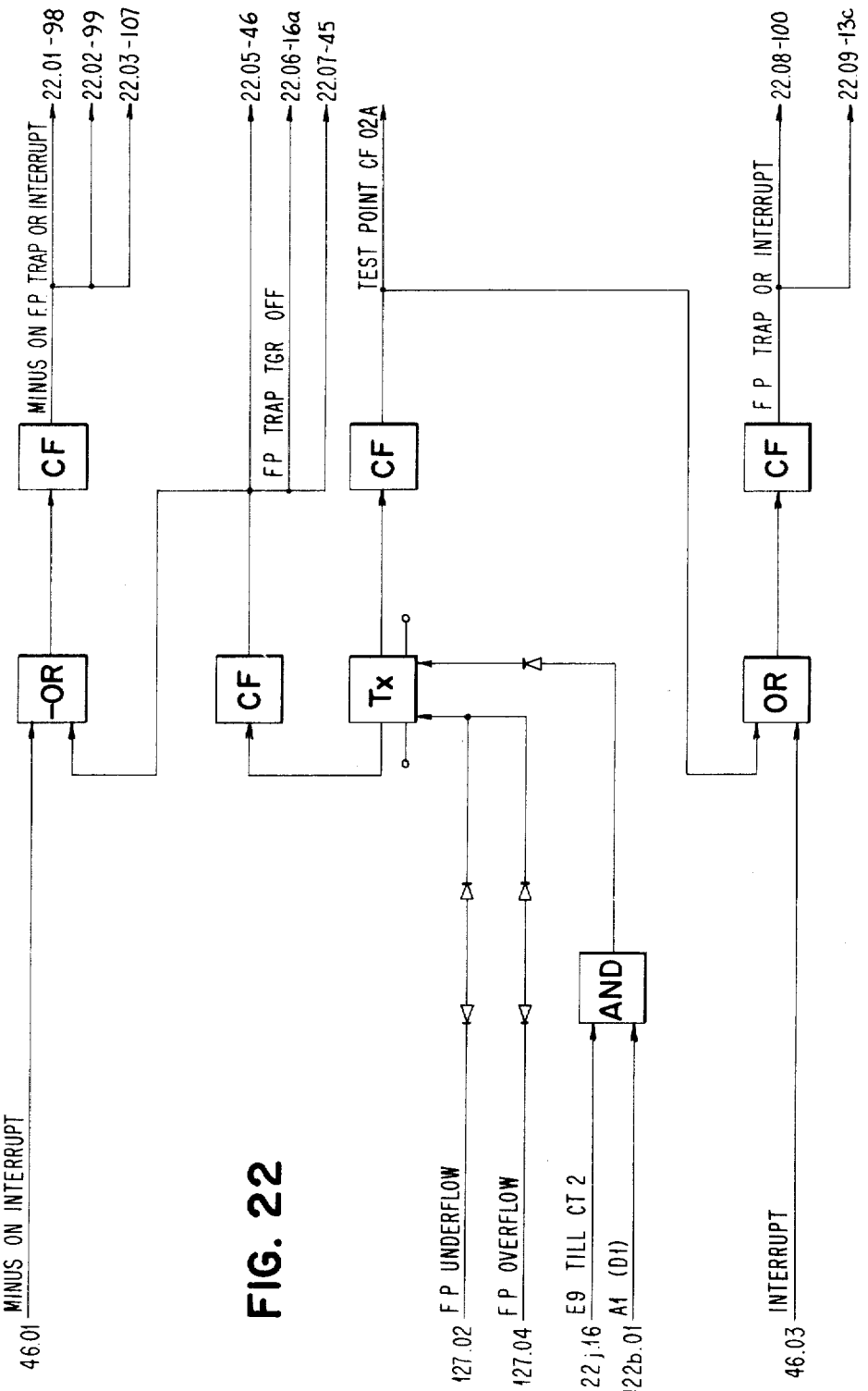


FIG. 22

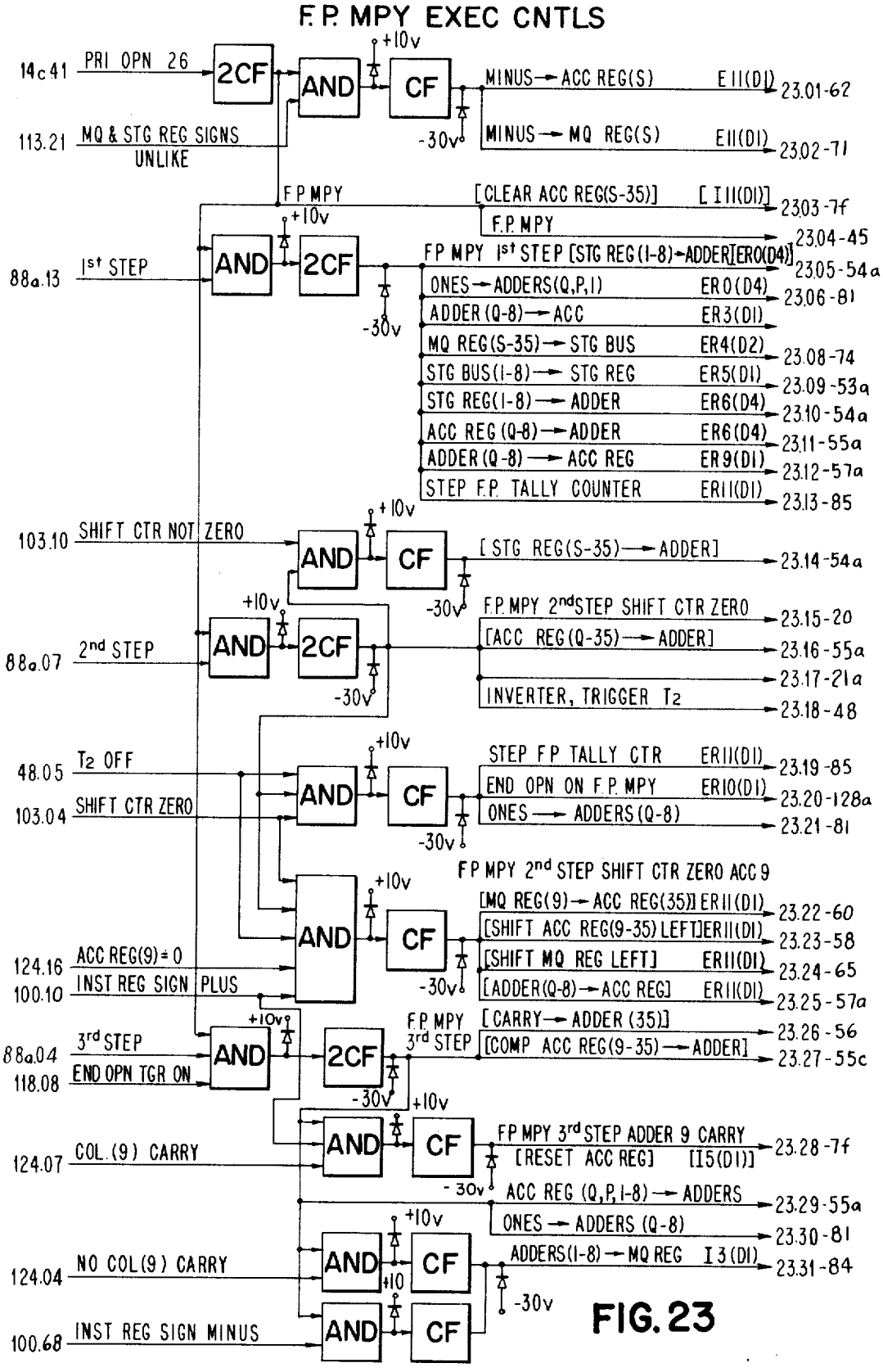

F.P. MPY EXEC CNTLS
14c.41 PRI OPN 26
2CF
AND
+10v
CF
-30v
MINUS → ACC REG(S) E II(DI) 23.01-62
113.21 MQ & STG REG SIGNS UNLIKE
MINUS → MQ REG(S) E II(DI) 23.02-71
F P MPY
[CLEAR ACC REG(S-35)] [I II(DI)] 23.03-7f
F.P. MPY 23.04-45
88a.13 1st STEP
FP MPY 1st STEP [STG REG(1-8)→ADDER][ER0(D4)] 23.05-54a
ONES → ADDERS(Q,P,1) ER0(D4) 23.06-81
ADDER(Q-8) → ACC ER3(DI)
MQ REG(S-35) → STG BUS ER4(D2) 23.08-74
STG BUS(1-8) → STG REG ER5(DI) 23.09-53a
STG REG(1-8) → ADDER ER6(D4) 23.10-54a
ACC REG(Q-8) → ADDER ER6(D4) 23.11-55a
ADDER(Q-8) → ACC REG ER9(DI) 23.12-57a
STEP F.P. TALLY COUNTER ERII(DI) 23.13-85
103.10 SHIFT CTR NOT ZERO
[STG REG(S-35) → ADDER] 23.14-54a
88a.07 2nd STEP
F.P. MPY 2nd STEP SHIFT CTR ZERO 23.15-20
[ACC REG(Q-35) → ADDER] 23.16-55a
23.17-21a
INVERTER, TRIGGER T2 23.18-48
48.05 T2 OFF
103.04 SHIFT CTR ZERO
STEP F.P. TALLY CTR ERII(DI) 23.19-85
END OPN ON F.P. MPY ERI0(DI) 23.20-128a
ONES → ADDERS(Q-8) 23.21-81
FP MPY 2nd STEP SHIFT CTR ZERO ACC 9
[MQ REG(9) → ACC REG(35)] ERII(DI) 23.22-60
[SHIFT ACC REG(9-35) LEFT] ERII(DI) 23.23-58
124.16 ACC REG(9) ≠ 0
100.10 INST REG SIGN PLUS
[SHIFT MQ REG LEFT] ERII(DI) 23.24-65
[ADDER(Q-8) → ACC REG] ERII(DI) 23.25-57a
88a.04 3rd STEP
118.08 END OPN TGR ON
F.P. MPY 3rd STEP
[CARRY → ADDER (35)] 23.26-56
[COMP ACC REG(9-35) → ADDER] 23.27-55c
124.07 COL. (9) CARRY
FP MPY 3rd STEP ADDER 9 CARRY 23.28-7f
[RESET ACC REG] [I5(DI)]
ACC REG (Q,P,1-8) → ADDERS 23.29-55a
ONES → ADDERS (Q-8) 23.30-81
124.04 NO COL(9) CARRY
ADDERS(1-8) → MQ REG I 3(DI) 23.31-84
100.68 INST REG SIGN MINUS

FIG. 23

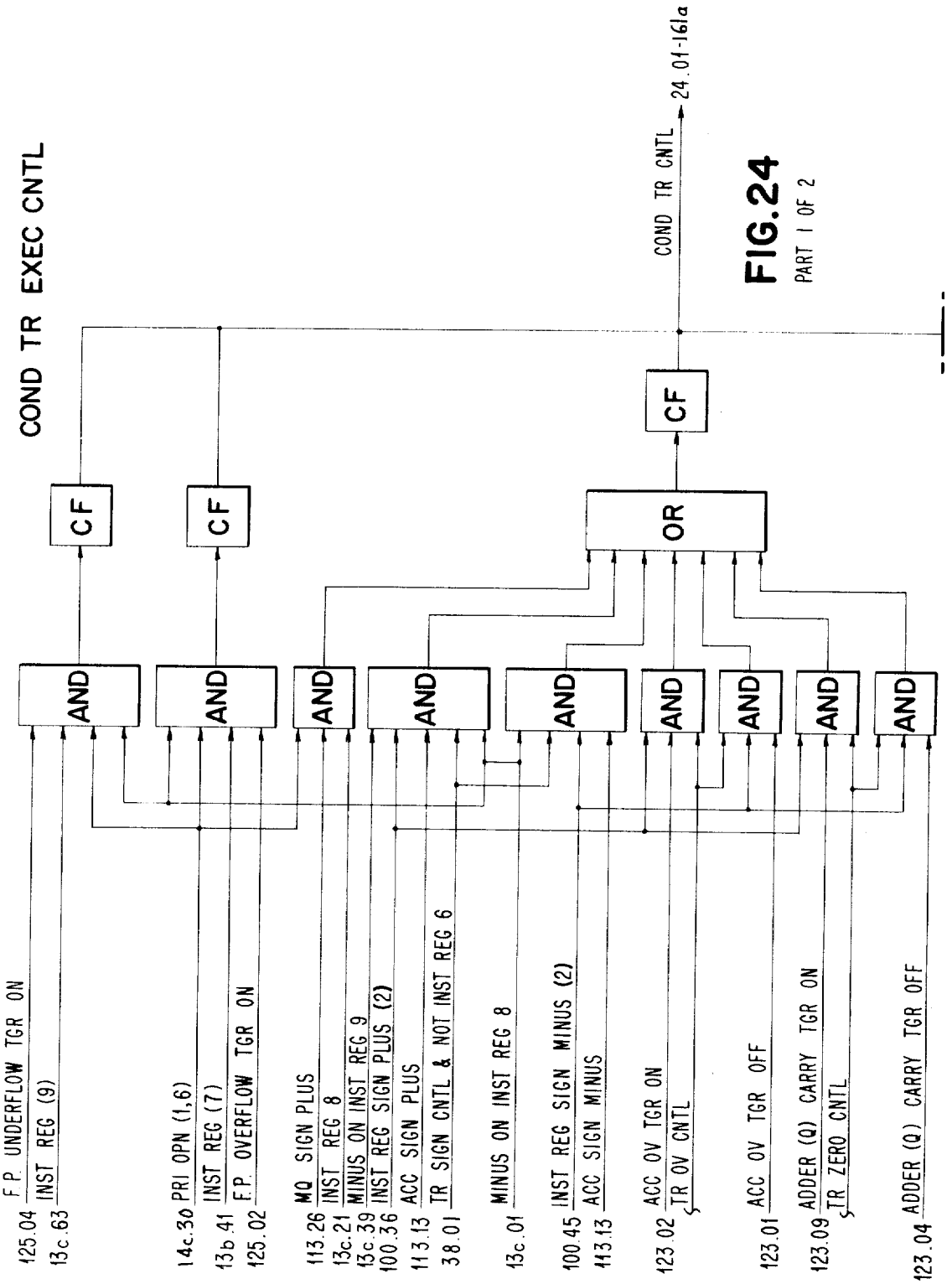


FIG.24

PART 1 OF 2

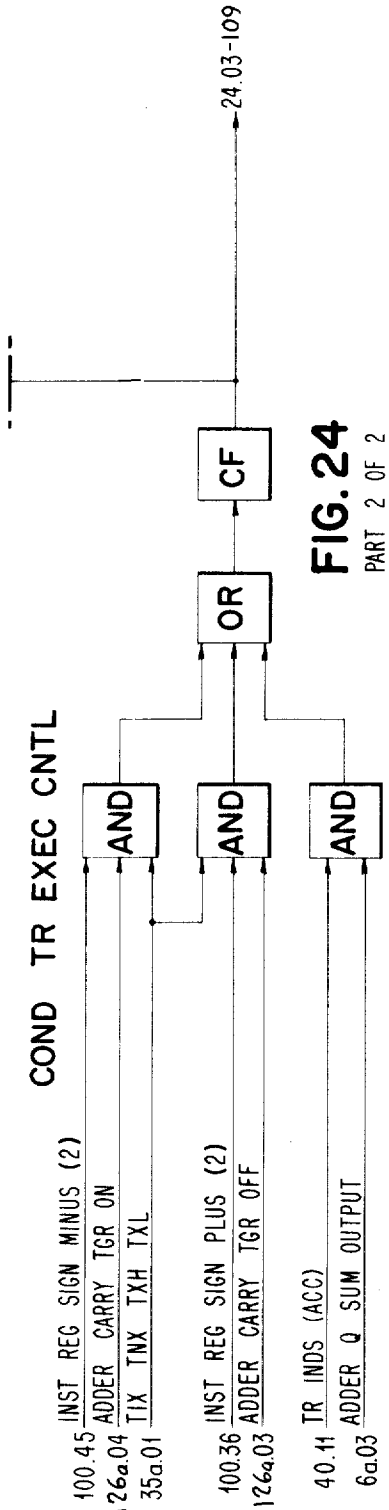


FIG. 24
PART 2 OF 2

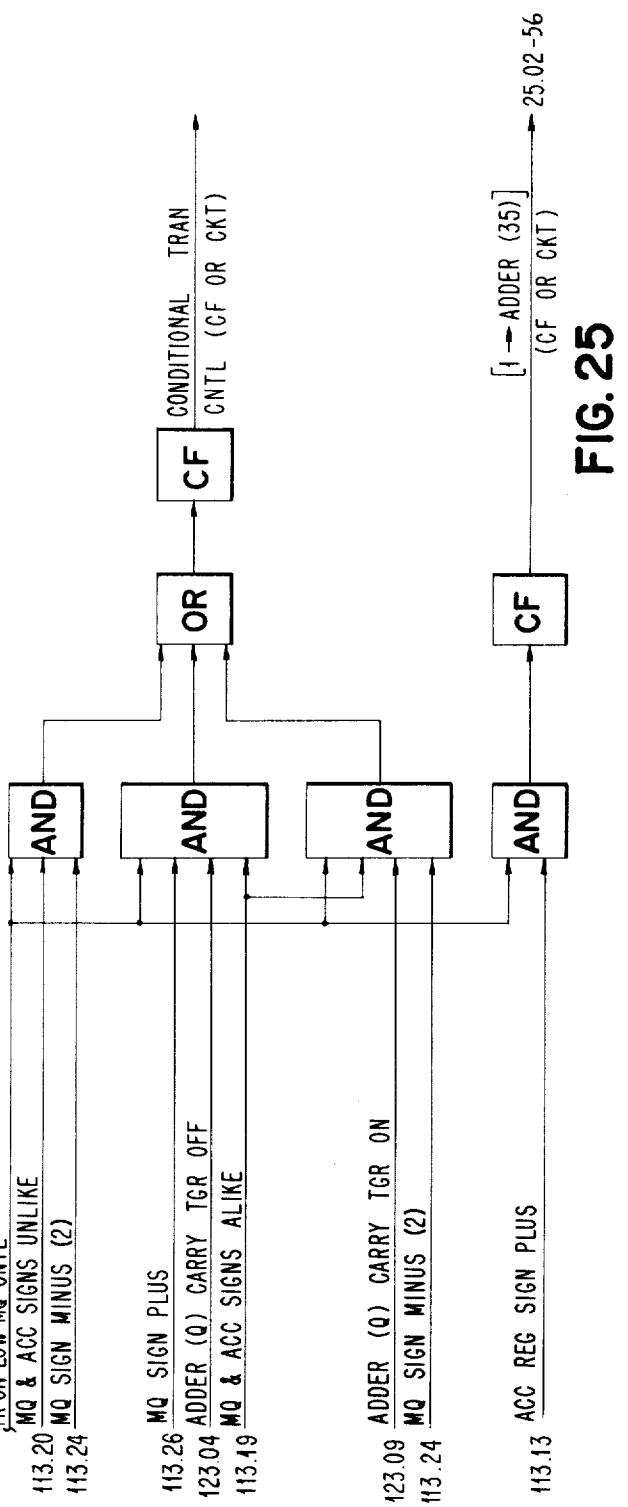
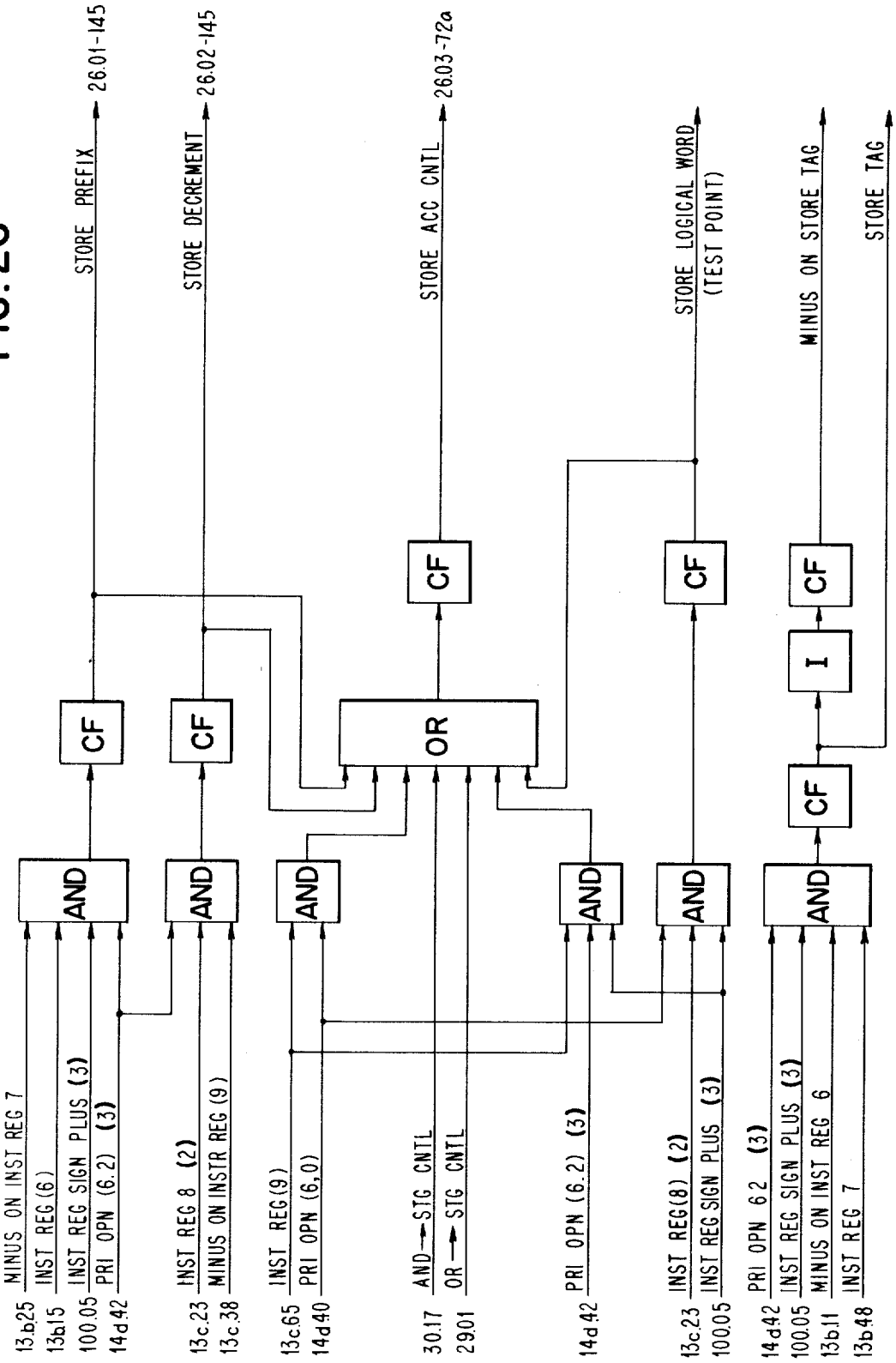
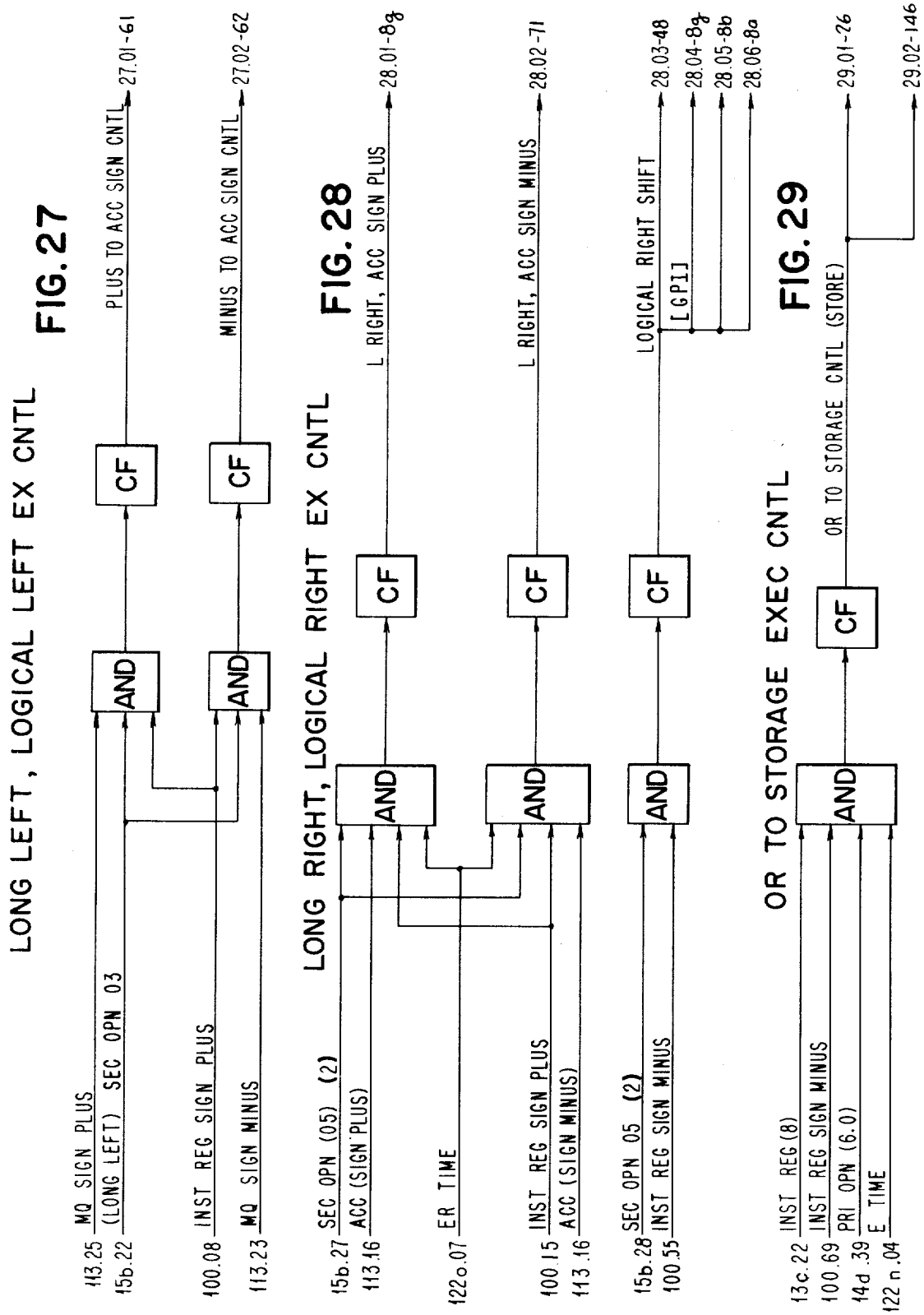


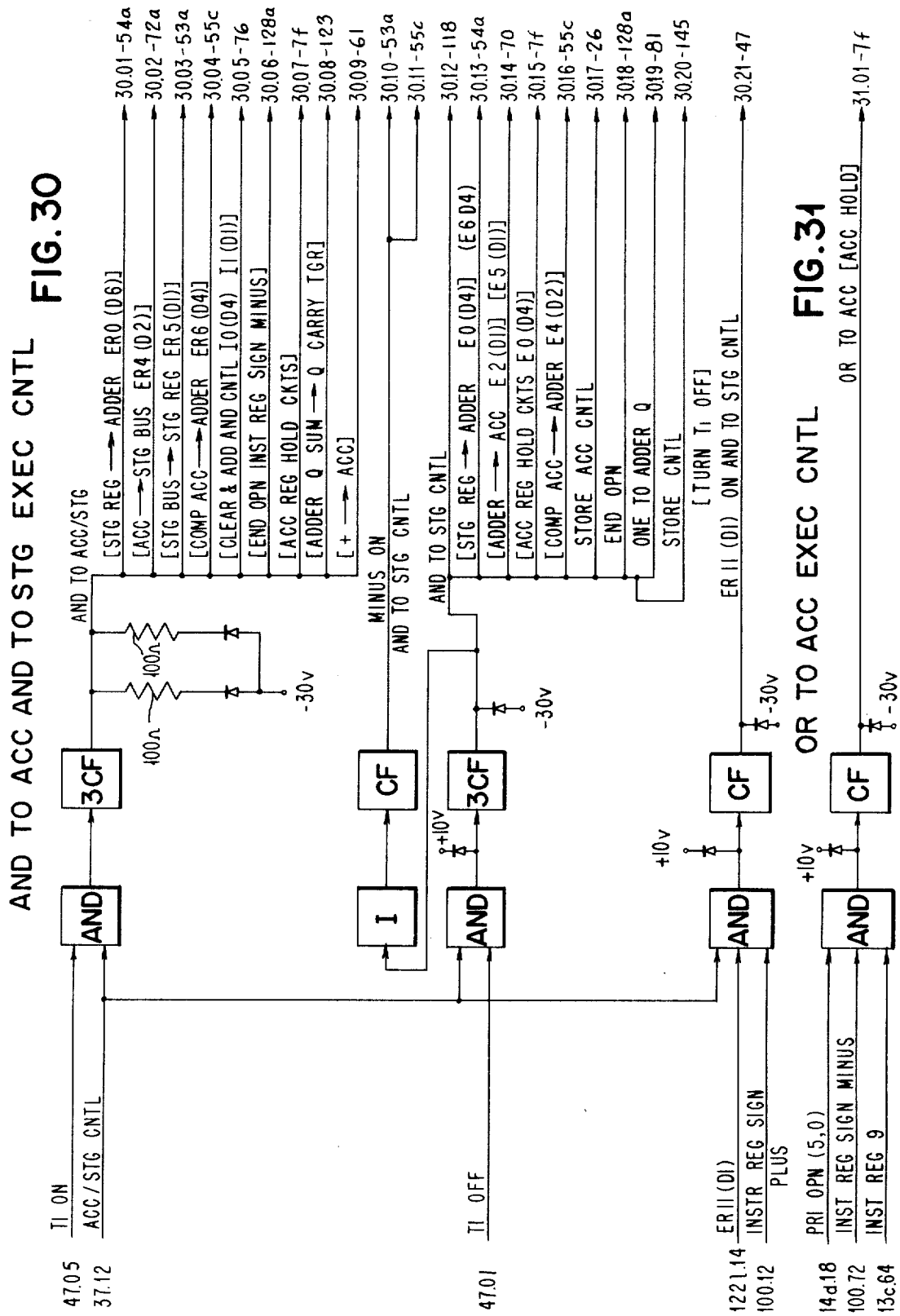
FIG. 25

FIG. 26

STORE EXECUTION CNTL




LONG LEFT, LOGICAL LEFT EX CNTL
FIG. 27
113.25 MQ SIGN PLUS
15b.22 (LONG LEFT) SEC OPN 03
100.08 INST REG SIGN PLUS
113.23 MQ SIGN MINUS
AND
AND
CF
CF
PLUS TO ACC SIGN CNTL
27.01-61
MINUS TO ACC SIGN CNTL
27.02-62
LONG RIGHT, LOGICAL RIGHT EX CNTL
FIG. 28
15b.27 SEC OPN (05) (2)
113.16 ACC (SIGN PLUS)
122o.07 ER TIME
100.15 INST REG SIGN PLUS
113.16 ACC (SIGN MINUS)
15b.28 SEC OPN 05 (2)
100.55 INST REG SIGN MINUS
AND
AND
AND
CF
CF
CF
L RIGHT, ACC SIGN PLUS
28.01-8g
L RIGHT, ACC SIGN MINUS
28.02-71
LOGICAL RIGHT SHIFT
28.03-48
[GP1]
28.04-8g
28.05-8b
28.06-8a
OR TO STORAGE EXEC CNTL
FIG. 29
13c.22 INST REG (8)
100.69 INST REG SIGN MINUS
14d.39 PRI OPN (6.0)
122 n.04 E TIME
AND
CF
OR TO STORAGE CNTL (STORE)
29.01-26
29.02-146


AND TO ACC AND TO STG EXEC CNTL
FIG. 30
AND TO ACC/STG
[STG REG → ADDER ERO (D6)]
[ACC → STG BUS ER4 (D2)]
[STG BUS → STG REG ER5(DI)]
[COMP ACC → ADDER ER6 (D4)]
[CLEAR & ADD AND CNTL IO(D4) II(DI)]
[END OPN INST REG SIGN MINUS]
[ACC REG HOLD CKTS]
[ADDER Q SUM → Q CARRY TGR]
[+ → ACC]
30.01-54a
30.02-72a
30.03-53a
30.04-55c
30.05-76
30.06-128a
30.07-7f
30.08-123
30.09-61
MINUS ON
AND TO STG CNTL
30.10-53a
30.11-55c
AND TO STG CNTL
[STG REG → ADDER E0(D4)] (E6 D4)
[ADDER → ACC E2(DI)] [E5(DI)]
[ACC REG HOLD CKTS E0(D4)]
[COMP ACC → ADDER E4(D2)]
STORE ACC CNTL
END OPN
ONE TO ADDER Q
STORE CNTL
[TURN TI OFF]
ER II (DI) ON AND TO STG CNTL
30.12-118
30.13-54a
30.14-70
30.15-7f
30.16-55c
30.17-26
30.18-128a
30.19-81
30.20-145
30.21-47
100Ω
100Ω
-30v
-30v
-30v
-30v
+10v
+10v
+10v
3CF
3CF
CF
CF
CF
AND
AND
AND
AND
I
TI ON
ACC/STG CNTL
TI OFF
ER II (DI)
INSTR REG SIGN
PLUS
PRI OPN (5,0)
INST REG SIGN MINUS
INST REG 9
47.05
37.12
47.01
122 1.14
100.12
14a.18
100.72
13c.64
FIG. 31
OR TO ACC EXEC CNTL
OR TO ACC [ACC HOLD]
31.01-7f

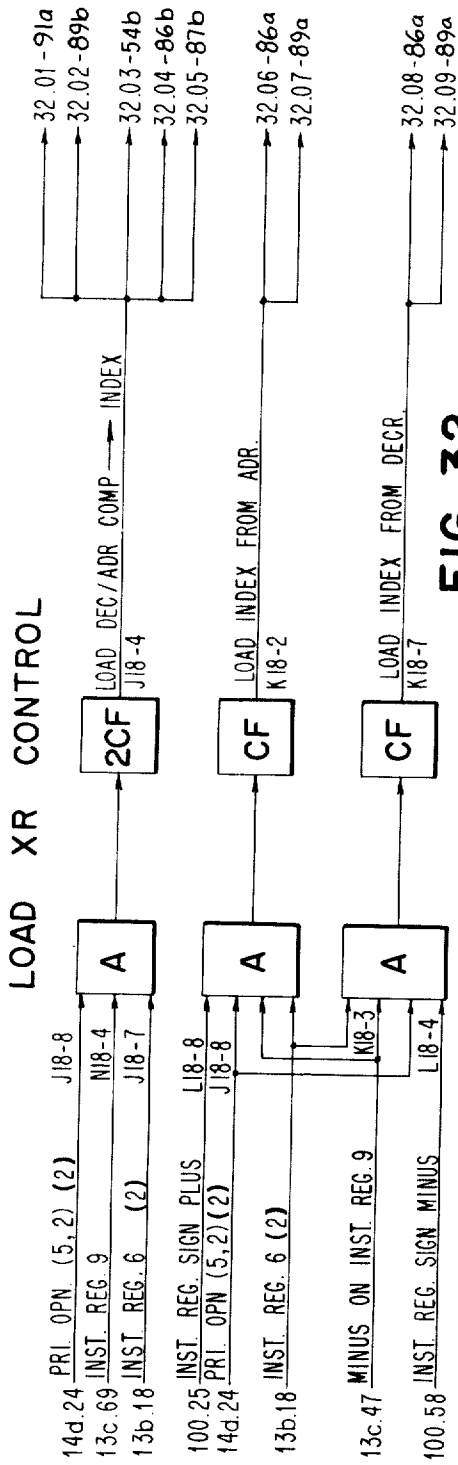

LOAD XR CONTROL
14d.24 PRI. OPN (5,2) (2) J18-8
13c.69 INST. REG. 9 N18-4
13b.18 INST. REG. 6 (2) J18-7
A
2CF
LOAD DEC/ADR COMP → INDEX
J18-4
32.01-91a
32.02-89b
32.03-54b
32.04-86b
32.05-87b
100.25 INST. REG. SIGN PLUS L18-8
14d.24 PRI. OPN (5,2)(2) J18-8
13b.18 INST. REG. 6 (2)
A
CF
LOAD INDEX FROM ADR.
K18-2
32.06-86a
32.07-89a
13c.47 MINUS ON INST. REG. 9 K18-3
100.58 INST. REG. SIGN MINUS L18-4
A
CF
LOAD INDEX FROM DECR.
K18-7
32.08-86a
32.09-89a

FIG. 32

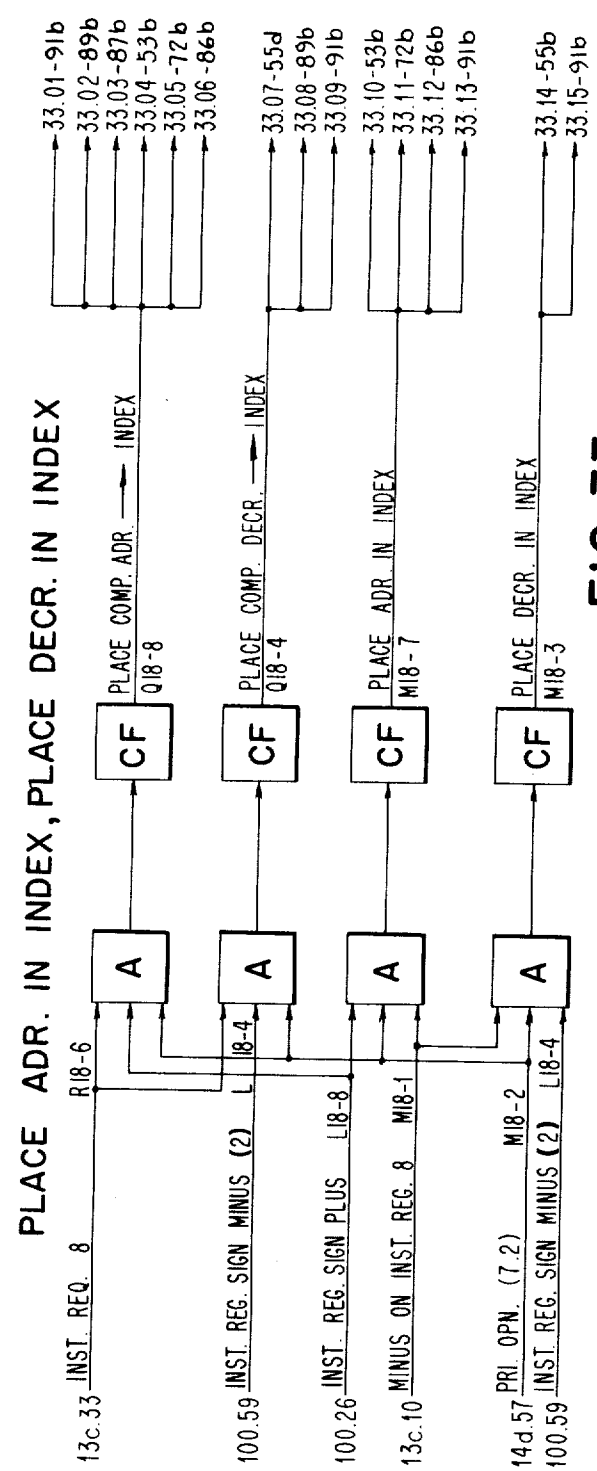

PLACE ADR. IN INDEX, PLACE DECR. IN INDEX
13c.33 INST. REQ. 8 R18-6
A
CF
PLACE COMP. ADR. → INDEX
Q18-8
33.01-91b
33.02-89b
33.03-87b
33.04-53b
33.05-72b
33.06-86b
100.59 INST. REG. SIGN MINUS (2) L 18-4
A
CF
PLACE COMP. DECR. → INDEX
Q18-4
33.07-55d
33.08-89b
33.09-91b
100.26 INST. REG. SIGN PLUS L18-8
13c.10 MINUS ON INST. REG. 8 M18-1
A
CF
PLACE ADR. IN INDEX
M18-7
33.10-53b
33.11-72b
33.12-86b
33.13-91b
14d.57 PRI. OPN. (7.2) M18-2
100.59 INST. REG. SIGN MINUS (2) L18-4
A
CF
PLACE DECR. IN INDEX
M18-3
33.14-55b
33.15-91b

FIG. 33

TRANSFER WITH INDEX RAISE EX. CNTL.

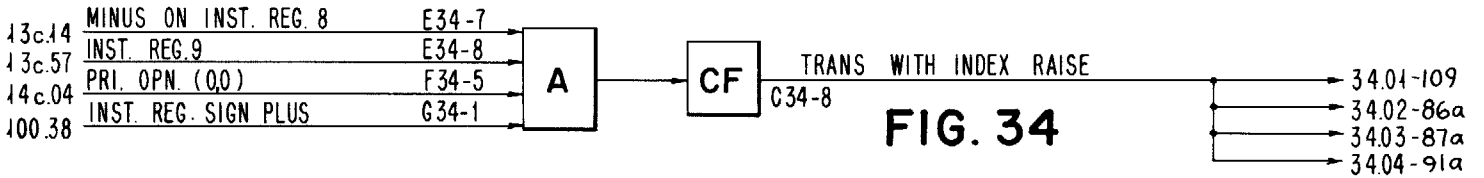


FIG. 34

INDEXING EXECUTION CONTROL

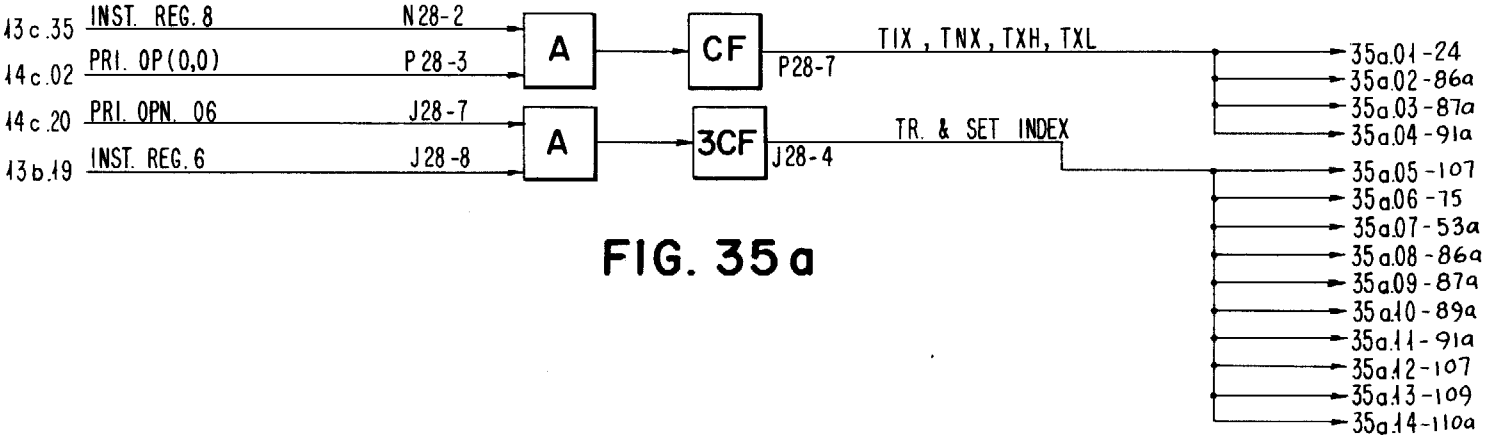


FIG. 35a

INDEXING EXECUTION CONTROL

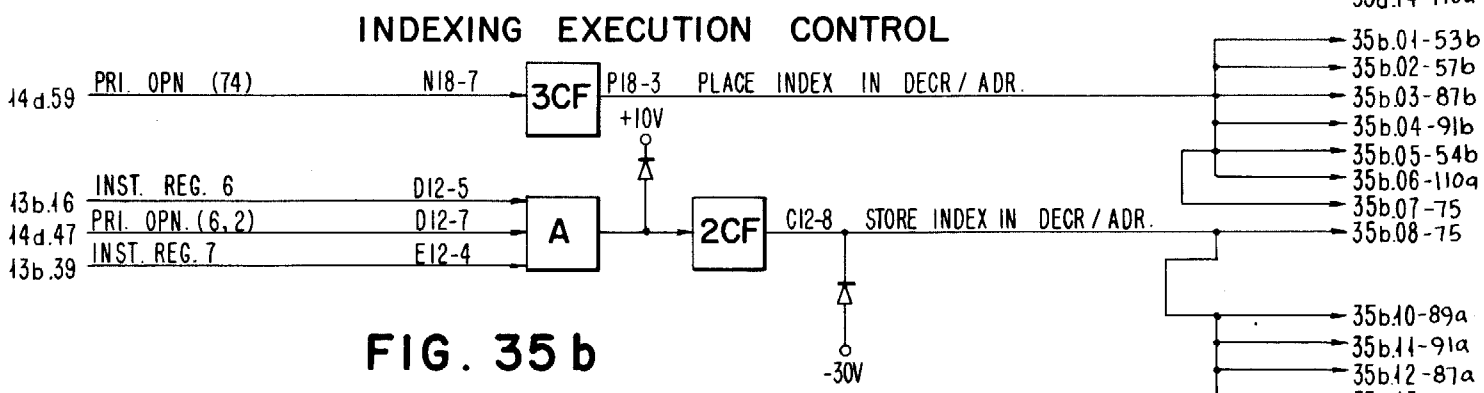
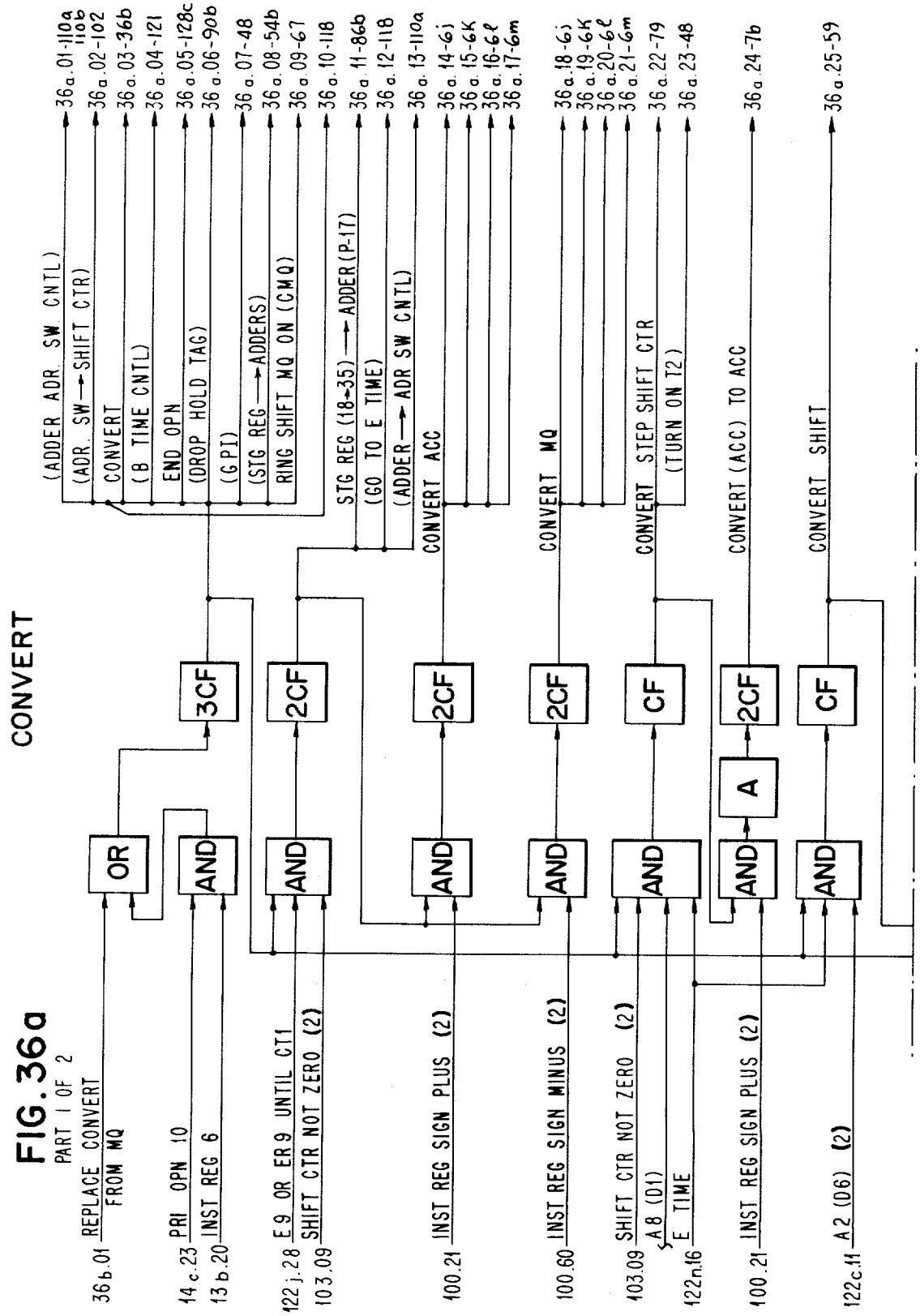


FIG. 35b


CONVERT
FIG. 36a
PART 1 OF 2
36b.01 REPLACE CONVERT FROM MQ
14 c.23 PRI OPN 10
13 b.20 INST REG 6
122 j.28 E 9 OR ER 9 UNTIL CT1
103.09 SHIFT CTR NOT ZERO (2)
100.21 INST REG SIGN PLUS (2)
100.60 INST REG SIGN MINUS (2)
103.09 SHIFT CTR NOT ZERO (2)
A 8 (D1)
E TIME
122n.16
100.21 INST REG SIGN PLUS (2)
122c.11 A 2 (06) (2)
OR
AND
3CF
2CF
CF
A
(ADDER ADR SW CNTL)
(ADR. SW → SHIFT CTR)
CONVERT
(B TIME CNTL)
END OPN
(DROP HOLD TAG)
(GPI)
(STG REG → ADDERS)
RING SHIFT MQ ON (CMQ)
STG REG (18-35) → ADDER (P-17)
(GO TO E TIME)
(ADDER → ADR SW CNTL)
CONVERT ACC
CONVERT MQ
CONVERT STEP SHIFT CTR
(TURN ON T2)
CONVERT (ACC) TO ACC
CONVERT SHIFT
36a.01-110a 110b
36a.02-102
36a.03-36b
36a.04-121
36a.05-128c
36a.06-90b
36a.07-48
36a.08-54b
36a.09-67
36a.10-118
36a.11-86b
36a.12-118
36a.13-110a
36a.14-6j
36a.15-6K
36a.16-6ℓ
36a.17-6m
36a.18-6j
36a.19-6K
36a.20-6ℓ
36a.21-6m
36a.22-79
36a.23-48
36a.24-7b
36a.25-59

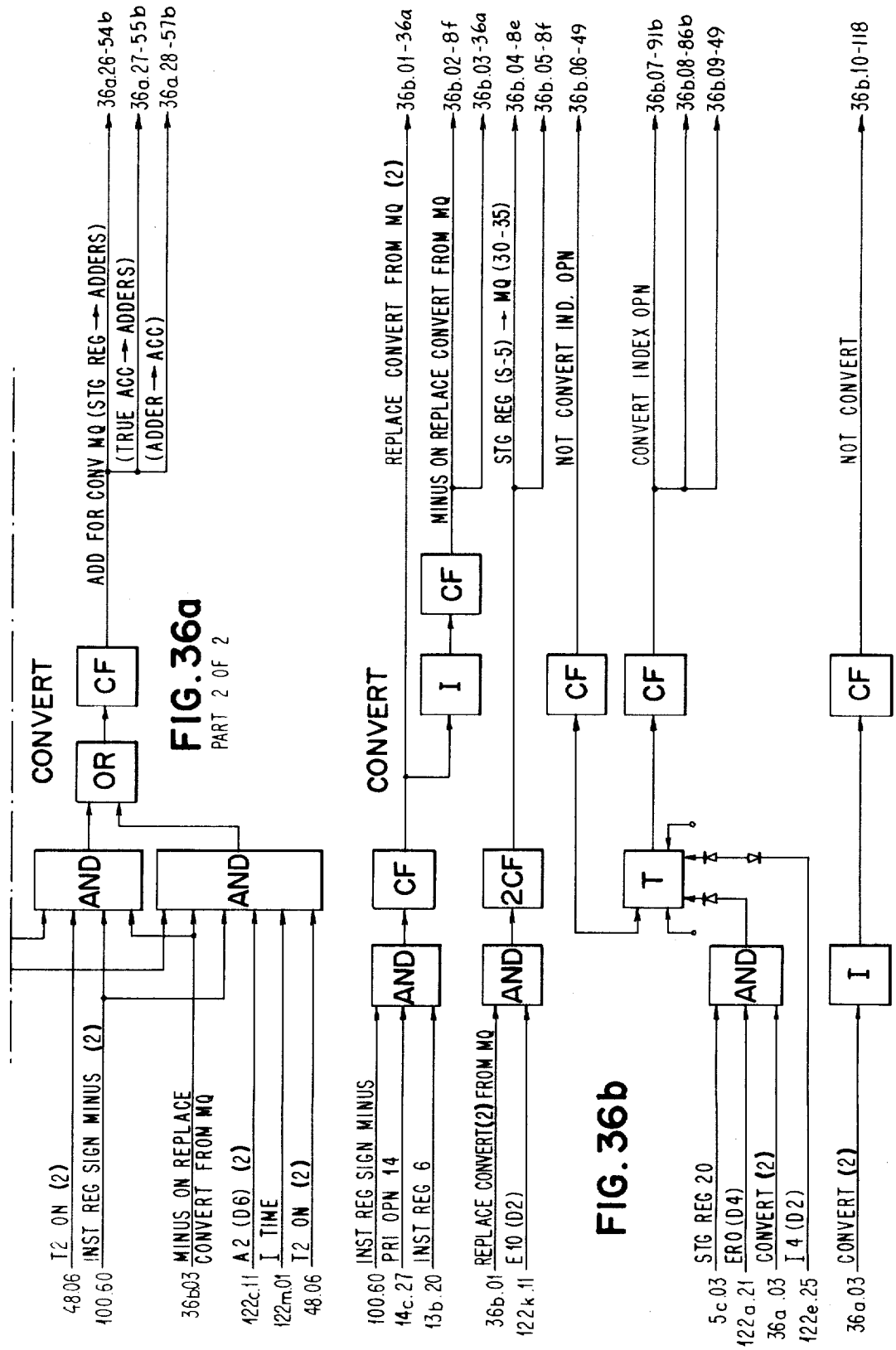
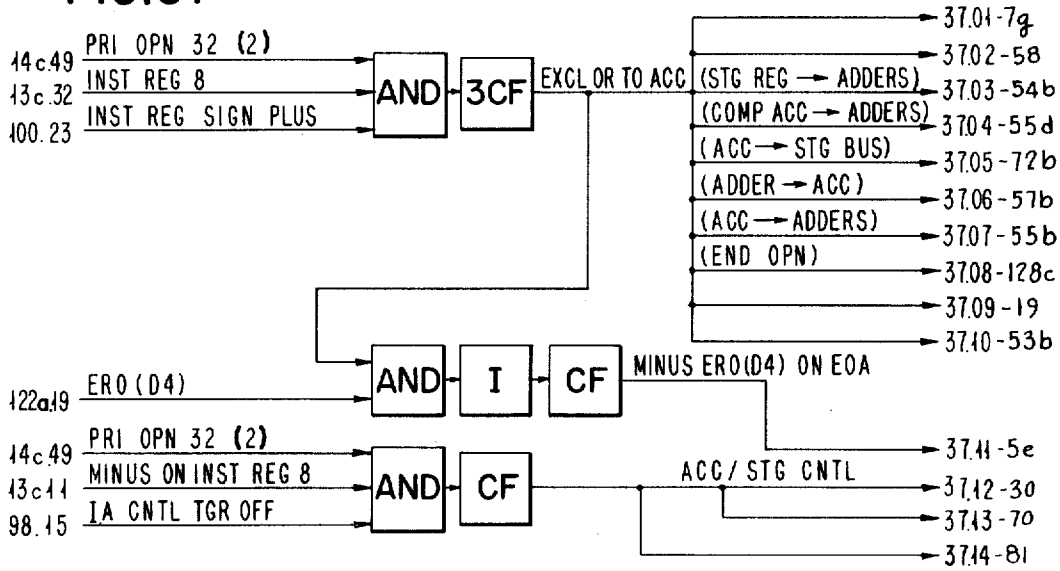


FIG. 36a
PART 2 OF 2

FIG. 36b

FIG.37 EXCLUSIVE OR TO ACC



EXCHANGE, TRANSFER SIGN CONTROL

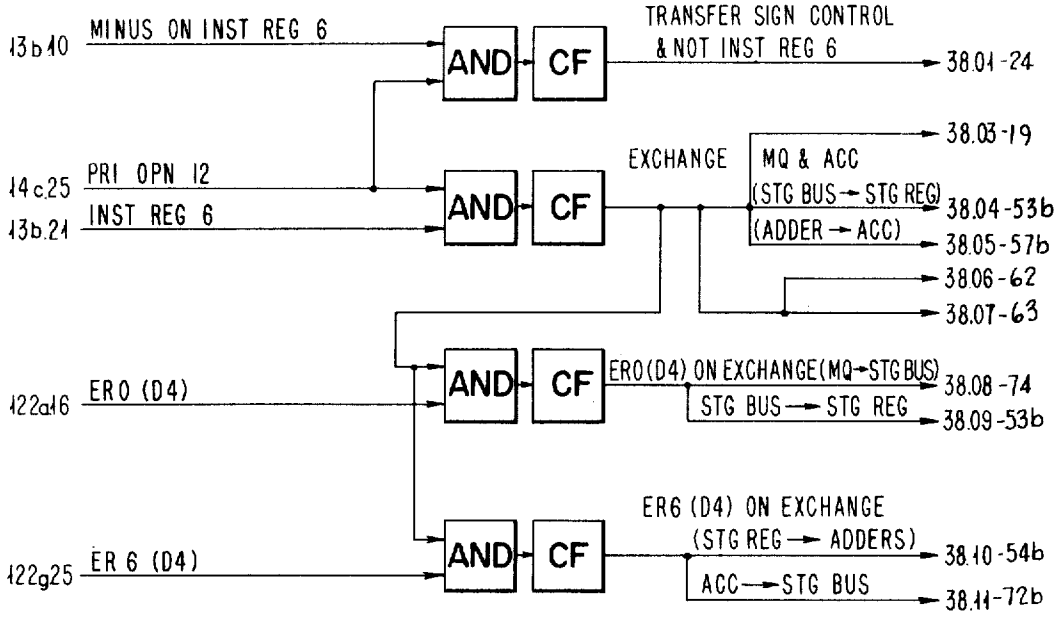
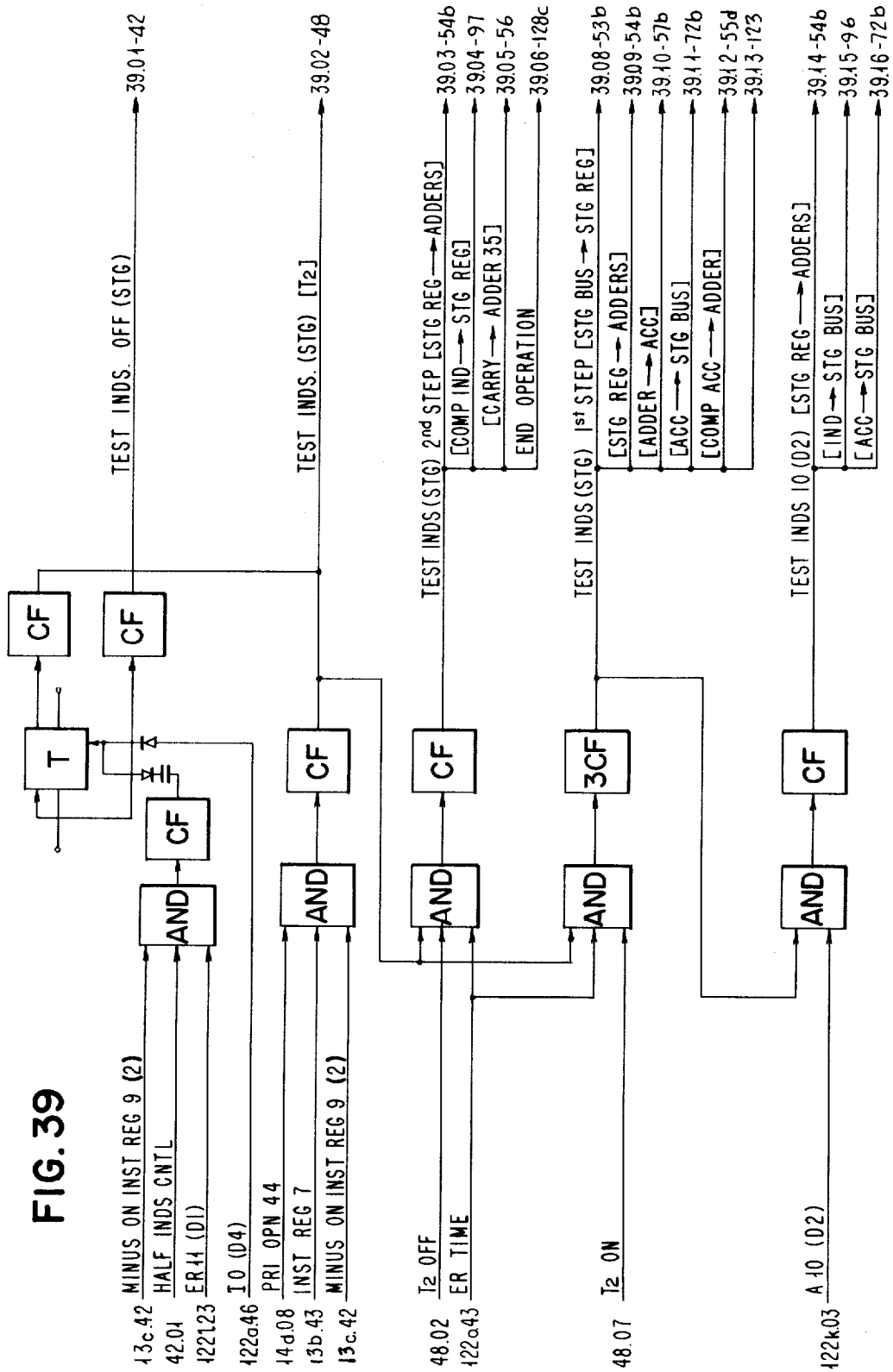


FIG. 38

TEST INDICATORS (STORAGE) HALF TEST INDICATORS

FIG. 39



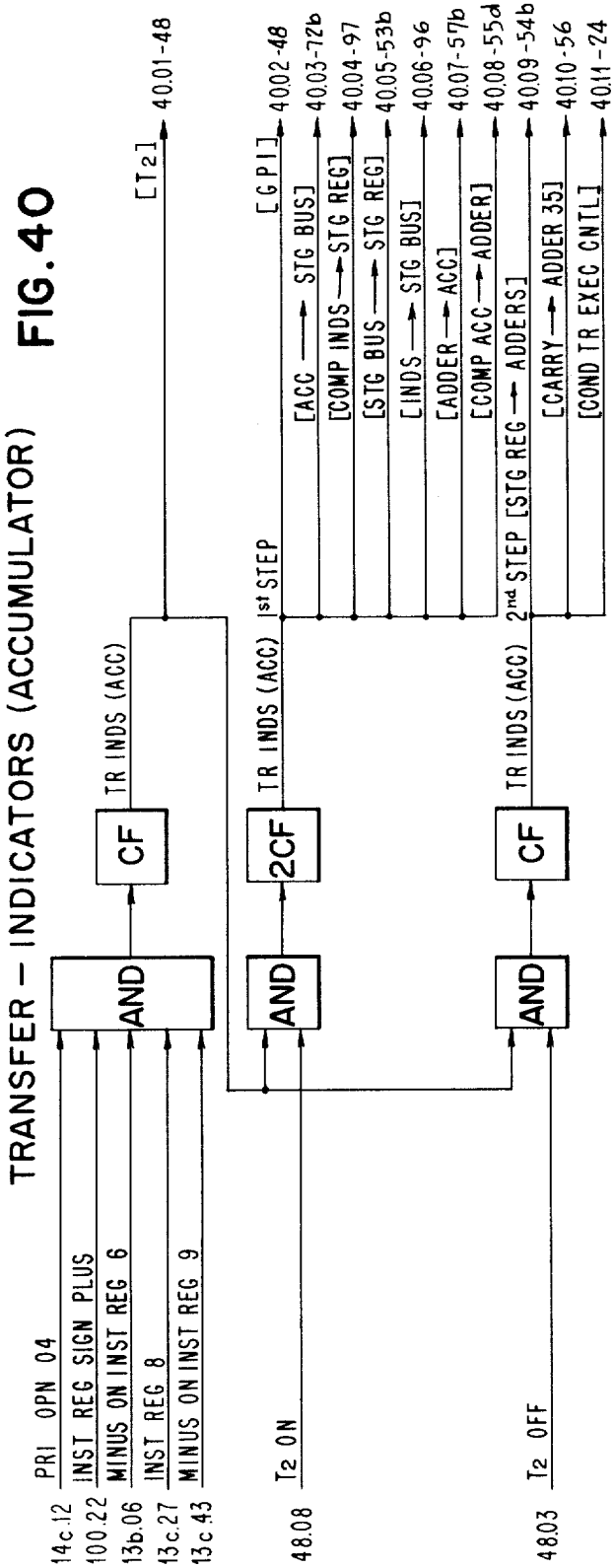

TRANSFER – INDICATORS (ACCUMULATOR)
PRI OPN 04
INST REG SIGN PLUS
MINUS ON INST REG 6
INST REG 8
MINUS ON INST REG 9
14c.12
100.22
13b.06
13c.27
13c.43
AND
CF
TR INDS (ACC)
[T2]
40.01-48
T2 ON
48.08
AND
2CF
TR INDS (ACC)
1st STEP
[G P I]
40.02-48
[ACC → STG BUS]
40.03-72b
[COMP INDS → STG REG]
40.04-97
[STG BUS → STG REG]
40.05-53b
[INDS → STG BUS]
40.06-96
[ADDER → ACC]
40.07-57b
[COMP ACC → ADDER]
40.08-55d
T2 OFF
48.03
AND
CF
TR INDS (ACC)
2nd STEP [STG REG → ADDERS]
40.09-54b
[CARRY → ADDER 35]
40.10-56
[COND TR EXEC CNTL]
40.11-24

FIG. 40

PLACE INDICATORS IN ACCUMULATOR
RESET INDICATORS FROM ACCUMULATOR
PRI OPN 04 (2)
INST REG SIGN MINUS (2)
MINUS ON INST REG 6 (2)
INST REG 7
MINUS ON INST REG 9
14c.16
100.64
13b.07
13b44
13c.44
AND
CF
PLACE INDS → ACC [STG BUS → STG REG]
41.01-53b
[INDS → STG BUS]
41.02-96
STG REG → ADDERS
41.03-54b
[ADDERS → ACC]
41.04-57b
[PLUS TO ACC REG SIGN]
41.05-19
PRI OPN 04 (2)
MINUS ON INST REG 6 (2)
MINUS ON INST REG 7
INST REG SIGN MINUS (2)
14c.16
13b.07
13b44
100.64
AND
CF
RESET INDS (ACC) [STG BUS → STG REG]
41.06-53b
[ACC → STG BUS]
41.07-72b
[RESET INDS]
41.08-93

FIG. 41

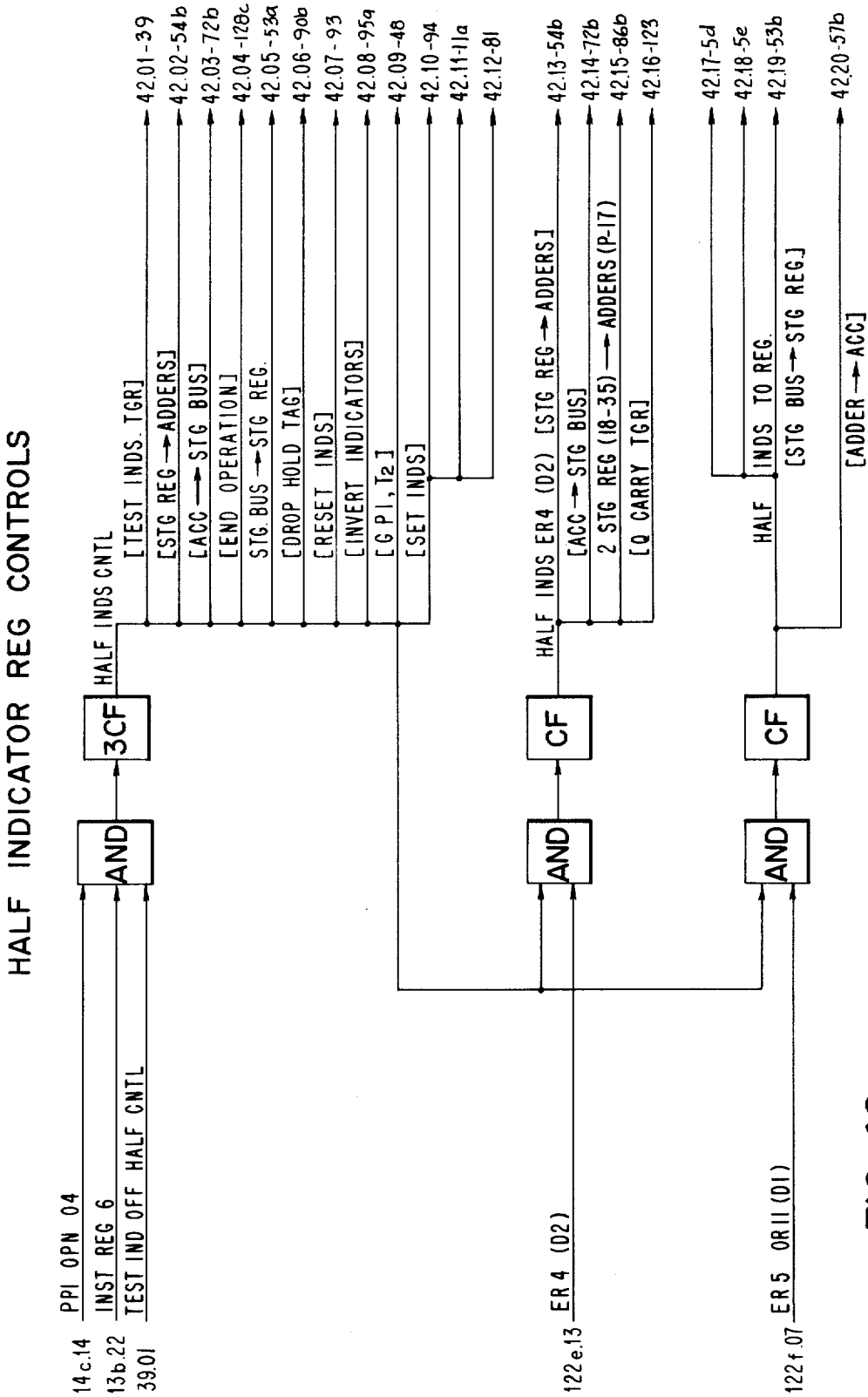

HALF INDICATOR REG CONTROLS
14 c.14 PPI OPN 04
13b.22 INST REG 6
39.01 TEST IND OFF HALF CNTL
AND
3CF
HALF INDS CNTL
[TEST INDS. TGR]
[STG REG → ADDERS]
[ACC → STG BUS]
[END OPERATION]
STG. BUS → STG REG.
[DROP HOLD TAG]
[RESET INDS]
[INVERT INDICATORS]
[G P1, T2]
[SET INDS]
42.01-39
42.02-54b
42.03-72b
42.04-128c
42.05-53a
42.06-90b
42.07-93
42.08-95a
42.09-48
42.10-94
42.11-11a
42.12-81
122 e.13 ER 4 (02)
AND
CF
HALF INDS ER4 (02) [STG REG → ADDERS]
[ACC → STG BUS]
2 STG REG (18-35) → ADDERS (P-17)
[Q CARRY TGR]
42.13-54b
42.14-72b
42.15-86b
42.16-123
122 f 07 ER 5 OR 11 (01)
AND
CF
HALF INDS TO REG.
[STG BUS → STG REG.]
[ADDER → ACC]
42.17-5d
42.18-5e
42.19-53b
42.20-57b

FIG. 42

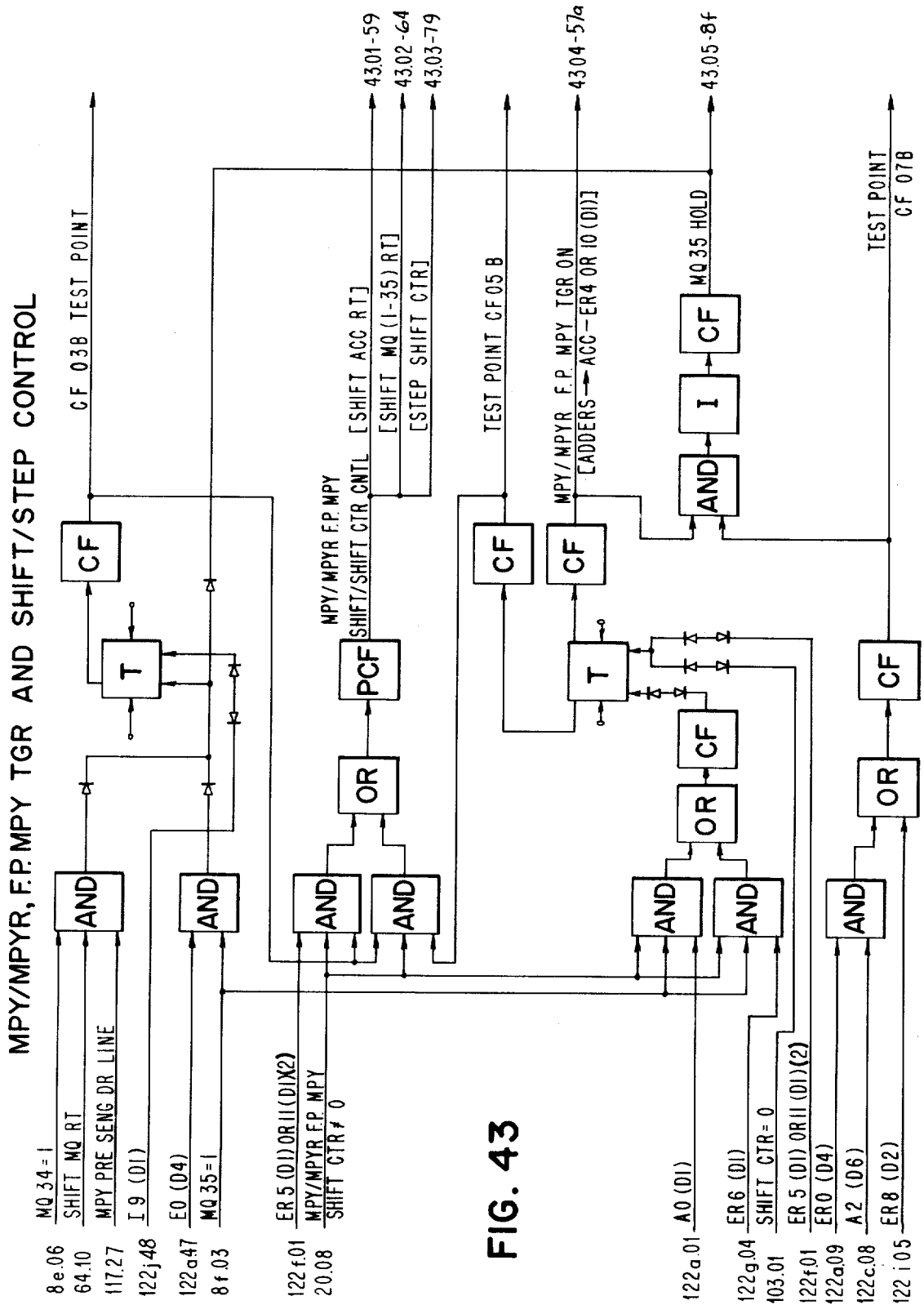
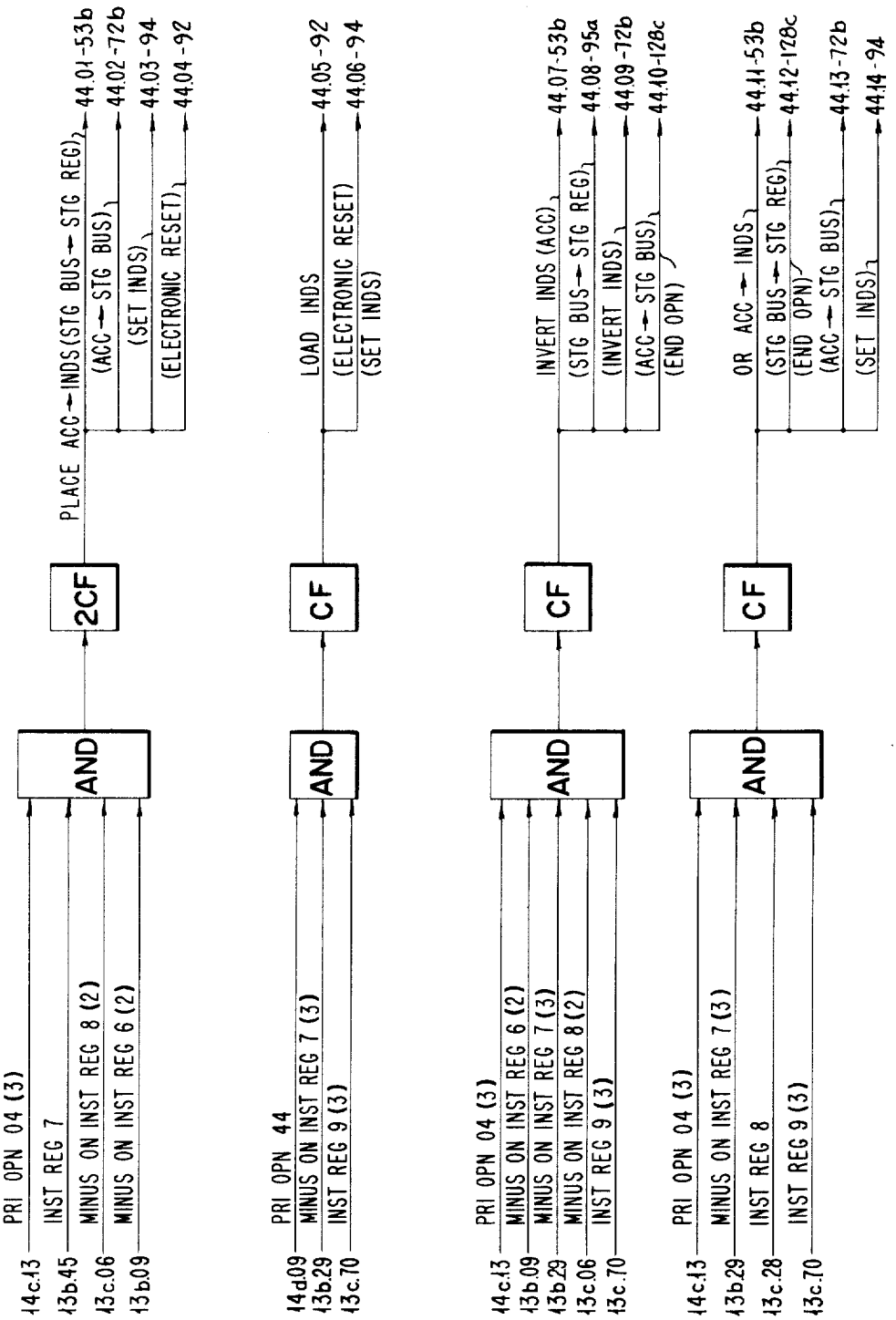

MPY/MPYR, F.P. MPY TGR AND SHIFT/STEP CONTROL
8e.06 MQ 34=1
64.10 SHIFT MQ RT
117.27 MPY PRE SEND OR LINE
122j48 I 9 (D1)
122a47 E0 (D4)
8f.03 MQ 35=1
122f.01 ER 5 (D1) OR II (D1X2)
20.08 MPY/MPYR F.P. MPY SHIFT CTR ≠ 0
122a.01 A0 (D1)
122g.04 ER6 (D1)
103.01 SHIFT CTR=0
122f.01 ER 5 (D1) OR II (D1)(2)
122a.09 ER0 (D4)
122c.08 A2 (D6)
122 i 05 ER8 (D2)
AND
OR
CF
T
PCF
I
MPY/MPYR F.P. MPY SHIFT/SHIFT CTR CNTL
[SHIFT ACC RT]
[SHIFT MQ (1-35) RT]
[STEP SHIFT CTR]
43.01-59
43.02-64
43.03-79
CF 03B TEST POINT
TEST POINT CF 05 B
MPY/MPYR F.P. MPY TGR ON
[ADDERS → ACC-ER4 OR 10 (D1)]
43.04-57a
MQ 35 HOLD
43.05-8f
TEST POINT
CF 07B

FIG. 43

FIG. 44a

PLACE ACCUMULATOR IN INDICATORS
LOAD INDICATORS, INVERT INDICATORS,
OR ACCUMULATOR TO INDICATORS



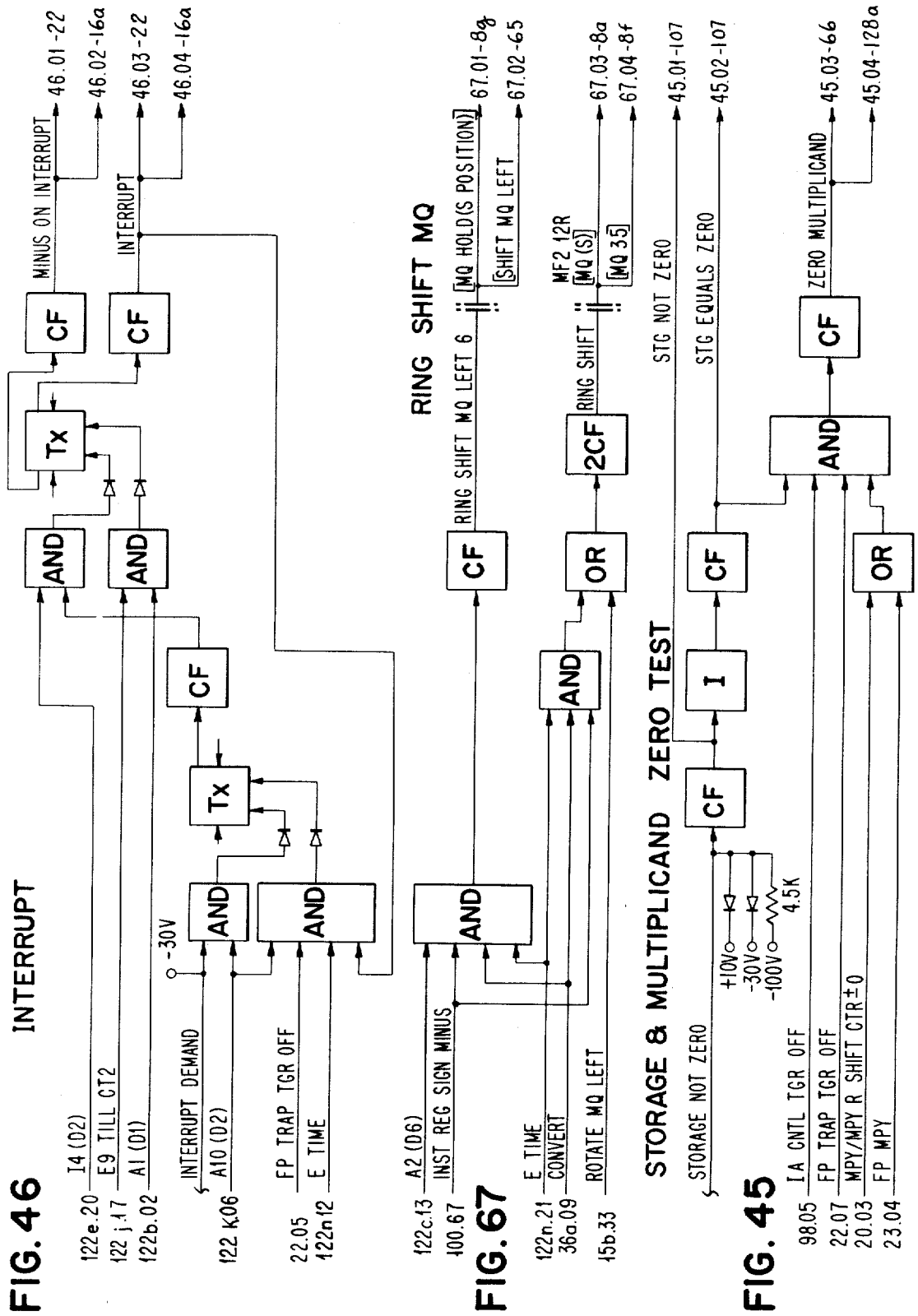


FIG. 46

FIG. 67

FIG. 45

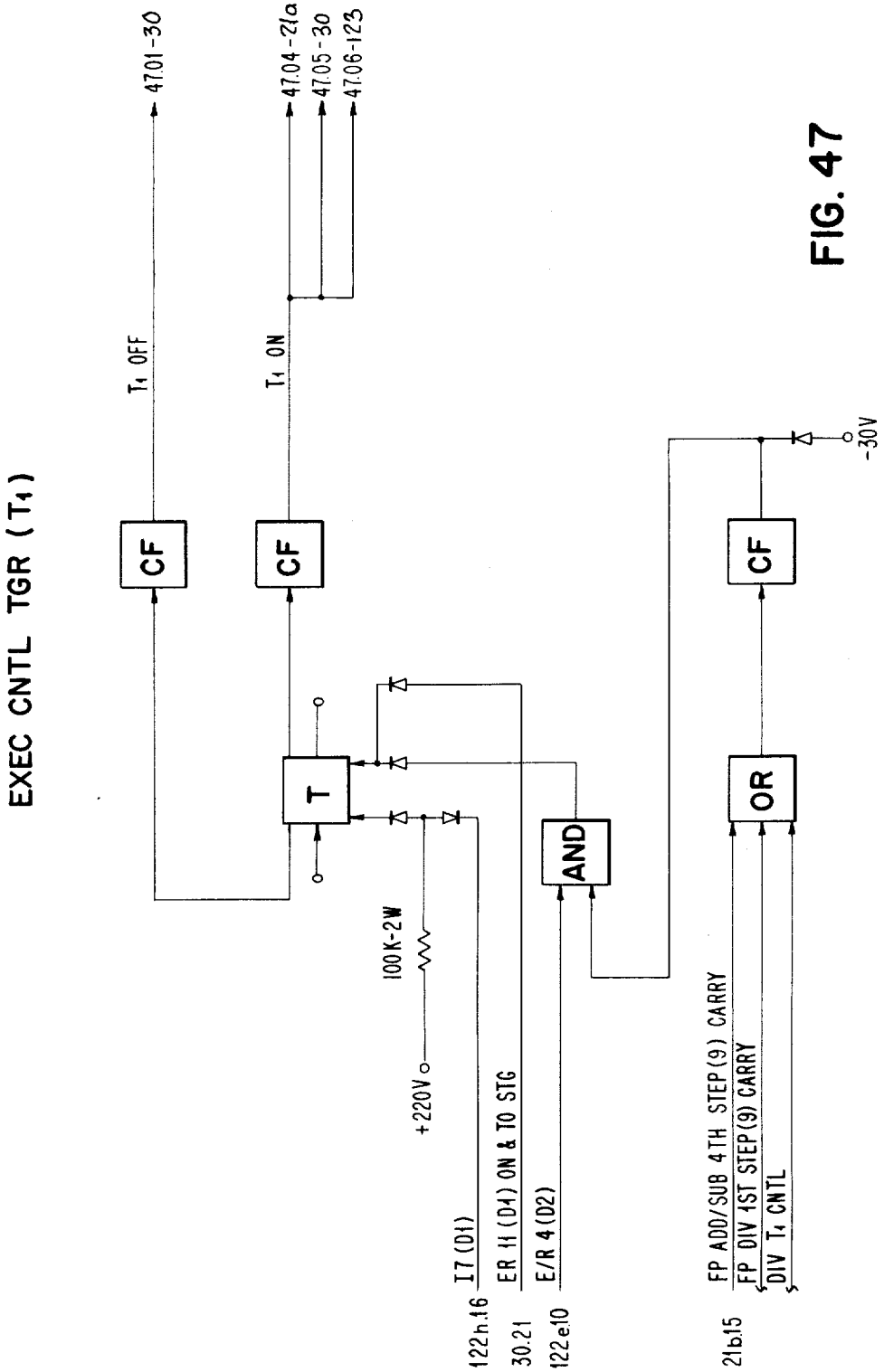

EXEC CNTL TGR (T4)
47.01-30
47.04-21a
47.05-30
47.06-123
T4 OFF
T4 ON
CF
CF
CF
T
AND
OR
-30V
100K-2W
+220V
122h.16 I7 (D1)
30.21 ER 11 (D4) ON & TO STG
122e.10 E/R 4 (D2)
21b.15 FP ADD/SUB 4TH STEP (9) CARRY
FP DIV 1ST STEP (9) CARRY
DIV T4 CNTL

FIG. 47

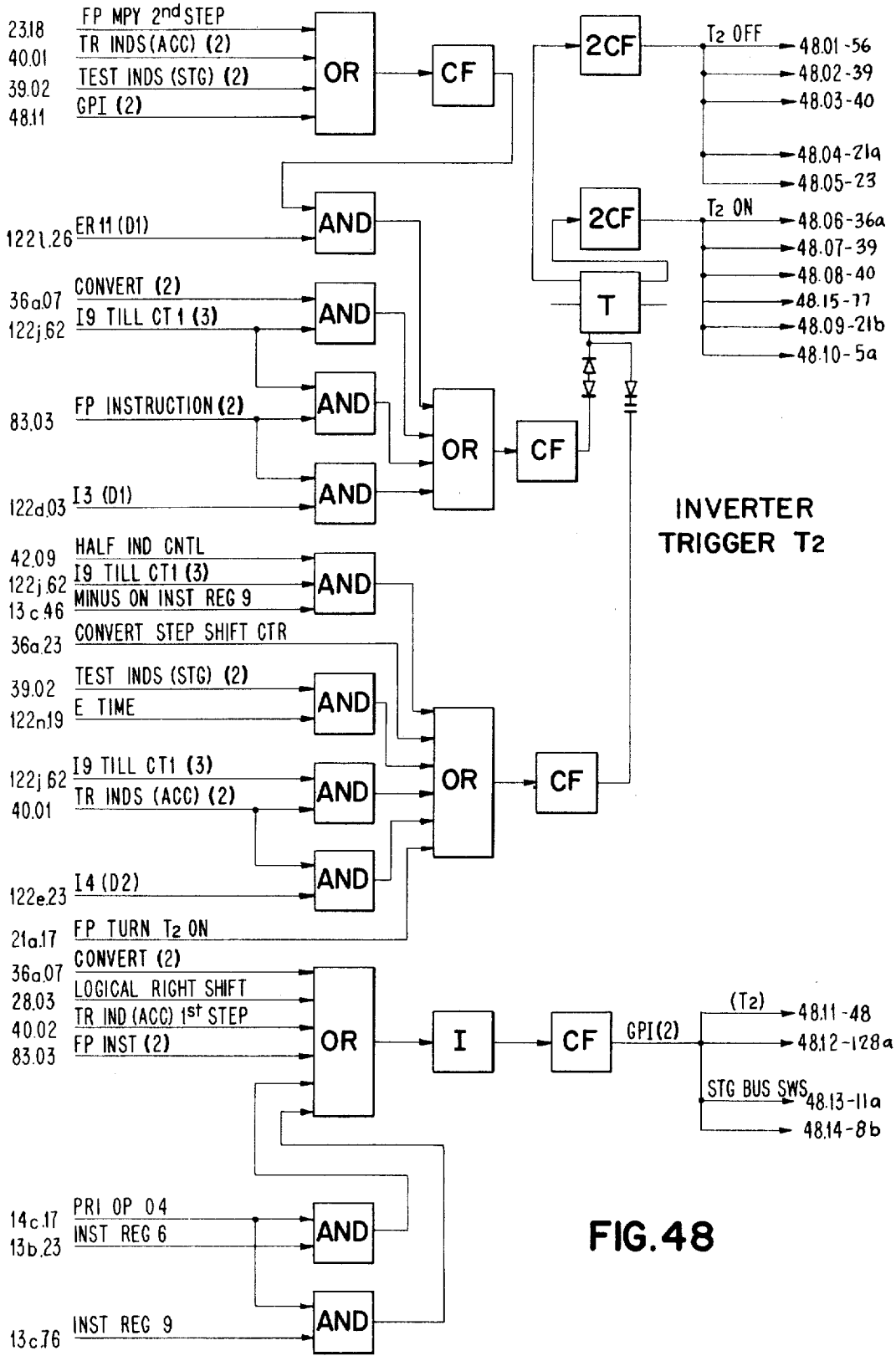

23.18
40.01
39.02
48.11
FP MPY 2nd STEP
TR INDS (ACC) (2)
TEST INDS (STG) (2)
GPI (2)
OR
CF
2CF
T2 OFF
48.01-56
48.02-39
48.03-40
48.04-21q
48.05-23
122l.26
ER 11 (D1)
AND
2CF
T2 ON
48.06-36a
48.07-39
48.08-40
48.15-77
48.09-21b
48.10-5a
36a.07
122j.62
CONVERT (2)
I9 TILL CT 1 (3)
T
83.03
FP INSTRUCTION (2)
122d.03
I3 (D1)
INVERTER
TRIGGER T2
42.09
122j.62
13c.46
HALF IND CNTL
I9 TILL CT1 (3)
MINUS ON INST REG 9
36a.23
CONVERT STEP SHIFT CTR
39.02
122n.19
TEST INDS (STG) (2)
E TIME
122j.62
40.01
I9 TILL CT1 (3)
TR INDS (ACC) (2)
122e.23
I4 (D2)
21a.17
FP TURN T2 ON
36a.07
28.03
40.02
83.03
CONVERT (2)
LOGICAL RIGHT SHIFT
TR IND (ACC) 1st STEP
FP INST (2)
I
GPI (2)
(T2)
48.11-48
48.12-128a
STG BUS SWS
48.13-11a
48.14-8b
14c.17
13b.23
PRI OP 04
INST REG 6
13c.76
INST REG 9

FIG.48

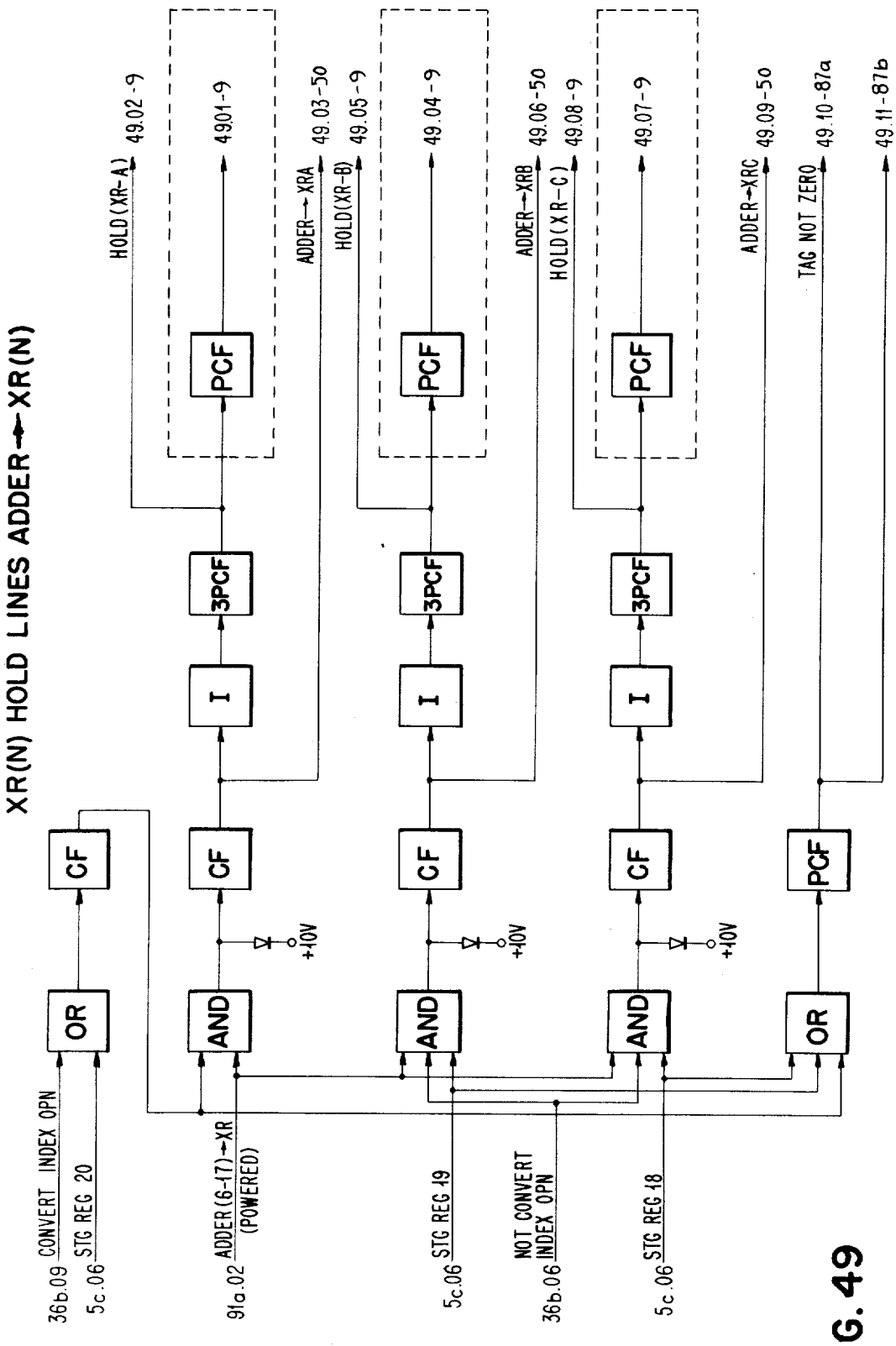

XR(N) HOLD LINES ADDER→XR(N)
36b.09 CONVERT INDEX OPN
5c.06 STG REG 20
91a.02 ADDER(6-17)→XR (POWERED)
5c.06 STG REG 19
36b.06 NOT CONVERT INDEX OPN
5c.06 STG REG 18
OR
AND
CF
+10V
I
3PCF
PCF
HOLD(XR-A)
49.02-9
49.01-9
ADDER→XRA
49.03-50
HOLD(XR-B)
49.05-9
49.04-9
ADDER→XRB
49.06-50
HOLD(XR-C)
49.08-9
49.07-9
ADDER→XRC
49.09-50
TAG NOT ZERO
49.10-87a
49.11-87b

FIG. 49

TIMING PULSE CONTROL CIRCUITS

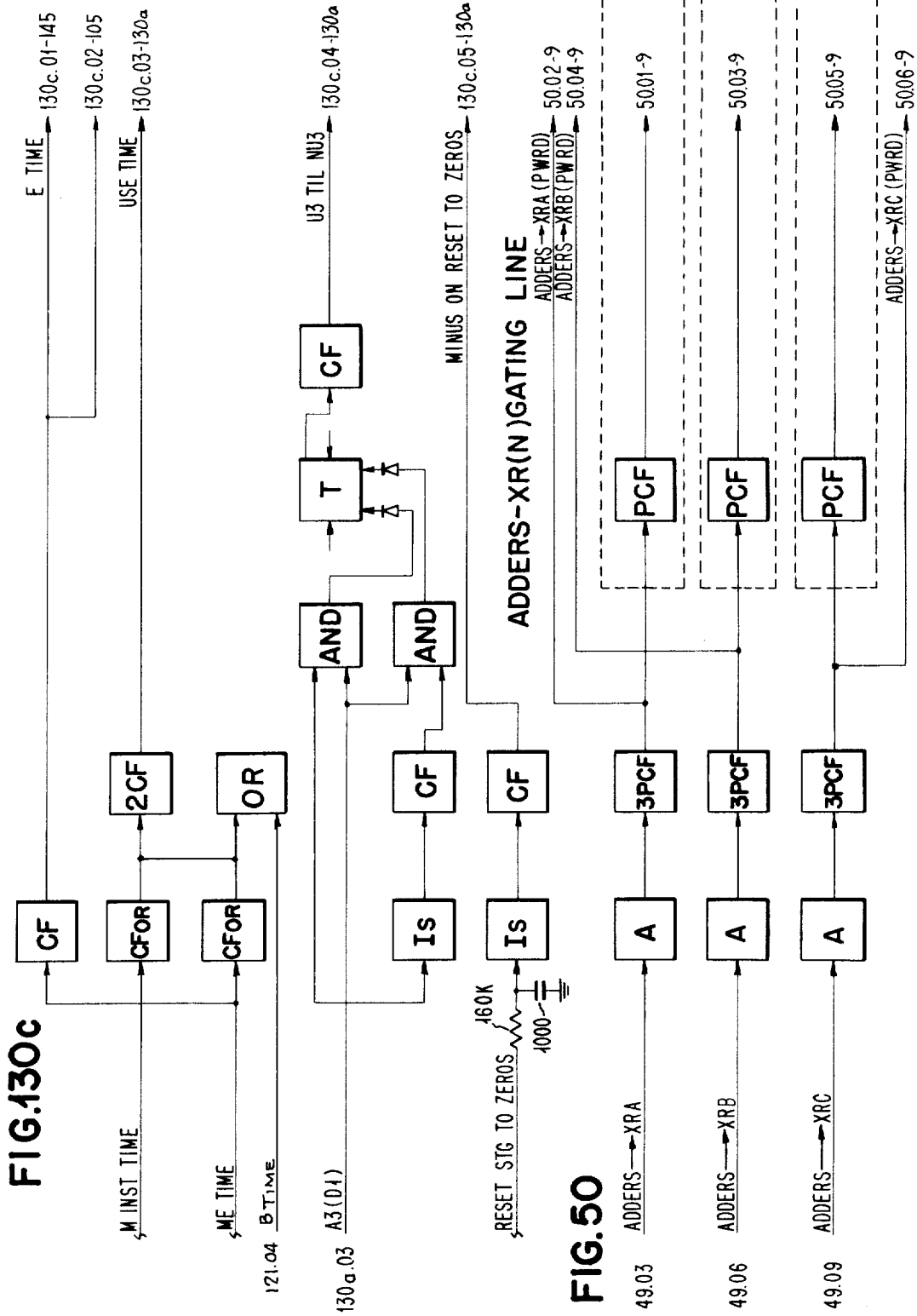


FIG.130c

FIG.50

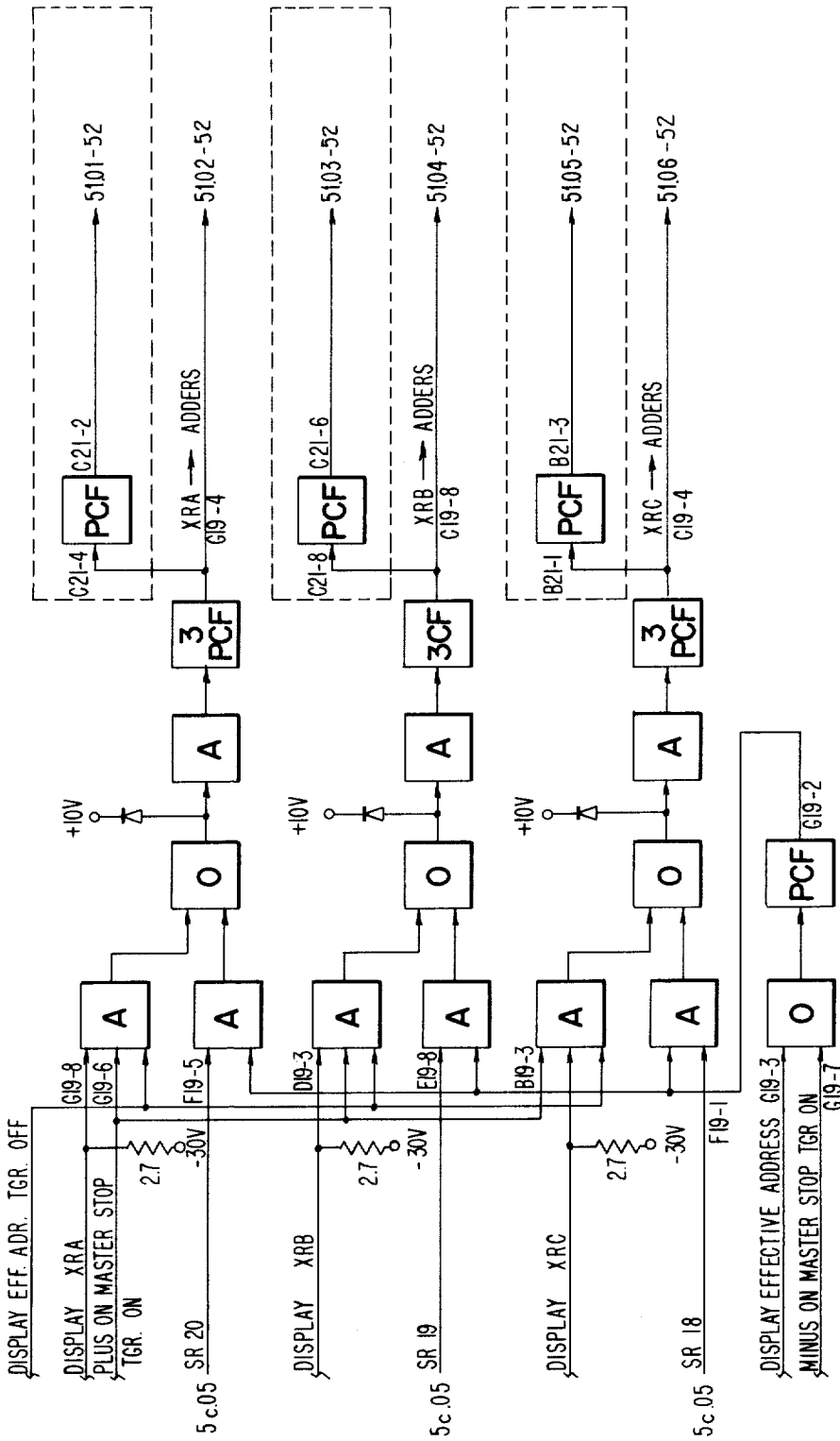
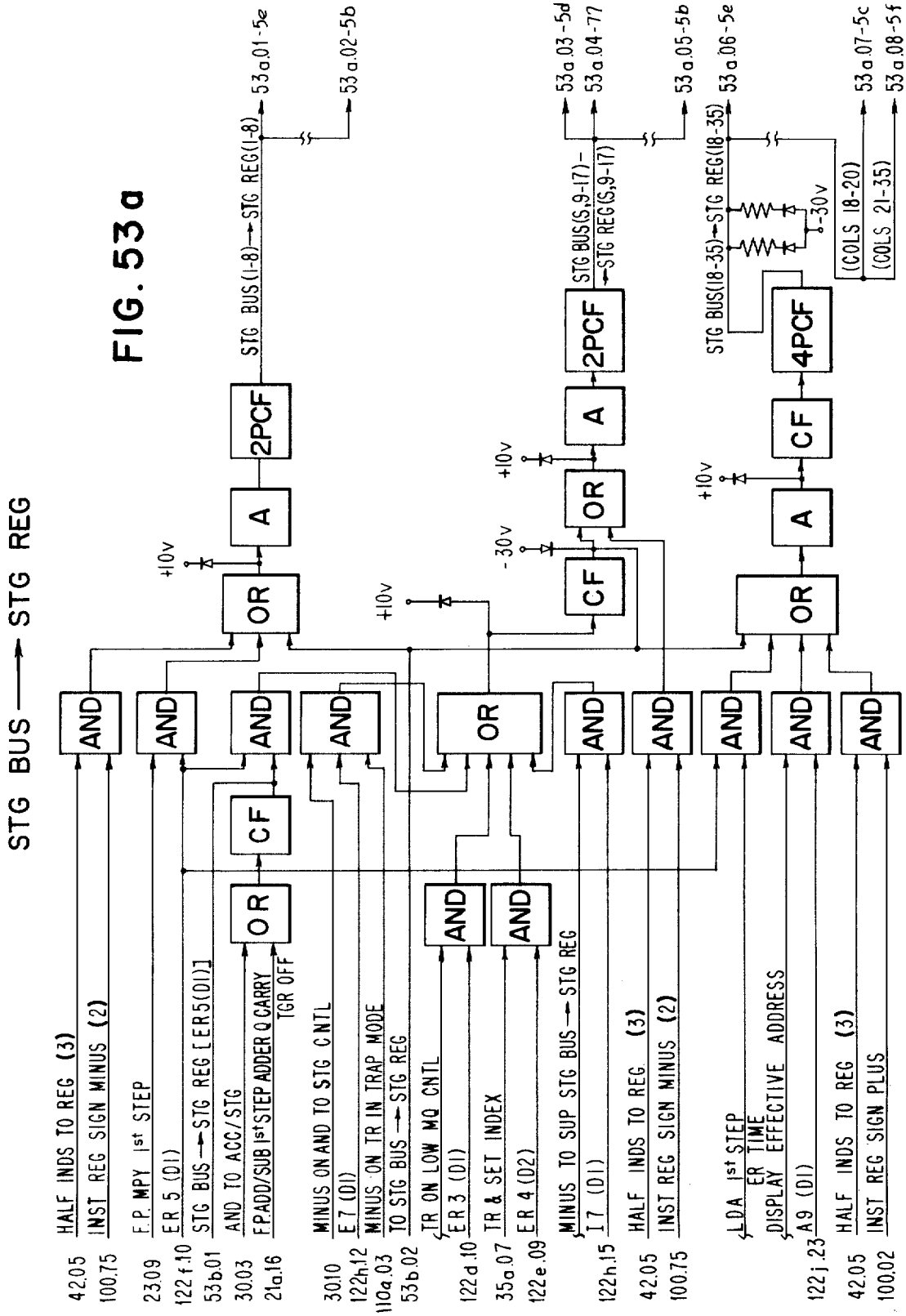

INDEX REGISTER → ADDERS GATING LINE
DISPLAY EFF. ADR. TGR. OFF
DISPLAY XRA
PLUS ON MASTER STOP
TGR. ON
5c.05 SR 20
DISPLAY XRB
5c.05 SR 19
DISPLAY XRC
5c.05 SR 18
DISPLAY EFFECTIVE ADDRESS
MINUS ON MASTER STOP TGR ON
G19-8
G19-6
F19-5
D19-3
E19-8
B19-3
F19-1
G19-3
G19-7
G19-2
2.7
-30V
+10V
A
O
3 PCF
3CF
PCF
C21-4
C21-2
C21-8
C21-6
B21-1
B21-3
XRA → ADDERS
XRB → ADDERS
XRC → ADDERS
G19-4
C19-8
G19-4
5101-52
5102-52
5103-52
5104-52
5105-52
5106-52

FIG. 51

FIG. 53a


STG BUS → STG REG
AND
OR
CF
A
2PCF
4PCF
+10v
-30v
HALF INDS TO REG (3)
INST REG SIGN MINUS (2)
F.P. MPY 1st STEP
ER 5 (01)
STG BUS → STG REG [ER5(01)]
AND TO ACC/STG
F.P.ADD/SUB 1st STEP ADDER Q CARRY
TGR OFF
MINUS ON AND TO STG CNTL
E 7 (01)
MINUS ON TR IN TRAP MODE
TO STG BUS → STG REG
TR ON LOW MQ CNTL
ER 3 (01)
TR & SET INDEX
ER 4 (02)
MINUS TO SUP STG BUS → STG REG
I 7 (01)
HALF INDS TO REG (3)
INST REG SIGN MINUS (2)
LDA 1st STEP
ER TIME
DISPLAY EFFECTIVE ADDRESS
A 9 (01)
HALF INDS TO REG (3)
INST REG SIGN PLUS
STG BUS(1-8)→STG REG(1-8)
STG BUS(S,9-17)→STG REG(S,9-17)
STG BUS(18-35)→STG REG(18-35)
(COLS 18-20)
(COLS 21-35)
42.05
100.75
23.09
122 f.10
53b.01
30.03
21a.16
30.10
122h.12
110a.03
53b.02
122d.10
35a.07
122e.09
122h.15
42.05
100.75
122j.23
42.05
100.02
53a.01-5e
53a.02-5b
53a.03-5d
53a.04-77
53a.05-5b
53a.06-5e
53a.07-5c
53a.08-5f

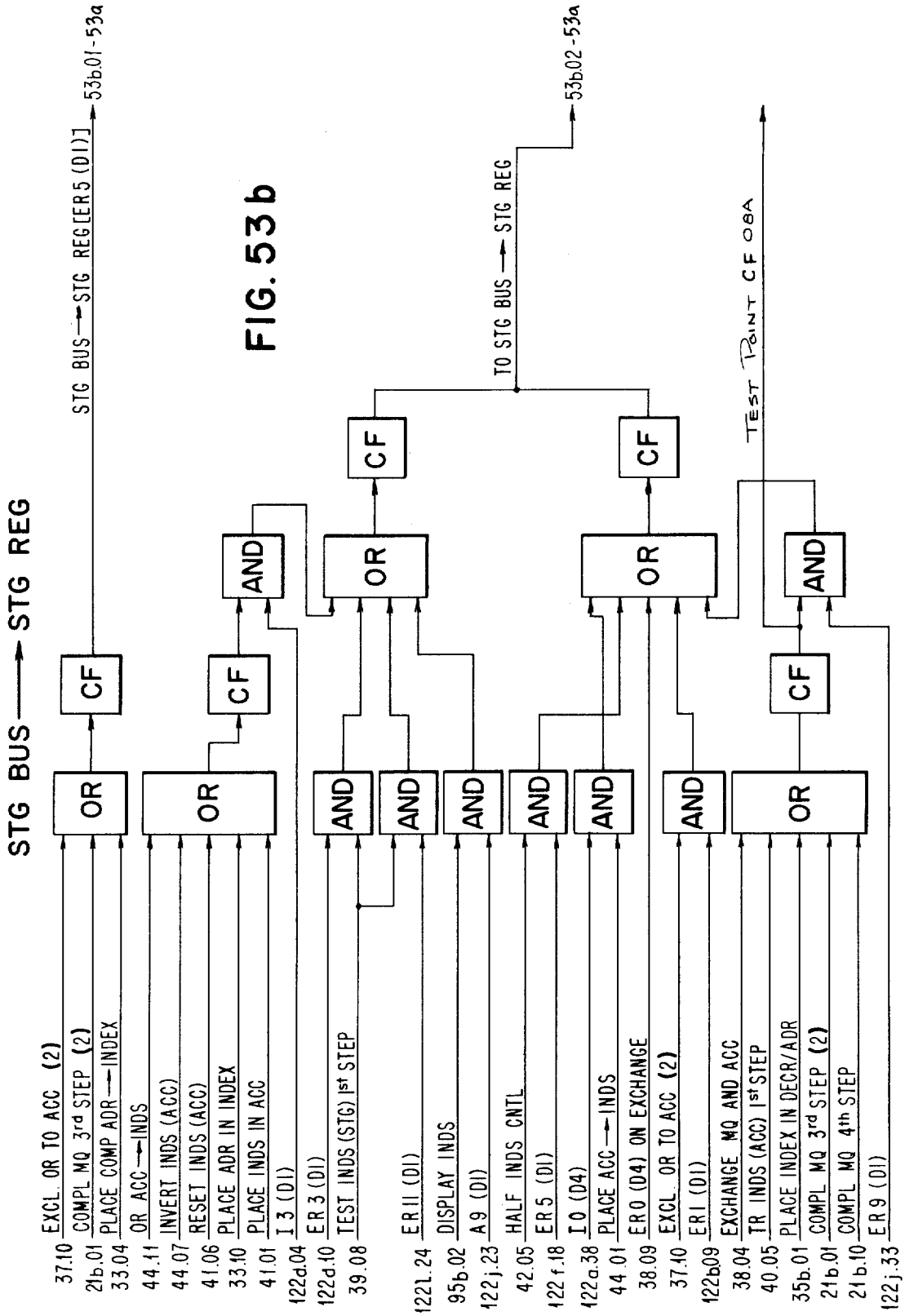
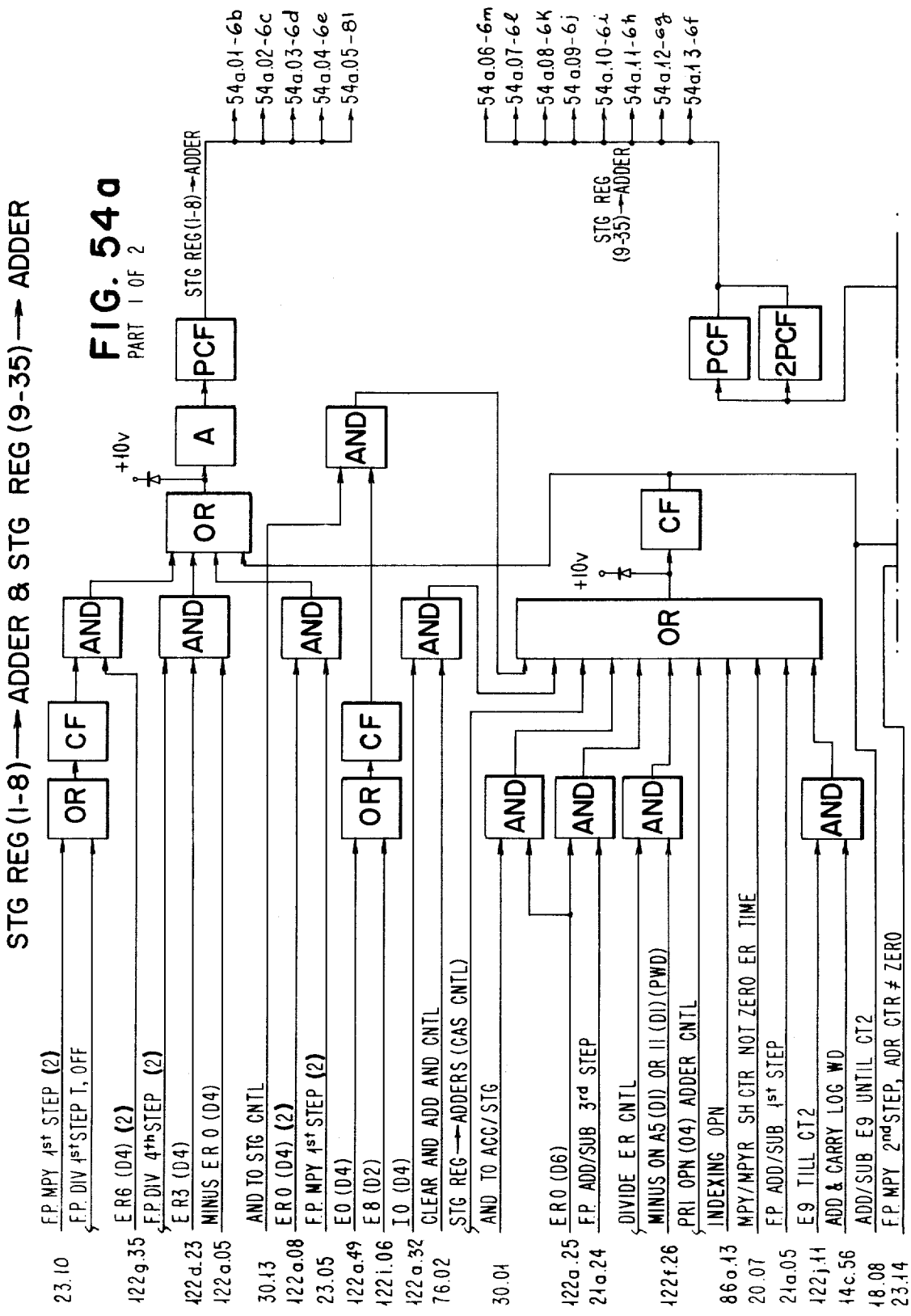

STG BUS → STG REG
37.10 EXCL. OR TO ACC (2)
21b.01 COMPL MQ 3rd STEP (2)
33.04 PLACE COMP ADR → INDEX
44.11 OR ACC → INDS
44.07 INVERT INDS (ACC)
41.06 RESET INDS (ACC)
33.10 PLACE ADR IN INDEX
41.01 PLACE INDS IN ACC
122d.04 I 3 (D1)
122d.10 ER 3 (D1)
39.08 TEST INDS (STG) 1st STEP
1221.24 ER 11 (D1)
95b.02 DISPLAY INDS
122j.23 A 9 (D1)
42.05 HALF INDS CNTL
122f.18 ER 5 (D1)
122a.38 I O (D4)
44.01 PLACE ACC → INDS
38.09 ER 0 (D4) ON EXCHANGE
37.10 EXCL. OR TO ACC (2)
122b.09 ER 1 (D1)
38.04 EXCHANGE MQ AND ACC
40.05 TR INDS (ACC) 1st STEP
35b.01 PLACE INDEX IN DECR/ADR
21b.01 COMPL MQ 3rd STEP (2)
21b.10 COMPL MQ 4th STEP
122j.33 ER 9 (D1)
OR
CF
AND
STG BUS → STG REG [ER 5 (D1)]
53b.01-53a
TO STG BUS → STG REG
53b.02-53a
TEST POINT CF 08A

FIG. 53b


STG REG (1-8) → ADDER & STG REG (9-35) → ADDER
FIG. 54a
PART 1 OF 2
F.P. MPY 1st STEP (2)
F.P. DIV 1st STEP T, OFF
E R6 (D4) (2)
F.P. DIV 4thSTEP (2)
E R3 (D4)
MINUS E R 0 (D4)
AND TO STG CNTL
E R 0 (D4) (2)
F.P. MPY 1st STEP (2)
E 0 (D4)
E 8 (D2)
I 0 (D4)
CLEAR AND ADD AND CNTL
STG REG → ADDERS (CAS CNTL)
AND TO ACC/STG
E R 0 (D6)
F.P. ADD/SUB 3rd STEP
DIVIDE E R CNTL
MINUS ON A5 (DI) OR 11 (DI) (PWD)
PRI OPN (04) ADDER CNTL
INDEXING OPN
MPY/MPYR SH CTR NOT ZERO ER TIME
F.P. ADD/SUB 1st STEP
E 9 TILL CT2
ADD & CARRY LOG WD
ADD/SUB E9 UNTIL CT2
F.P. MPY 2ndSTEP, ADR CTR ≠ ZERO
23.10
122g.35
422a.23
422a.05
30.13
122a.08
23.05
122a.49
422i.06
422a.32
76.02
30.01
122a.25
21a.24
422f.26
86a.13
20.07
21a.05
122j.11
14c.56
18.08
23.14
OR
CF
AND
+10v
A
PCF
STG REG (1-8) → ADDER
54a.01-6b
54a.02-6c
54a.03-6d
54a.04-6e
54a.05-81
54a.06-6m
54a.07-6l
54a.08-6K
54a.09-6j
54a.10-6i
54a.11-6h
54a.12-6g
54a.13-6f
STG REG (9-35) → ADDER
2PCF

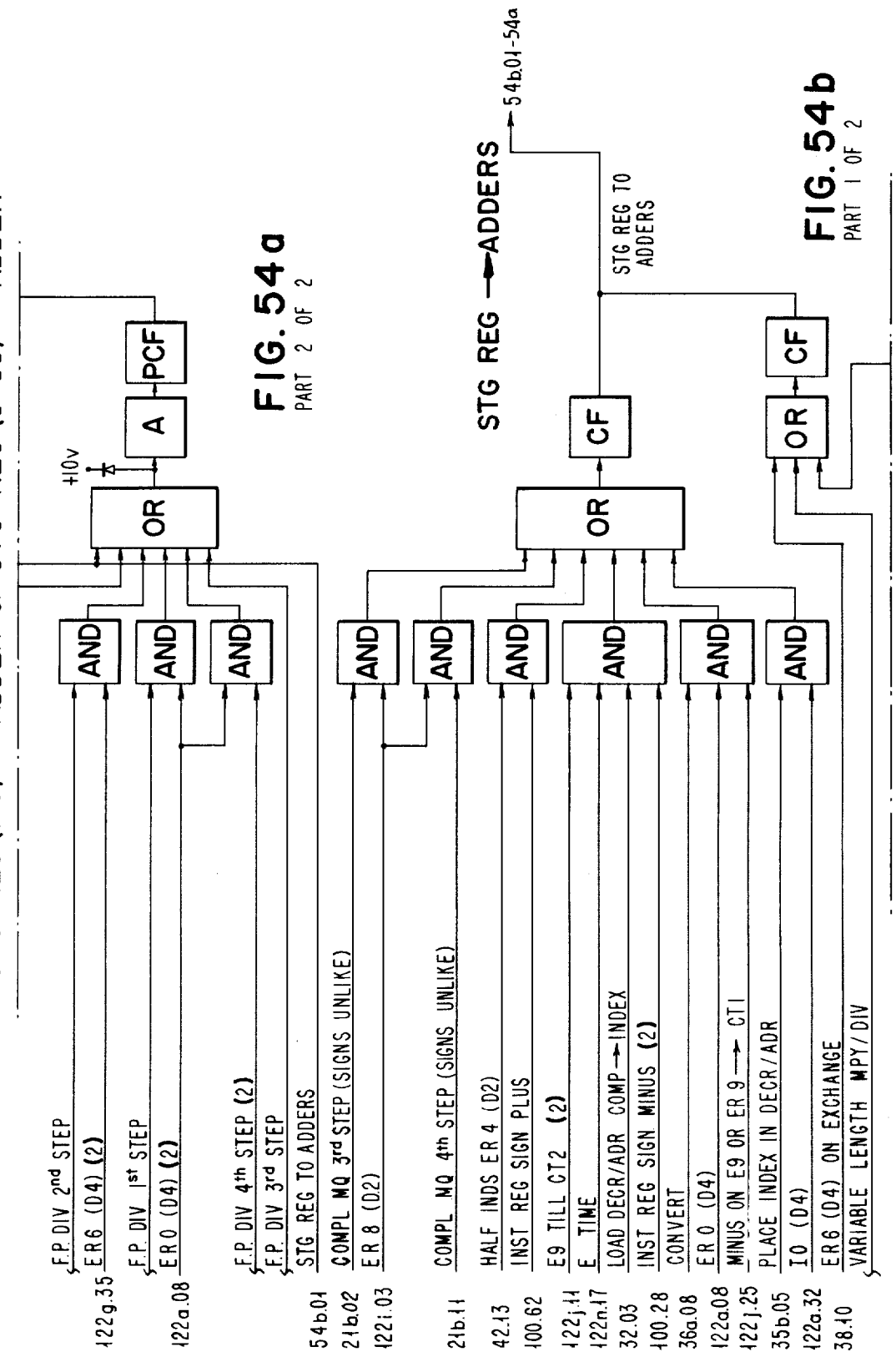


FIG. 54a
PART 2 OF 2

FIG. 54b
PART 1 OF 2

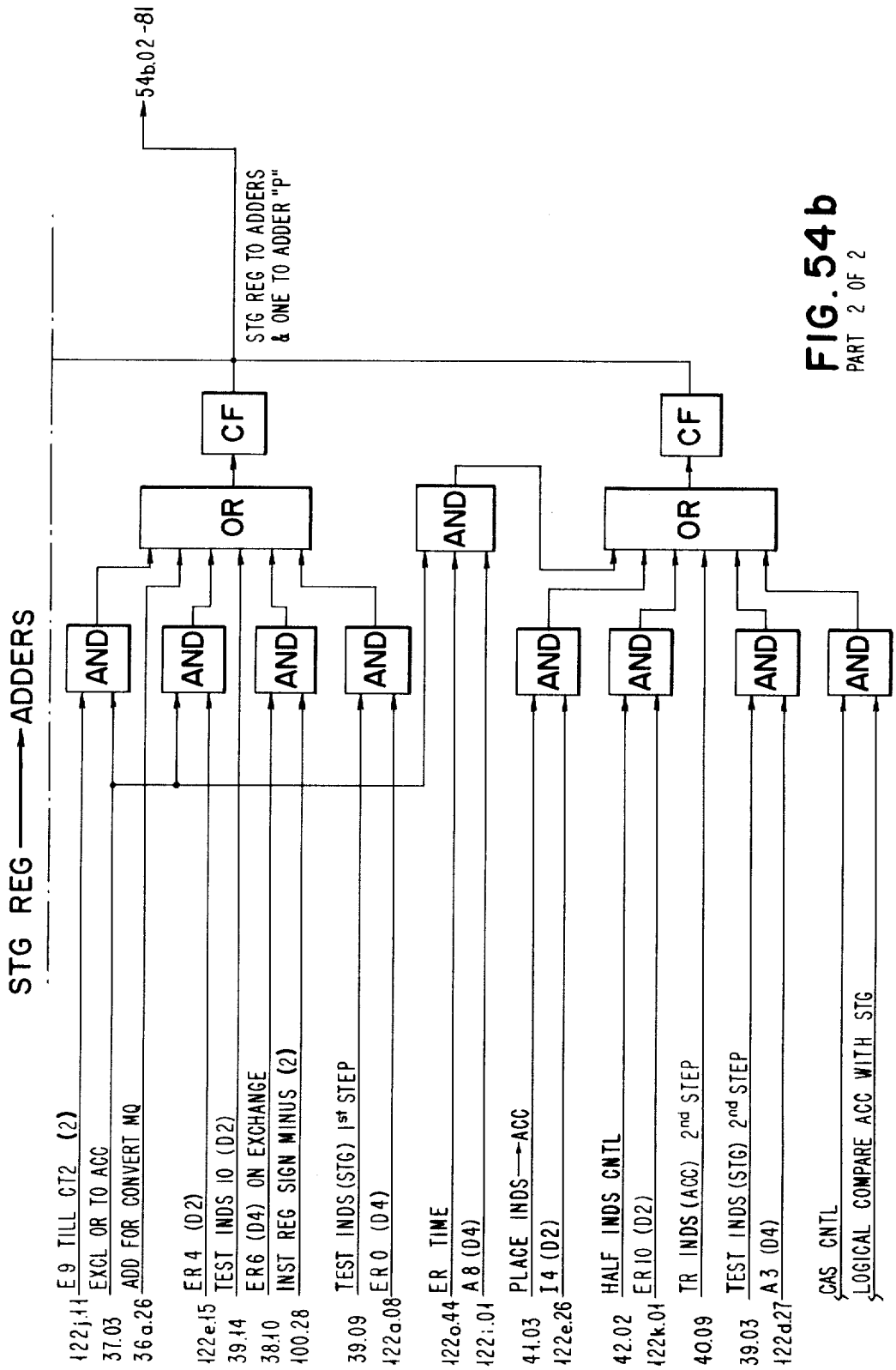


FIG. 54b
PART 2 OF 2

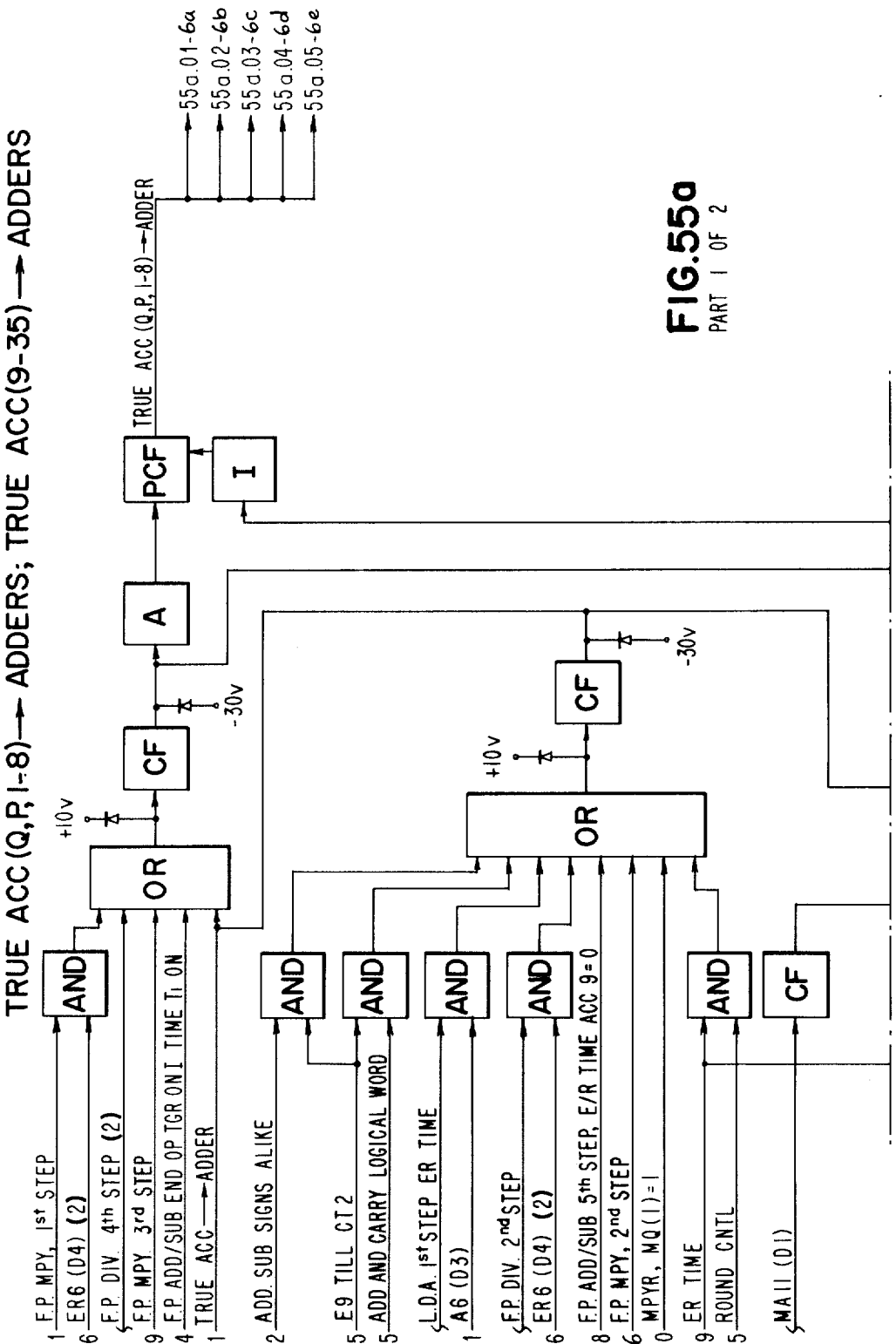


FIG.55a
PART 1 OF 2

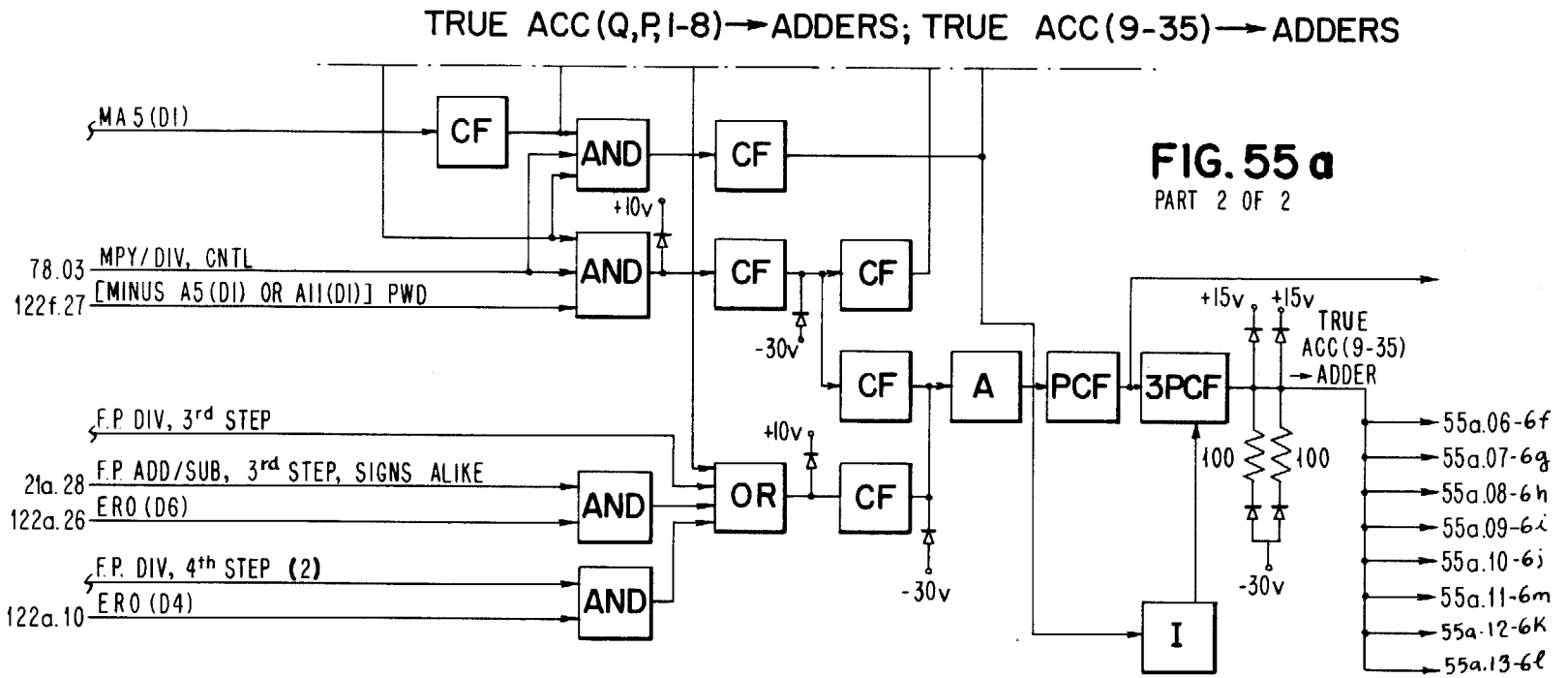


FIG. 55a
PART 2 OF 2

FIG. 55b

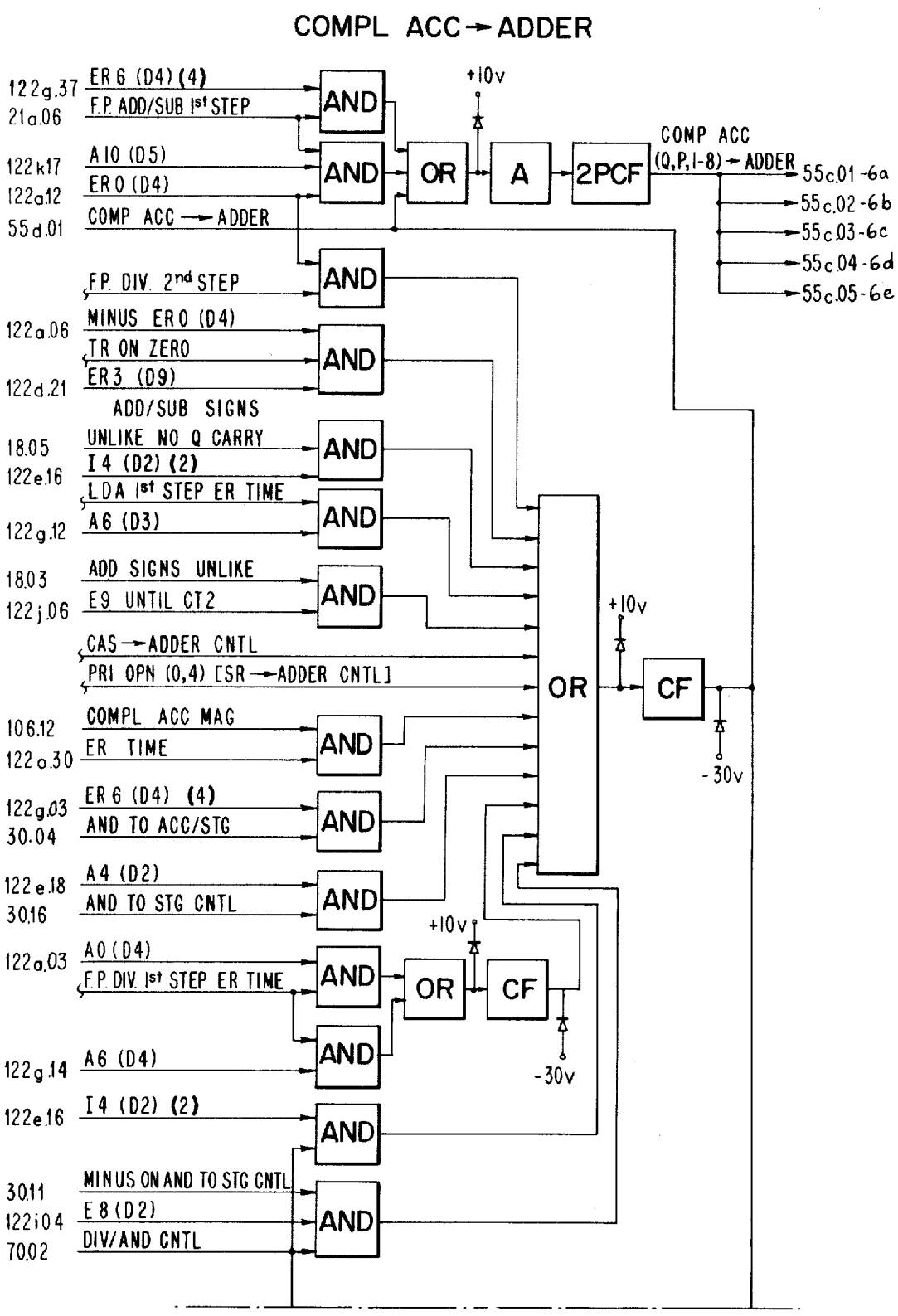


FIG. 55c
PART 1 OF 2

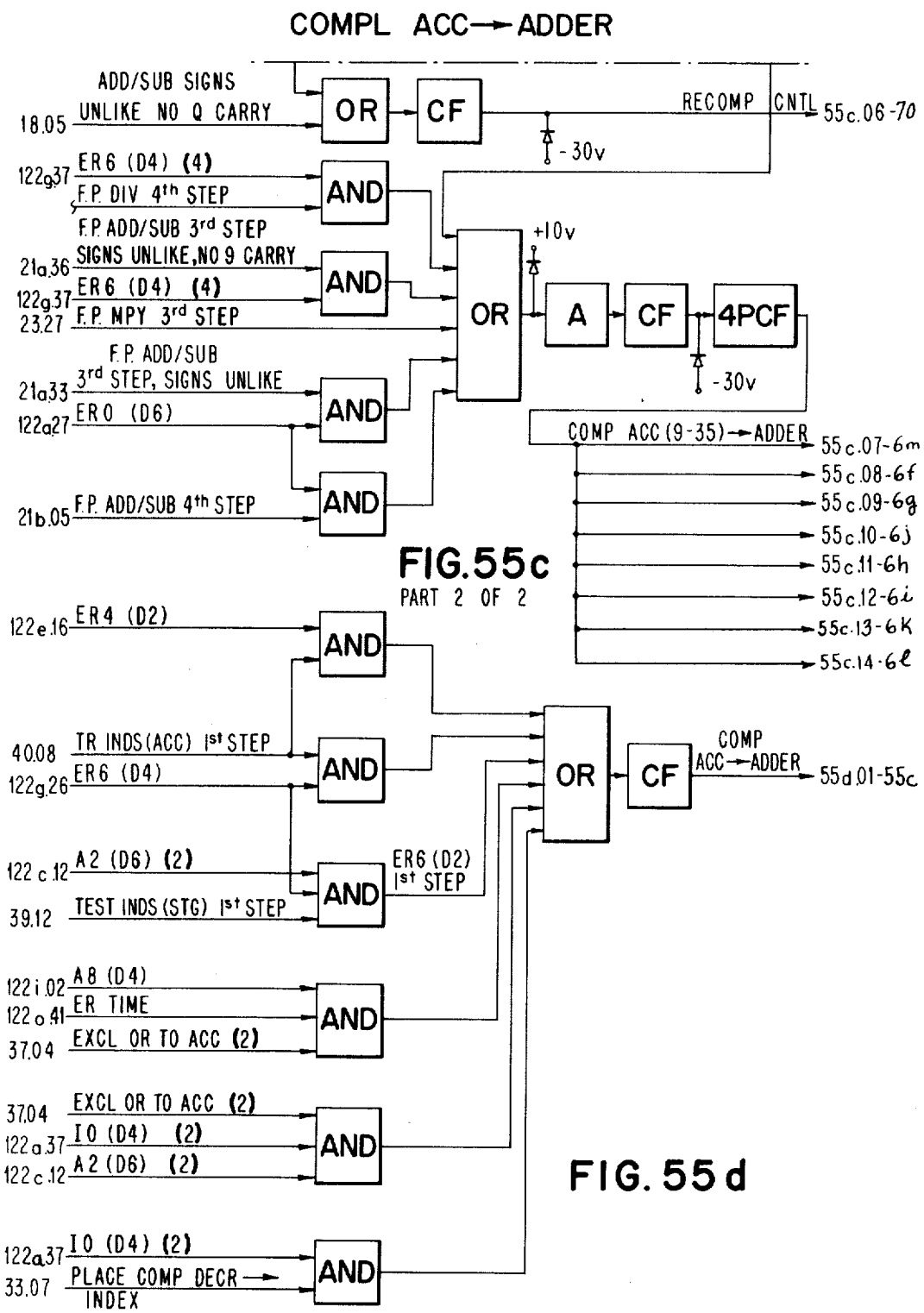
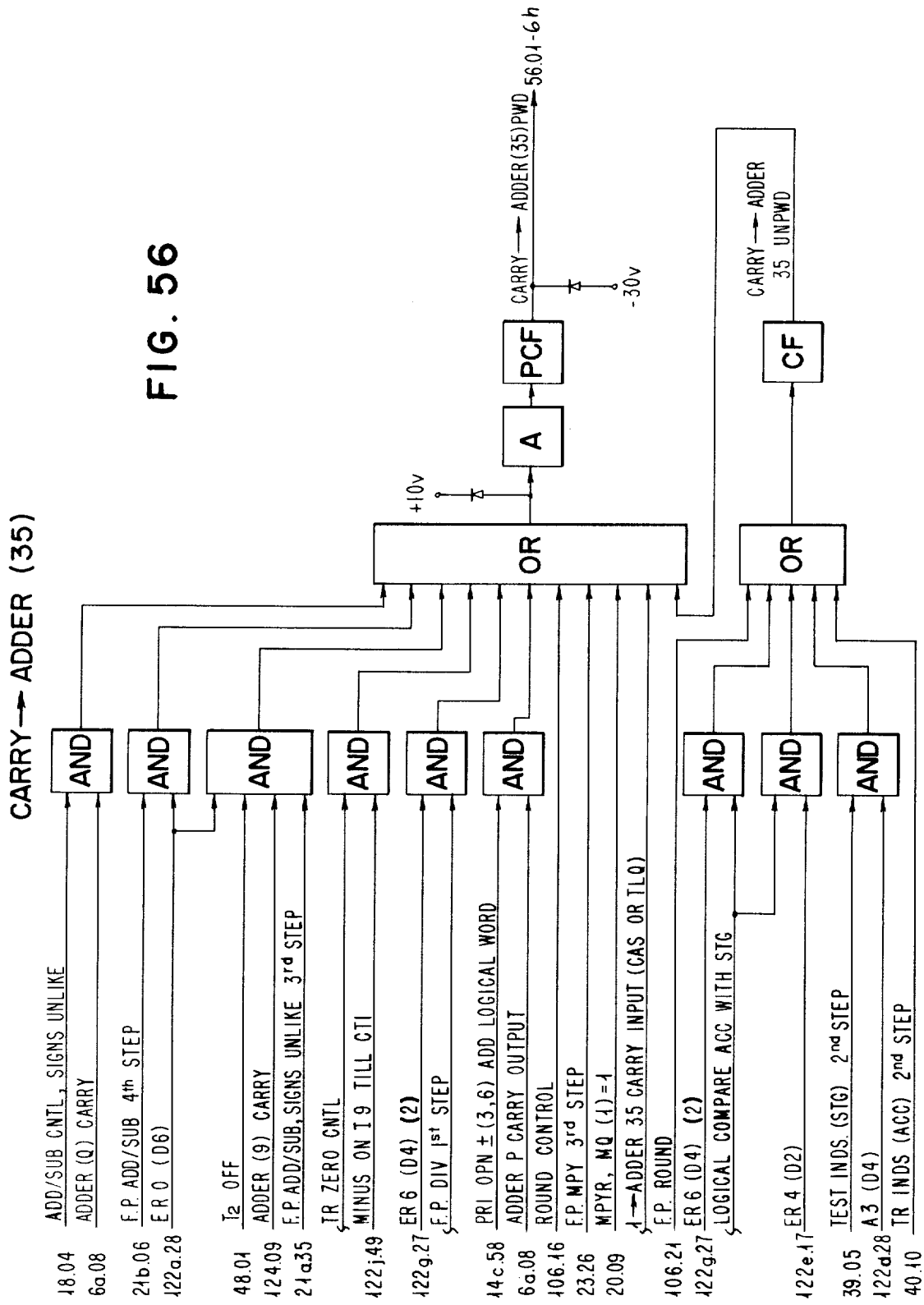

COMPL ACC→ADDER
ADD/SUB SIGNS UNLIKE NO Q CARRY
18.05
OR
CF
RECOMP CNTL
55c.06-70
-30v
122g.37 ER6 (D4) (4)
F.P. DIV 4th STEP
F.P. ADD/SUB 3rd STEP
AND
+10v
21a.36 SIGNS UNLIKE, NO 9 CARRY
122g.37 ER6 (D4) (4)
23.27 F.P. MPY 3rd STEP
AND
OR
A
CF
4PCF
-30v
F.P. ADD/SUB 3rd STEP, SIGNS UNLIKE
21a.33
122a.27 ER0 (D6)
AND
COMP ACC (9-35)→ADDER
55c.07-6m
55c.08-6f
55c.09-6g
55c.10-6j
55c.11-6h
55c.12-6i
55c.13-6K
55c.14-6ℓ
21b.05 F.P. ADD/SUB 4th STEP
AND
FIG.55c
PART 2 OF 2
122e.16 ER4 (D2)
AND
40.08 TR INDS (ACC) 1st STEP
122g.26 ER6 (D4)
AND
OR
CF
COMP ACC→ADDER
55d.01-55c
122c.12 A2 (D6) (2)
39.12 TEST INDS (STG) 1st STEP
AND
ER6 (D2) 1st STEP
122i.02 A8 (D4)
122o.41 ER TIME
37.04 EXCL OR TO ACC (2)
AND
37.04 EXCL OR TO ACC (2)
122a.37 IO (D4) (2)
122c.12 A2 (D6) (2)
AND
FIG. 55d
122a.37 IO (D4) (2)
33.07 PLACE COMP DECR→ INDEX
AND

FIG. 56


CARRY → ADDER (35)
AND
OR
A
PCF
CF
+10v
-30v
CARRY → ADDER (35) PWD
56.01-6h
CARRY → ADDER 35 UNPWD
18.04 ADD/SUB CNTL, SIGNS UNLIKE
6a.08 ADDER (Q) CARRY
21b.06 F.P. ADD/SUB 4th STEP
122a.28 ER 0 (D6)
48.01 T2 OFF
124.09 ADDER (9) CARRY
21a35 F.P. ADD/SUB, SIGNS UNLIKE 3rd STEP
122j.49 TR ZERO CNTL
MINUS ON T 9 TILL CTI
122g.27 ER 6 (D4) (2)
F.P. DIV 1st STEP
14c.58 PRI OPN ±(3,6) ADD LOGICAL WORD
6a.08 ADDER P CARRY OUTPUT
106.16 ROUND CONTROL
23.26 F.P. MPY 3rd STEP
20.09 MPYR, MQ (1) = 1
1 → ADDER 35 CARRY INPUT (CAS OR TLQ)
106.21 F.P. ROUND
122g.27 ER 6 (D4) (2)
LOGICAL COMPARE ACC WITH STG
122e.17 ER 4 (D2)
39.05 TEST INDS. (STG) 2nd STEP
122d.28 A3 (D4)
40.10 TR INDS (ACC) 2nd STEP

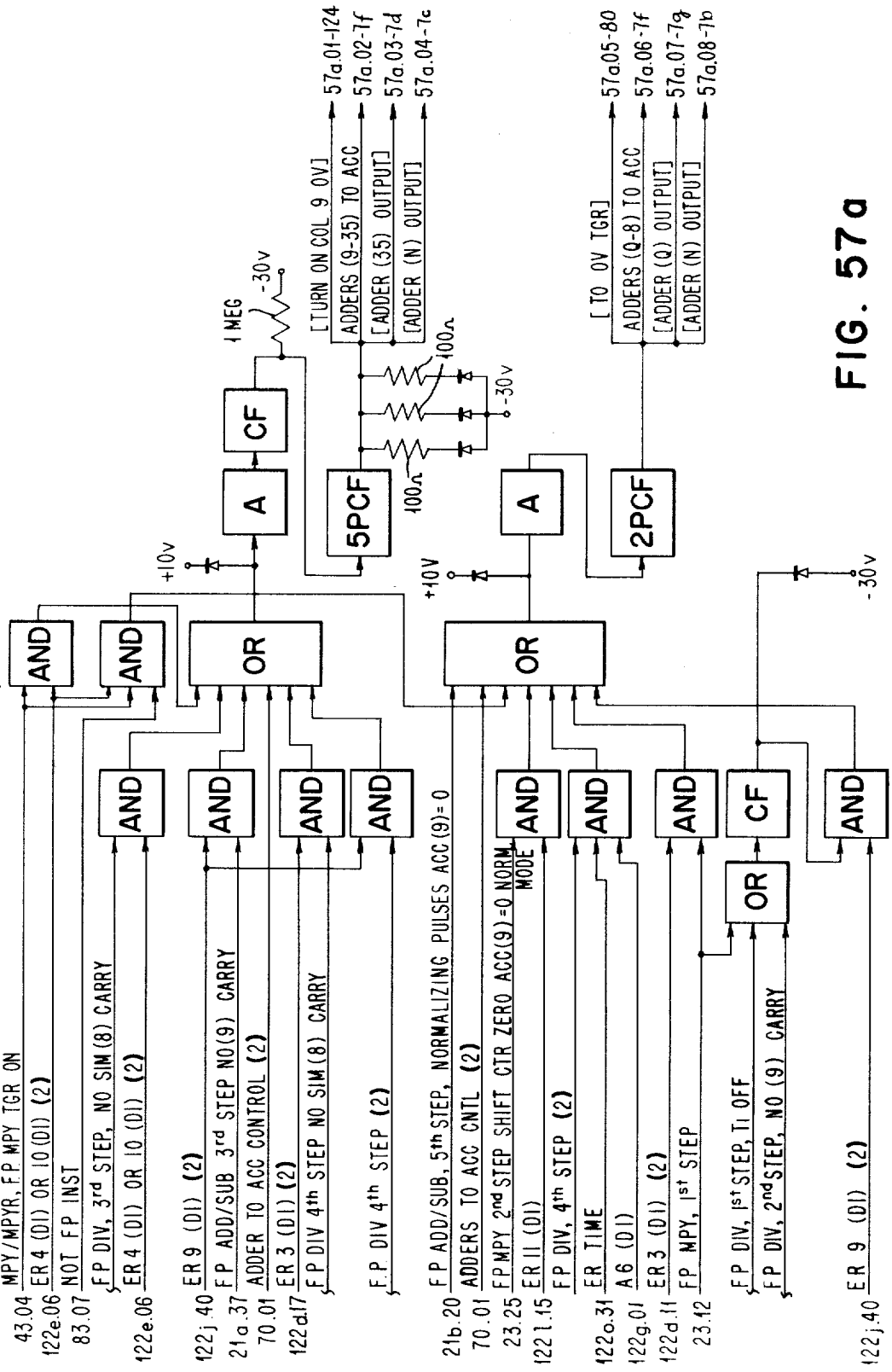

ADDER (Q,P,1-8) TO ACC; ADDER (9-35) TO ACC
MPY/MPYR, F P MPY TGR ON
43.04
ER 4 (D1) OR 10 (D1) (2)
122e.06
NOT F P INST
83.07
F P DIV, 3rd STEP, NO SIM (8) CARRY
ER 4 (D1) OR 10 (D1) (2)
122e.06
ER 9 (D1) (2)
122j.40
F P ADD/SUB 3rd STEP NO(9) CARRY
21a.37
ADDER TO ACC CONTROL (2)
70.01
ER 3 (D1) (2)
122d.17
F P DIV 4th STEP NO SIM (8) CARRY
F P DIV 4th STEP (2)
AND
OR
A
CF
5PCF
+10v
-30v
1 MEG
100Ω
[TURN ON COL 9 OV]
ADDERS (9-35) TO ACC
[ADDER (35) OUTPUT]
[ADDER (N) OUTPUT]
57a.01-124
57a.02-1f
57a.03-7d
57a.04-7c
21b.20
F P ADD/SUB, 5th STEP, NORMALIZING PULSES ACC(9)=0
70.01
ADDERS TO ACC CNTL (2)
23.25
F P MPY 2nd STEP SHIFT CTR ZERO ACC(9)=0 NORM MODE
122l.15
ER 11 (D1)
F P DIV, 4th STEP (2)
122o.31
ER TIME
122g.01
A6 (D1)
122d.11
ER 3 (D1) (2)
23.12
F P MPY, 1st STEP
F P DIV, 1st STEP, T1 OFF
F P DIV, 2nd STEP, NO (9) CARRY
122j.40
ER 9 (D1) (2)
[TO 0V TGR]
ADDERS (Q-8) TO ACC
[ADDER (Q) OUTPUT]
[ADDER (N) OUTPUT]
2PCF
57a.05-8c
57a.06-7f
57a.07-7g
57a.08-7b

FIG. 57a

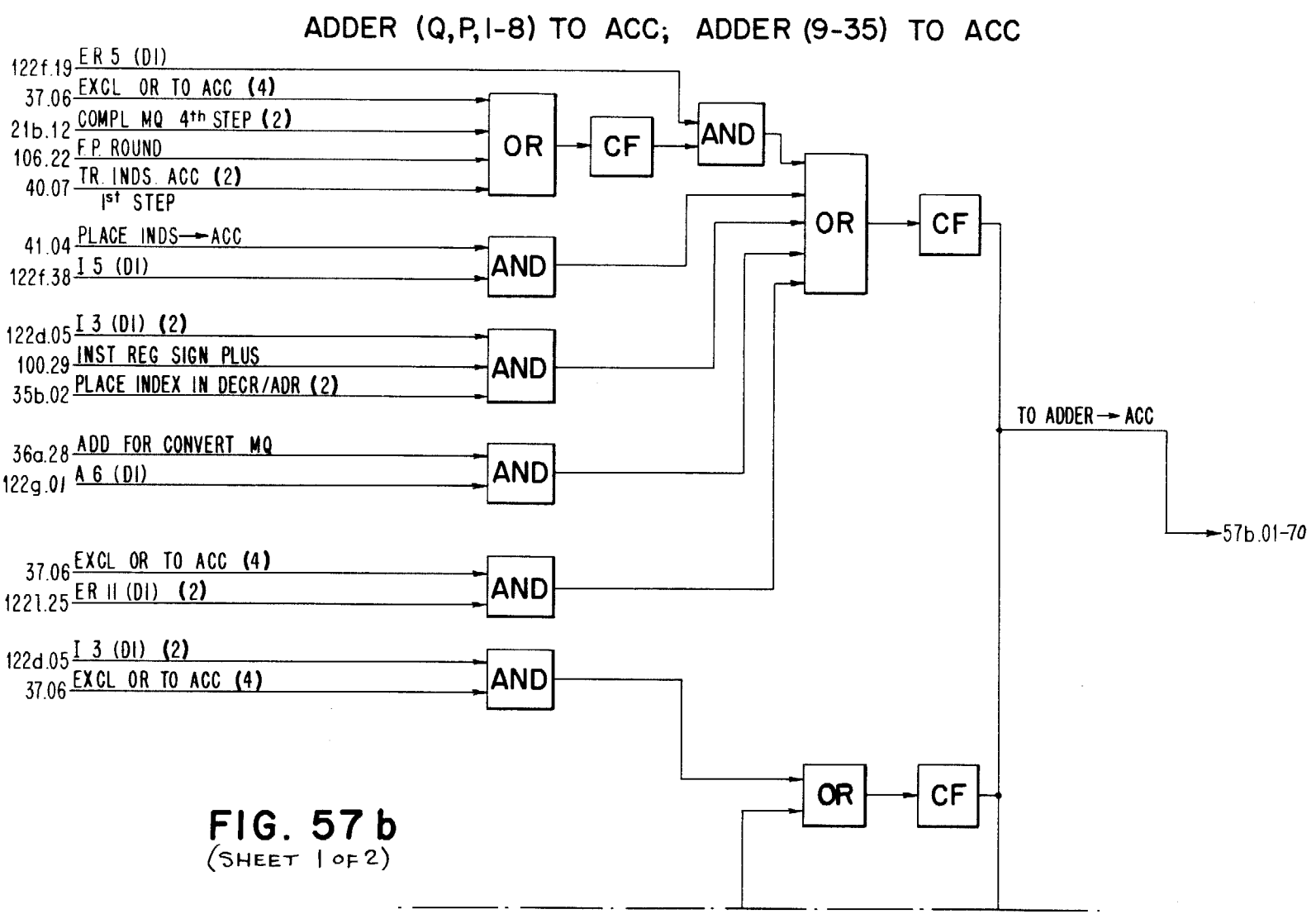


FIG. 57 b
(SHEET 1 OF 2)

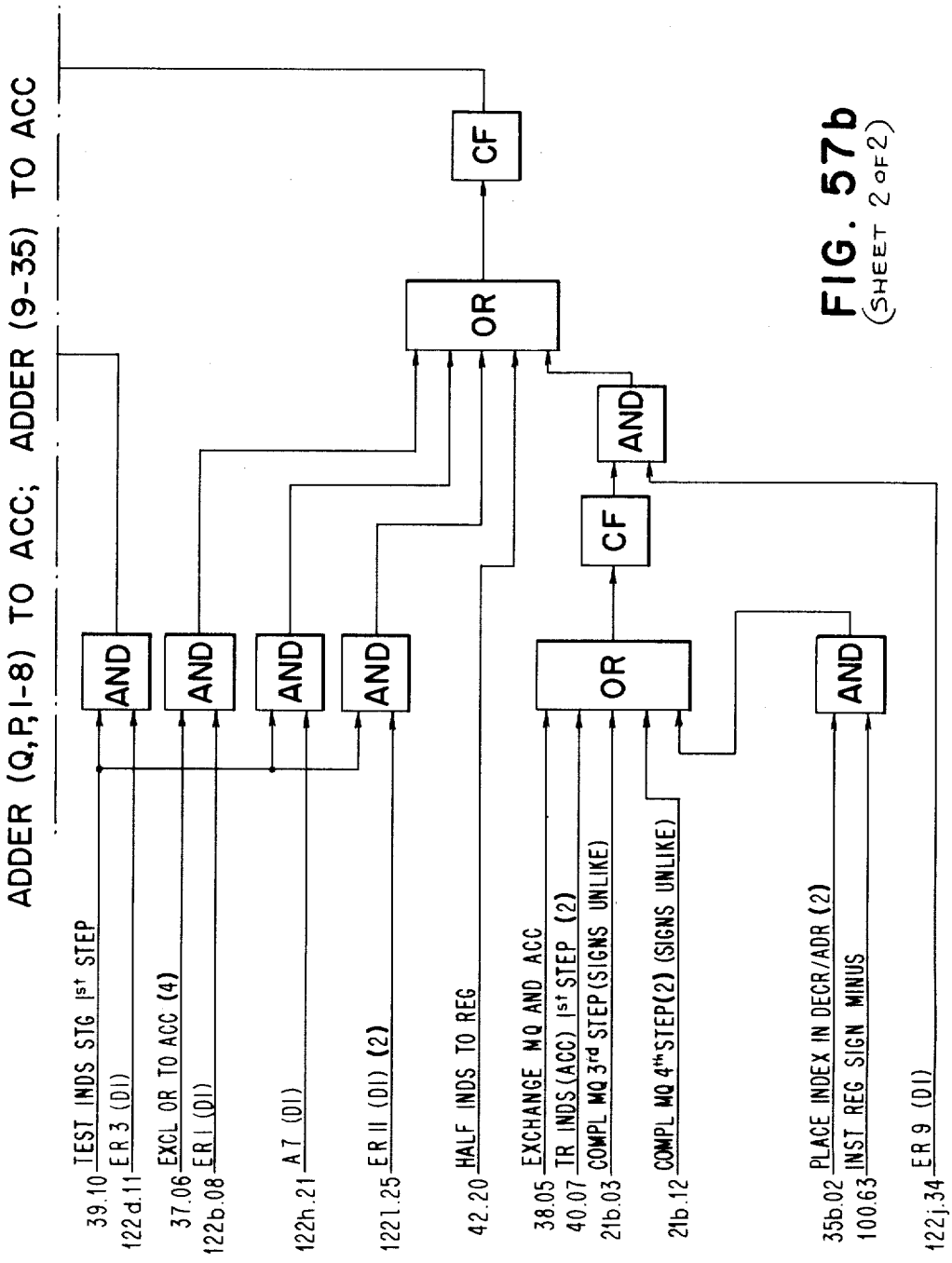
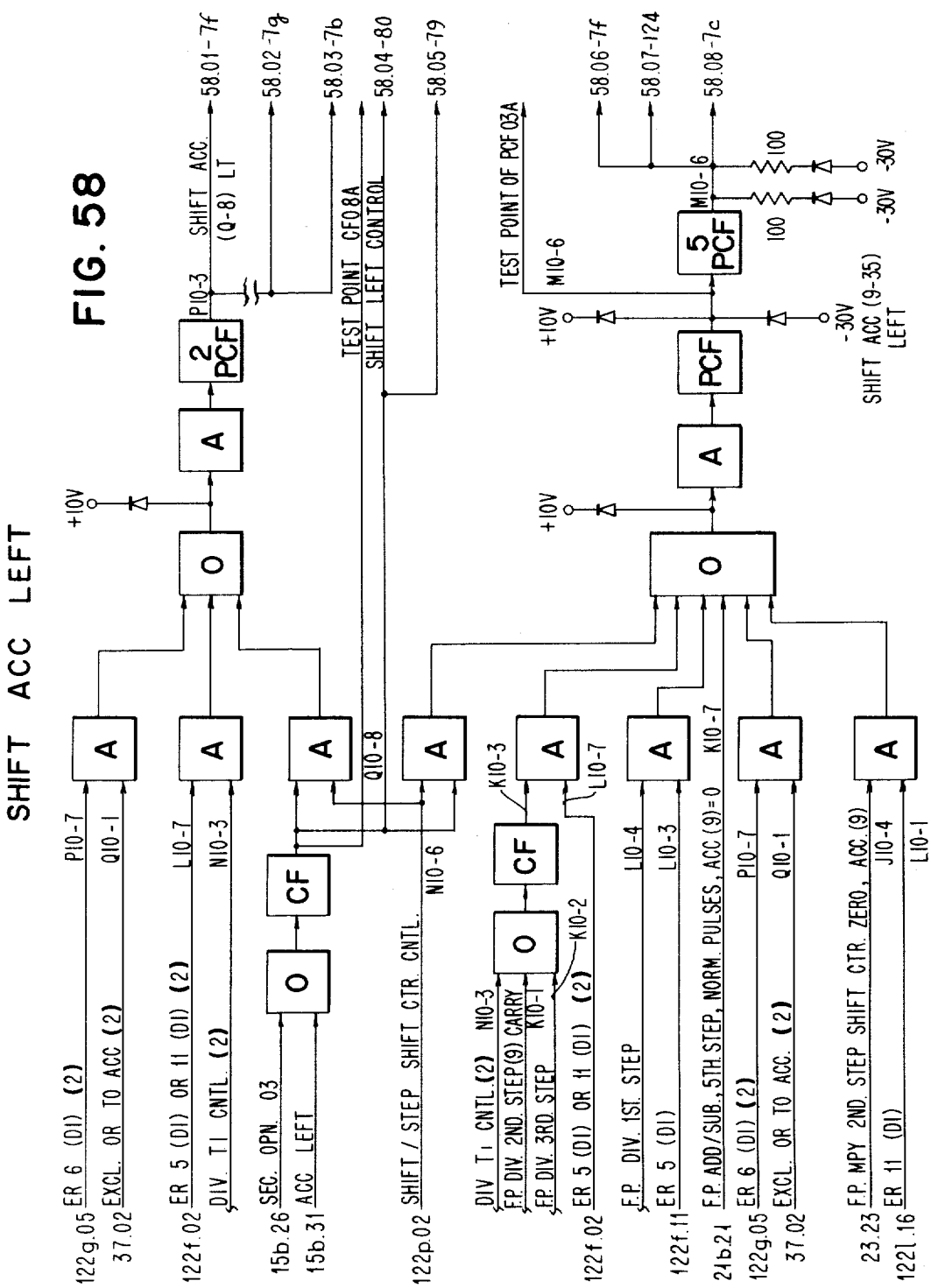


FIG. 57b
(SHEET 2 OF 2)

FIG. 58


SHIFT ACC LEFT
122g.05 ER 6 (D1) (2) P10-7
37.02 EXCL. OR TO ACC (2) Q10-1
122f.02 ER 5 (D1) OR 11 (D1) (2) L10-7
DIV. TI CNTL. (2) N10-3
15b.26 SEC. OPN. 03
15b.31 ACC LEFT
122p.02 SHIFT / STEP SHIFT CTR. CNTL. N10-6
DIV TI CNTL.(2) N10-3
F.P. DIV. 2ND. STEP (9) CARRY K10-3
F.P. DIV. 3RD. STEP K10-1
122f.02 ER 5 (D1) OR 11 (D1) (2) K10-2
F.P. DIV. 1ST. STEP L10-4
122f.11 ER 5 (D1) L10-3
21b.21 F.P. ADD/SUB., 5TH. STEP, NORM. PULSES, ACC (9)=0 K10-7
122g.05 ER 6 (D1) (2) P10-7
37.02 EXCL. OR TO ACC. (2) Q10-1
23.23 F.P. MPY 2ND. STEP SHIFT CTR. ZERO, ACC. (9) J10-4
122l.16 ER 11 (D1) L10-1
+10V
A
O
CF
2 PCF
P10-3 SHIFT ACC. (Q-8) LT
58.01-7f
58.02-7g
58.03-7b
58.04-80
58.05-79
TEST POINT CF0.8A
SHIFT LEFT CONTROL
Q10-8
TEST POINT OF PCF 03A
M10-6
5 PCF
M10-6
58.06-7f
58.07-124
58.08-7c
100
100
-30V
-30V
-30V
SHIFT ACC (9-35) LEFT

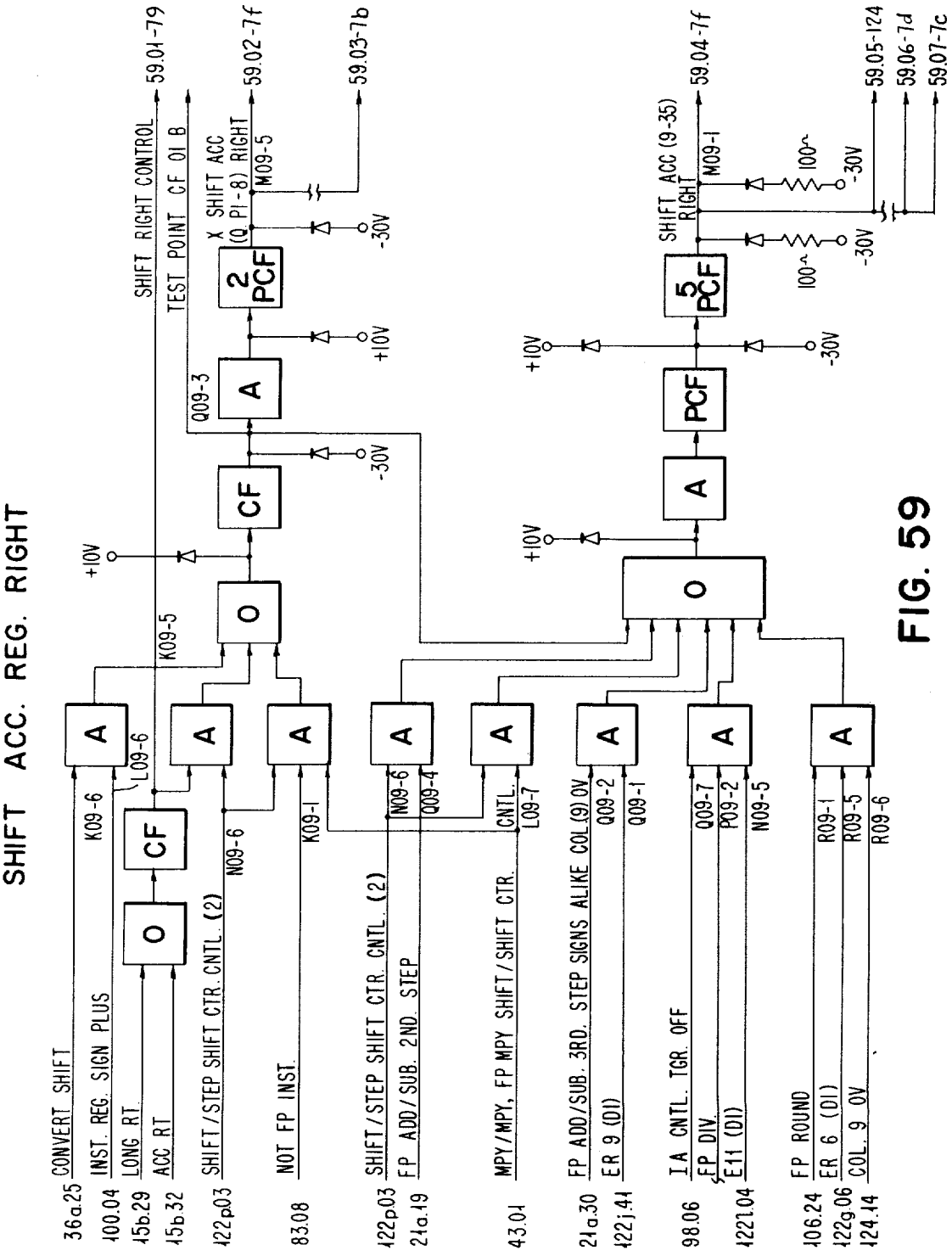

SHIFT ACC. REG. RIGHT
36a.25 CONVERT SHIFT
100.04 INST. REG. SIGN PLUS
45b.29 LONG RT
45b.32 ACC RT
422p03 SHIFT/STEP SHIFT CTR. CNTL. (2)
83.08 NOT FP INST.
422p03 SHIFT/STEP SHIFT CTR. CNTL. (2)
21a.19 FP ADD/SUB. 2ND. STEP
43.01 MPY/MPY, FP MPY SHIFT/SHIFT CTR.
21a.30 FP ADD/SUB. 3RD. STEP SIGNS ALIKE COL (9) 0V
422j.41 ER 9 (01)
98.06 IA CNTL. TGR. OFF
FP DIV.
422l.04 E11 (01)
106.24 FP ROUND
122g.06 ER 6 (01)
124.14 COL. 9 0V
K09-6
L09-6
K09-5
N09-6
K09-1
N09-6
Q09-4
CNTL.
L09-7
Q09-2
Q09-1
Q09-7
P09-2
N09-5
R09-1
R09-5
R09-6
A
O
CF
PCF
+10V
-30V
Q09-3
2 PCF
5 PCF
SHIFT RIGHT CONTROL
59.01-79
TEST POINT CF 01 B
X SHIFT ACC (Q P1-8) RIGHT
M09-5
59.02-7f
59.03-7b
SHIFT ACC (9-35) RIGHT
M09-1
59.04-7f
100Ω
59.05-12d
59.06-7d
59.07-7c

FIG. 59

MQ (S), (1) OR(9) TO ACC. (35), 1 TO ACC. (35)

FIG. 60

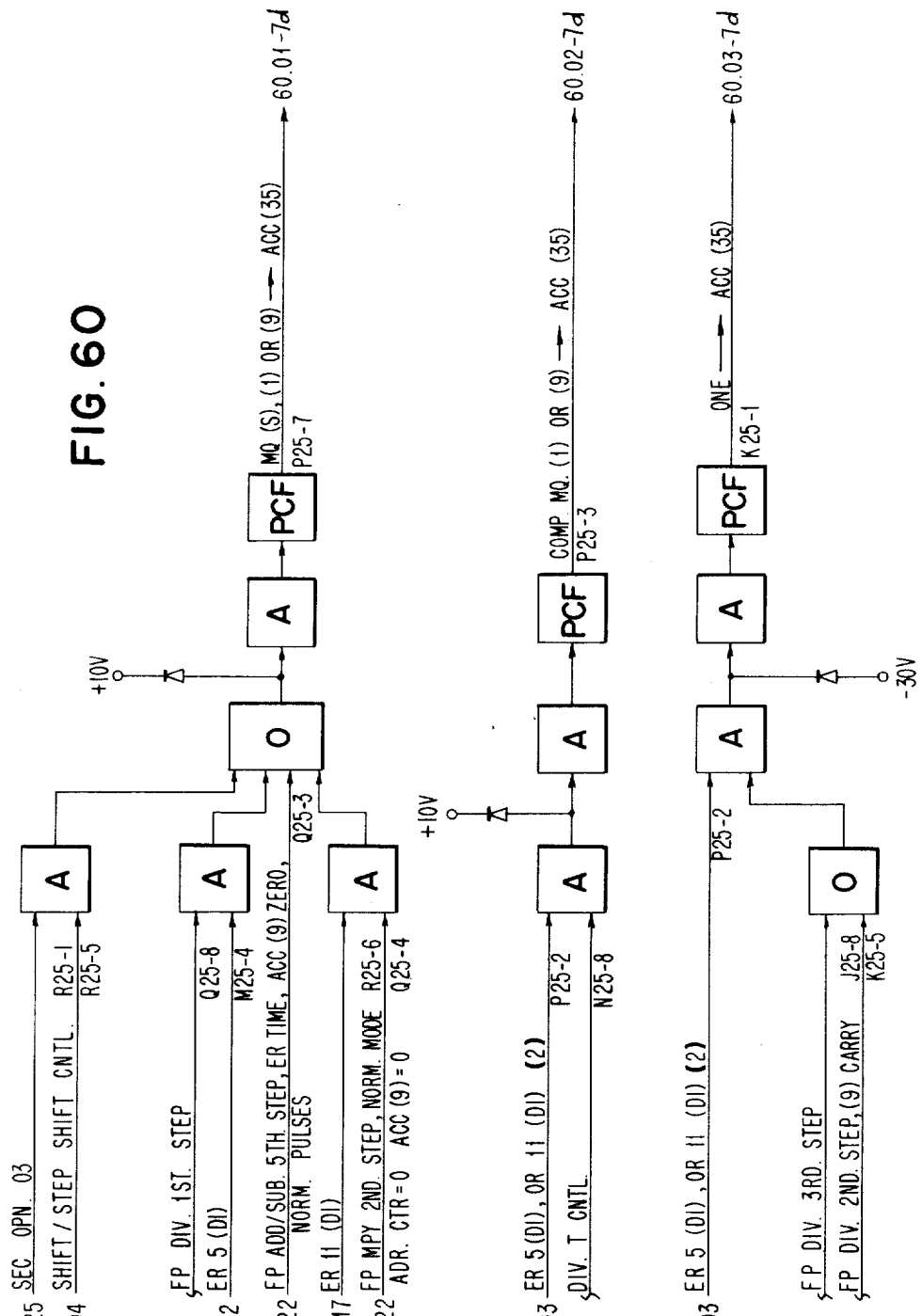
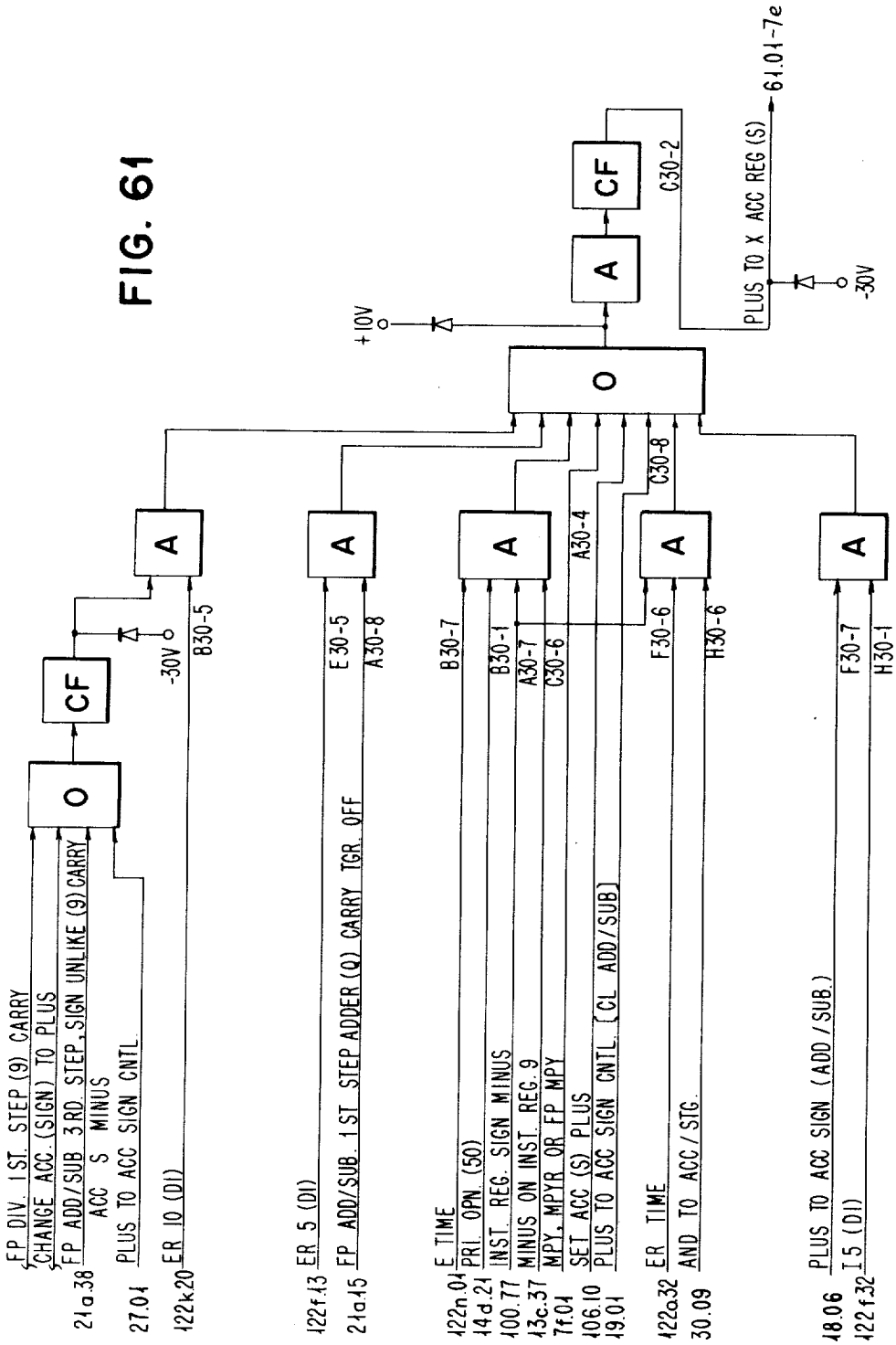


FIG. 61

PLUS TO ACC. REG. (S)



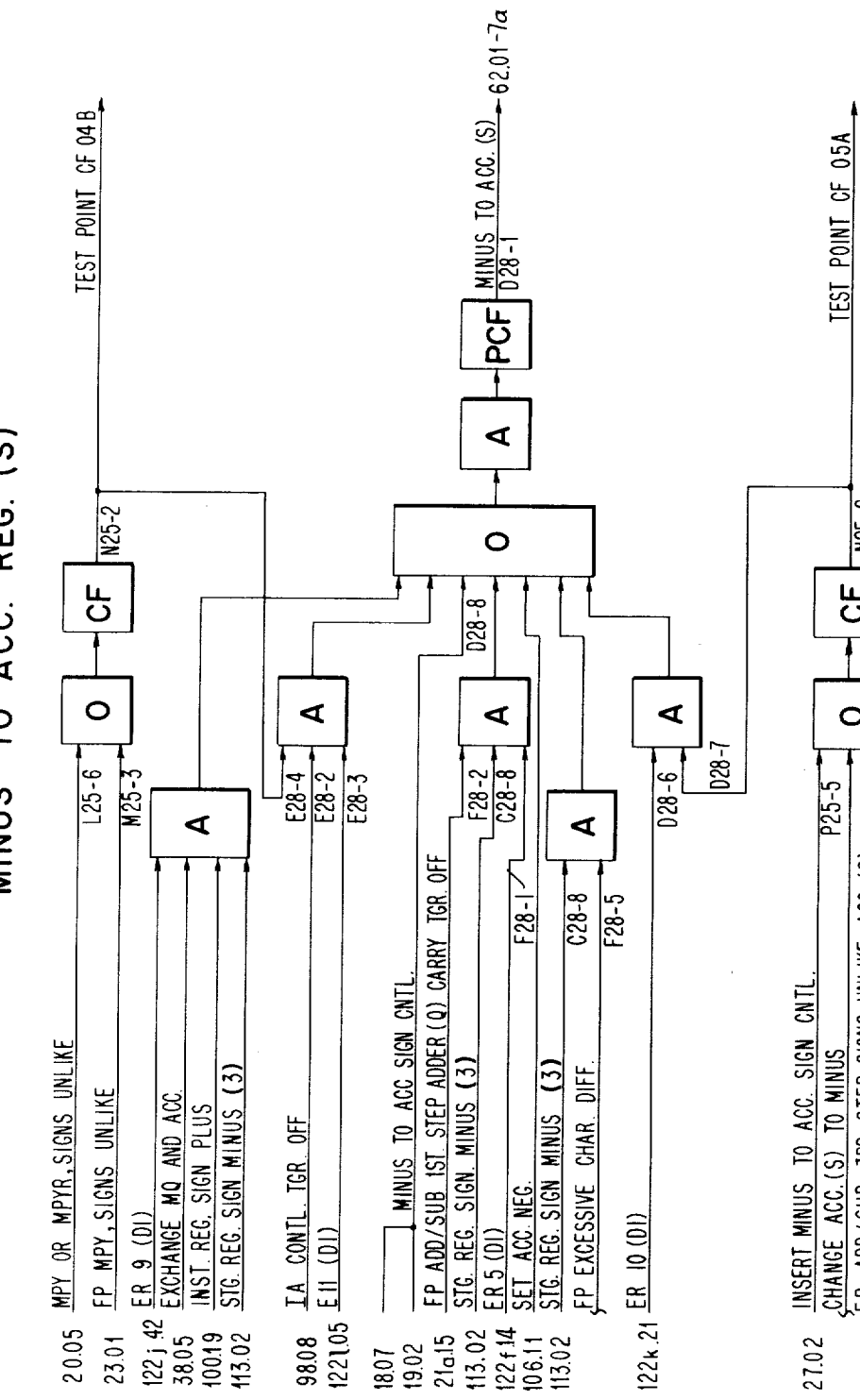
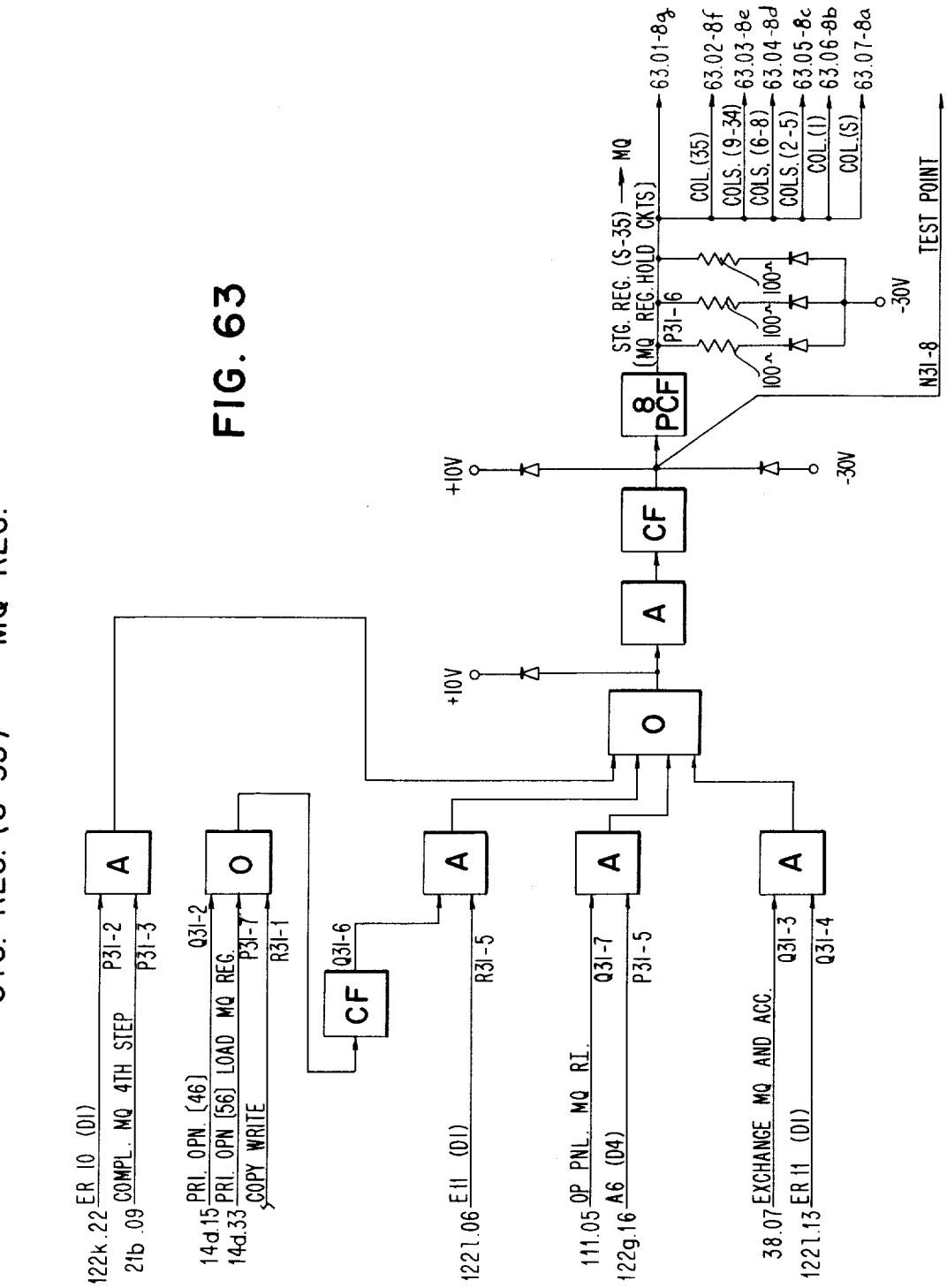

MINUS TO ACC. REG. (S)
20.05 MPY OR MPYR, SIGNS UNLIKE
23.01 FP MPY, SIGNS UNLIKE
122j.42 ER 9 (DI)
38.05 EXCHANGE MQ AND ACC
100.19 INST. REG. SIGN PLUS
113.02 STG. REG. SIGN MINUS (3)
98.08 IA CONTL. TGR. OFF
122l.05 E11 (DI)
18.07 MINUS TO ACC SIGN CNTL.
19.02 FP ADD/SUB 1ST. STEP ADDER (Q) CARRY TGR. OFF
21a.15 STG. REG. SIGN MINUS (3)
113.02 ER 5 (DI)
122f.14 SET ACC. NEG.
106.11 STG. REG. SIGN MINUS (3)
113.02 FP EXCESSIVE CHAR. DIFF.
122k.21 ER 10 (DI)
27.02 INSERT MINUS TO ACC. SIGN CNTL.
CHANGE ACC. (S) TO MINUS
21a.41 FP ADD/SUB. 3RD. STEP SIGNS UNLIKE ACC (S)
PLUS (9) CARRY
L25-6
M25-3
E28-4
E28-2
E28-3
F28-2
C28-8
F28-1
C28-8
F28-5
D28-6
D28-7
D28-8
P25-5
N25-7
N25-6
N25-2
D28-1
O
A
CF
PCF
TEST POINT CF 04 B
TEST POINT CF 05A
MINUS TO ACC. (S)
62.01-7a

FIG. 62

FIG. 63


STG. REG. (S-35) → MQ REG.
122k.22 ER 10 (01)
21b .09 COMPL. MQ 4TH STEP
P31-2
P31-3
A
14d.15 PRI. OPN. (46)
14d.33 PRI. OPN (56) LOAD MQ REG.
COPY WRITE
Q31-2
P31-7
R31-1
O
Q31-6
CF
1221.06 E11 (01)
R31-5
A
111.05 OP PNL. MQ RI.
122g.16 A6 (04)
Q31-7
P31-5
A
38.07 EXCHANGE MQ AND ACC.
1221.13 ER 11 (01)
Q31-3
Q31-4
A
+10V
+10V
O
A
CF
8 PCF
STG. REG. (S-35) → MQ (MQ REG. HOLD CKTS)
P31-6
100Ω
100Ω
100Ω
100Ω
-30V
-30V
N31-8
TEST POINT
COL. (35)
COLS. (9-34)
COLS. (6-8)
COLS. (2-5)
COL. (1)
COL. (S)
63.01-8g
63.02-8f
63.03-8e
63.04-8d
63.05-8c
63.06-8b
63.07-8a

SHIFT MQ RIGHT

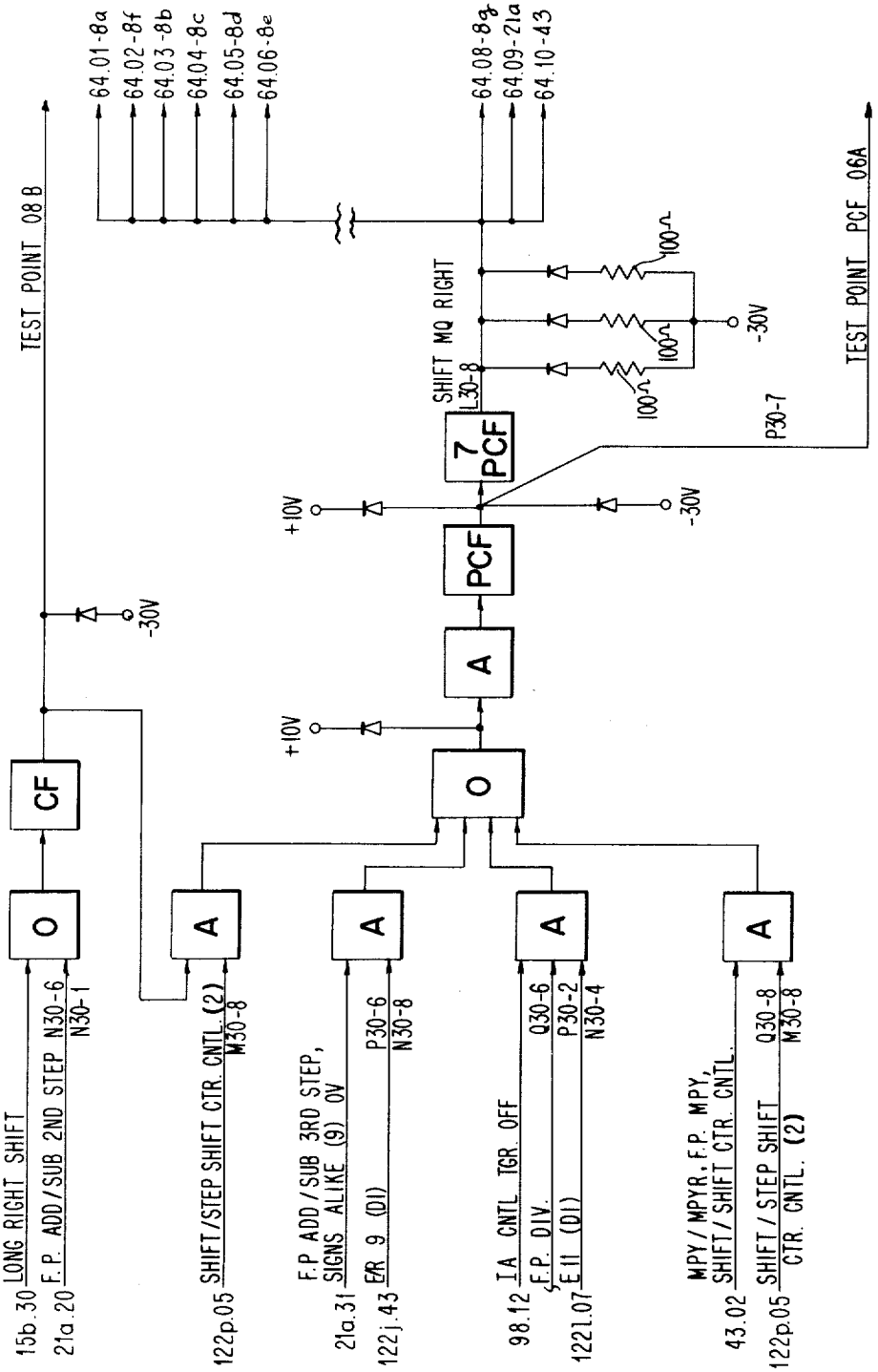


FIG. 64

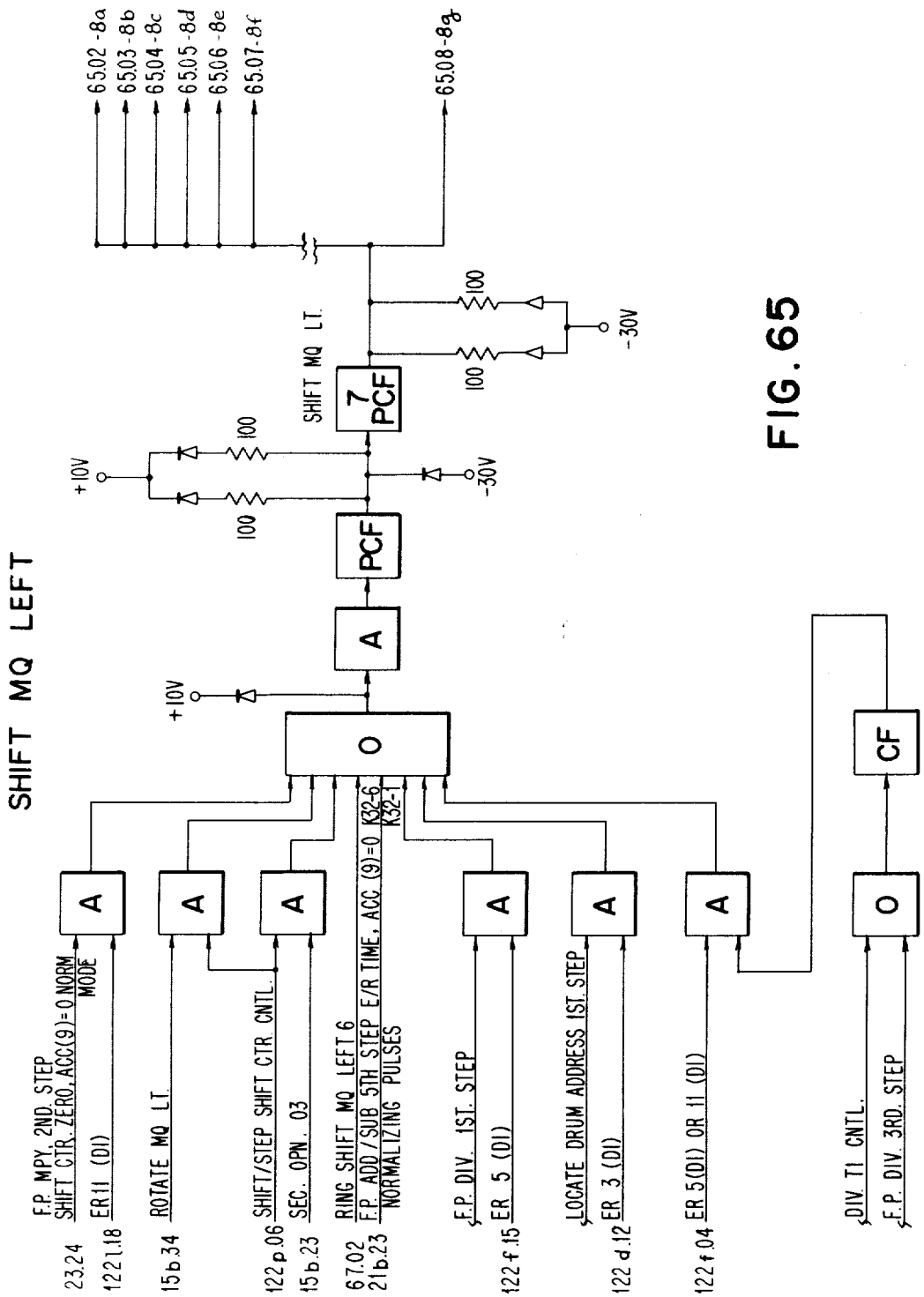

SHIFT MQ LEFT
65.02 -8a
65.03 -8b
65.04 -8c
65.05 -8d
65.06 -8e
65.07 -8f
65.08 -8g
SHIFT MQ LT.
7 PCF
PCF
A
O
CF
100
-30V
+10V
F.P. MPY. 2ND. STEP
SHIFT CTR. ZERO, ACC(9)=0 NORM MODE
23.24
ER 11 (DI)
1221.18
ROTATE MQ LT.
15b.34
SHIFT/STEP SHIFT CTR CNTL.
122 p.06
SEC. OPN. 03
15b.23
RING SHIFT MQ LEFT 6
67.02
F.P. ADD/SUB 5TH STEP E/R TIME, ACC (9)=0 K32-6 K32-1
21b.23
NORMALIZING PULSES
F.P. DIV. 1ST. STEP
ER 5 (DI)
122 f.15
LOCATE DRUM ADDRESS 1ST. STEP
ER 3 (DI)
122 d.12
ER 5(DI) OR 11 (DI)
122 f.04
DIV. T1 CNTL.
F.P. DIV. 3RD. STEP

FIG. 65

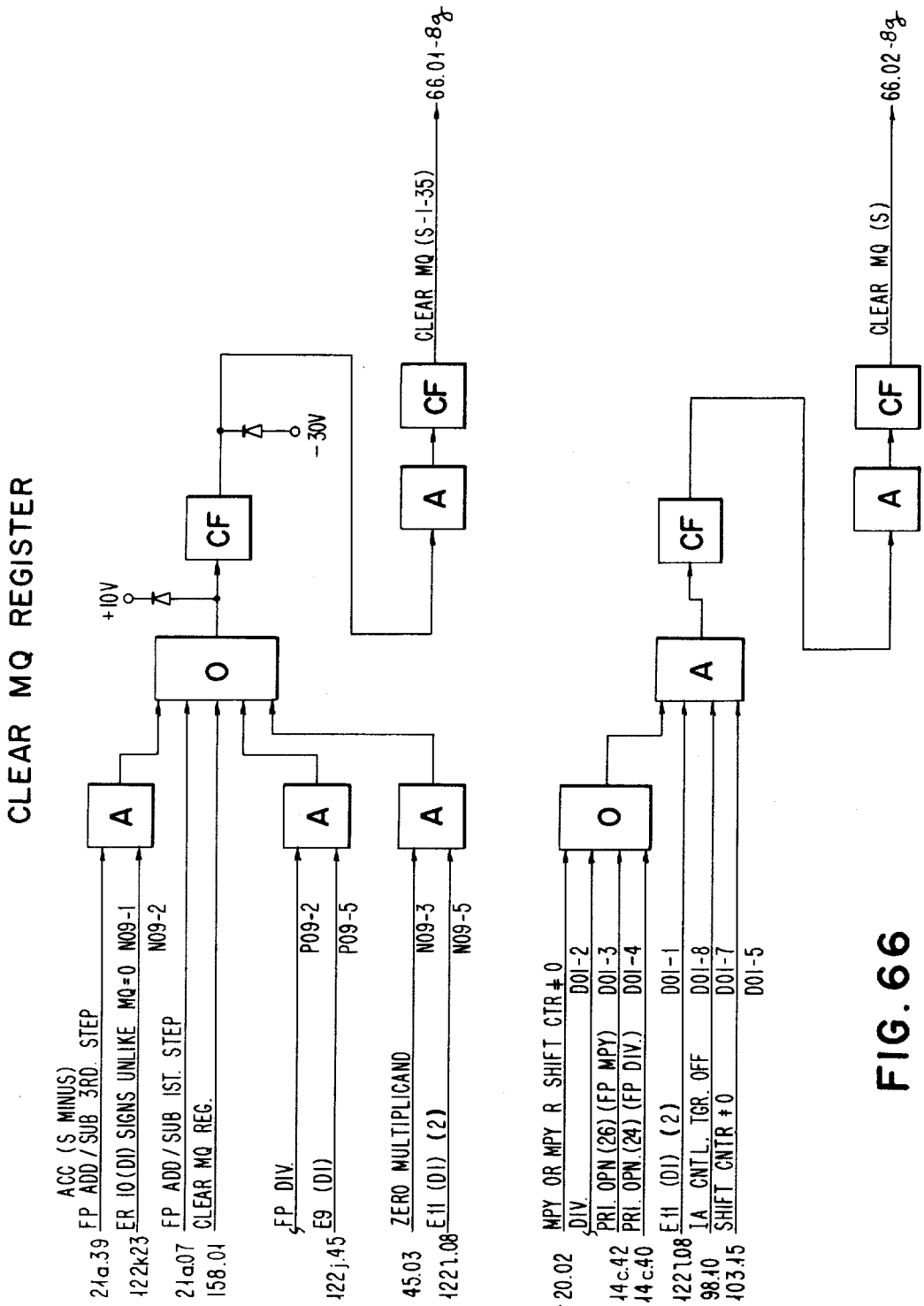
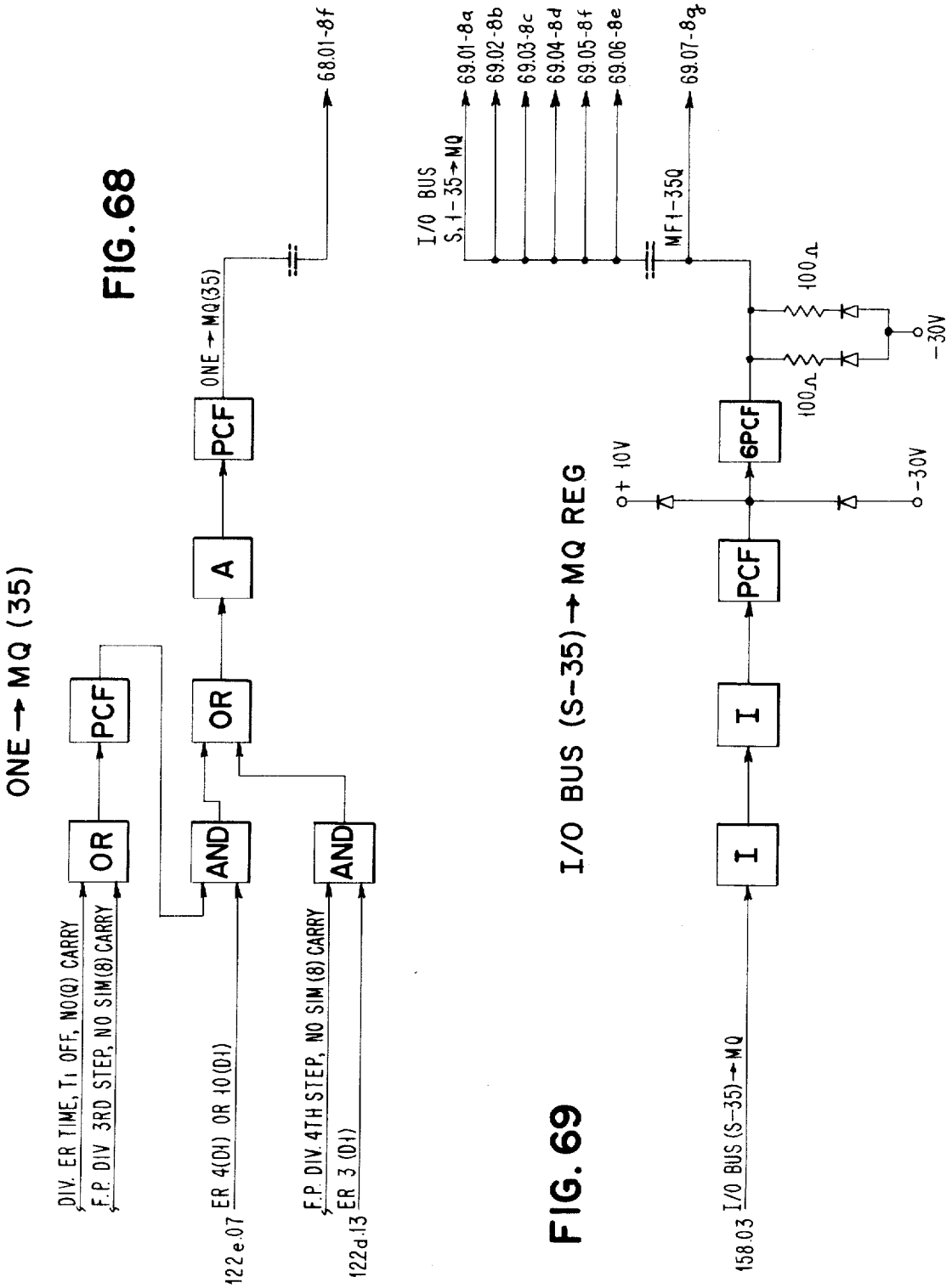

CLEAR MQ REGISTER
ACC (S MINUS)
21a.39 FP ADD/SUB 3RD. STEP
122k23 ER 10(D1) SIGNS UNLIKE MQ=0 N09-1
N09-2
21a.07 FP ADD/SUB 1ST. STEP
158.01 CLEAR MQ REG.
FP DIV.
122j.45 E9 (D1) P09-2
P09-5
45.03 ZERO MULTIPLICAND N09-3
1221.08 E11 (D1) (2) N09-5
+10V
-30V
A
O
CF
CLEAR MQ (S-1-35)
66.01-8g
20.02 MPY OR MPY R SHIFT CTR ≠ 0
DIV. D01-2
14c.42 PRI. OPN (26) (FP MPY) D01-3
14c.40 PRI. OPN (24) (FP DIV.) D01-4
1221.08 E11 (D1) (2) D01-1
98.10 IA CNTL. TGR. OFF D01-8
103.15 SHIFT CNTR ≠ 0 D01-7
D01-5
CLEAR MQ (S)
66.02-8g

FIG. 66


ONE → MQ (35)
DIV. ER TIME, T1 OFF, NO(Q) CARRY
F.P. DIV 3RD STEP, NO SIM (8) CARRY
OR
PCF
122 e.07 ER 4(D1) OR 10 (D1)
AND
OR
A
PCF
ONE → MQ(35)
68.01-8f
F.P. DIV. 4TH STEP, NO SIM (8) CARRY
122d.13 ER 3 (D1)
AND
FIG. 68
I/O BUS (S-35) → MQ REG
158 03 I/O BUS (S-35) → MQ
I
I
PCF
+ 10V
6PCF
-30V
100Ω
100Ω
-30V
MF1-35Q
I/O BUS S,1-35 → MQ
69.01-8a
69.02-8b
69.03-8c
69.04-8d
69.05-8f
69.06-8e
69.07-8g
FIG. 69

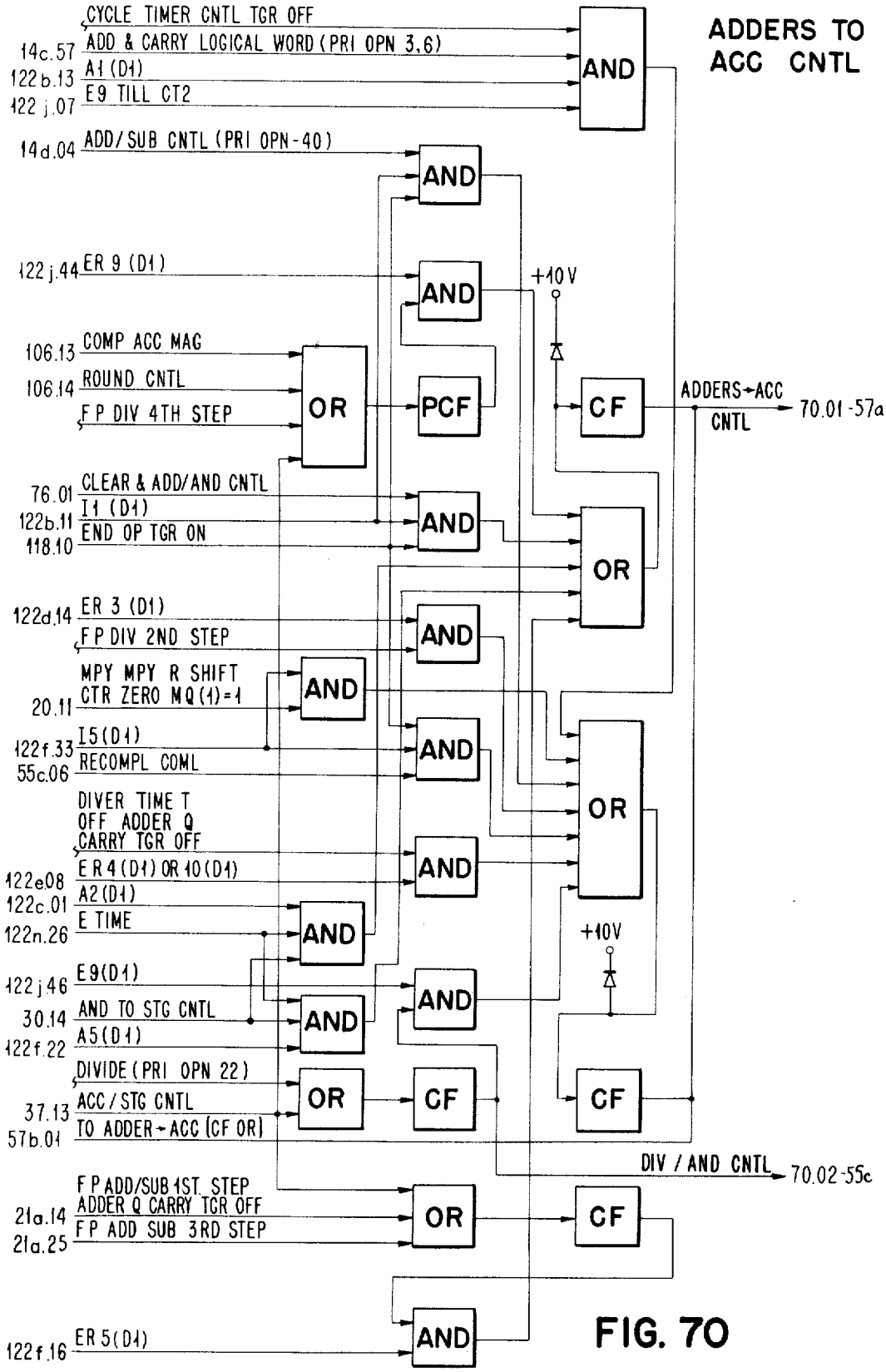

CYCLE TIMER CNTL TGR OFF
14c.57 ADD & CARRY LOGICAL WORD (PRI OPN 3,6)
122b.13 A1 (D1)
122j.07 E9 TILL CT2
AND
ADDERS TO ACC CNTL
14d.04 ADD/SUB CNTL (PRI OPN-40)
AND
122j.44 ER 9 (D1)
AND
+10V
106.13 COMP ACC MAG
106.14 ROUND CNTL
F P DIV 4TH STEP
OR
PCF
CF
ADDERS→ACC CNTL
70.01-57a
76.01 CLEAR & ADD/AND CNTL
122b.11 I1 (D1)
118.10 END OP TGR ON
AND
OR
122d.14 ER 3 (D1)
F P DIV 2ND STEP
AND
MPY MPY R SHIFT CTR ZERO MQ(1)=1
20.11
AND
122f.33 I5(D1)
55c.06 RECOMPL COML
AND
OR
DIVER TIME T OFF ADDER Q CARRY TGR OFF
AND
122e.08 E R 4 (D1) OR 10 (D1)
122c.01 A2(D1)
122n.26 E TIME
AND
+10V
122j.46 E9(D1)
AND
30.14 AND TO STG CNTL
122f.22 A5(D1)
AND
DIVIDE (PRI OPN 22)
37.13 ACC/STG CNTL
57b.01 TO ADDER-ACC (CF OR)
OR
CF
CF
DIV / AND CNTL
70.02-55c
F P ADD/SUB 1ST. STEP
21a.14 ADDER Q CARRY TGR OFF
21a.25 F P ADD SUB 3RD STEP
OR
CF
122f.16 ER 5(D1)
AND

FIG. 70

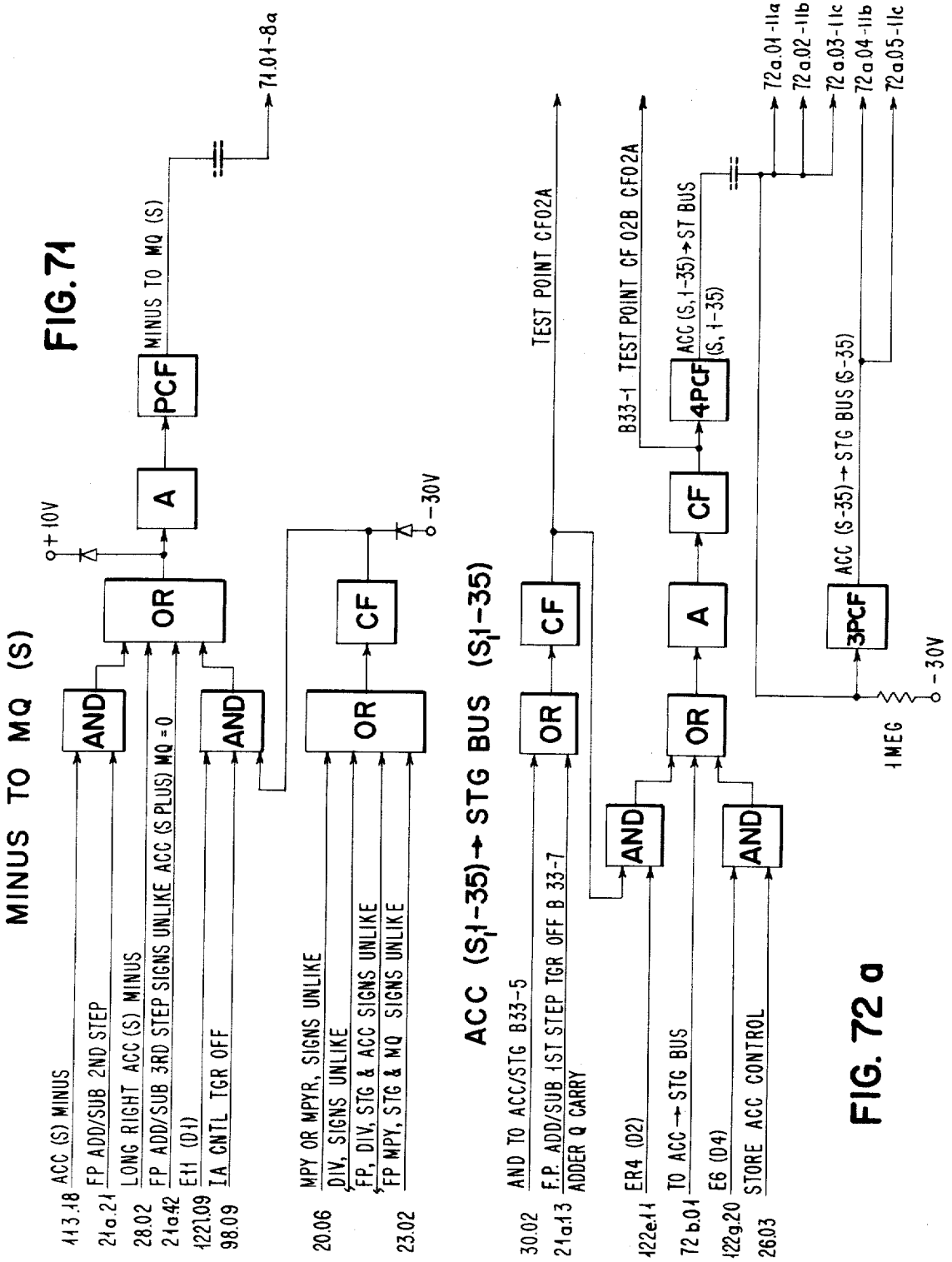
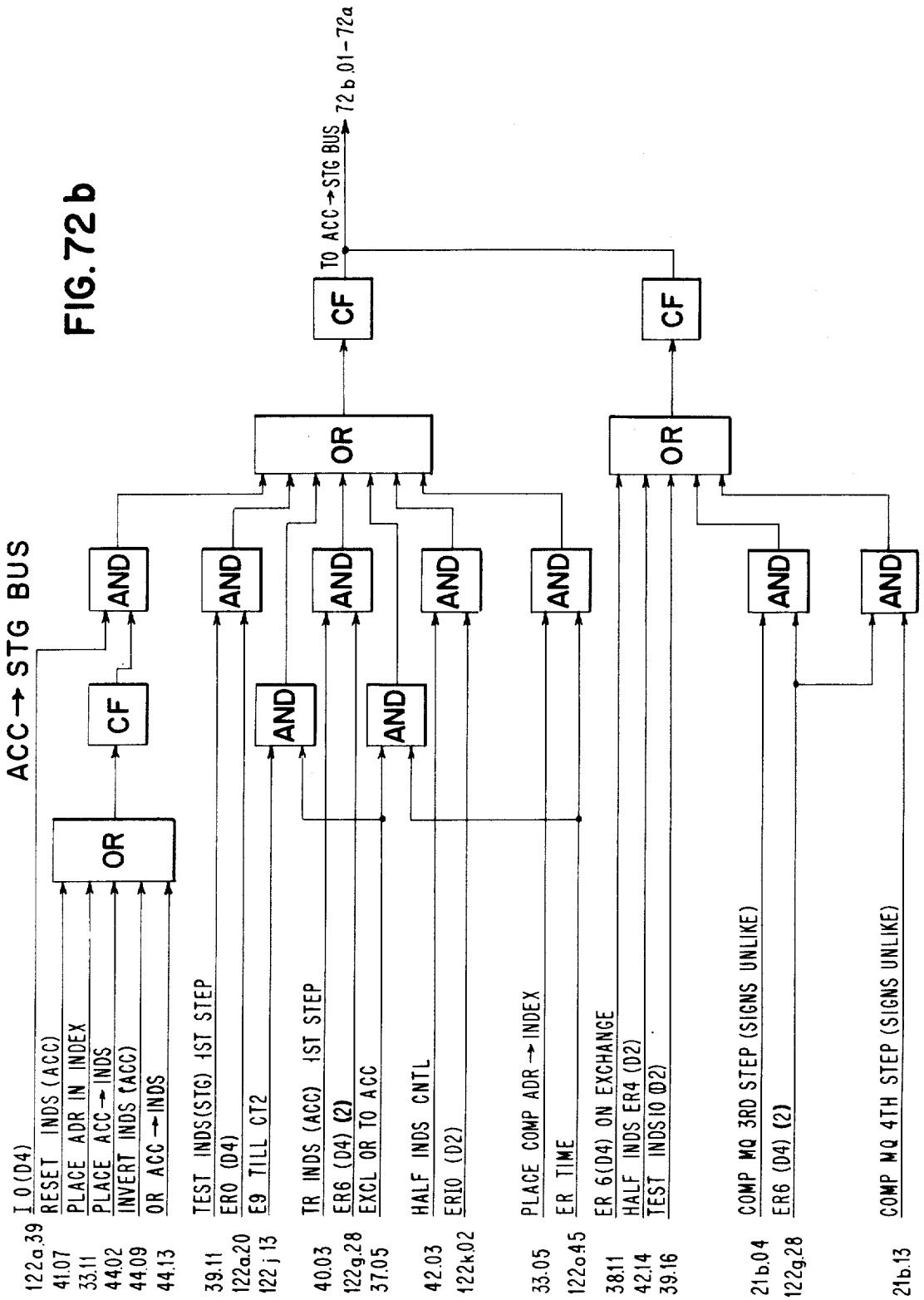


FIG. 71

FIG. 72a

FIG. 72b


ACC→STG BUS
122a.39 I 0(D4)
41.07 RESET INDS (ACC)
33.11 PLACE ADR IN INDEX
44.02 PLACE ACC→INDS
44.09 INVERT INDS (ACC)
44.13 OR ACC→INDS
OR
CF
AND
39.11 TEST INDS(STG) 1ST STEP
122a.20 ERO (D4)
122 j 13 E9 TILL CT2
40.03 TR INDS (ACC) 1ST STEP
122g.28 ER6 (D4) (2)
37.05 EXCL OR TO ACC
42.03 HALF INDS CNTL
122k.02 ERIO (D2)
33.05 PLACE COMP ADR→INDEX
122a.45 ER TIME
38.11 ER 6(D4) ON EXCHANGE
42.14 HALF INDS ER4 (D2)
39.16 TEST INDS10 (D2)
21b.04 COMP MQ 3RD STEP (SIGNS UNLIKE)
122g.28 ER6 (D4) (2)
21b.13 COMP MQ 4TH STEP (SIGNS UNLIKE)
TO ACC→STG BUS 72b.01-72a

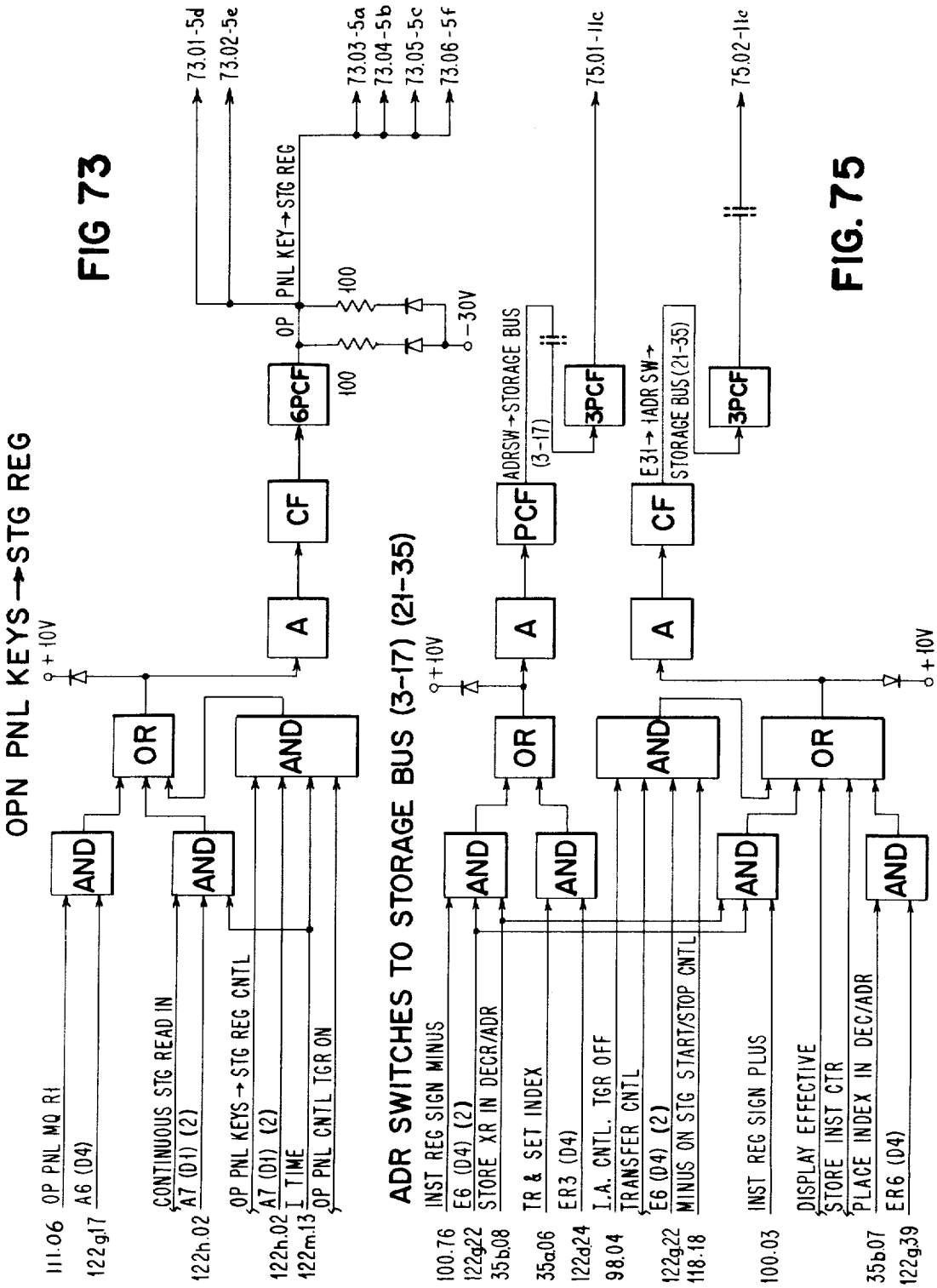

OPN PNL KEYS→STG REG
111.06 OP PNL MQ RI
122g17 A6 (D4)
122h.02 CONTINUOUS STG READ IN A7 (D1) (2)
122h.02 OP PNL KEYS→STG REG CNTL A7 (D1) (2)
122m.13 I TIME
OP PNL CNTL TGR ON
AND
OR
AND
A
CF
6PCF
+10V
100
100
-30V
OP PNL KEY→STG REG
73.01-5d
73.02-5e
73.03-5a
73.04-5b
73.05-5c
73.06-5f
FIG 73
ADR SWITCHES TO STORAGE BUS (3-17) (21-35)
100.76 INST REG SIGN MINUS
122g22 E6 (D4) (2)
35b08 STORE XR IN DECR/ADR
35a06 TR & SET INDEX
122d24 ER3 (D4)
98.04 I.A. CNTL. TGR OFF
122g22 TRANSFER CNTL E6 (D4) (2)
118.18 MINUS ON STG START/STOP CNTL
100.03 INST REG SIGN PLUS
DISPLAY EFFECTIVE
STORE INST CTR
35b07 PLACE INDEX IN DEC/ADR
122g39 ER6 (D4)
AND
OR
AND
A
PCF
3PCF
ADRSW→STORAGE BUS (3-17)
75.01-11c
AND
A
CF
3PCF
E31→1ADR SW→ STORAGE BUS (21-35)
75.02-11c
+10V
FIG. 75

FIG. 74

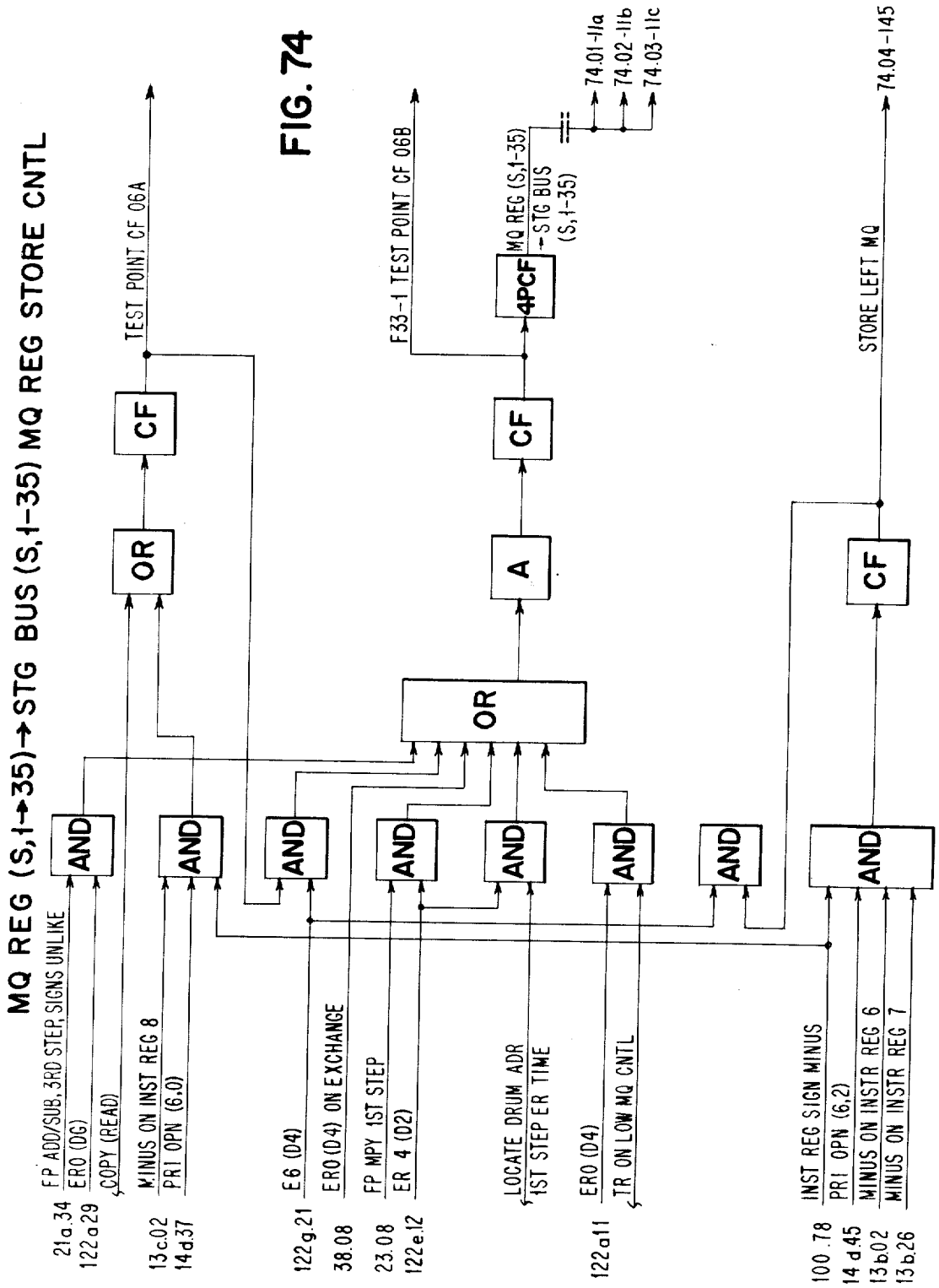

MQ REG (S,1→35)→STG BUS (S,1-35) MQ REG STORE CNTL
21a.34 FP ADD/SUB, 3RD STEP, SIGNS UNLIKE
122a29 ERO (DG)
COPY (READ)
13c.02 MINUS ON INST REG 8
14d.37 PR1 OPN (6,0)
122g.21 E6 (D4)
38.08 ERO (D4) ON EXCHANGE
23.08 FP MPY 1ST STEP
122e.12 ER 4 (D2)
LOCATE DRUM ADR
1ST STEP ER TIME
122a11 ERO (D4)
TR ON LOW MQ CNTL
100.78 INST REG SIGN MINUS
14d.45 PR1 OPN (6,2)
13b.02 MINUS ON INSTR REG 6
13b.26 MINUS ON INSTR REG 7
AND
OR
CF
A
4PCF
TEST POINT CF 06A
F33-1 TEST POINT CF 06B
MQ REG (S,1-35) → STG BUS (S,1-35)
STORE LEFT MQ
74.01-11a
74.02-11b
74.03-11c
74.04-145

FIG. 76

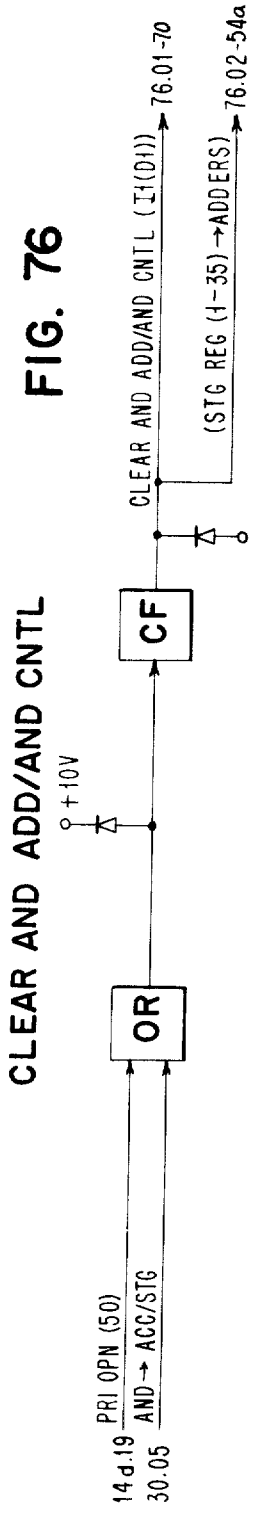

CLEAR AND ADD/AND CNTL
+10V
-30V
CF
OR
CLEAR AND ADD/AND CNTL (I1(01))
(STG REG (1-35) → ADDERS)
76.01-70
76.02-54a
14d.19 PRI OPN (50)
30.05 AND → ACC/STG

FIG. 77

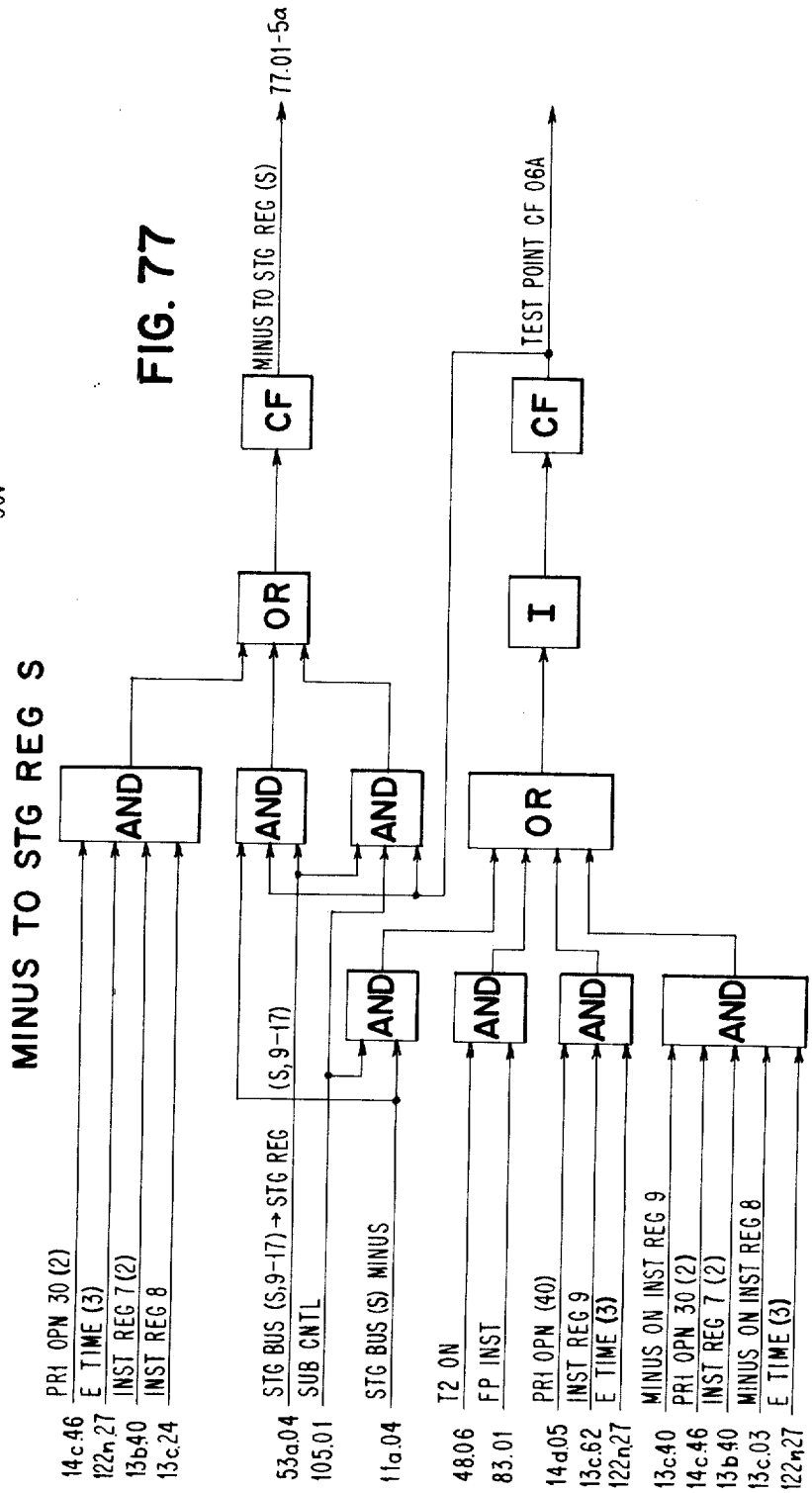

MINUS TO STG REG S
AND
OR
CF
I
MINUS TO STG REG (S)
77.01-5a
TEST POINT CF 06A
14c.46 PRI OPN 30 (2)
122n.27 E TIME (3)
13b40 INST REG 7 (2)
13c24 INST REG 8
53a.04 STG BUS (S,9-17) → STG REG
105.01 SUB CNTL
(S, 9-17)
11a.04 STG BUS (S) MINUS
48.06 T2 ON
83.01 FP INST
14d05 PRI OPN (40)
13c.62 INST REG 9
122n27 E TIME (3)
13c40 MINUS ON INST REG 9
14c46 PRI OPN 30 (2)
13b40 INST REG 7 (2)
13c.03 MINUS ON INST REG 8
122n27 E TIME (3)

FIG. 78

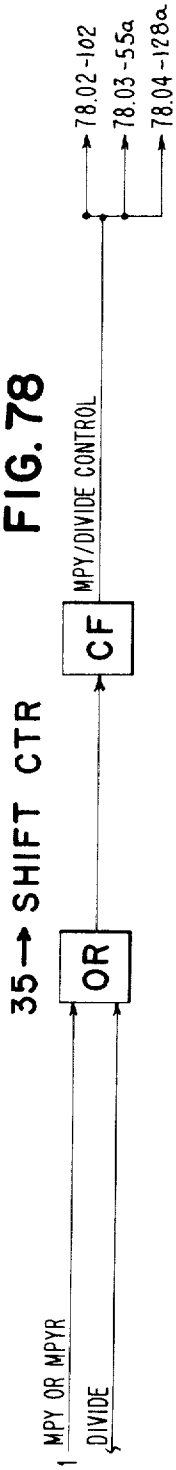
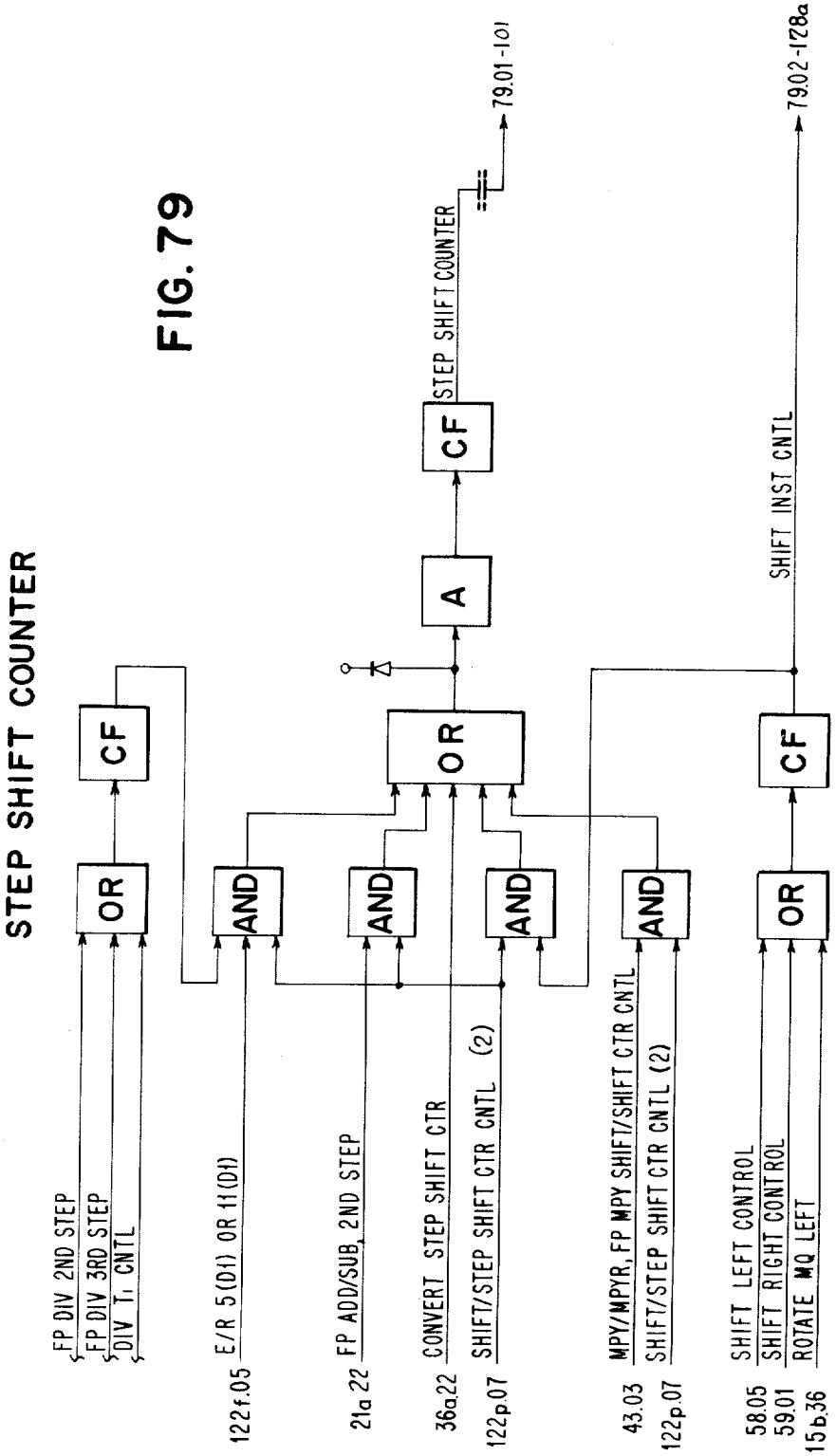
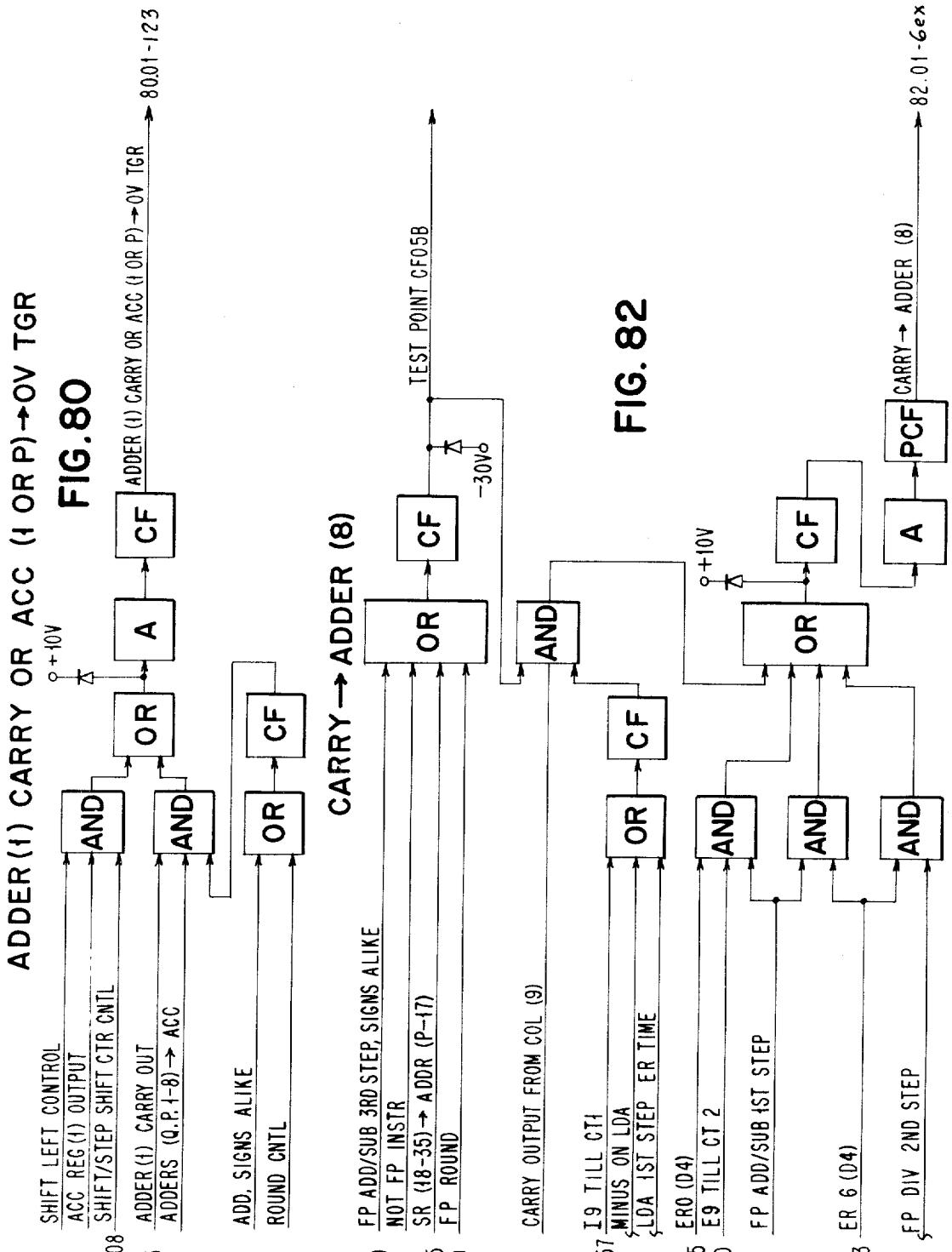

35→ SHIFT CTR
OR
CF
MPY/DIVIDE CONTROL
78.02-102
78.03-55a
78.04-128a
20.01
MPY OR MPYR
DIVIDE

FIG. 79


STEP SHIFT COUNTER
CF
OR
AND
A
OR
CF
STEP SHIFT COUNTER
79.01-101
SHIFT INST CNTL
79.02-128a
FP DIV 2ND STEP
FP DIV 3RD STEP
DIV T1 CNTL
122f.05
E/R 5(D1) OR 11(D1)
21a 22
FP ADD/SUB, 2ND STEP
36a,22
CONVERT STEP SHIFT CTR
122p.07
SHIFT/STEP SHIFT CTR CNTL (2)
43.03
MPY/MPYR, FP MPY SHIFT/SHIFT CTR CNTL
122p.07
SHIFT/STEP SHIFT CTR CNTL (2)
58.05
SHIFT LEFT CONTROL
59.01
SHIFT RIGHT CONTROL
15b.36
ROTATE MQ LEFT


ADDER (1) CARRY OR ACC (1 OR P)→OV TGR
FIG. 80
SHIFT LEFT CONTROL
ACC REG (1) OUTPUT
SHIFT/STEP SHIFT CTR CNTL
ADDER (1) CARRY OUT
ADDERS (Q, P, 1-8) → ACC
ADD. SIGNS ALIKE
ROUND CNTL
AND
OR
A
CF
+10V
ADDER (1) CARRY OR ACC (1 OR P)→OV TGR
80.01-123
58.04
7b.06
122p.08
6b.05
57a.05
18.01
106.17
CARRY→ ADDER (8)
FIG. 82
FP ADD/SUB 3RD STEP, SIGNS ALIKE
NOT FP INSTR
SR (18-35)→ ADDR (P-17)
FP ROUND
CARRY OUTPUT FROM COL (9)
I9 TILL CT1
MINUS ON LDA
LDA 1ST STEP ER TIME
ER0 (D4)
E9 TILL CT 2
FP ADD/SUB 1ST STEP
ER 6 (D4)
FP DIV 2ND STEP
TEST POINT CF05B
-30V
+10V
PCF
CARRY→ ADDER (8)
82.01-6ex
21a.29
83.06
86a.05
106.19
6f.03
122j.57
122a.15
122j.10
21a.11
122g.33

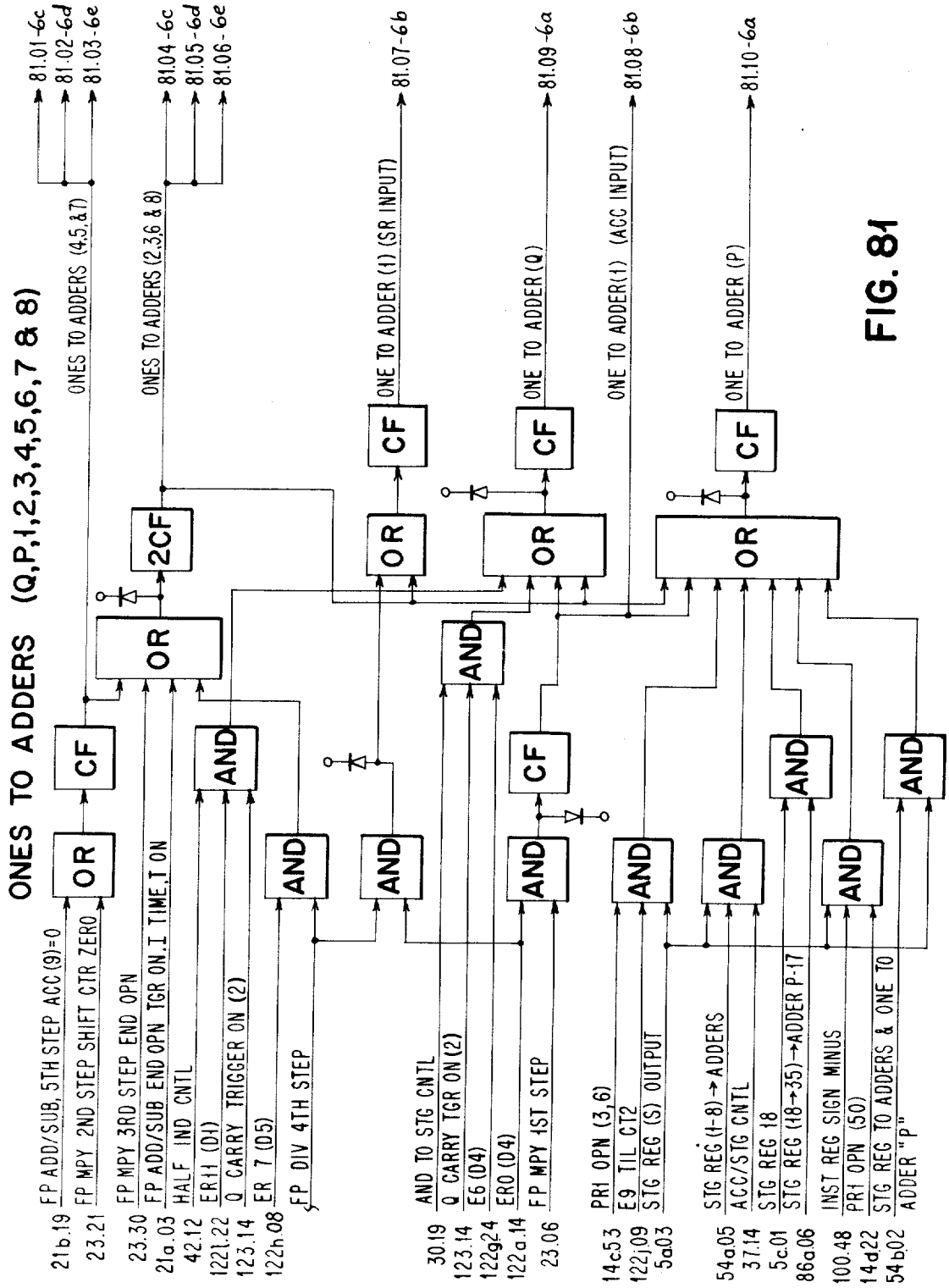

ONES TO ADDERS (Q,P,1,2,3,4,5,6,7 & 8)
21b.19 FP ADD/SUB, 5TH STEP ACC(9)=0
23.21 FP MPY 2ND STEP SHIFT CTR ZERO
OR
CF
ONES TO ADDERS (4,5,&7)
81.01-6c
81.02-6d
81.03-6e
23.30 FP MPY 3RD STEP END OPN
21a.03 FP ADD/SUB END OPN TGR ON.I TIME,I ON
42.12 HALF IND CNTL
1221.22 ER11 (D1)
123.14 Q CARRY TRIGGER ON (2)
122h.08 ER 7 (D5)
FP DIV 4TH STEP
OR
2CF
AND
AND
ONES TO ADDERS (2,3,6 & 8)
81.04-6c
81.05-6d
81.06-6e
30.19 AND TO STG CNTL
123.14 Q CARRY TGR ON (2)
122g24 E6 (D4)
122a.14 ER0 (D4)
23.06 FP MPY 1ST STEP
AND
AND
CF
OR
CF
ONE TO ADDER (1) (SR INPUT)
81.07-6b
14c.53 PR1 OPN (3,6)
122j.09 E9 TIL CT2
5a03 STG REG (S) OUTPUT
AND
AND
CF
OR
CF
ONE TO ADDER(Q)
81.09-6a
54a.05 STG REG (1-8)→ADDERS
37.14 ACC/STG CNTL
5c.01 STG REG 18
86a.06 STG REG (18→35)→ADDER P-17
100.48 INST REG SIGN MINUS
14d.22 PR1 OPN (50)
54b.02 STG REG TO ADDERS & ONE TO ADDER "P"
AND
AND
AND
AND
OR
CF
ONE TO ADDER(1) (ACC INPUT)
81.08-6b
ONE TO ADDER (P)
81.10-6a

FIG. 81

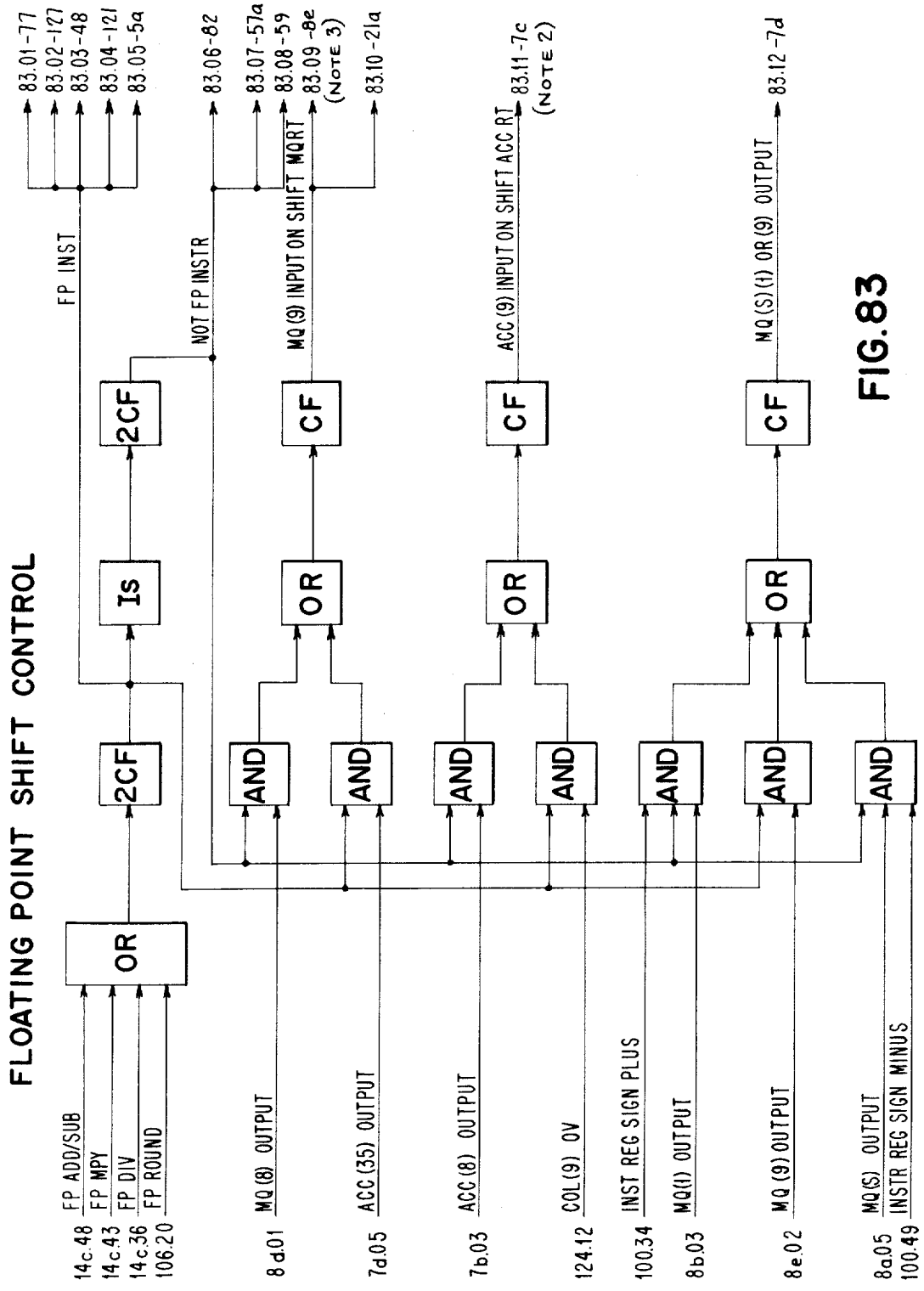

FLOATING POINT SHIFT CONTROL
14c.48 FP ADD/SUB
14c.43 FP MPY
14c.36 FP DIV
106.20 FP ROUND
OR
2CF
Is
2CF
FP INST
NOT FP INSTR
8d.01 MQ(8) OUTPUT
7d.05 ACC(35) OUTPUT
AND
AND
OR
CF
MQ(9) INPUT ON SHIFT MQRT
7b.03 ACC(8) OUTPUT
124.12 COL(9) 0V
AND
AND
OR
CF
ACC(9) INPUT ON SHIFT ACC RT
100.34 INST REG SIGN PLUS
8b.03 MQ(1) OUTPUT
8e.02 MQ(9) OUTPUT
8a.05 MQ(S) OUTPUT
100.49 INSTR REG SIGN MINUS
AND
AND
OR
CF
MQ(S)(1) OR(9) OUTPUT
83.01-77
83.02-127
83.03-48
83.04-121
83.05-5a
83.06-82
83.07-57a
83.08-59
83.09-8e (NOTE 3)
83.10-21a
83.11-7c (NOTE 2)
83.12-7d

FIG. 83

ADDERS (1-8)→MQ(1-8)

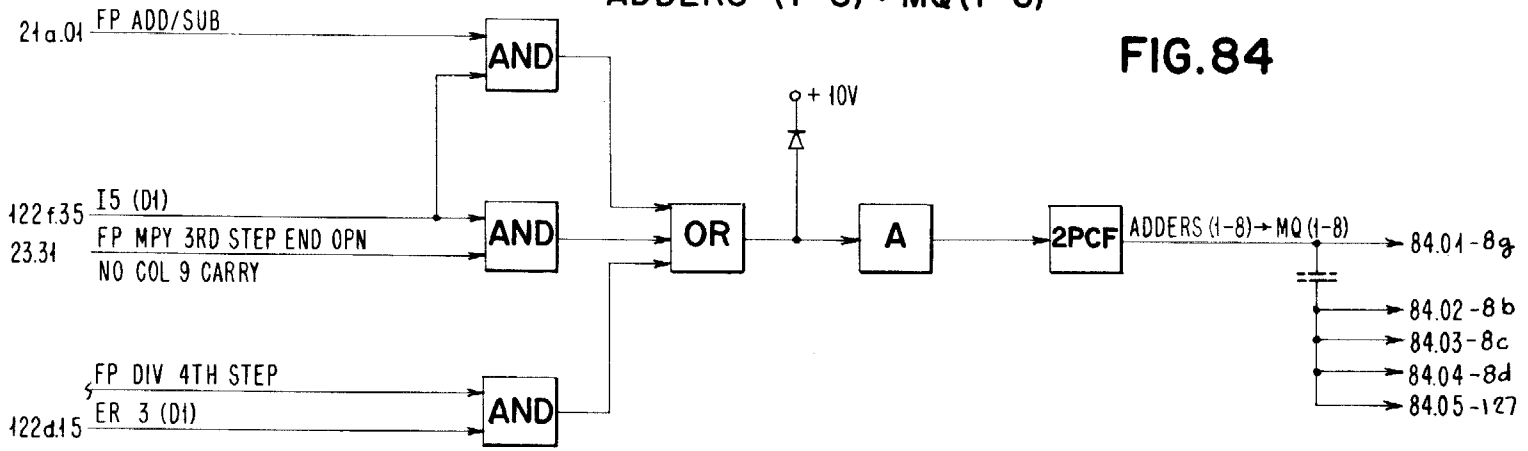


FIG. 84

STEP FLOATING POINT TALLY COUNTER

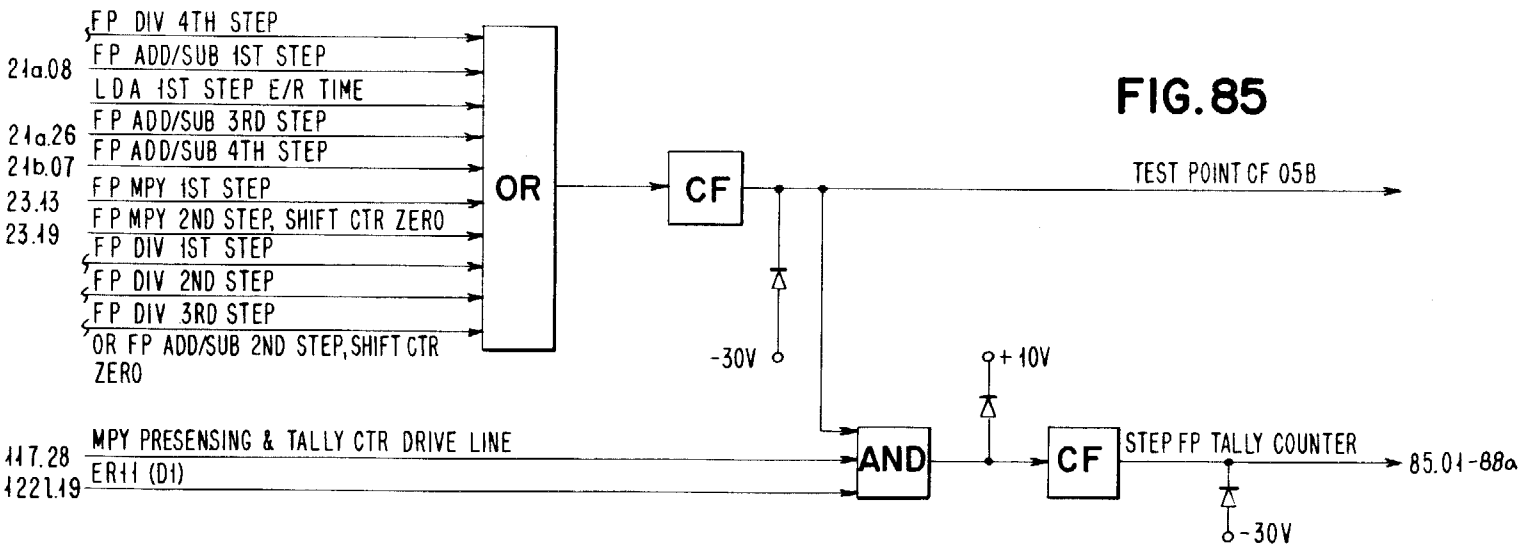


FIG. 85

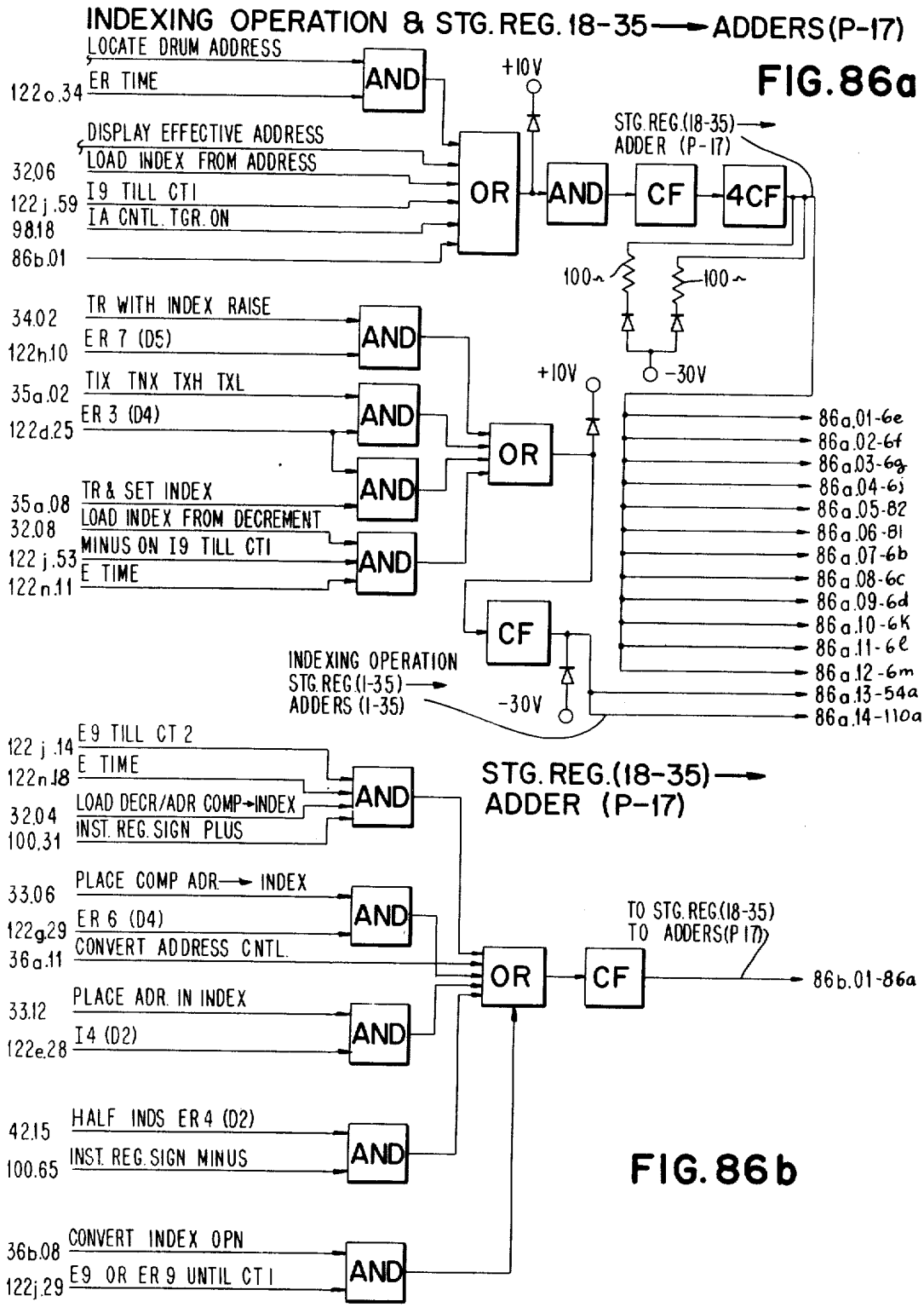


FIG. 86a

FIG. 86b

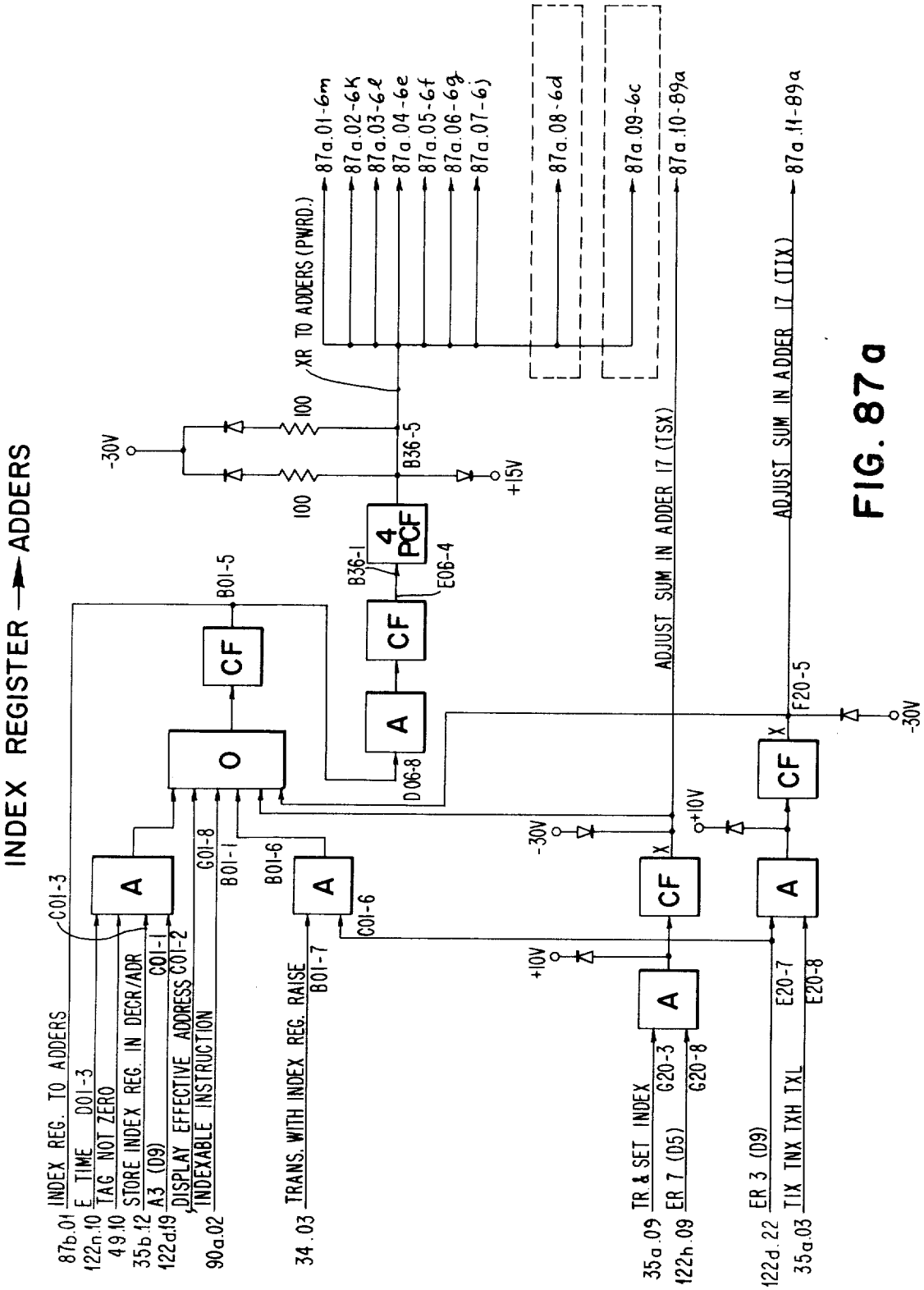

INDEX REGISTER → ADDERS
87b.01 INDEX REG. TO ADDERS
122n.10 E TIME D01-3
49.10 TAG NOT ZERO
35b.12 STORE INDEX REG. IN DECR/ADR
122d.19 A3 (09)
DISPLAY EFFECTIVE ADDRESS
INDEXABLE INSTRUCTION
90a.02
34.03 TRANS. WITH INDEX REG. RAISE
35a.09 TR & SET INDEX
122h.09 ER 7 (05)
122d.22 ER 3 (09)
35a.03 TIX TNX TXH TXL
C01-3
C01-1
C01-2
G01-8
B01-1
B01-6
B01-7
C01-6
G20-3
G20-8
E20-7
E20-8
A
O
CF
4 PCF
X
B01-5
B36-1
B36-5
E06-4
D06-8
F20-5
-30V
+15V
+10V
100
XR TO ADDERS (PWRD.)
87a.01-6m
87a.02-6k
87a.03-6l
87a.04-6e
87a.05-6f
87a.06-6g
87a.07-6j
87a.08-6d
87a.09-6c
87a.10-89a
87a.11-89a
ADJUST SUM IN ADDER 17 (TSX)
ADJUST SUM IN ADDER 17 (TIX)

FIG. 87a

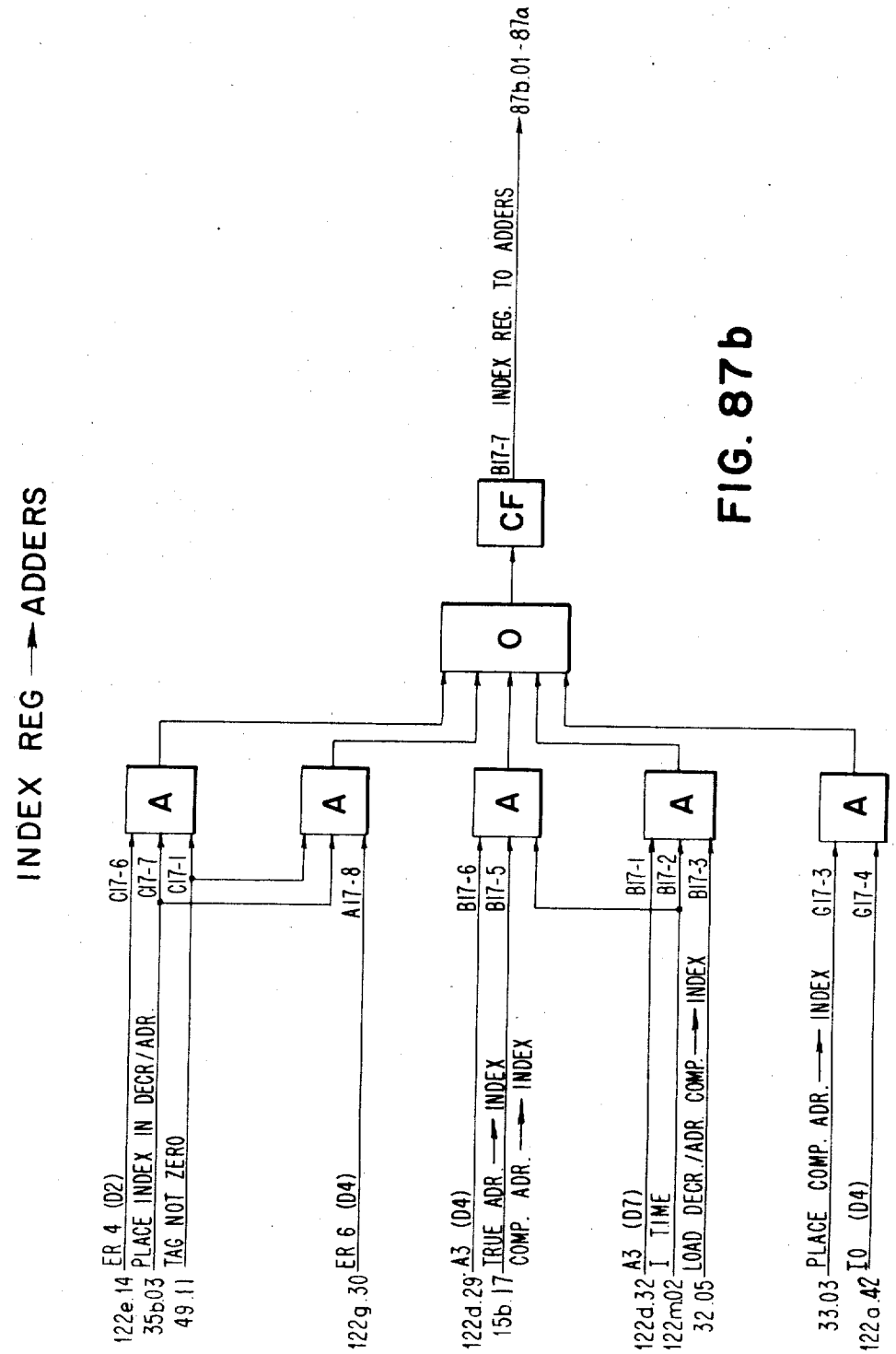

INDEX REG → ADDERS
122e.14 ER 4 (02)
35b03 PLACE INDEX IN DECR/ADR.
49.11 TAG NOT ZERO
C17-6
C17-7
C17-1
A
122g.30 ER 6 (04)
A17-8
122d.29 A3 (04)
15b 17 TRUE ADR. → INDEX
COMP. ADR. → INDEX
B17-6
B17-5
122d.32 A3 (07)
122m02 I TIME
32.05 LOAD DECR./ADR. COMP. → INDEX
B17-1
B17-2
B17-3
33.03 PLACE COMP. ADR. → INDEX
122a.42 IO (04)
G17-3
G17-4
O
CF
B17-7 INDEX REG. TO ADDERS → 87b.01-87a

FIG. 87b

FLOATING POINT TALLY COUNTER

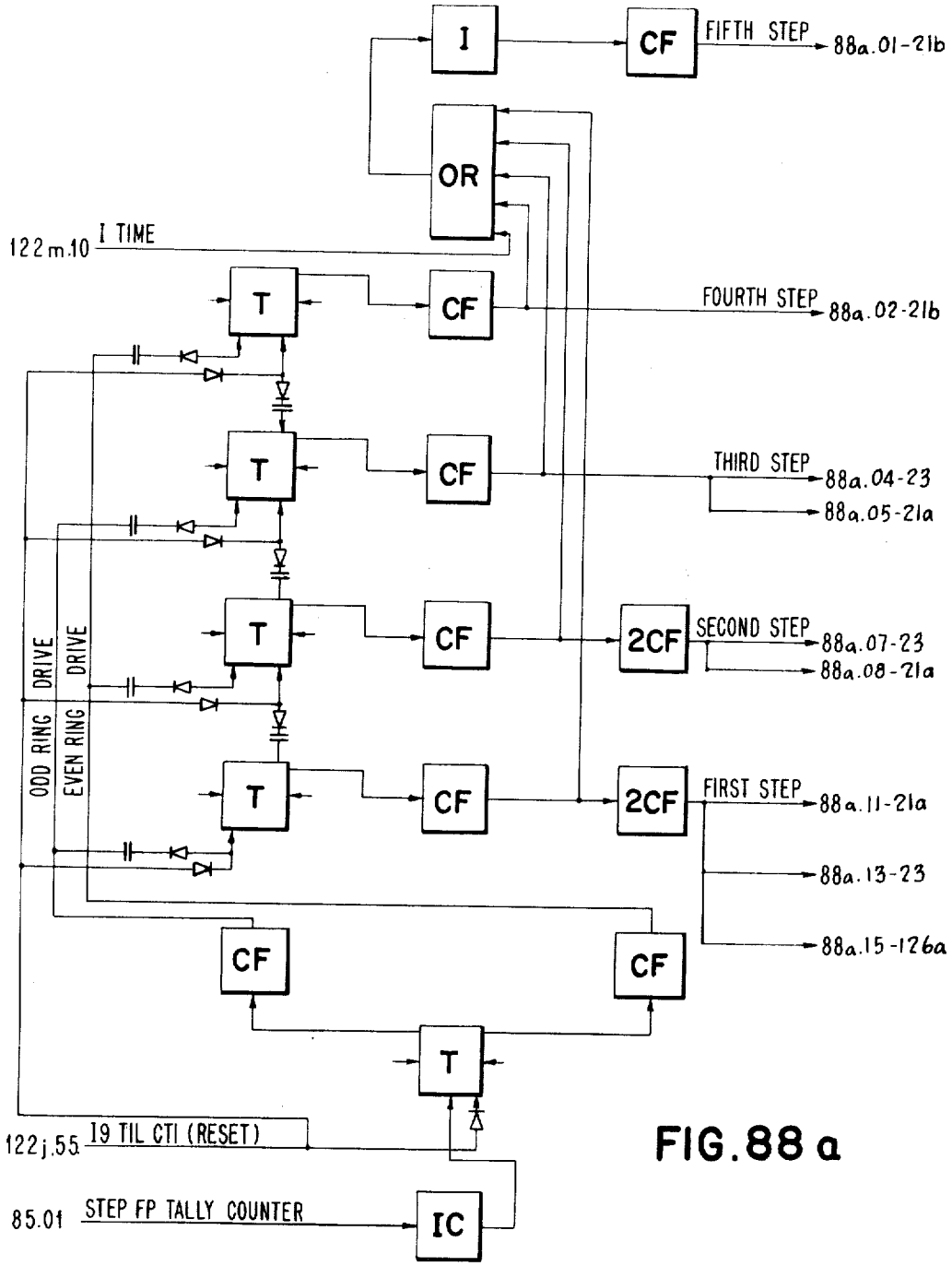


FIG.88a

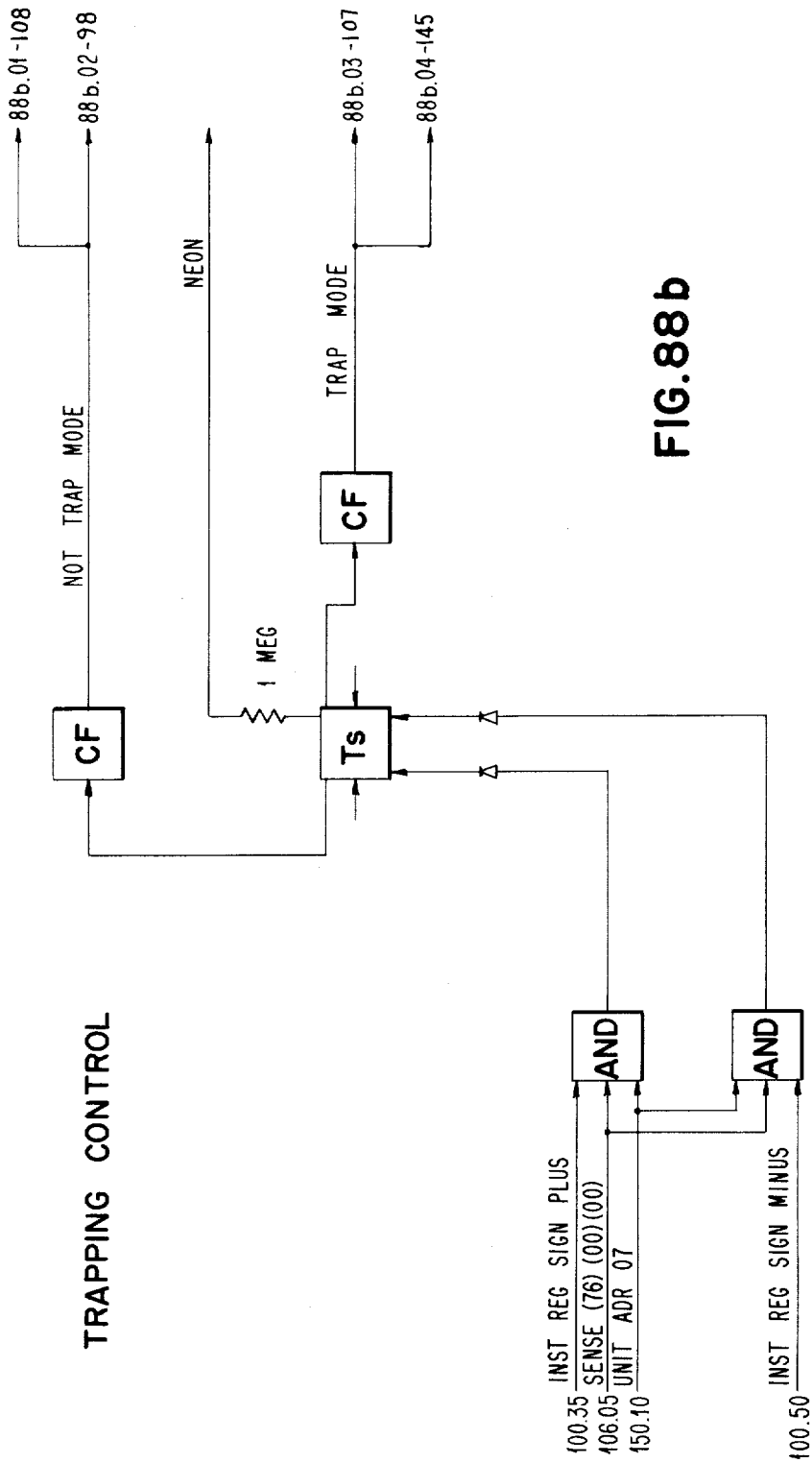

88b.01-108
88b.02-98
88b.03-107
88b.04-145
NEON
TRAP MODE
NOT TRAP MODE
CF
CF
1 MEG
Ts
AND
AND
INST REG SIGN PLUS
100.35
SENSE (76)(00)(00)
106.05
UNIT ADR 07
150.10
INST REG SIGN MINUS
100.50
TRAPPING CONTROL

FIG.88b

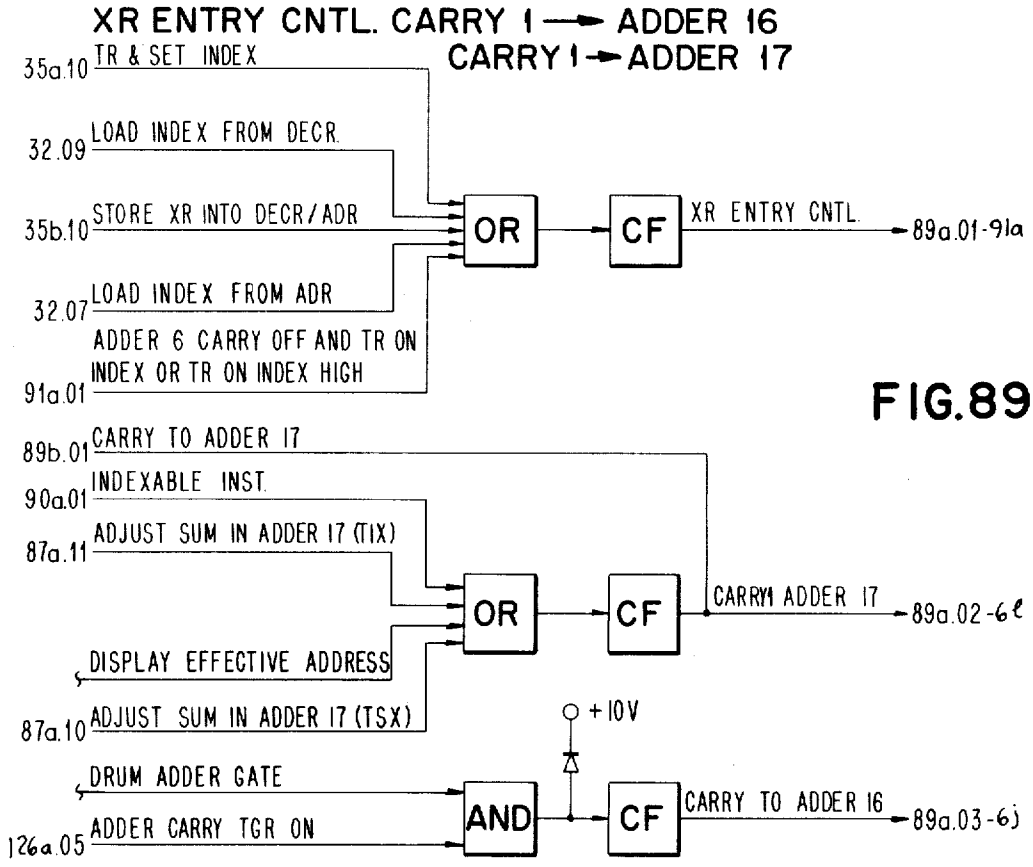


FIG.89a

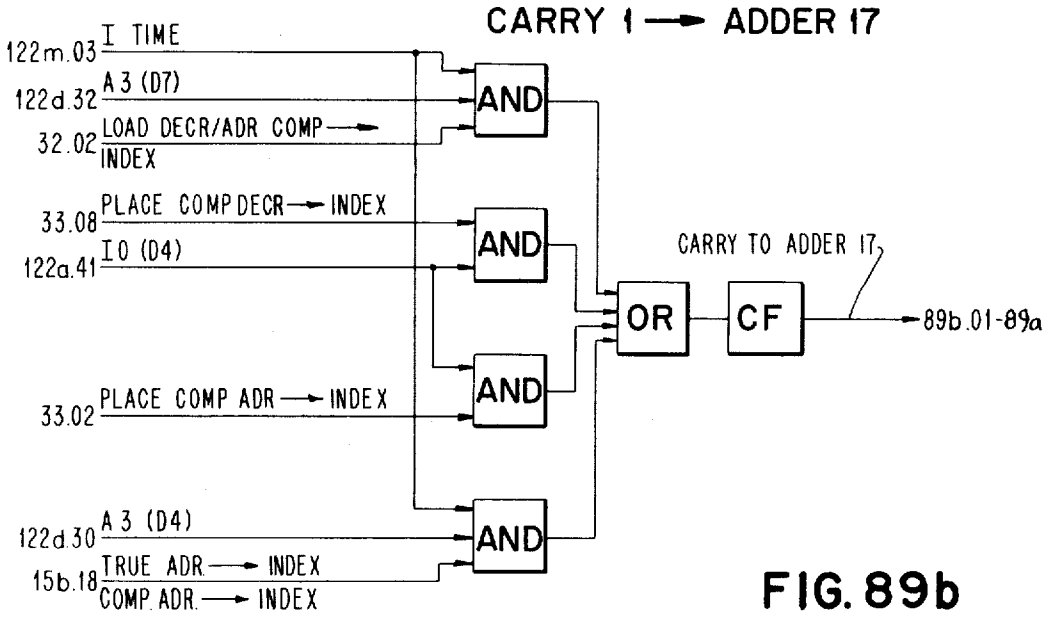
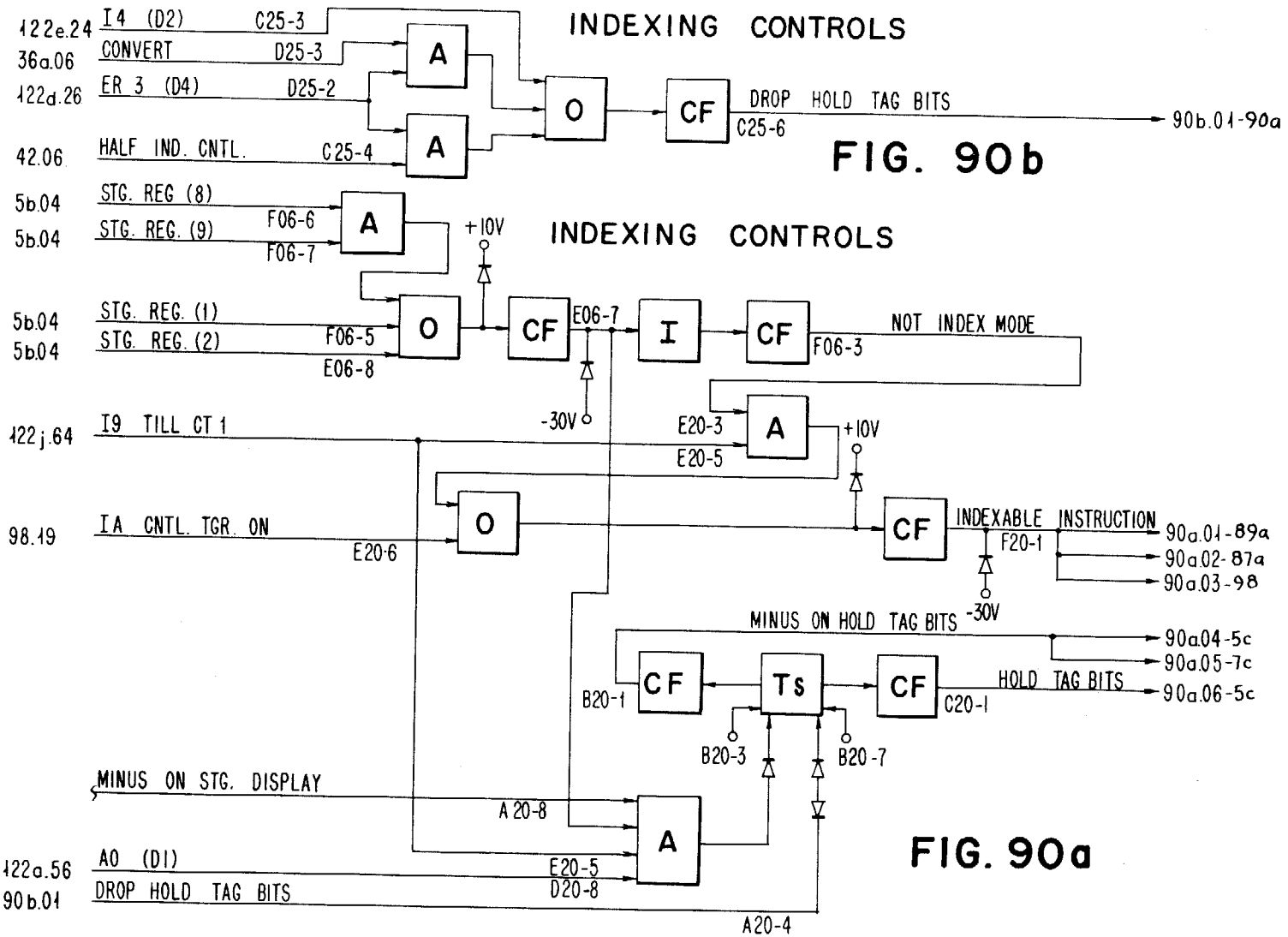


FIG. 89b


INDEXING CONTROLS
122e.24
I4 (D2)
C25-3
36a.06
CONVERT
D25-3
122d.26
ER 3 (D4)
D25-2
42.06
HALF IND. CNTL.
C25-4
A
A
O
CF
DROP HOLD TAG BITS
C25-6
90b.01-90a
FIG. 90b
INDEXING CONTROLS
5b.04
STG. REG (8)
5b.04
STG. REG. (9)
F06-6
F06-7
A
+10V
5b.04
STG. REG. (1)
5b.04
STG. REG. (2)
F06-5
E06-8
O
CF
E06-7
I
CF
NOT INDEX MODE
F06-3
-30V
122j.64
I9 TILL CT 1
E20-3
E20-5
A
+10V
98.19
IA CNTL. TGR. ON
E20-6
O
CF
INDEXABLE INSTRUCTION
F20-1
-30V
90a.01-89a
90a.02-87a
90a.03-98
MINUS ON HOLD TAG BITS
90a.04-5c
90a.05-7c
B20-1
CF
Ts
CF
HOLD TAG BITS
C20-1
90a.06-5c
B20-3
B20-7
MINUS ON STG. DISPLAY
A 20-8
A
122a.56
A0 (D1)
E20-5
90b.01
DROP HOLD TAG BITS
D20-8
A20-4
FIG. 90a

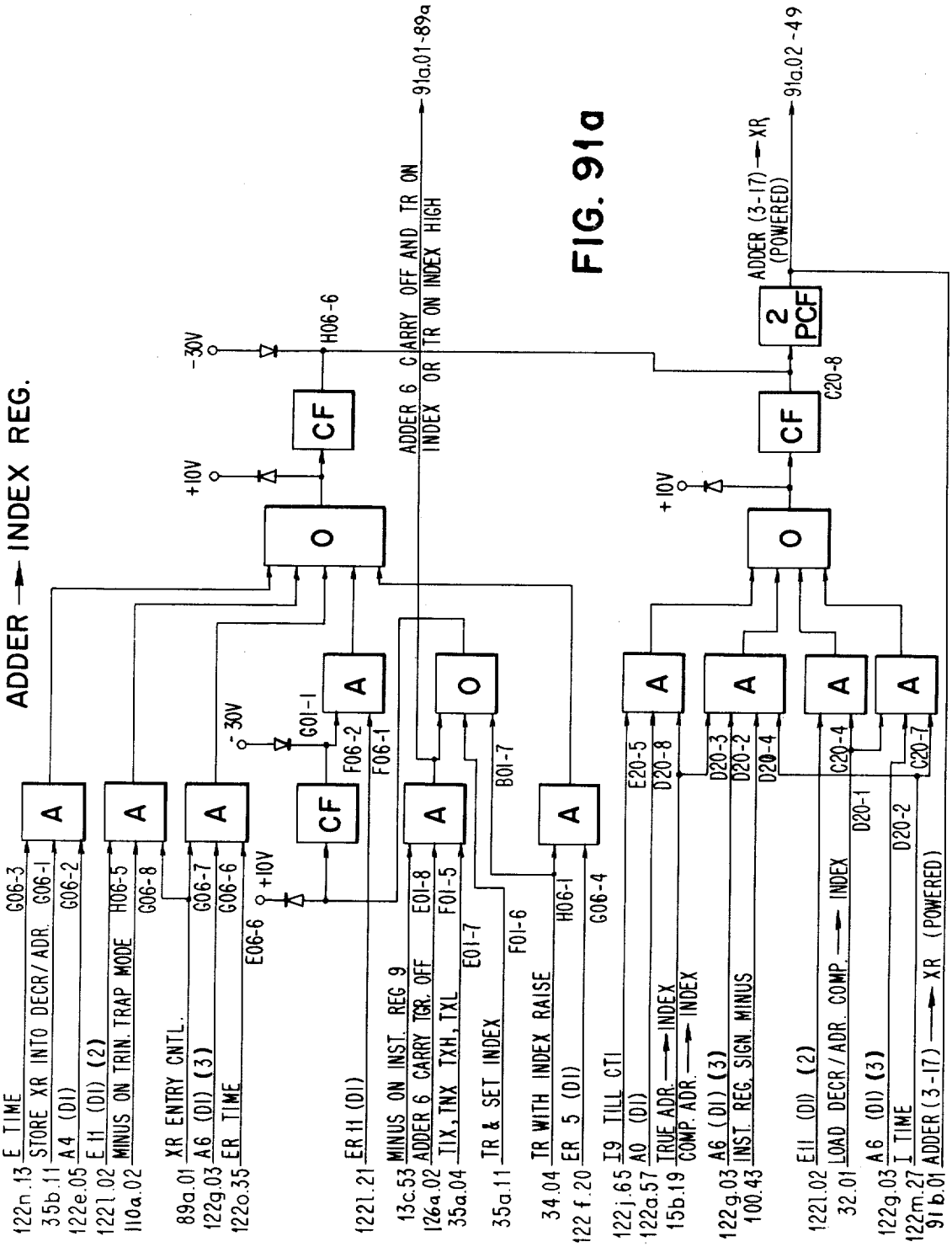

ADDER → INDEX REG.
E TIME
STORE XR INTO DECR/ADR.
A4 (01)
E11 (01) (2)
MINUS ON TRIN. TRAP MODE
XR ENTRY CNTL.
A6 (01) (3)
ER TIME
ER 11 (01)
MINUS ON INST. REG 9
ADDER 6 CARRY TGR. OFF
TIX, TNX TXH, TXL
TR & SET INDEX
TR WITH INDEX RAISE
ER 5 (01)
I9 TILL CTI
A0 (01)
TRUE ADR. → INDEX
COMP. ADR. → INDEX
A6 (01) (3)
INST. REG. SIGN. MINUS
E11 (01) (2)
LOAD DECR/ADR. COMP. → INDEX
A6 (01) (3)
I TIME
ADDER (3-17) → XR (POWERED)
-30V
+10V
CF
O
A
ADDER 6 CARRY OFF AND TR ON
INDEX OR TR ON INDEX HIGH
ADDER (3-17) → XR (POWERED)
2 PCF

FIG. 91a

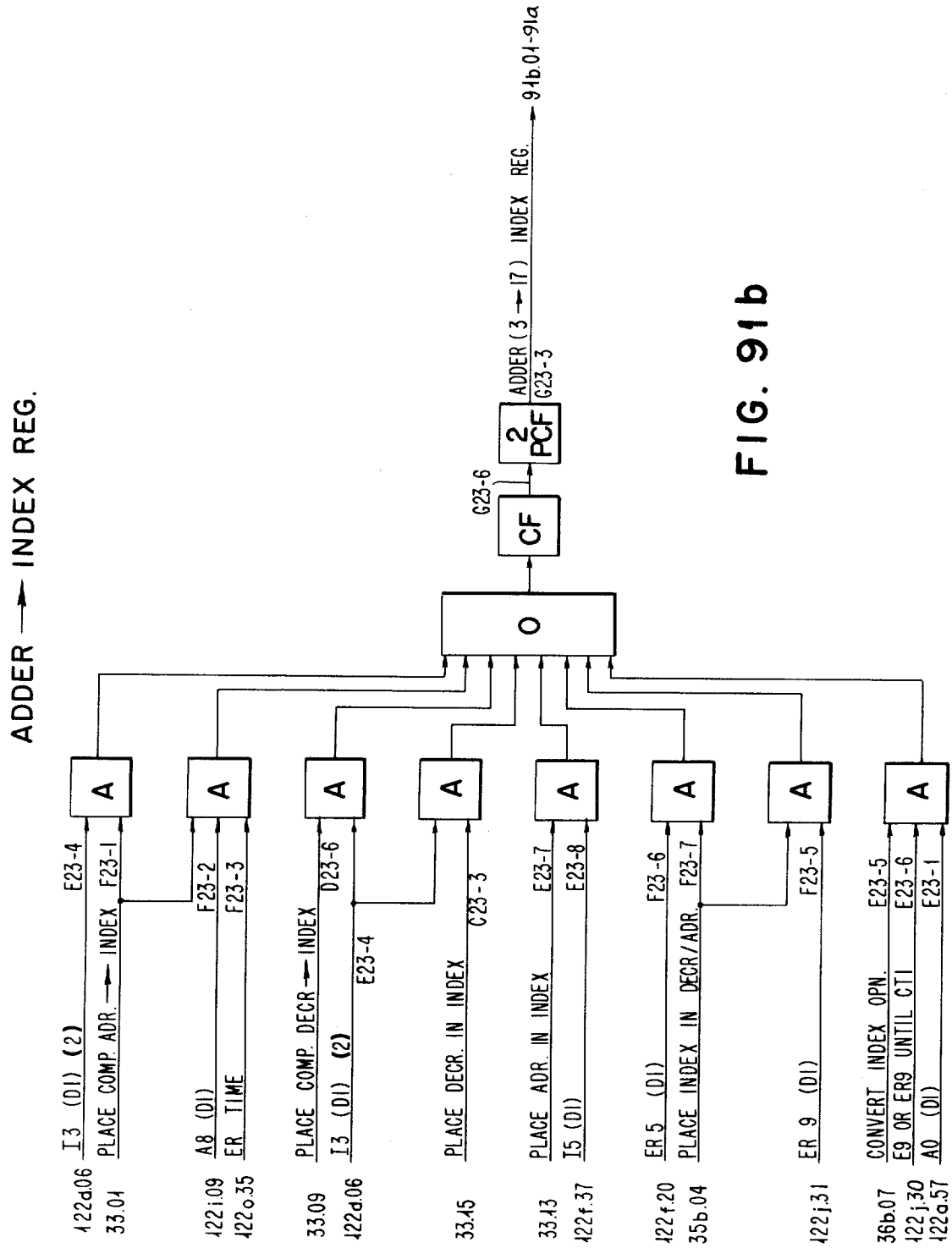

ADDER → INDEX REG.
I3 (D1) (2)
PLACE COMP. ADR. → INDEX
A8 (D1)
ER TIME
PLACE COMP. DECR → INDEX
I3 (D1) (2)
PLACE DECR. IN INDEX
PLACE ADR. IN INDEX
I5 (D1)
ER 5 (D1)
PLACE INDEX IN DECR/ADR.
ER 9 (D1)
CONVERT INDEX OPN.
E9 OR ER9 UNTIL CTI
A0 (D1)
E23-4
F23-1
F23-2
F23-3
D23-6
E23-4
C23-3
E23-7
E23-8
F23-6
F23-7
F23-5
E23-5
E23-6
E23-1
A
O
CF
G23-6
2 PCF
ADDER (3 → 17) INDEX REG.
G23-3
91b.01-91a
122d.06
33.01
122i.09
122o.35
33.09
122d.06
33.15
33.13
122f.37
122f.20
35b.04
122j.31
36b.07
122j.30
122a.57

FIG. 91b

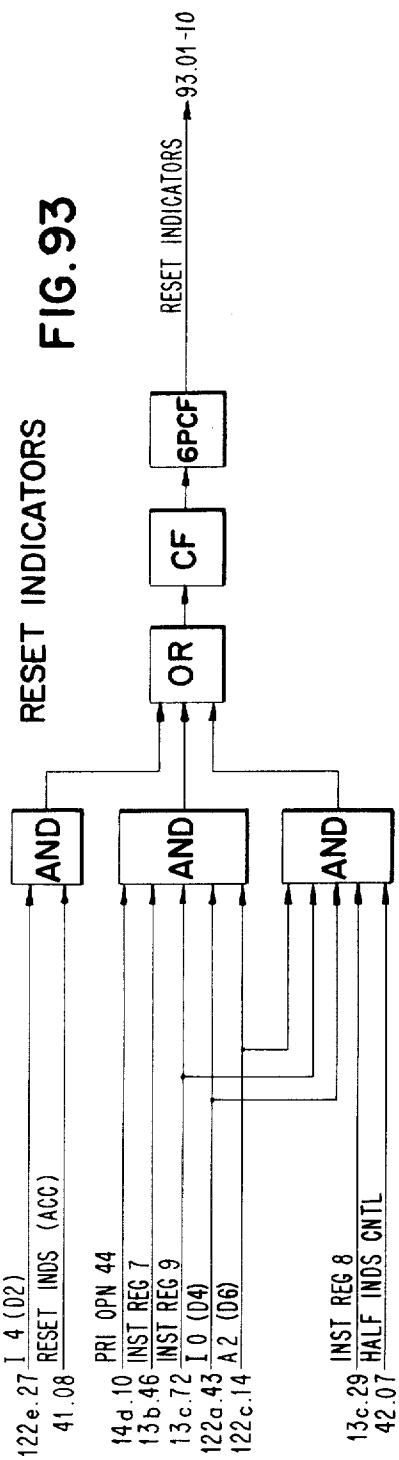

RESET INDICATORS
AND
OR
CF
6PCF
RESET INDICATORS
93.01-10
122e.27 I 4 (02)
41.08 RESET INDS (ACC)
PRI OPN 44
14d.10 INST REG 7
13b.46 INST REG 9
13c.72 I 0 (04)
122a.43 A 2 (06)
122c.14
13c.29 INST REG 8
42.07 HALF INDS CNTL

FIG. 93

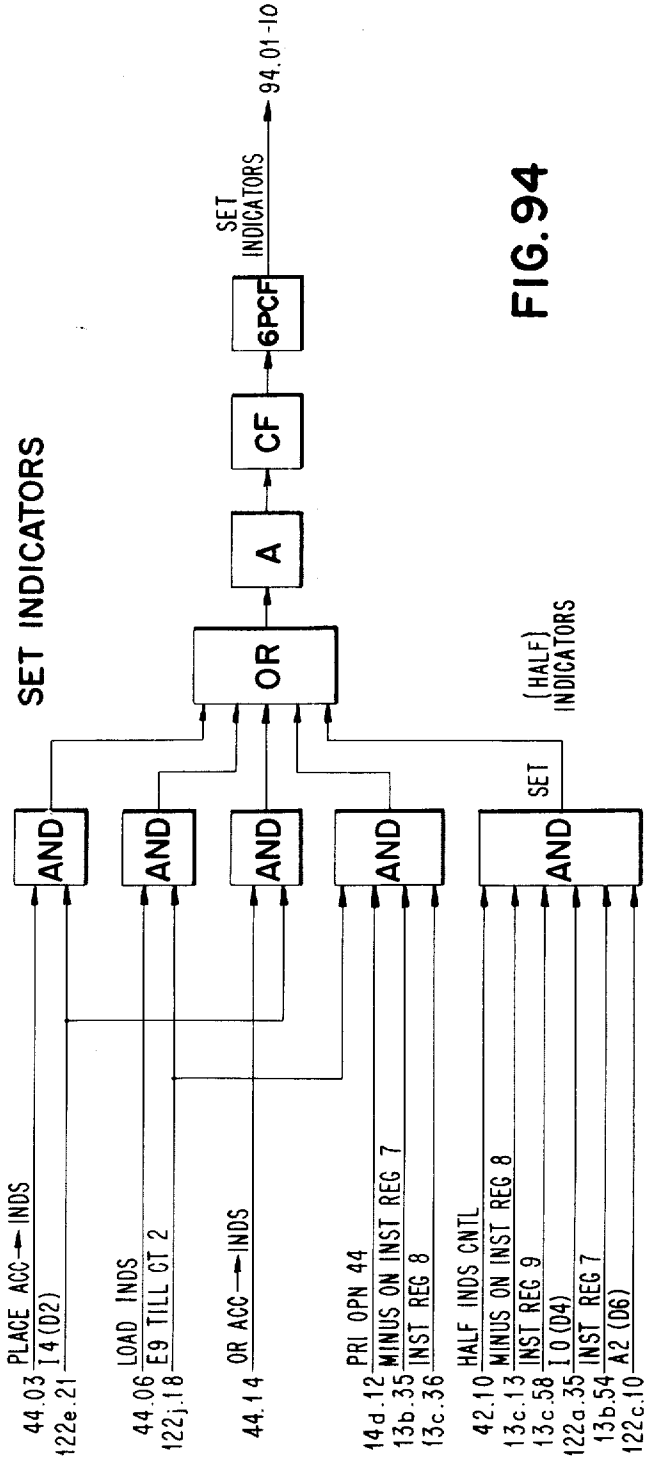

SET INDICATORS
AND
OR
A
CF
6PCF
SET INDICATORS
94.01-10
(HALF) INDICATORS
SET
44.03 PLACE ACC→INDS
122e.21 I 4 (02)
44.06 LOAD INDS
122j.18 E 9 TILL CT 2
44.14 OR ACC→INDS
14d.12 PRI OPN 44
13b.35 MINUS ON INST REG 7
13c.36 INST REG 8
42.10 HALF INDS CNTL
13c.13 MINUS ON INST REG 8
13c.58 INST REG 9
122a.35 I 0 (04)
13b.54 INST REG 7
122c.10 A 2 (06)

FIG. 94

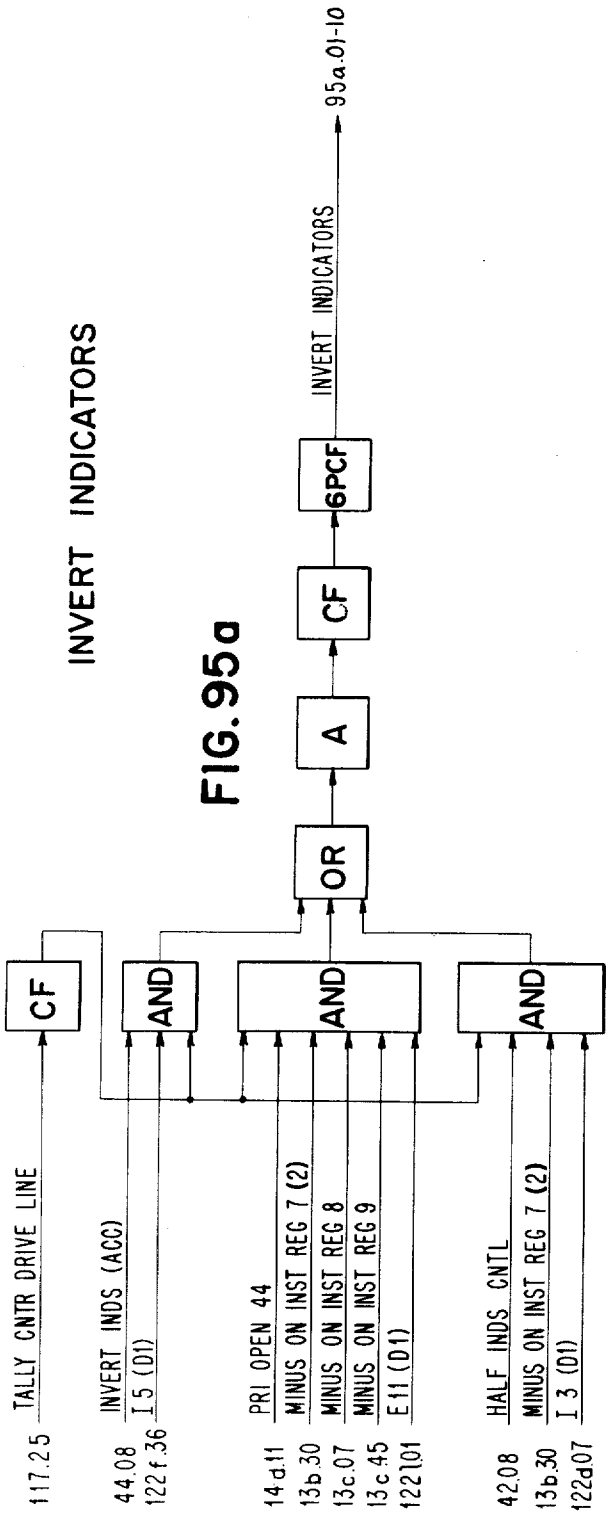


FIG. 95a

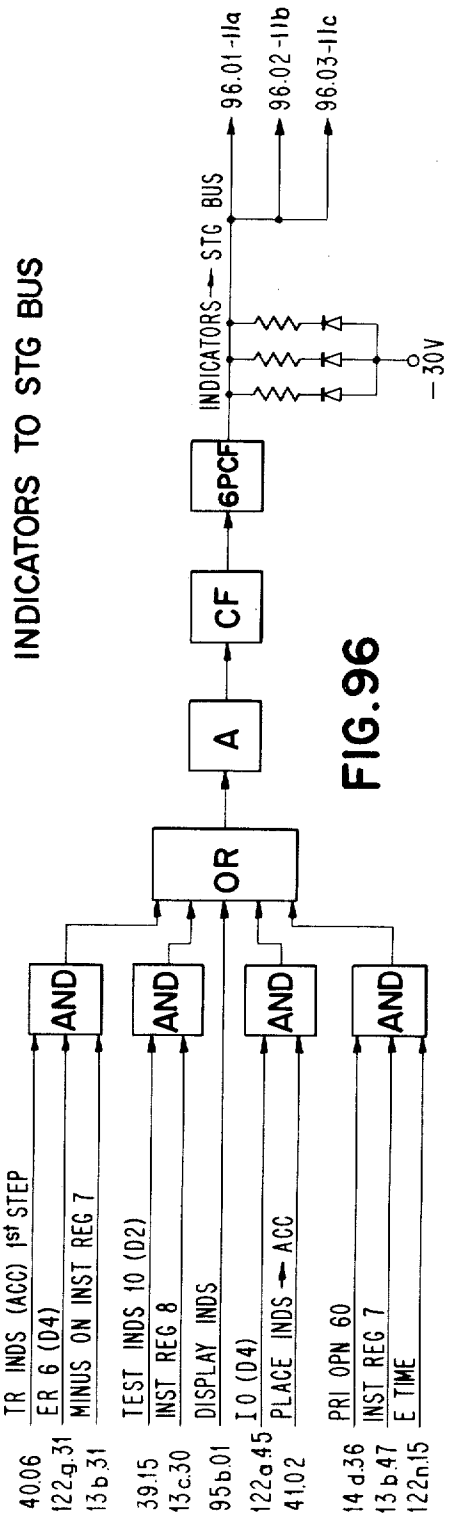


FIG. 96

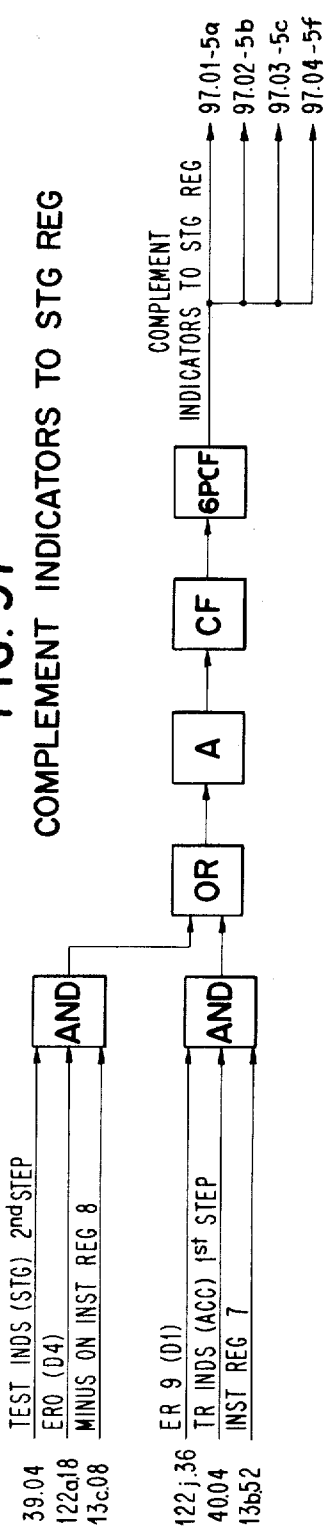


FIG. 97
COMPLEMENT INDICATORS TO STG REG

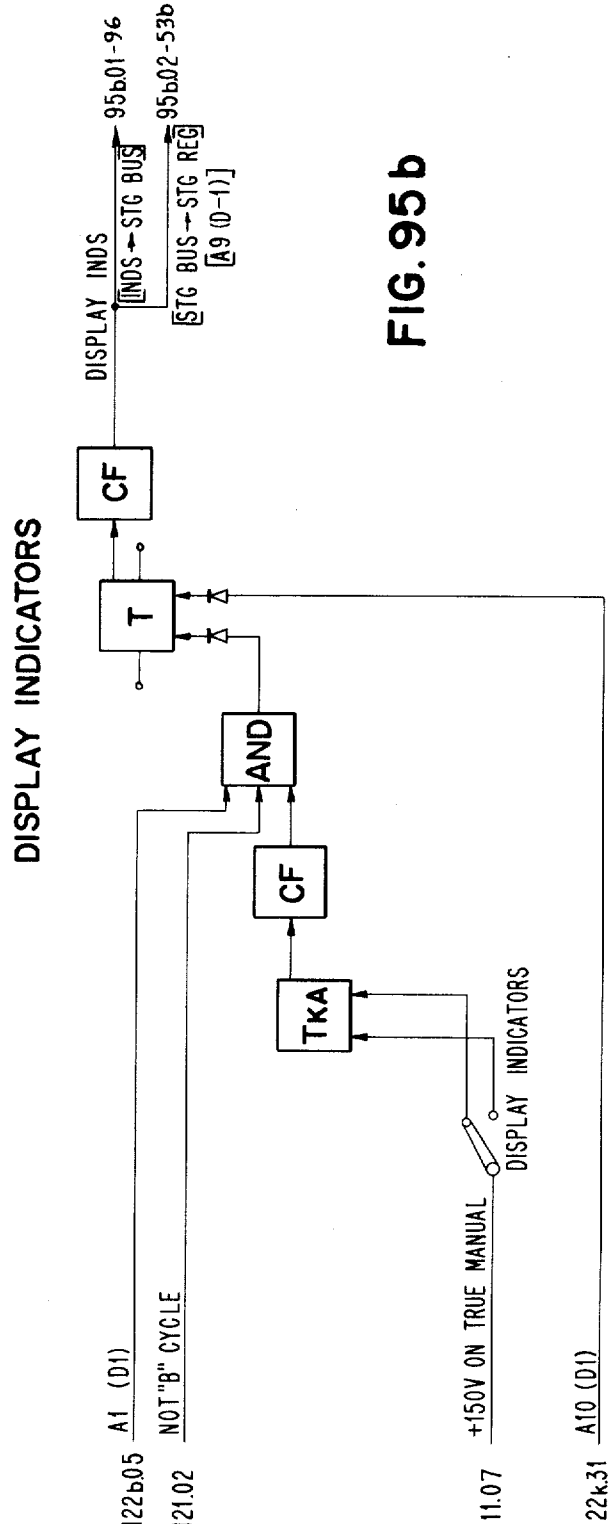
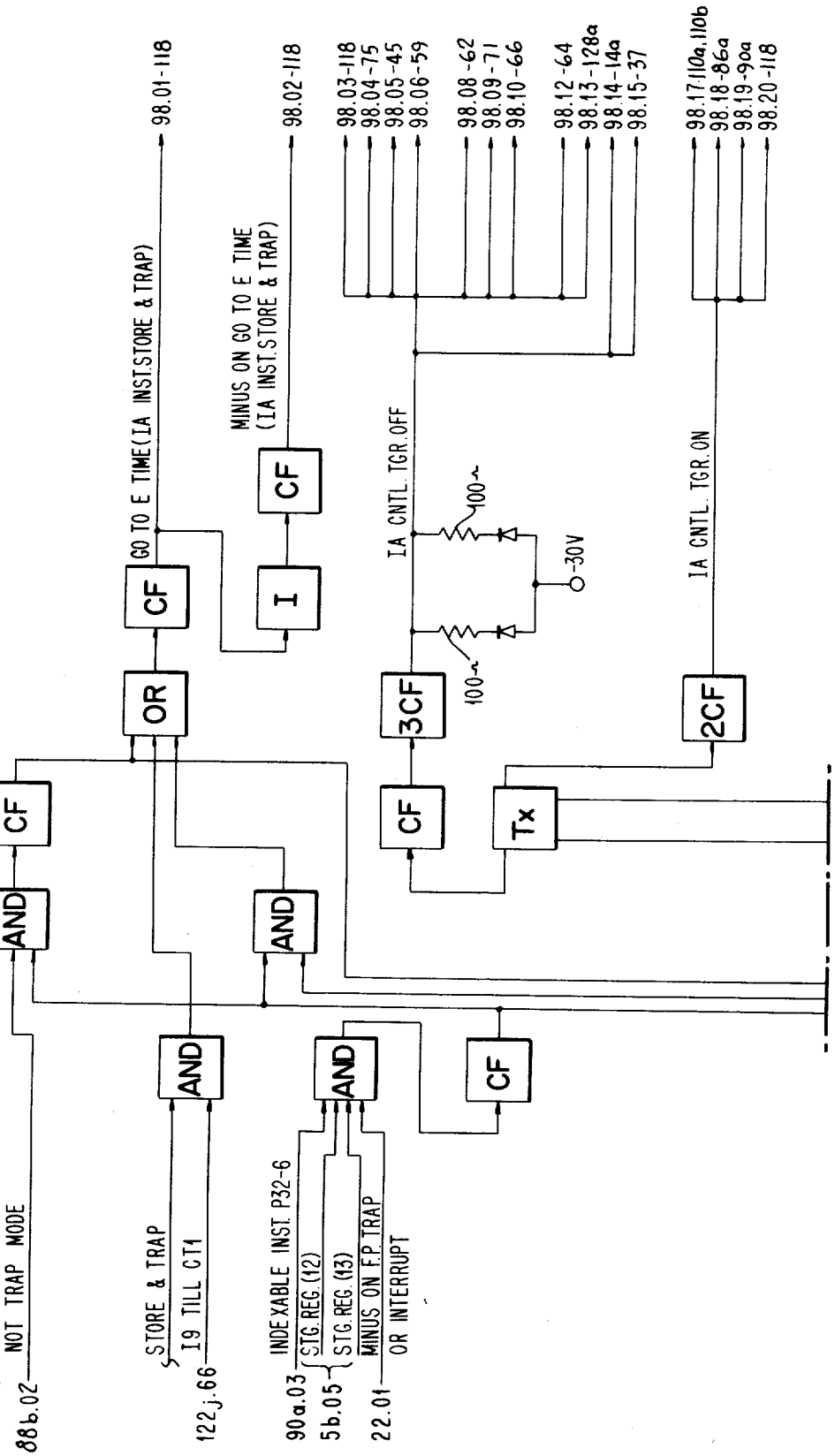


FIG. 95b

FIG. 98
(SHEET 1 OF 2)

INDIRECT ADDRESSING CONTROLS



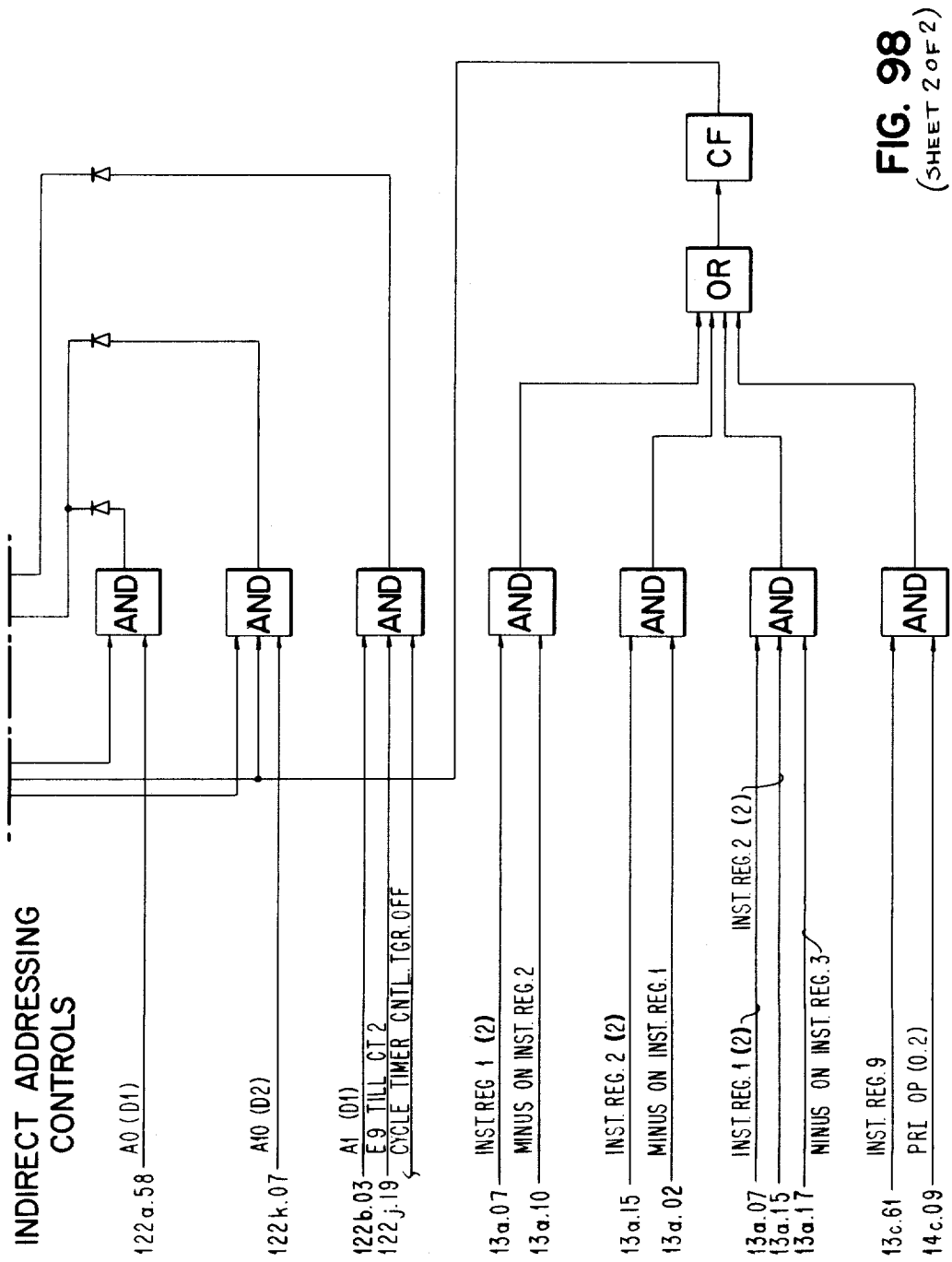


FIG. 98
(SHEET 2 OF 2)

INSTRUCTION REGISTER PULSE GENERATOR

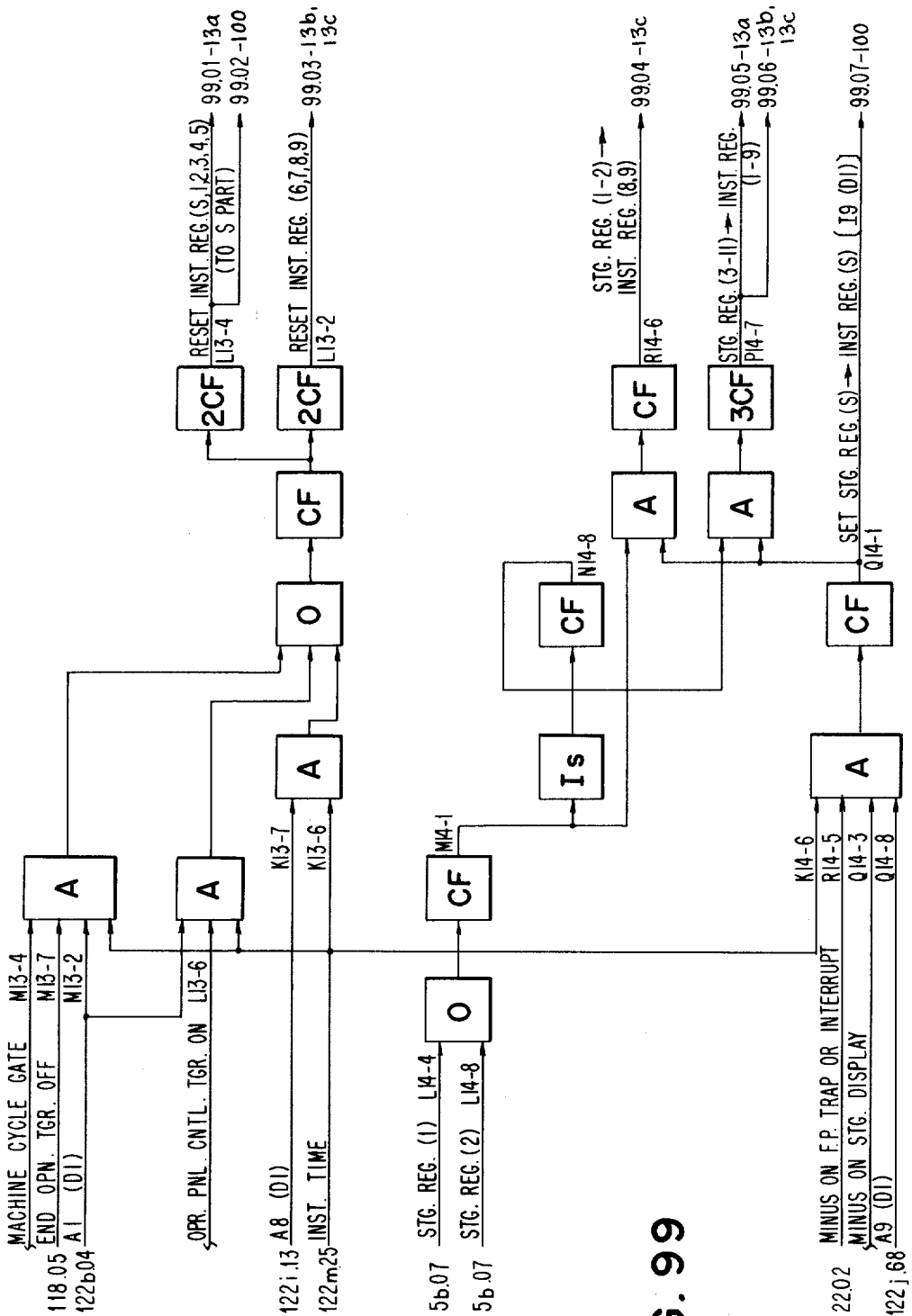


FIG. 99

INSTRUCTION REGISTER SIGN PLUS & MINUS

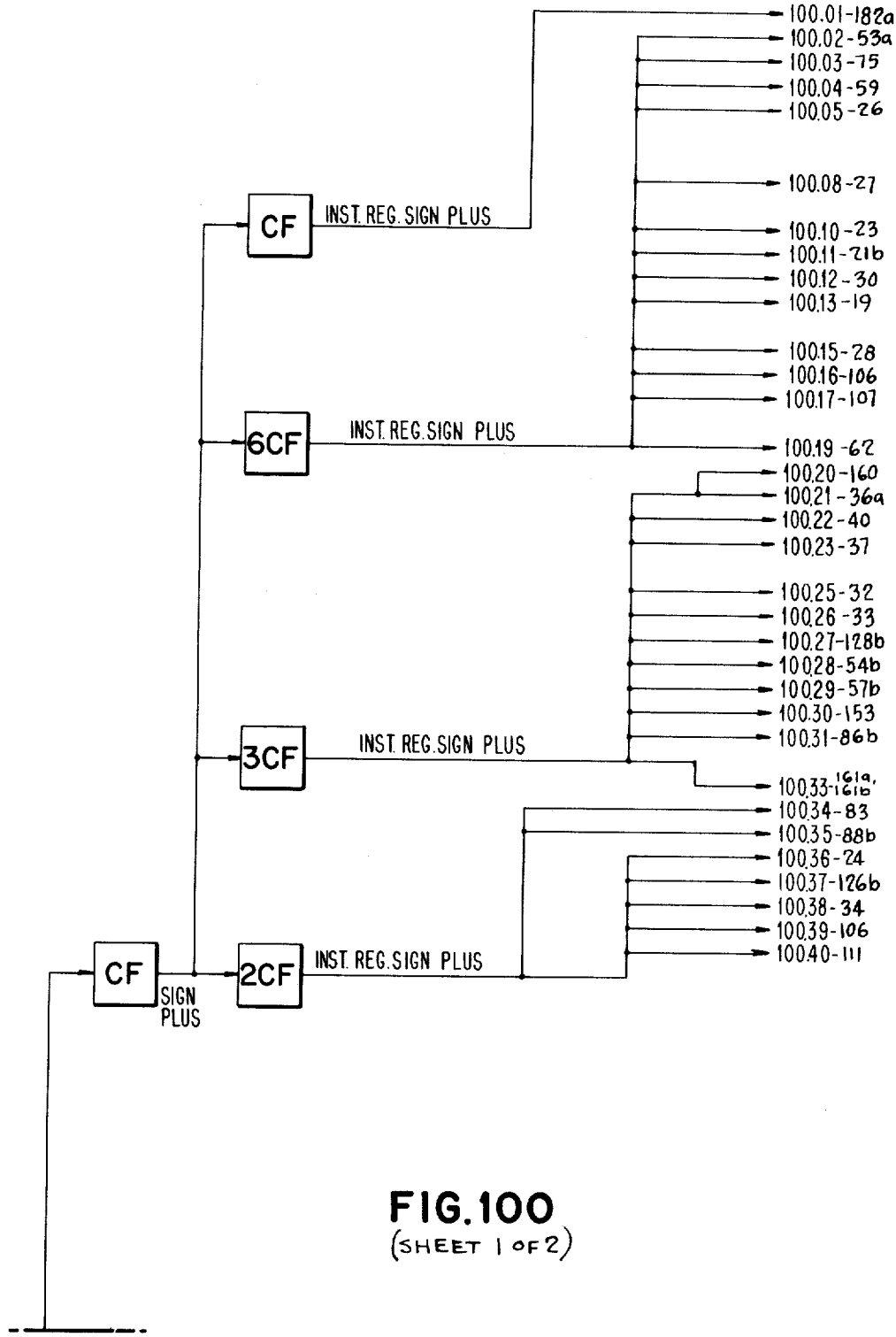


FIG. 100
(SHEET 1 OF 2)

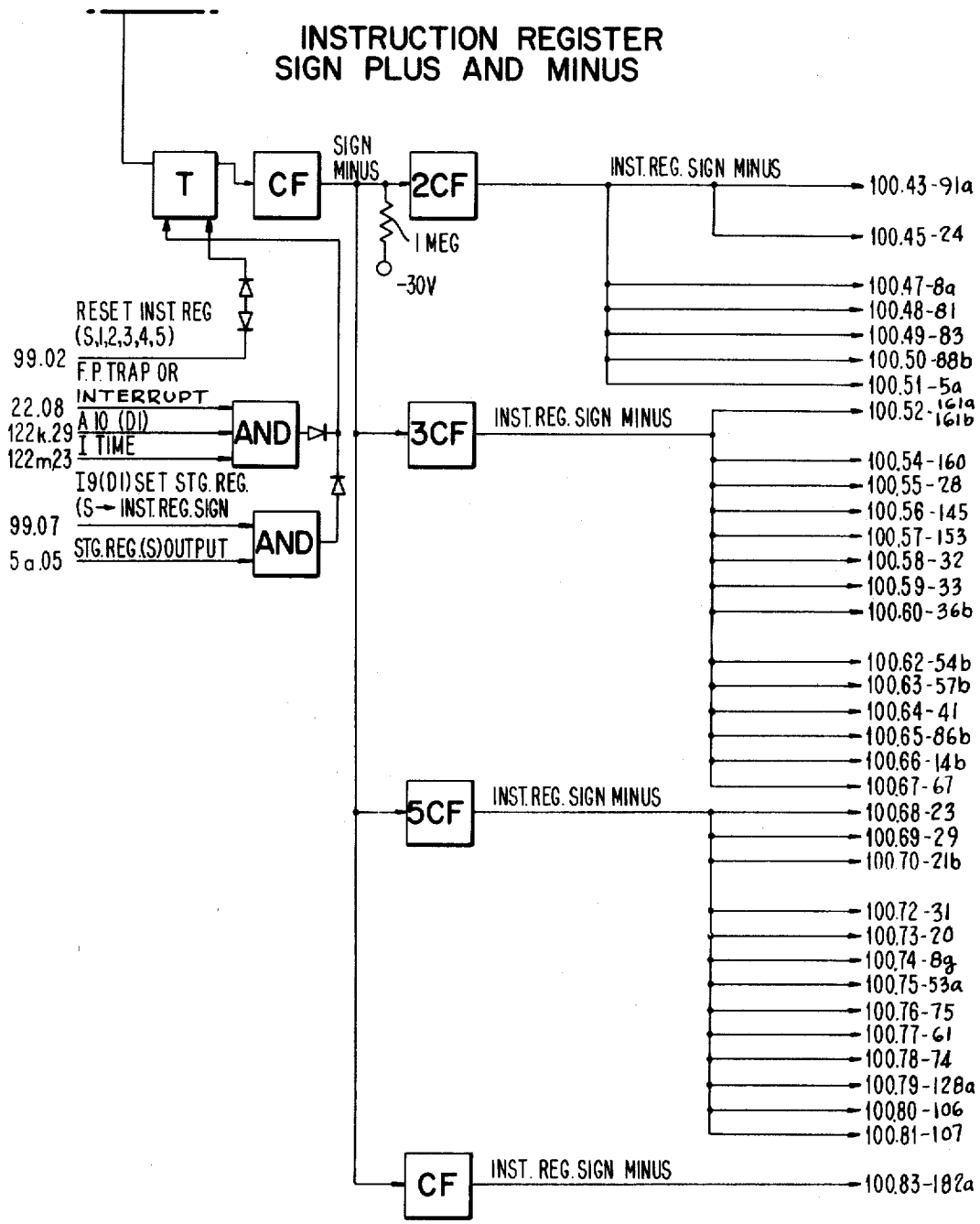
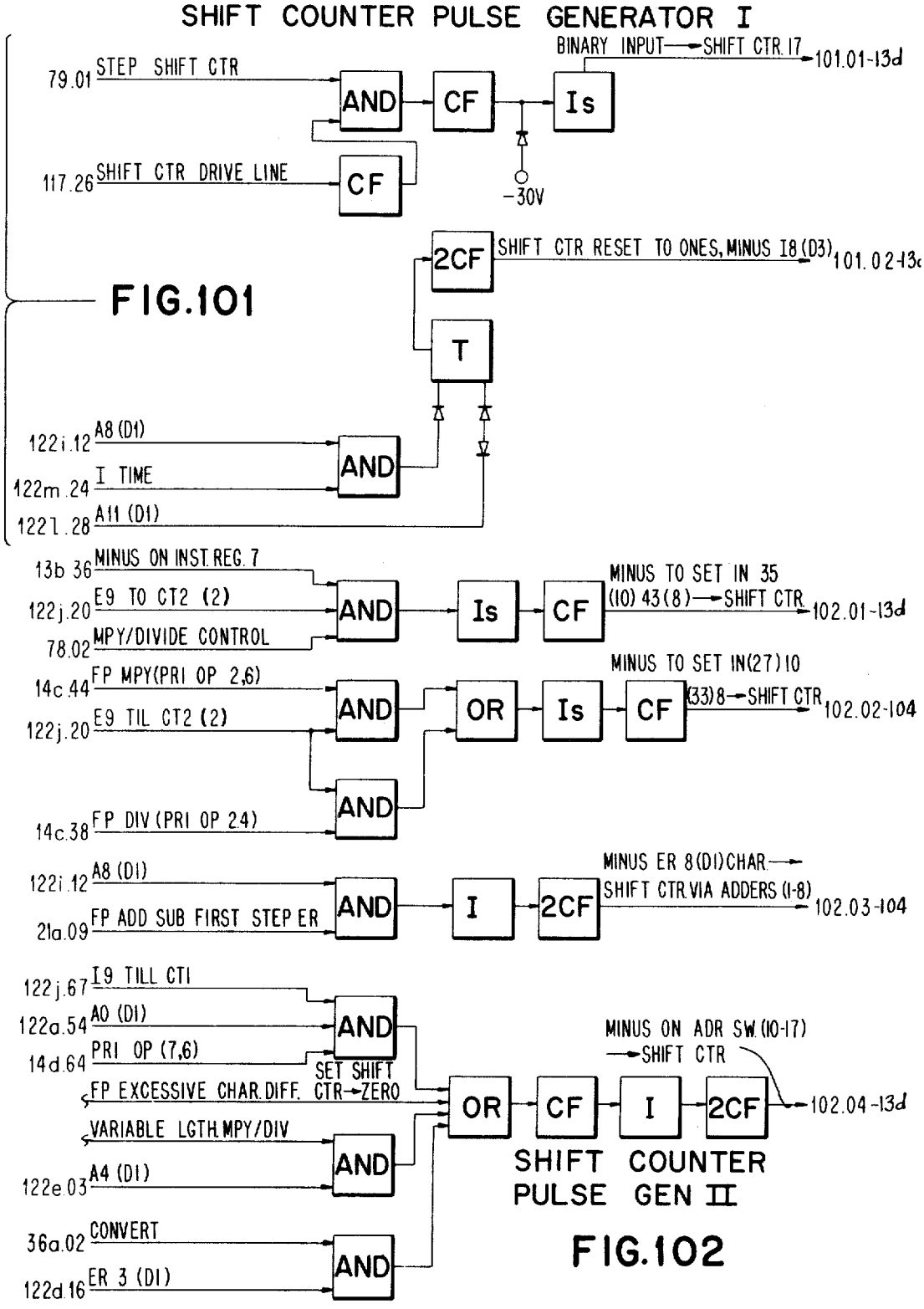


FIG. 100
(SHEET 2 OF 2)


SHIFT COUNTER PULSE GENERATOR I
79.01 STEP SHIFT CTR
AND
CF
Is
BINARY INPUT → SHIFT CTR 17
101.01-13d
117.26 SHIFT CTR DRIVE LINE
CF
-30V
2CF
SHIFT CTR RESET TO ONES, MINUS 18 (D3)
101.02-13c
T
122i.12 A8 (D1)
122m.24 I TIME
122l.28 A11 (D1)
AND
FIG.101
13b 36 MINUS ON INST. REG. 7
122j.20 E9 TO CT2 (2)
78.02 MPY/DIVIDE CONTROL
AND
Is
CF
MINUS TO SET IN 35
(10) 43 (8) → SHIFT CTR
102.01-13d
14c.44 FP MPY (PRI OP 2,6)
122j.20 E9 TIL CT2 (2)
AND
OR
Is
CF
MINUS TO SET IN (27) 10
(33) 8 → SHIFT CTR
102.02-104
14c.38 FP DIV (PRI OP 24)
AND
122i.12 A8 (D1)
21a.09 FP ADD SUB FIRST STEP ER
AND
I
2CF
MINUS ER 8 (D1) CHAR →
SHIFT CTR VIA ADDERS (1-8)
102.03-104
122j.67 I9 TILL CT1
122a.54 A0 (D1)
14d.64 PRI OP (7,6)
AND
SET SHIFT
FP EXCESSIVE CHAR. DIFF. CTR → ZERO
VARIABLE LGTH MPY/DIV
AND
122e.03 A4 (D1)
36a.02 CONVERT
122d.16 ER 3 (D1)
AND
OR
CF
I
2CF
MINUS ON ADR SW (10-17)
→ SHIFT CTR
102.04-13d
SHIFT COUNTER
PULSE GEN II
FIG.102

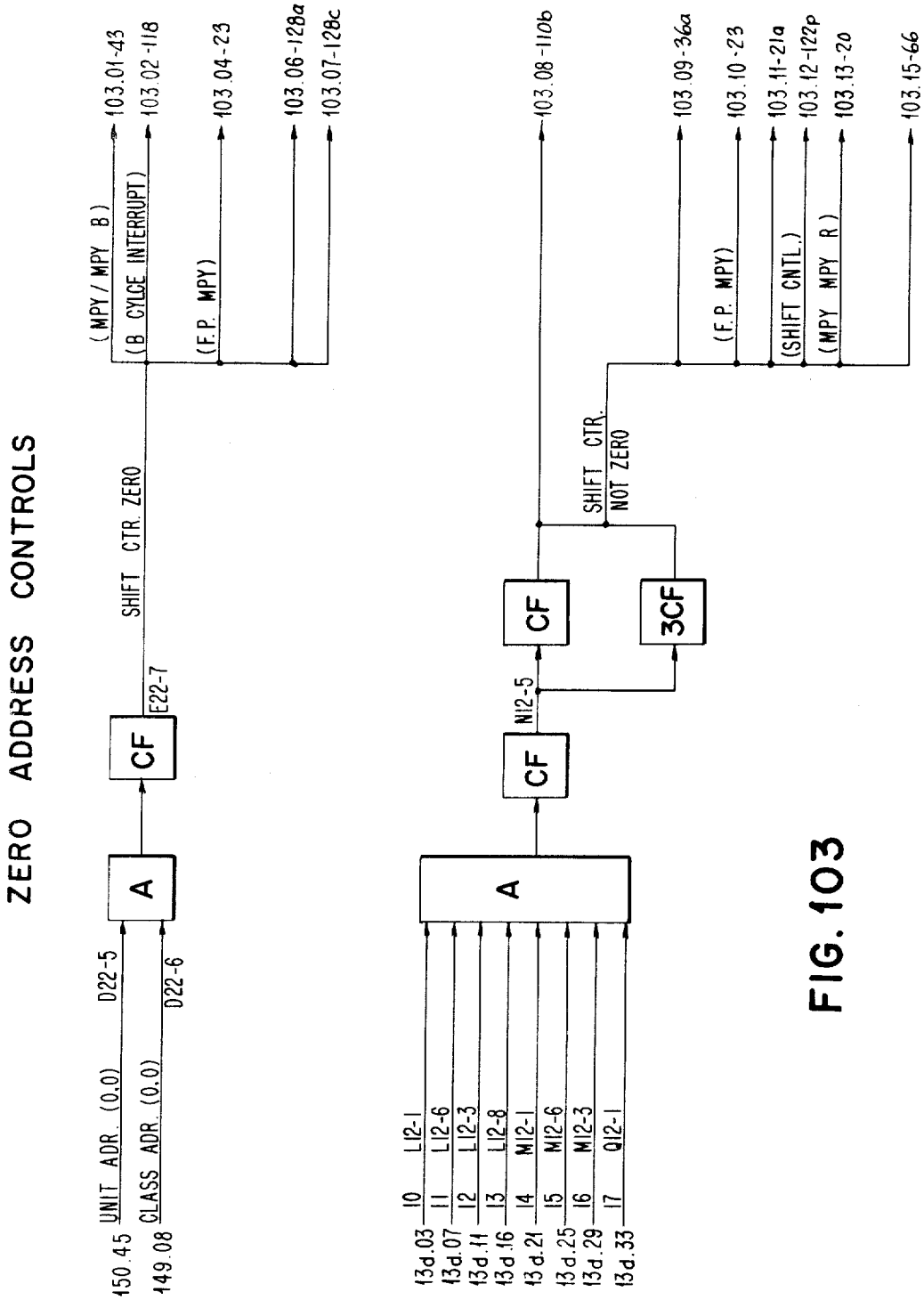

ZERO ADDRESS CONTROLS
150.45 UNIT ADR. (0,0)
149.08 CLASS ADR. (0,0)
D22-5
D22-6
A
CF
E22-7
SHIFT CTR. ZERO
(MPY / MPY B)
(B CYLCE INTERRUPT)
(F.P. MPY)
103.01-43
103.02-118
103.04-23
103.06-128a
103.07-128c
13d.03 10 L12-1
13d.07 11 L12-6
13d.11 12 L12-3
13d.16 13 L12-8
13d.21 14 M12-1
13d.25 15 M12-6
13d.29 16 M12-3
13d.33 17 Q12-1
A
CF
N12-5
CF
3CF
SHIFT CTR. NOT ZERO
103.08-110b
103.09-36a
(F.P. MPY)
103.10-23
(SHIFT CNTL.)
103.11-21a
(MPY MPY R)
103.12-122p
103.13-20
103.15-66

FIG. 103

F.P. ENTRY TO SHIFT CTR. (10-17)

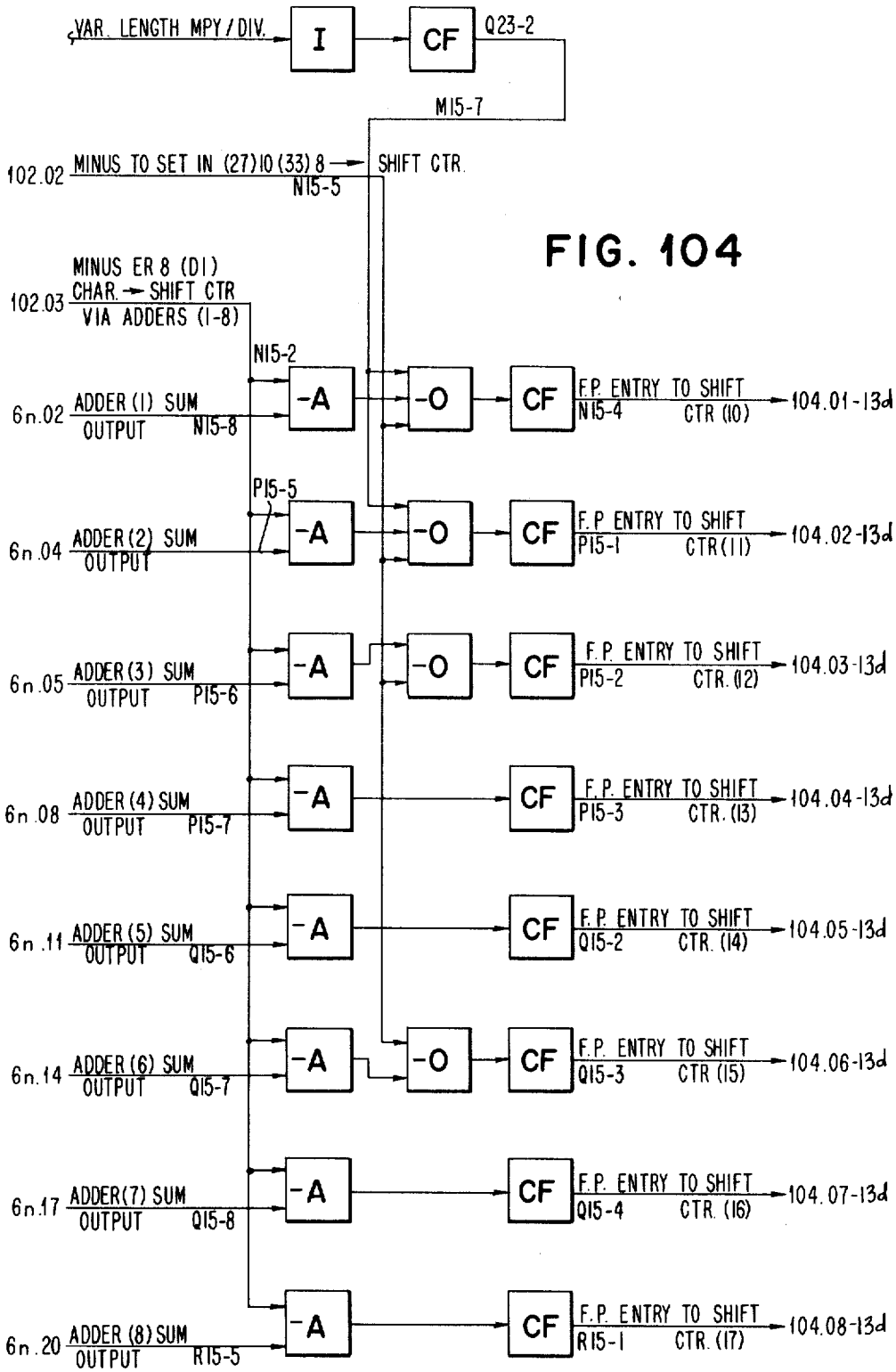


FIG. 104

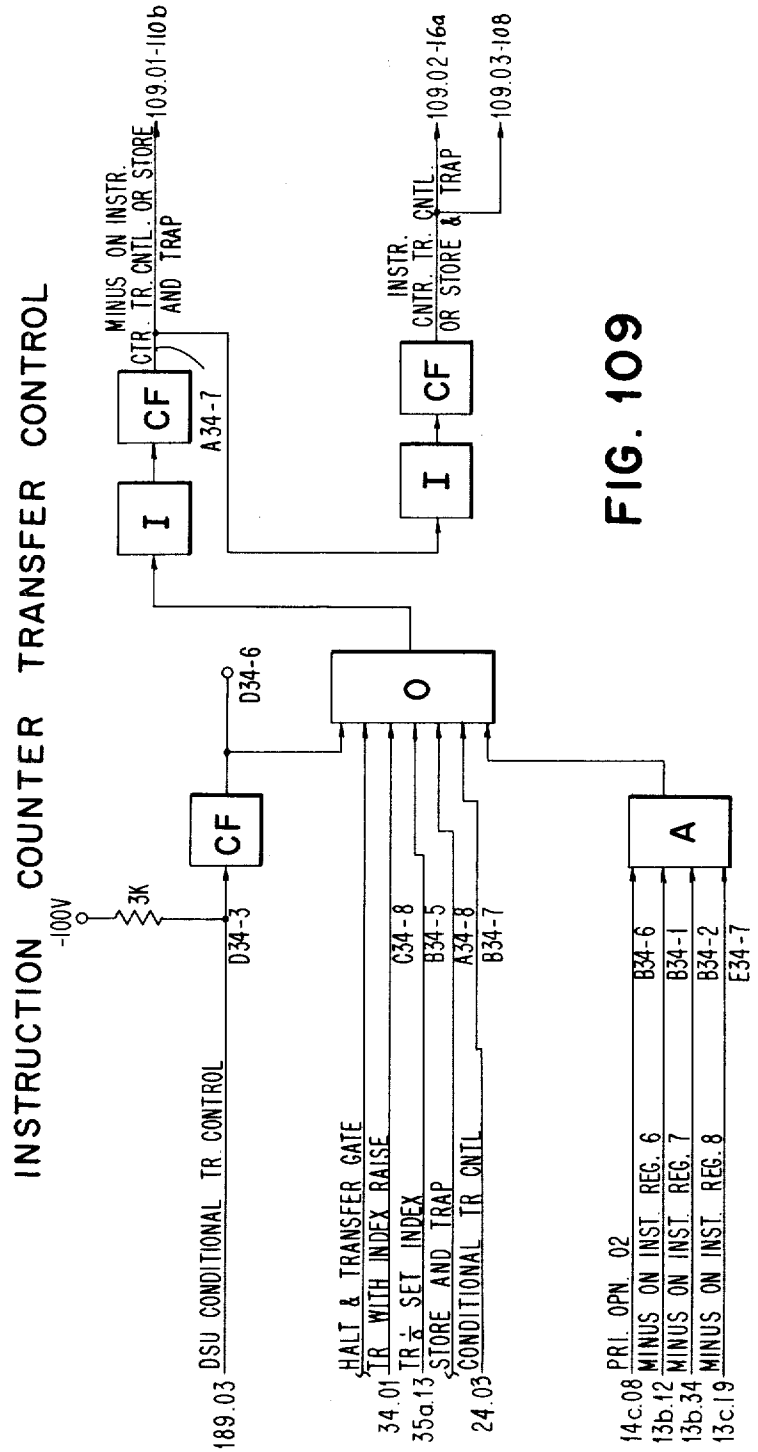


FIG. 109

FIG. 105

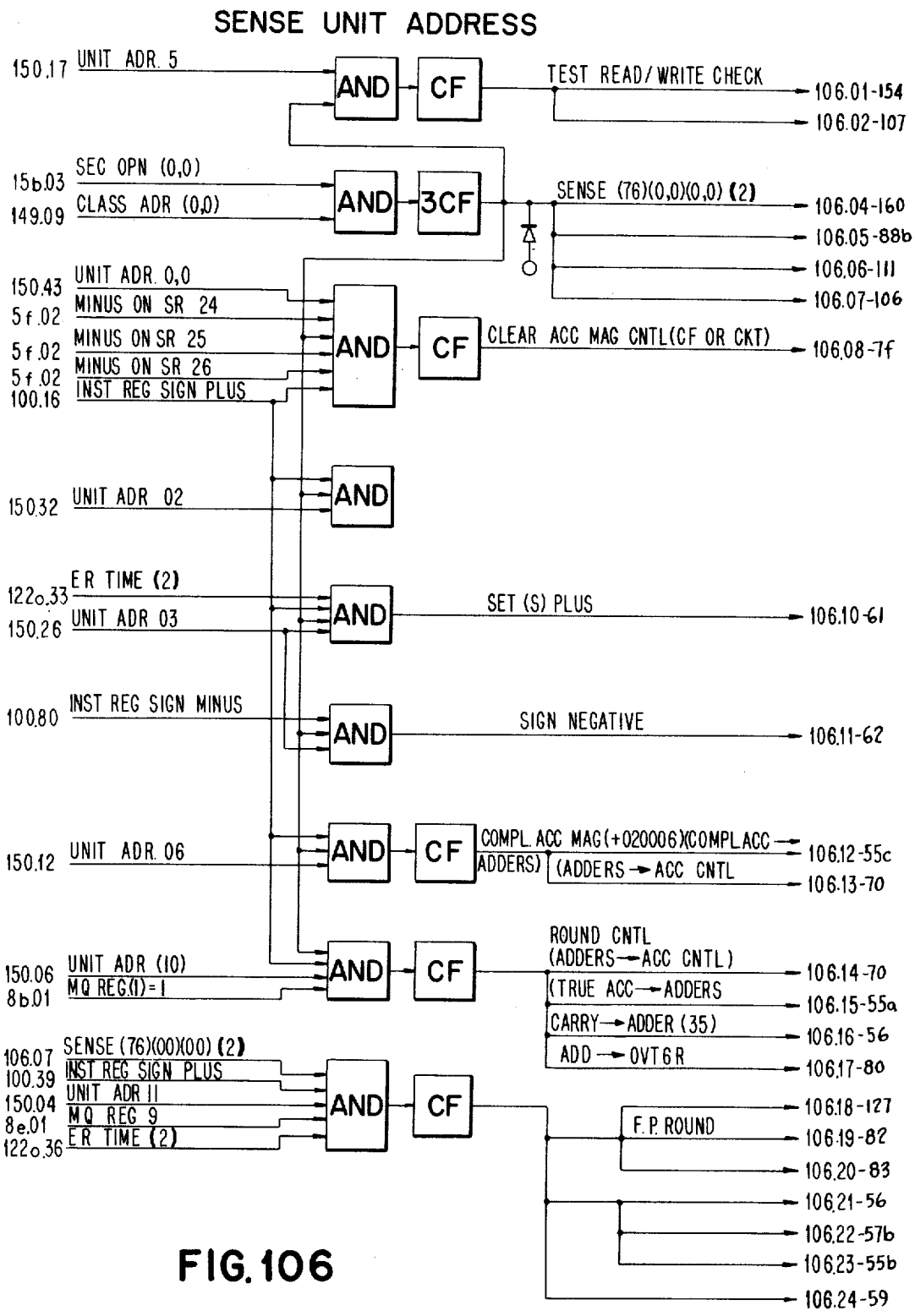
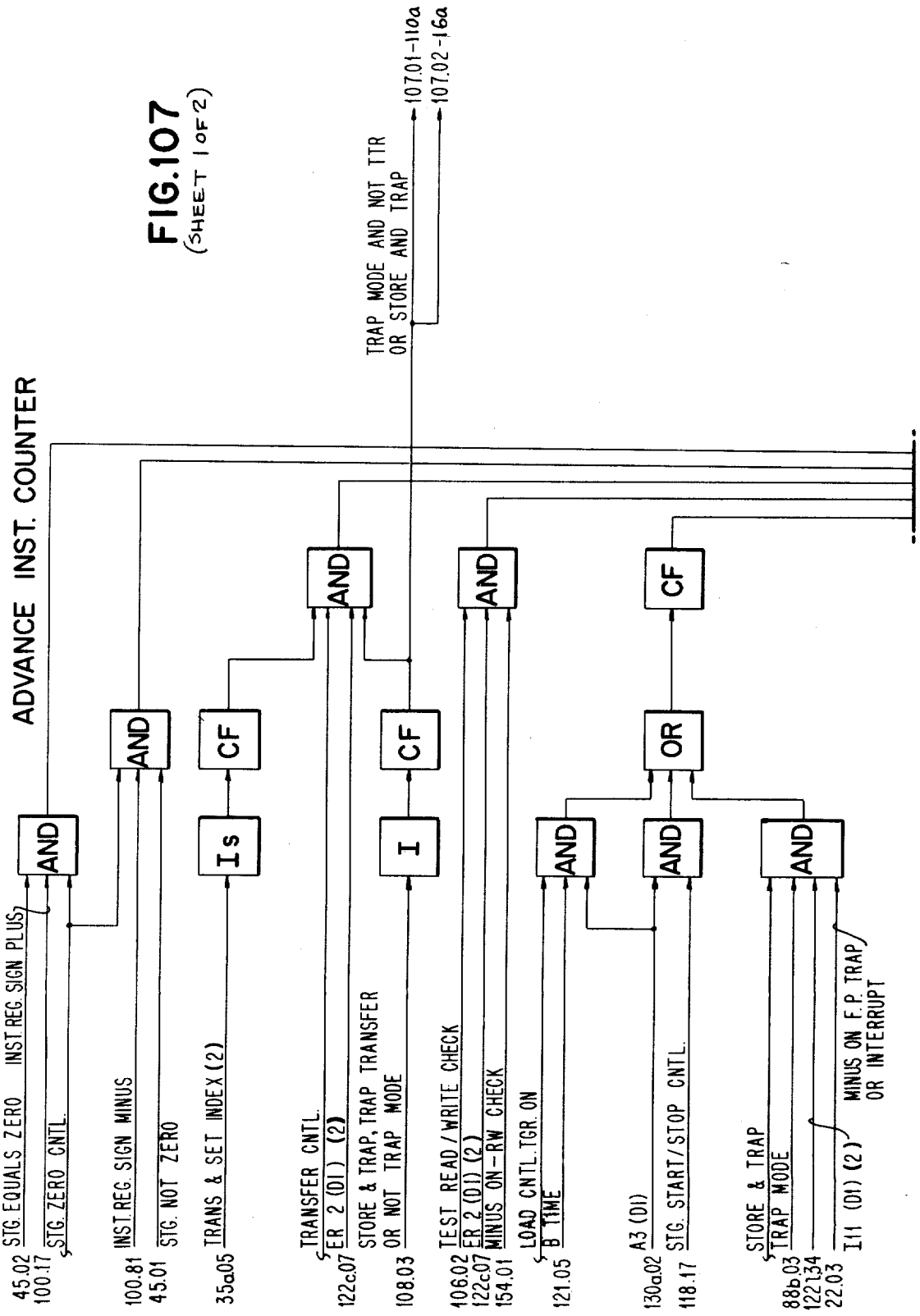

SENSE UNIT ADDRESS
150.17 UNIT ADR. 5
AND
CF
TEST READ/WRITE CHECK
106.01-154
106.02-107
15b.03 SEC OPN (0,0)
149.09 CLASS ADR (0,0)
AND
3CF
SENSE (76)(0,0)(0,0) (2)
106.04-160
106.05-88b
106.06-111
106.07-106
150.43 UNIT ADR. 0,0
5f.02 MINUS ON SR 24
5f.02 MINUS ON SR 25
5f.02 MINUS ON SR 26
100.16 INST REG SIGN PLUS
AND
CF
CLEAR ACC MAG CNTL(CF OR CKT)
106.08-71
150.32 UNIT ADR 02
AND
122o.33 E R TIME (2)
150.26 UNIT ADR 03
AND
SET (S) PLUS
106.10-61
100.80 INST REG SIGN MINUS
AND
SIGN NEGATIVE
106.11-62
150.12 UNIT ADR. 06
AND
CF
COMPL. ACC MAG (+020006) (COMPL ACC ADDERS)
(ADDERS → ACC CNTL
106.12-55c
106.13-70
150.06 UNIT ADR (10)
8b.01 MQ REG.(1) = 1
AND
CF
ROUND CNTL (ADDERS → ACC CNTL)
(TRUE ACC → ADDERS
CARRY → ADDER (35)
ADD → OVT 6 R
106.14-70
106.15-55a
106.16-56
106.17-80
106.07 SENSE (76)(00)(00) (2)
100.39 INST REG SIGN PLUS
150.04 UNIT ADR 11
8e.01 MQ REG 9
122o.36 E R TIME (2)
AND
CF
F. P. ROUND
106.18-127
106.19-82
106.20-83
106.21-56
106.22-57b
106.23-55b
106.24-59

FIG. 106

FIG.107
(SHEET 1 OF 2)



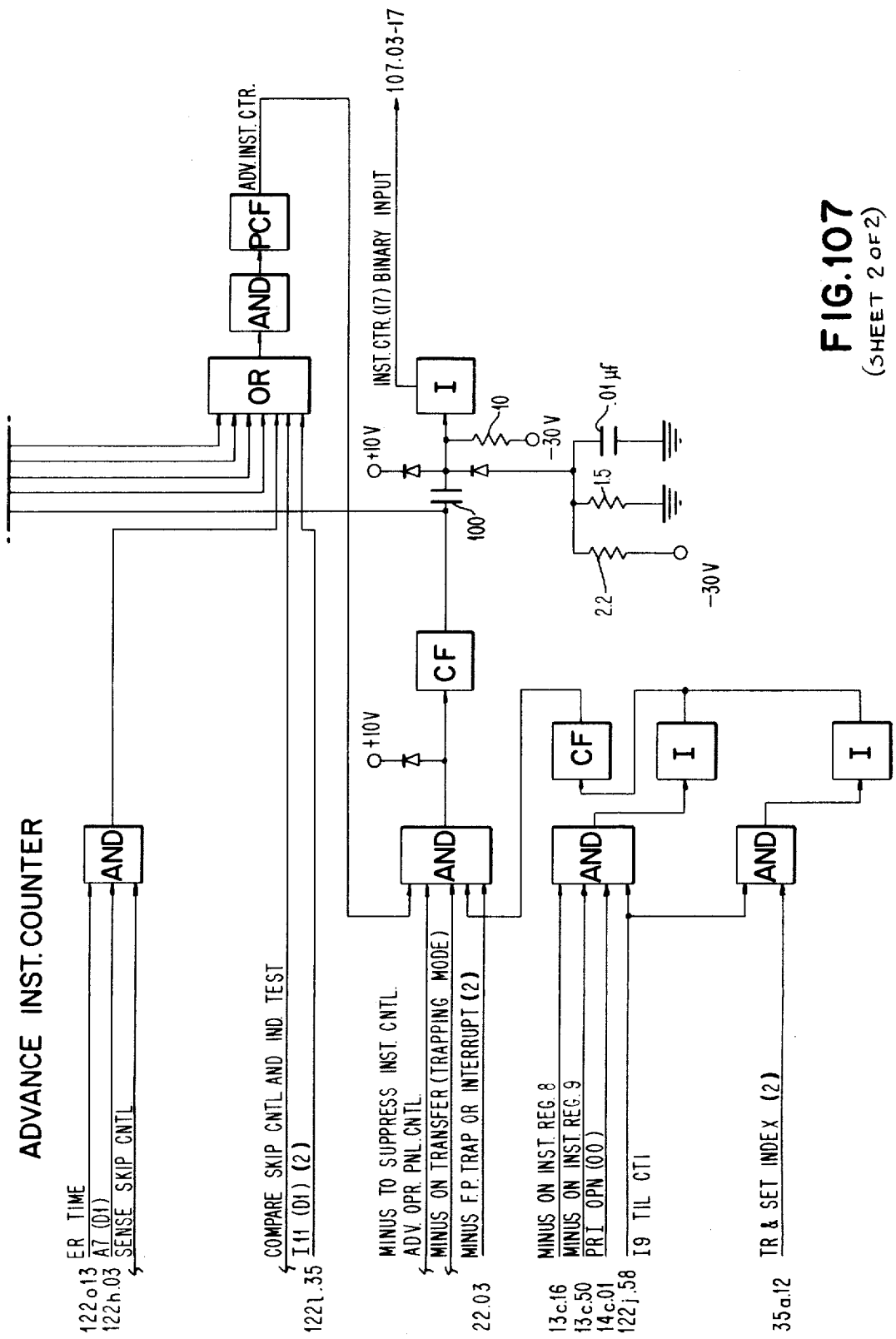


FIG.107
(SHEET 2 OF 2)

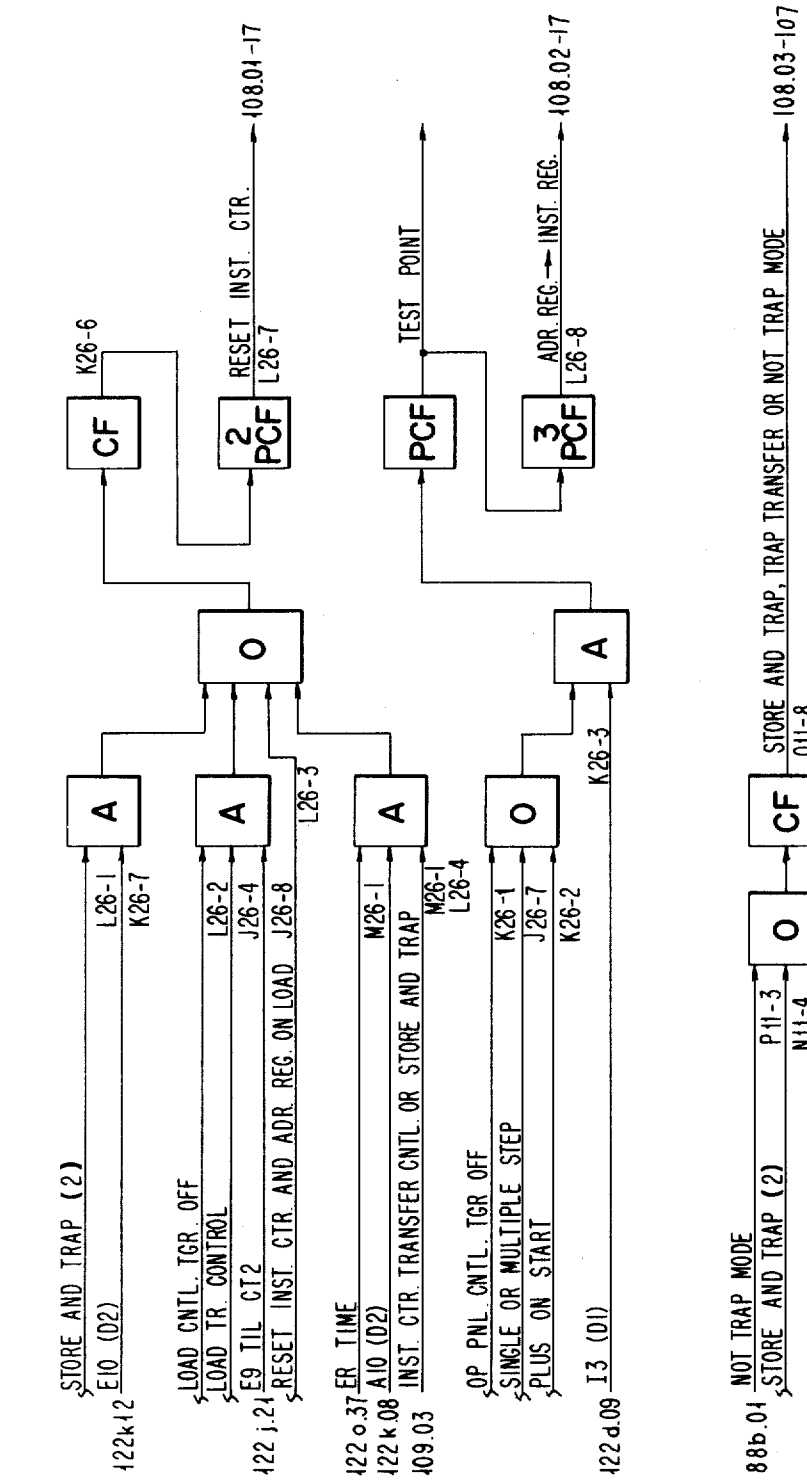

RESET INST. CTR. ADR. SW - INST. CTR.
STORE AND TRAP (2)
E10 (02)
122k12
L26-1
K26-7
A
CF
K26-6
LOAD CNTL. TGR. OFF
LOAD TR. CONTROL
E9 TIL CT2
RESET INST. CTR. AND ADR. REG. ON LOAD
122 j.21
L26-2
J26-4
J26-8
A
O
2 PCF
RESET INST. CTR.
L26-7
108.01-17
L26-3
ER TIME
A10 (02)
INST. CTR. TRANSFER CNTL. OR STORE AND TRAP
122 o.37
122 k.08
409.03
M26-1
M26-1
L26-4
A
PCF
TEST POINT
OP PNL CNTL. TGR OFF
SINGLE OR MULTIPLE STEP
PLUS ON START
I3 (01)
122 d.09
K26-1
J26-7
K26-2
O
3 PCF
ADR. REG. → INST. REG.
L26-8
108.02-17
K26-3
A
88b.01
NOT TRAP MODE
STORE AND TRAP (2)
P11-3
N11-4
O
CF
STORE AND TRAP, TRAP TRANSFER OR NOT TRAP MODE
Q11-8
108.03-107
14c.07
13c.60
13b.13
13c.18
PRI OPN 02
INST. REG. 9
MINUS ON INST. REG.6
MINUS ON INST. REG.8
Q11-3
Q11-4
Q11-6
Q11-7
A

FIG. 108

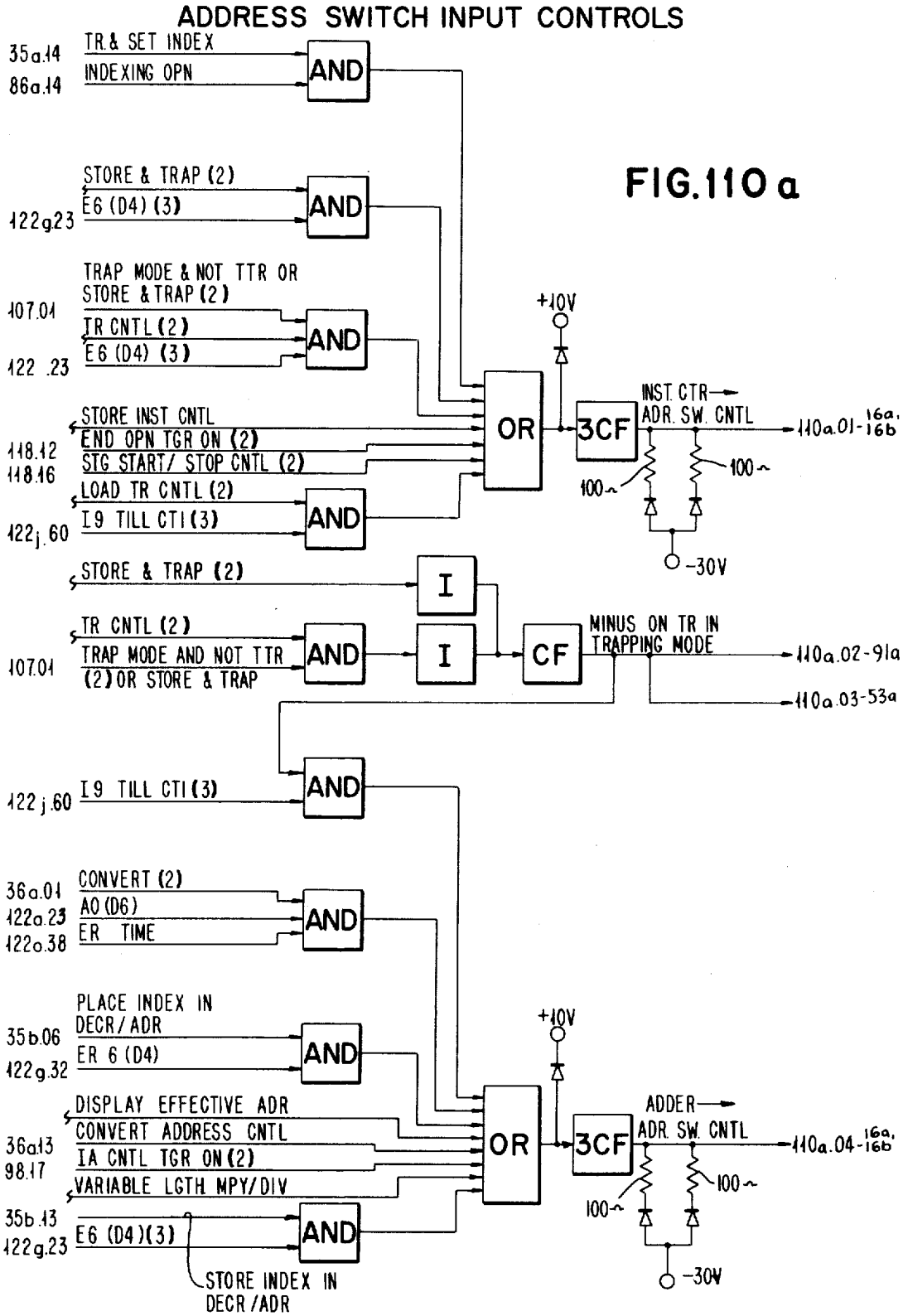

ADDRESS SWITCH INPUT CONTROLS
35a.14
86a.14
TR & SET INDEX
INDEXING OPN
AND
STORE & TRAP (2)
122g.23
E6 (D4) (3)
AND
TRAP MODE & NOT TTR OR STORE & TRAP (2)
107.01
TR CNTL (2)
122 .23
E6 (D4) (3)
AND
+10V
STORE INST CNTL
118.12
END OPN TGR ON (2)
118.16
STG START/ STOP CNTL (2)
OR
3CF
INST CTR ADR. SW. CNTL
110a.01-16a, 16b
100
100
-30V
LOAD TR CNTL (2)
122j.60
I9 TILL CTI (3)
AND
STORE & TRAP (2)
I
TR CNTL (2)
107.01
TRAP MODE AND NOT TTR (2) OR STORE & TRAP
AND
I
CF
MINUS ON TR IN TRAPPING MODE
110a.02-91a
110a.03-53a
122j.60
I9 TILL CTI (3)
AND
36a.01
122a.23
122a.38
CONVERT (2)
AO (D6)
ER TIME
AND
PLACE INDEX IN DECR/ADR
35b.06
122g.32
ER 6 (D4)
AND
+10V
DISPLAY EFFECTIVE ADR
CONVERT ADDRESS CNTL
36a.13
98.17
IA CNTL TGR ON (2)
VARIABLE LGTH MPY/DIV
OR
3CF
ADDER ADR. SW. CNTL
110a.04-16a, 16b
100
100
-30V
35b.13
122g.23
E6 (D4)(3)
AND
STORE INDEX IN DECR/ADR

FIG.110a

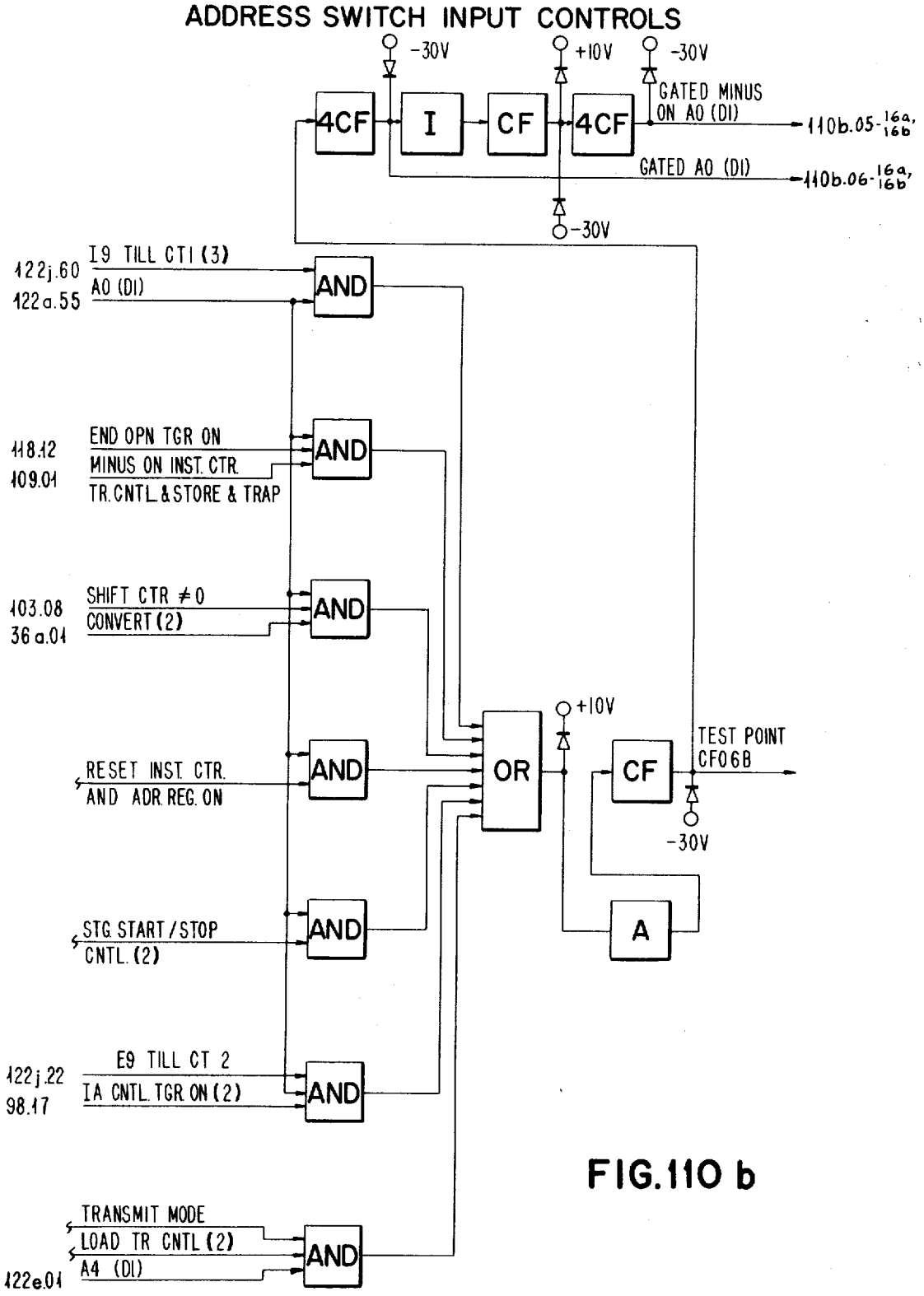

ADDRESS SWITCH INPUT CONTROLS
-30V
+10V
-30V
4CF
I
CF
4CF
GATED MINUS ON A0 (DI)
110b.05-16a, 16b
GATED A0 (DI)
110b.06-16a, 16b
-30V
I9 TILL CTI (3)
122j.60
A0 (DI)
122a.55
AND
END OPN TGR ON
118.12
MINUS ON INST. CTR.
109.01
TR. CNTL. & STORE & TRAP
AND
SHIFT CTR ≠ 0
103.08
CONVERT (2)
36a.01
AND
+10V
RESET INST. CTR.
AND ADR. REG. ON
AND
OR
CF
TEST POINT CF06B
-30V
STG. START / STOP
CNTL. (2)
AND
A
E9 TILL CT 2
122j.22
IA CNTL. TGR. ON (2)
98.17
AND
TRANSMIT MODE
LOAD TR CNTL (2)
A4 (DI)
122e.04
AND

FIG. 110 b

ENTER MQ

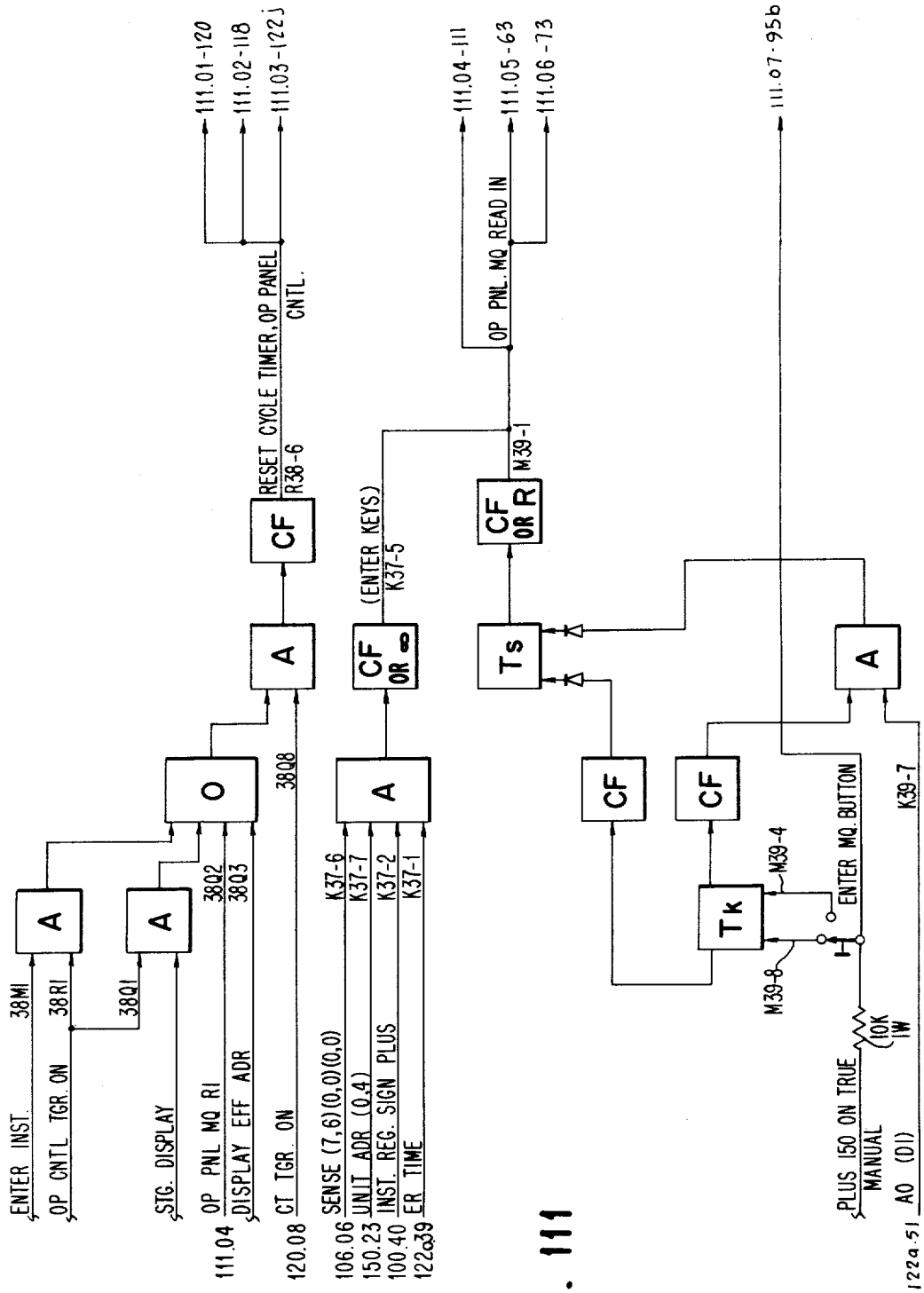
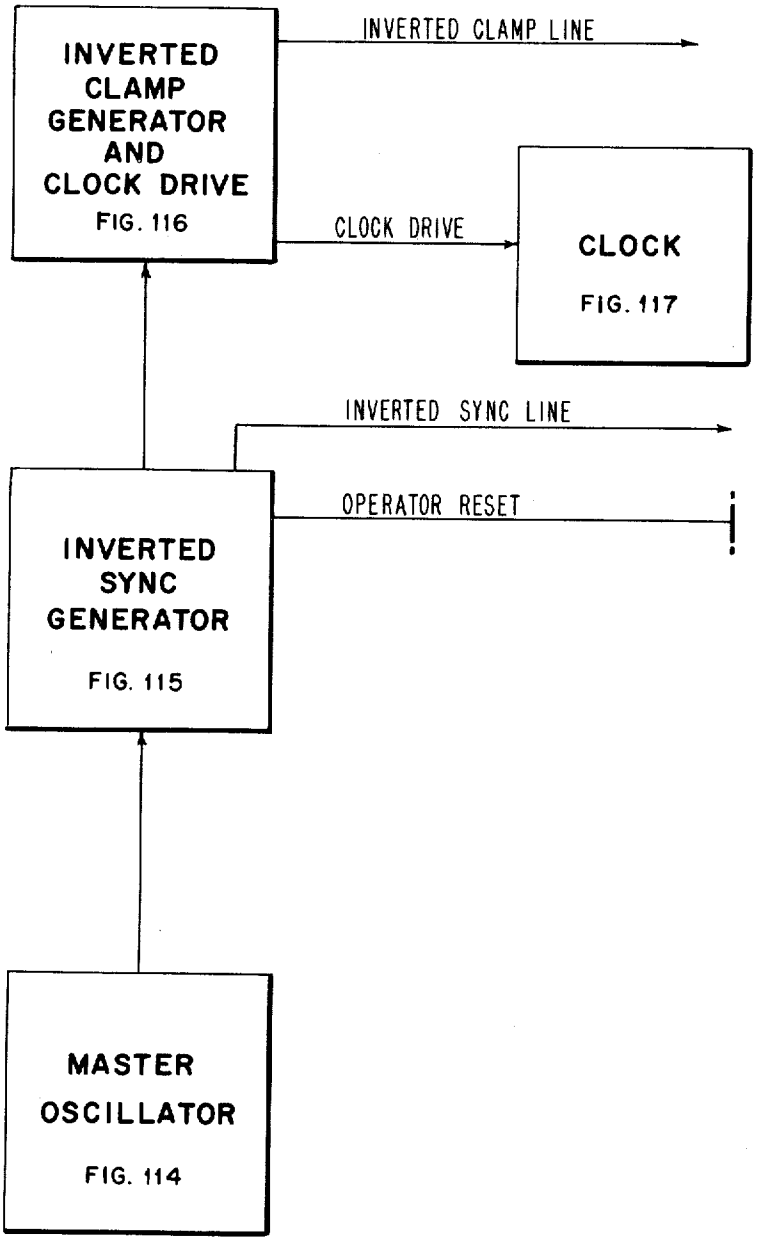


FIG. 111

FIG. 112

PRIMARY DRIVE CIRCUITS



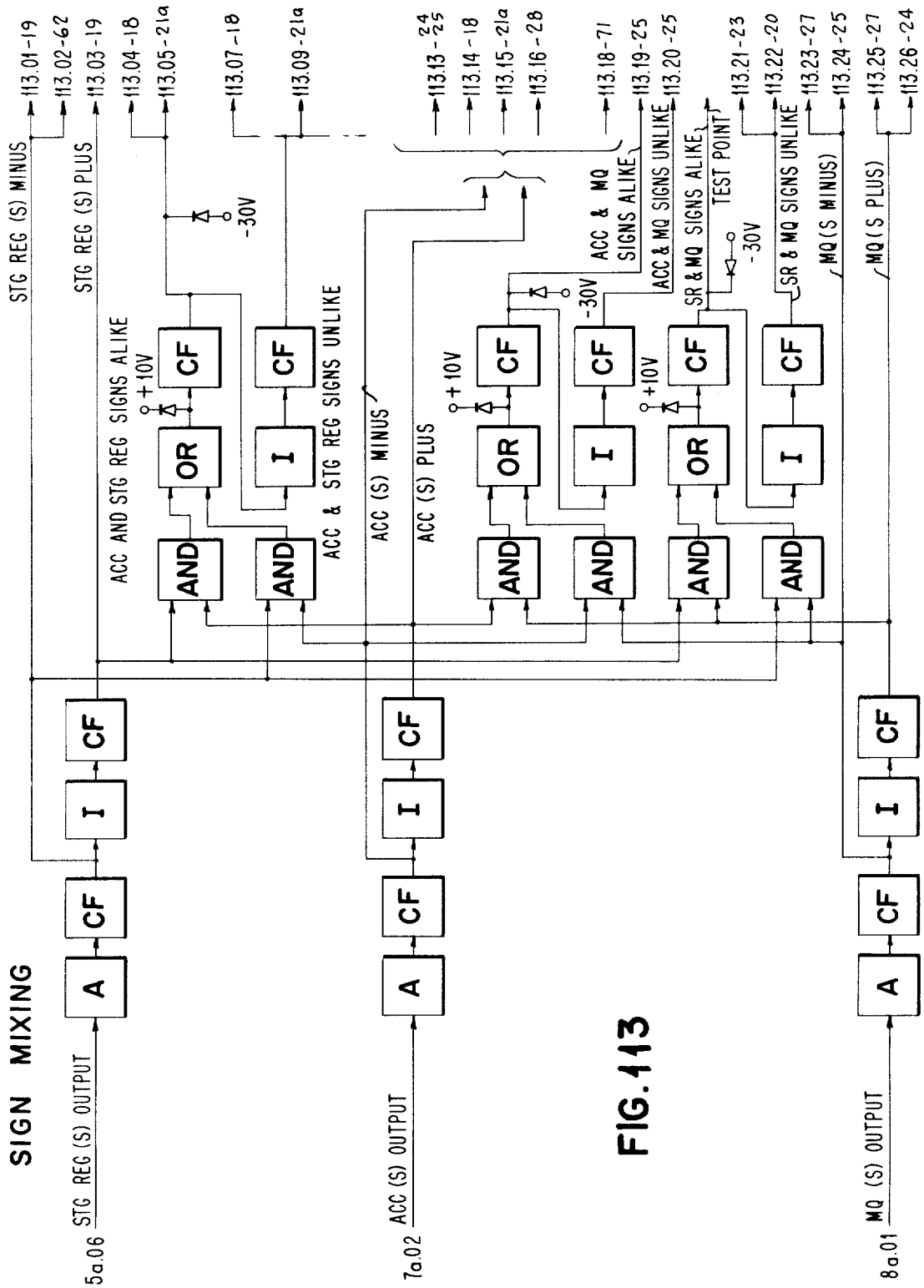

SIGN MIXING
5a.06 STG REG (S) OUTPUT
7a.02 ACC (S) OUTPUT
8a.01 MQ (S) OUTPUT
A
CF
I
AND
OR
+10V
-30V
STG REG (S) MINUS
STG REG (S) PLUS
ACC AND STG REG SIGNS ALIKE
ACC & STG REG SIGNS UNLIKE
ACC (S) MINUS
ACC (S) PLUS
ACC & MQ SIGNS ALIKE
ACC & MQ SIGNS UNLIKE
SR & MQ SIGNS ALIKE
SR & MQ SIGNS UNLIKE
TEST POINT
MQ(S MINUS)
MQ(S PLUS)
113.01-19
113.02-62
113.03-19
113.04-18
113.05-21a
113.07-18
113.09-21a
113.13-24 25
113.14-18
113.15-21a
113.16-28
113.18-71
113.19-25
113.20-25
113.21-23
113.22-20
113.23-27
113.24-25
113.25-27
113.26-24

FIG. 413

FIG. 114

MASTER OSCILLATOR

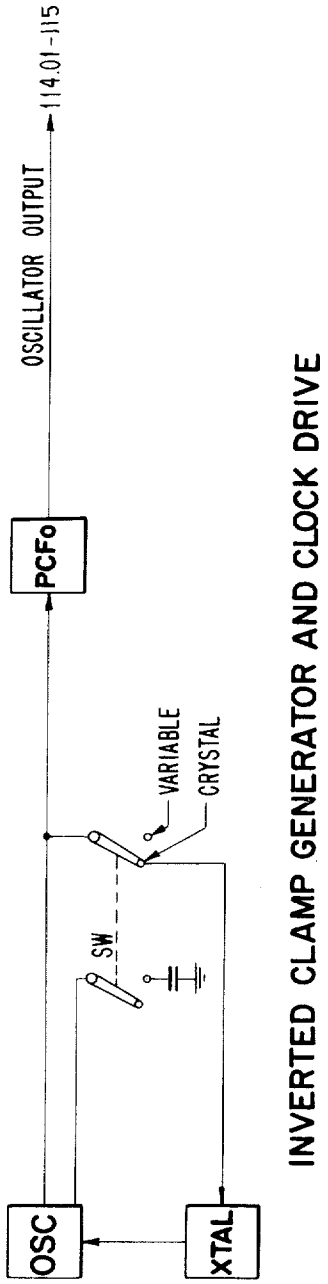


FIG. 116

INVERTED CLAMP GENERATOR AND CLOCK DRIVE

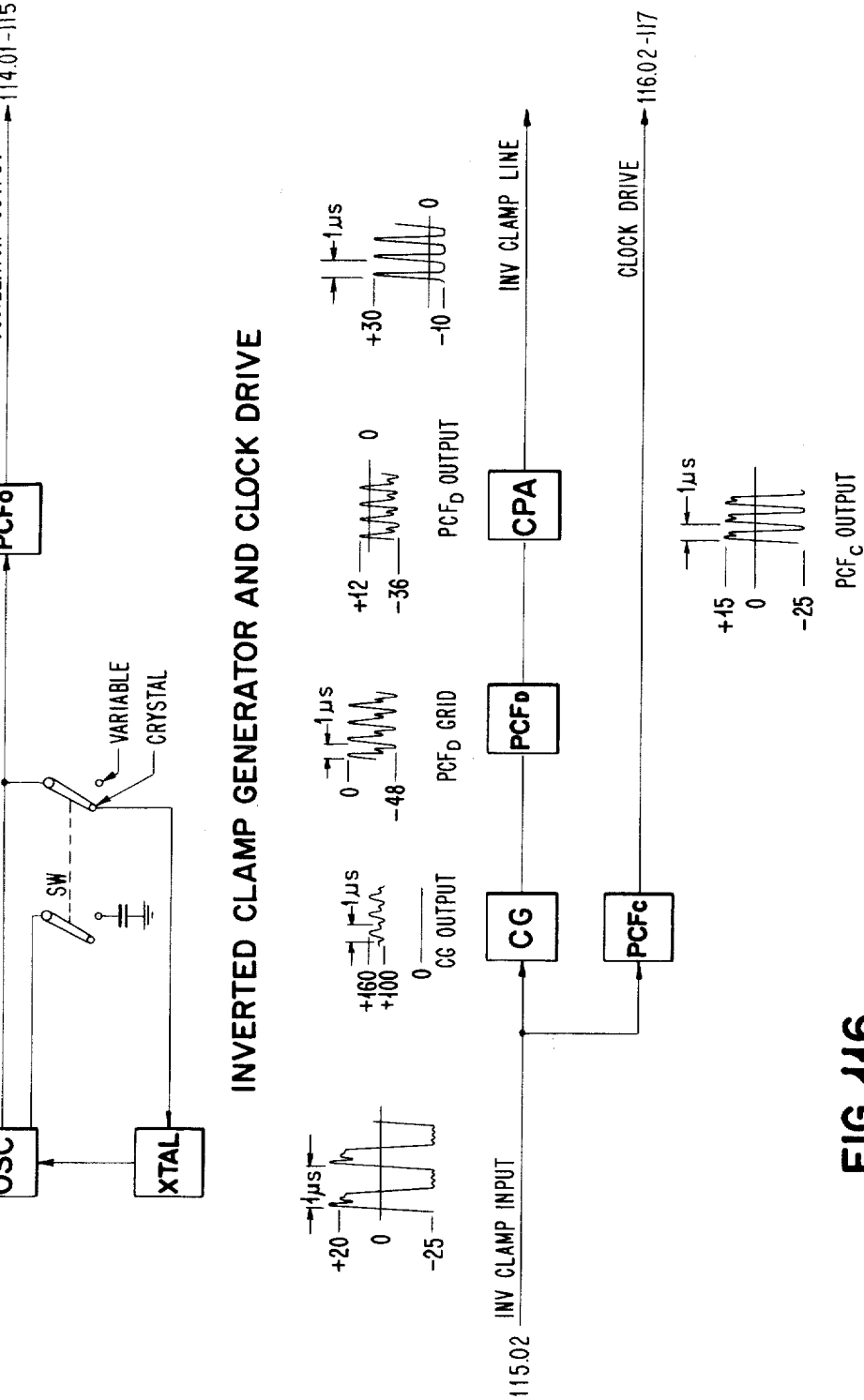
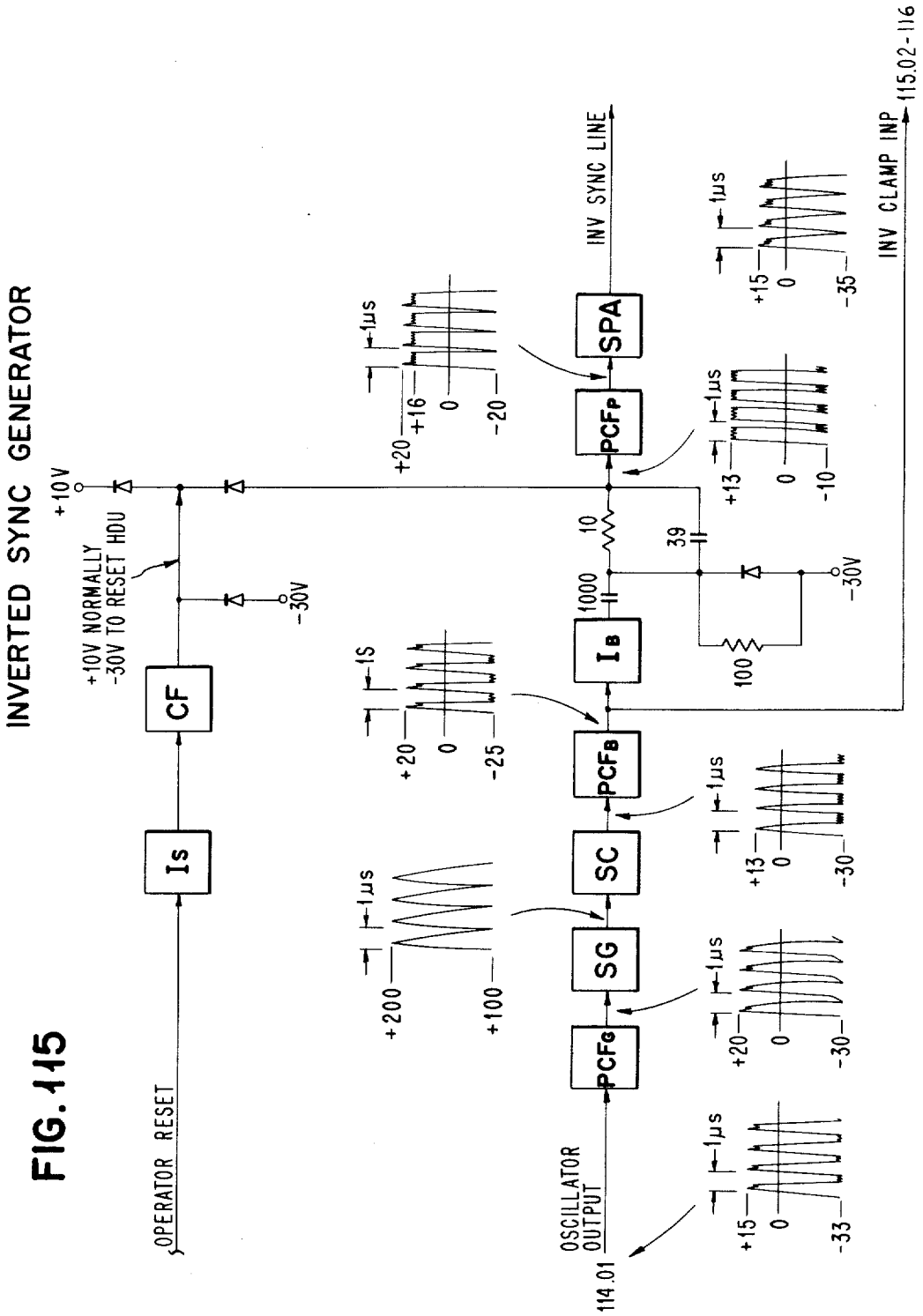


FIG. 115


INVERTED SYNC GENERATOR
OPERATOR RESET
Is
CF
+10V
+10V NORMALLY
-30V TO RESET HDU
-30V
OSCILLATOR
OUTPUT
114.01
PCFG
SG
SC
PCFB
IB
PCFP
SPA
INV SYNC LINE
INV CLAMP INP
115.02-116
10
39
1000
100
-30V
+200
+100
+20
0
-30
+15
-33
+20
-25
+16
-20
+13
-10
-35
1µs
1S

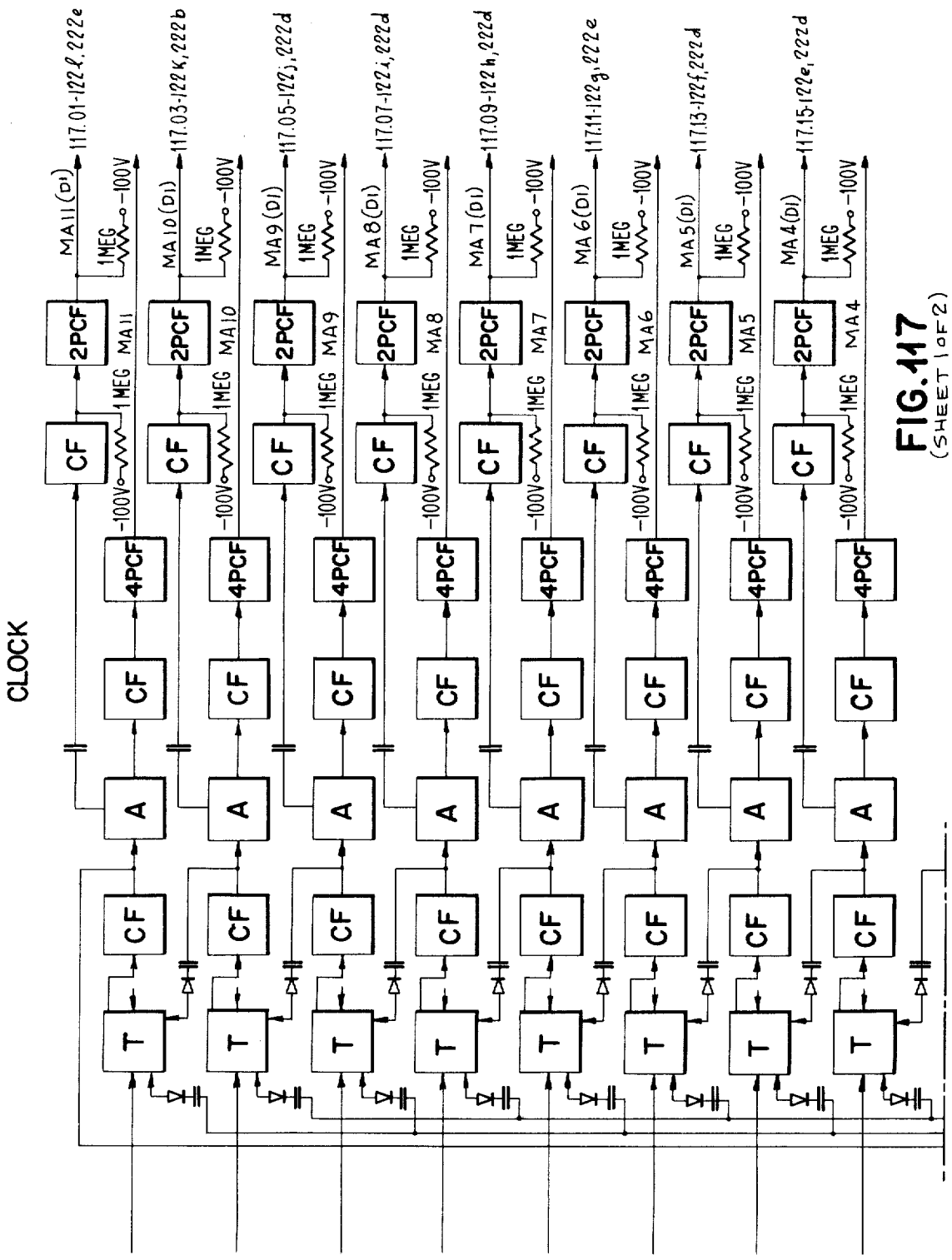


FIG.117
(SHEET 1 OF 2)

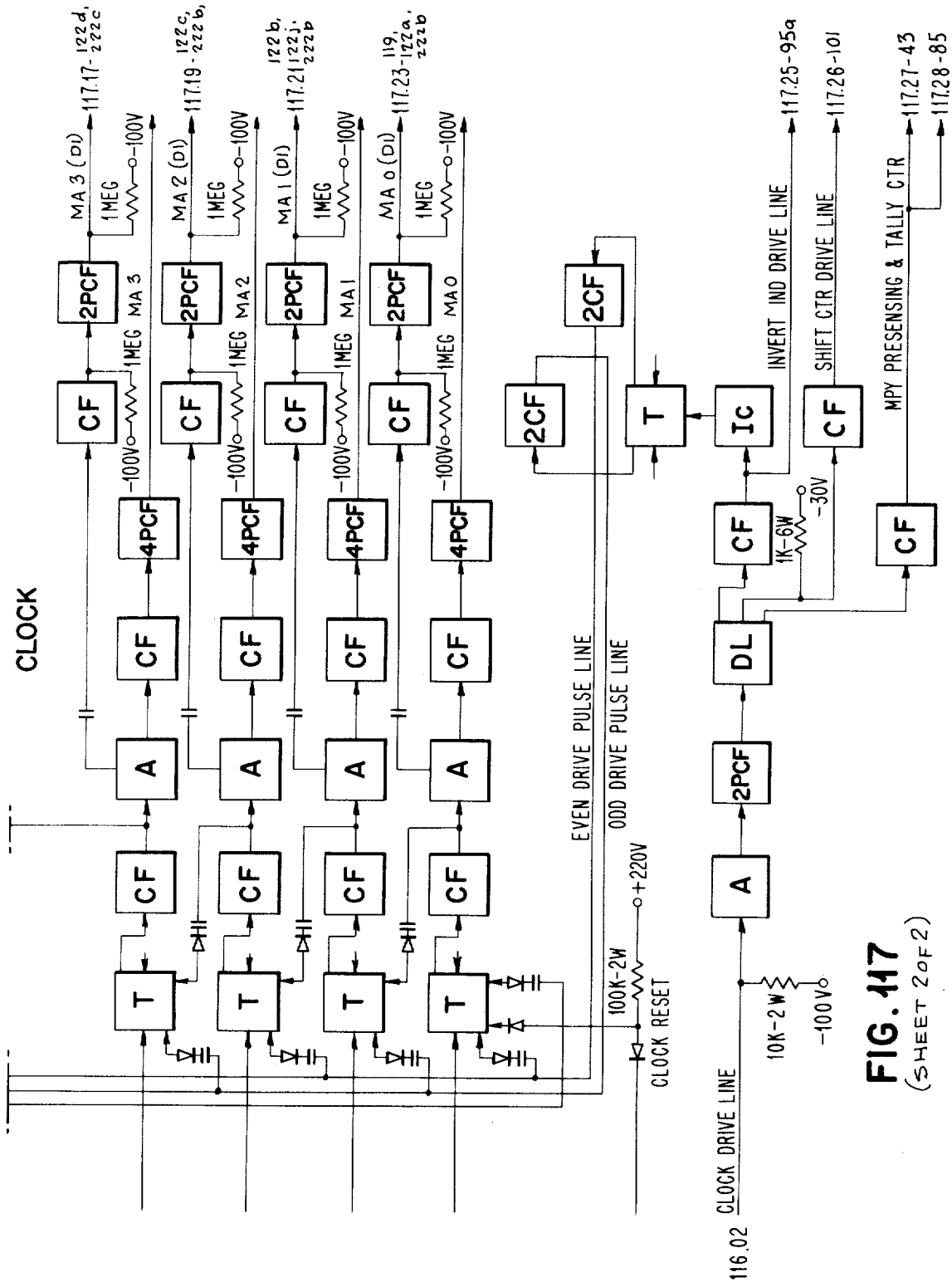
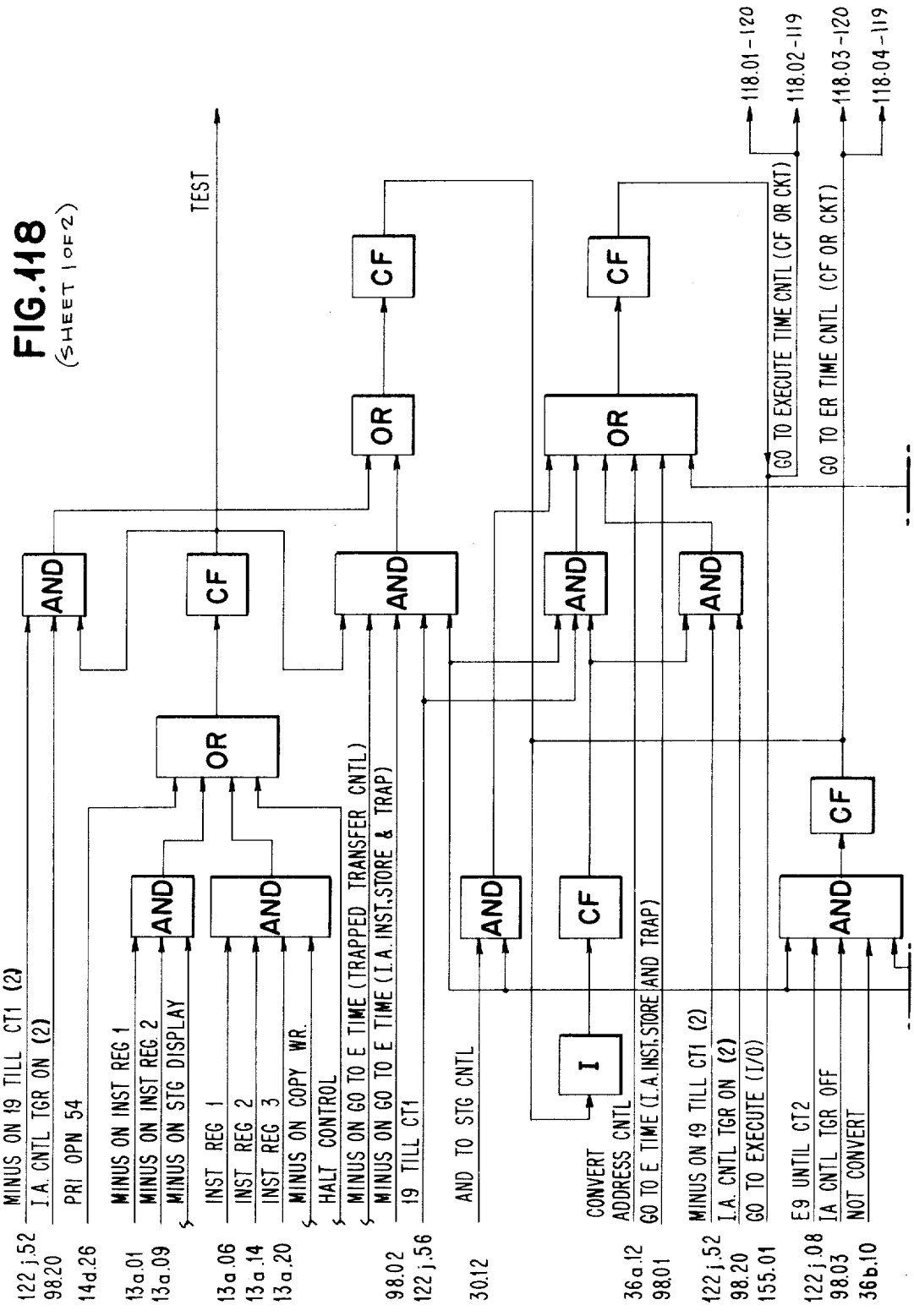


FIG. 117
(SHEET 2 OF 2)

CYCLE TIMER CONTROL

FIG.118
(SHEET 1 OF 2)



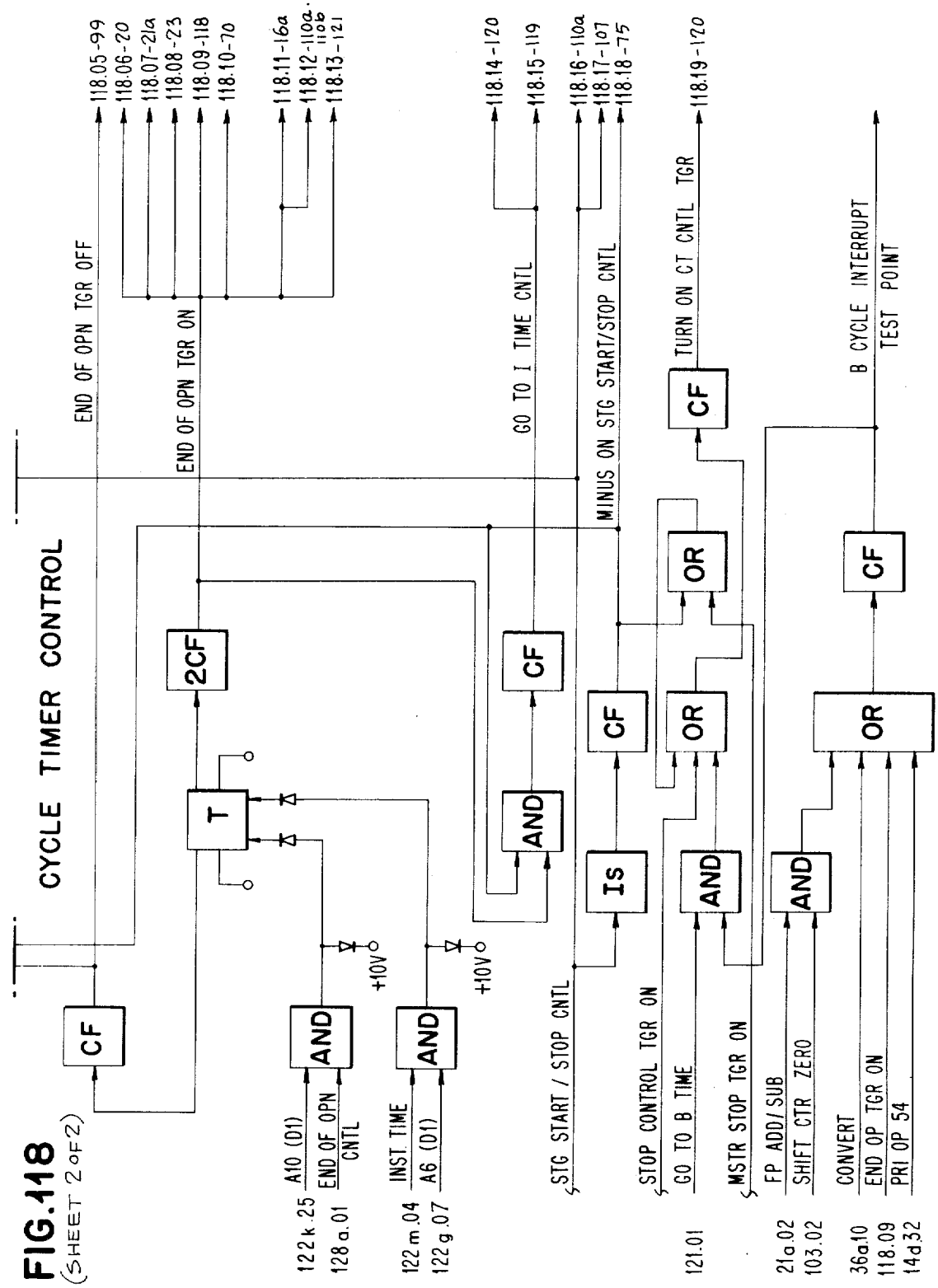


FIG.118
(SHEET 2 OF 2)

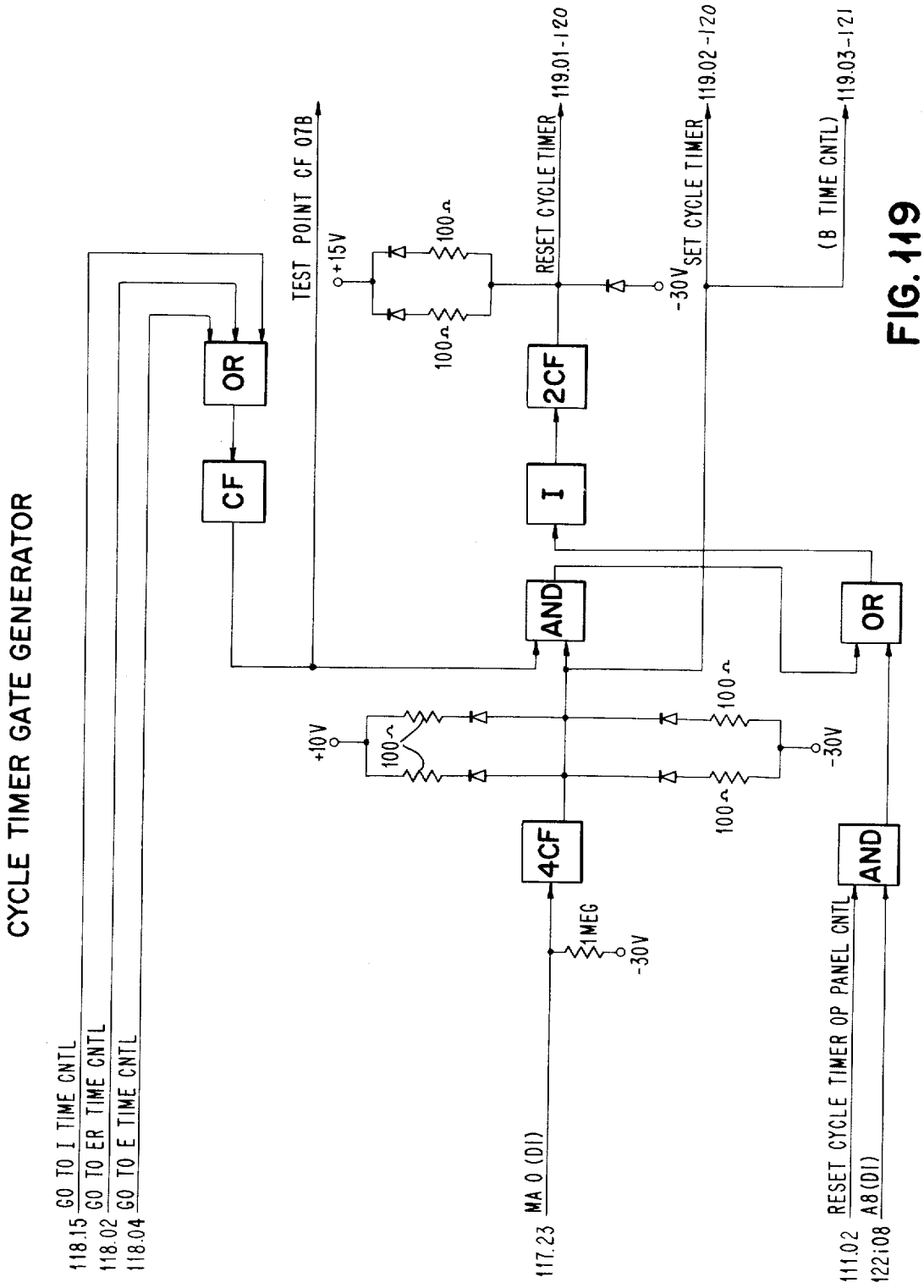
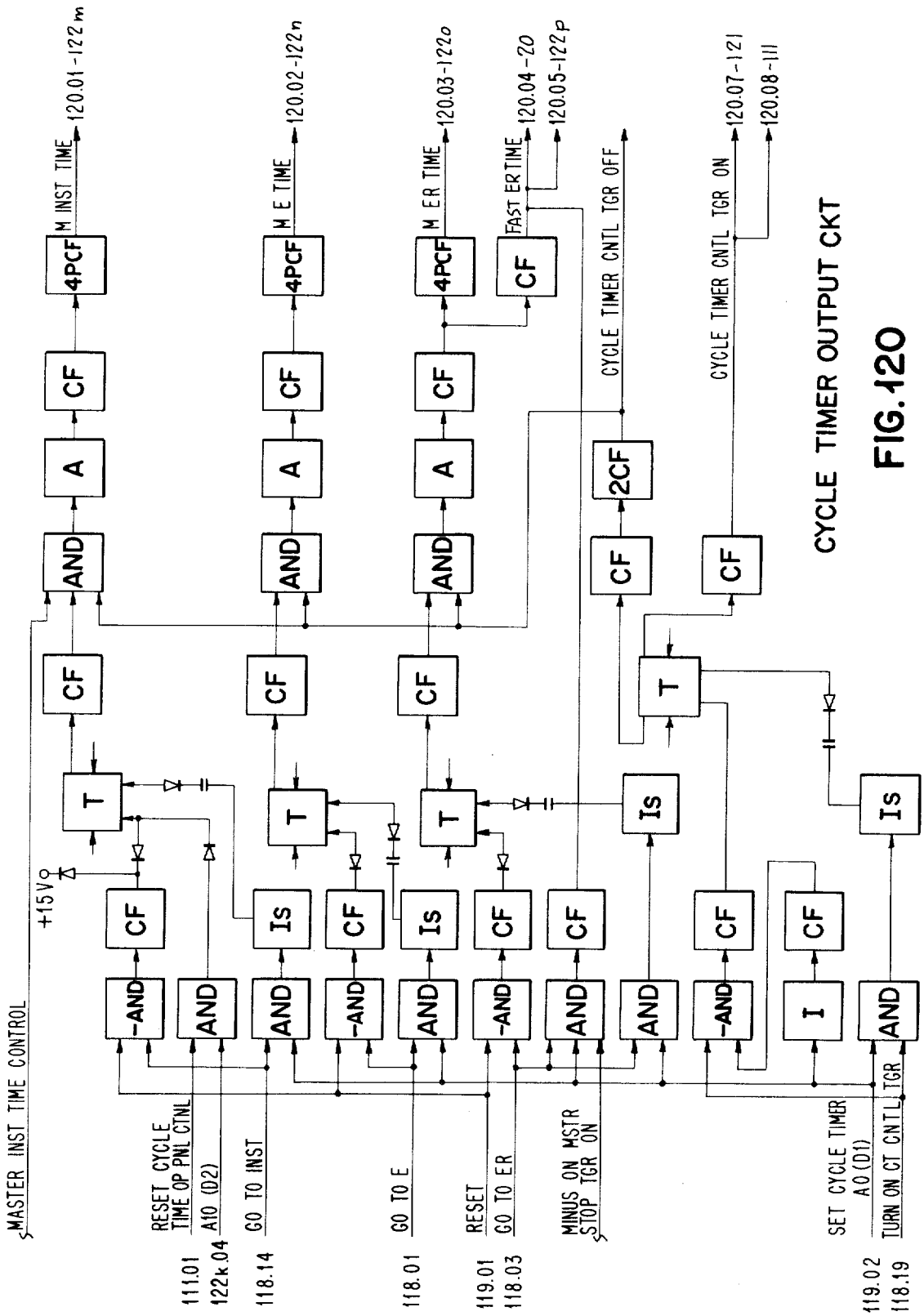

CYCLE TIMER GATE GENERATOR
118.15 GO TO I TIME CNTL
118.02 GO TO ER TIME CNTL
118.04 GO TO E TIME CNTL
OR
CF
TEST POINT CF 07B
+15V
100Ω
100Ω
RESET CYCLE TIMER
119.01-120
-30V
SET CYCLE TIMER
119.02-120
(B TIME CNTL)
119.03-121
2CF
I
AND
OR
+10V
100Ω
100Ω
100Ω
-30V
4CF
1MEG
-30V
117.23 MA 0 (DI)
AND
111.02 RESET CYCLE TIMER OP PANEL CNTL
122i08 A8 (DI)

FIG. 119

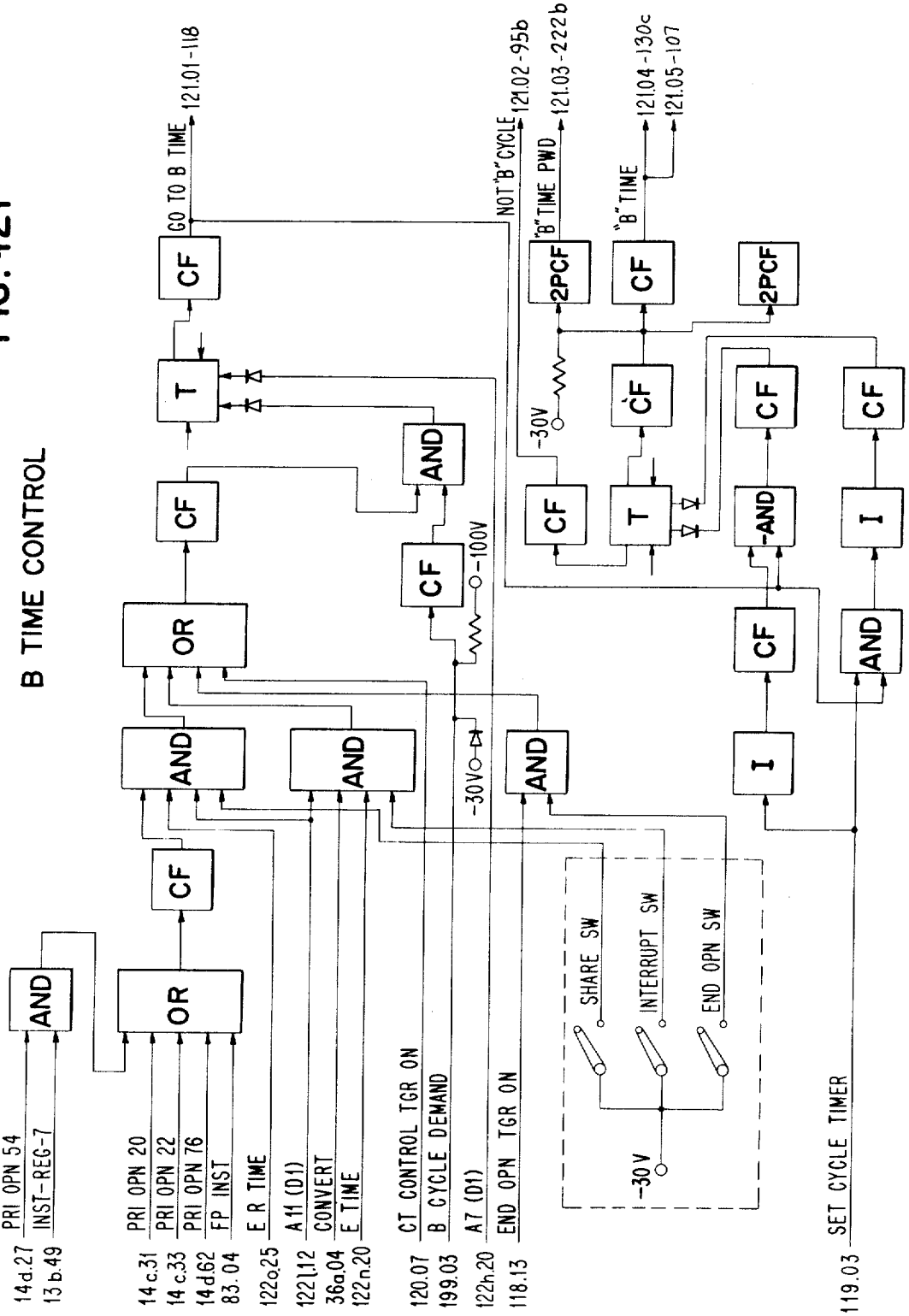


CYCLE TIMER OUTPUT CKT

FIG. 120

FIG. 121

B TIME CONTROL



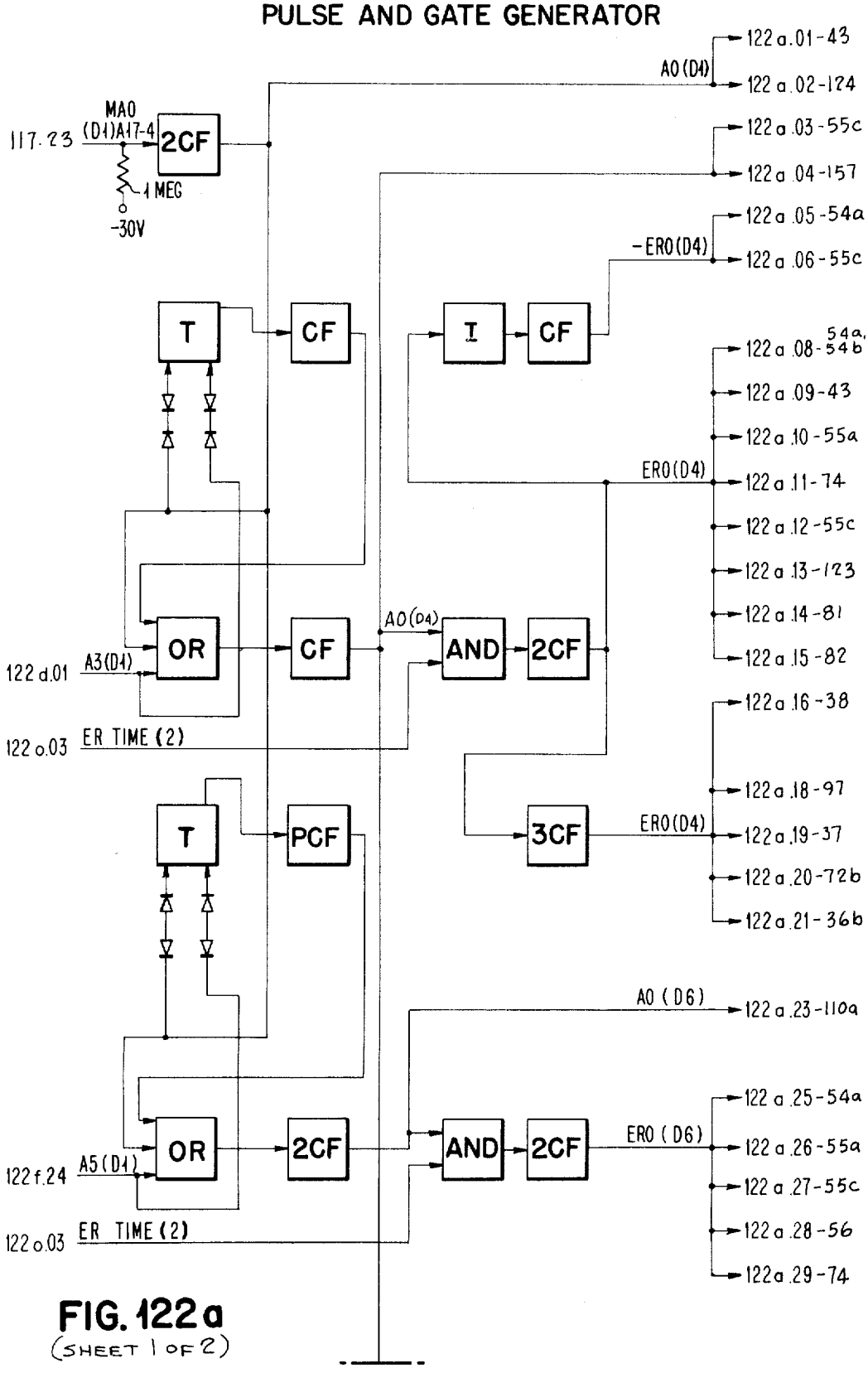


FIG. 122a
(SHEET 1 OF 2)

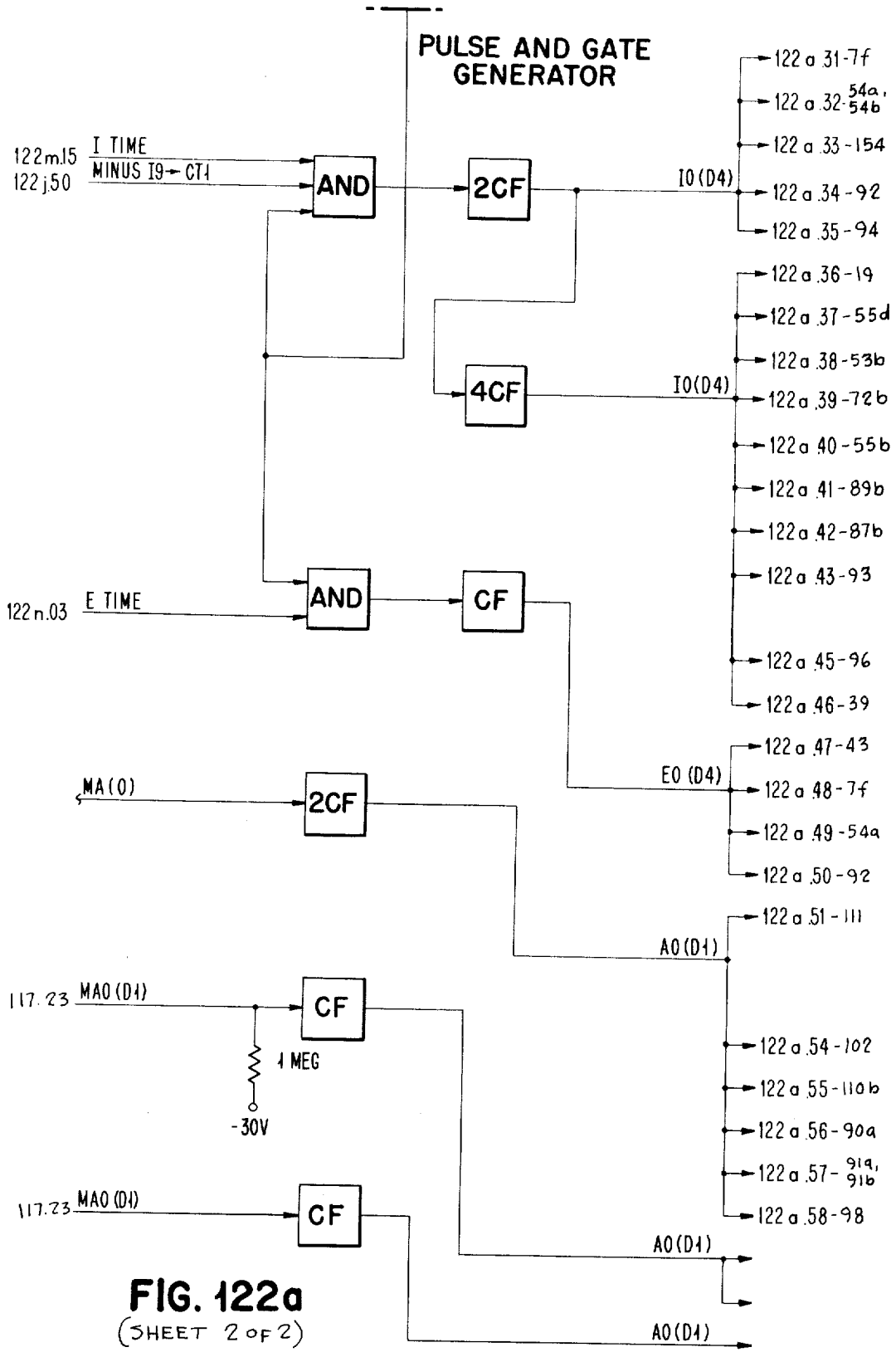


FIG. 122a
(SHEET 2 OF 2)

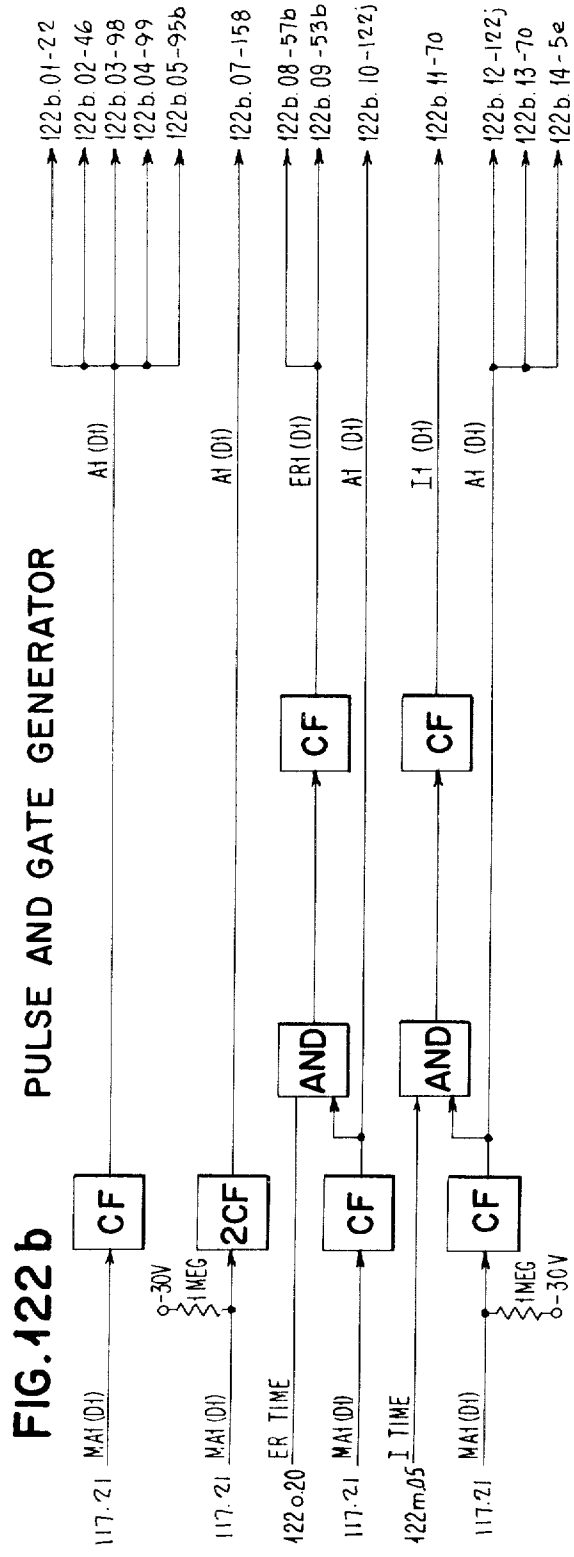


FIG.122b

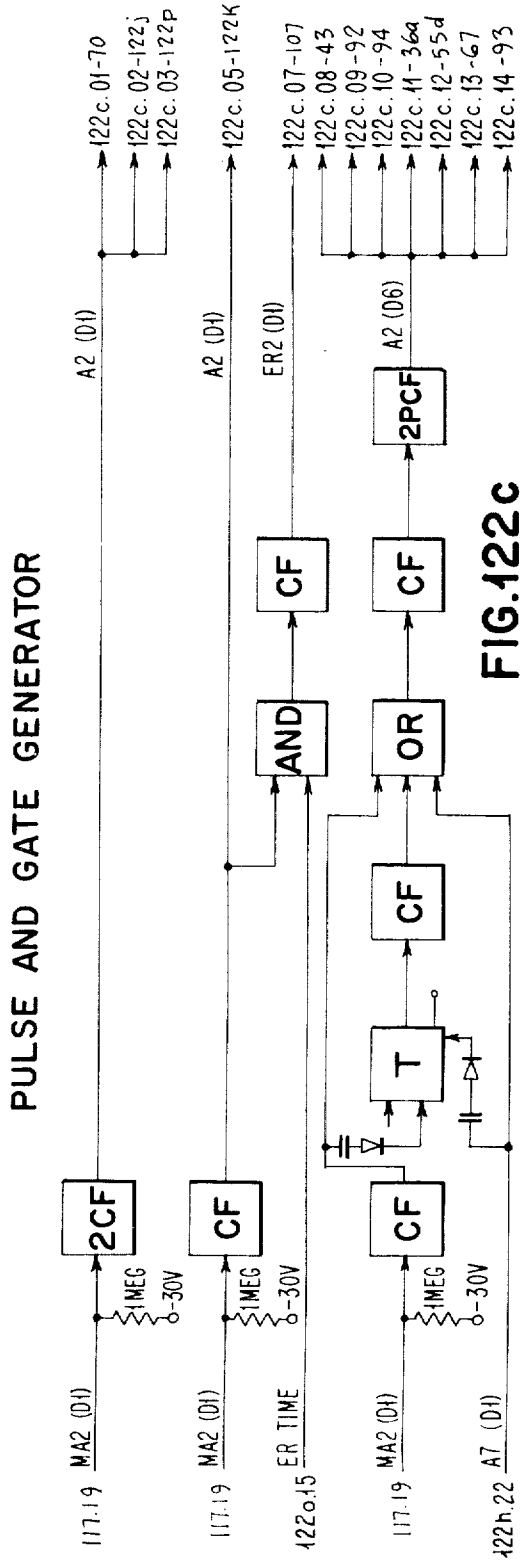


FIG.122c

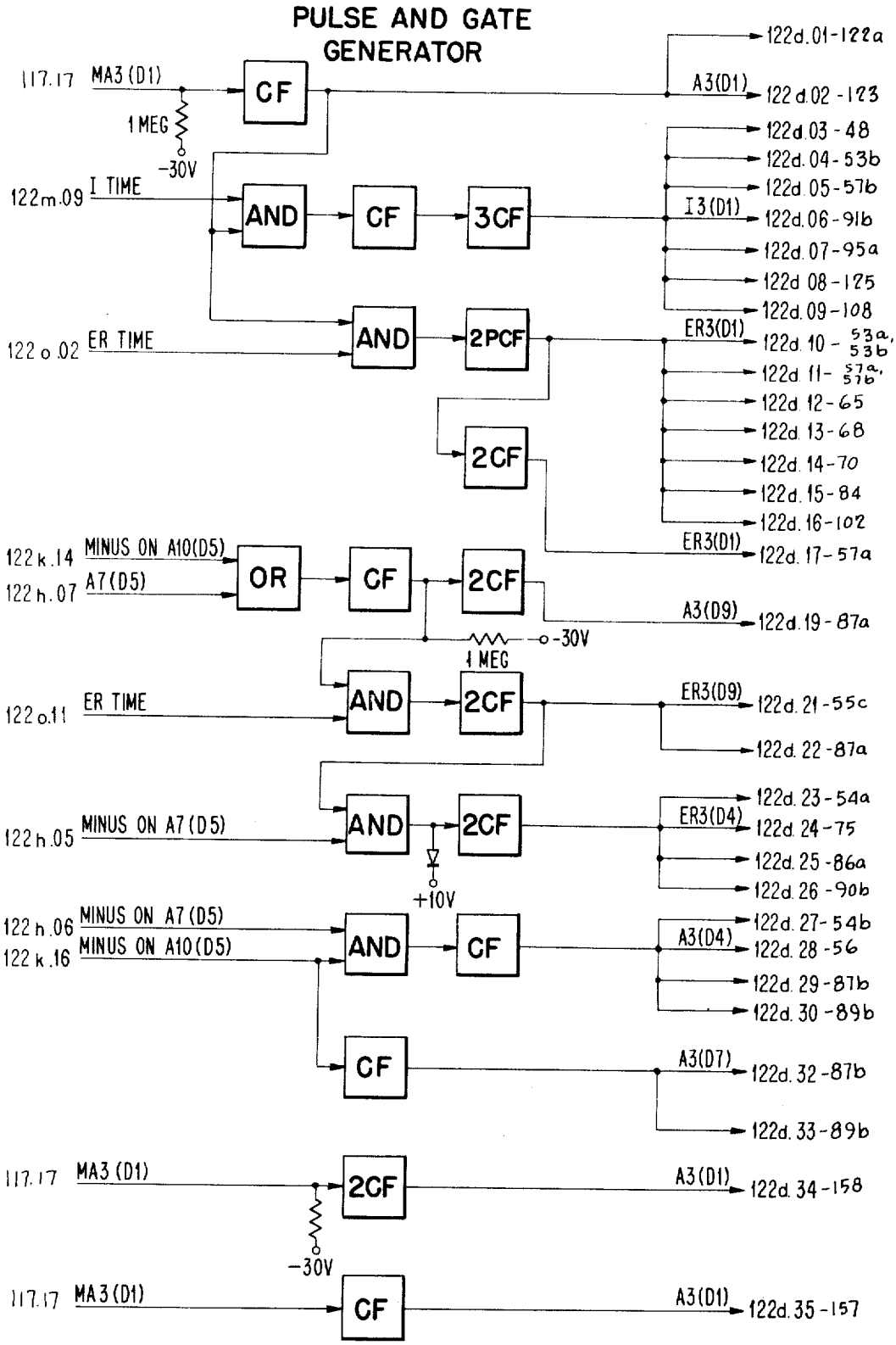
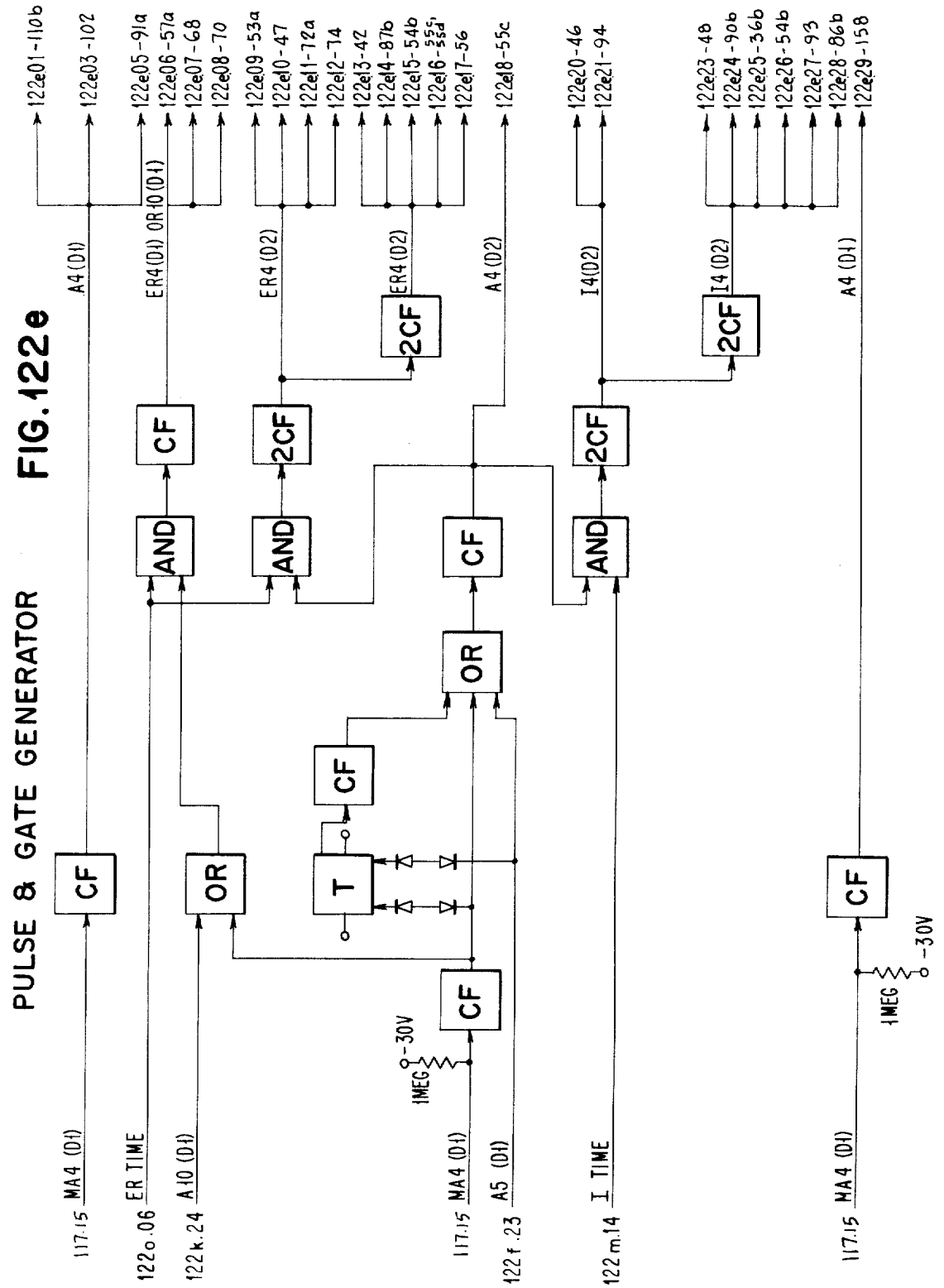

PULSE AND GATE GENERATOR
117.17 MA3 (D1)
1 MEG
-30V
CF
122d.01-122a
A3(D1)
122d.02-123
122m.09 I TIME
AND
CF
3CF
I3(D1)
122d.03-48
122d.04-53b
122d.05-57b
122d.06-91b
122d.07-95a
122d.08-125
122d.09-108
122o.02 ER TIME
AND
2PCF
ER3(D1)
122d.10-53a, 53b
122d.11-57a, 57b
122d.12-65
122d.13-68
122d.14-70
122d.15-84
122d.16-102
2CF
ER3(D1)
122d.17-57a
122k.14 MINUS ON A10(D5)
122h.07 A7(D5)
OR
CF
2CF
A3(D9)
122d.19-87a
-30V
1 MEG
122o.11 ER TIME
AND
2CF
ER3(D9)
122d.21-55c
122d.22-87a
122h.05 MINUS ON A7(D5)
AND
2CF
ER3(D4)
122d.23-54a
122d.24-75
122d.25-86a
122d.26-90b
+10V
122h.06 MINUS ON A7(D5)
122k.16 MINUS ON A10(D5)
AND
CF
A3(D4)
122d.27-54b
122d.28-56
122d.29-87b
122d.30-89b
CF
A3(D7)
122d.32-87b
122d.33-89b
117.17 MA3 (D1)
2CF
A3(D1)
122d.34-158
-30V
117.17 MA3 (D1)
CF
A3(D1)
122d.35-157

FIG. 122d

FIG. 122e

PULSE & GATE GENERATOR



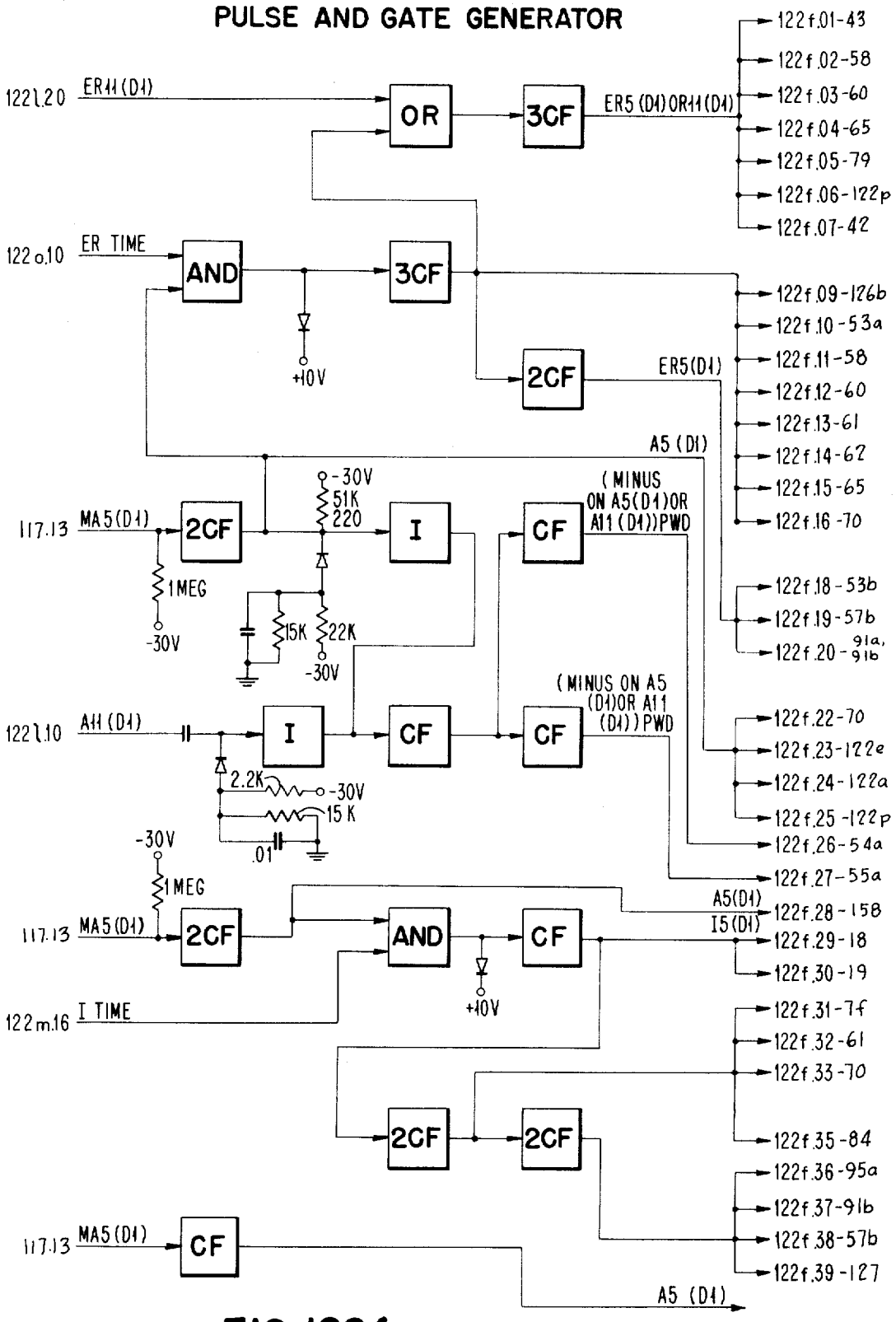

PULSE AND GATE GENERATOR
122l.20
ER11(D1)
OR
3CF
ER5(D1)OR11(D1)
122f.01-43
122f.02-58
122f.03-60
122f.04-65
122f.05-79
122f.06-122p
122f.07-42
122o.10
ER TIME
AND
3CF
+10V
2CF
ER5(D1)
122f.09-126b
122f.10-53a
122f.11-58
122f.12-60
122f.13-61
122f.14-62
122f.15-65
122f.16-70
A5(D1)
-30V
51K
220
117.13
MA5(D1)
2CF
I
CF
(MINUS ON A5(D1)OR A11(D1))PWD
1MEG
-30V
15K
22K
-30V
122f.18-53b
122f.19-57b
122f.20-91a, 91b
122l.10
A11(D1)
I
CF
CF
(MINUS ON A5 (D1)OR A11 (D1))PWD
2.2K
-30V
15K
.01
122f.22-70
122f.23-122e
122f.24-122a
122f.25-122p
122f.26-54a
122f.27-55a
-30V
1MEG
117.13
MA5(D1)
2CF
AND
CF
A5(D1)
I5(D1)
122f.28-158
122f.29-18
122f.30-19
+10V
122m.16
I TIME
122f.31-7f
122f.32-61
122f.33-70
2CF
2CF
122f.35-84
122f.36-95a
122f.37-91b
122f.38-57b
122f.39-127
117.13
MA5(D1)
CF
A5(D1)

FIG.122f

PULSE AND GATE GENERATOR

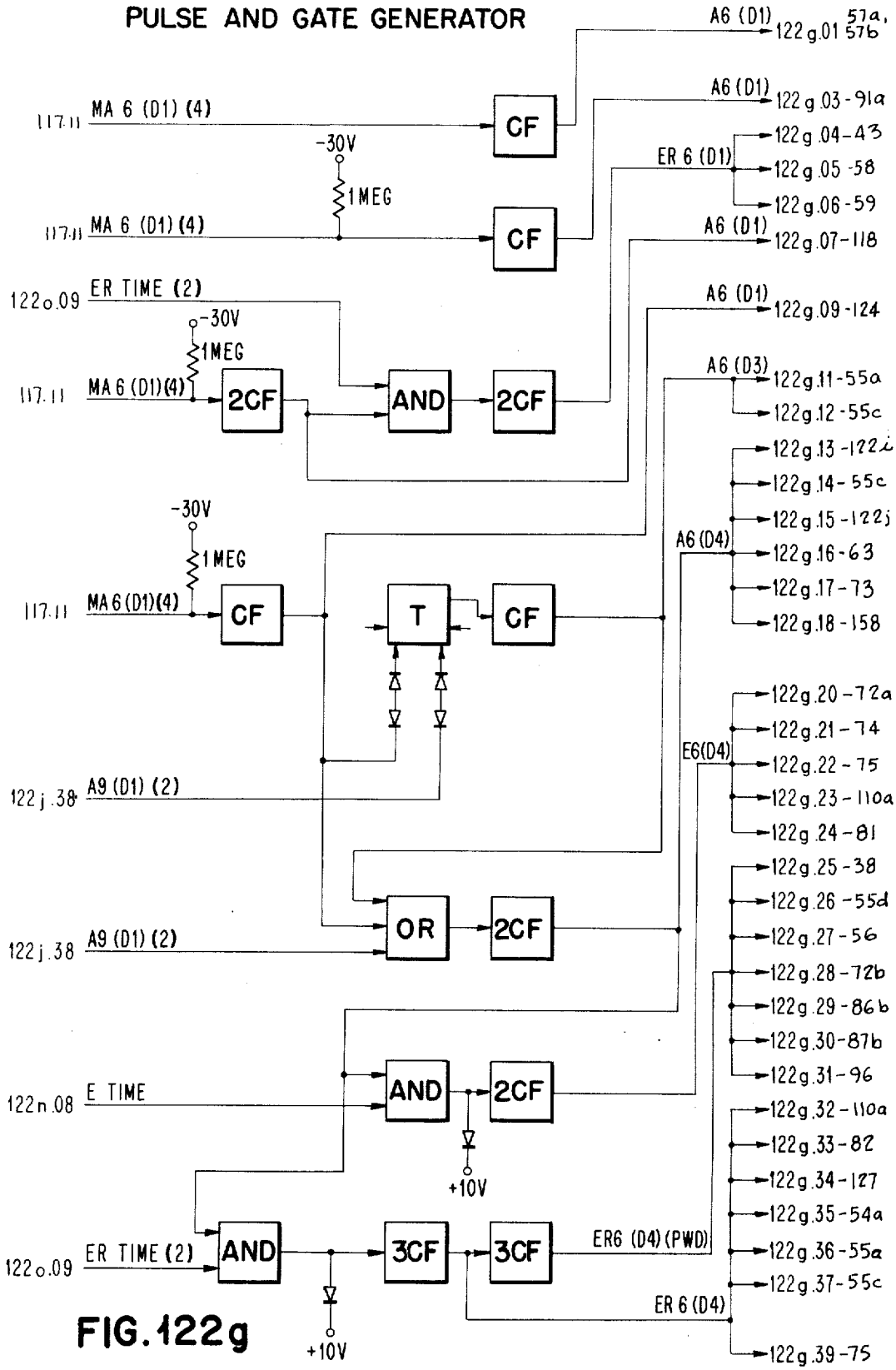


FIG. 122g

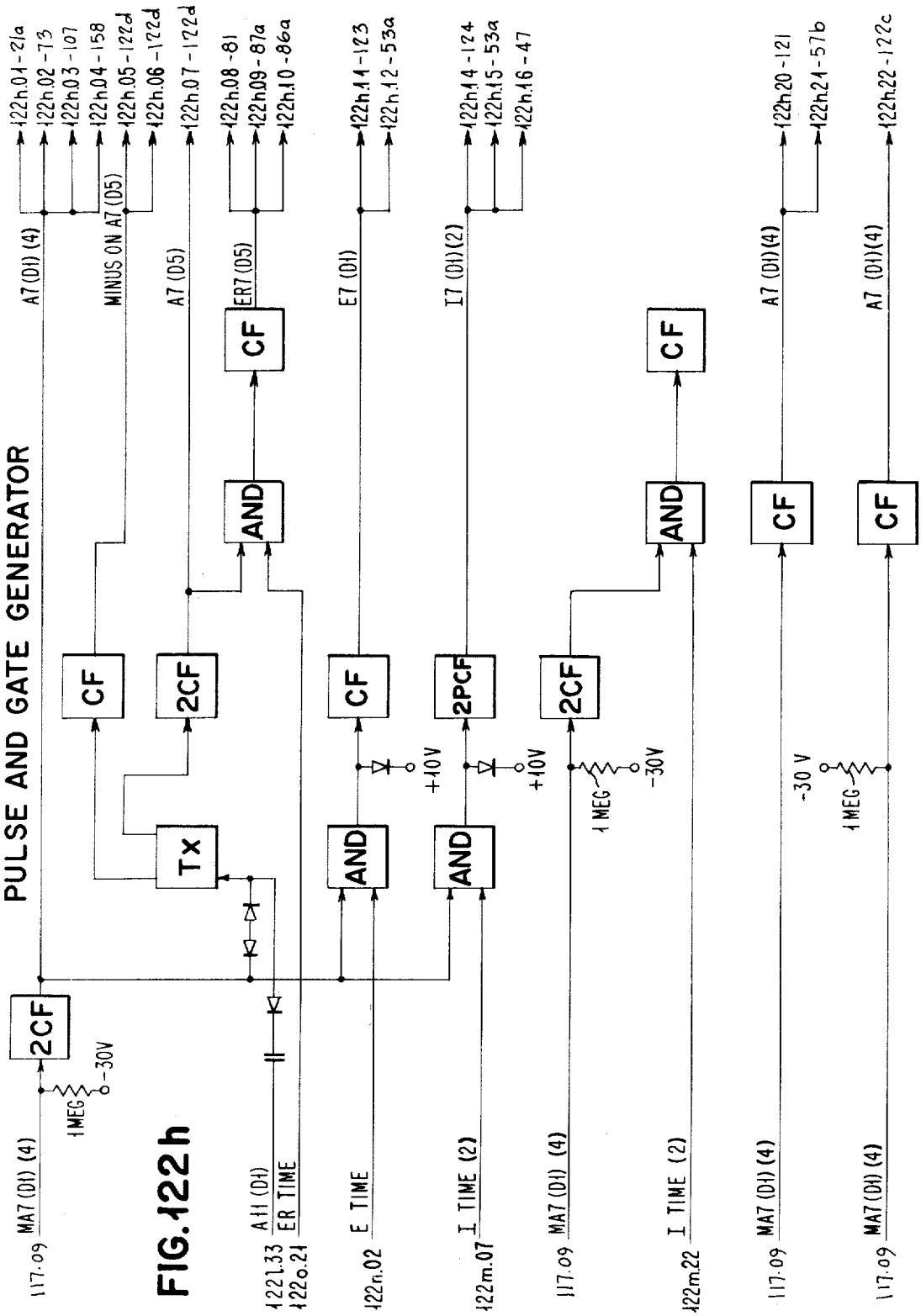
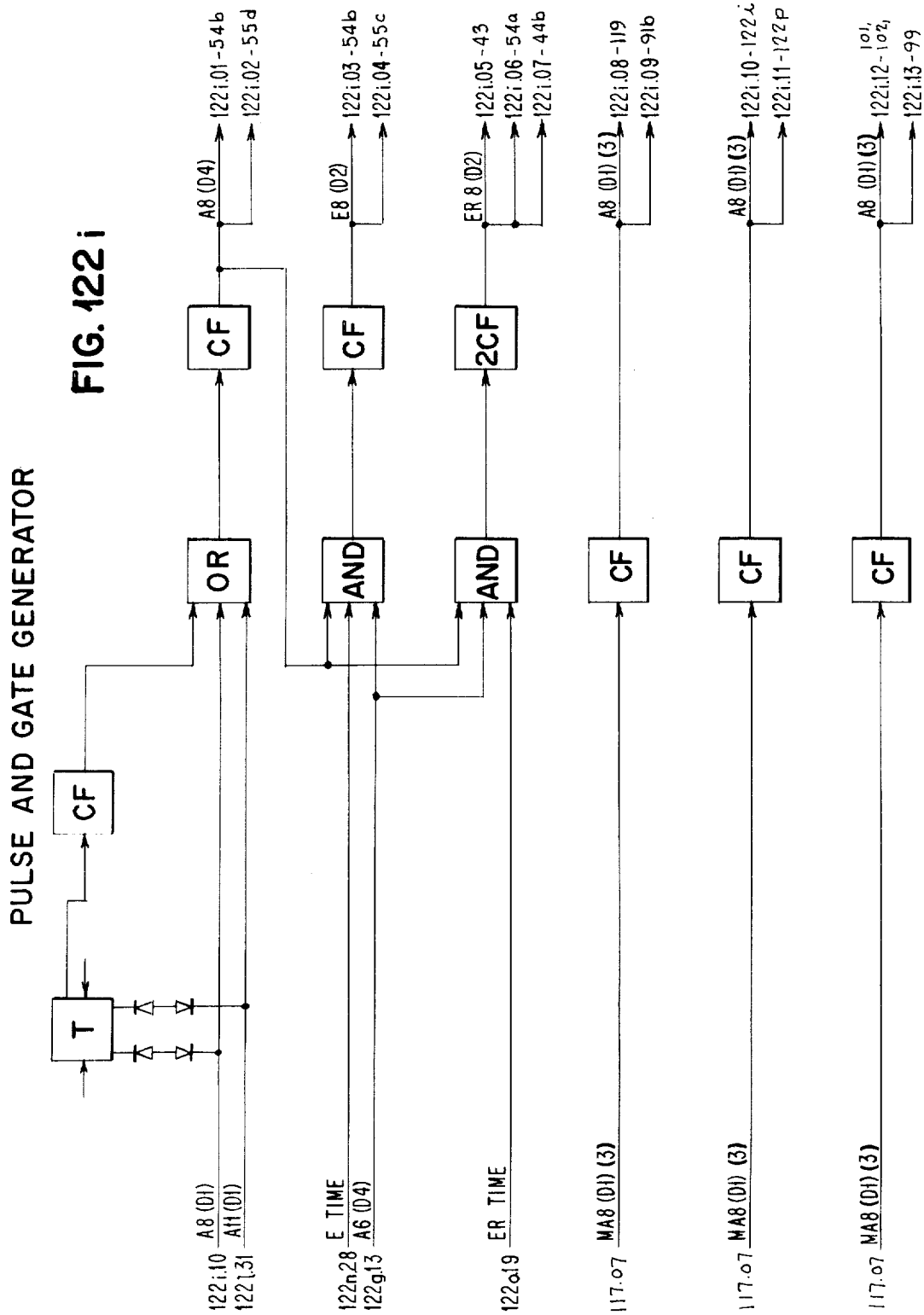

PULSE AND GATE GENERATOR
2CF
CF
2CF
Tx
AND
CF
ER7 (D5)
AND
CF
2PCF
AND
2CF
AND
CF
CF
CF
CF
1 MEG
-30V
+10V
+10V
1 MEG
-30V
-30 V
1 MEG
A7 (D1) (4)
MINUS ON A7 (D5)
A7 (D5)
E7 (D1)
I7 (D1)(2)
A7 (D1)(4)
A7 (D1)(4)
A7 (D1)(4)
117.09 MA7 (D1) (4)
1221.33 A11 (D1)
122o.21 ER TIME
122n.02 E TIME
122m.07 I TIME (2)
117.09 MA7 (D1) (4)
122m.22 I TIME (2)
117.09 MA7 (D1) (4)
117.09 MA7 (D1) (4)
122h.01-21a
122h.02-73
122h.03-107
122h.04-158
122h.05-122d
122h.06-122d
122h.07-122d
122h.08-81
122h.09-87a
122h.10-86a
122h.11-123
122h.12-53a
122h.14-124
122h.15-53a
122h.16-47
122h.20-121
122h.21-57b
122h.22-122c

FIG.122h

FIG. 122 i


PULSE AND GATE GENERATOR
T
CF
OR
CF
AND
CF
AND
2CF
CF
CF
CF
A8 (D1)
A11 (D1)
122i.10
122i.31
E TIME
A6 (D4)
122n.28
122g.13
ER TIME
122a.19
MA8 (D1) (3)
117.07
A8 (D4)
122i.01-54b
122i.02-55d
E8 (D2)
122i.03-54b
122i.04-55c
ER 8 (D2)
122i.05-43
122i.06-54a
122i.07-44b
A8 (D1) (3)
122i.08-119
122i.09-91b
A8 (D1) (3)
122i.10-122i
122i.11-122p
A8 (D1) (3)
122i.12-101, 102,
122i.13-99

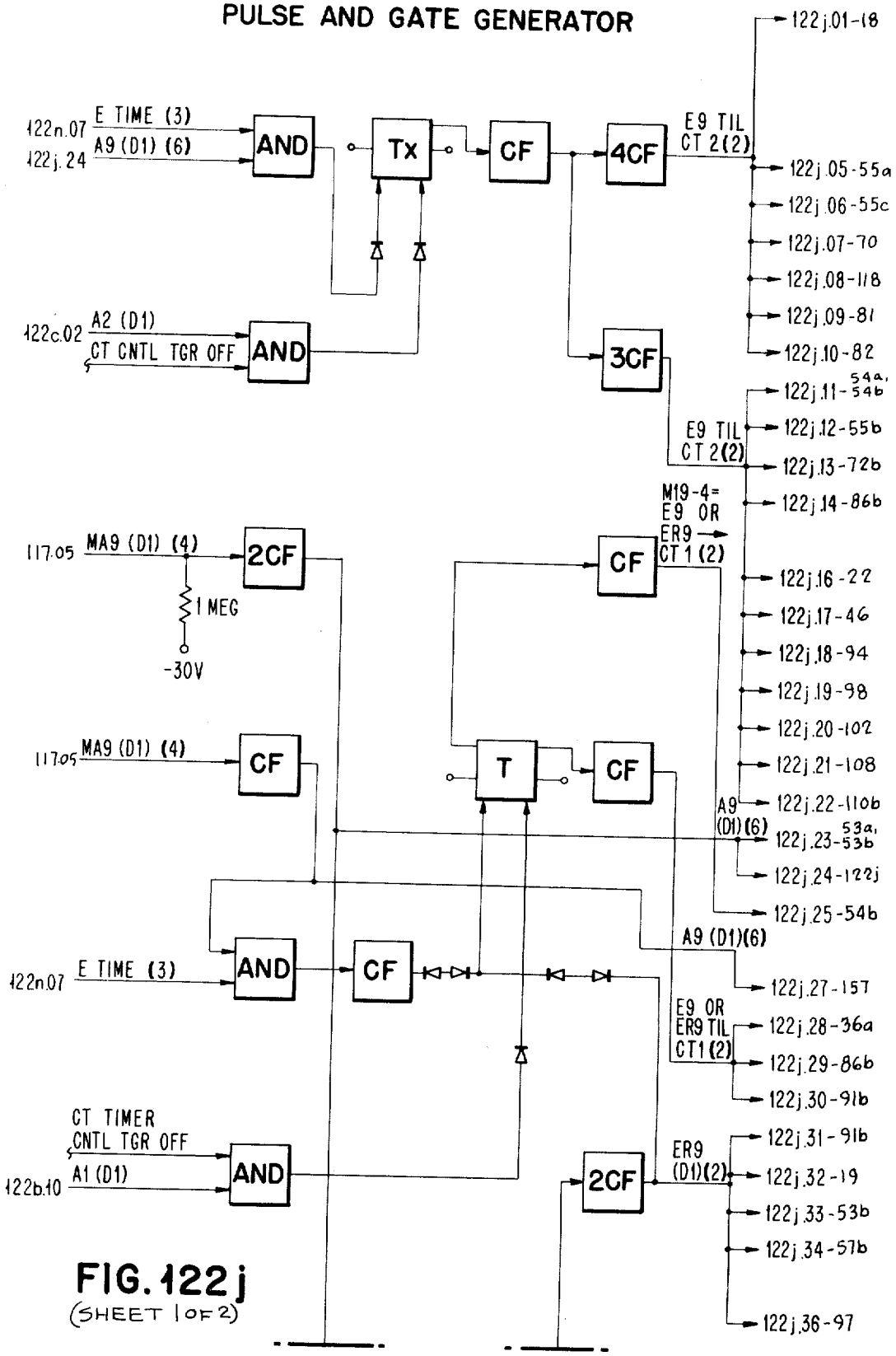


FIG. 122j
(SHEET 1 OF 2)

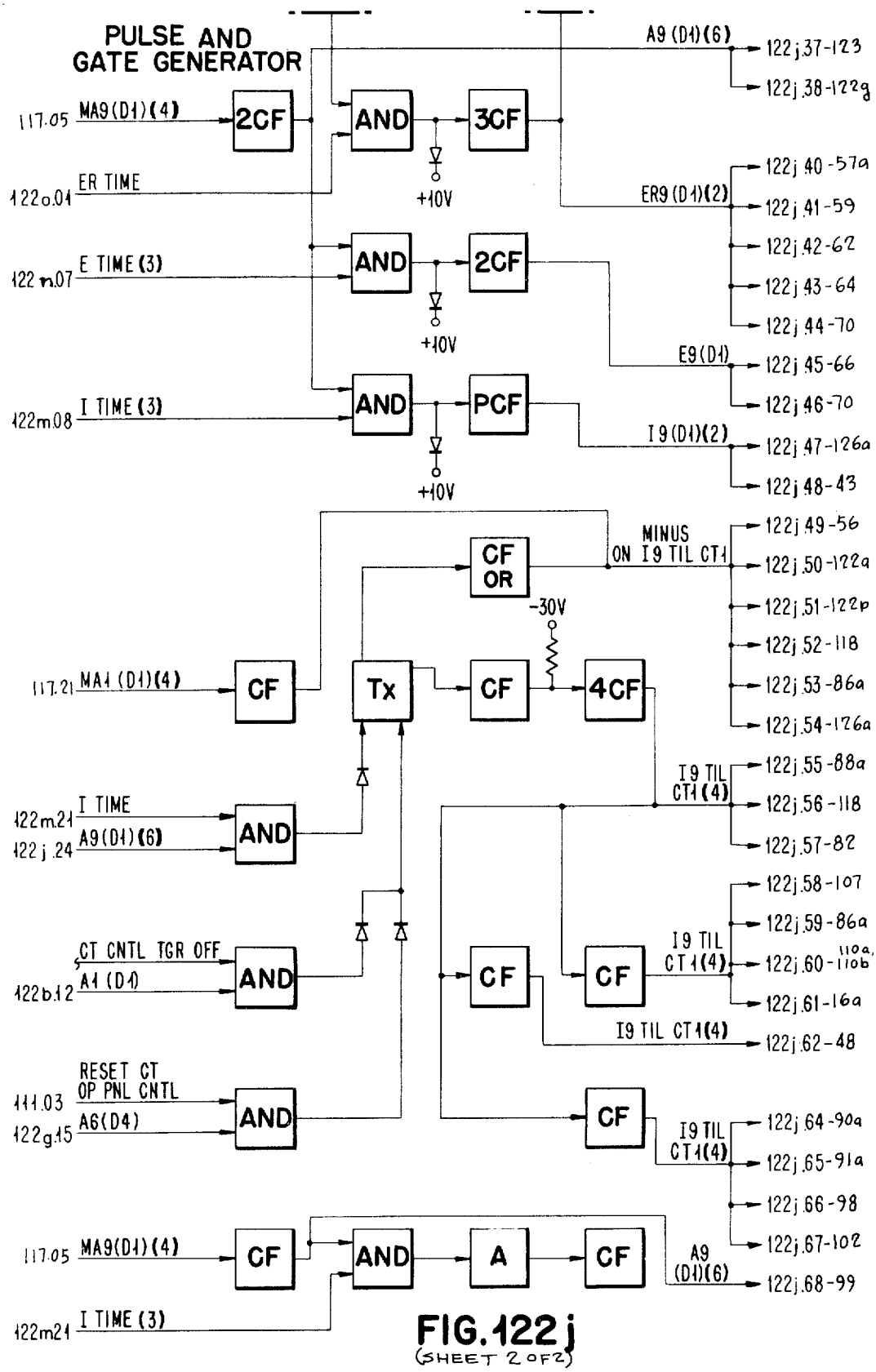


FIG. 122j
(SHEET 2 OF 2)

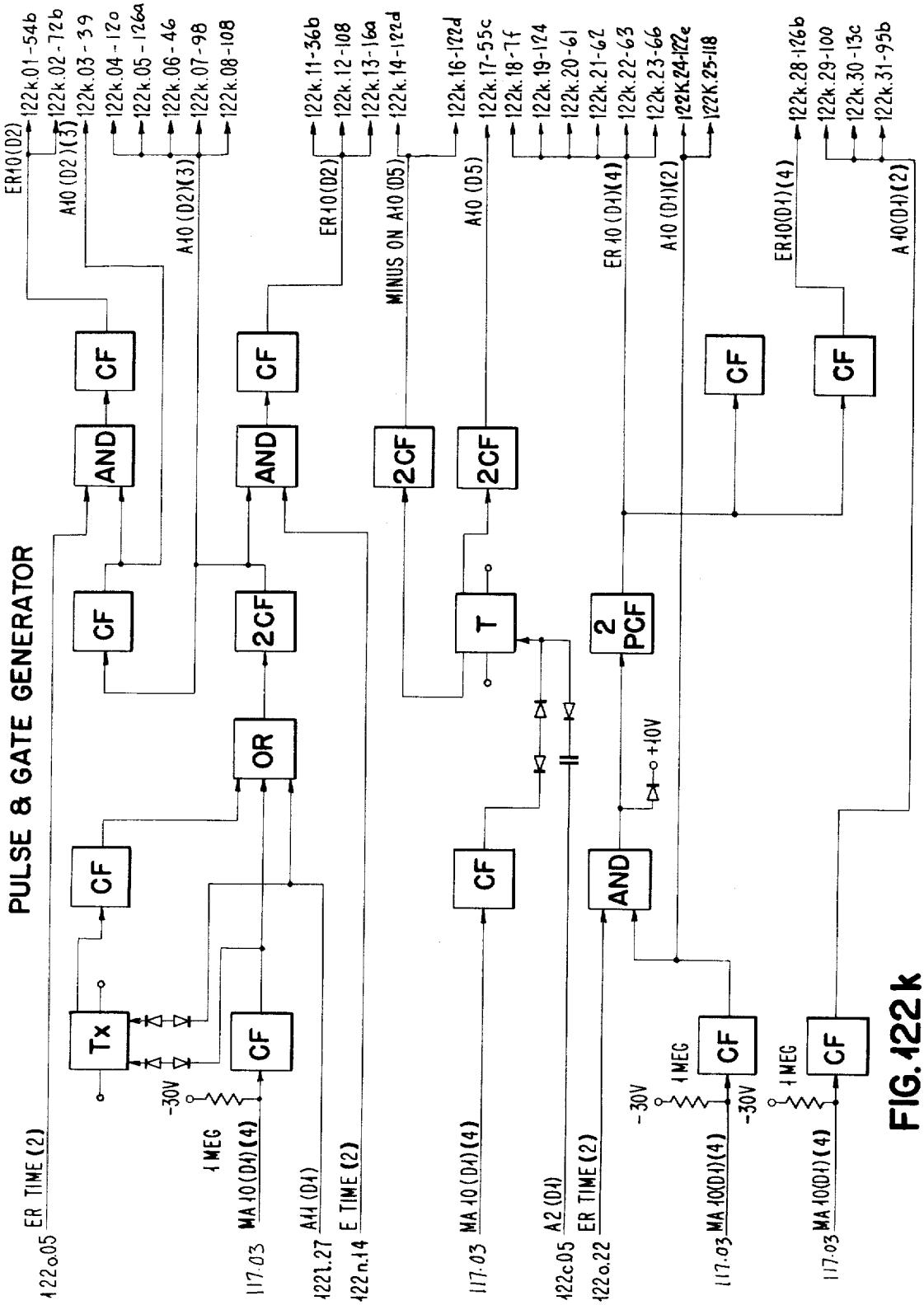

PULSE & GATE GENERATOR
ER TIME (2)
122o.05
Tx
CF
-30V
1 MEG
MA 10 (D4) (4)
117.03
CF
OR
A11 (D1)
1221.27
E TIME (2)
122n.14
CF
AND
CF
A10 (D2) (3)
ER10 (D2)
122k.01-54b
122k.02-72b
122k.03-39
122k.04-120
122k.05-126a
122k.06-46
122k.07-98
122k.08-108
2CF
AND
CF
A10 (D2) (3)
ER10 (D2)
122k.11-36b
122k.12-108
122k.13-16a
2CF
MINUS ON A10 (D5)
122k.14-122d
122k.16-122d
T
CF
A10 (D5)
122k.17-55c
122k.18-71f
122k.19-124
122k.20-61
122k.21-62
122k.22-63
122k.23-66
122k.24-122e
122K.25-118
MA 10 (D4) (4)
117.03
A2 (D4)
122c.05
ER TIME (2)
122o.22
2 PCF
+10V
AND
ER 10 (D1) (4)
A10 (D1) (2)
CF
CF
-30V
1 MEG
MA 10 (D1) (4)
117.03
-30V
1 MEG
MA 10 (D1) (4)
117.03
CF
CF
ER10 (D1) (4)
A10 (D1) (2)
122k.28-126b
122k.29-100
122k.30-13c
122k.31-95b

FIG. 122k

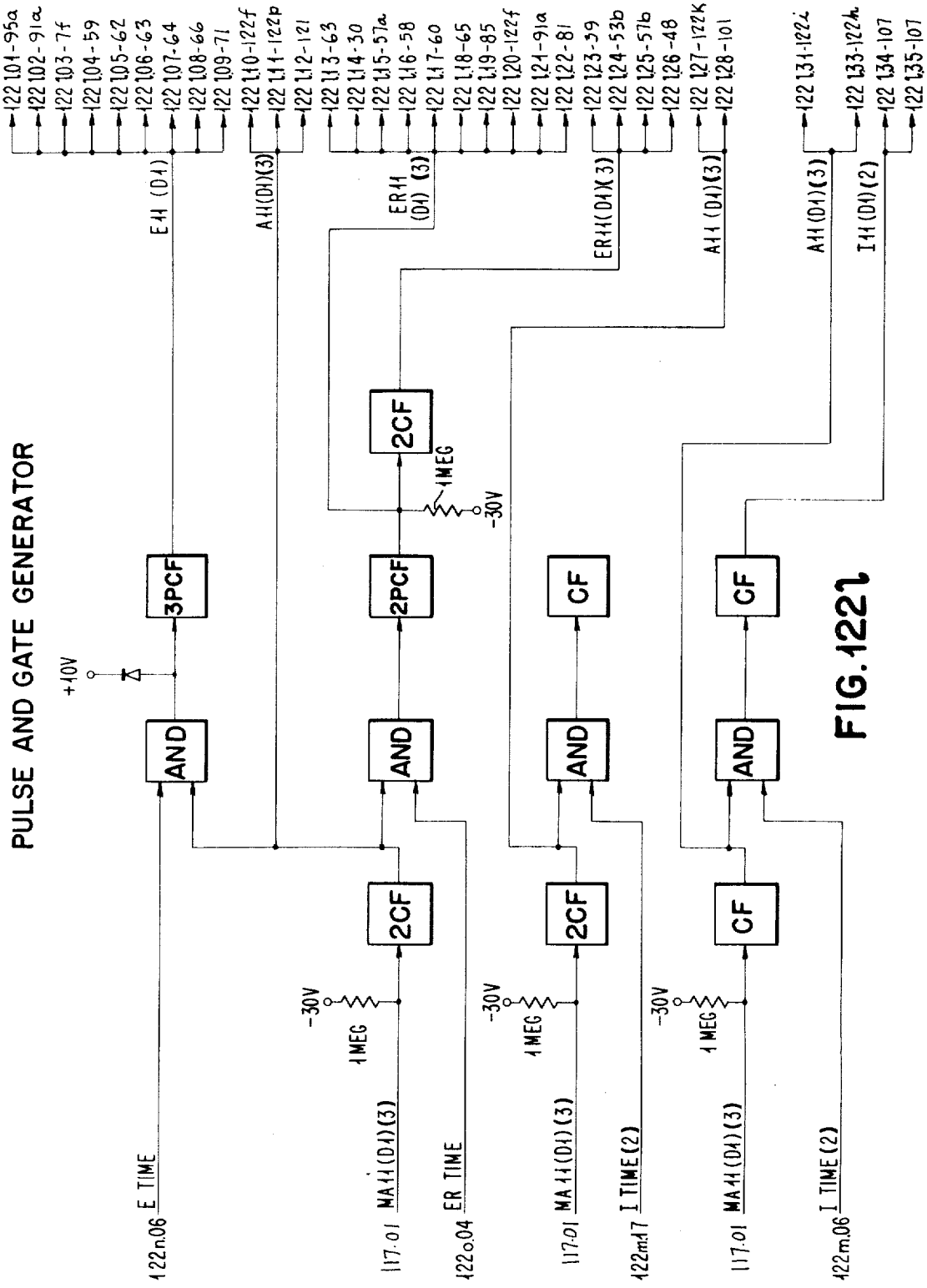

PULSE AND GATE GENERATOR
122 101-95a
122 102-91a
122 103-7f
122 104-59
122 105-62
122 106-63
122 107-64
122 108-66
122 109-71
122 110-122f
122 111-122p
122 112-121
122 113-63
122 114-30
122 115-57a
122 116-58
122 117-60
122 118-65
122 119-85
122 120-122f
122 121-91a
122 122-81
122 123-39
122 124-53b
122 125-57b
122 126-48
122 127-122K
122 128-101
122 131-122i
122 133-122h
122 134-107
122 135-107
E11 (D1)
A11(D1)(3)
ER11 (D1) (3)
A11 (D1)(3)
ER11(D1)(3)
A11 (D1)(3)
I11(D1)(2)
+10V
3PCF
2PCF
2CF
CF
AND
-30V
1MEG
122n.06 E TIME
117.01 MA11(D1)(3)
122o.04 ER TIME
117.01 MA11(D1)(3)
122m.17 I TIME(2)
117.01 MA11(D1)(3)
122m.06 I TIME(2)

FIG. 1221

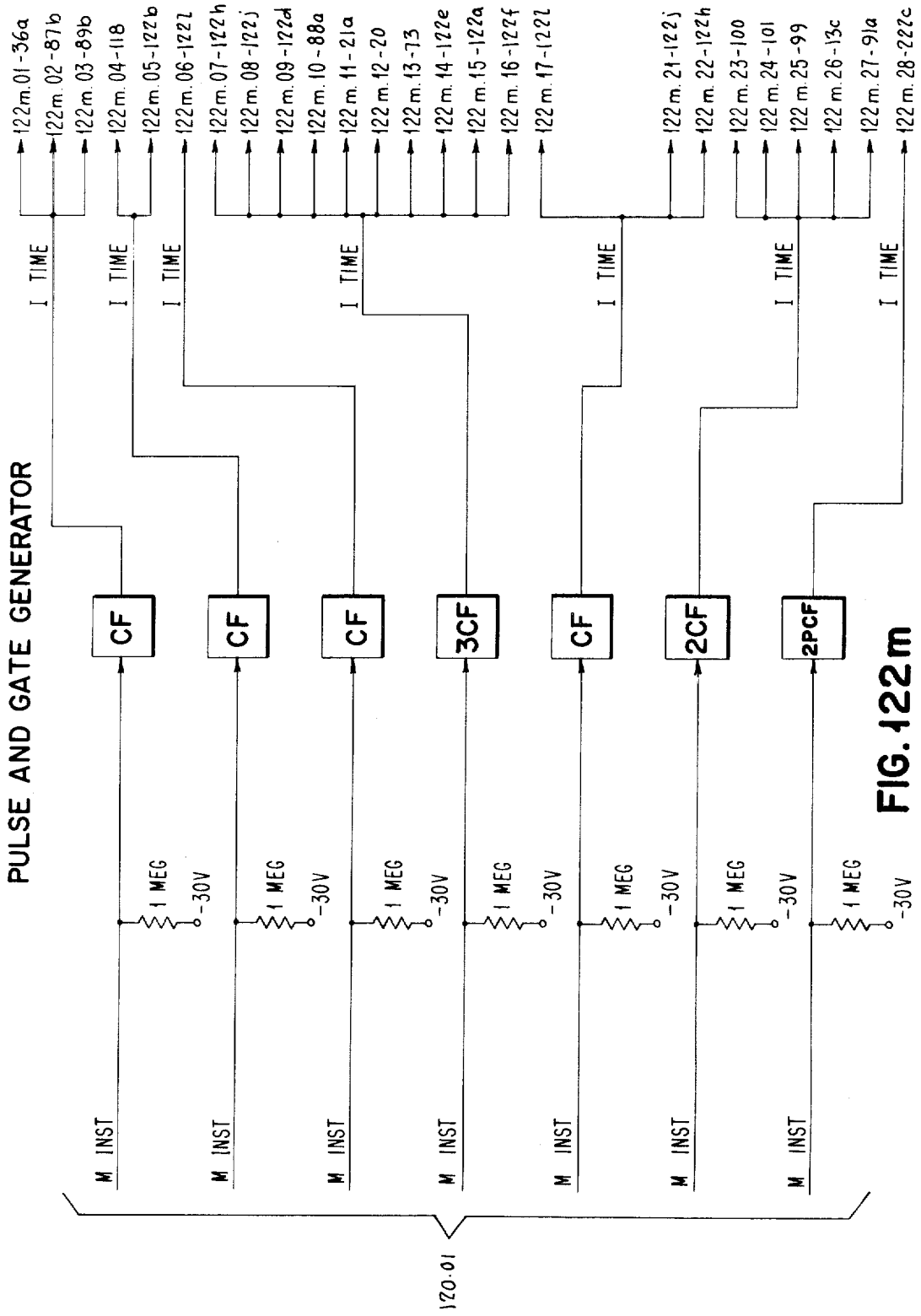

PULSE AND GATE GENERATOR
122m.01-36a
122m.02-87b
122m.03-89b
122m.04-118
122m.05-122b
122m.06-122l
122m.07-122h
122m.08-122j
122m.09-122d
122m.10-88a
122m.11-21a
122m.12-20
122m.13-73
122m.14-122e
122m.15-122a
122m.16-122f
122m.17-122l
122m.21-122j
122m.22-122h
122m.23-100
122m.24-101
122m.25-99
122m.26-13c
122m.27-91a
122m.28-222c
I TIME
CF
3CF
2CF
2PCF
1 MEG
-30V
M INST
120.01

FIG. 122m

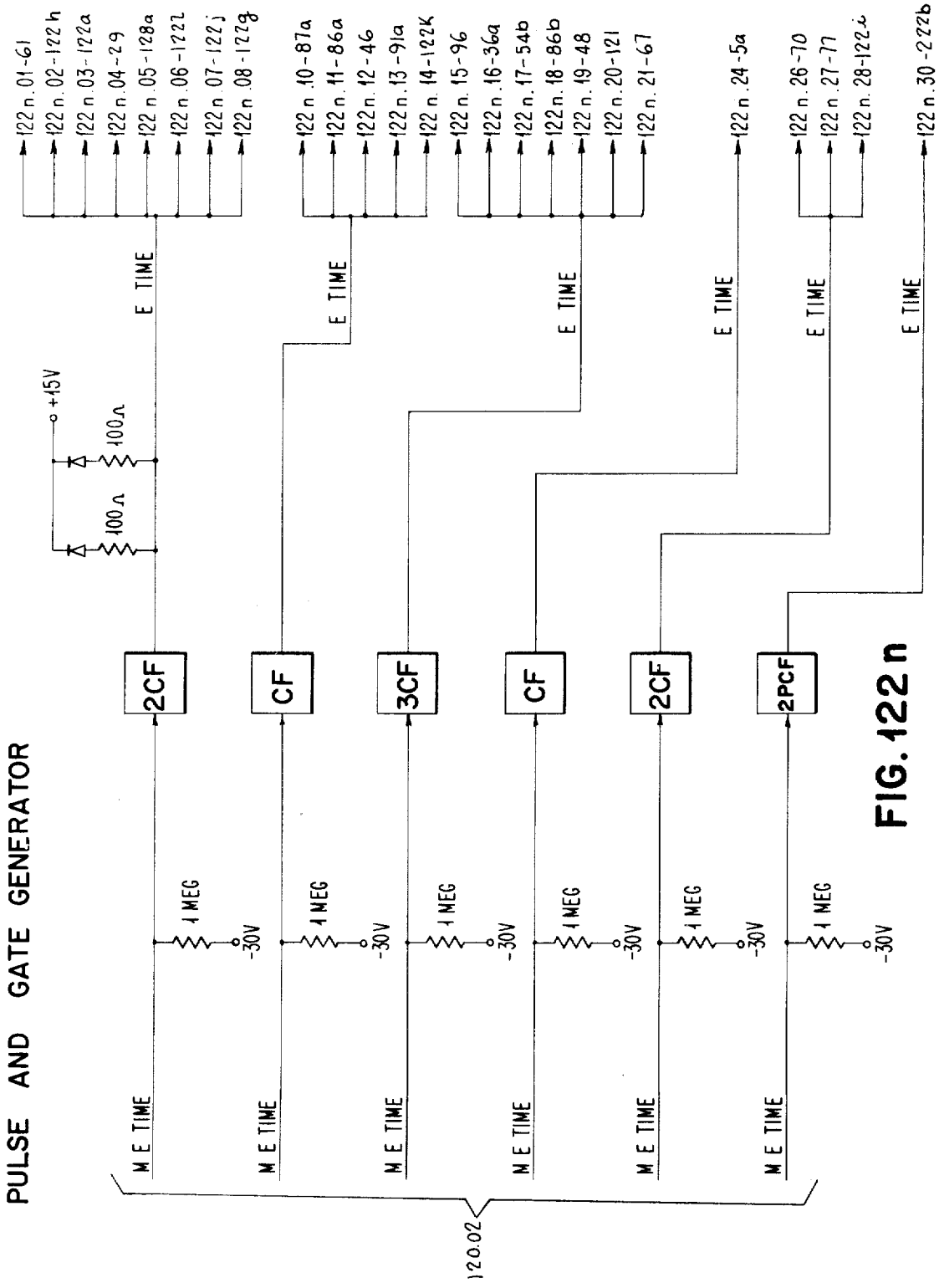
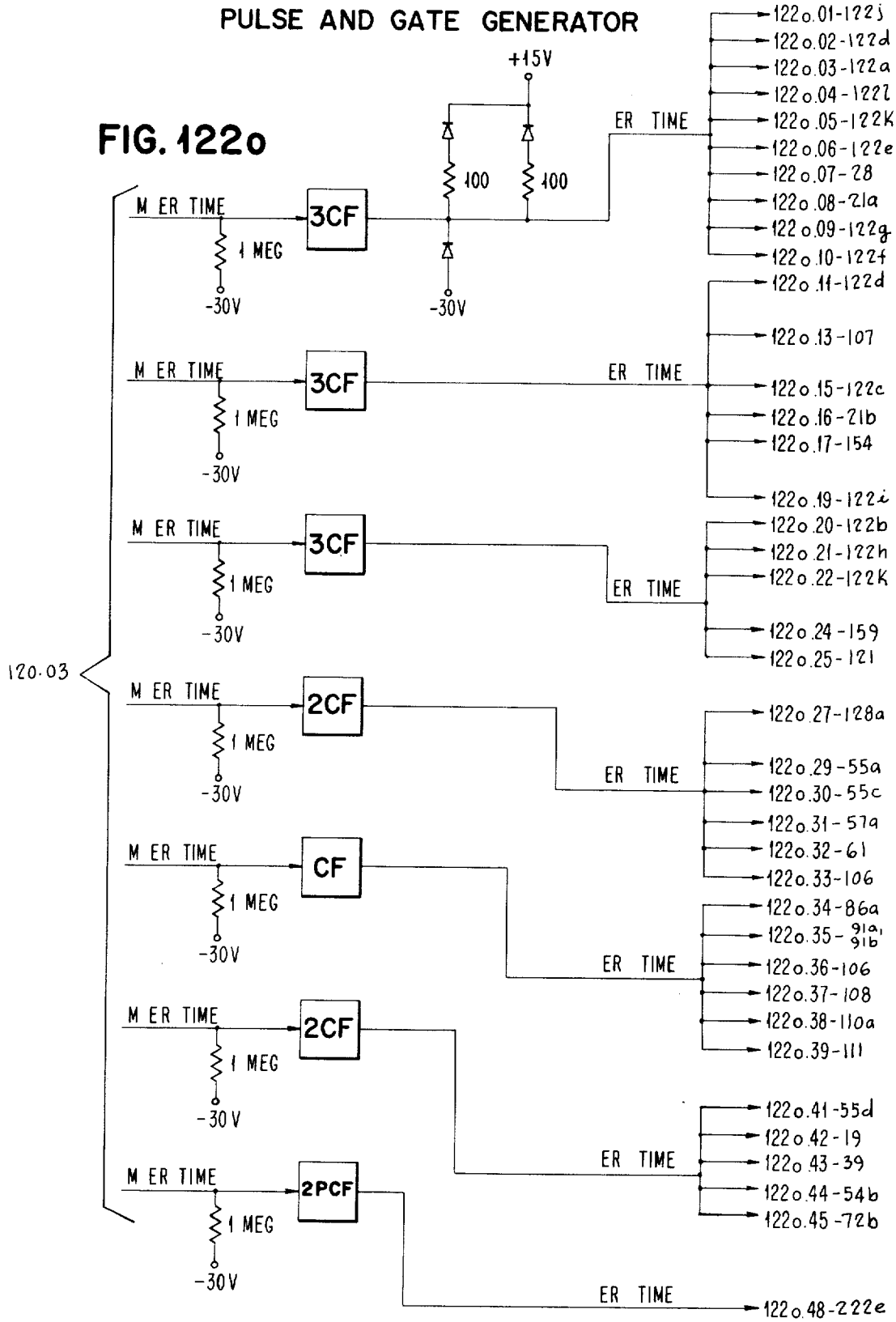

PULSE AND GATE GENERATOR
120.02
M E TIME
1 MEG
-30V
2CF
CF
3CF
CF
2CF
2PCF
E TIME
+15V
100Ω
100Ω
122 n .01-61
122 n .02-122 h
122 n .03-122a
122 n .04-29
122 n .05-128a
122 n .06-122l
122 n .07-122 j
122 n .08-122g
122 n .10-87a
122 n .11-86a
122 n .12-46
122 n .13-91a
122 n .14-122K
122 n .15-96
122 n .16-36a
122 n .17-54b
122 n .18-86b
122 n .19-48
122 n .20-121
122 n .21-67
122 n .24-5a
122 n .26-70
122 n .27-77
122 n .28-122 i
122 n .30-222b

FIG. 122 n

PULSE AND GATE GENERATOR

FIG. 122o



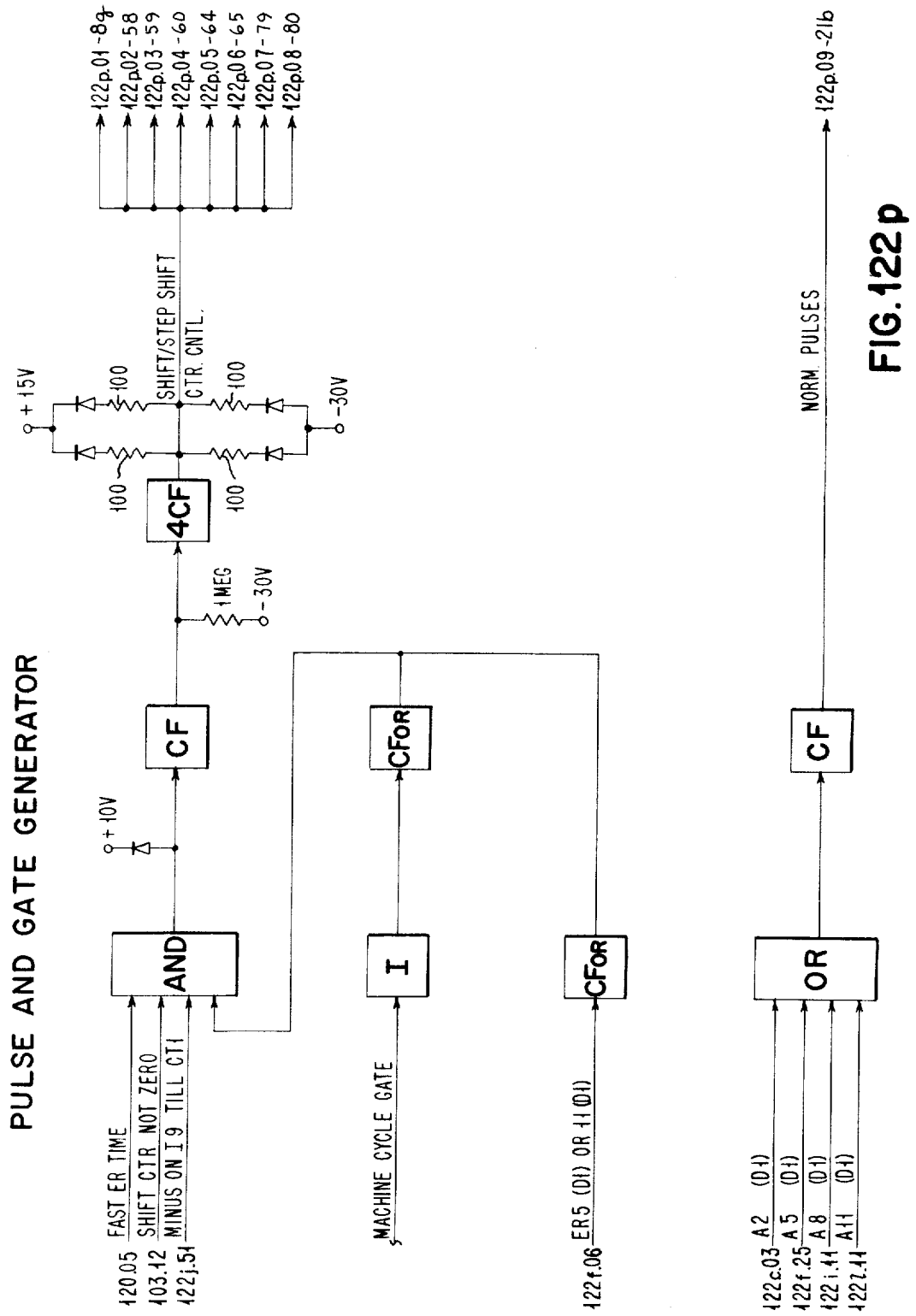

PULSE AND GATE GENERATOR
120.05 FAST ER TIME
103.12 SHIFT CTR NOT ZERO
122j.54 MINUS ON I 9 TILL CTI
AND
+10V
CF
1 MEG
-30V
4CF
100
100
100
100
+15V
-30V
SHIFT/STEP SHIFT CTR. CNTL.
122p.01-8
122p.02-58
122p.03-59
122p.04-60
122p.05-64
122p.06-65
122p.07-79
122p.08-80
MACHINE CYCLE GATE
I
CFOR
122r.06 ER5 (D1) OR 11 (D1)
CFOR
122c.03 A2 (D1)
122f.25 A5 (D1)
122i.11 A8 (D1)
122l.11 A11 (D1)
OR
CF
NORM PULSES
122p.09-21b

FIG.122p

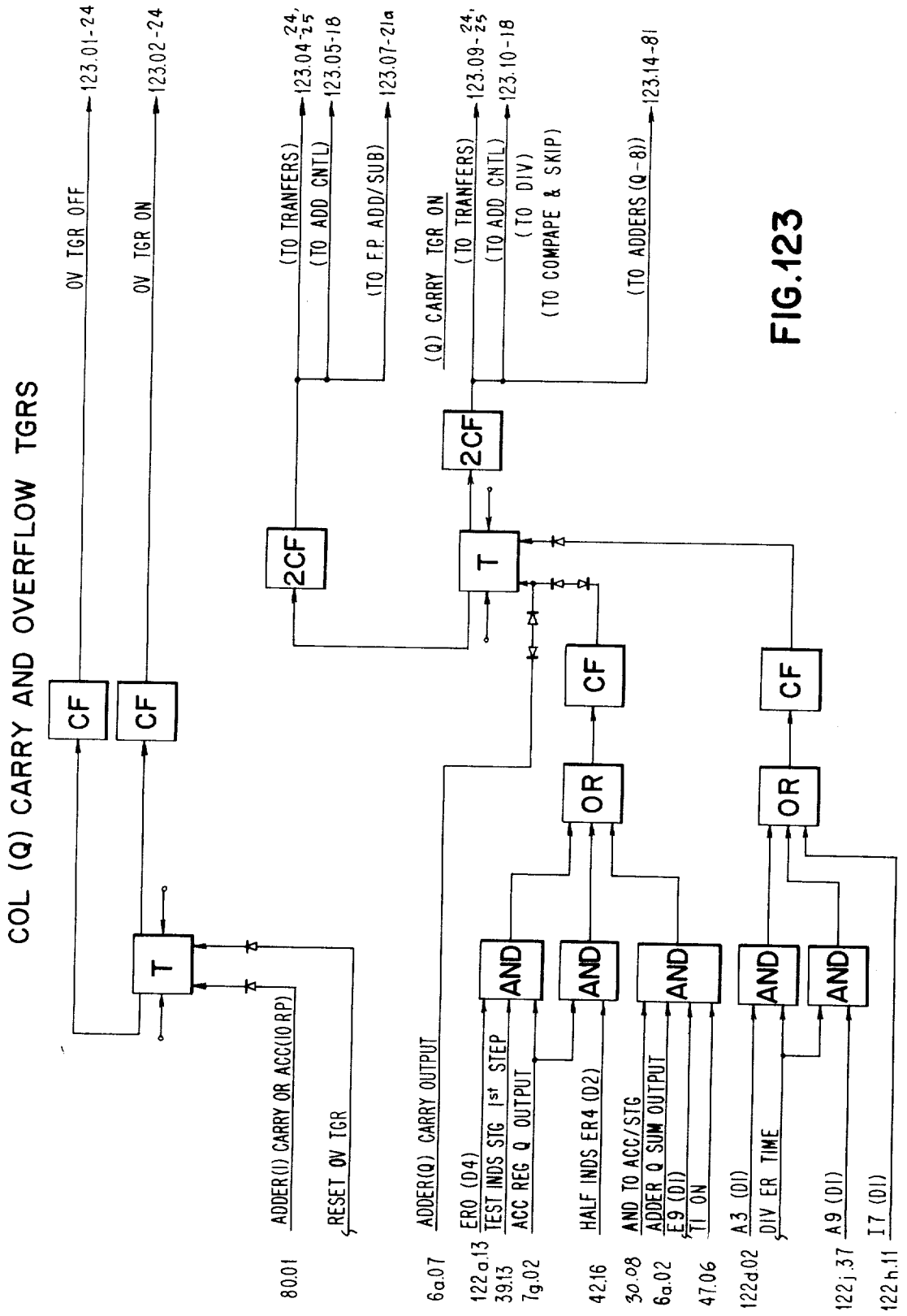
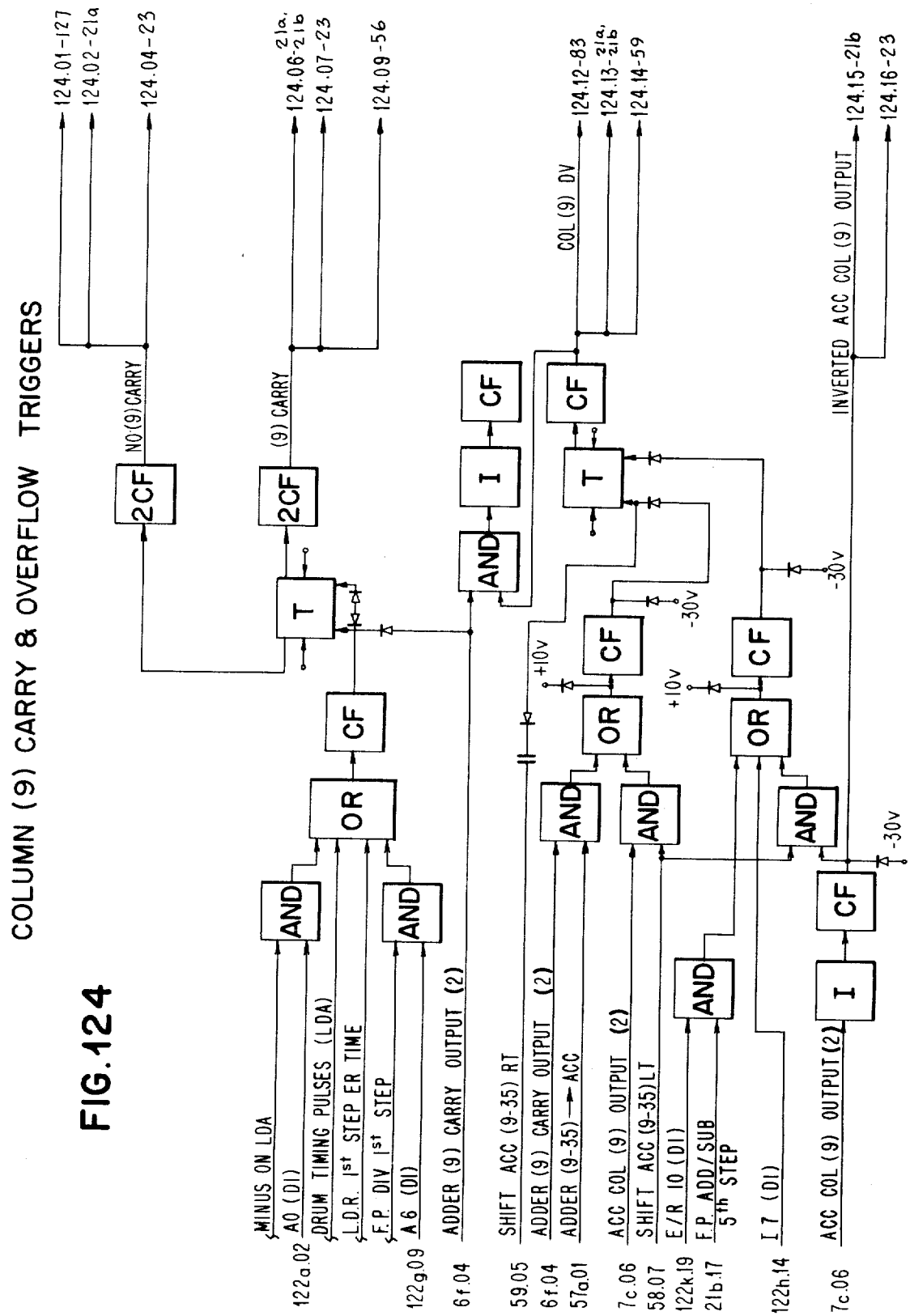

COL (Q) CARRY AND OVERFLOW TGRS
OV TGR OFF
123.01-24
OV TGR ON
123.02-24
(TO TRANFERS)
123.04-24, 25
(TO ADD CNTL)
123.05-18
(TO F.P. ADD/SUB)
123.07-21a
(Q) CARRY TGR ON
(TO TRANFERS)
123.09-24, 25
(TO ADD CNTL)
123.10-18
(TO DIV)
(TO COMPARE & SKIP)
(TO ADDERS (Q-81))
123.14-81
CF
CF
T
2CF
2CF
T
CF
CF
OR
OR
AND
AND
AND
AND
AND
80.01 ADDER(I) CARRY OR ACC(10 RP)
RESET OV TGR
6a.07 ADDER(Q) CARRY OUTPUT
122a.13 ERO (04)
39.13 TEST INDS STG 1st STEP
7g.02 ACC REG Q OUTPUT
42.16 HALF INDS ER4 (02)
30.08 AND TO ACC/STG
6a.02 ADDER Q SUM OUTPUT
E9 (01)
47.06 TI ON
122d.02 A3 (01)
DIV ER TIME
122j.37 A9 (01)
122h.11 I7 (01)

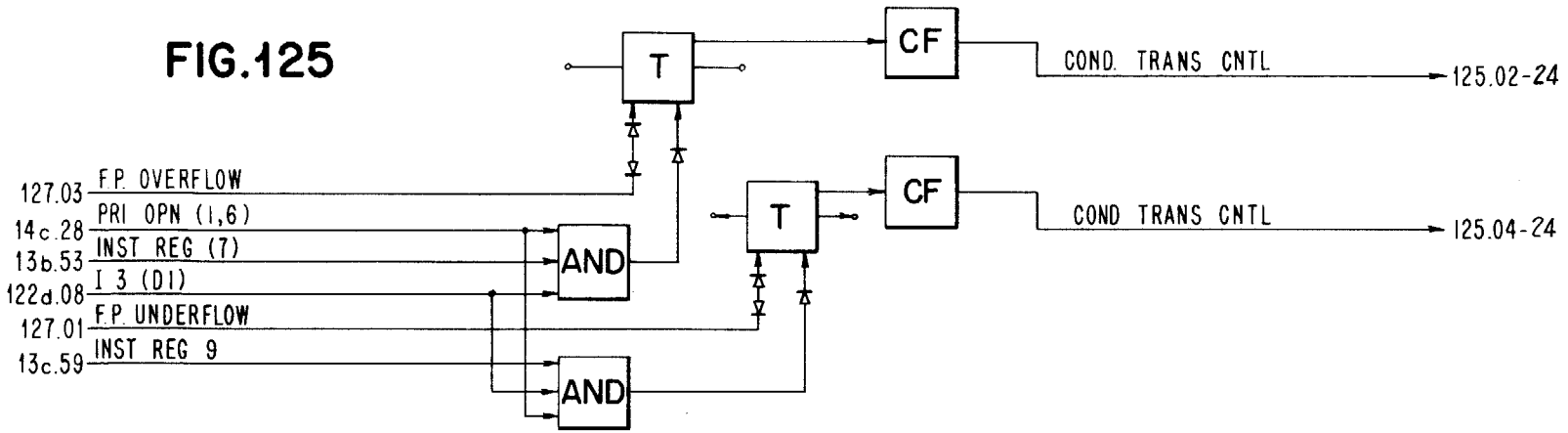
FIG.123

FIG.124

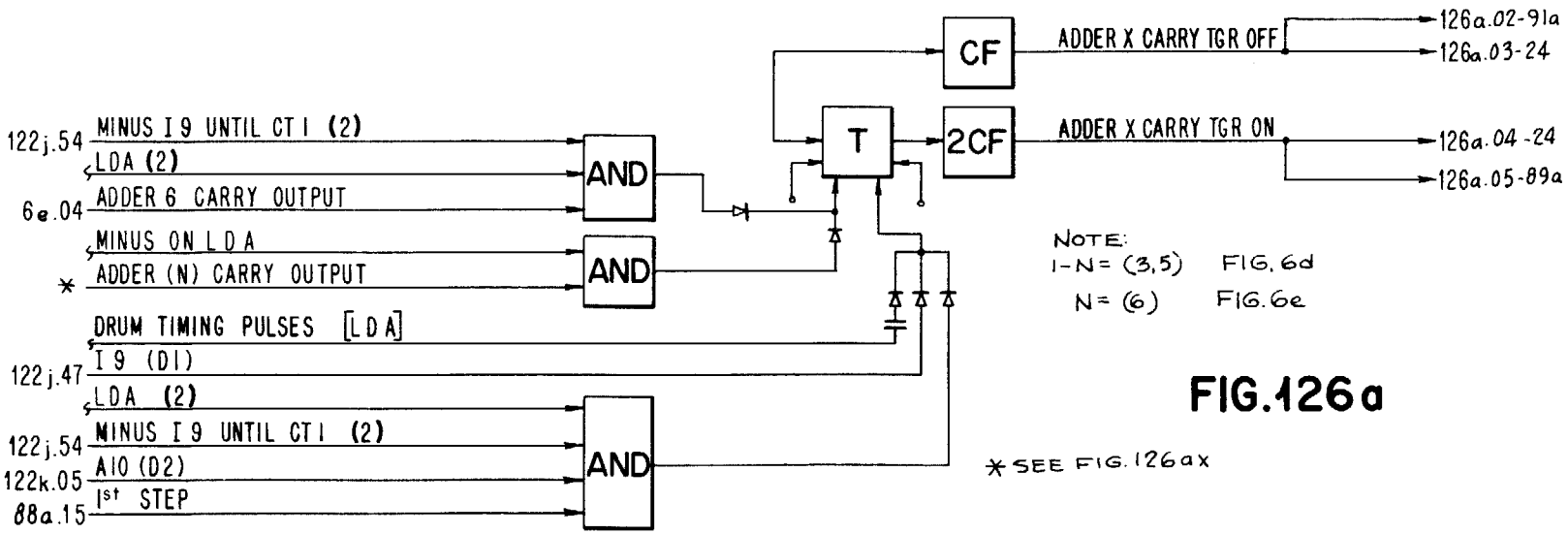

COLUMN (9) CARRY & OVERFLOW TRIGGERS
124.01-127
124.02-21a
124.04-23
124.06-21a, 21b
124.07-23
124.09-56
124.12-83
124.13-21a, 21b
124.14-59
124.15-21b
124.16-23
NO (9) CARRY
(9) CARRY
COL (9) DV
INVERTED ACC COL (9) OUTPUT
2CF
T
I
CF
AND
OR
-30v
+10v
MINUS ON LDA
122a.02 A0 (D1)
DRUM TIMING PULSES (LDA)
L.D.R. 1st STEP ER TIME
F.P. DIV 1st STEP
122g.09 A6 (D1)
6f.04 ADDER (9) CARRY OUTPUT (2)
59.05 SHIFT ACC (9-35) RT
6f.04 ADDER (9) CARRY OUTPUT (2)
57a.01 ADDER (9-35) → ACC
7c.06 ACC COL (9) OUTPUT (2)
58.07 SHIFT ACC (9-35) LT
122k.19 E/R 10 (D1)
21b.17 F.P. ADD/SUB
5th STEP
122h.14 I 7 (D1)
7c.06 ACC COL (9) OUTPUT (2)

F.P. OVERFLOW TGR., F.P. UNDERFLOW TGR.

FIG.125



ADDER X CARRY TRIGGER



NOTE:
I-N = (3,5) FIG. 6d
N = (6) FIG. 6e

FIG.126a

* SEE FIG. 126ax

F P OVERFLOW AND UNDERFLOW DETECTION

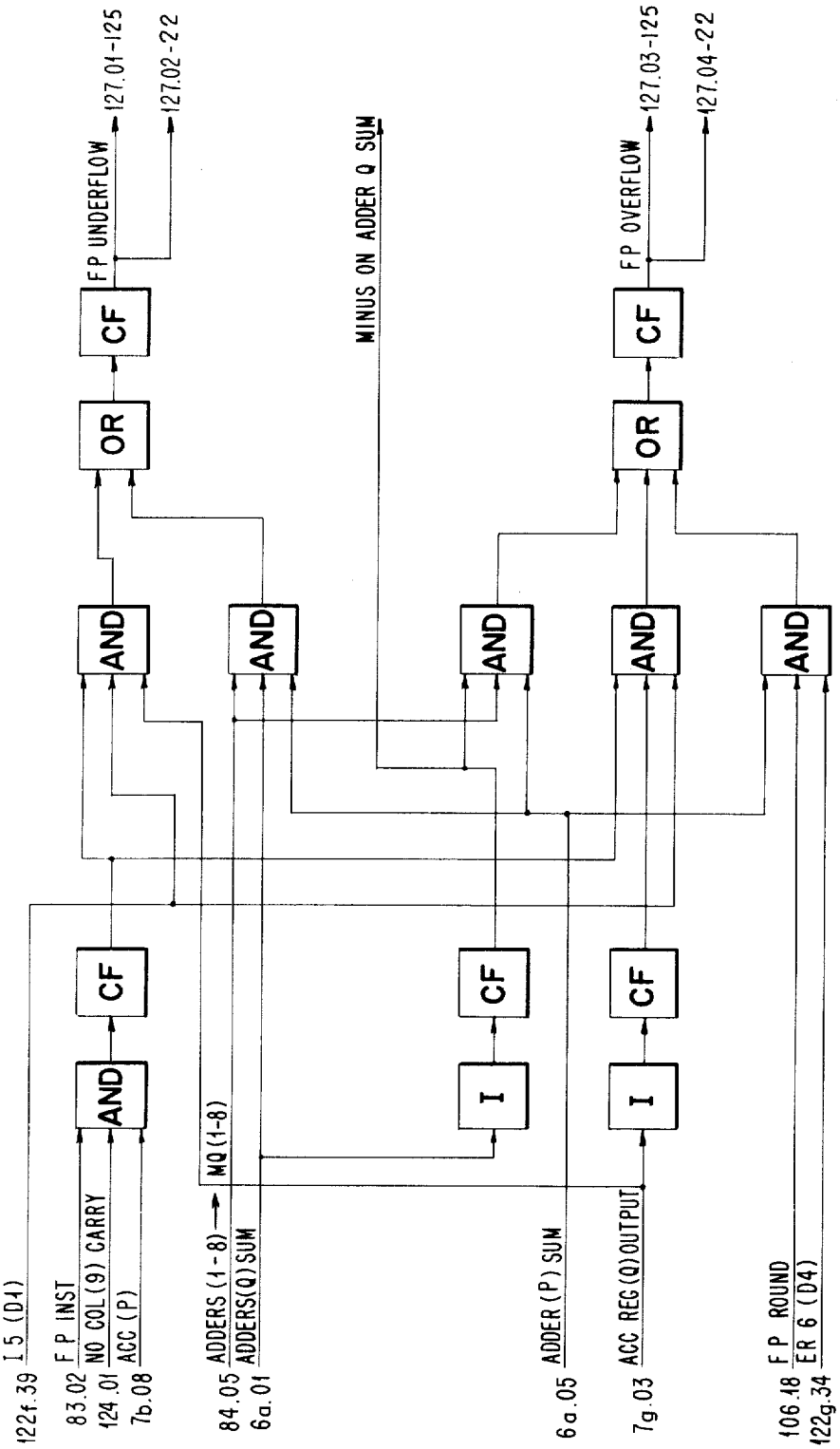
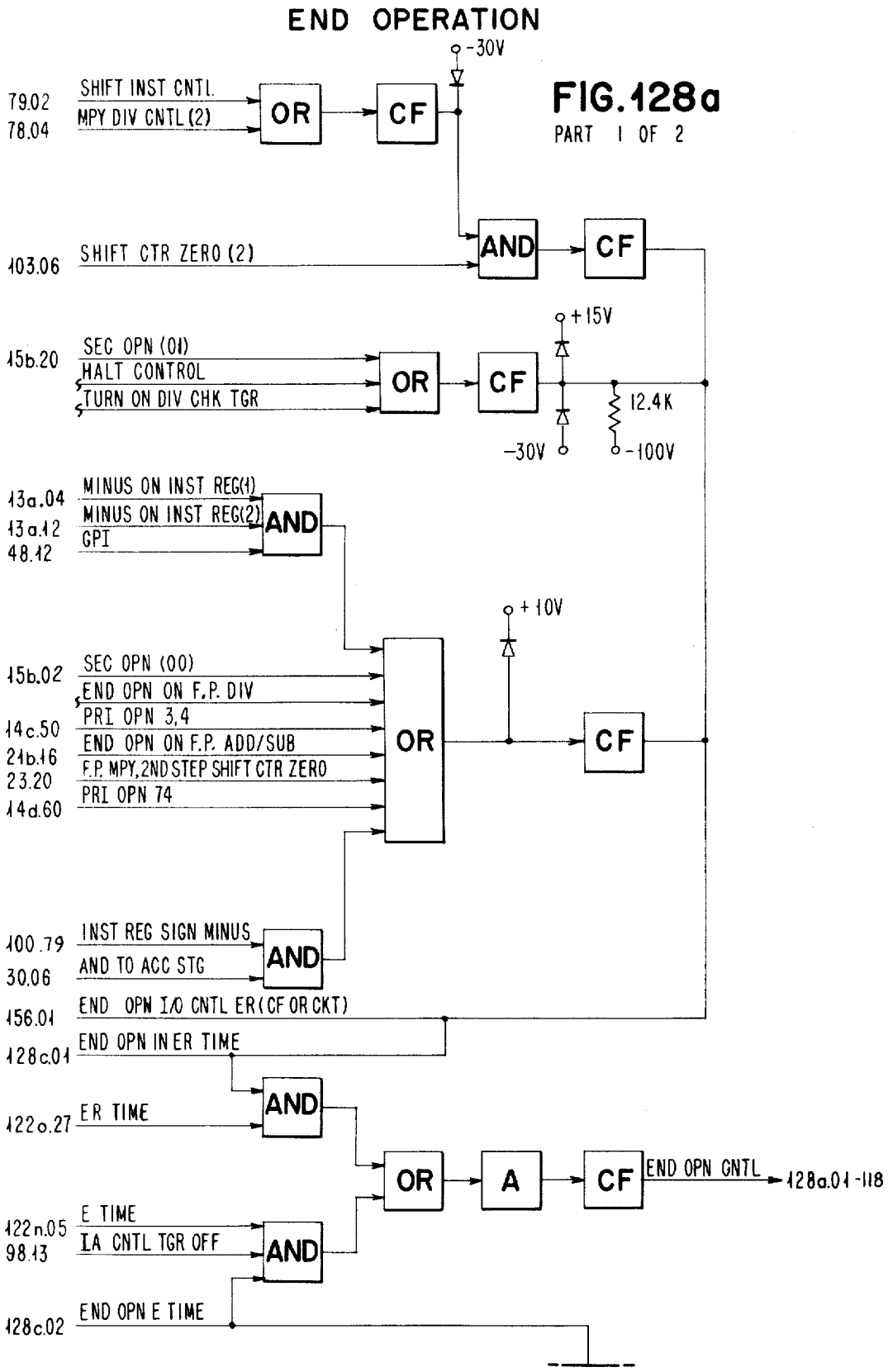


FIG. 127


END OPERATION
-30V
79.02
78.04
SHIFT INST CNTL.
MPY DIV CNTL (2)
OR
CF
FIG. 128a
PART 1 OF 2
103.06
SHIFT CTR ZERO (2)
AND
CF
+15V
15b.20
SEC OPN (01)
HALT CONTROL
TURN ON DIV CHK TGR
OR
CF
12.4K
-30V
-100V
13a.04
13a.12
48.12
MINUS ON INST REG(1)
MINUS ON INST REG(2)
GPI
AND
+10V
15b.02
14c.50
21b.16
23.20
14d.60
SEC OPN (00)
END OPN ON F.P. DIV
PRI OPN 3,4
END OPN ON F.P. ADD/SUB
F.P. MPY, 2ND STEP SHIFT CTR ZERO
PRI OPN 74
OR
CF
100.79
30.06
INST REG SIGN MINUS
AND TO ACC STG
AND
156.01
END OPN I/O CNTL ER (CF OR CKT)
128c.01
END OPN INTER TIME
122o.27
ER TIME
AND
OR
A
CF
END OPN CNTL
128a.01-118
122n.05
98.13
E TIME
IA CNTL TGR OFF
AND
128c.02
END OPN E TIME

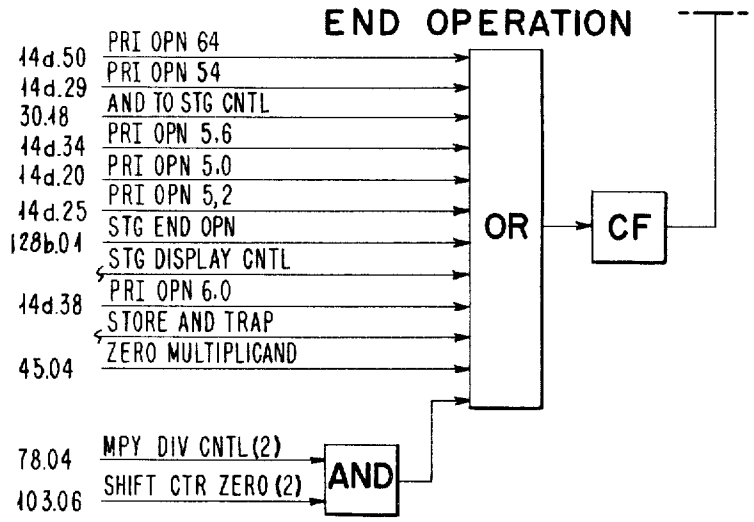


FIG. 128a
PART 2 OF 2

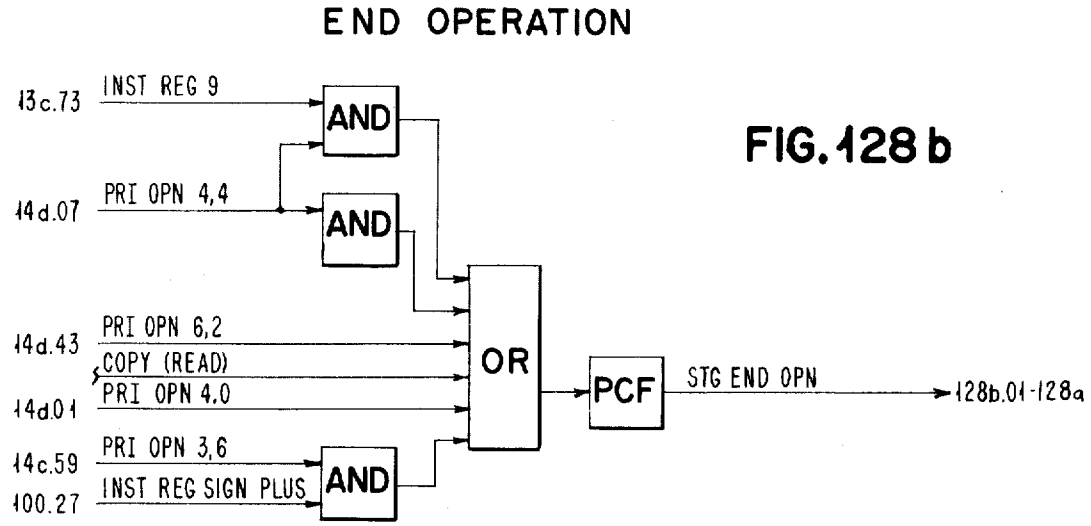


FIG. 128b

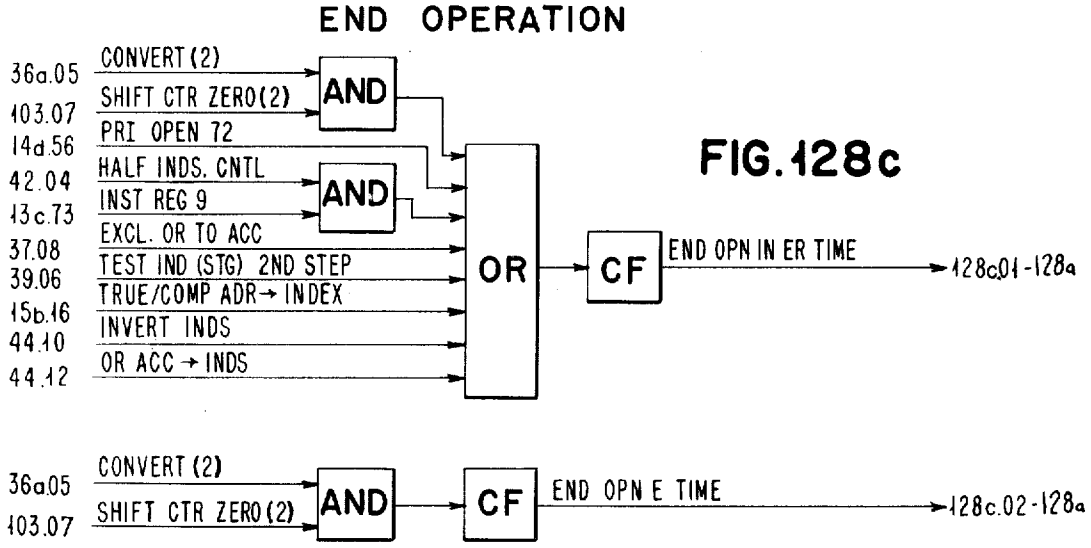


FIG. 128c

FIG. 129a STORAGE ADDRESS REGISTER

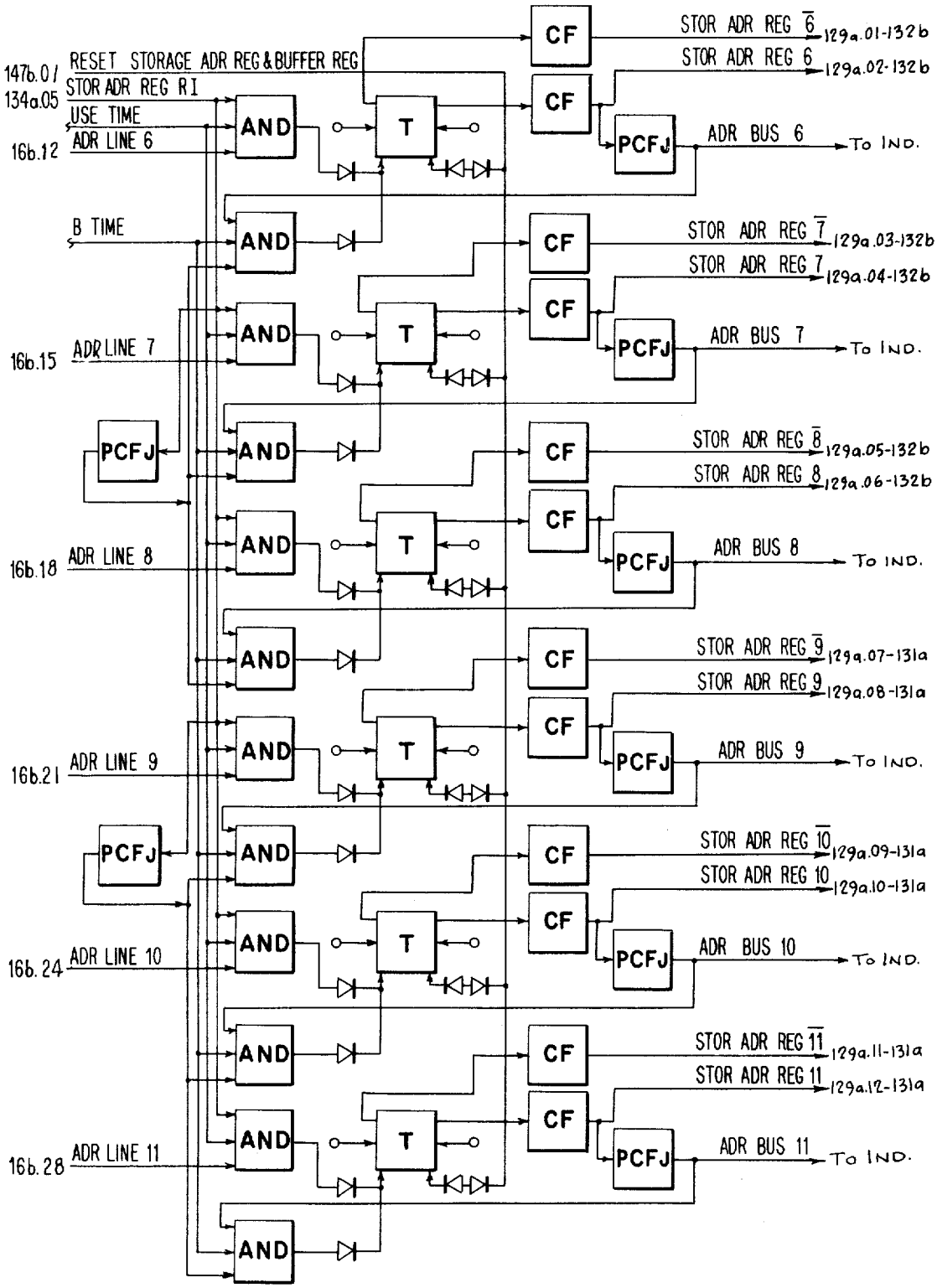
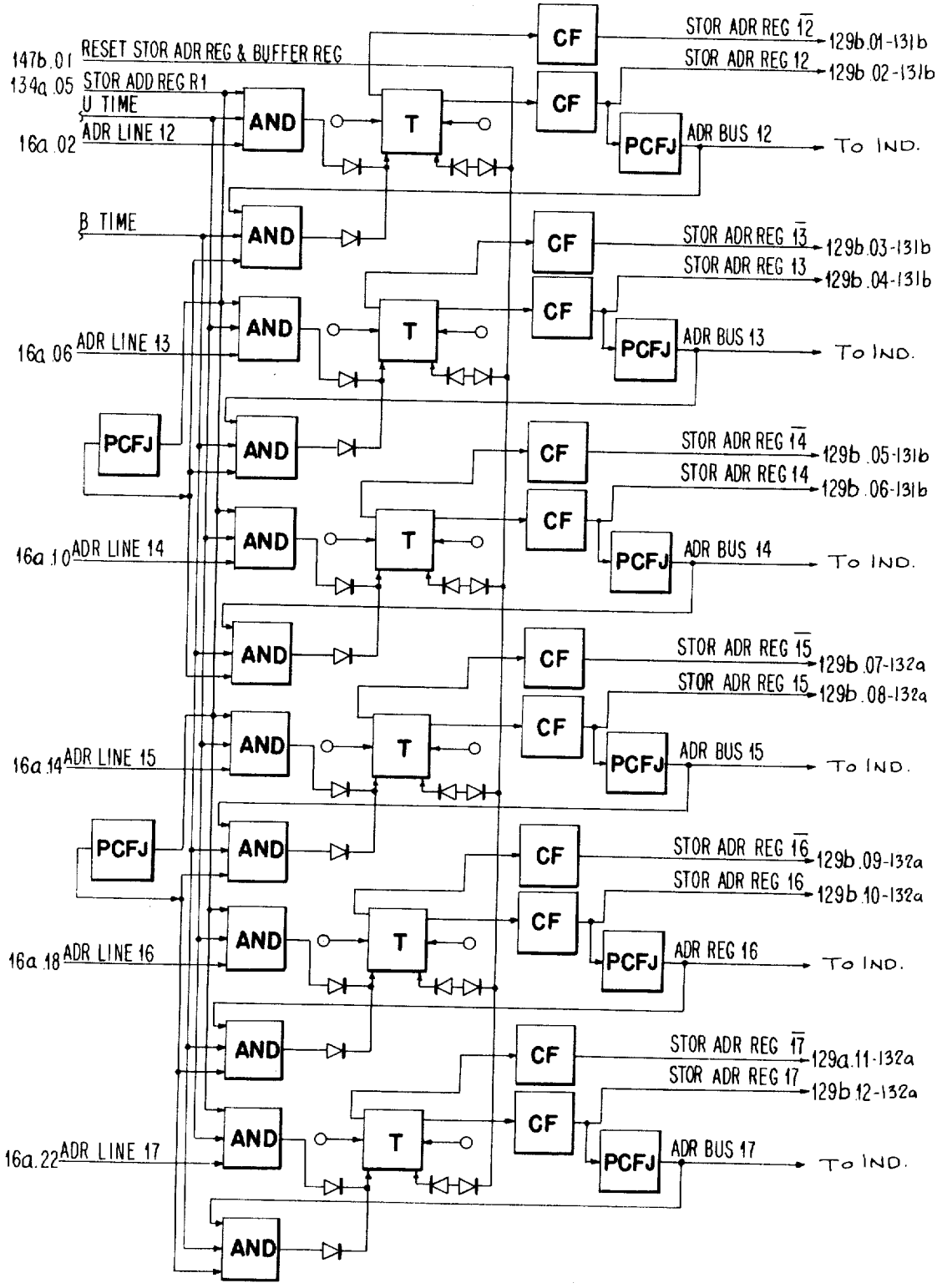


FIG. 129b STORAGE ADDRESS REGISTER



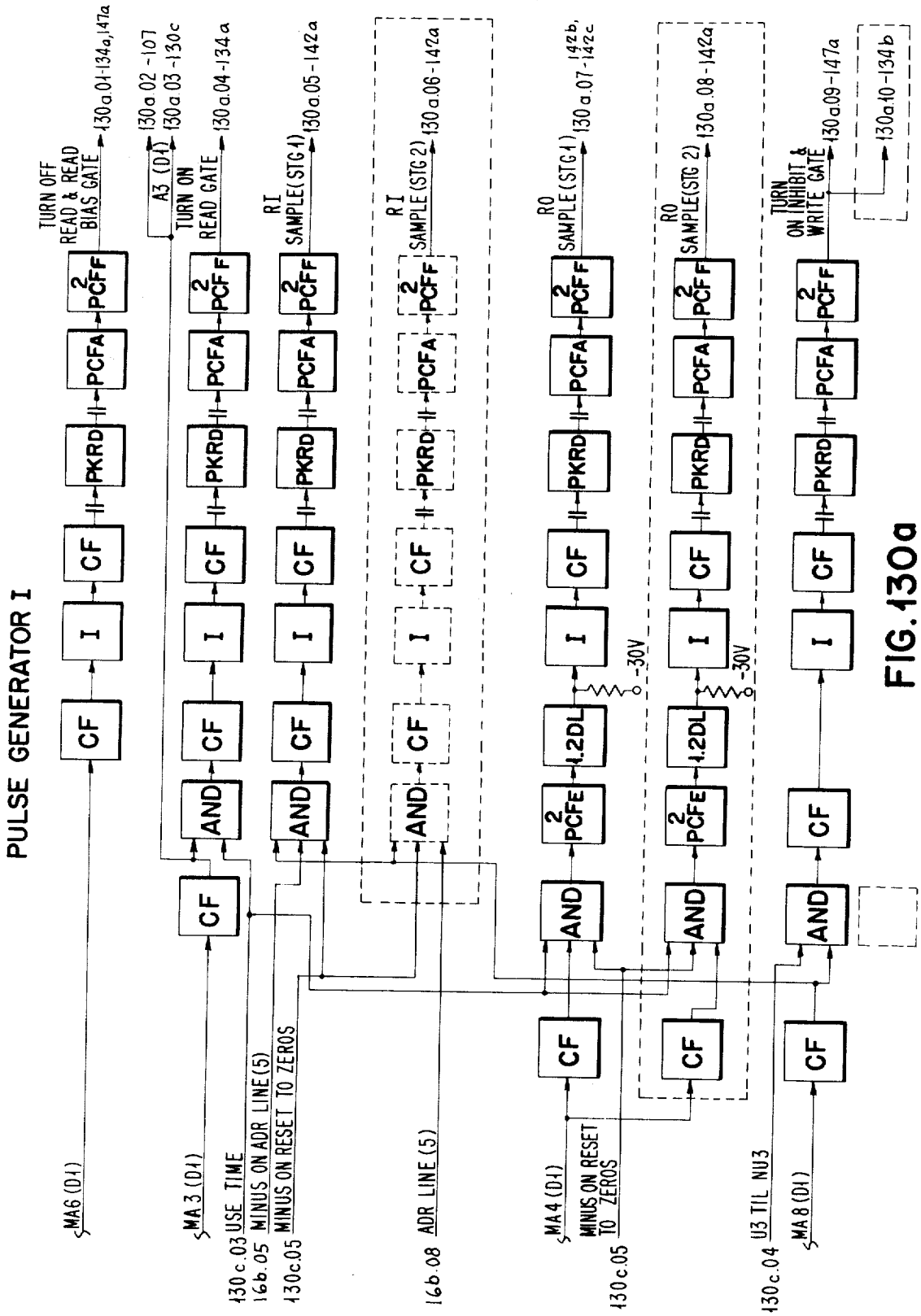

PULSE GENERATOR I
MA6 (D1)
CF
I
CF
PKRD
PCFA
2 PCFF
TURN OFF READ & READ BIAS GATE
130a.01-134a,147a
A3 (D1)
130a.02-107
130a.03-130c
TURN ON READ GATE
130a.04-134a
RI SAMPLE(STG 1)
130a.05-142a
RI SAMPLE(STG 2)
130a.06-142a
RO SAMPLE(STG 1)
130a.07-142b, 142c
RO SAMPLE(STG 2)
130a.08-142a
TURN ON INHIBIT & WRITE GATE
130a.09-147a
130a.10-134b
MA 3 (D1)
USE TIME
130c.03
MINUS ON ADR LINE (5)
16b.05
MINUS ON RESET TO ZEROS
130c.05
ADR LINE (5)
16b.08
MA 4 (D1)
MINUS ON RESET TO ZEROS
130c.05
U3 TIL NU3
130c.04
MA 8 (D1)
AND
2 PCFE
1.2DL
-30V

FIG. 130a

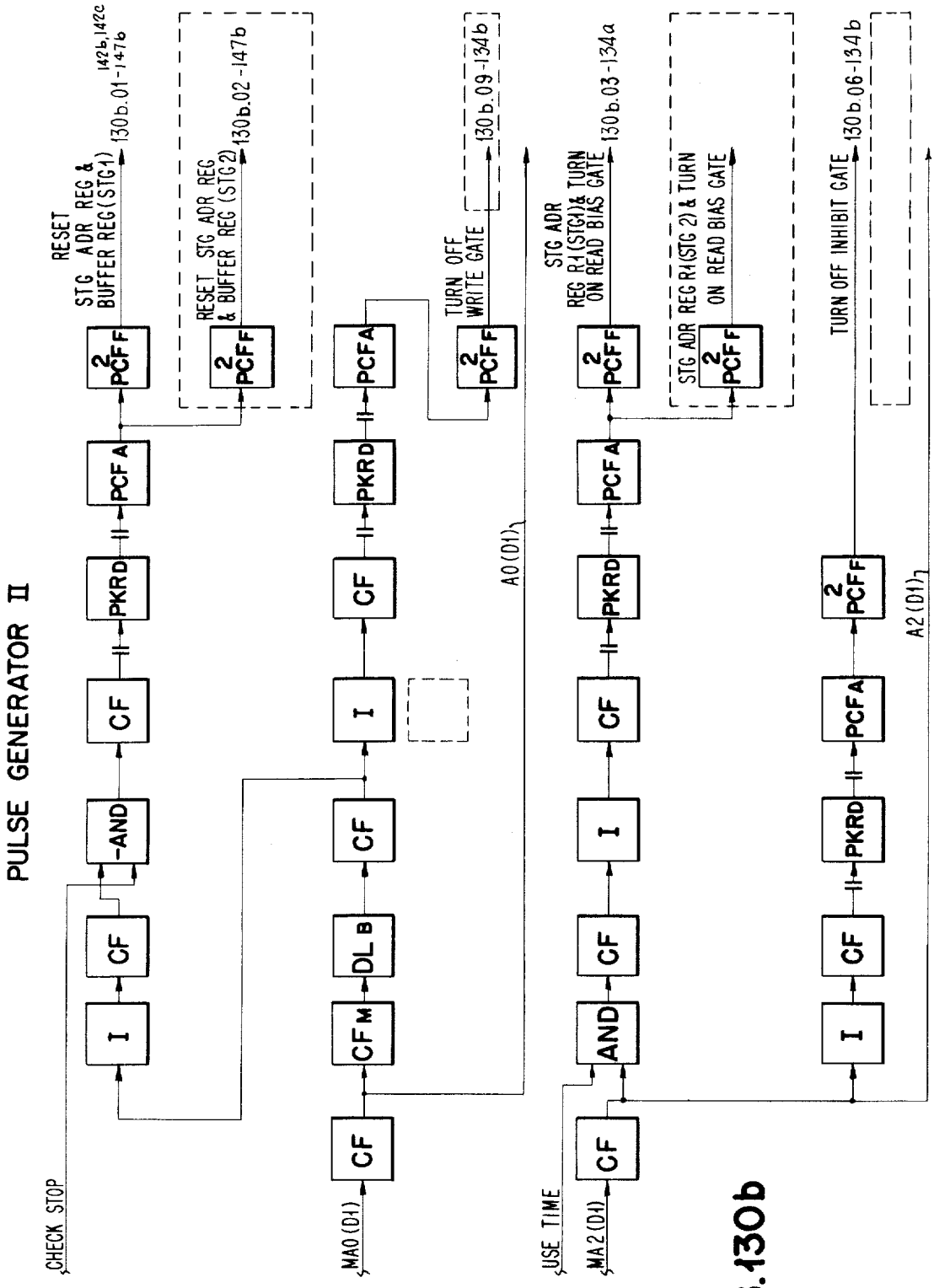

PULSE GENERATOR II
CHECK STOP
I
CF
-AND
CF
PKRD
PCF A
2 PCF F
RESET STG ADR REG & BUFFER REG (STG1)
130b.01-147b
142b,142c
RESET STG ADR REG & BUFFER REG (STG2)
130b.02-147b
MA0(D1)
CF
CF M
DL B
CF
I
CF
PKRD
PCF A
2 PCF F
TURN OFF WRITE GATE
130b.09-134b
A0(D1)
USE TIME
MA2(D1)
CF
AND
CF
I
CF
PKRD
PCF A
2 PCF F
STG ADR REG R1(STG1)& TURN ON READ BIAS GATE
130b.03-134a
STG ADR REG R1(STG 2)& TURN ON READ BIAS GATE
I
CF
PKRD
PCF A
2 PCF F
TURN OFF INHIBIT GATE
130b.06-134b
A2(D1)

FIG. 130b

FIG. 131a

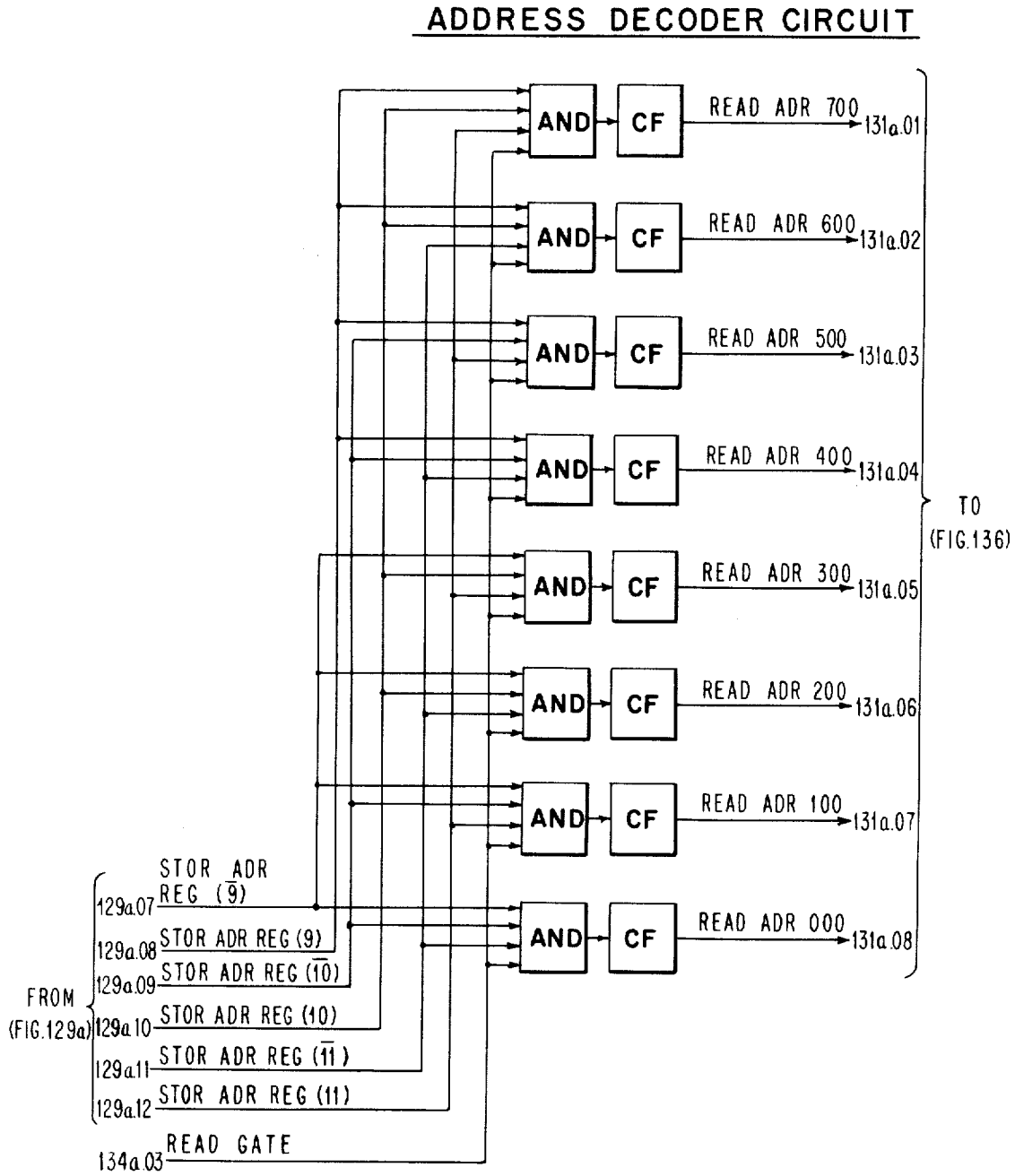

ADDRESS DECODER CIRCUIT
AND
CF
READ ADR 700
131a.01
READ ADR 600
131a.02
READ ADR 500
131a.03
READ ADR 400
131a.04
READ ADR 300
131a.05
READ ADR 200
131a.06
READ ADR 100
131a.07
READ ADR 000
131a.08
TO
(FIG.136)
FROM
(FIG.129a)
129a.07 STOR ADR REG (9)
129a.08 STOR ADR REG (9)
129a.09 STOR ADR REG (10)
129a.10 STOR ADR REG (10)
129a.11 STOR ADR REG (11)
129a.12 STOR ADR REG (11)
134a.03 READ GATE

FIG. 131b

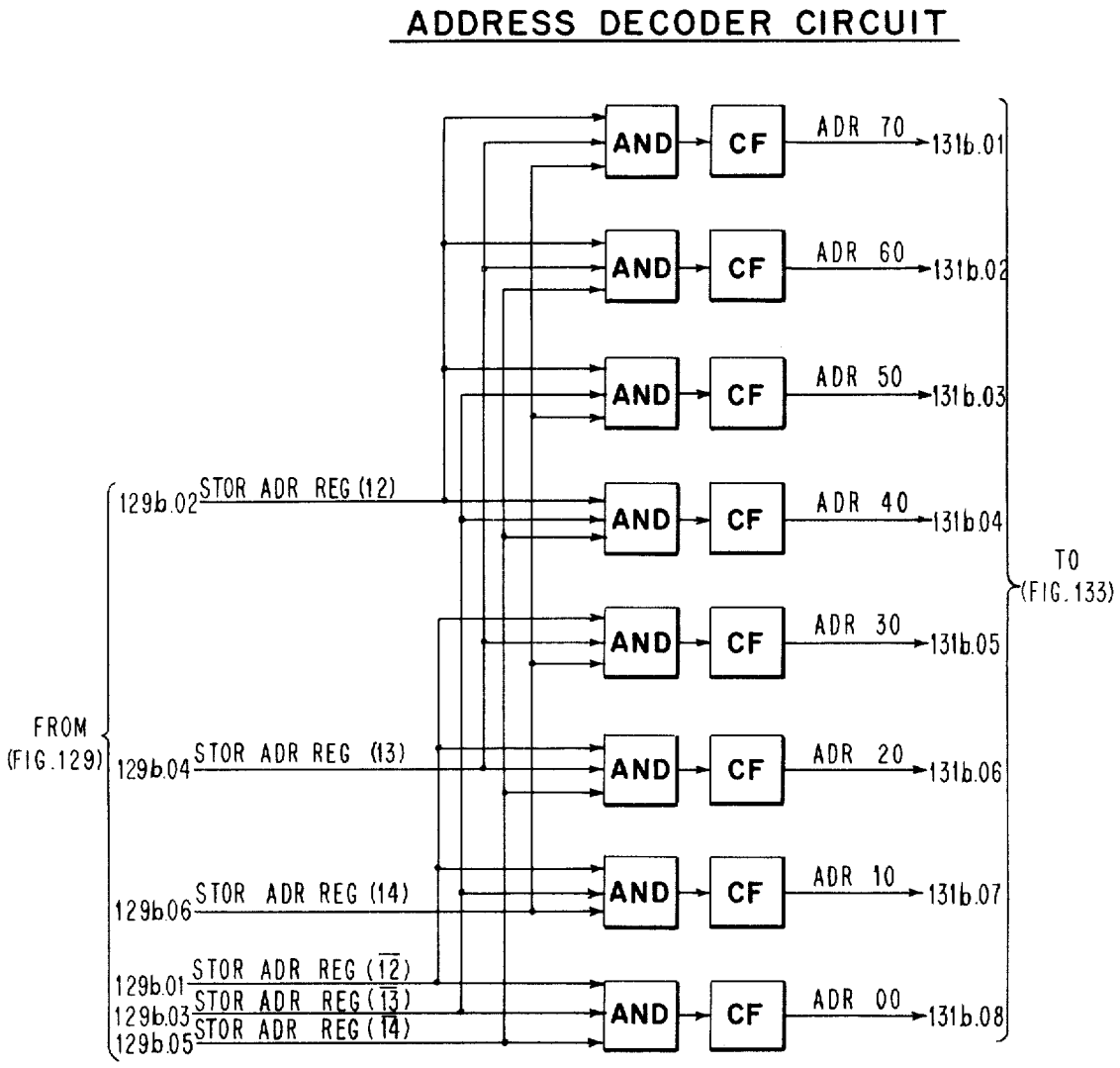

ADDRESS DECODER CIRCUIT
AND
CF
ADR 70
131b.01
ADR 60
131b.02
ADR 50
131b.03
ADR 40
131b.04
ADR 30
131b.05
ADR 20
131b.06
ADR 10
131b.07
ADR 00
131b.08
TO (FIG. 133)
FROM (FIG. 129)
129b.02 STOR ADR REG (12)
129b.04 STOR ADR REG (13)
129b.06 STOR ADR REG (14)
129b.01 STOR ADR REG ($\overline{12}$)
129b.03 STOR ADR REG ($\overline{13}$)
129b.05 STOR ADR REG ($\overline{14}$)

FIG. 132a

ADDRESS DECODER CIRCUIT

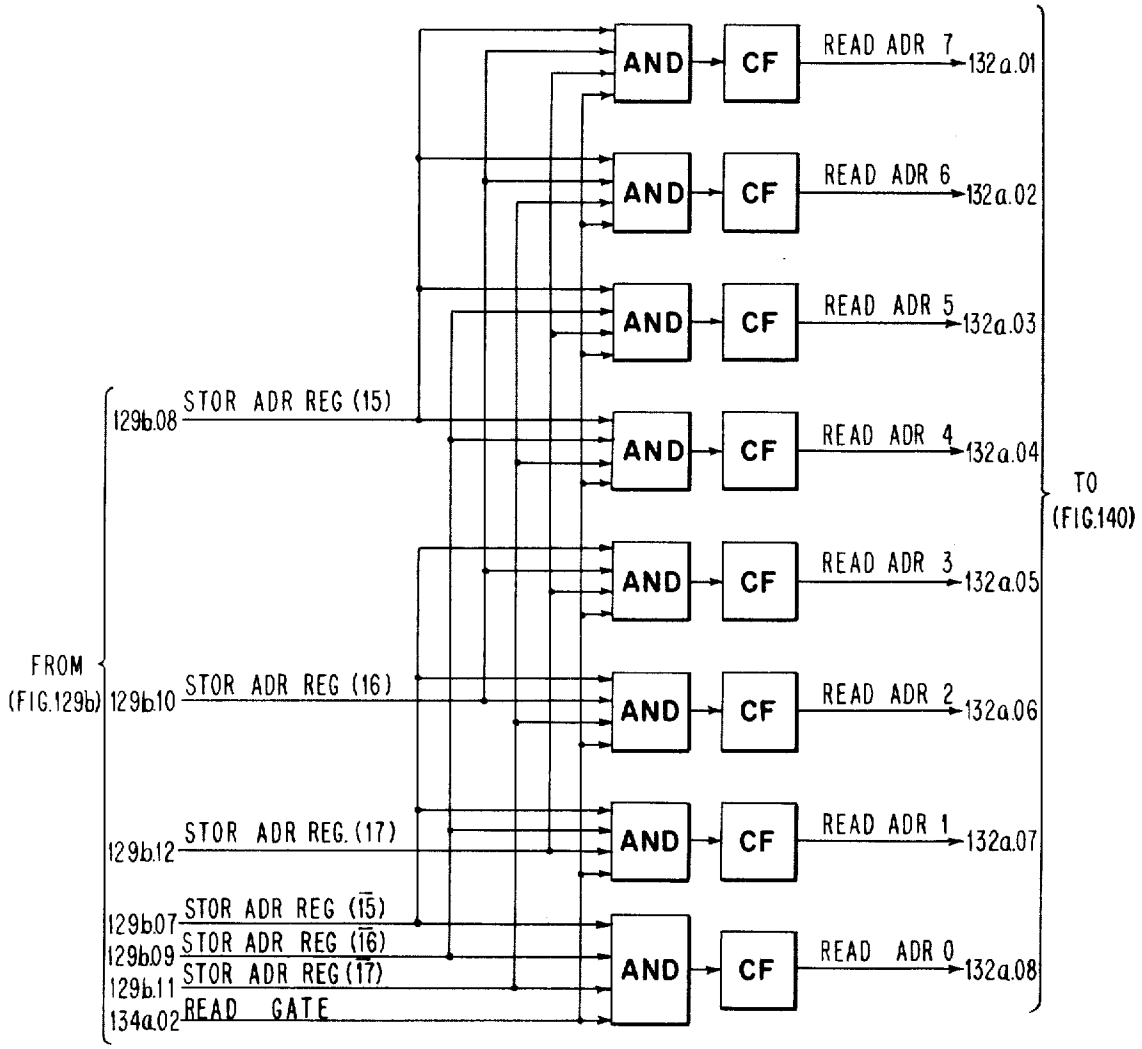
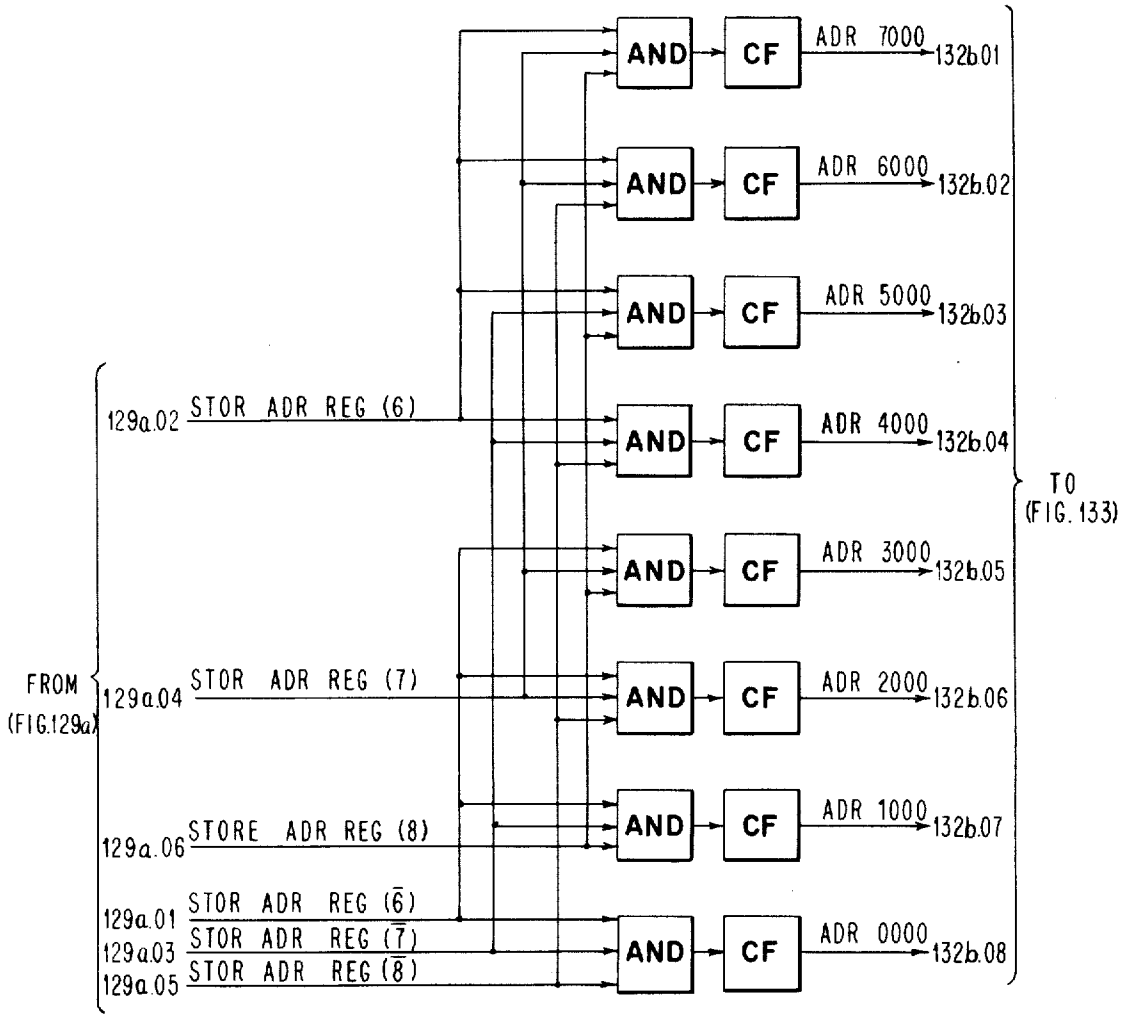


FIG. 132b


ADDRESS DECODER CIRCUIT
AND
CF
ADR 7000
132b.01
ADR 6000
132b.02
ADR 5000
132b.03
ADR 4000
132b.04
ADR 3000
132b.05
ADR 2000
132b.06
ADR 1000
132b.07
ADR 0000
132b.08
TO (FIG. 133)
FROM (FIG. 129a)
129a.02 STOR ADR REG (6)
129a.04 STOR ADR REG (7)
129a.06 STORE ADR REG (8)
129a.01 STOR ADR REG (6̄)
129a.03 STOR ADR REG (7̄)
129a.05 STOR ADR REG (8̄)

WRITE DRIVER SELECT CIRCUITS

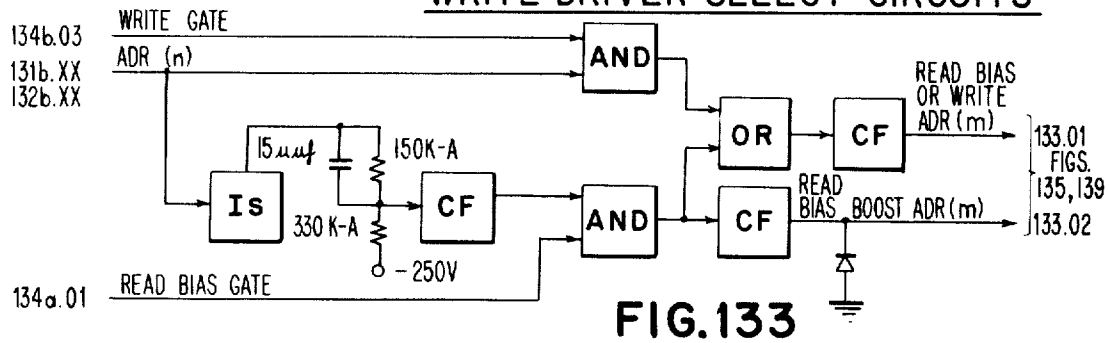


FIG.133

FIG.135 X MATRIX SWITCH WRITE DRIVER

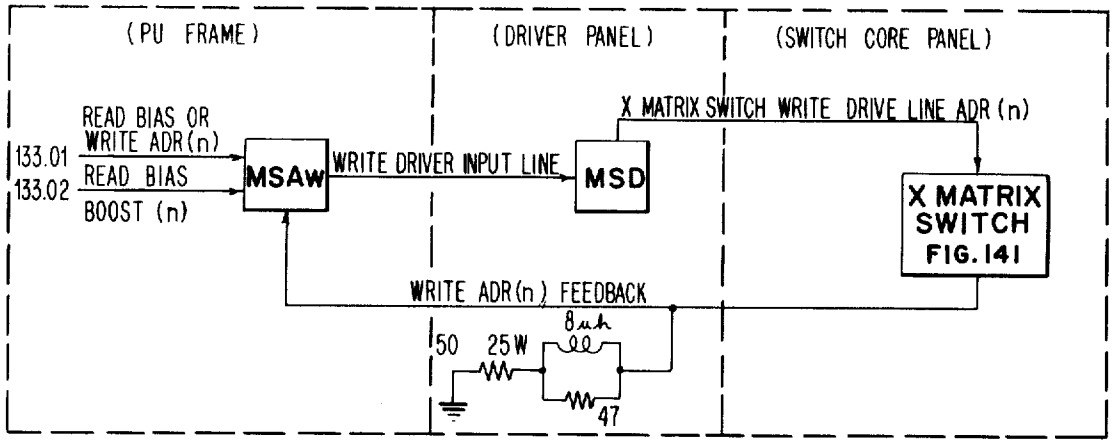
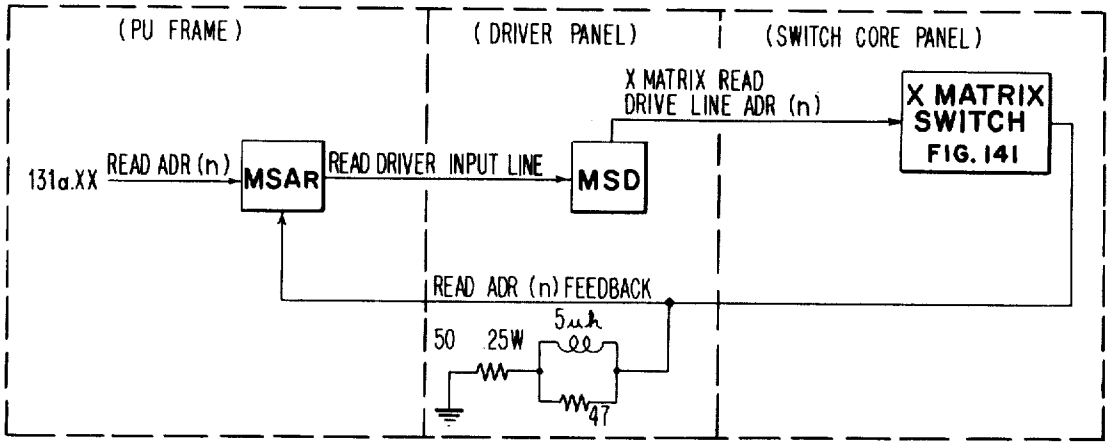


FIG.136 X MATRIX SWITCH READ DRIVER



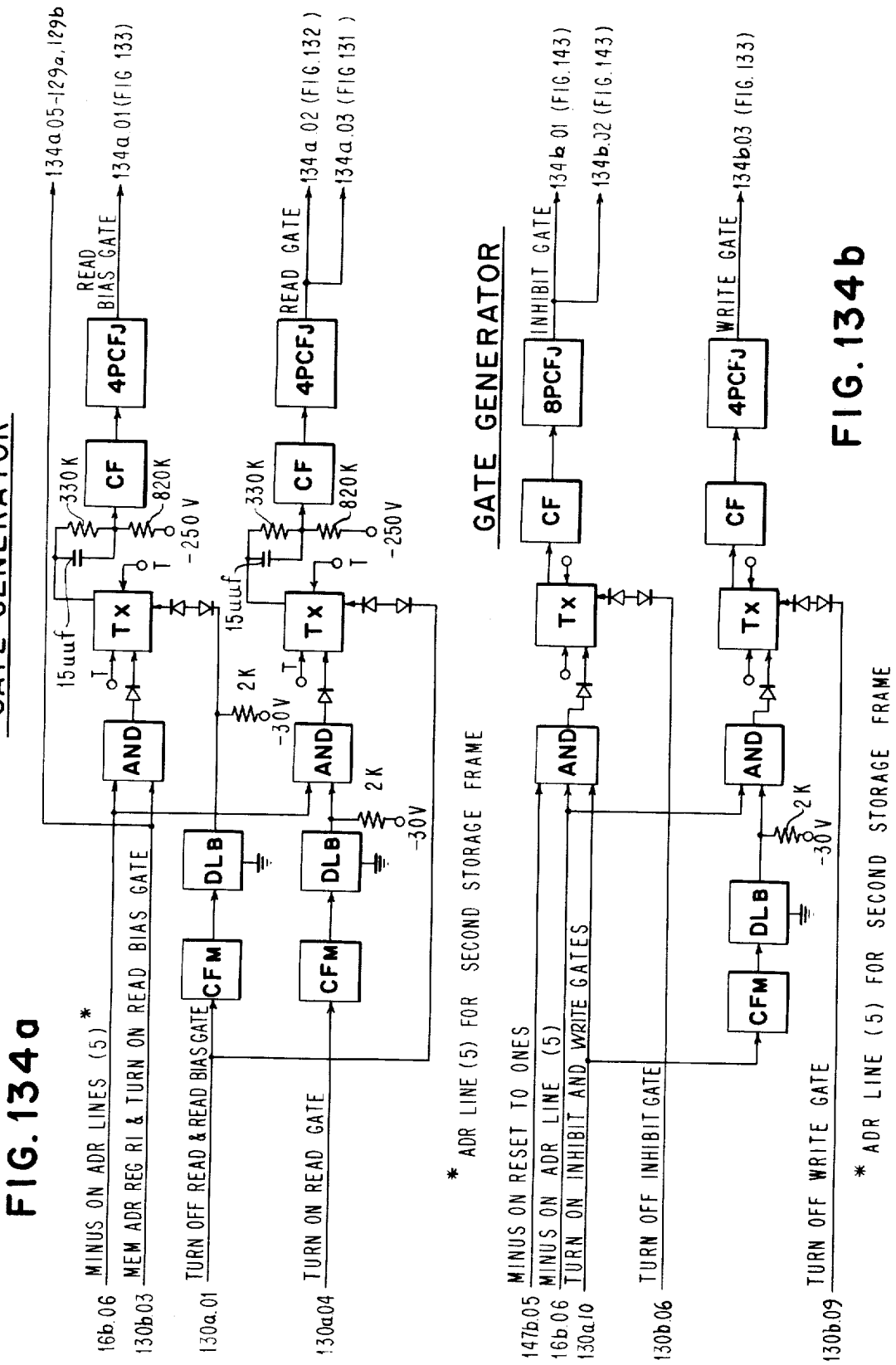


FIG. 134a

FIG. 134b

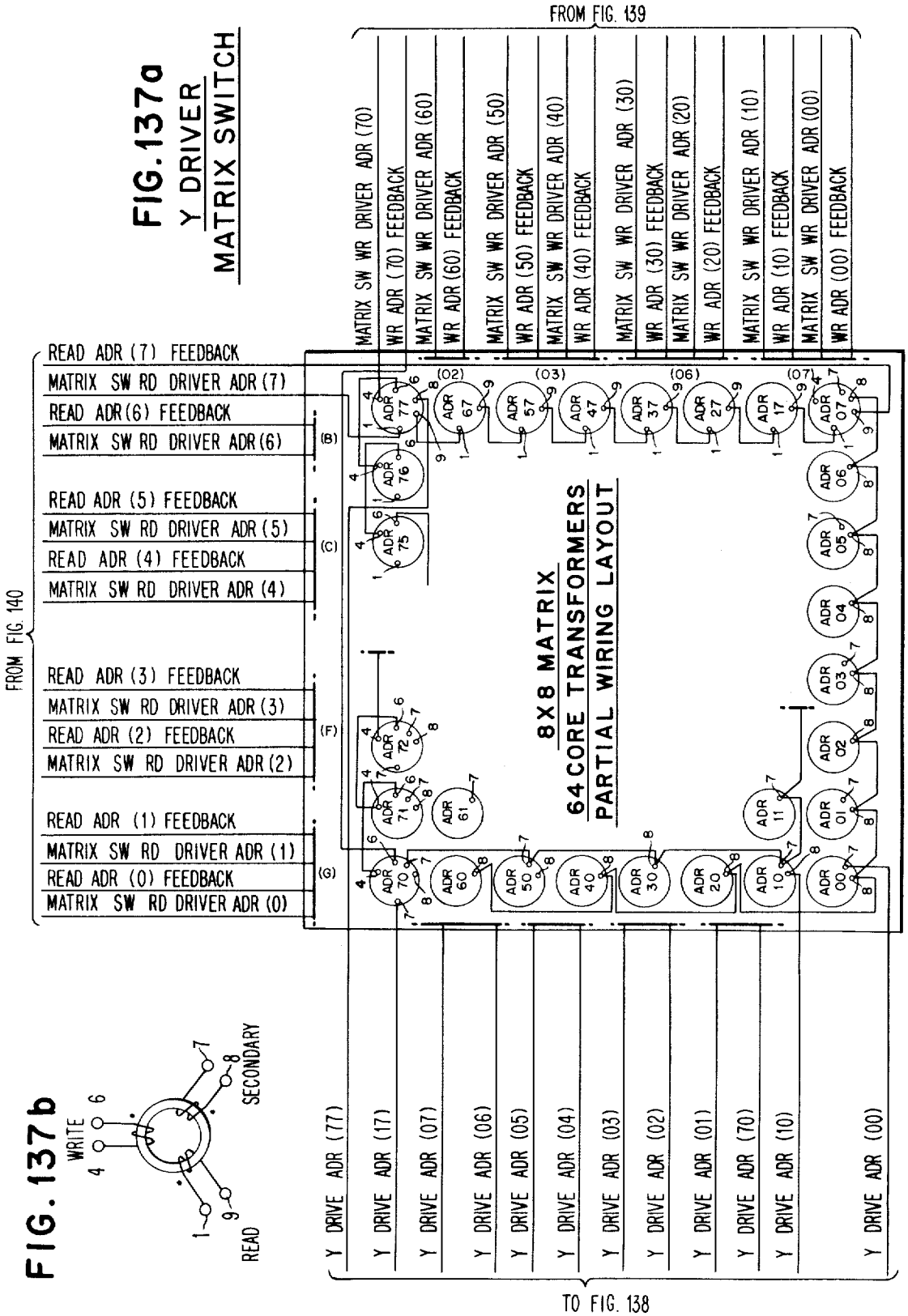

FIG. 137a
Y DRIVER
MATRIX SWITCH
FROM FIG. 139
MATRIX SW WR DRIVER ADR (70)
WR ADR (70) FEEDBACK
MATRIX SW WR DRIVER ADR (60)
WR ADR (60) FEEDBACK
MATRIX SW WR DRIVER ADR (50)
WR ADR (50) FEEDBACK
MATRIX SW WR DRIVER ADR (40)
WR ADR (40) FEEDBACK
MATRIX SW WR DRIVER ADR (30)
WR ADR (30) FEEDBACK
MATRIX SW WR DRIVER ADR (20)
WR ADR (20) FEEDBACK
MATRIX SW WR DRIVER ADR (10)
WR ADR (10) FEEDBACK
MATRIX SW WR DRIVER ADR (00)
WR ADR (00) FEEDBACK
FROM FIG. 140
READ ADR (7) FEEDBACK
MATRIX SW RD DRIVER ADR (7)
READ ADR (6) FEEDBACK
MATRIX SW RD DRIVER ADR (6)
READ ADR (5) FEEDBACK
MATRIX SW RD DRIVER ADR (5)
READ ADR (4) FEEDBACK
MATRIX SW RD DRIVER ADR (4)
READ ADR (3) FEEDBACK
MATRIX SW RD DRIVER ADR (3)
READ ADR (2) FEEDBACK
MATRIX SW RD DRIVER ADR (2)
READ ADR (1) FEEDBACK
MATRIX SW RD DRIVER ADR (1)
READ ADR (0) FEEDBACK
MATRIX SW RD DRIVER ADR (0)
(B)
(C)
(F)
(G)
8X8 MATRIX
64 CORE TRANSFORMERS
PARTIAL WIRING LAYOUT
(02)
(03)
(06)
(07)
FIG. 137b
WRITE
SECONDARY
READ
Y DRIVE ADR (77)
Y DRIVE ADR (17)
Y DRIVE ADR (07)
Y DRIVE ADR (06)
Y DRIVE ADR (05)
Y DRIVE ADR (04)
Y DRIVE ADR (03)
Y DRIVE ADR (02)
Y DRIVE ADR (01)
Y DRIVE ADR (70)
Y DRIVE ADR (10)
Y DRIVE ADR (00)
TO FIG. 138

FIG.138b

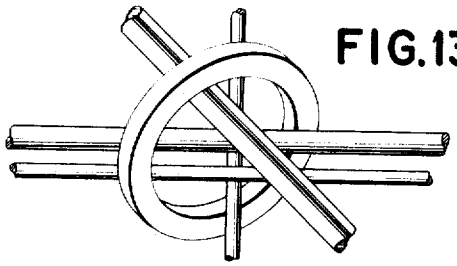


FIG.138a

CORE ARRAY

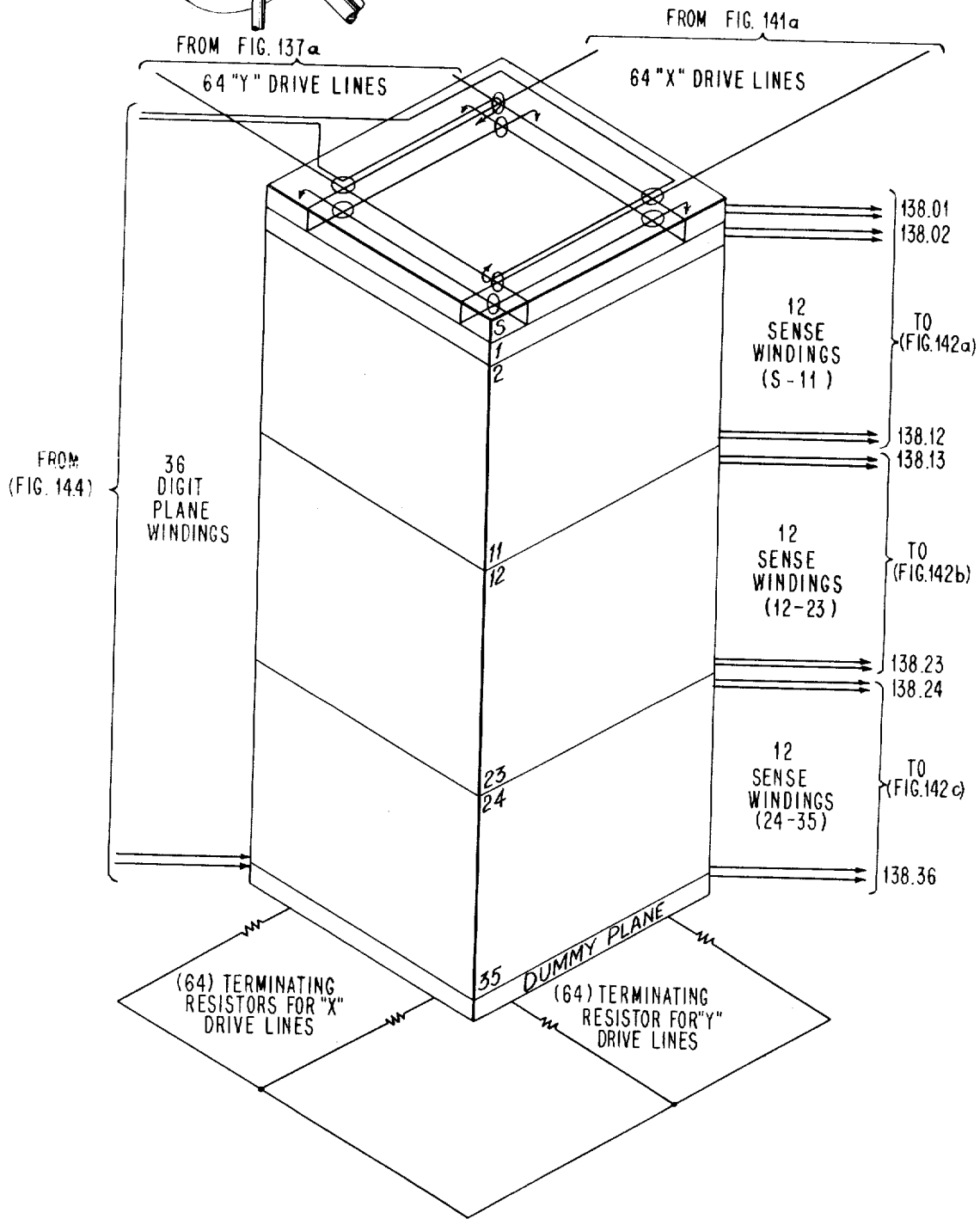


FIG. 139 Y MATRIX SWITCH WRITE DRIVER

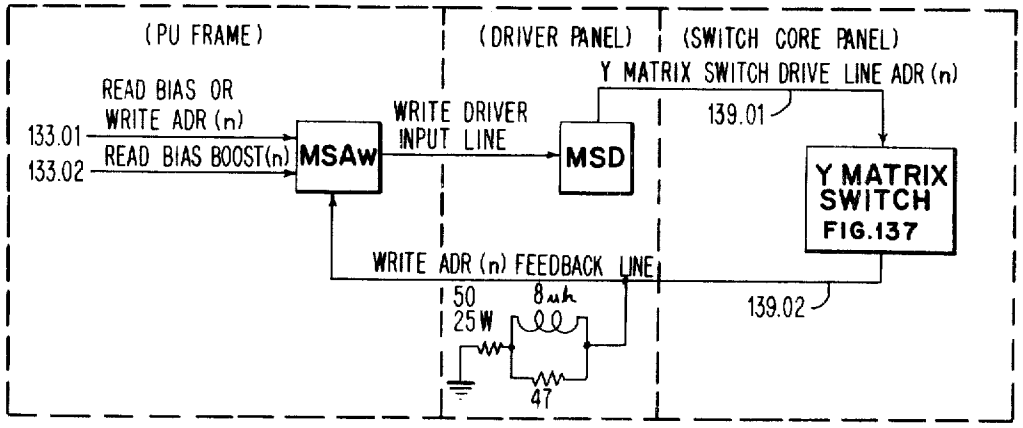


FIG. 140 Y MATRIX SWITCH READ DRIVER

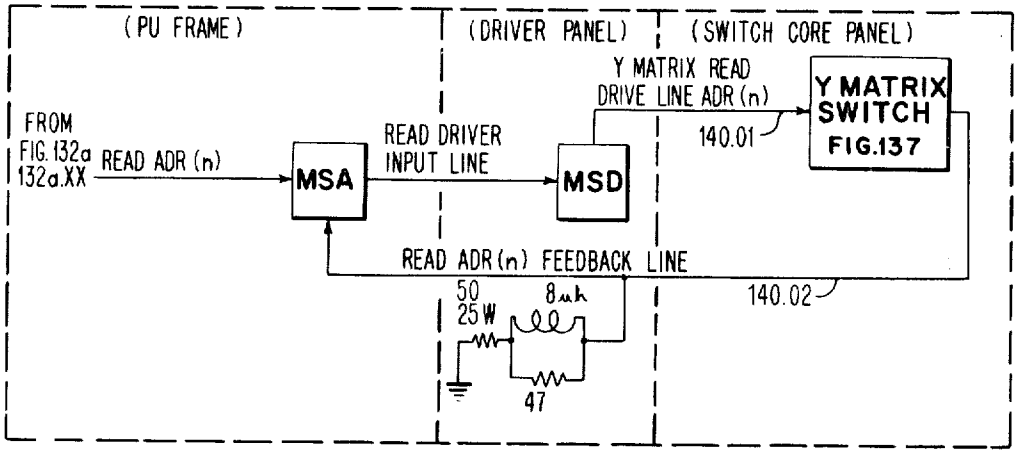


FIG. 143 DIGIT PLANE SELECT CIRCUITS



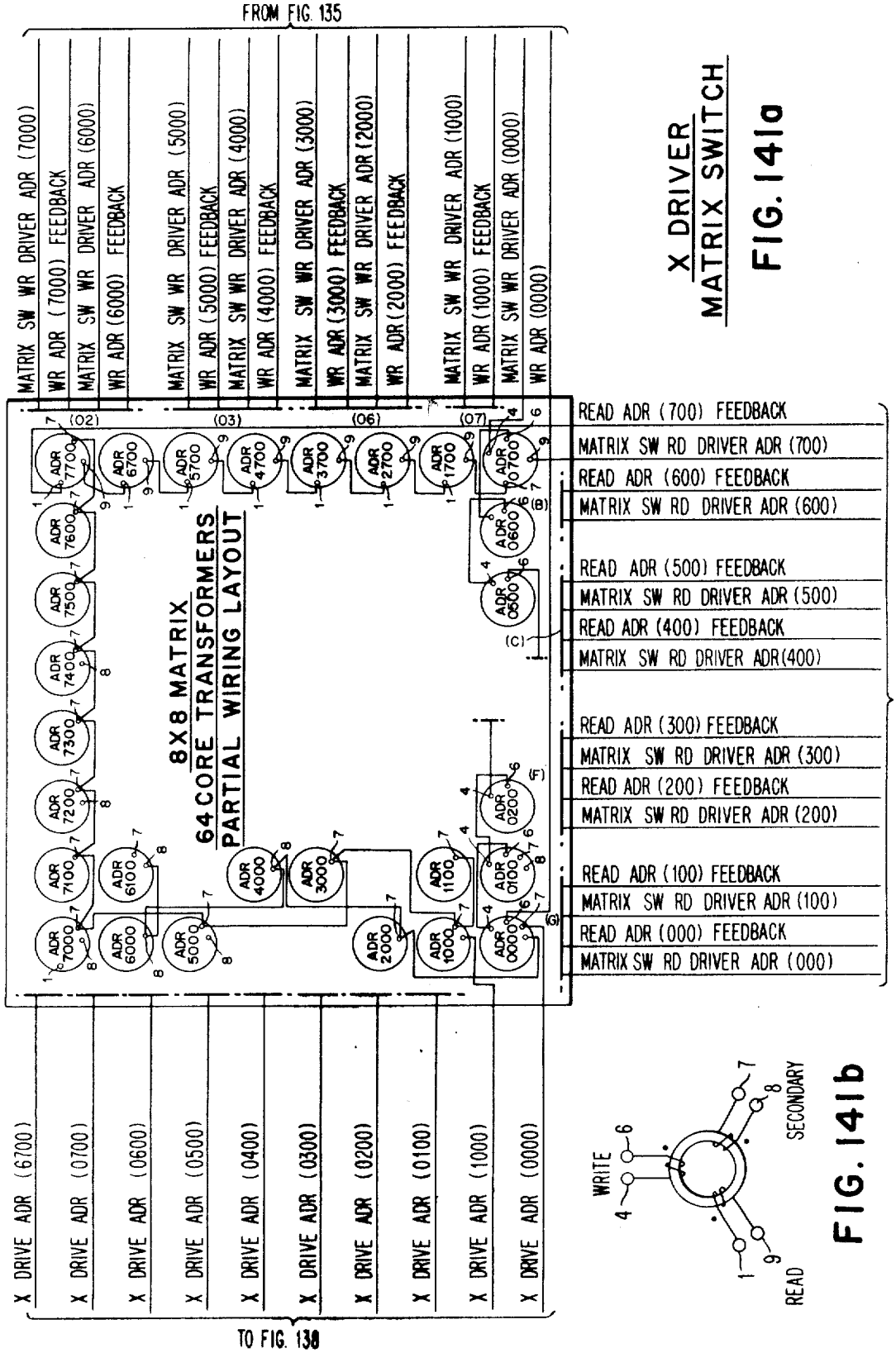


FIG. 141a

FIG. 141b

SENSE AMP, BUFFER REGISTER & I/O SWITCHING

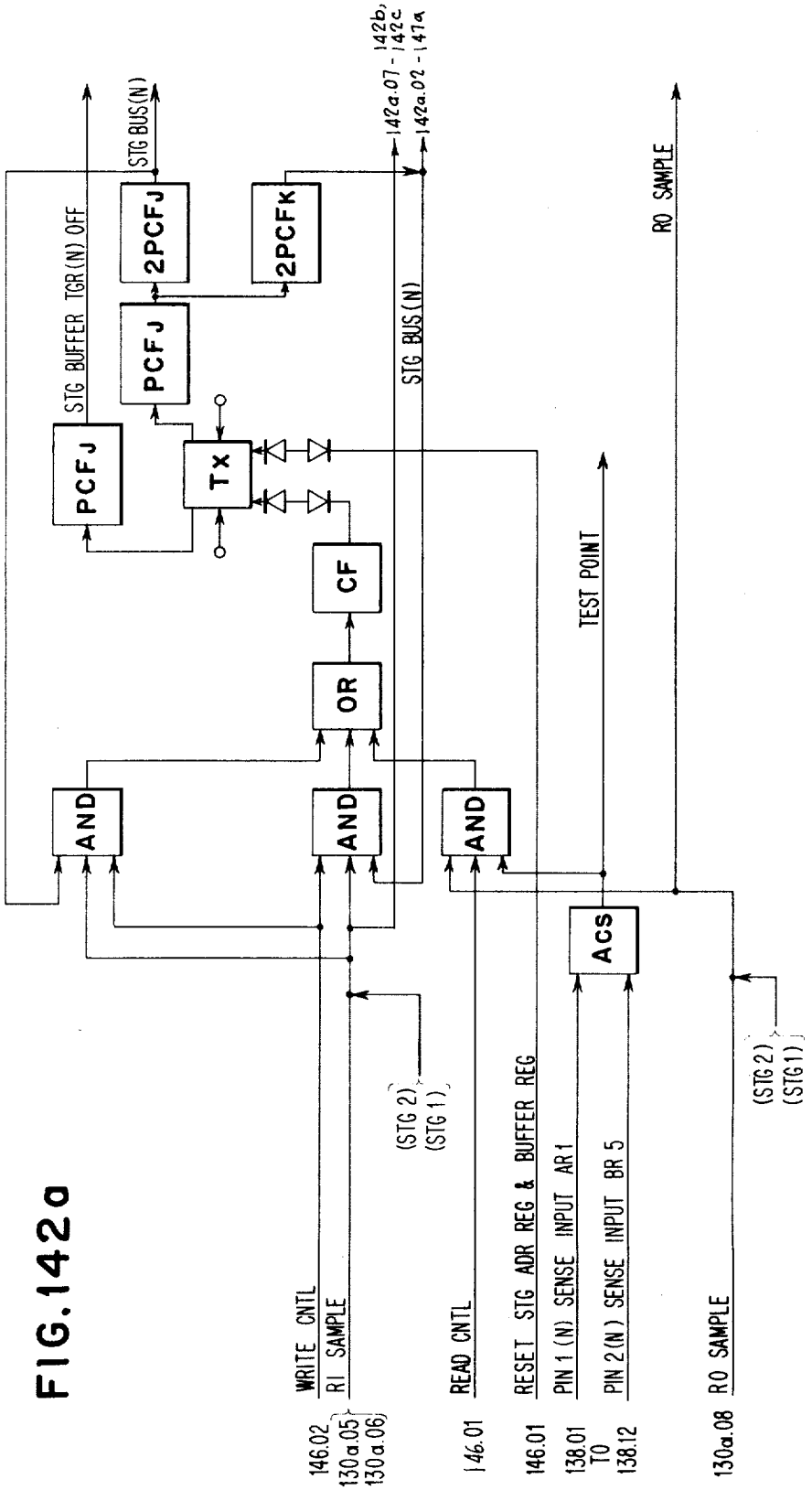


FIG.142a

SENSE AMP, BUFFER REGISTER & I/O SWITCHING

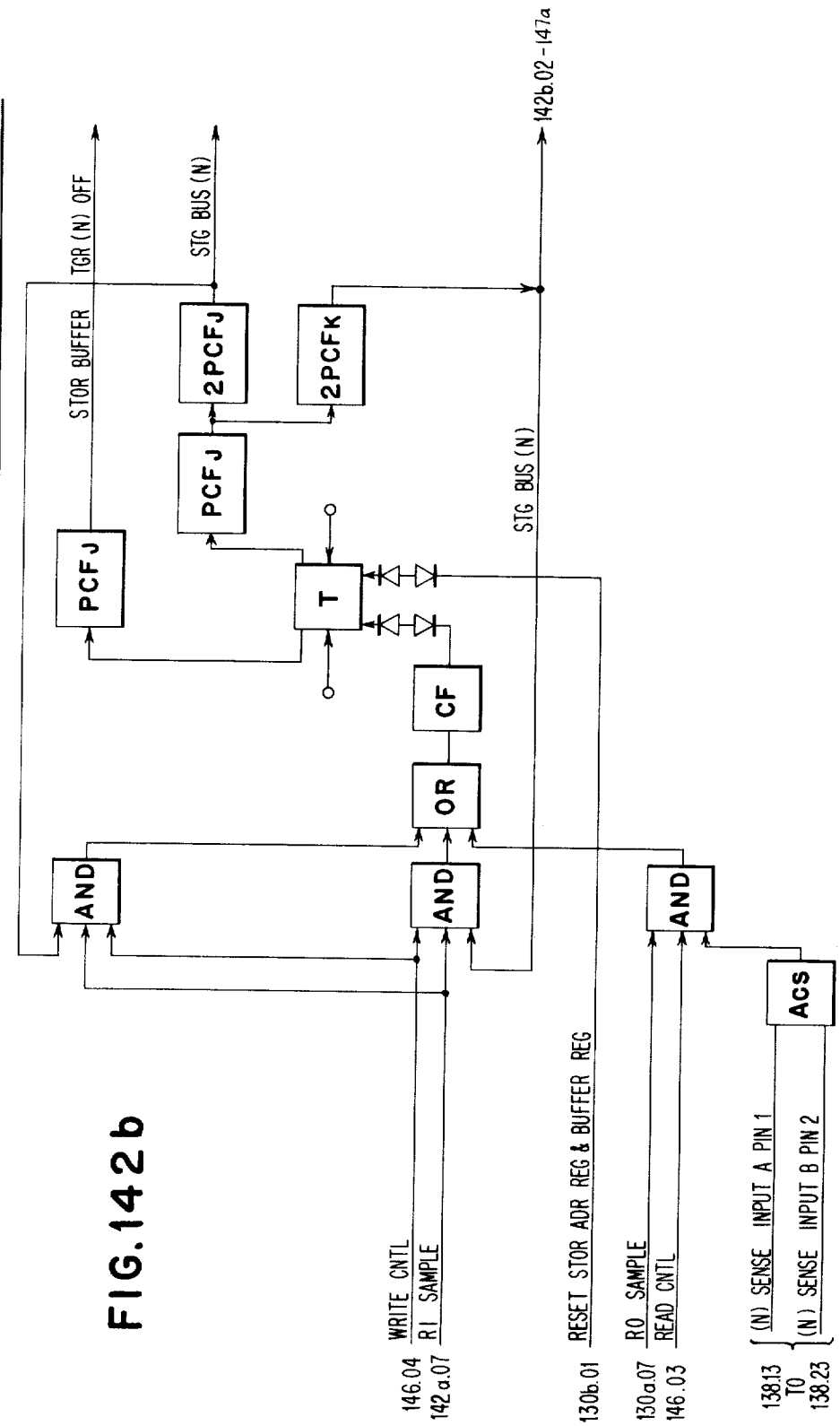


FIG. 142b

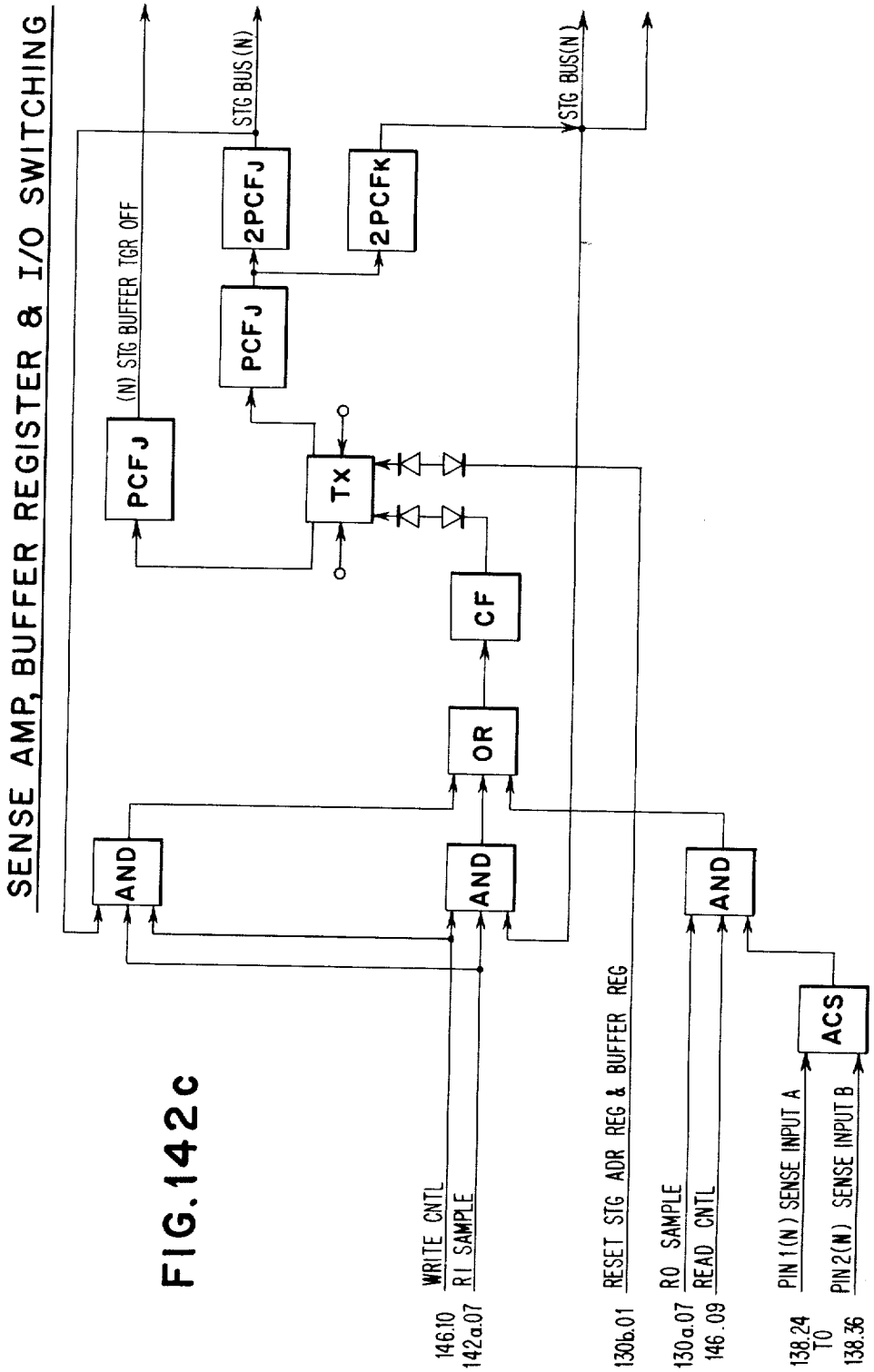

SENSE AMP, BUFFER REGISTER & I/O SWITCHING
(N) STG BUFFER TGR OFF
STG BUS (N)
STG BUS(N)
PCFJ
2PCFJ
PCFJ
2PCFK
TX
CF
OR
AND
AND
AND
ACS
WRITE CNTL
R1 SAMPLE
RESET STG ADR REG & BUFFER REG
R0 SAMPLE
READ CNTL
PIN 1(N) SENSE INPUT A
PIN 2(N) SENSE INPUT B
146.10
142a.07
130b.01
130a.07
146.09
138.24
TO
138.36

FIG. 142c

FIG.147c

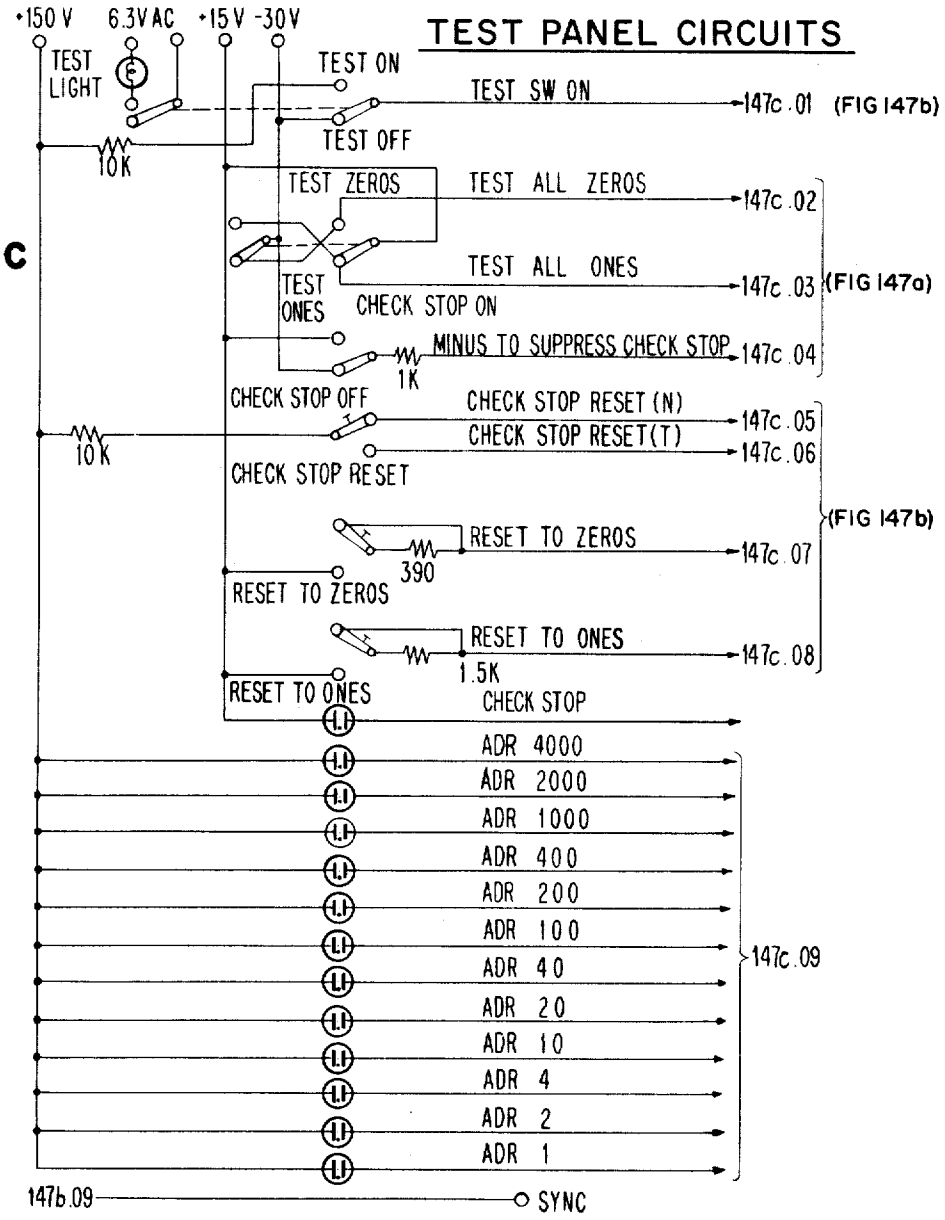


FIG.144

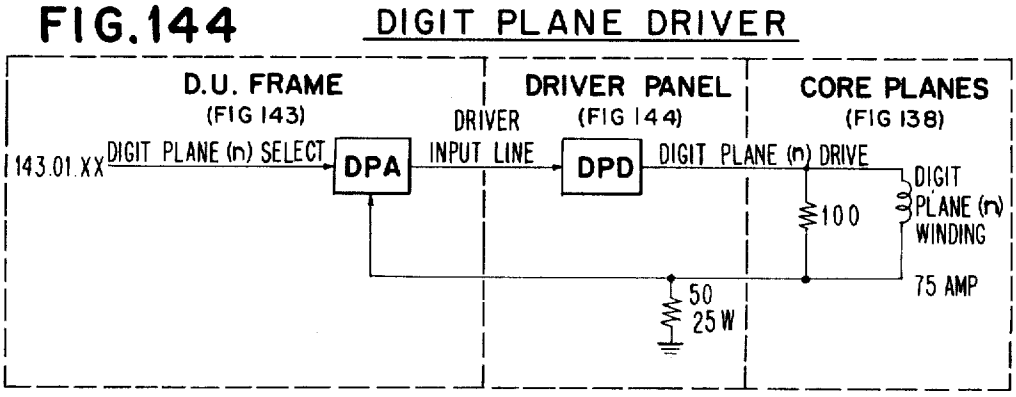


FIG. 145

ADDRESS & OPERATION CONTROL

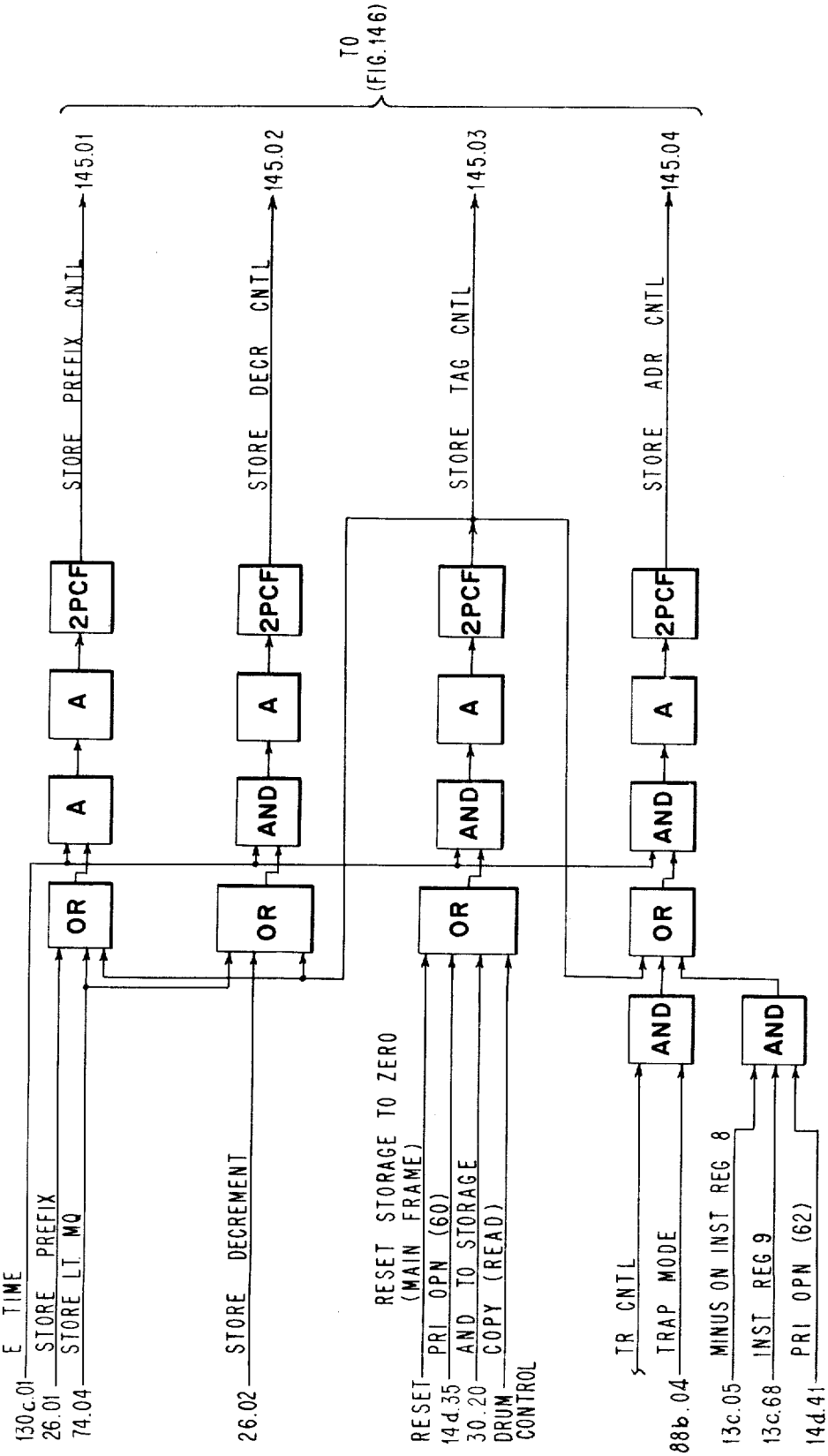


FIG. 146

READ/WRITE CONTROLS

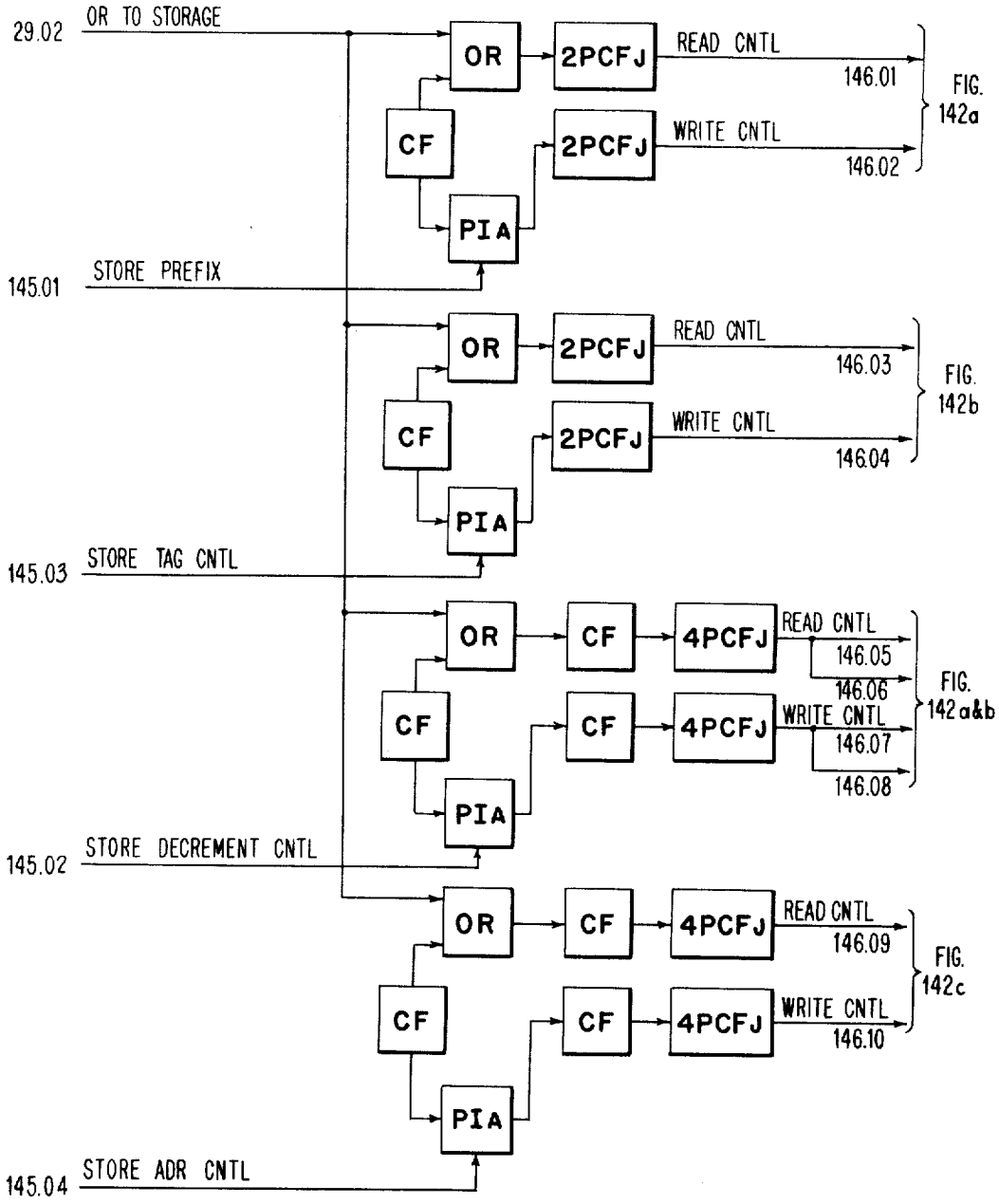


FIG.147a

TEST CIRCUIT

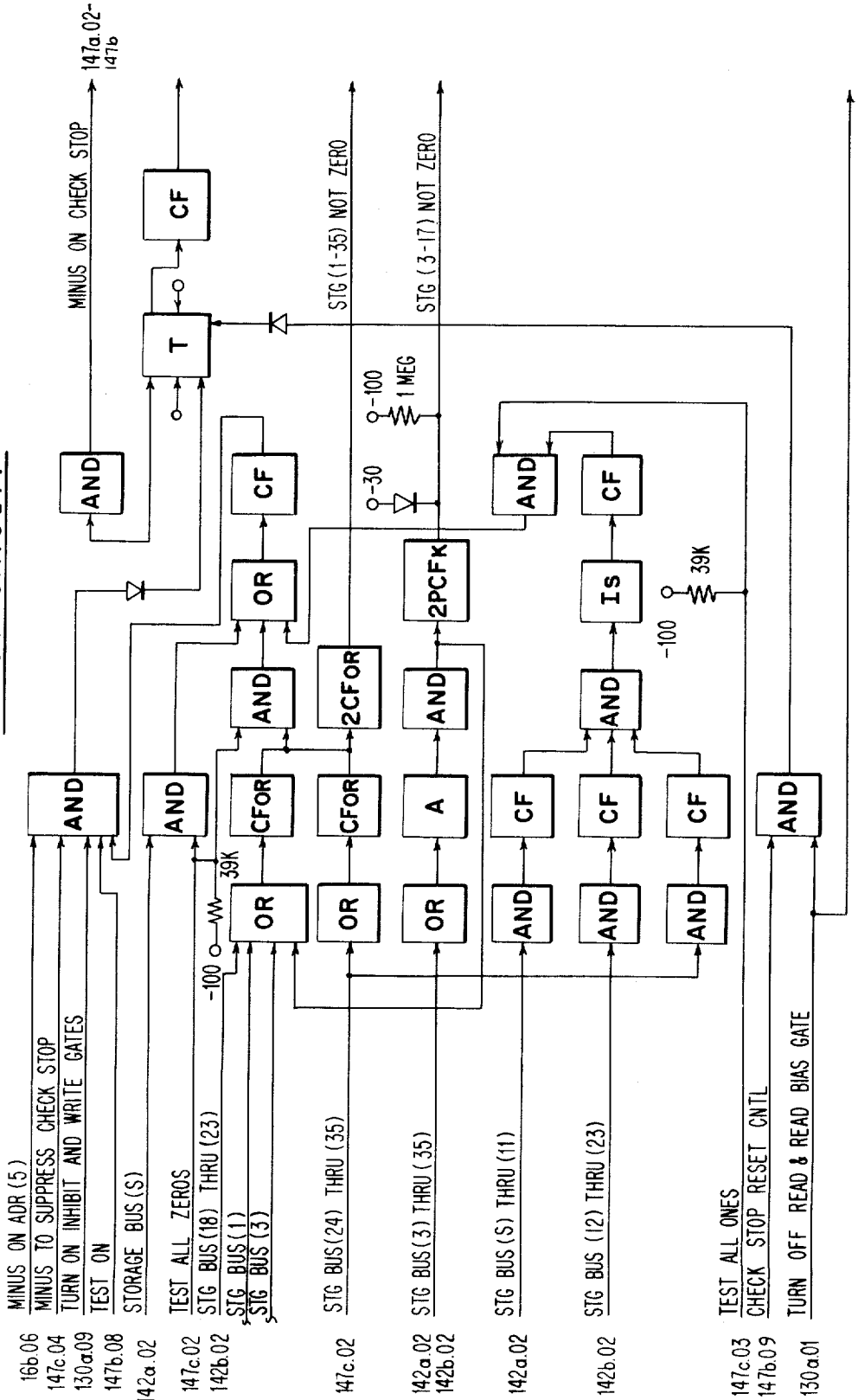


FIG. 147b

TEST & RESET CONTROLS

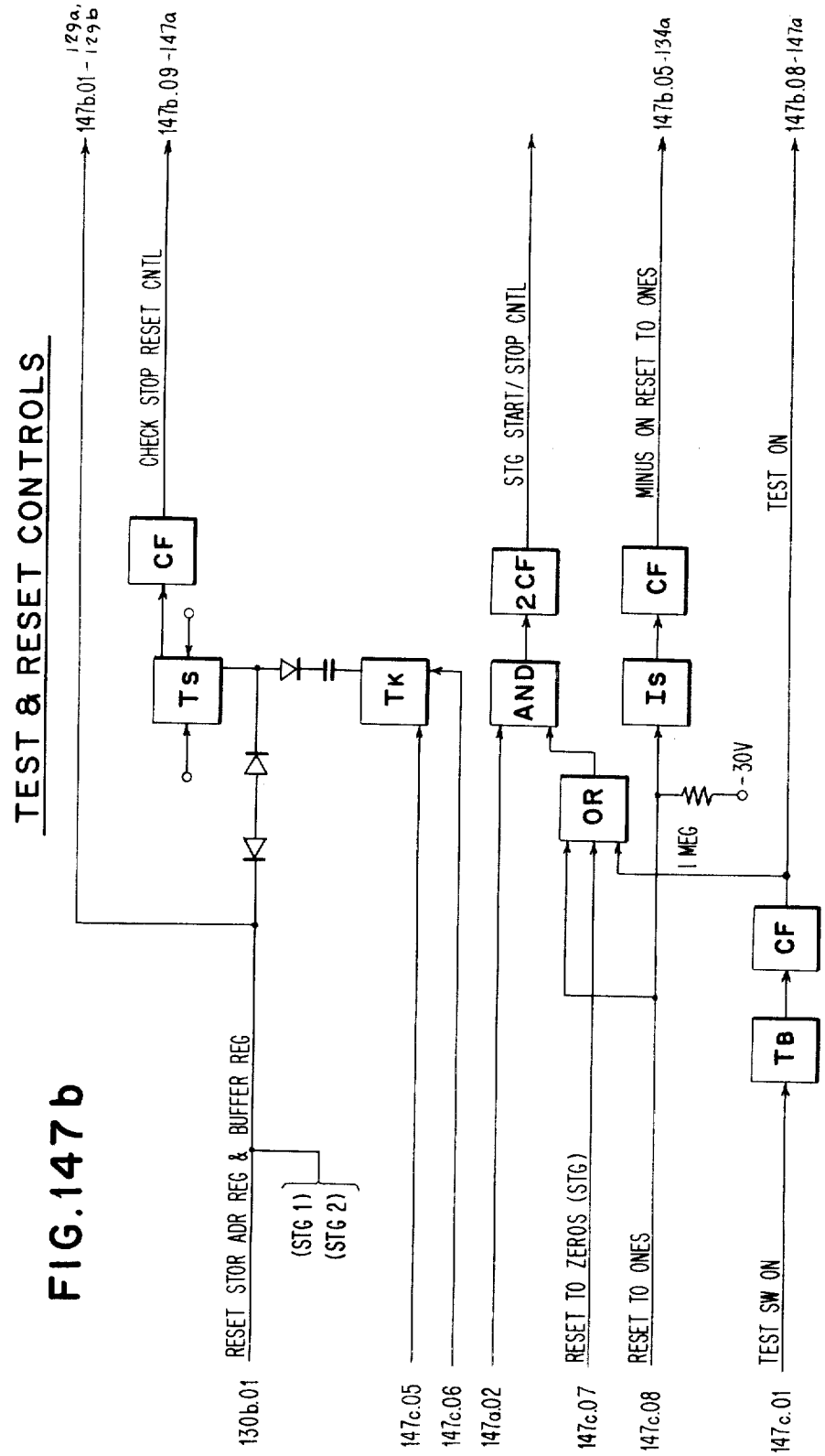
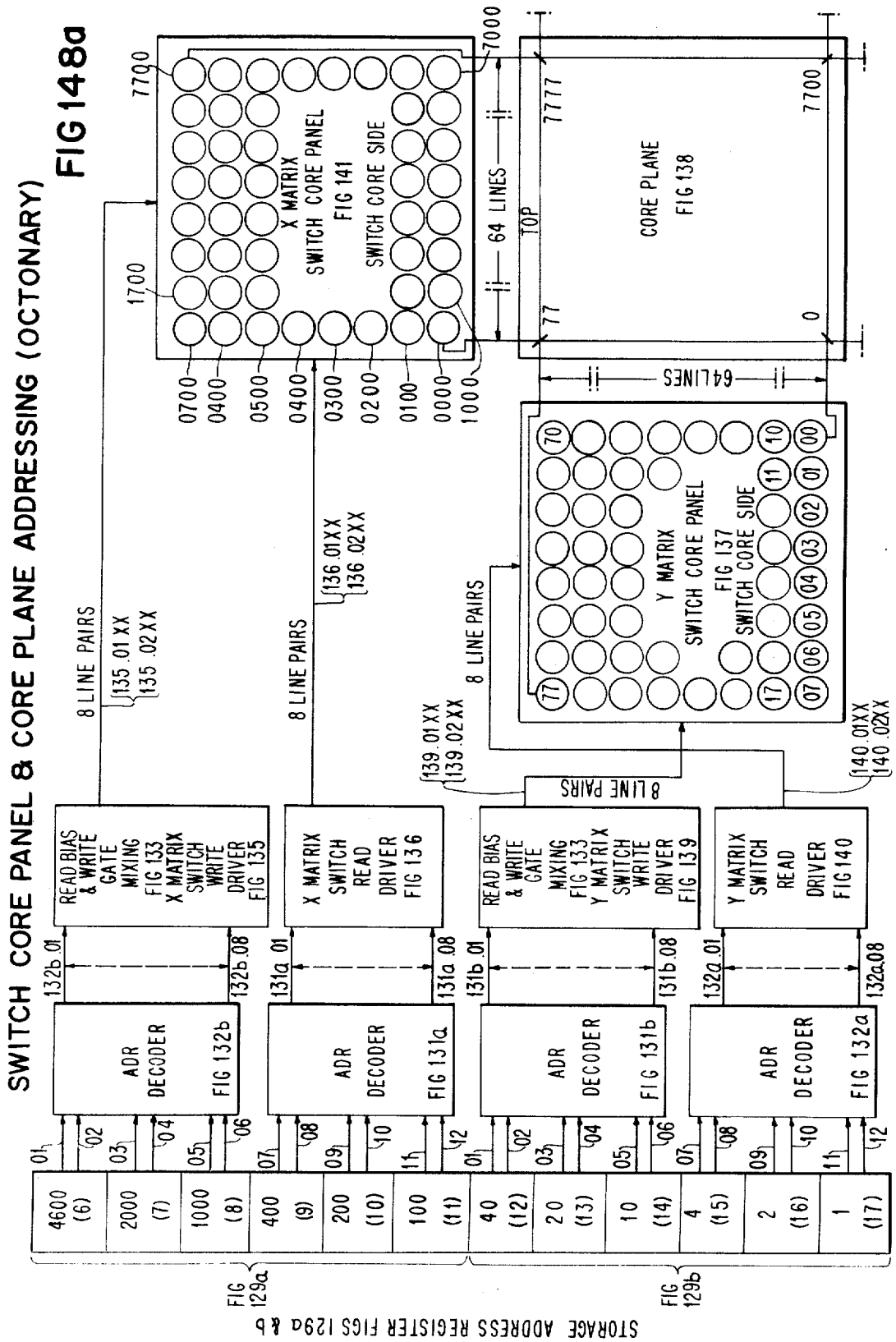


FIG 148a

SWITCH CORE PANEL & CORE PLANE ADDRESSING (OCTONARY)



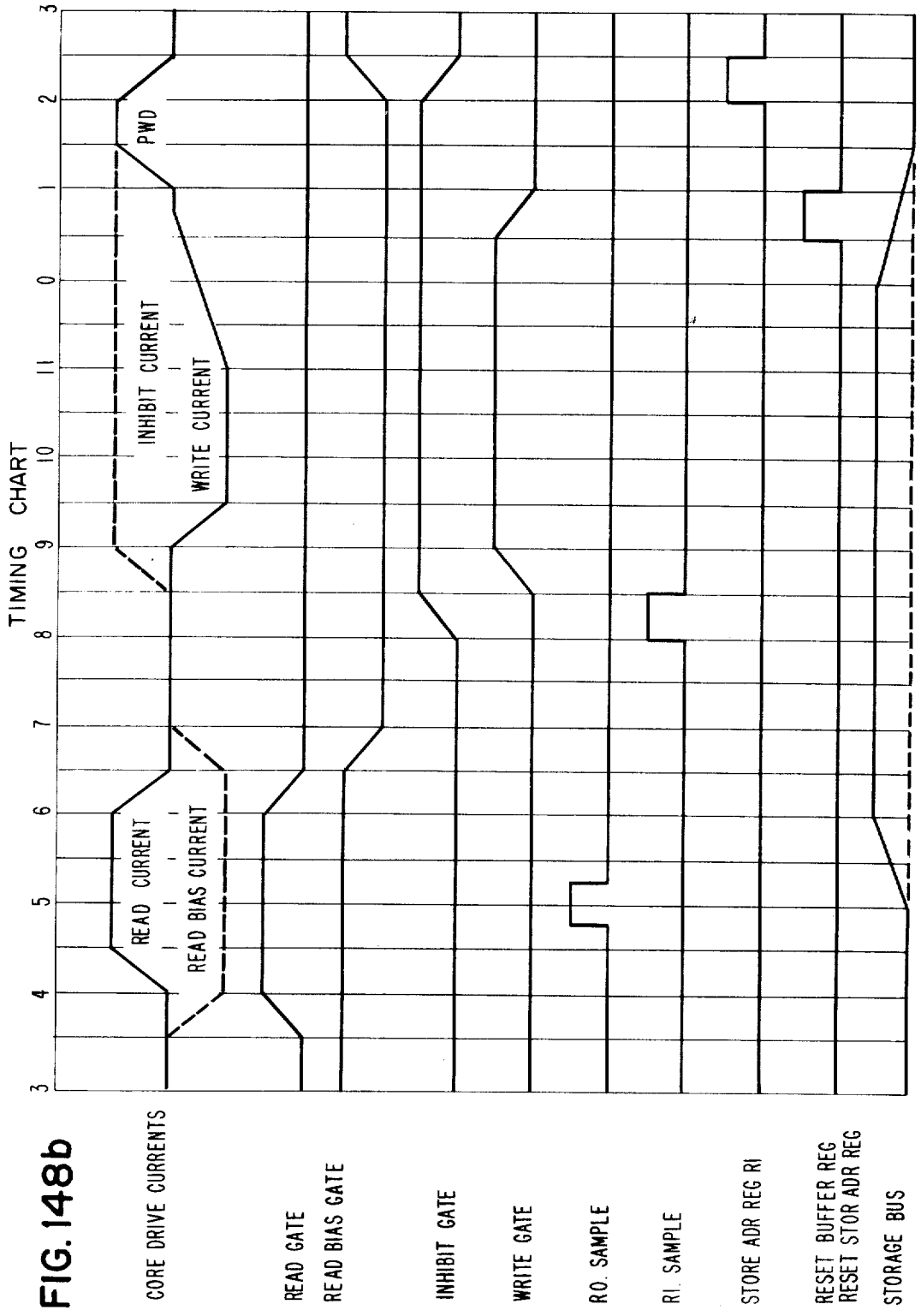
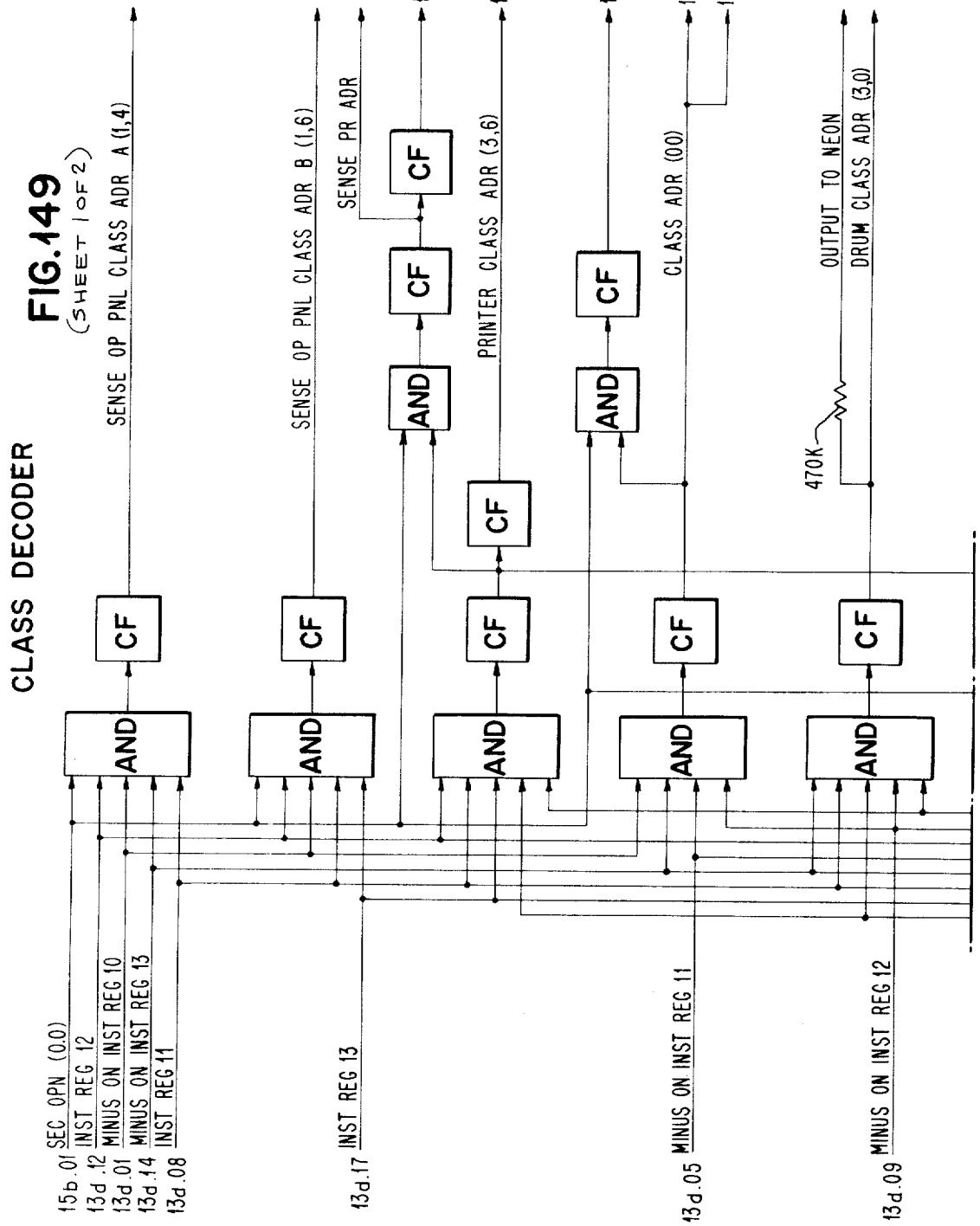

TIMING CHART
3
4
5
6
7
8
9
10
11
0
1
2
3
READ CURRENT
READ BIAS CURRENT
INHIBIT CURRENT
WRITE CURRENT
PWD
CORE DRIVE CURRENTS
READ GATE
READ BIAS GATE
INHIBIT GATE
WRITE GATE
RO. SAMPLE
RI. SAMPLE
STORE ADR REG RI
RESET BUFFER REG
RESET STOR ADR REG
STORAGE BUS

FIG. 148b

FIG.149
(SHEET 1 OF 2)



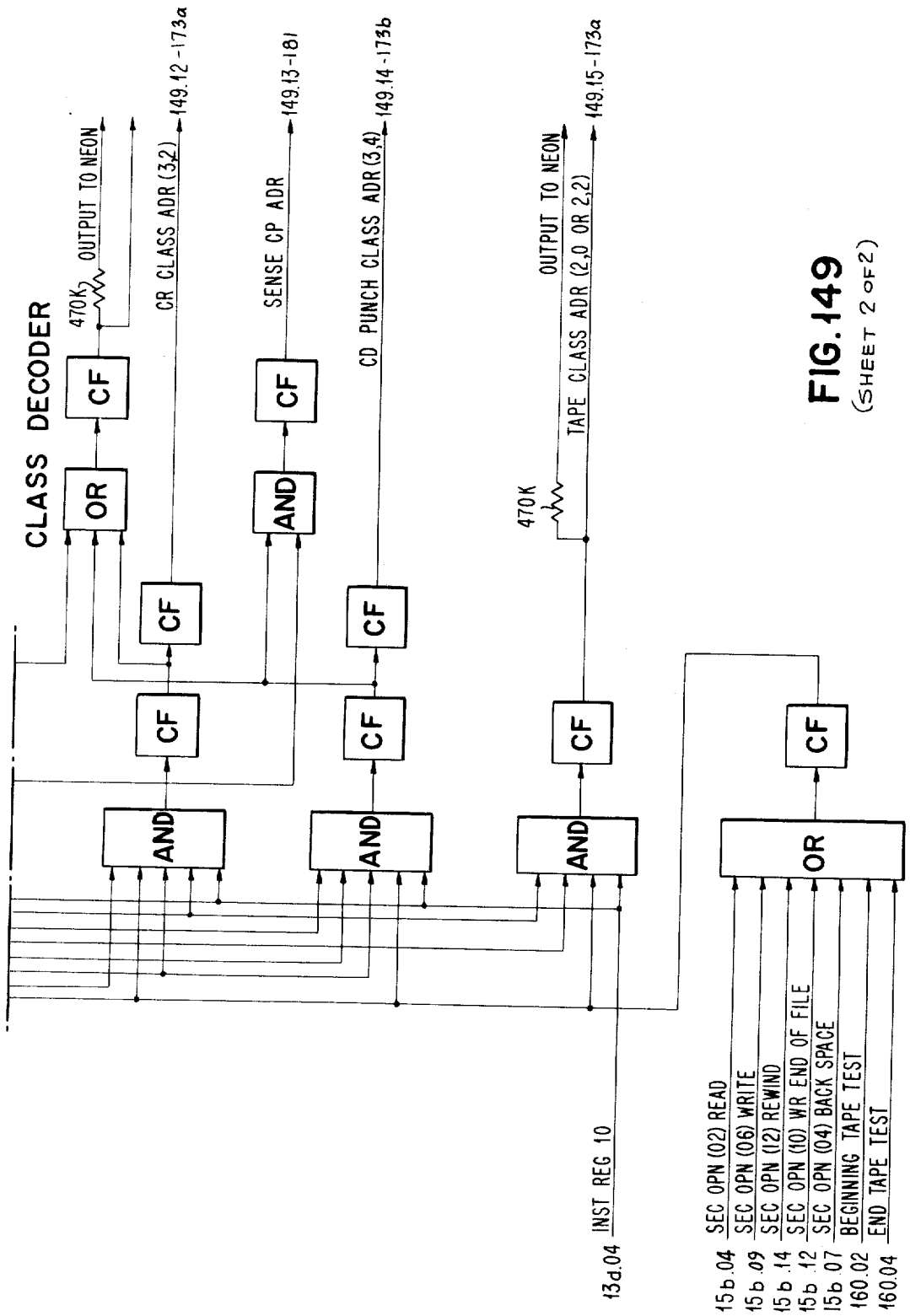


FIG. 149
(SHEET 2 OF 2)

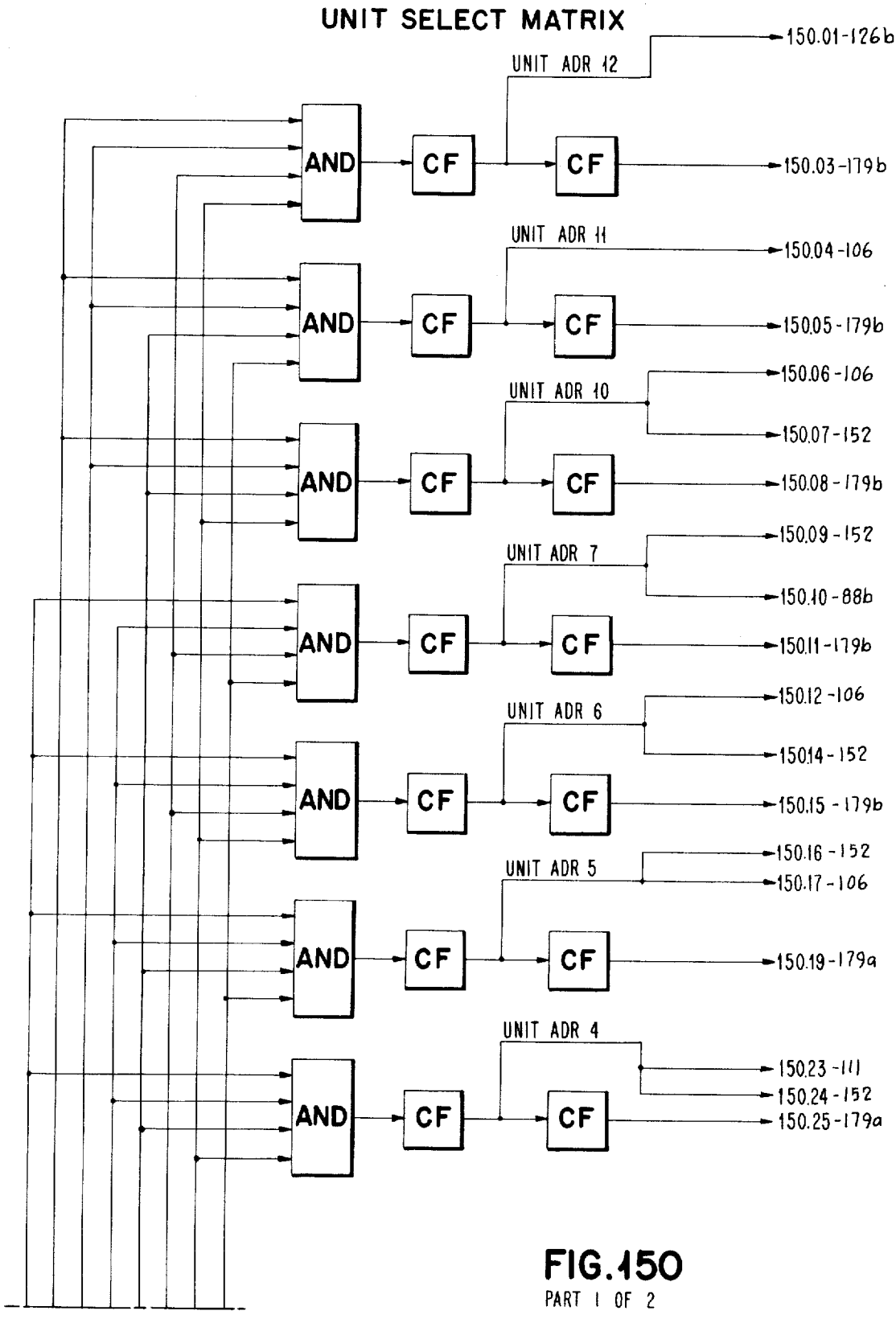


FIG.150
PART 1 OF 2

UNIT SELECT MATRIX PART 2 OF 2

FIG. 150

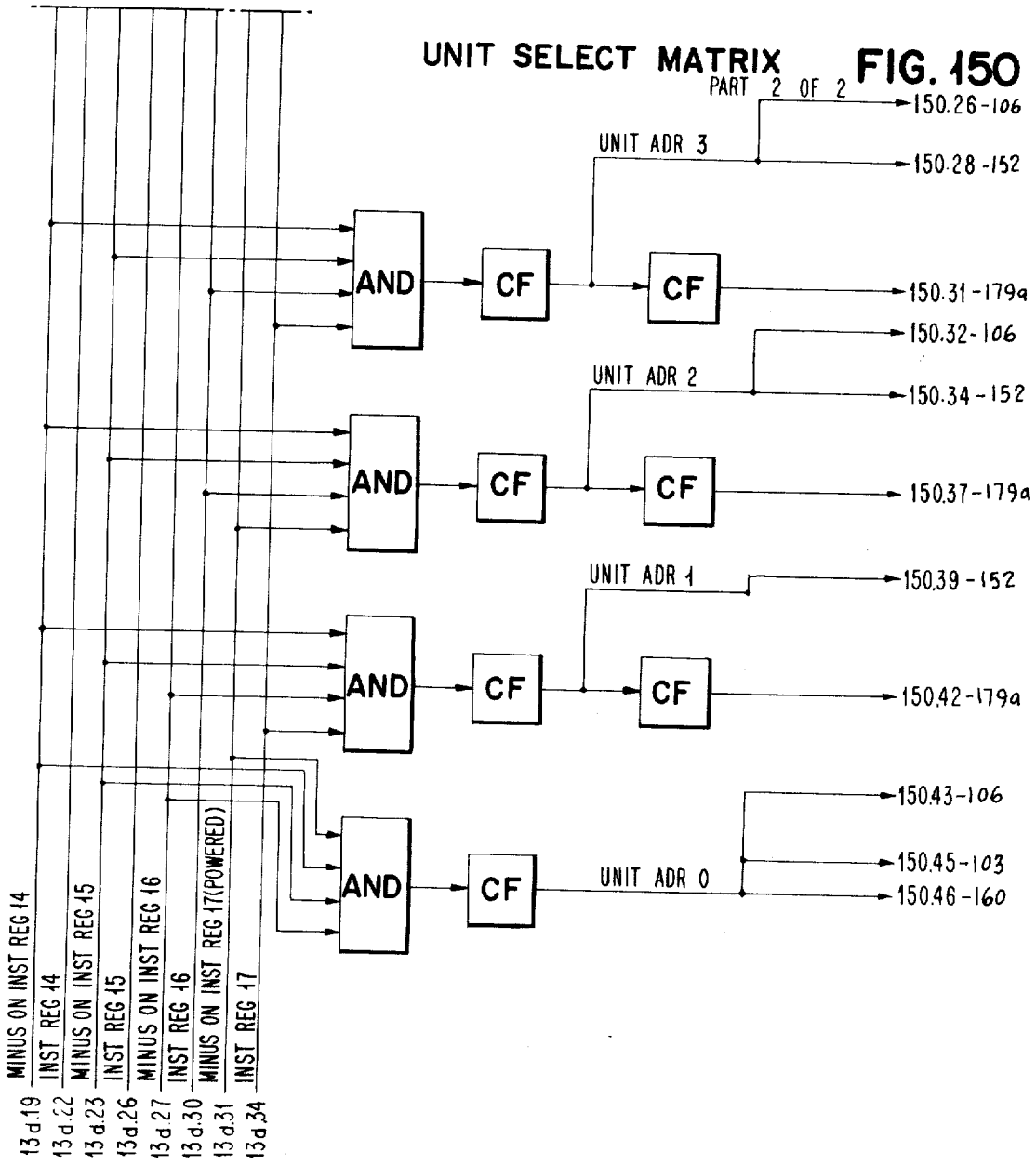


FIG. 151

I/O SELECTION INTERLOCK

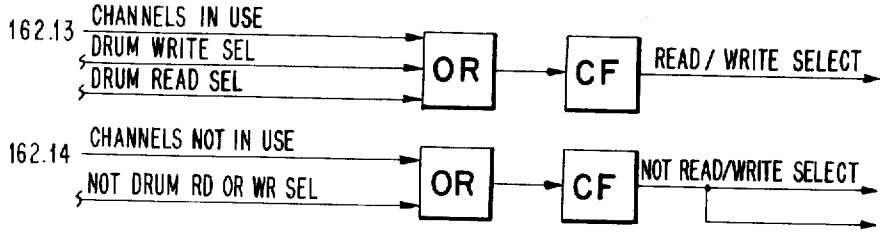
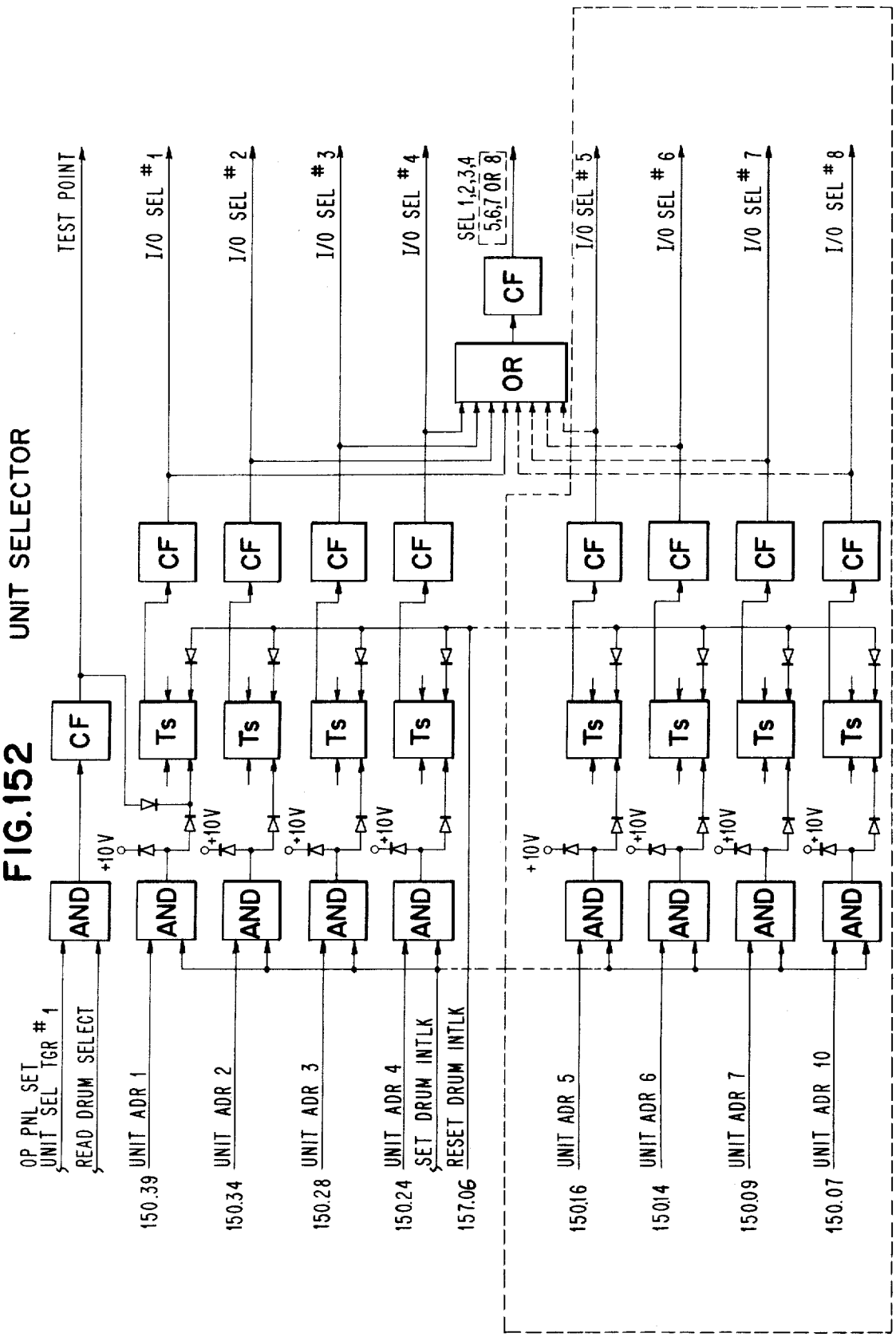


FIG.152


UNIT SELECTOR
TEST POINT
I/O SEL #1
I/O SEL #2
I/O SEL #3
I/O SEL #4
SEL 1,2,3,4 5,6,7 OR 8
I/O SEL #5
I/O SEL #6
I/O SEL #7
I/O SEL #8
CF
OR
Ts
AND
+10V
OP PNL SET UNIT SEL TGR #1
READ DRUM SELECT
UNIT ADR 1
UNIT ADR 2
UNIT ADR 3
UNIT ADR 4
SET DRUM INTLK
RESET DRUM INTLK
UNIT ADR 5
UNIT ADR 6
UNIT ADR 7
UNIT ADR 10
150.39
150.34
150.28
150.24
157.06
150.16
150.14
150.09
150.07

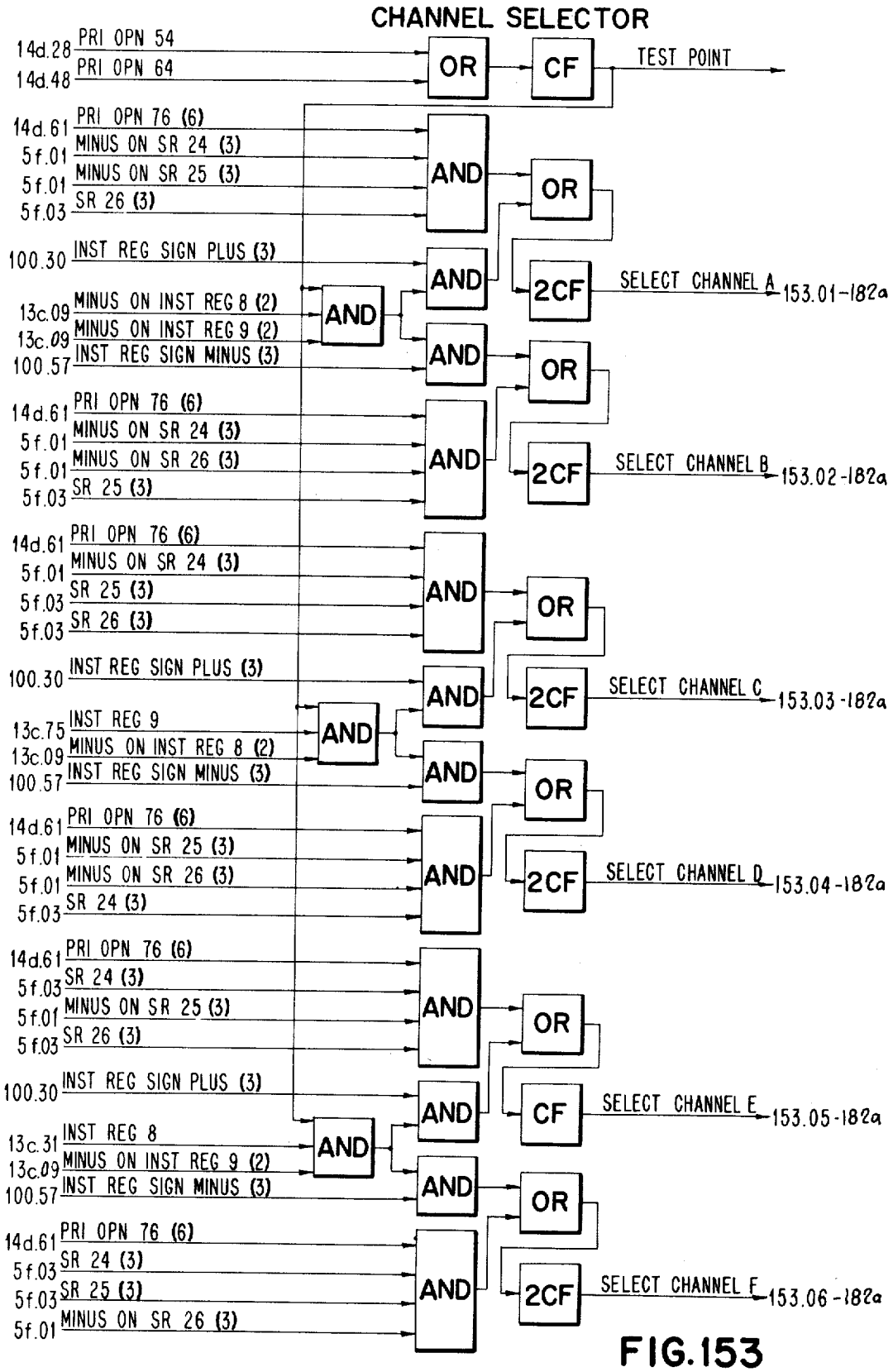
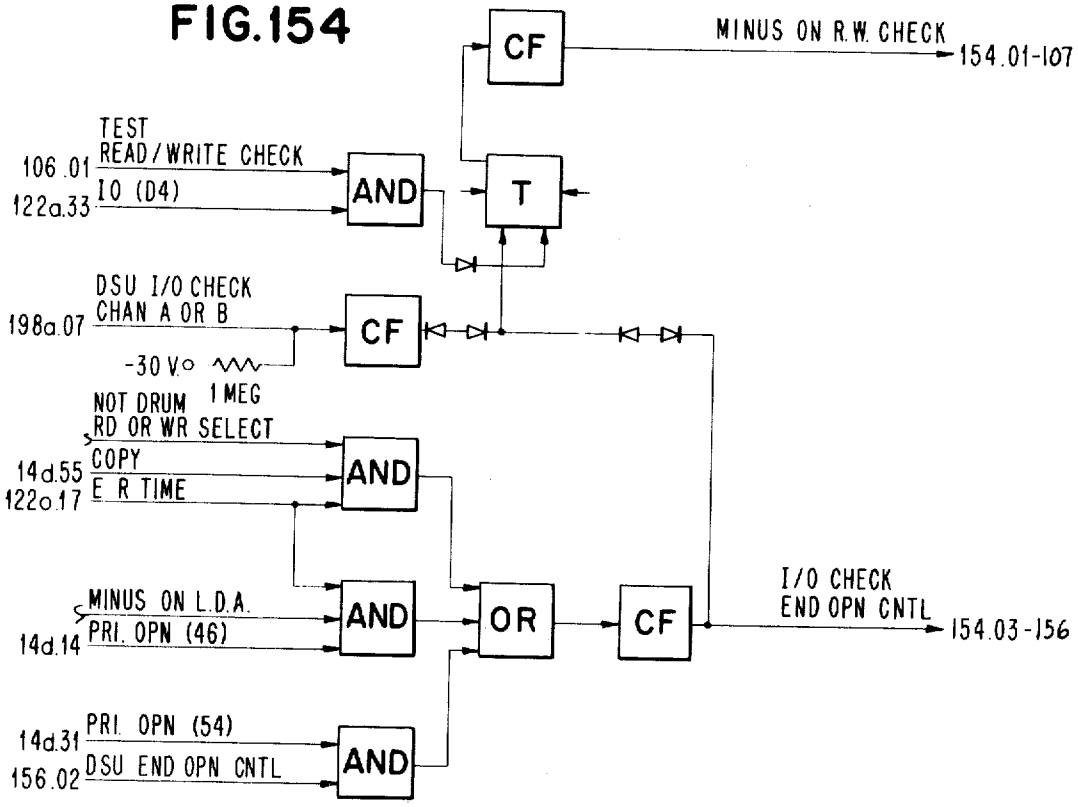

CHANNEL SELECTOR
14d.28 PRI OPN 54
14d.48 PRI OPN 64
OR
CF
TEST POINT
14d.61 PRI OPN 76 (6)
5f.01 MINUS ON SR 24 (3)
5f.01 MINUS ON SR 25 (3)
5f.03 SR 26 (3)
AND
OR
100.30 INST REG SIGN PLUS (3)
AND
2CF
SELECT CHANNEL A 153.01-182a
13c.09 MINUS ON INST REG 8 (2)
13c.09 MINUS ON INST REG 9 (2)
100.57 INST REG SIGN MINUS (3)
AND
AND
OR
14d.61 PRI OPN 76 (6)
5f.01 MINUS ON SR 24 (3)
5f.01 MINUS ON SR 26 (3)
5f.03 SR 25 (3)
AND
2CF
SELECT CHANNEL B 153.02-182a
14d.61 PRI OPN 76 (6)
5f.01 MINUS ON SR 24 (3)
5f.03 SR 25 (3)
5f.03 SR 26 (3)
AND
OR
100.30 INST REG SIGN PLUS (3)
AND
2CF
SELECT CHANNEL C 153.03-182a
13c.75 INST REG 9
13c.09 MINUS ON INST REG 8 (2)
100.57 INST REG SIGN MINUS (3)
AND
AND
OR
14d.61 PRI OPN 76 (6)
5f.01 MINUS ON SR 25 (3)
5f.01 MINUS ON SR 26 (3)
5f.03 SR 24 (3)
AND
2CF
SELECT CHANNEL D 153.04-182a
14d.61 PRI OPN 76 (6)
5f.03 SR 24 (3)
5f.01 MINUS ON SR 25 (3)
5f.03 SR 26 (3)
AND
OR
100.30 INST REG SIGN PLUS (3)
AND
CF
SELECT CHANNEL E 153.05-182a
13c.31 INST REG 8
13c.09 MINUS ON INST REG 9 (2)
100.57 INST REG SIGN MINUS (3)
AND
AND
OR
14d.61 PRI OPN 76 (6)
5f.03 SR 24 (3)
5f.03 SR 25 (3)
5f.01 MINUS ON SR 26 (3)
AND
2CF
SELECT CHANNEL F 153.06-182a

FIG.153

INTLK TEST SKIP CNTL

FIG.154



ENTER EXECUTE FIG.155

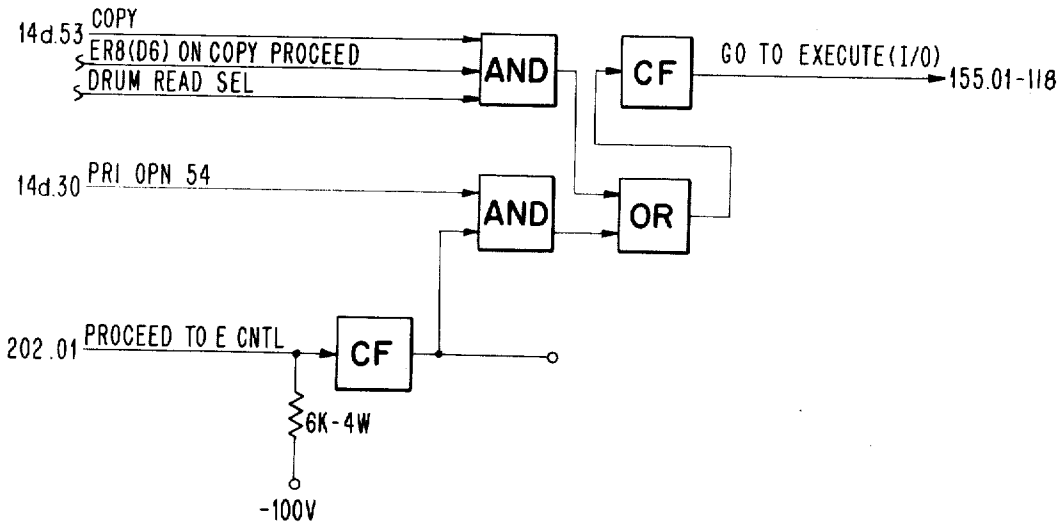


FIG. 156

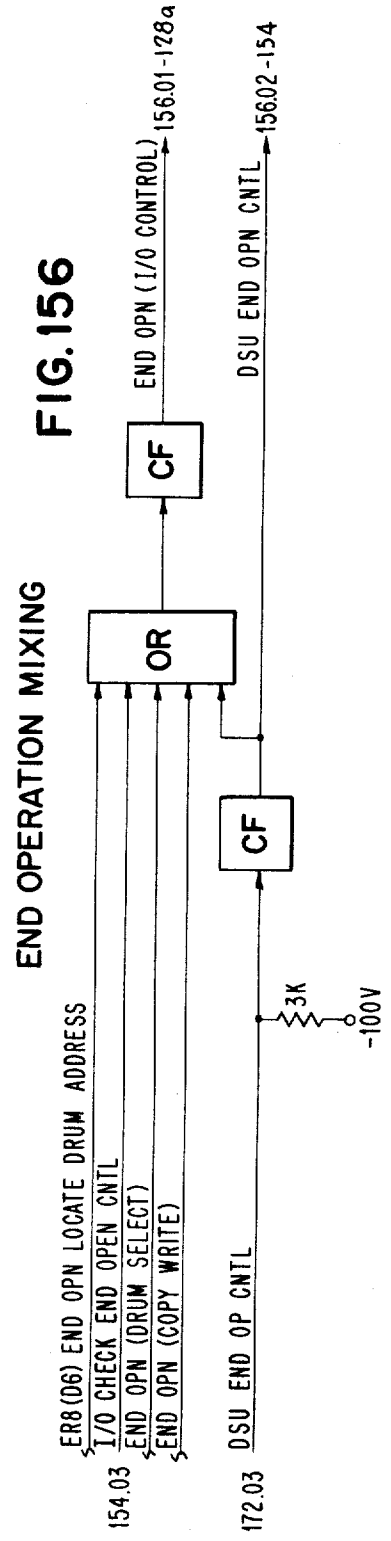
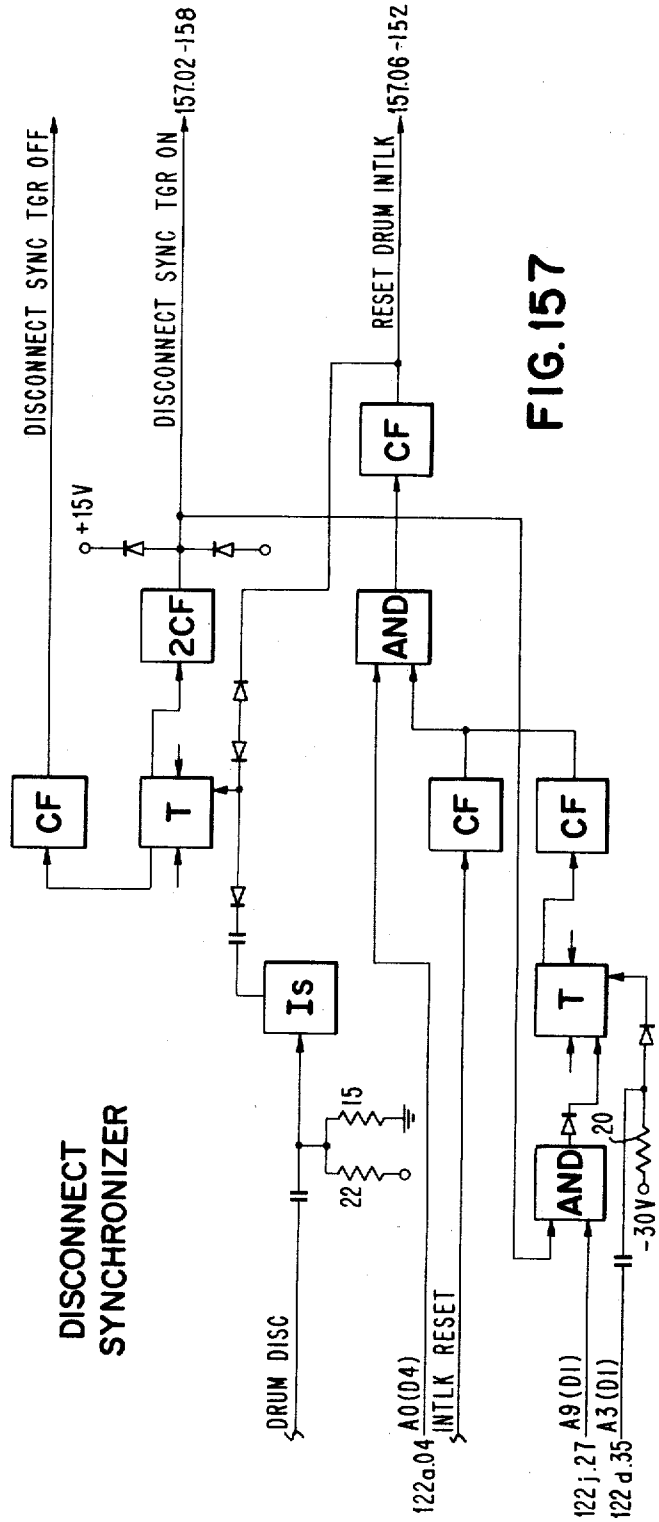


FIG. 157



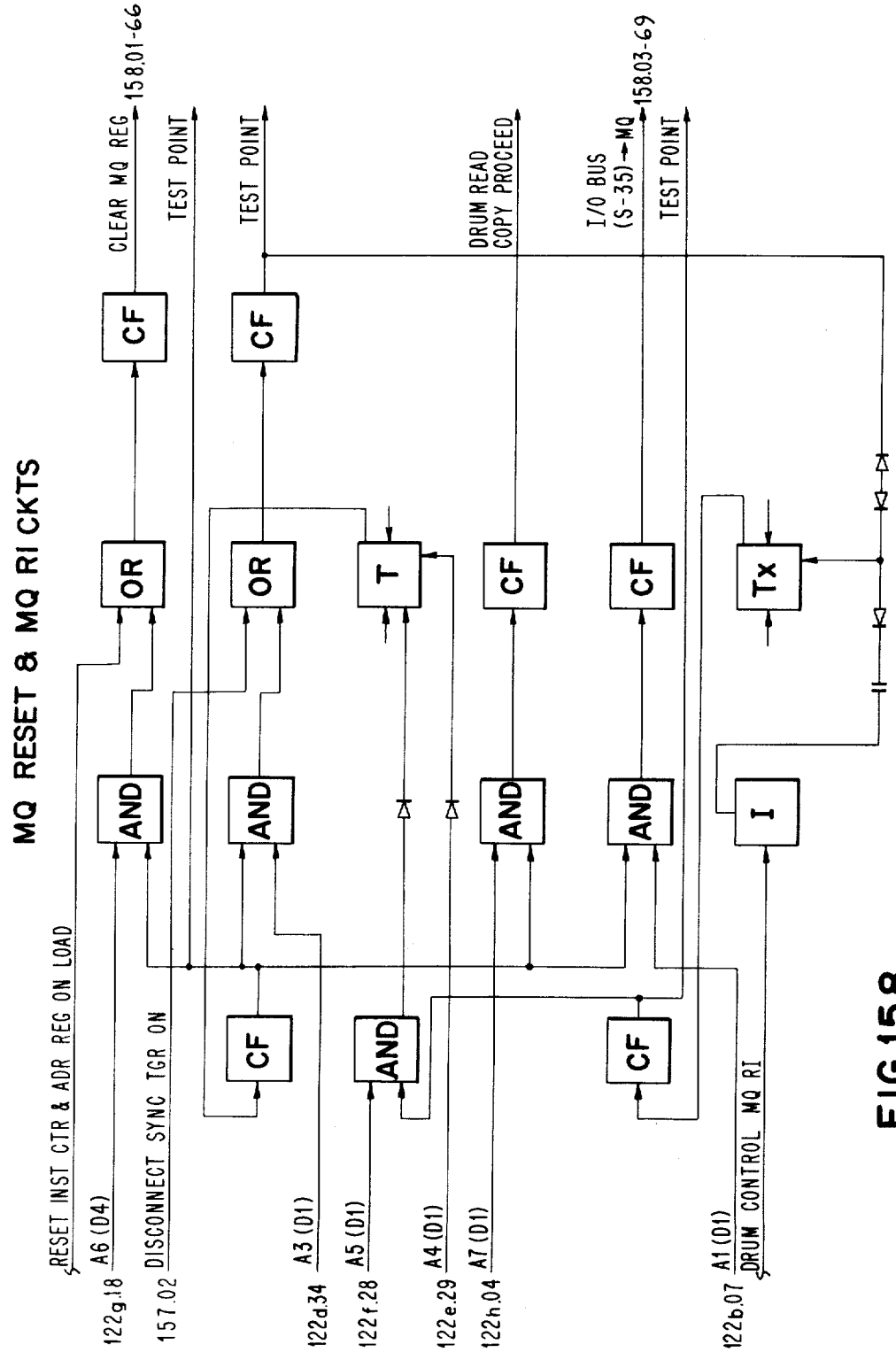
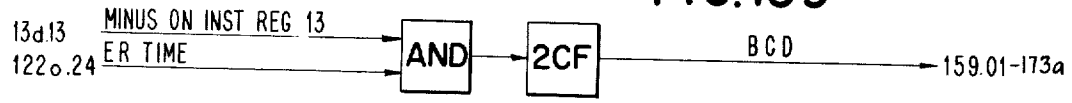

MQ RESET & MQ RI CKTS
RESET INST CTR & ADR REG ON LOAD
A6 (D4)
122g.18
DISCONNECT SYNC TGR ON
157.02
A3 (D1)
122d.34
A5 (D1)
122f.28
A4 (D1)
122e.29
A7 (D1)
122h.04
A1 (D1)
DRUM CONTROL MQ RI
122b.07
AND
OR
CF
T
Tx
I
CLEAR MQ REG
158.01-66
TEST POINT
DRUM READ
COPY PROCEED
I/O BUS
(S-35)→MQ
158.03-69

FIG.158

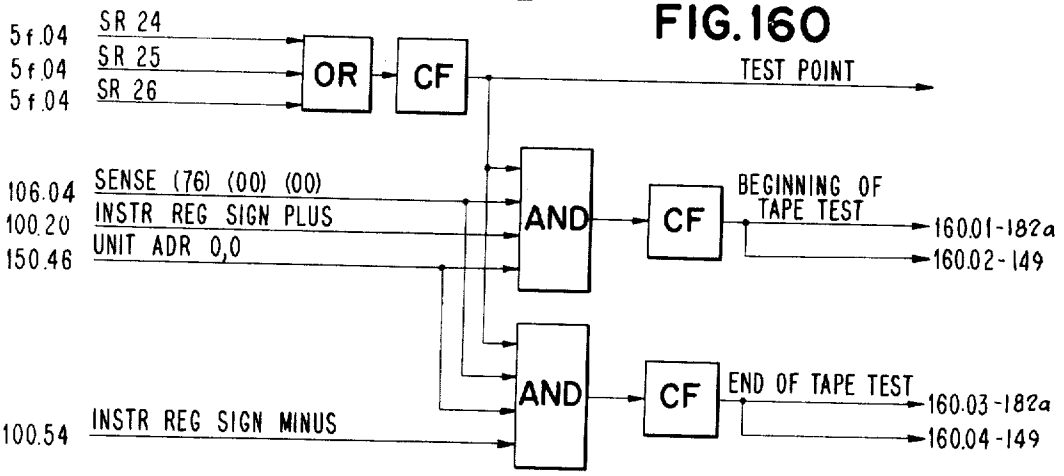
TAPE CONTROL

FIG.159



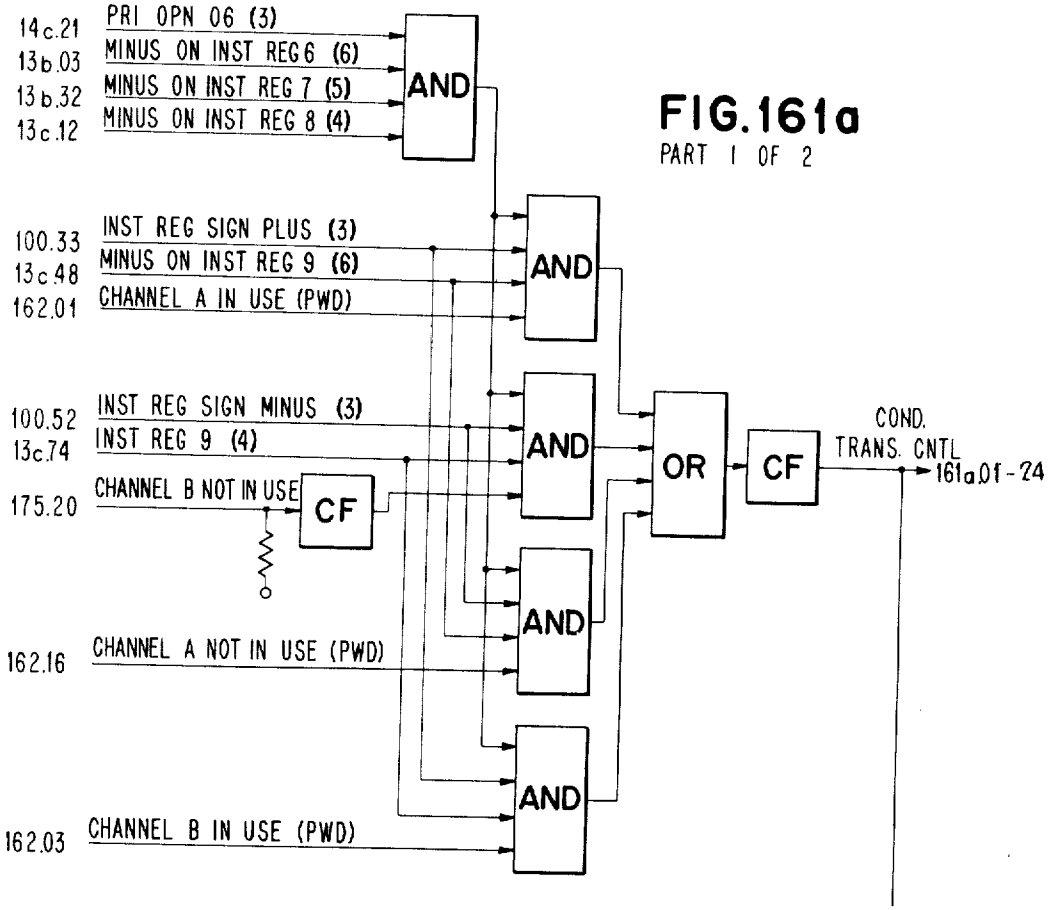
D S U INSTR DECODER

FIG.160



D S U CONDITIONAL TRANSFER

FIG.161a
PART 1 OF 2



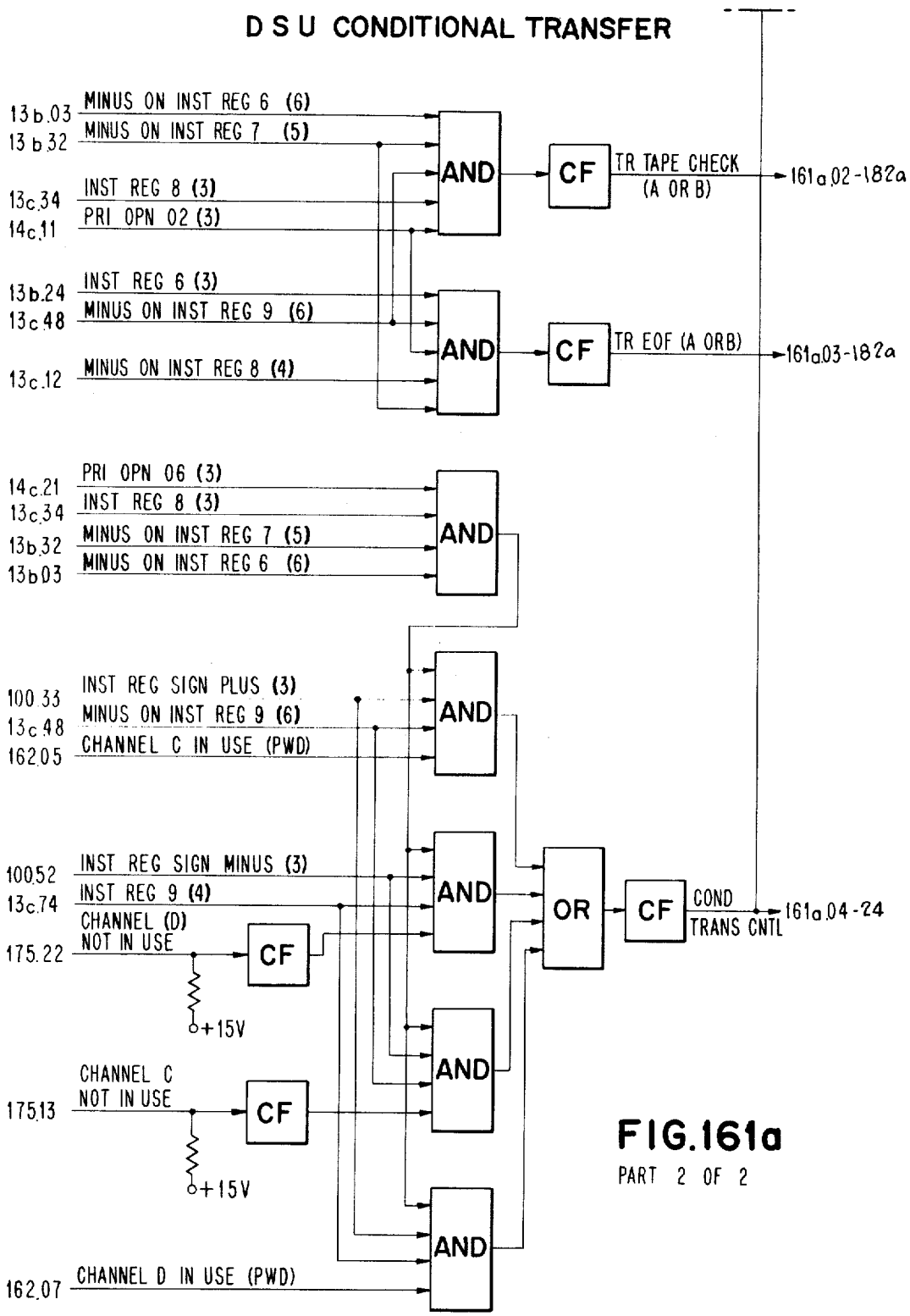
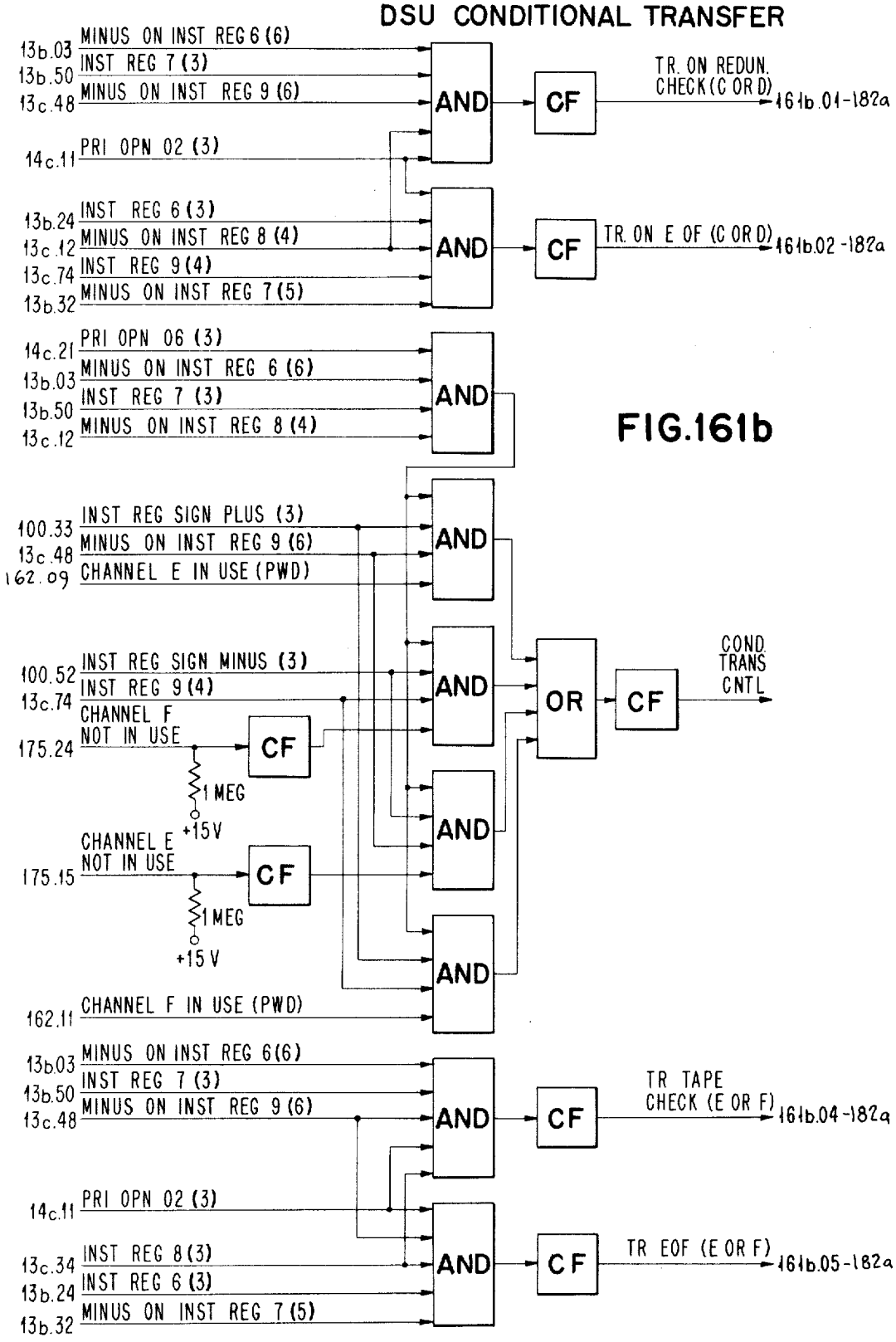


FIG.161a

PART 2 OF 2


DSU CONDITIONAL TRANSFER
13b.03 MINUS ON INST REG 6 (6)
13b.50 INST REG 7 (3)
13c.48 MINUS ON INST REG 9 (6)
AND
CF
TR. ON REDUN. CHECK (C OR D)
161b.01-182a
14c.11 PRI OPN 02 (3)
13b.24 INST REG 6 (3)
13c.12 MINUS ON INST REG 8 (4)
13c.74 INST REG 9 (4)
13b.32 MINUS ON INST REG 7 (5)
AND
CF
TR. ON E OF (C OR D)
161b.02-182a
14c.21 PRI OPN 06 (3)
13b.03 MINUS ON INST REG 6 (6)
13b.50 INST REG 7 (3)
13c.12 MINUS ON INST REG 8 (4)
AND
FIG.161b
100.33 INST REG SIGN PLUS (3)
13c.48 MINUS ON INST REG 9 (6)
162.09 CHANNEL E IN USE (PWD)
AND
100.52 INST REG SIGN MINUS (3)
13c.74 INST REG 9 (4)
CHANNEL F NOT IN USE
175.24
CF
1 MEG
+15V
AND
CHANNEL E NOT IN USE
175.15
CF
1 MEG
+15 V
AND
162.11 CHANNEL F IN USE (PWD)
AND
OR
CF
COND. TRANS CNTL
13b.03 MINUS ON INST REG 6 (6)
13b.50 INST REG 7 (3)
13c.48 MINUS ON INST REG 9 (6)
AND
CF
TR TAPE CHECK (E OR F)
161b.04-182a
14c.11 PRI OPN 02 (3)
13c.34 INST REG 8 (3)
13b.24 INST REG 6 (3)
13b.32 MINUS ON INST REG 7 (5)
AND
CF
TR EOF (E OR F)
161b.05-182a

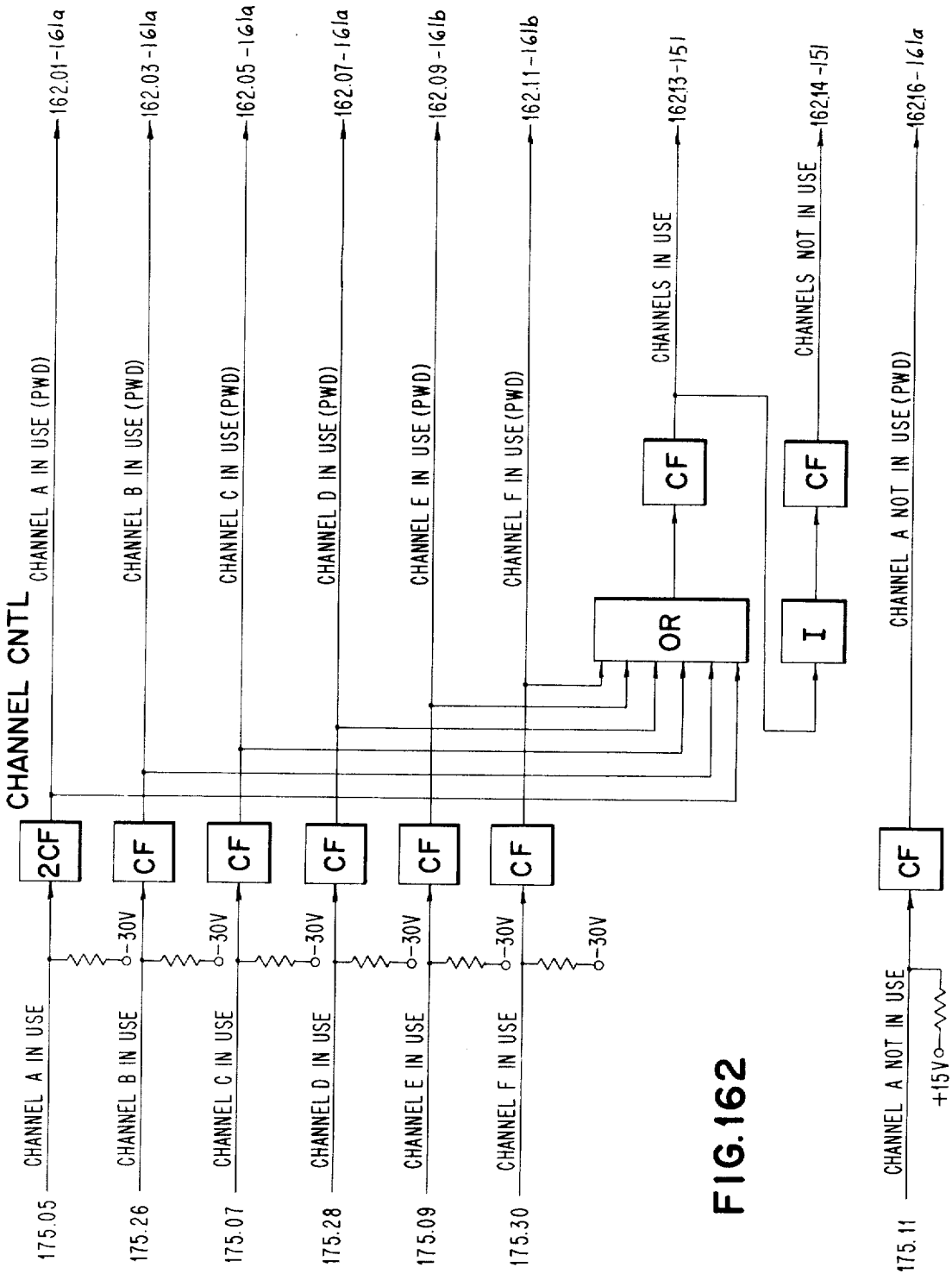

CHANNEL CNTL
CHANNEL A IN USE (PWD)
CHANNEL B IN USE (PWD)
CHANNEL C IN USE (PWD)
CHANNEL D IN USE (PWD)
CHANNEL E IN USE (PWD)
CHANNEL F IN USE (PWD)
162.01-161a
162.03-161a
162.05-161a
162.07-161a
162.09-161b
162.11-161b
2CF
CF
CF
CF
CF
CF
-30V
-30V
-30V
-30V
-30V
-30V
CHANNEL A IN USE
CHANNEL B IN USE
CHANNEL C IN USE
CHANNEL D IN USE
CHANNEL E IN USE
CHANNEL F IN USE
175.05
175.26
175.07
175.28
175.09
175.30
OR
CF
CHANNELS IN USE
16213-151
I
CF
CHANNELS NOT IN USE
16214-151
CHANNEL A NOT IN USE (PWD)
16216-161a
CF
CHANNEL A NOT IN USE
+15V
175.11

FIG.162

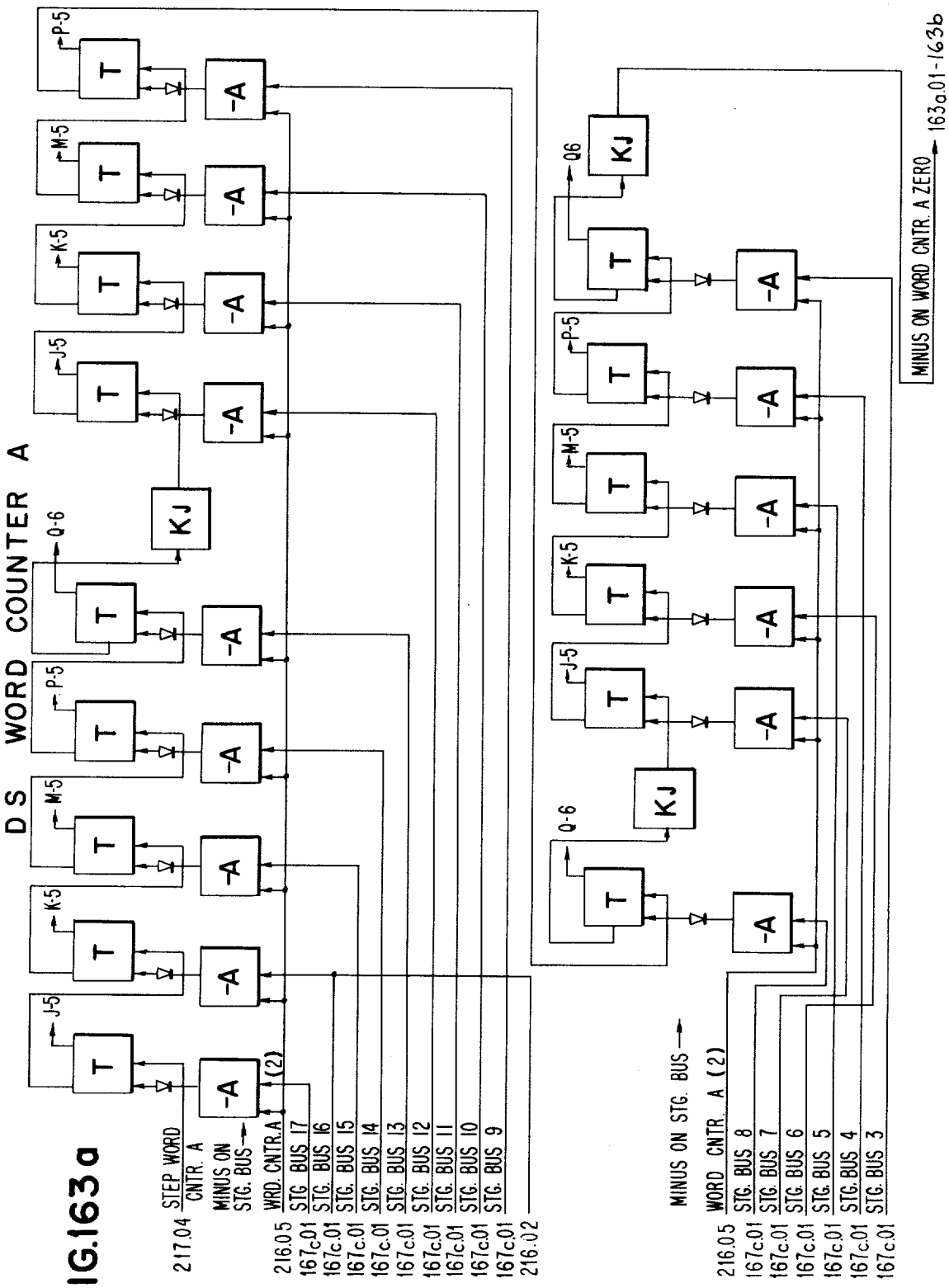

DS WORD COUNTER A
J-5
K-5
M-5
P-5
Q-6
T
-A
KJ
STEP WORD CNTR. A
217.04
MINUS ON STG. BUS
WRD. CNTR. A (2)
216.05
167c.01
STG. BUS 17
STG. BUS 16
STG. BUS 15
STG. BUS 14
STG. BUS 13
STG. BUS 12
STG. BUS 11
STG. BUS 10
STG. BUS 9
216.02
MINUS ON STG. BUS
WORD CNTR. A (2)
STG. BUS 8
STG. BUS 7
STG. BUS 6
STG. BUS 5
STG. BUS 4
STG. BUS 3
MINUS ON WORD CNTR. A ZERO
163a.01-1636

FIG.163a

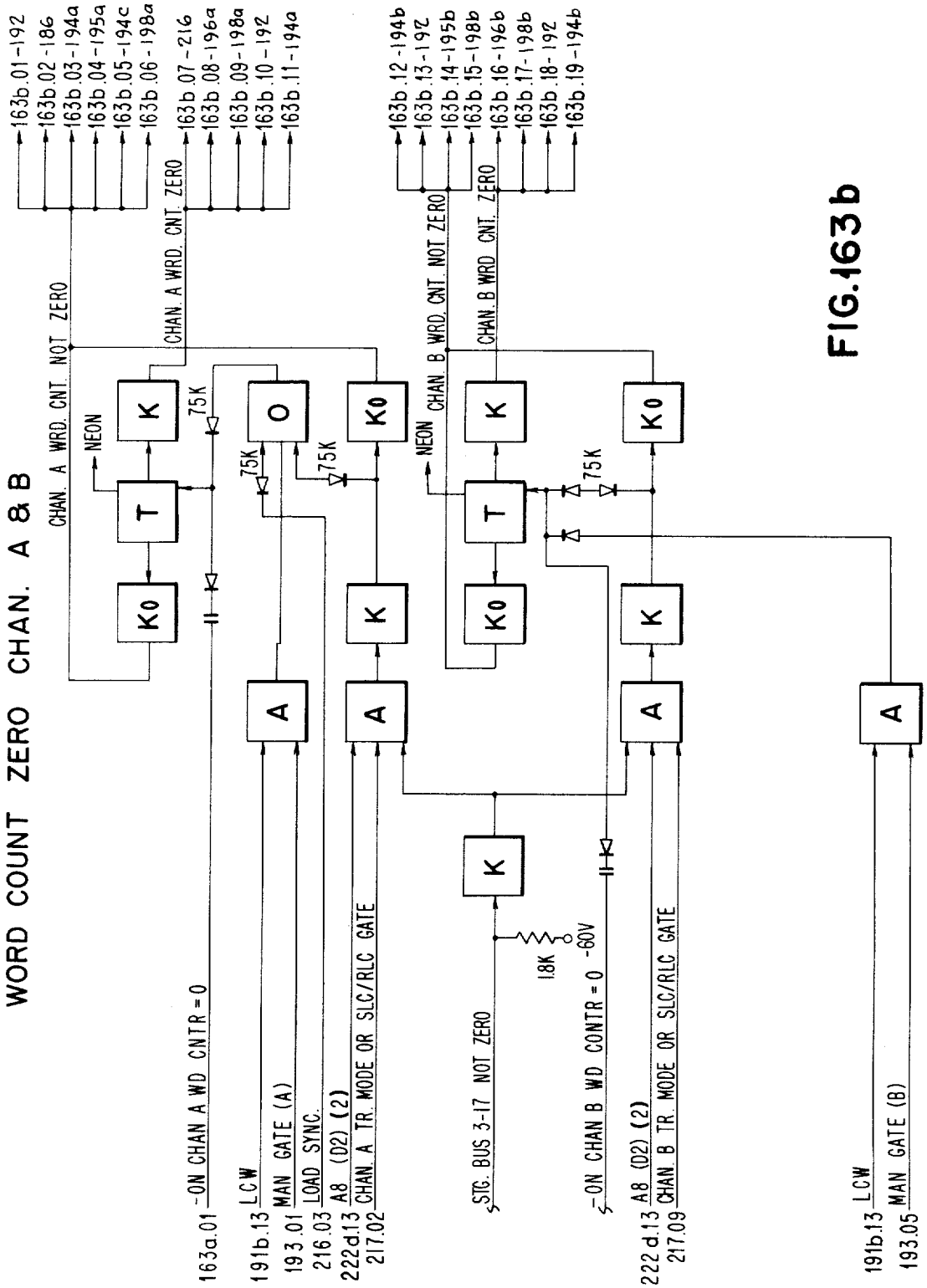
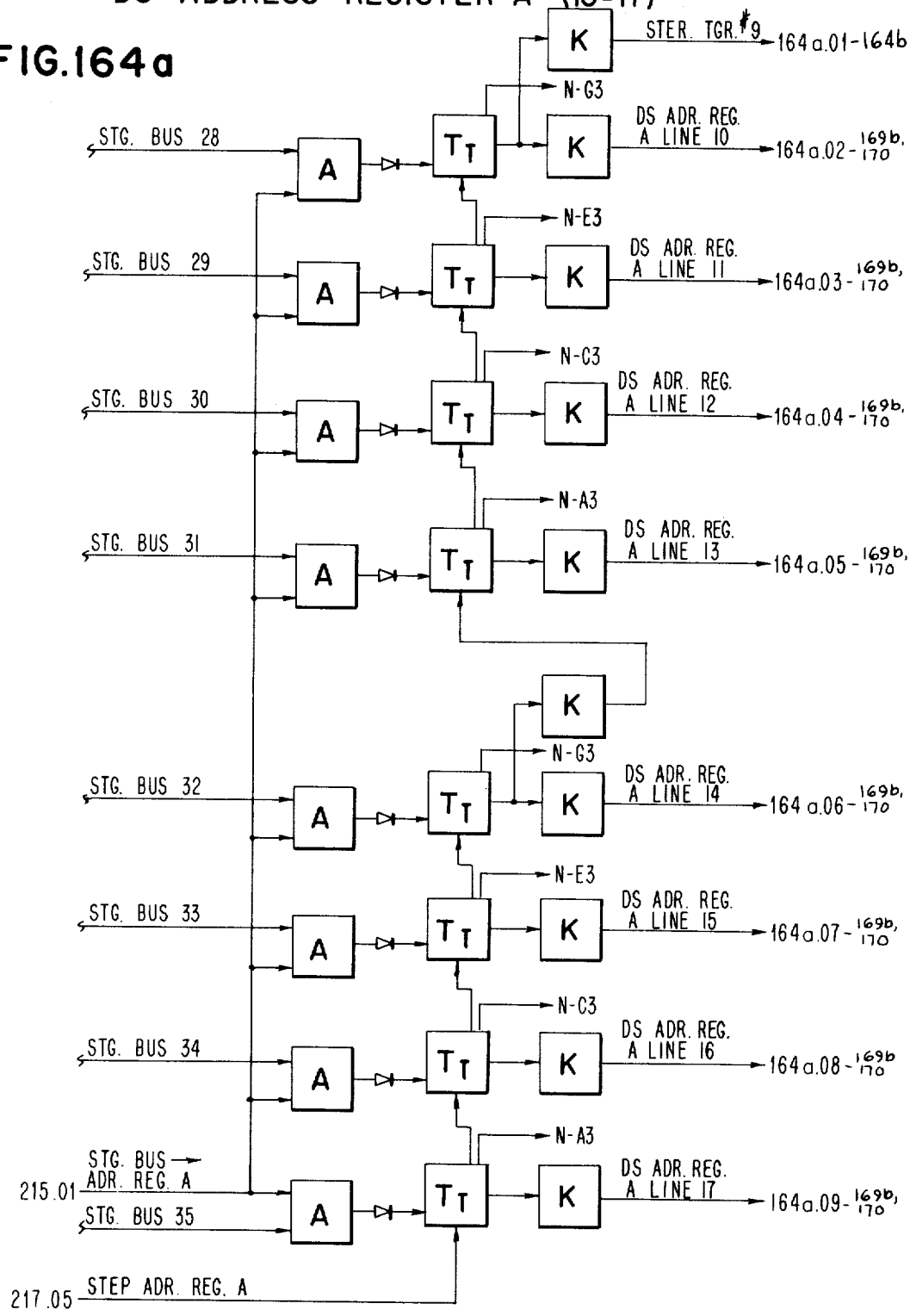

WORD COUNT ZERO CHAN. A & B
CHAN. A WRD. CNT. NOT ZERO
CHAN. A WRD. CNT. ZERO
CHAN. B WRD. CNT. NOT ZERO
CHAN. B WRD. CNT. ZERO
NEON
75K
1.8K
-60V
K
T
K0
O
A
163b.01-192
163b.02-186
163b.03-194a
163b.04-195a
163b.05-194c
163b.06-198a
163b.07-216
163b.08-196a
163b.09-198a
163b.10-192
163b.11-194a
163b.12-194b
163b.13-192
163b.14-195b
163b.15-198b
163b.16-196b
163b.17-198b
163b.18-192
163b.19-194b
163a.01 -ON CHAN A WD CNTR = 0
191b.13 LCW
193.01 MAN GATE (A)
216.03 LOAD SYNC.
222d.13 A8 (D2) (2)
217.02 CHAN. A TR. MODE OR SLC/RLC GATE
STG. BUS 3-17 NOT ZERO
-ON CHAN B WD CONTR = 0
222d.13 A8 (D2) (2)
217.09 CHAN B TR. MODE OR SLC/RLC GATE
191b.13 LCW
193.05 MAN GATE (B)

FIG.163b

DS ADDRESS REGISTER A (10-17)

FIG.164a



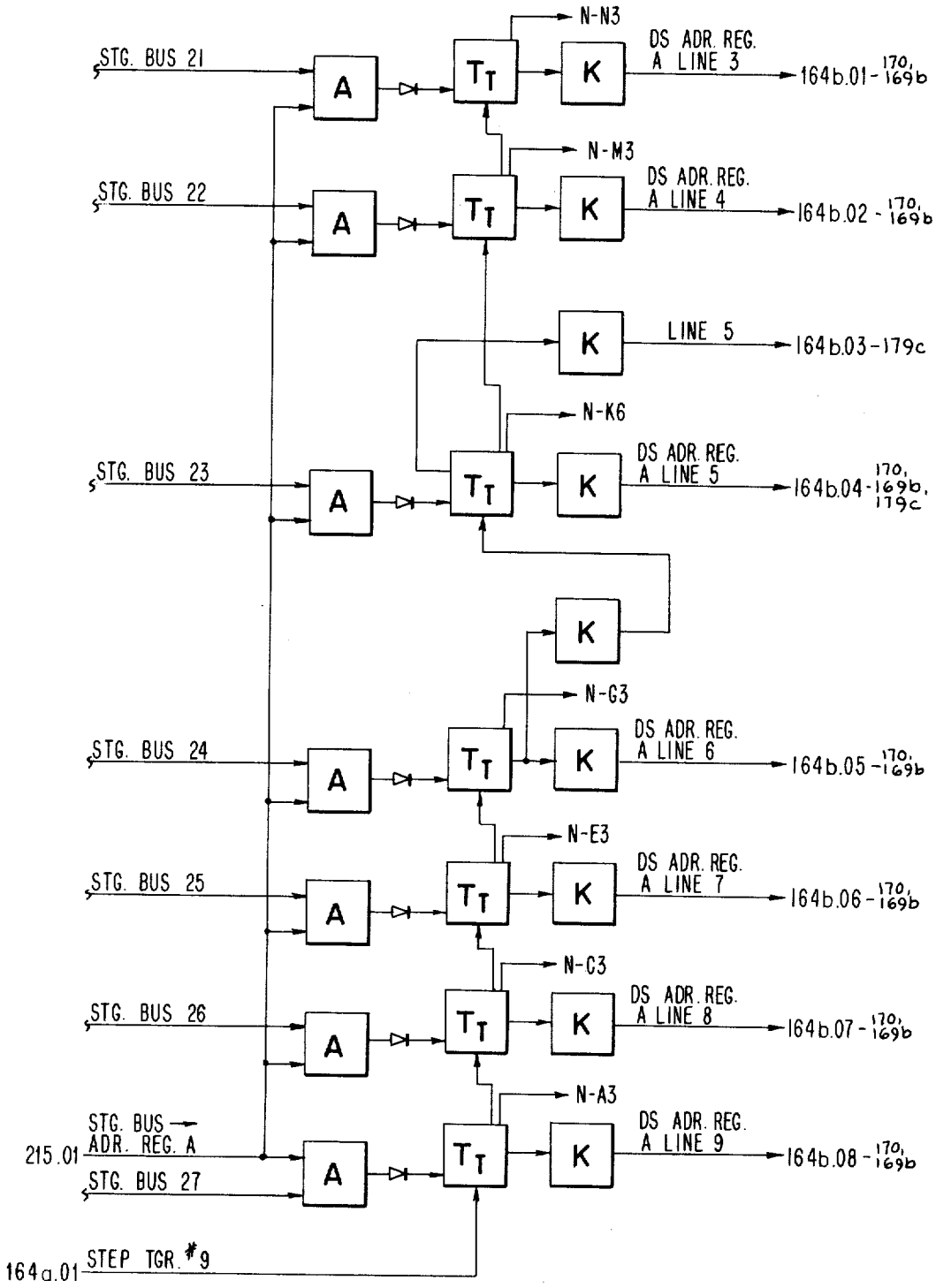
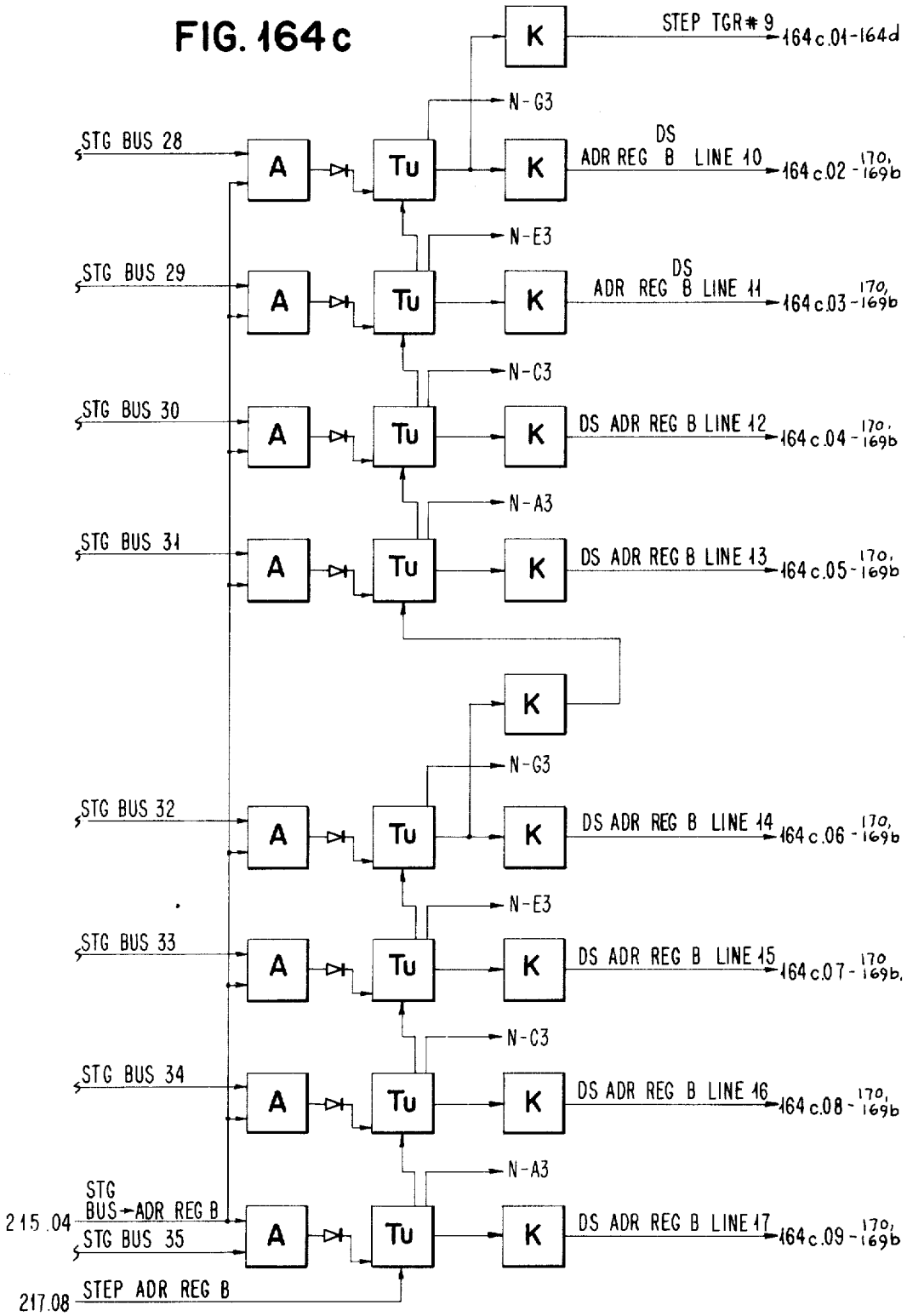

DS ADDRESS REGISTER A (2-9)
STG. BUS 21
STG. BUS 22
STG. BUS 23
STG. BUS 24
STG. BUS 25
STG. BUS 26
STG. BUS ADR. REG. A
215.01
STG. BUS 27
164a.01
STEP TGR. #9
A
TT
K
N-N3
N-M3
N-K6
N-G3
N-E3
N-C3
N-A3
DS ADR. REG. A LINE 3
DS ADR. REG. A LINE 4
LINE 5
DS ADR. REG. A LINE 5
DS ADR. REG. A LINE 6
DS ADR. REG. A LINE 7
DS ADR. REG. A LINE 8
DS ADR. REG. A LINE 9
164b.01-170, 169b
164b.02-170, 169b
164b.03-179c
164b.04-170, 169b, 179c
164b.05-170, 169b
164b.06-170, 169b
164b.07-170, 169b
164b.08-170, 169b

FIG. 164b

DS ADDRESS REGISTER B (10-17)

FIG. 164c



DS ADDRESS REG. B (2-9)

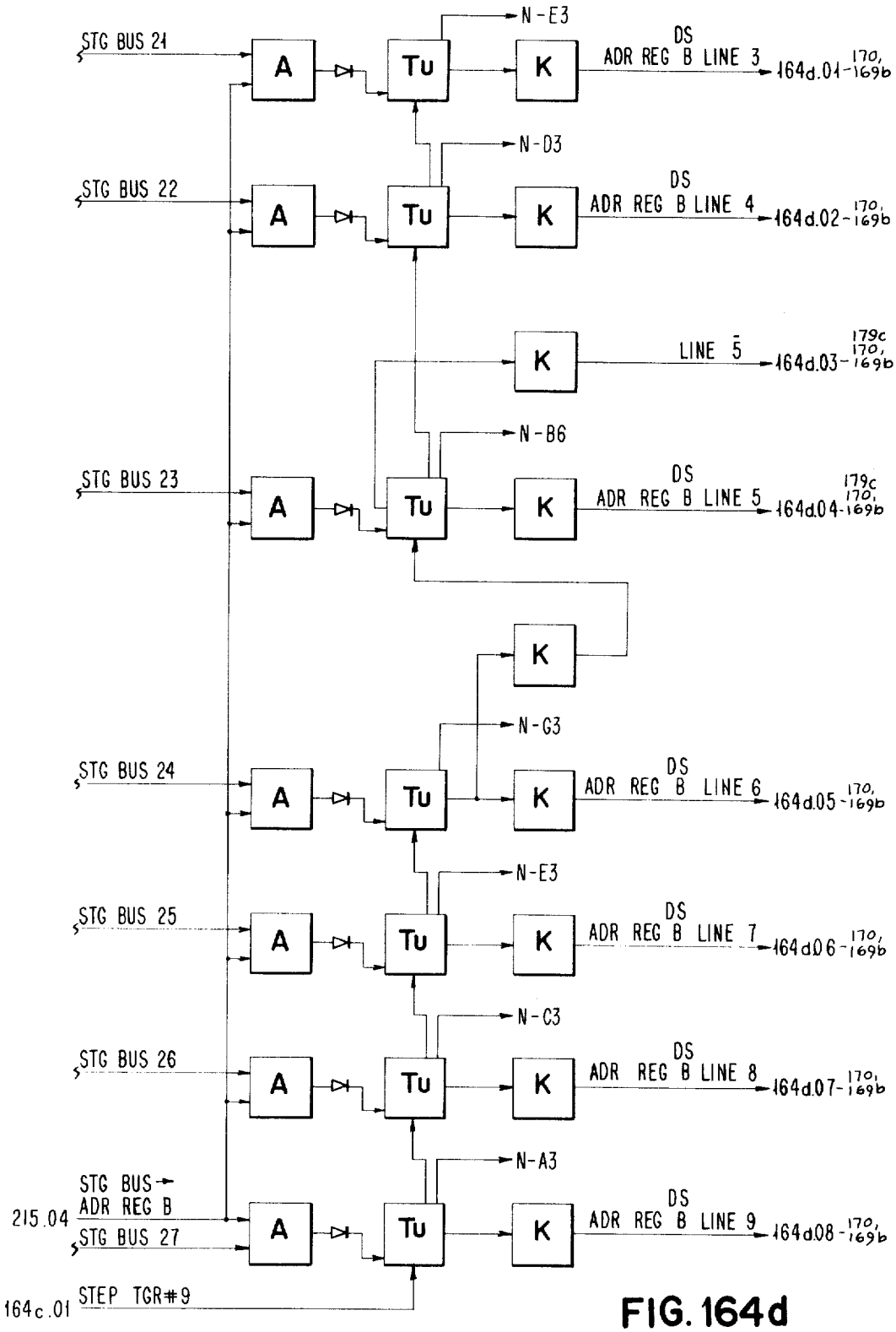


FIG. 164d

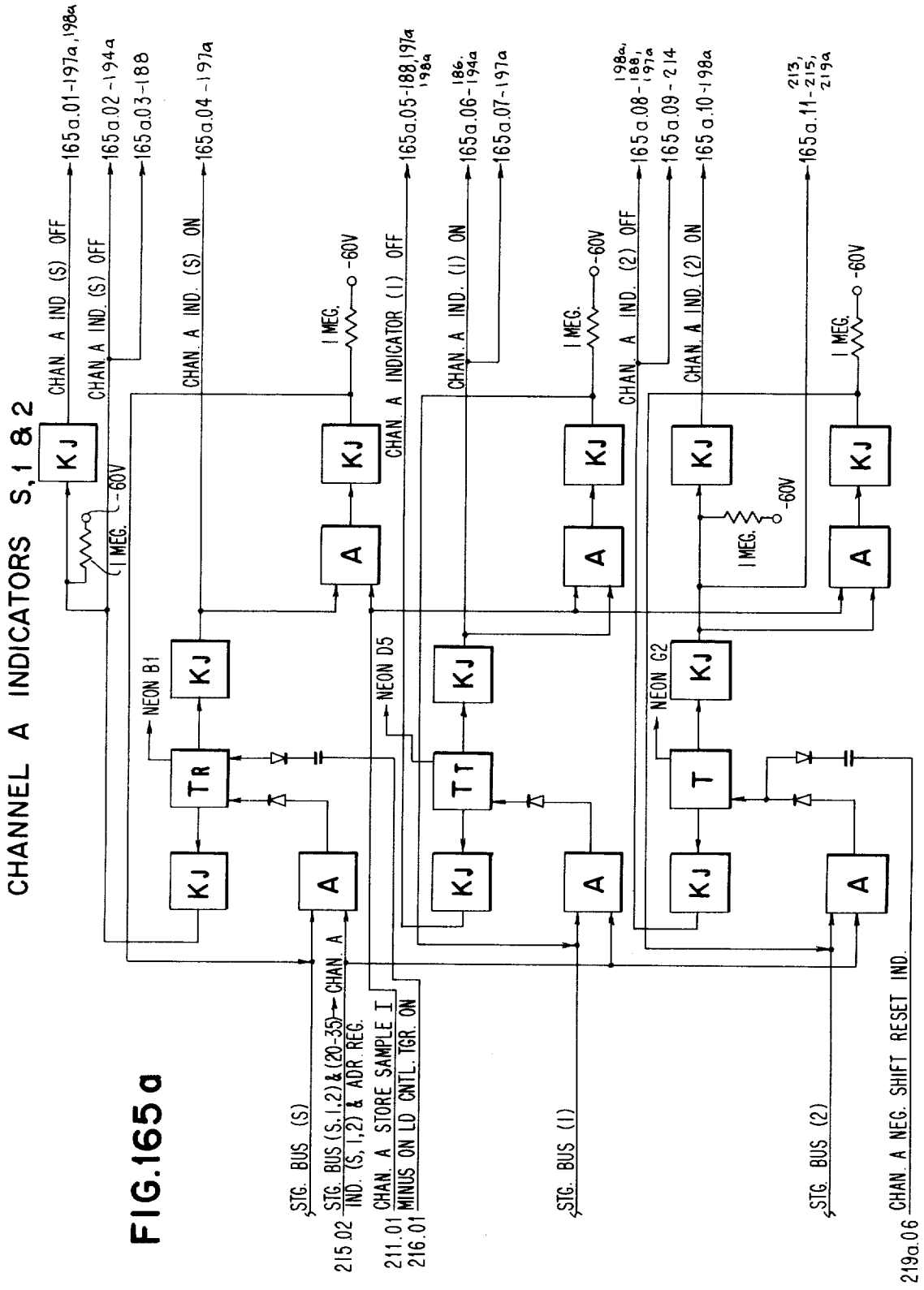

CHANNEL A INDICATORS S,1 & 2
CHAN. A IND. (S) OFF
CHAN. A IND. (S) OFF
CHAN. A IND. (S) ON
CHAN. A INDICATOR (1) OFF
CHAN. A IND. (1) ON
CHAN. A IND. (2) OFF
CHAN. A IND. (2) ON
1 MEG.
-60V
NEON B1
NEON D5
NEON G2
STG. BUS (S)
STG. BUS (S,1,2) & (20-35) → CHAN. A IND. (S,1,2) & ADR. REG.
CHAN. A STORE SAMPLE I
MINUS ON LD CNTL. TGR. ON
STG. BUS (1)
STG. BUS (2)
CHAN. A NEG. SHIFT RESET IND.
KJ
A
TR
TT
T

FIG.165a

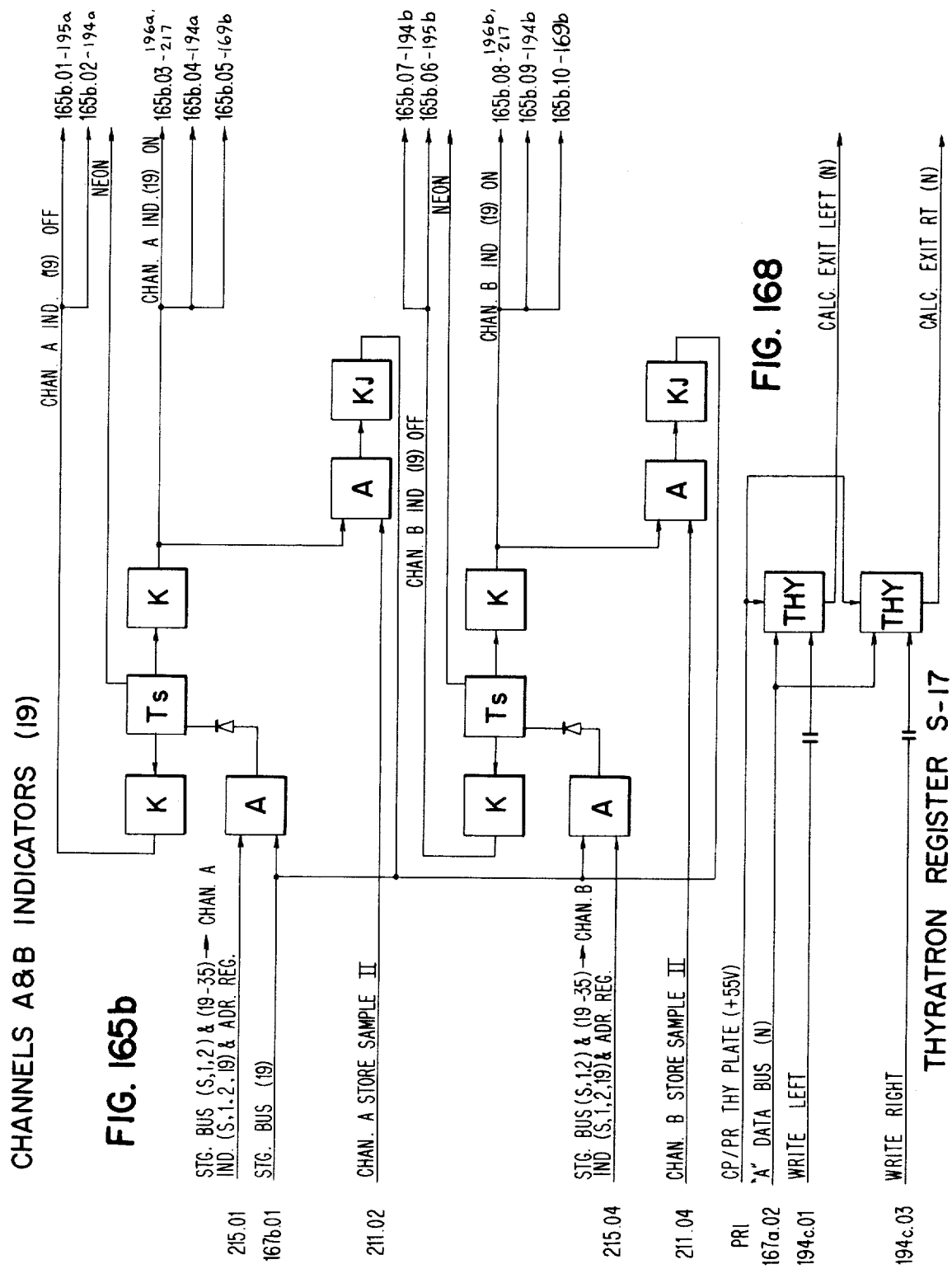
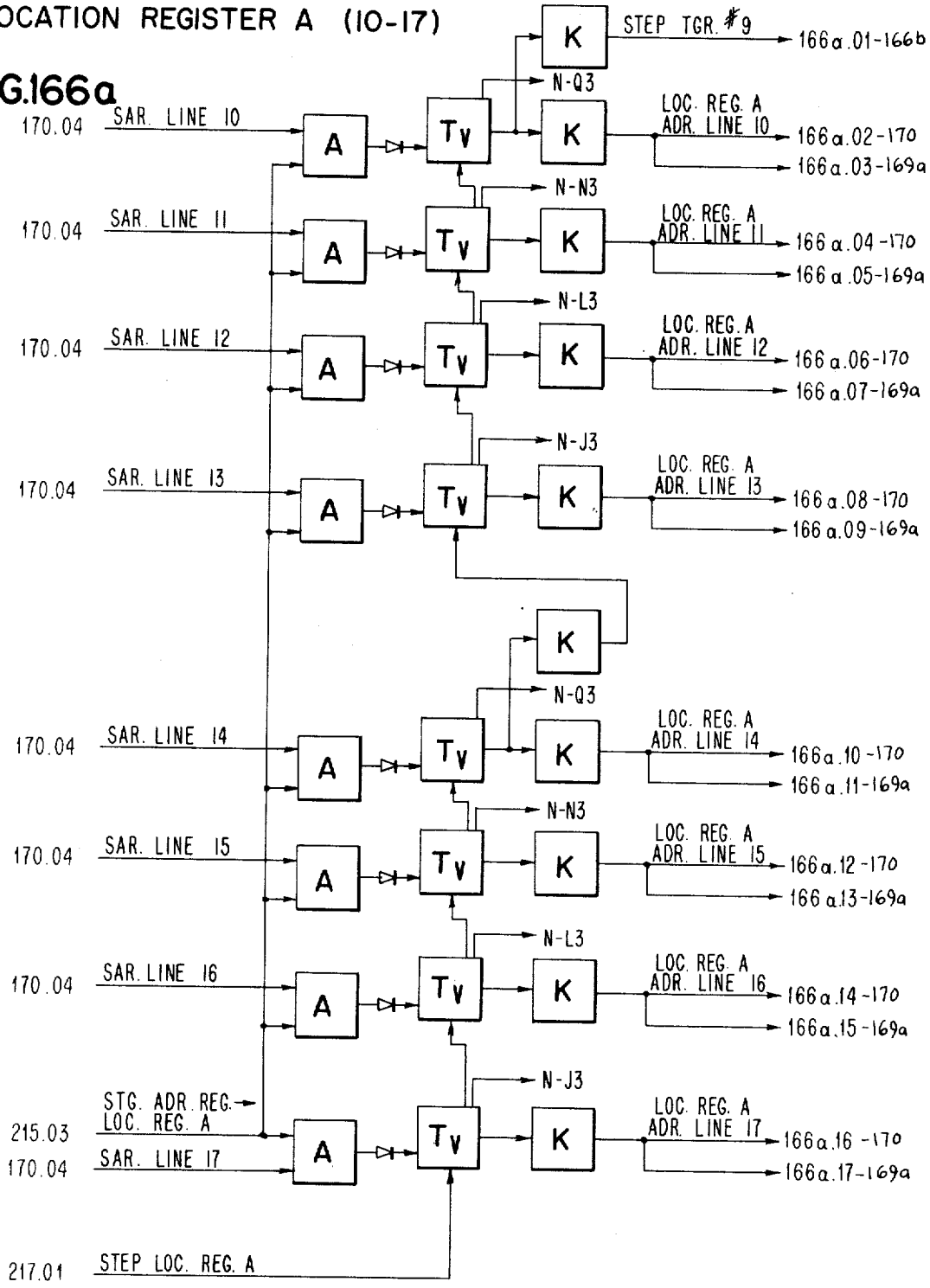


FIG. 165b

FIG. 168

LOCATION REGISTER A (10-17)

FIG.166a



LOCATION REGISTER A (2-9)

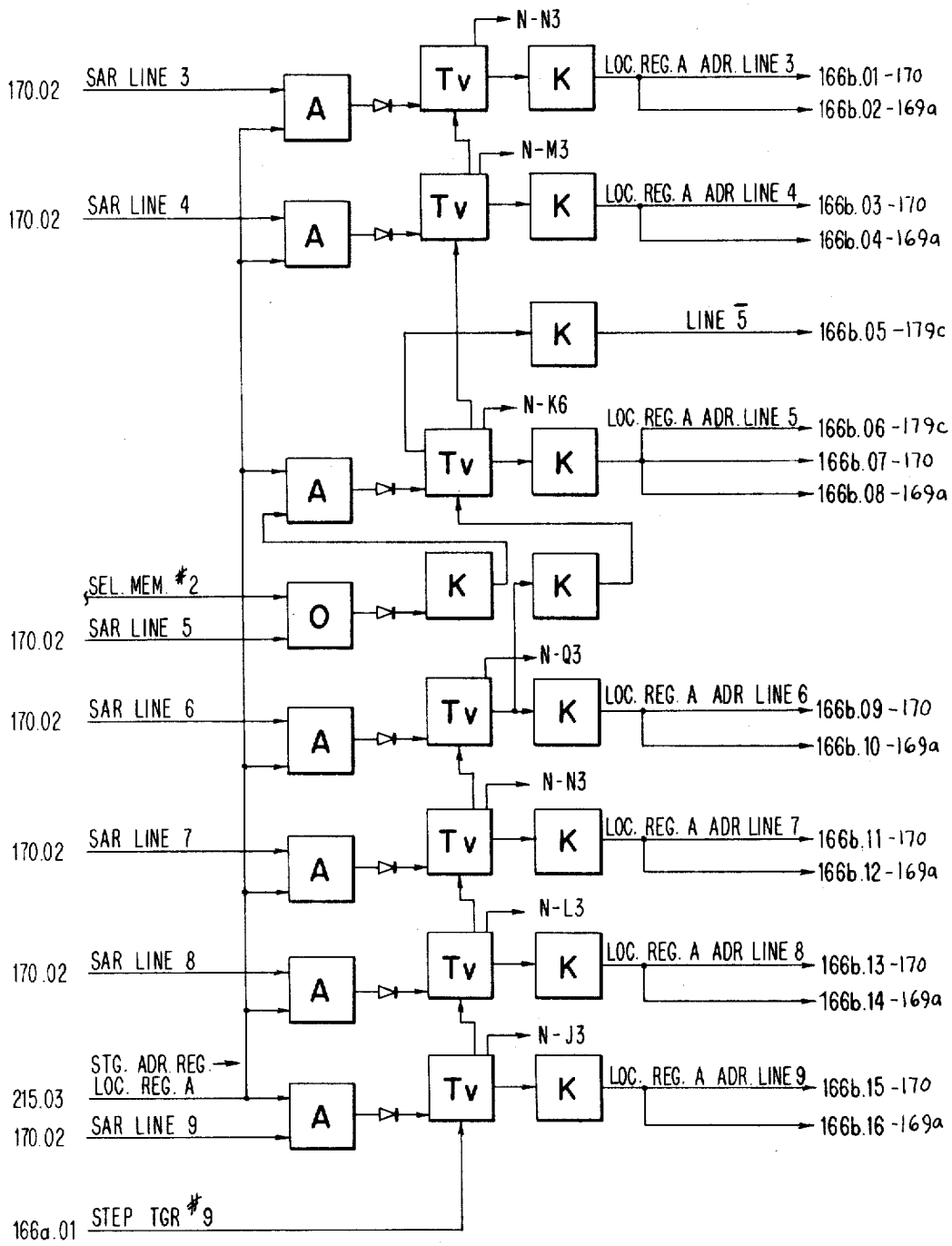
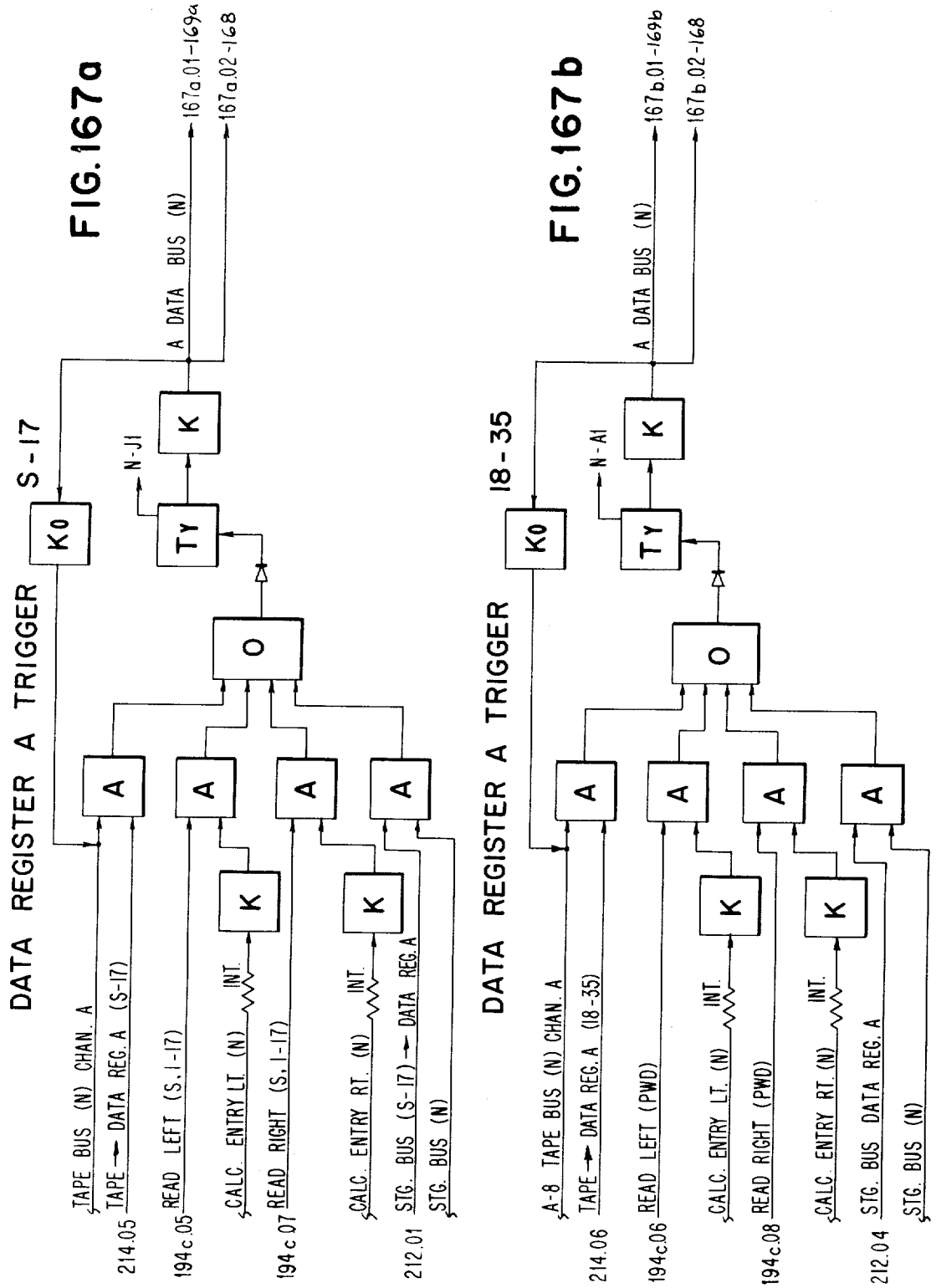


FIG. 166b


FIG. 167a
DATA REGISTER A TRIGGER S-17
K0
TY
N-J1
K
A DATA BUS (N)
167a.01-169a
167a.02-168
O
A
K
TAPE BUS (N) CHAN. A
214.05 TAPE → DATA REG. A (S-17)
194c.05 READ LEFT (S,1-17)
CALC. ENTRY LT. (N)
INT.
194c.07 READ RIGHT (S,1-17)
CALC. ENTRY RT. (N)
INT.
212.01 STG. BUS (S-17) → DATA REG. A
STG. BUS (N)
FIG. 167b
DATA REGISTER A TRIGGER 18-35
K0
TY
N-A1
K
A DATA BUS (N)
167b.01-169b
167b.02-168
O
A
K
A-8 TAPE BUS (N) CHAN. A
214.06 TAPE → DATA REG. A (18-35)
194c.06 READ LEFT (PWD)
CALC. ENTRY LT. (N)
INT.
194c.08 READ RIGHT (PWD)
CALC. ENTRY RT. (N)
INT.
212.04 STG. BUS DATA REG. A
STG. BUS (N)

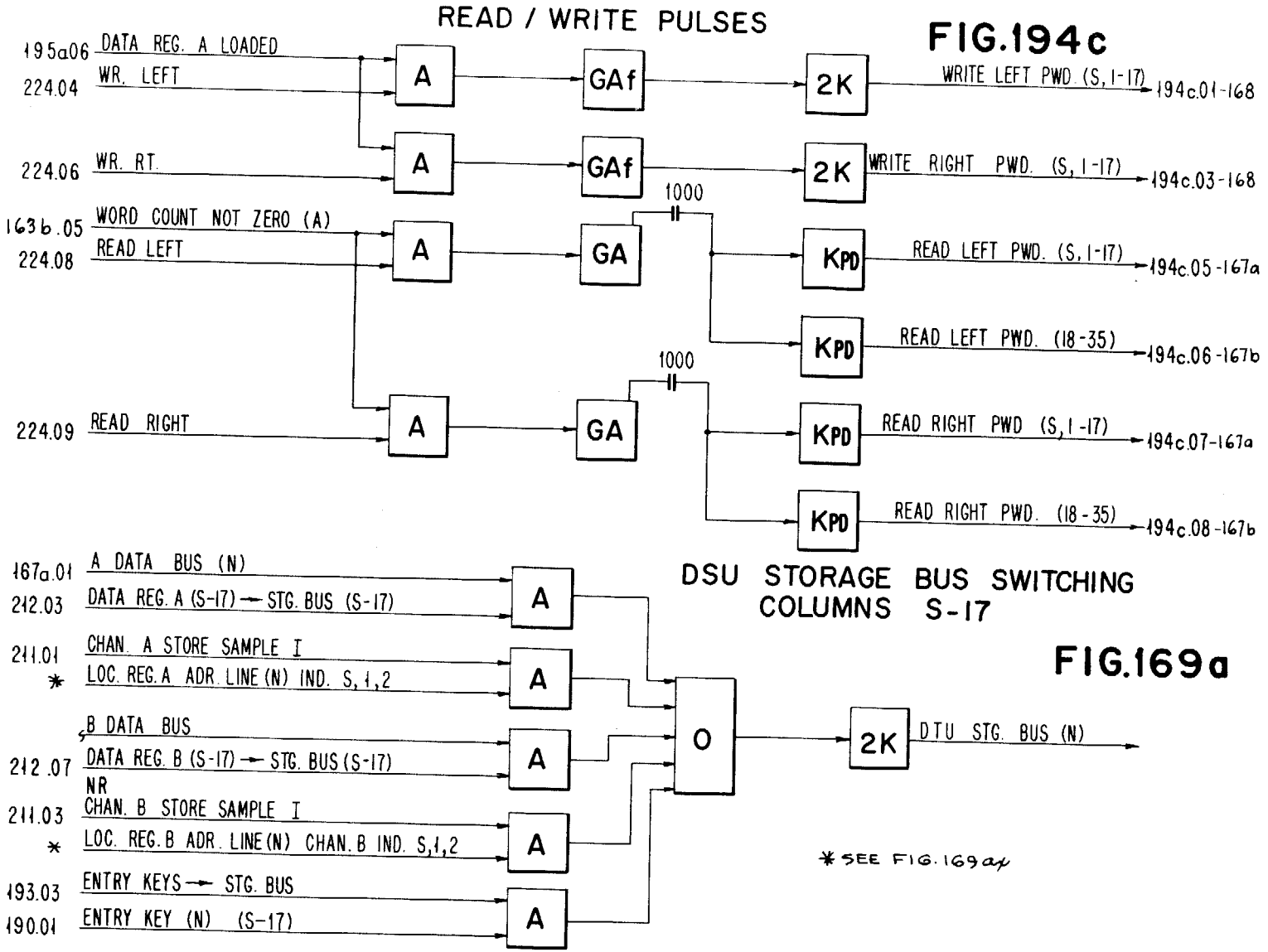

READ / WRITE PULSES
FIG.194c
195a06 DATA REG. A LOADED
224.04 WR. LEFT
224.06 WR. RT.
163b.05 WORD COUNT NOT ZERO (A)
224.08 READ LEFT
224.09 READ RIGHT
A
GAf
GA
1000
2K
KPD
WRITE LEFT PWD. (S,1-17) 194c.01-168
WRITE RIGHT PWD. (S,1-17) 194c.03-168
READ LEFT PWD. (S,1-17) 194c.05-167a
READ LEFT PWD. (18-35) 194c.06-167b
READ RIGHT PWD (S,1-17) 194c.07-167a
READ RIGHT PWD. (18-35) 194c.08-167b
DSU STORAGE BUS SWITCHING
COLUMNS S-17
FIG.169a
167a.01 A DATA BUS (N)
212.03 DATA REG. A (S-17) → STG. BUS (S-17)
211.01 CHAN. A STORE SAMPLE I
* LOC. REG. A ADR. LINE (N) IND. S,1,2
B DATA BUS
212.07 DATA REG. B (S-17) → STG. BUS (S-17)
NR
211.03 CHAN. B STORE SAMPLE I
* LOC. REG. B ADR. LINE (N) CHAN. B IND. S,1,2
193.03 ENTRY KEYS → STG. BUS
190.01 ENTRY KEY (N) (S-17)
O
DTU STG. BUS (N)
* SEE FIG. 169a

FIG. 169ax

DTU STG BUS (N)	LOC REG ADR LINE REG A-REG B (N)	FIG. NO. REG A	FIG. NO. REG B
S	IND. S	165a	
1	IND. 1	165a	
2	IND. 2	165a	
3	3	166b	166d
4	4	166b	166d
5	5	166b	166d
6	6	166b	166d
7	7	166b	166d
8	8	166b	166d
9	9	166b	166d
10	10	166a	166c
11	11	166a	166c
12	12	166a	166c
13	13	166a	166c
14	14	166a	166c
15	15	166a	166c
16	16	166a	166c
17	17	166a	166c

FIG. 169bx

DTU STG BUS (N)	ADR REG LINE REG A-REG B (N)	FIG. NO. REG A	FIG. NO. REG B
18			
19	IND. 19	165b	165b
20			
21	3	164b	164d
22	4	164b	164d
23	5	164b	164d
24	6	164b	164d
25	7	164b	164d
26	8	164b	164d
27	9	164b	164d
28	10	164a	164c
29	11	164a	164c
30	12	164a	164c
31	13	164a	164c
32	14	164a	164c
33	15	164a	164c
34	16	164a	164c
35	17	164a	164c

FIG. 170a

N	FIG. NO. △	FIG. NO. □	FIG. NO. ⊠	FIG. NO. ⊗
17	166a	166c	164a	164c
16	166a	166c	164a	164c
15	166a	166c	164a	164c
14	166a	166c	164a	164c
13	166a	166c	164a	164c
12	166a	166c	164a	164c
11	166a	166c	164a	164c
10	166a	166c	164a	164c
09	166b	166d	164b	164d
08	166b	166d	164b	164d
07	166b	166d	164b	164d
06	166b	166d	164b	164d
05	166b	166d	164b	164d
04	166b	166d	164b	164d
03	166b	166d	164b	164d

FIG. 231a

CHANNEL	LINE REG N FIG. NO.	LINE REG $\overline{N}$ FIG. NO.
C	232a	232a
B	232b, 232c	232b
A	232a, 232b, 232c	232a, 232b
8	232c	232c
4	232c, 232d	
2	232c	232c
1	232c, 232d	

DSU STORAGE BUS SWITCHING COLUMNS 18-35

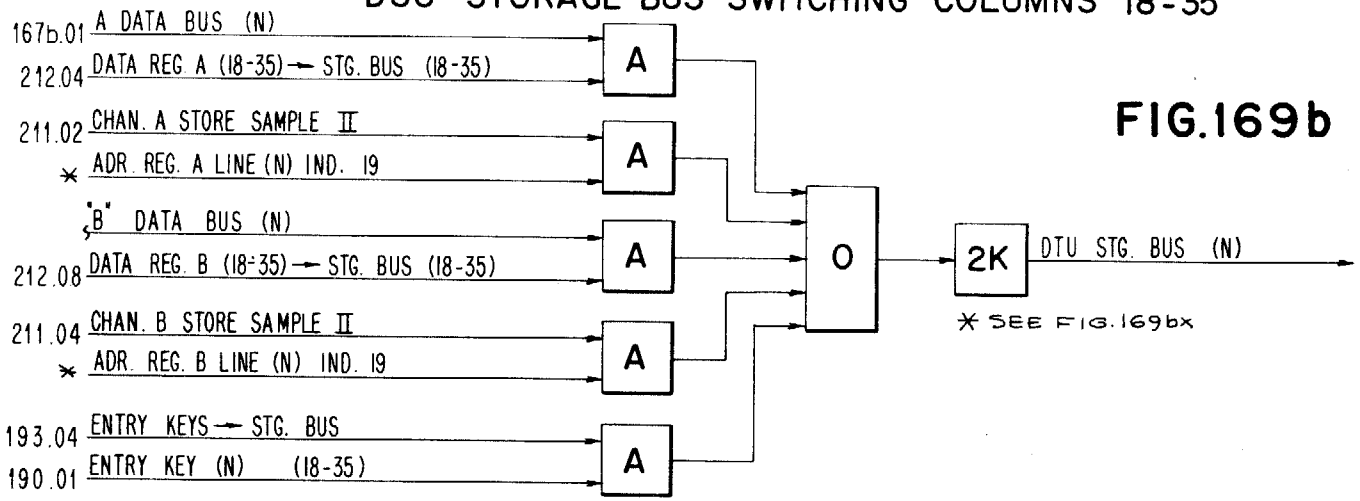


FIG.169b

DSU ADDRESS SWITCHING

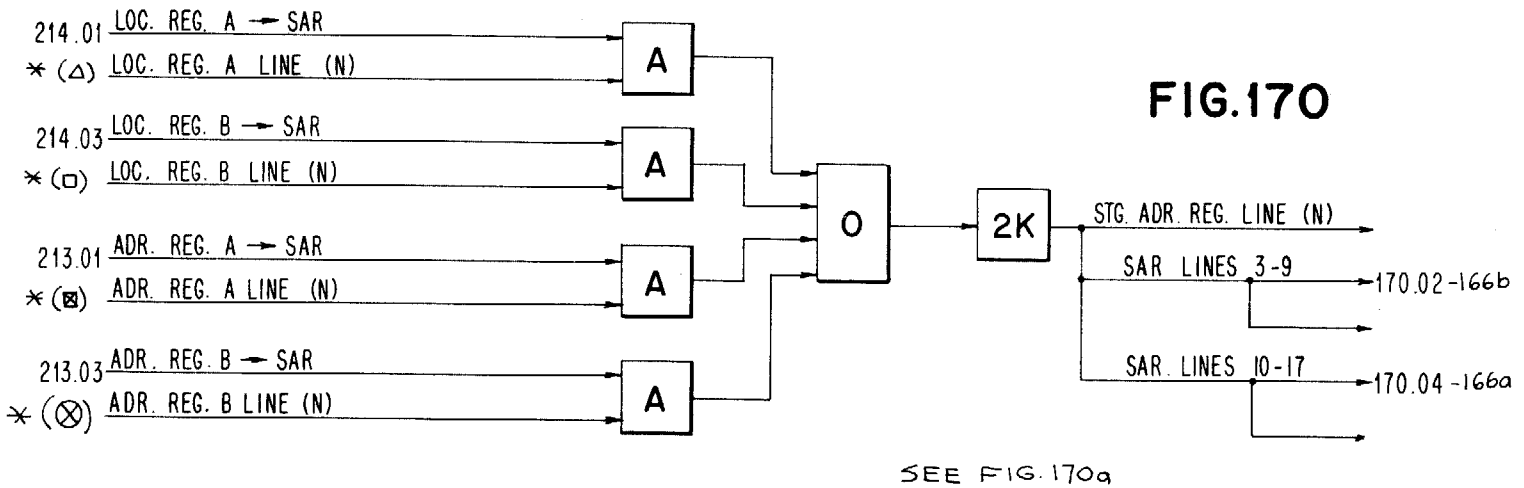
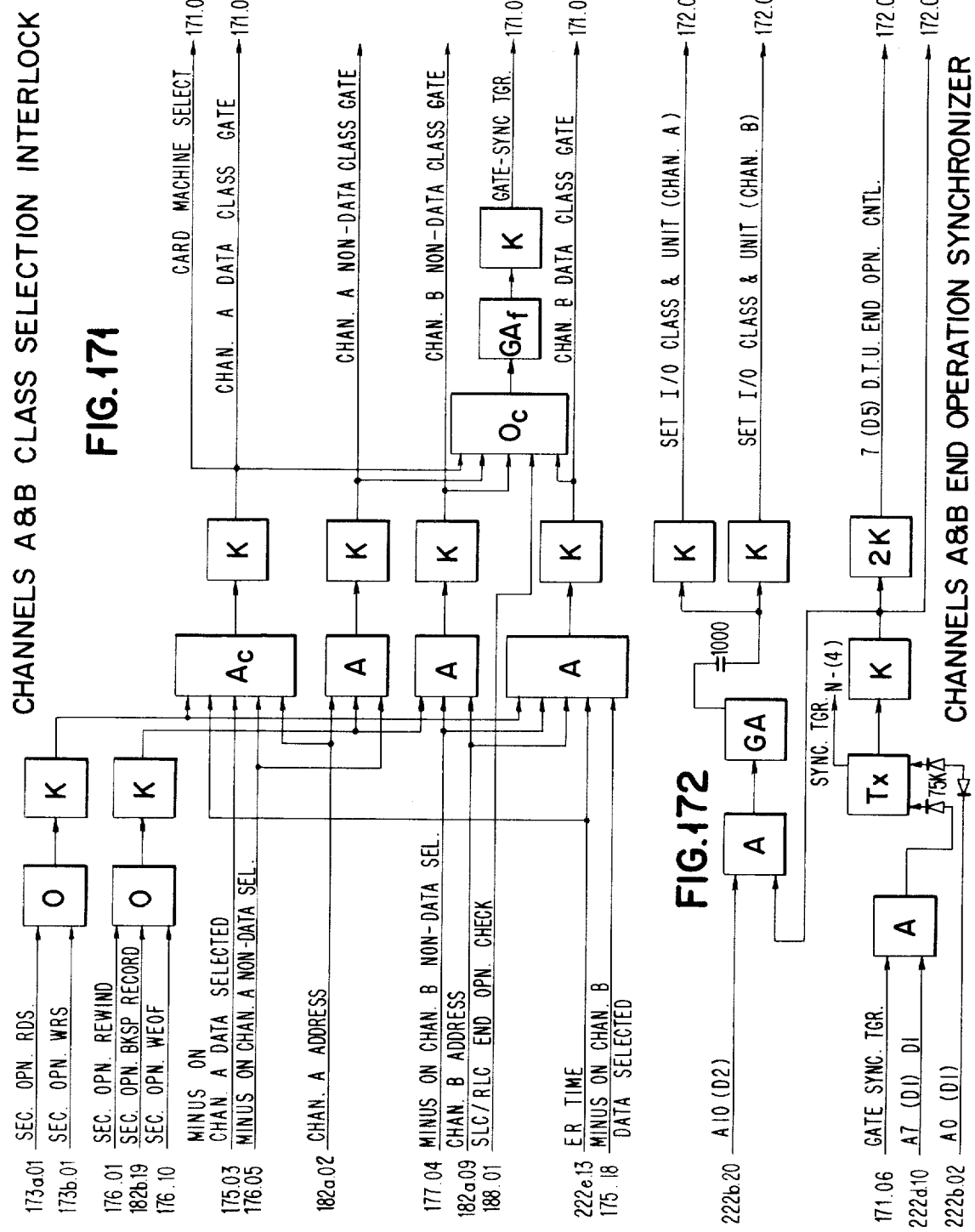


FIG.170

SEE FIG. 170a


CHANNELS A&B CLASS SELECTION INTERLOCK
173a.01 SEC. OPN. RDS.
173b.01 SEC. OPN. WRS
176.01 SEC. OPN. REWIND
182b.19 SEC. OPN. BKSP RECORD
176.10 SEC. OPN. WEOF
175.03 MINUS ON CHAN. A DATA SELECTED
176.05 MINUS ON CHAN. A NON-DATA SEL.
182a.02 CHAN. A ADDRESS
177.04 MINUS ON CHAN. B NON-DATA SEL.
182a.09 CHAN. B ADDRESS
188.01 SLC/RLC END OPN. CHECK
222e.13 E.R. TIME
175.18 MINUS ON CHAN. B DATA SELECTED
O
K
Ac
A
Oc
GAf
CARD MACHINE SELECT
171.01-178
CHAN. A DATA CLASS GATE
171.02-219a
CHAN. A NON-DATA CLASS GATE
CHAN. B NON-DATA CLASS GATE
GATE-SYNC TGR.
171.06-172
CHAN. B DATA CLASS GATE
171.07-219b
FIG.171
222b.20 A10 (D2)
GA
÷1000
SET I/O CLASS & UNIT (CHAN. A)
SET I/O CLASS & UNIT (CHAN. B)
173a, 173b, 176, 179a, 179b
172.01-176, 179a, 179b
172.02-174, 177, 180a, 180b
SYNC. TGR. N-(4)
FIG.172
171.06 GATE SYNC. TGR.
222d.10 A7 (D1) D1
222b.02 A0 (D1)
Tx
75K
2K
7 (D5) D.T.U. END OPN. CNTL.
172.03-156
172.04-219a, 219b
CHANNELS A&B END OPERATION SYNCHRONIZER

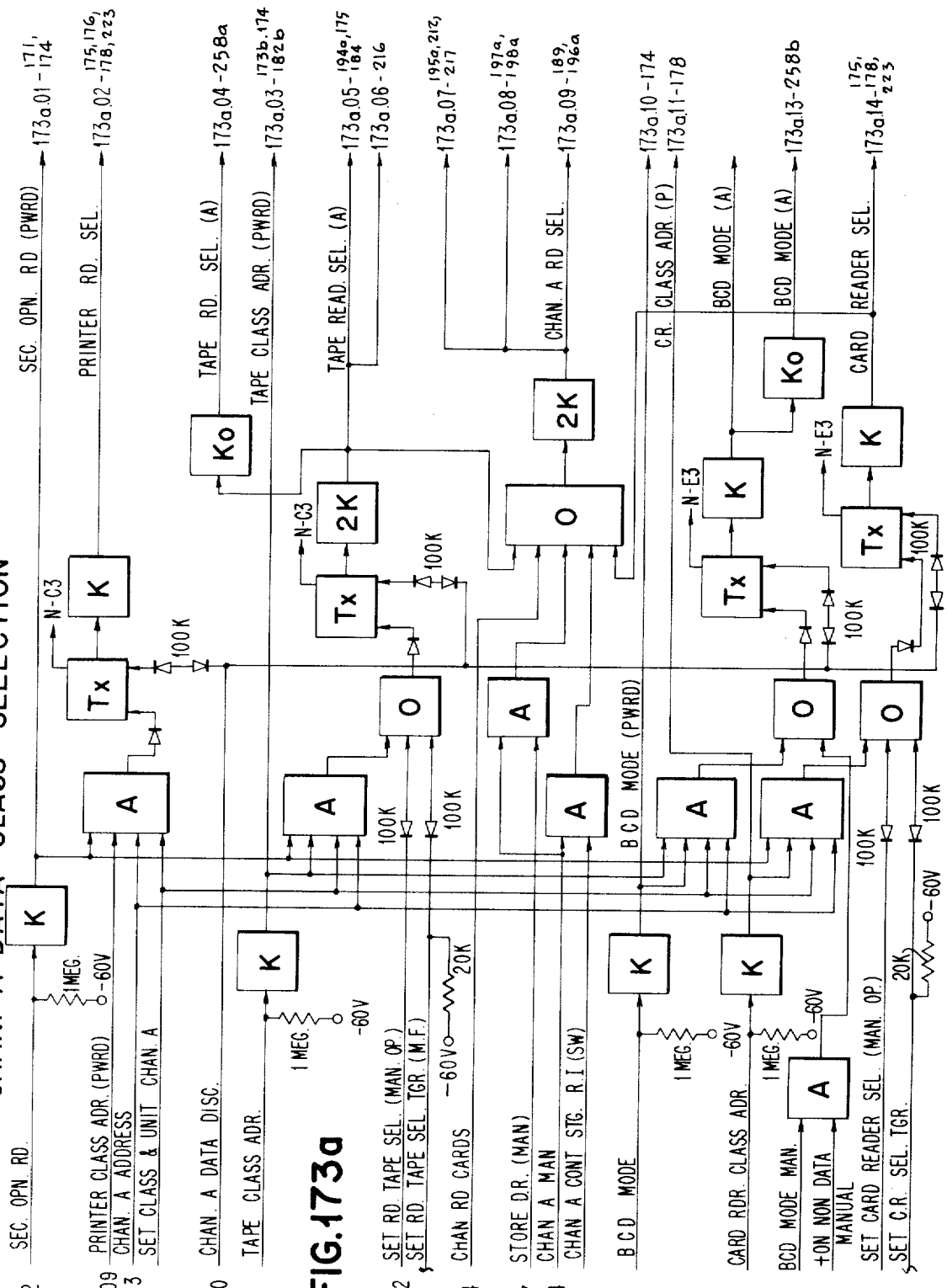

CHAN. A DATA CLASS SELECTION
SEC. OPN. RD
PRINTER CLASS ADR. (PWRD)
CHAN. A ADDRESS
SET CLASS & UNIT CHAN. A
CHAN. A DATA DISC.
TAPE CLASS ADR.
SET RD. TAPE SEL. (MAN. OP.)
SET RD. TAPE SEL. TGR. (M.F.)
CHAN RD CARDS
STORE D.R. (MAN.)
CHAN A MAN
CHAN A CONT STG. R.I. (SW)
B C D MODE
CARD RDR. CLASS ADR.
BCD MODE MAN.
+ON NON DATA
MANUAL
SET CARD READER SEL. (MAN. OP.)
SET C.R. SEL. TGR.
SEC. OPN. RD (PWRD)
PRINTER RD. SEL.
TAPE RD. SEL. (A)
TAPE CLASS ADR. (PWRD)
TAPE READ. SEL. (A)
CHAN A RD SEL.
B C D MODE (PWRD)
C.R. CLASS ADR. (P)
BCD MODE (A)
BCD MODE (A)
CARD READER SEL.
1 MEG.
-60V
100K
20K
N-C3
N-E3
K
A
O
Tx
2K
Ko
15a.02
173b.09
182a.03
172.01
198a.10
149.15
191c.02
223.04
191b.07
191a.04
192.02
192.10
159.01
149.12
191d.01
191d.06
191c.01
173a.01 - 171, 174
173a.02 - 175, 176, 178, 223
173a.04 - 258a
173a.03 - 173b, 174, 182b
173a.05 - 194a, 175, 184
173a.06 - 216
173a.07 - 195a, 212, 217
173a.08 - 197a, 198a
173a.09 - 189, 196a
173a.10 - 174
173a.11 - 178
173a.13 - 258b
173a.14 - 175, 178, 223

FIG.173a

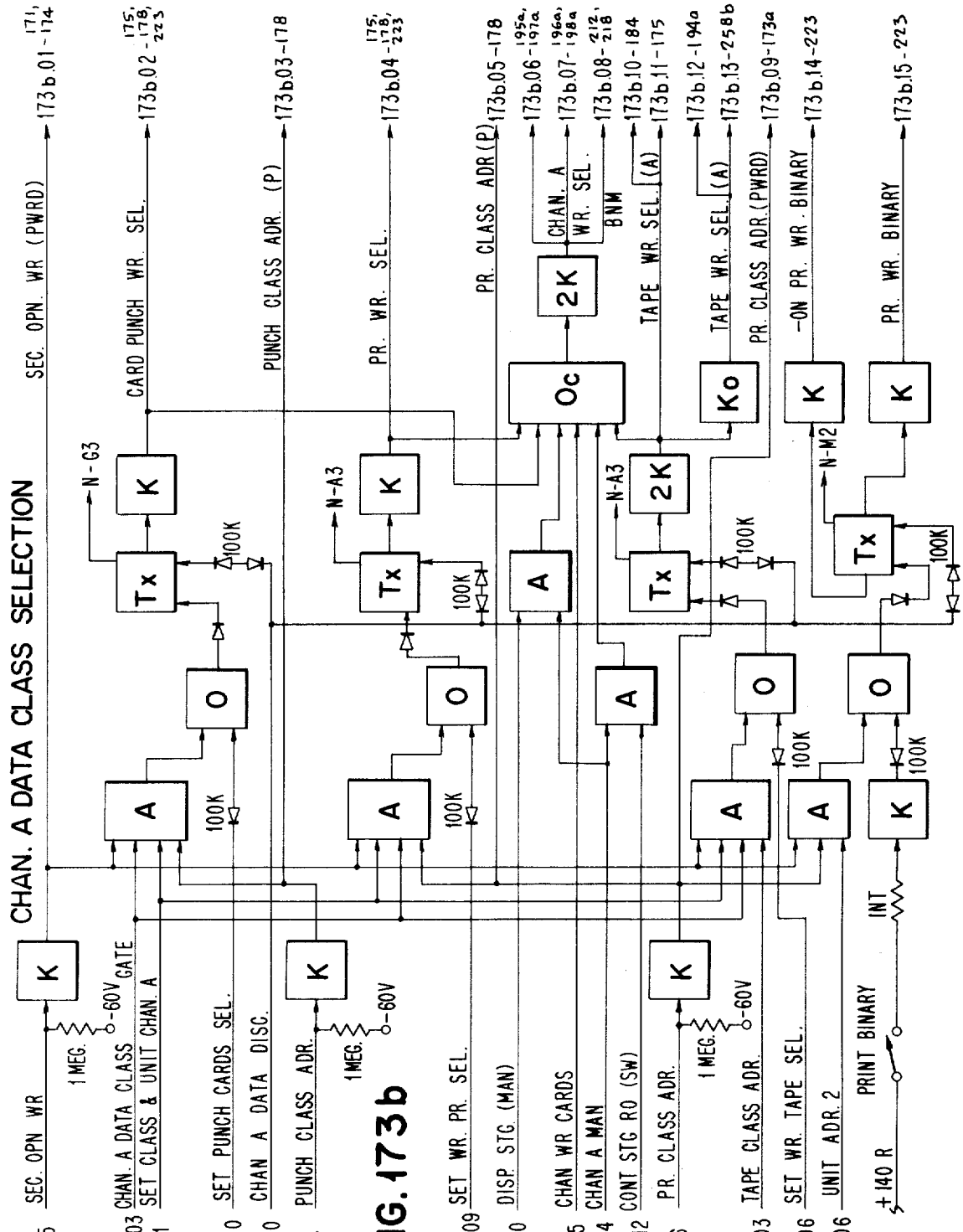

CHAN. A DATA CLASS SELECTION
SEC. OPN. WR (PWRD)
173b.01-171, 174
CARD PUNCH WR. SEL.
173b.02-175, 178, 223
PUNCH CLASS ADR. (P)
173b.03-178
PR. WR. SEL.
173b.04-175, 178, 223
PR. CLASS ADR.(P)
173b.05-178
CHAN. A WR. SEL. BNM
173b.06-195a, 197a
173b.07-196a, 198a
173b.08-212, 218
TAPE WR. SEL. (A)
173b.10-184
173b.11-175
TAPE WR. SEL. (A)
173b.12-194a
173b.13-258b
PR. CLASS ADR.(PWRD)
173b.09-173a
-ON PR. WR. BINARY
173b.14-223
PR. WR. BINARY
173b.15-223
15a.05 SEC. OPN WR
182a.03 CHAN. A DATA CLASS
172.01 SET CLASS & UNIT CHAN. A
191c.10 SET PUNCH CARDS SEL.
198a.10 CHAN A DATA DISC.
149.14 PUNCH CLASS ADR.
191c.09 SET WR. PR. SEL.
191b.20 DISP STG. (MAN)
223.05 CHAN WR CARDS
191a.04 CHAN A MAN
192.04, 192.12 CONT STG RO (SW)
149.06 PR. CLASS ADR.
173a.03 TAPE CLASS ADR.
191c.06 SET WR. TAPE SEL.
179a.06 UNIT ADR. 2
+140 R
PRINT BINARY
INT
1 MEG.
-60V
GATE
100K
N-G3
N-A3
N-M2
K
A
O
Tx
2K
Oc
Ko

FIG. 173b

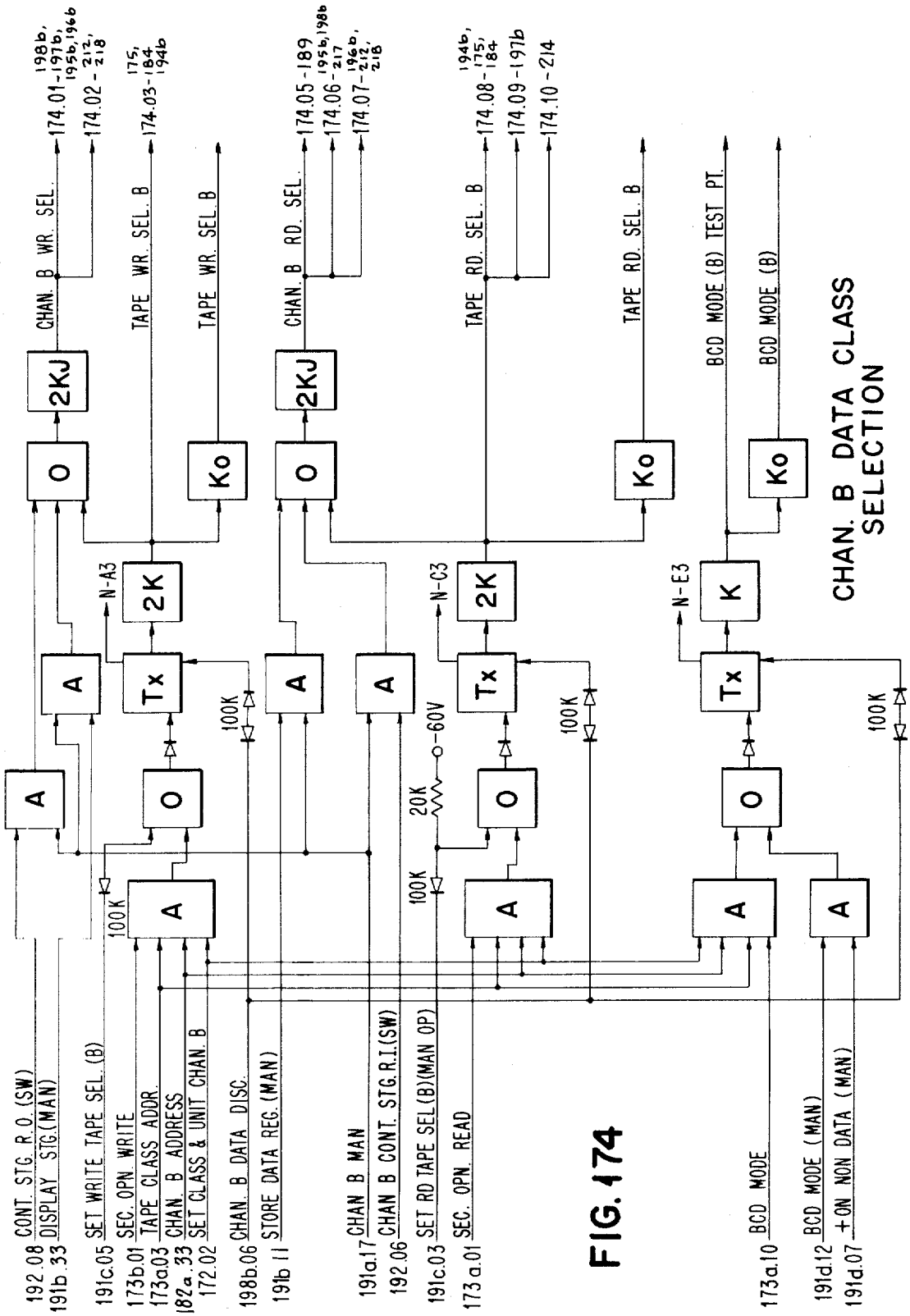

CHAN. B DATA CLASS SELECTION
CHAN. B WR. SEL.
TAPE WR. SEL. B
TAPE WR. SEL B
CHAN. B RD. SEL.
TAPE RD. SEL. B
TAPE RD. SEL. B
BCD MODE (B) TEST PT.
BCD MODE (B)
174.01 - 198b, 197b, 195b, 196b
174.02 - 212, 218
174.03 - 175, 184, 194b
174.05 - 189, 195b, 198b
174.06 - 217
174.07 - 196b, 212, 218
174.08 - 194b, 175, 184
174.09 - 197b
174.10 - 214
2KJ
2K
K
Ko
O
A
Tx
N-A3
N-C3
N-E3
100K
20K
-60V
192.08 CONT. STG. R.O. (SW)
191b.33 DISPLAY STG. (MAN)
191c.05 SET WRITE TAPE SEL. (B)
173b.01 SEC. OPN. WRITE
173a.03 TAPE CLASS ADDR.
182a.33 CHAN. B ADDRESS
172.02 SET CLASS & UNIT CHAN. B
198b.06 CHAN. B DATA DISC.
191b 11 STORE DATA REG. (MAN)
191a.17 CHAN B MAN
192.06 CHAN B CONT. STG. R.I. (SW)
191c.03 SET RD TAPE SEL (B) (MAN OP)
173 a.01 SEC. OPN. READ
173a.10 BCD MODE
191d.12 BCD MODE (MAN)
191a.07 +ON NON DATA (MAN)

FIG. 174

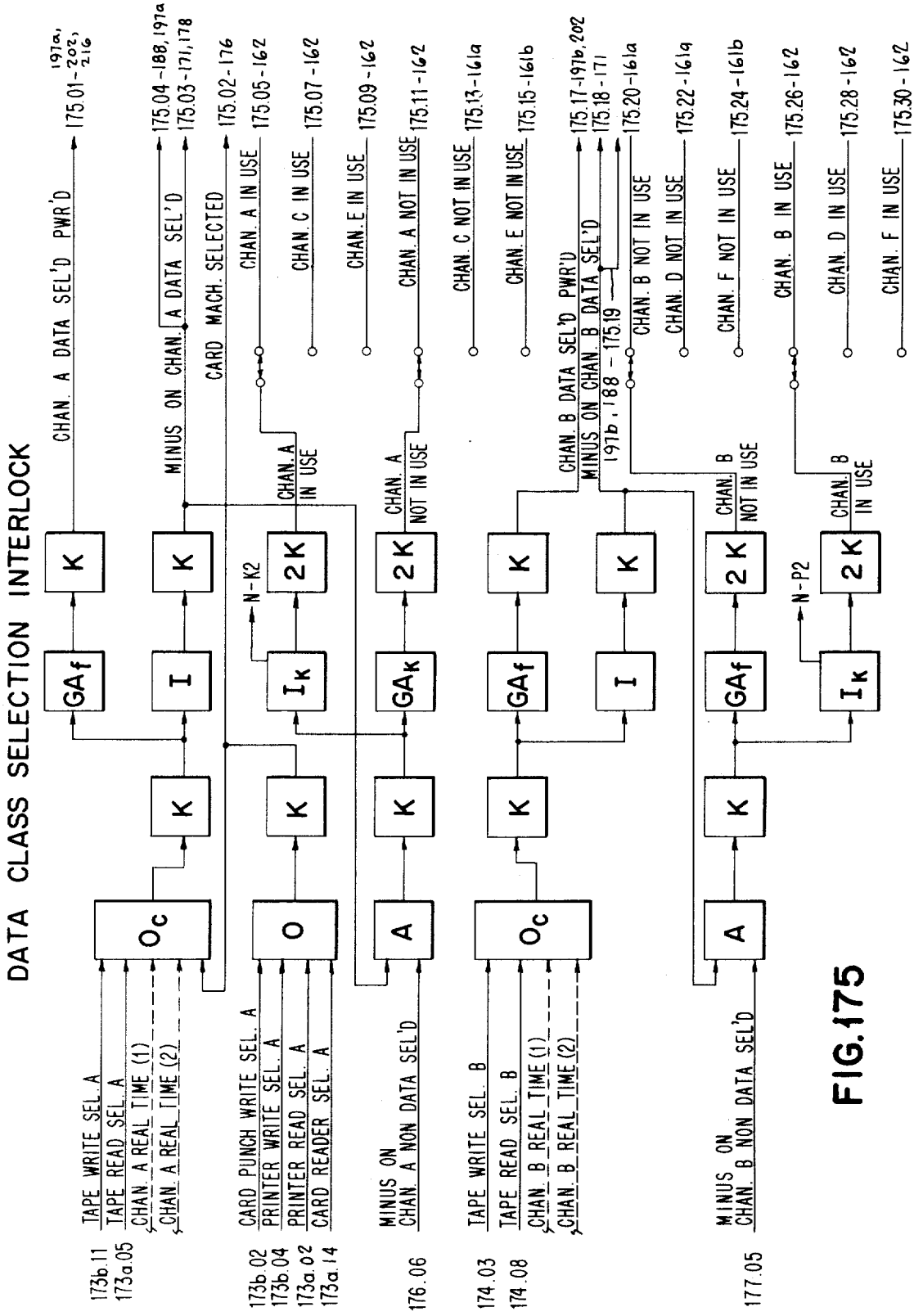

DATA CLASS SELECTION INTERLOCK
TAPE WRITE SEL. A
TAPE READ SEL. A
CHAN. A REAL TIME (1)
CHAN. A REAL TIME (2)
173b.11
173a.05
Oc
K
GAf
CHAN. A DATA SEL'D PWR'D
175.01-197a, 202, 216
I
MINUS ON CHAN. A DATA SEL'D
175.04-188, 197a
CARD MACH. SELECTED
175.03-171, 178
175.02-176
CARD PUNCH WRITE SEL. A
PRINTER WRITE SEL. A
PRINTER READ SEL. A
CARD READER SEL. A
173b.02
173b.04
173a.02
173a.14
O
N-K2
Ik
2K
CHAN. A IN USE
175.05-162
CHAN. A IN USE
CHAN. C IN USE
175.07-162
CHAN. E IN USE
175.09-162
MINUS ON CHAN. A NON DATA SEL'D
176.06
A
GAk
CHAN. A NOT IN USE
175.11-162
CHAN. C NOT IN USE
175.13-161a
CHAN. E NOT IN USE
175.15-161b
TAPE WRITE SEL. B
TAPE READ SEL. B
CHAN. B REAL TIME (1)
CHAN. B REAL TIME (2)
174.03
174.08
CHAN. B DATA SEL'D PWR'D
MINUS ON CHAN. B DATA SEL'D
197b, 188 - 175.19
175.17-197b, 202
175.18-171
175.20-161a
CHAN. B NOT IN USE
CHAN. D NOT IN USE
175.22-161a
MINUS ON CHAN. B NON DATA SEL'D
177.05
CHAN. B NOT IN USE
CHAN. F NOT IN USE
175.24-161b
N-P2
CHAN. B IN USE
175.26-162
CHAN. B IN USE
CHAN. D IN USE
175.28-162
CHAN. F IN USE
175.30-162

FIG.175

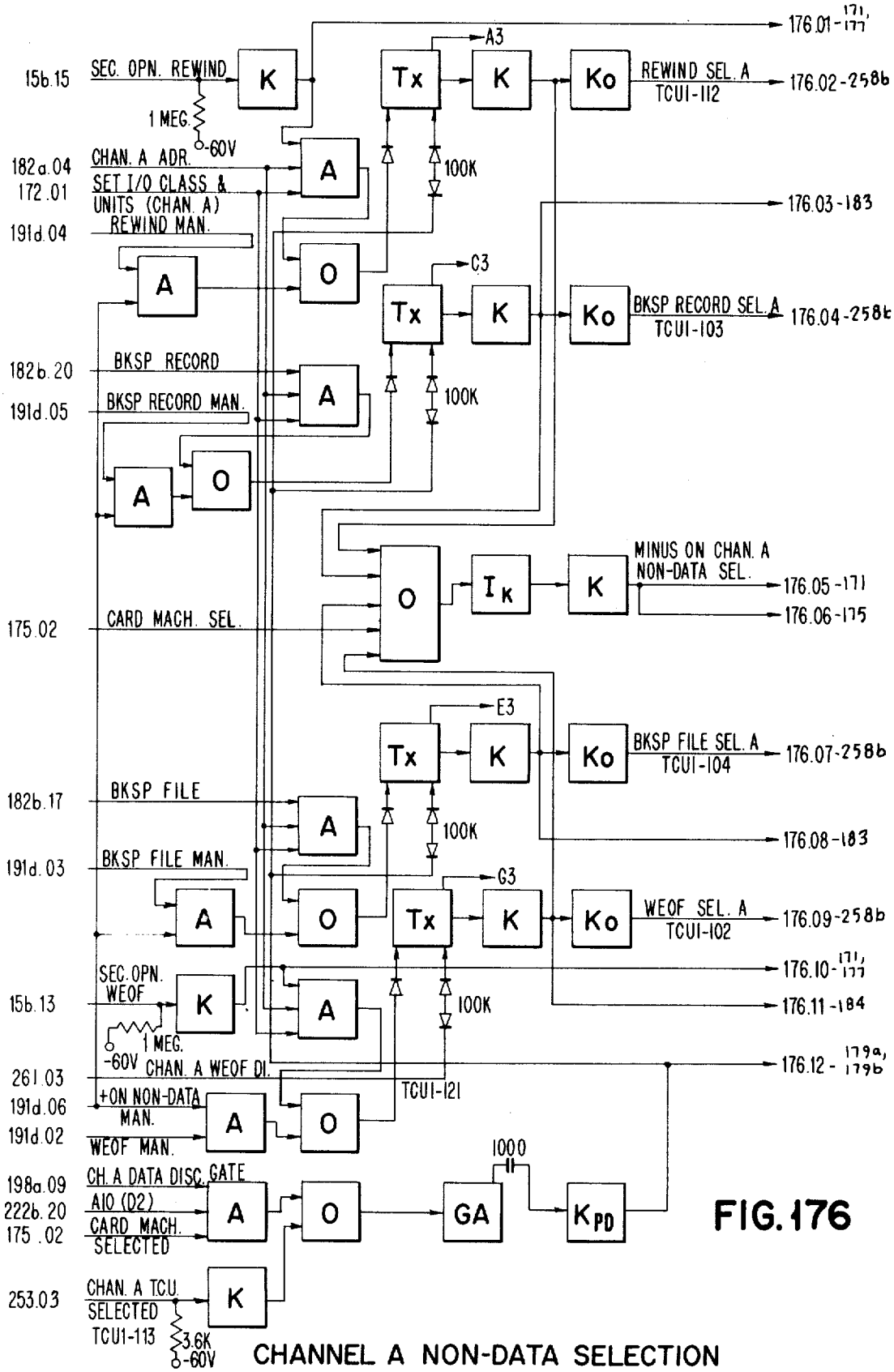


FIG. 176

CHANNEL A NON-DATA SELECTION

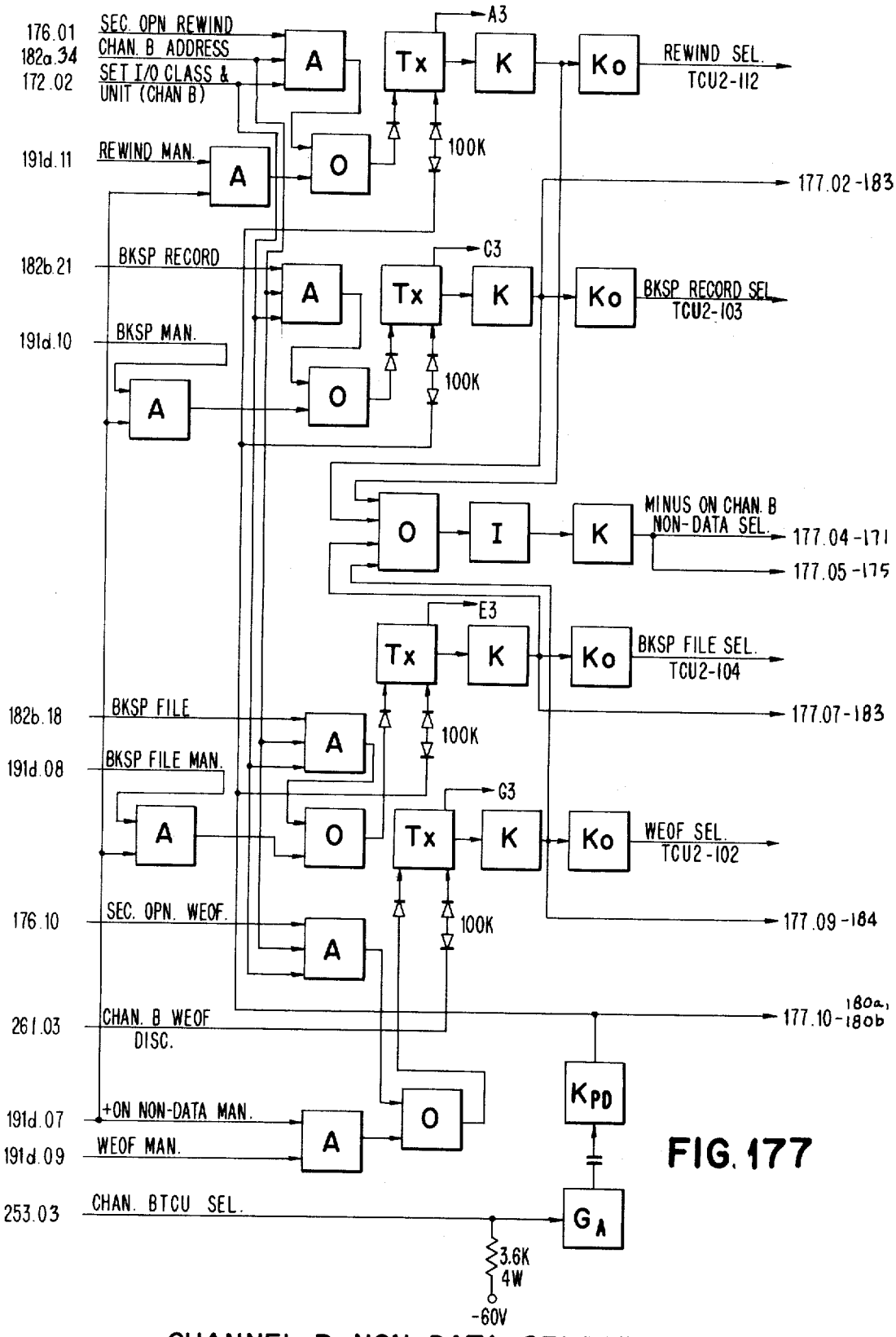


FIG. 177

CHANNEL B NON-DATA SELECTION

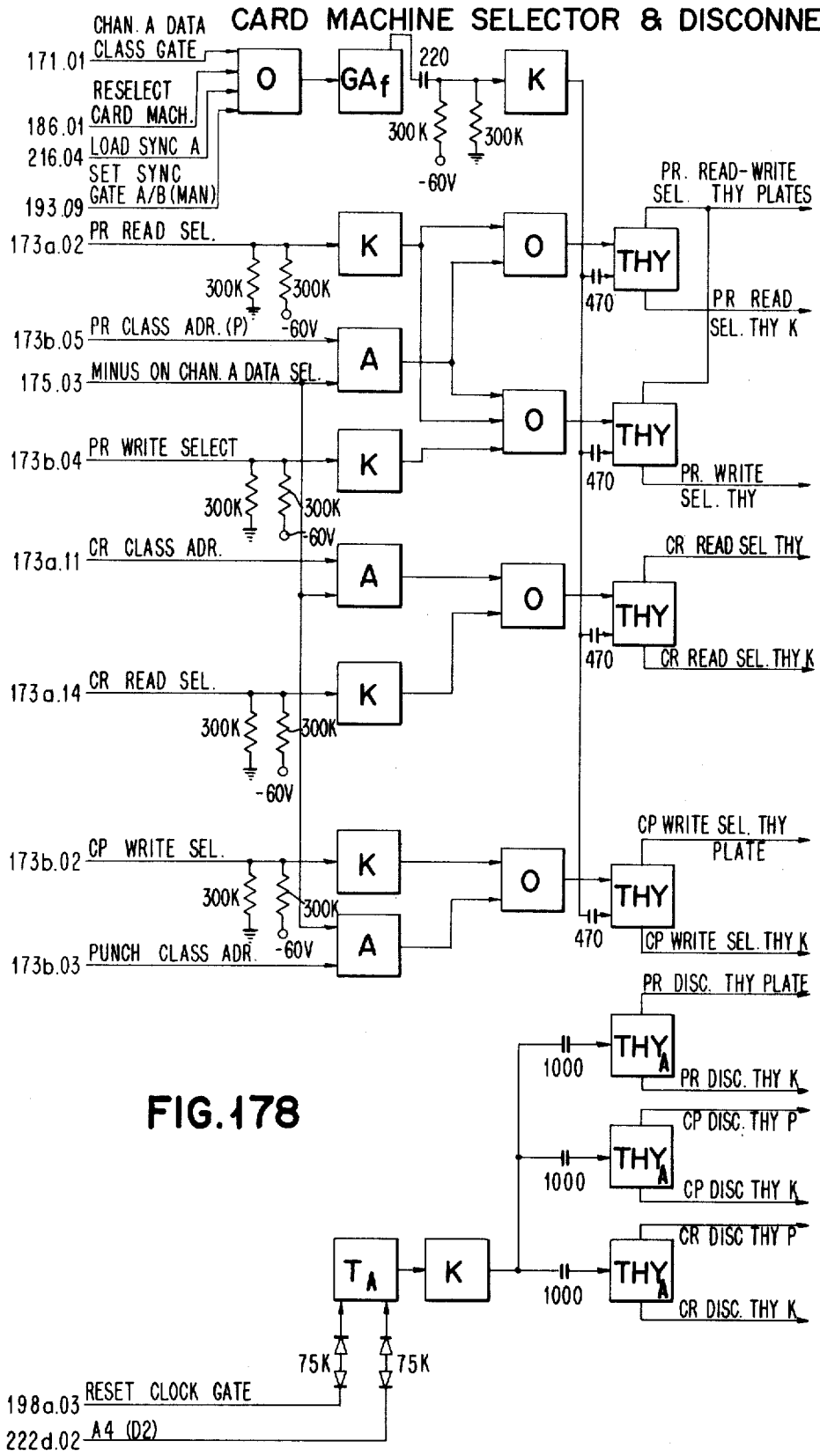

CARD MACHINE SELECTOR & DISCONNECTOR
CHAN. A DATA CLASS GATE
171.01
RESELECT CARD MACH.
186.01
LOAD SYNC A
216.04
SET SYNC GATE A/B (MAN)
193.09
O
GAf
220
300K
300K
-60V
K
PR. READ-WRITE SEL. THY PLATES
PR READ SEL. THY K
PR. WRITE SEL. THY
CR READ SEL THY
CR READ SEL. THY K
CP WRITE SEL. THY PLATE
CP WRITE SEL. THY K
PR DISC. THY PLATE
PR DISC. THY K
CP DISC. THY P
CP DISC THY K
CR DISC THY P
CR DISC. THY K
THY
THYA
470
1000
PR. READ SEL.
173a.02
PR CLASS ADR. (P)
173b.05
MINUS ON CHAN. A DATA SEL.
175.03
PR WRITE SELECT
173b.04
CR CLASS ADR.
173a.11
CR READ SEL.
173a.14
CP WRITE SEL.
173b.02
PUNCH CLASS ADR.
173b.03
A
TA
75K
RESET CLOCK GATE
198a.03
A4 (D2)
222d.02

FIG. 178

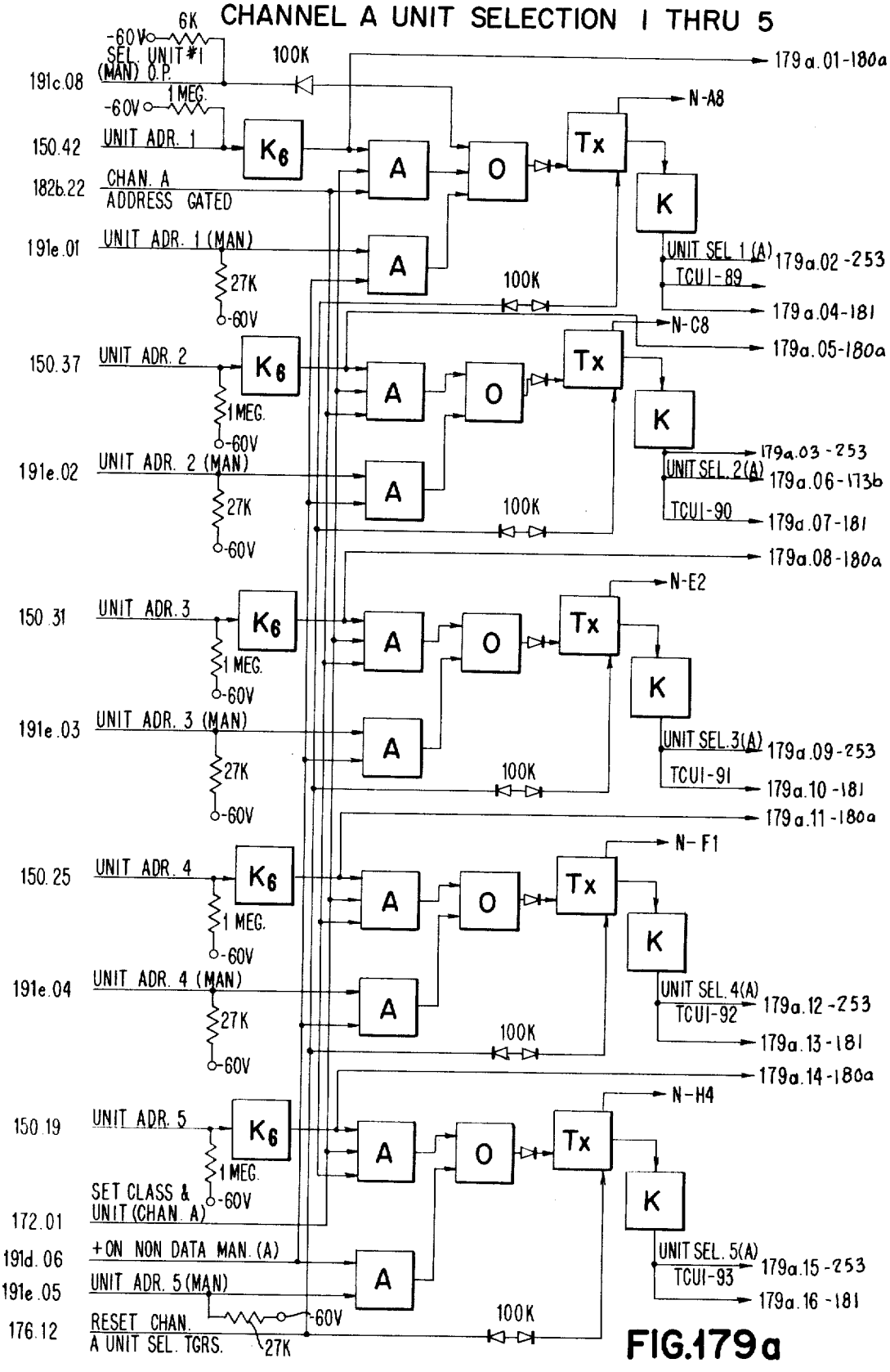

CHANNEL A UNIT SELECTION 1 THRU 5
-60V
6K
SEL. UNIT #1 (MAN) O.P.
100K
191c.08
1 MEG.
-60V
150.42
UNIT ADR. 1
K6
182b.22
CHAN. A ADDRESS GATED
A
O
Tx
K
191e.01
UNIT ADR. 1 (MAN)
27K
-60V
100K
UNIT SEL. 1 (A)
TCUI-89
179a.01-180a
N-A8
179a.02-253
179a.04-181
N-C8
179a.05-180a
150.37
UNIT ADR. 2
1 MEG.
191e.02
UNIT ADR. 2 (MAN)
179a.03-253
UNIT SEL. 2(A)
179a.06-173b
TCUI-90
179a.07-181
179a.08-180a
N-E2
150.31
UNIT ADR. 3
191e.03
UNIT ADR. 3 (MAN)
UNIT SEL. 3(A)
179a.09-253
TCUI-91
179a.10-181
179a.11-180a
N-F1
150.25
UNIT ADR. 4
191e.04
UNIT ADR. 4 (MAN)
UNIT SEL. 4(A)
TCUI-92
179a.12-253
179a.13-181
179a.14-180a
N-H4
150.19
UNIT ADR. 5
SET CLASS & UNIT (CHAN. A)
172.01
+ON NON DATA MAN. (A)
191d.06
191e.05
UNIT ADR. 5 (MAN)
UNIT SEL. 5(A)
TCUI-93
179a.15-253
179a.16-181
176.12
RESET CHAN. A UNIT SEL. TGRS.
27K

FIG.179a

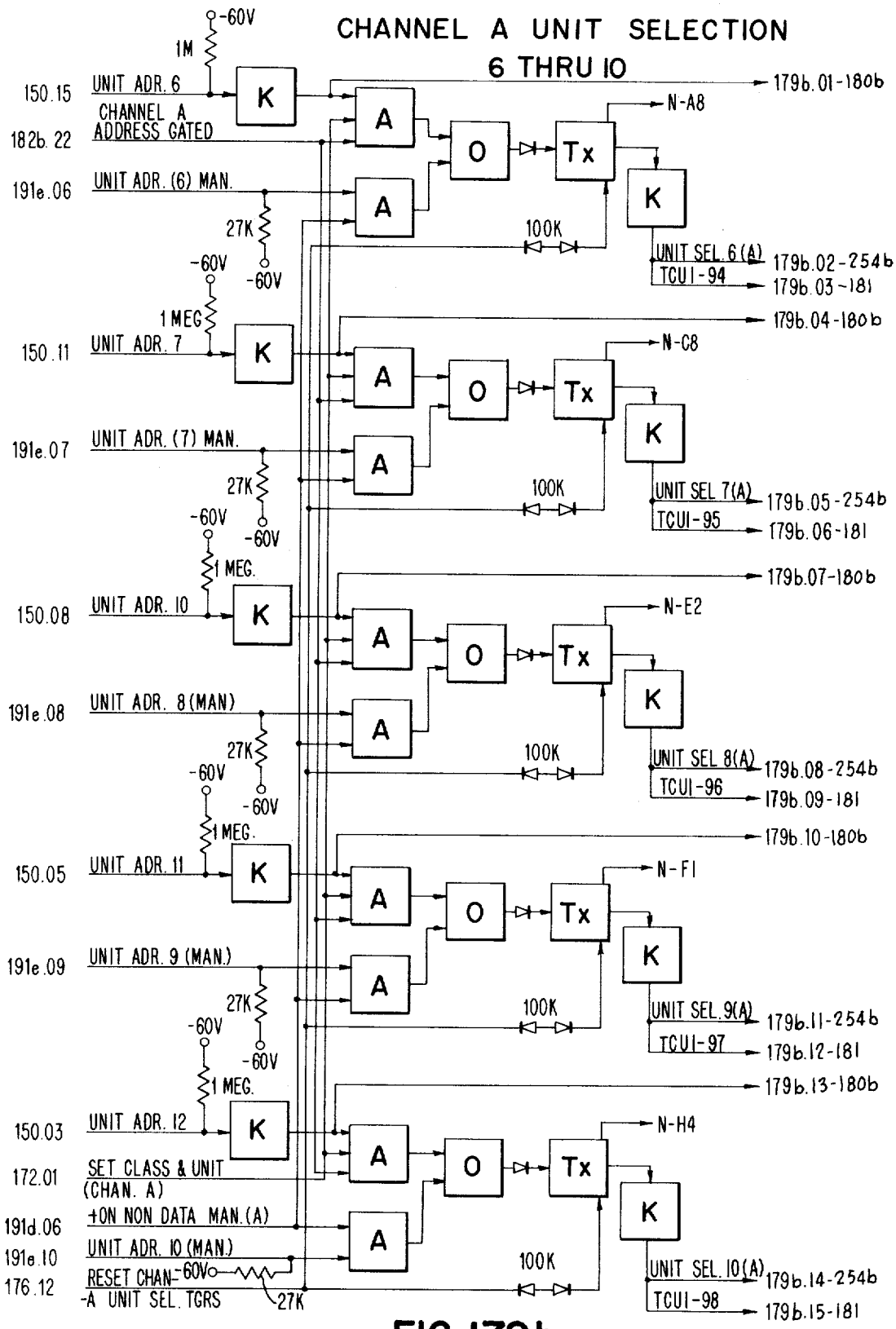

CHANNEL A UNIT SELECTION
6 THRU 10
-60V
1M
150.15
UNIT ADR. 6
CHANNEL A
ADDRESS GATED
182b. 22
191e.06
UNIT ADR. (6) MAN.
27K
-60V
-60V
1 MEG
150.11
UNIT ADR. 7
191e.07
UNIT ADR. (7) MAN.
27K
-60V
-60V
1 MEG.
150.08
UNIT ADR. 10
191e.08
UNIT ADR. 8 (MAN)
27K
-60V
-60V
1 MEG.
150.05
UNIT ADR. 11
191e.09
UNIT ADR. 9 (MAN.)
27K
-60V
-60V
1 MEG.
150.03
UNIT ADR. 12
172.01
SET CLASS & UNIT
(CHAN. A)
191d.06
+ON NON DATA MAN.(A)
191e.10
UNIT ADR. 10 (MAN.)
176.12
RESET CHAN-A UNIT SEL. TGRS
-60V
27K
K
A
O
Tx
100K
179b.01-180b
N-A8
UNIT SEL. 6(A)
TCUI-94
179b.02-254b
179b.03-181
179b.04-180b
N-C8
UNIT SEL 7(A)
TCUI-95
179b.05-254b
179b.06-181
179b.07-180b
N-E2
UNIT SEL 8(A)
TCUI-96
179b.08-254b
179b.09-181
179b.10-180b
N-F1
UNIT SEL.9(A)
TCUI-97
179b.11-254b
179b.12-181
179b.13-180b
N-H4
UNIT SEL. 10(A)
TCUI-98
179b.14-254b
179b.15-181

FIG. 179b

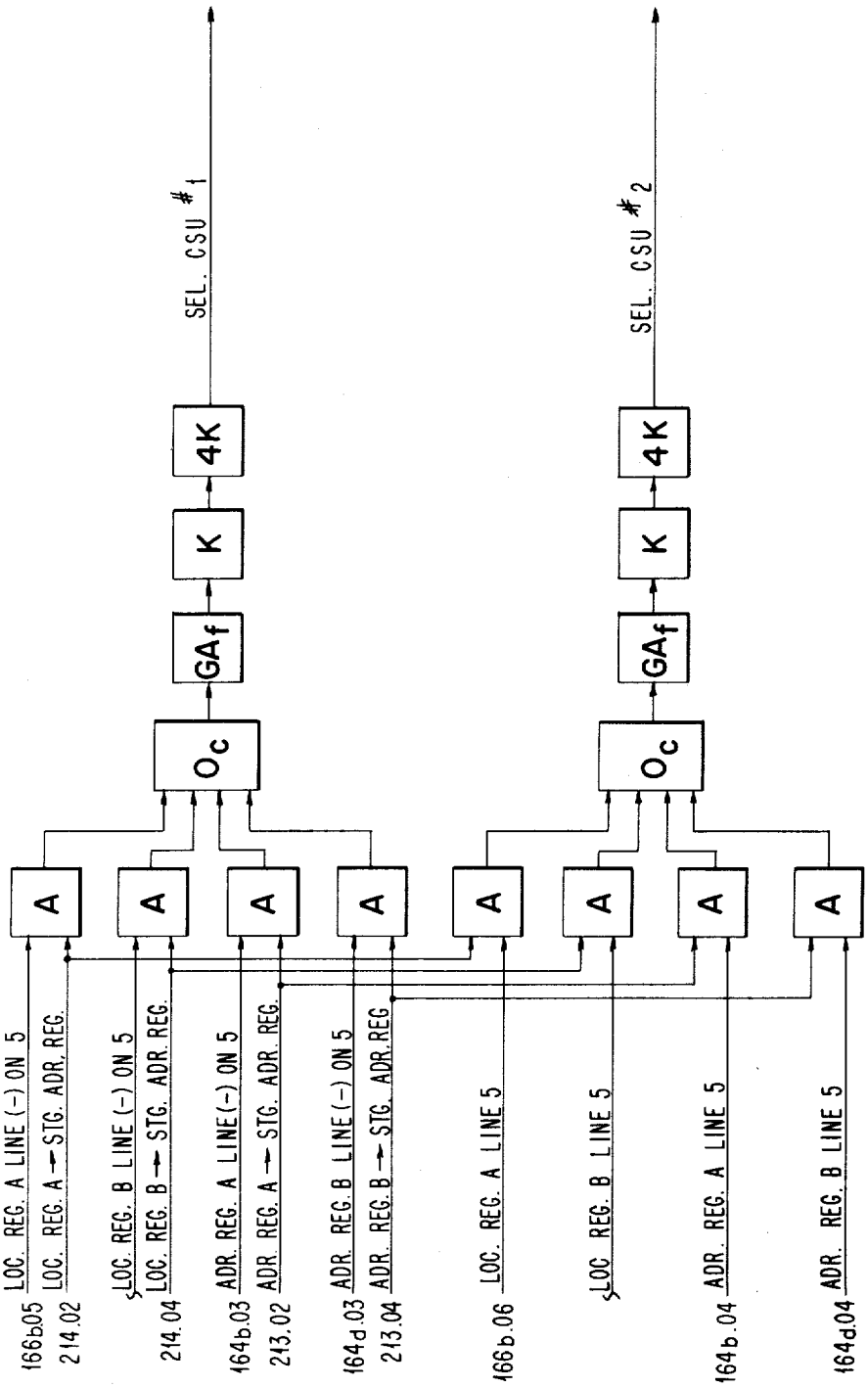

CORE STORAGE UNIT SELECTION (2-737's)
166b.05 LOC. REG. A LINE (-) ON 5
214.02 LOC. REG. A → STG. ADR. REG.
LOC. REG. B LINE (-) ON 5
214.04 LOC. REG. B → STG. ADR. REG.
164b.03 ADR. REG. A LINE (-) ON 5
213.02 ADR. REG. A → STG. ADR. REG.
164d.03 ADR. REG. B LINE (-) ON 5
213.04 ADR. REG. B → STG. ADR. REG
166b.06 LOC. REG. A LINE 5
LOC. REG. B LINE 5
164b.04 ADR. REG. A LINE 5
164d.04 ADR. REG. B LINE 5
A
Oc
GAf
K
4K
SEL. CSU #1
SEL. CSU #2

FIG.179c

CHANNEL B UNIT SELECTION - (1 THRU 5)

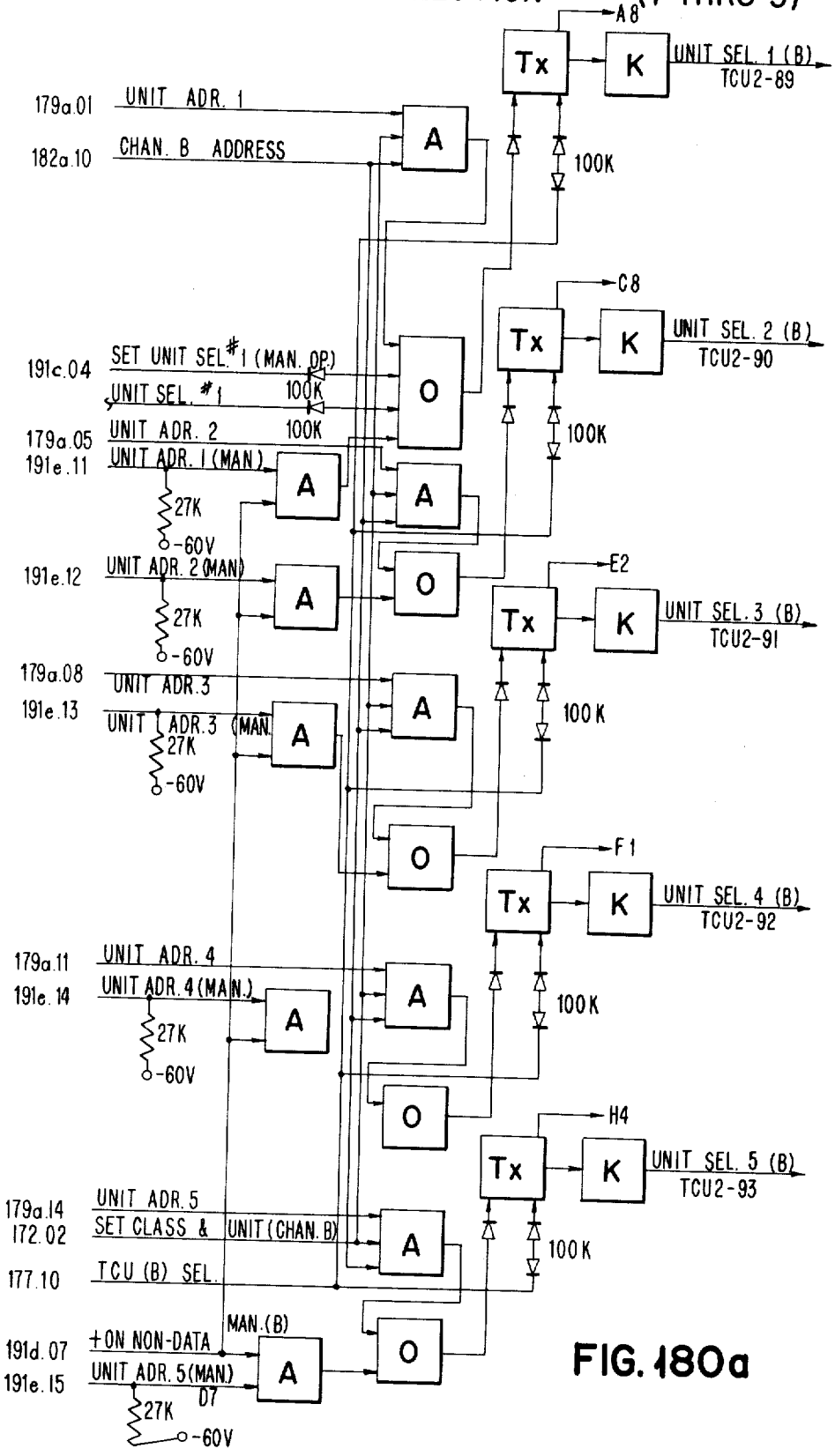


FIG. 180a

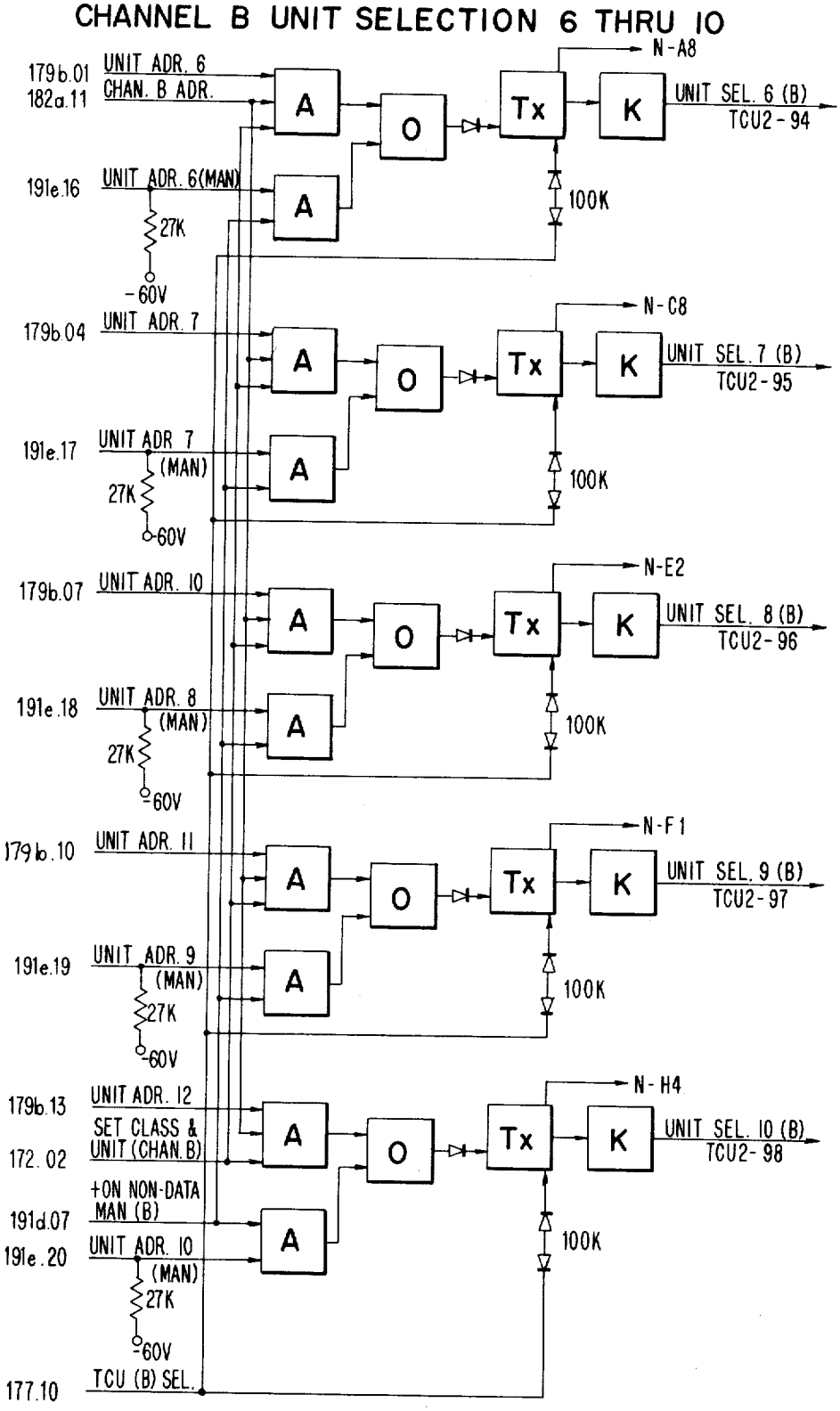

CHANNEL B UNIT SELECTION 6 THRU 10
179b.01
182a.11
UNIT ADR. 6
CHAN. B ADR.
191e.16
UNIT ADR. 6(MAN)
27K
-60V
179b.04
UNIT ADR. 7
191e.17
UNIT ADR 7
(MAN)
27K
-60V
179b.07
UNIT ADR. 10
191e.18
UNIT ADR. 8
(MAN)
27K
-60V
179b.10
UNIT ADR. 11
191e.19
UNIT ADR. 9
(MAN)
27K
-60V
179b.13
UNIT ADR. 12
172.02
SET CLASS & UNIT (CHAN. B)
191d.07
+ON NON-DATA MAN (B)
191e.20
UNIT ADR. 10
(MAN)
27K
-60V
177.10
TCU (B) SEL.
A
O
Tx
K
100K
N-A8
UNIT SEL. 6 (B)
TCU2-94
N-C8
UNIT SEL. 7 (B)
TCU2-95
N-E2
UNIT SEL. 8 (B)
TCU2-96
N-F1
UNIT SEL. 9 (B)
TCU2-97
N-H4
UNIT SEL. 10 (B)
TCU2-98

FIG. 180b

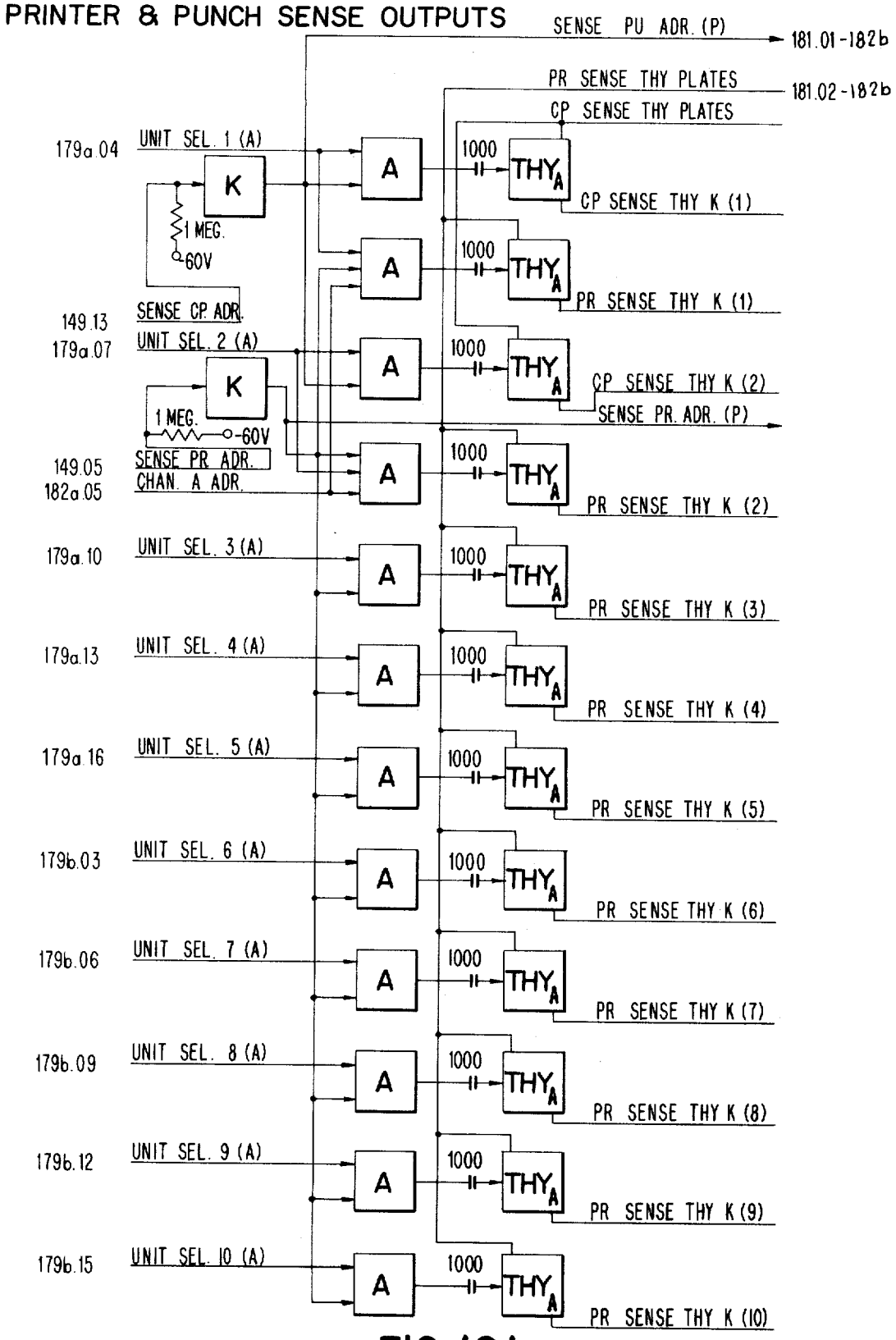
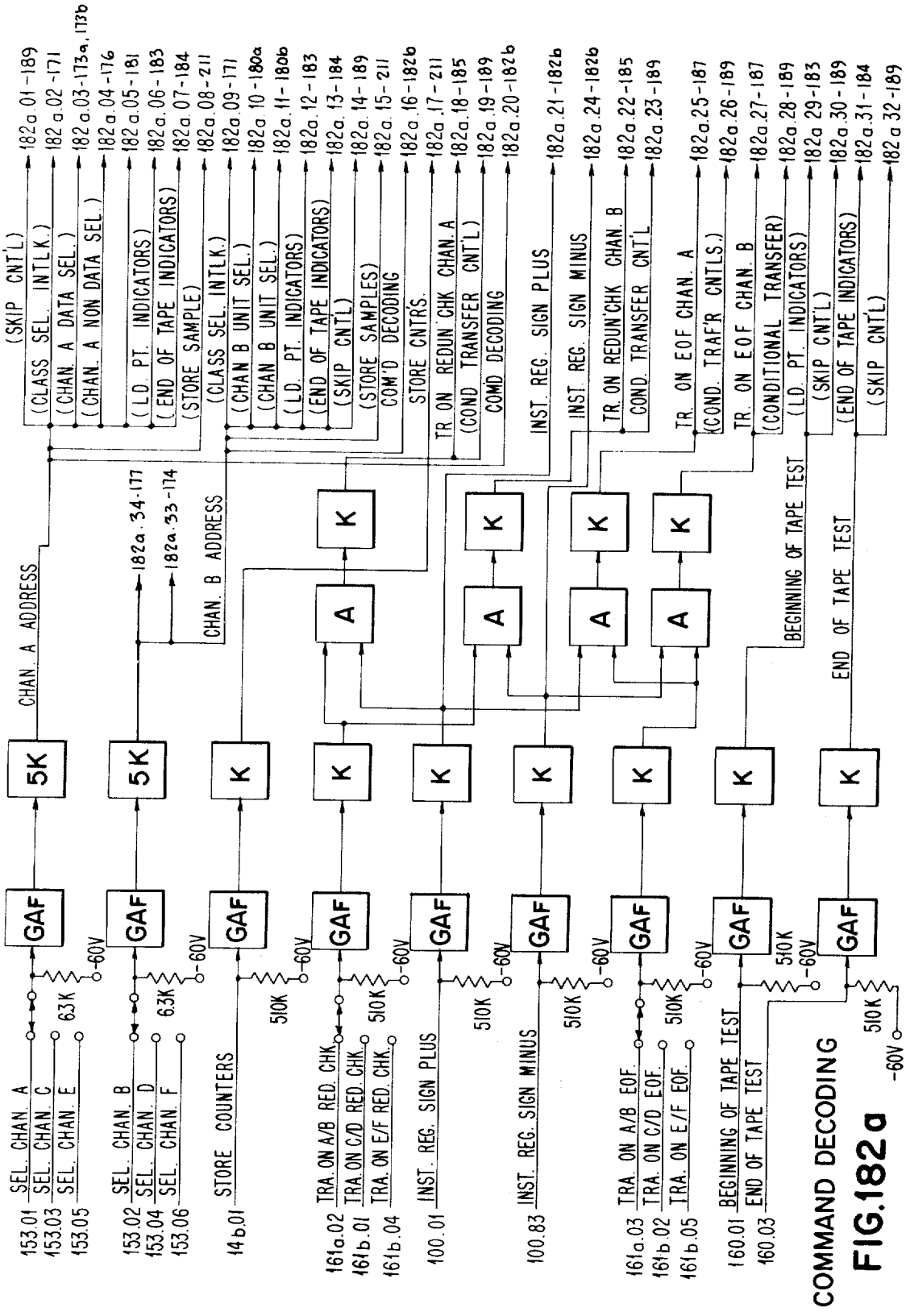

PRINTER & PUNCH SENSE OUTPUTS
SENSE PU ADR. (P)
181.01-182b
PR SENSE THY PLATES
181.02-182b
CP SENSE THY PLATES
179a.04
UNIT SEL. 1 (A)
K
1 MEG.
60V
A
1000
THY A
CP SENSE THY K (1)
PR SENSE THY K (1)
149.13
SENSE CP ADR.
179a.07
UNIT SEL. 2 (A)
CP SENSE THY K (2)
SENSE PR. ADR. (P)
149.05
SENSE PR ADR.
182a.05
CHAN. A ADR.
PR SENSE THY K (2)
179a.10
UNIT SEL. 3 (A)
PR SENSE THY K (3)
179a.13
UNIT SEL. 4 (A)
PR SENSE THY K (4)
179a.16
UNIT SEL. 5 (A)
PR SENSE THY K (5)
179b.03
UNIT SEL. 6 (A)
PR SENSE THY K (6)
179b.06
UNIT SEL. 7 (A)
PR SENSE THY K (7)
179b.09
UNIT SEL. 8 (A)
PR SENSE THY K (8)
179b.12
UNIT SEL. 9 (A)
PR SENSE THY K (9)
179b.15
UNIT SEL. 10 (A)
PR SENSE THY K (10)

FIG. 181



COMMAND DECODING

FIG.182a

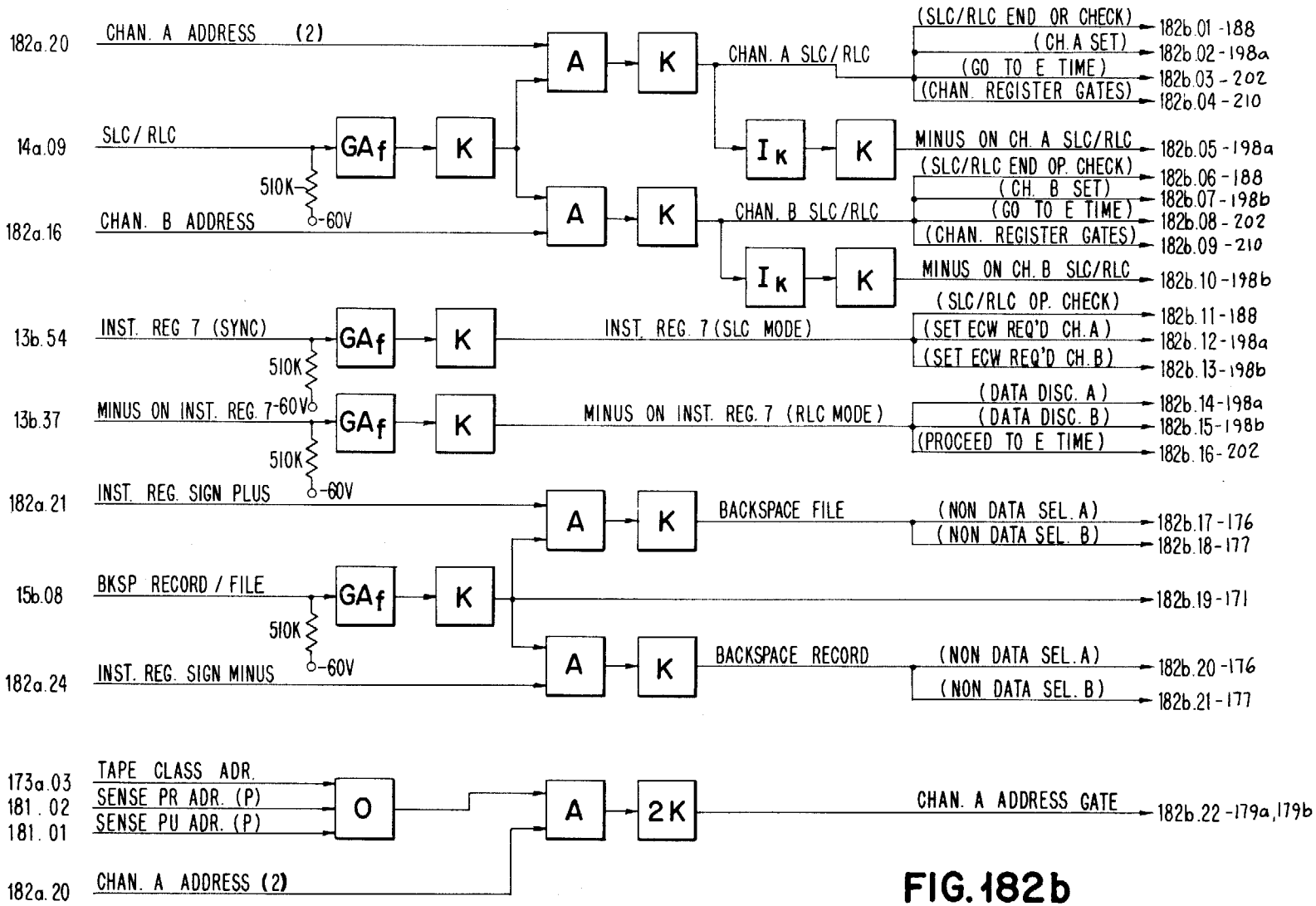
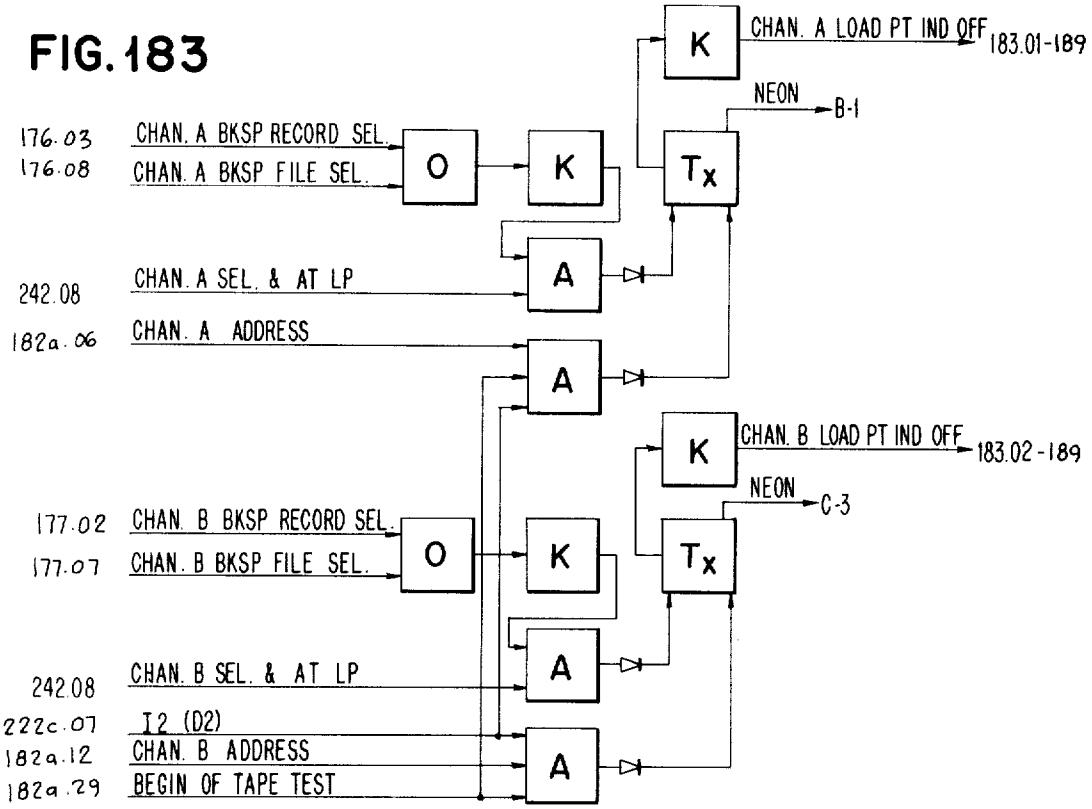


FIG. 182b

COMMAND DECODING

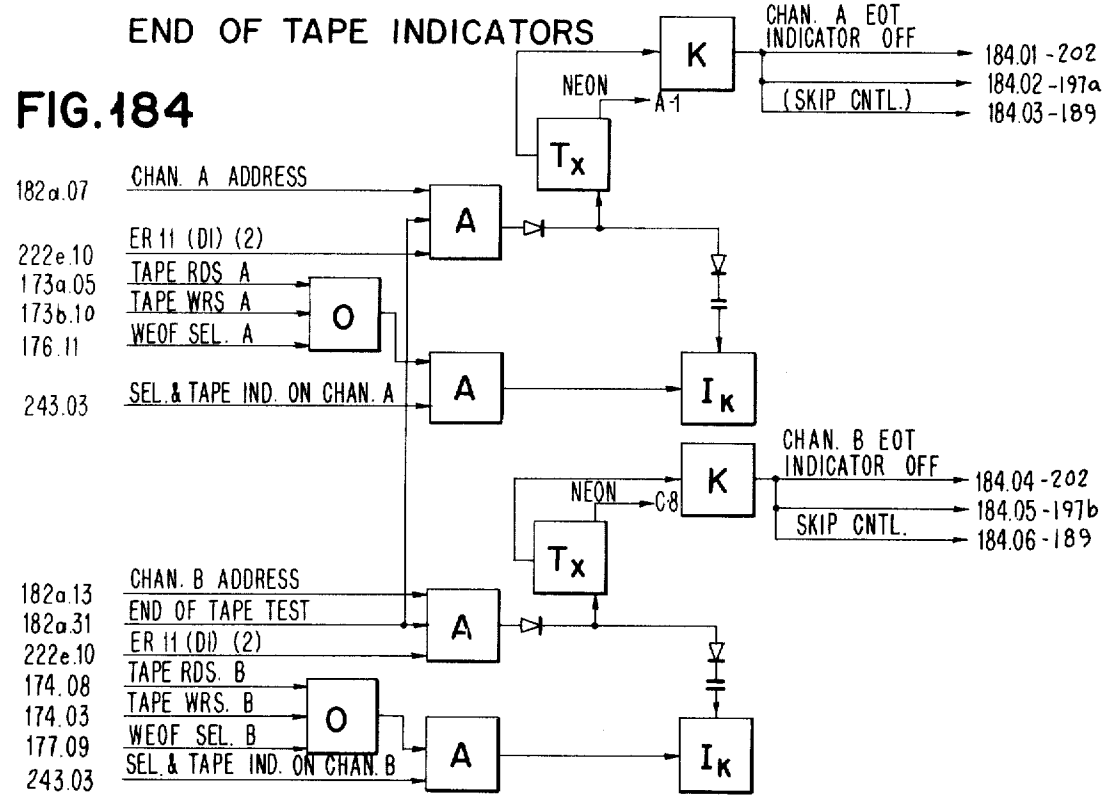
LOAD POINT INDICATORS

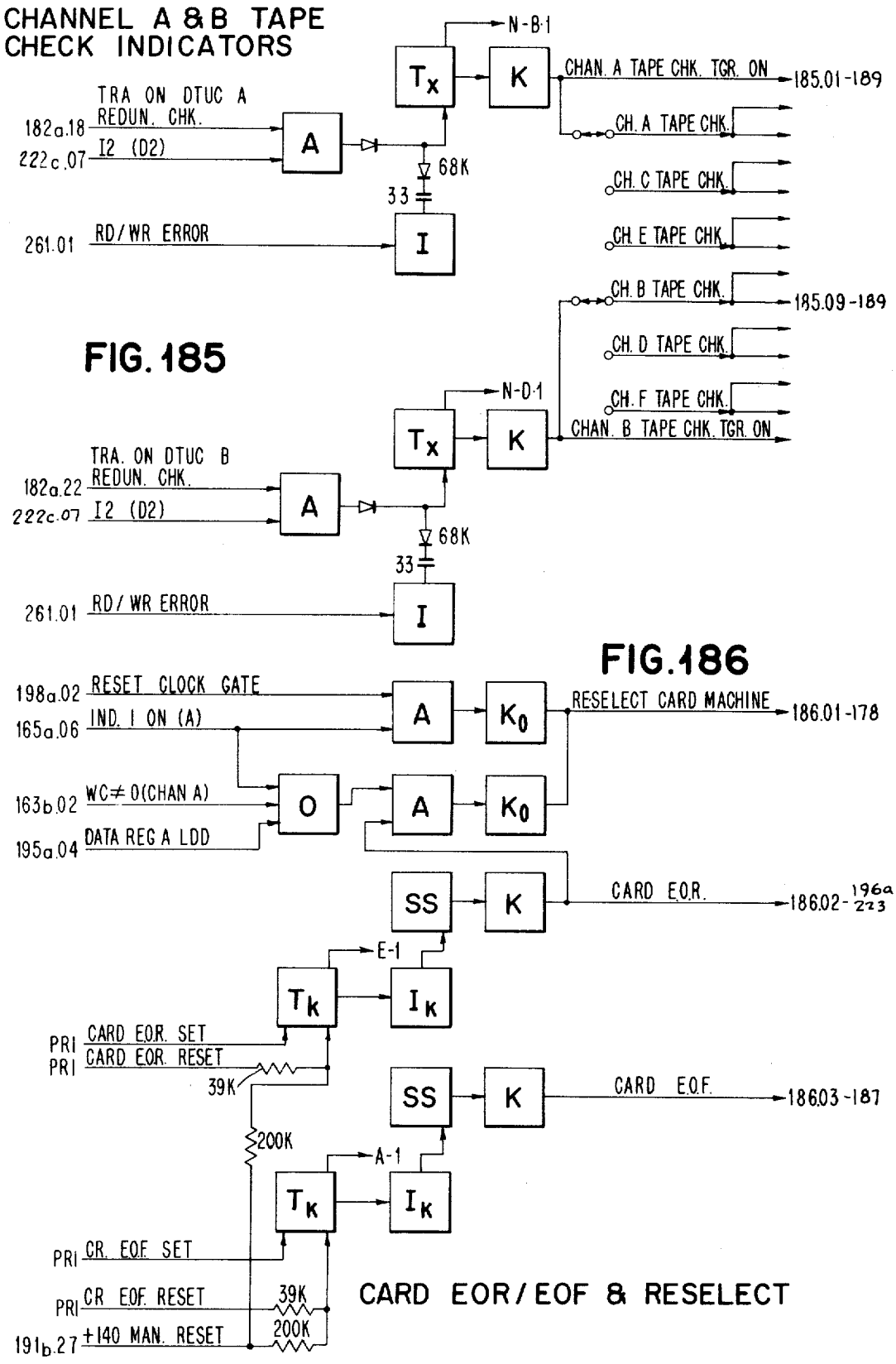
FIG. 183



END OF TAPE INDICATORS

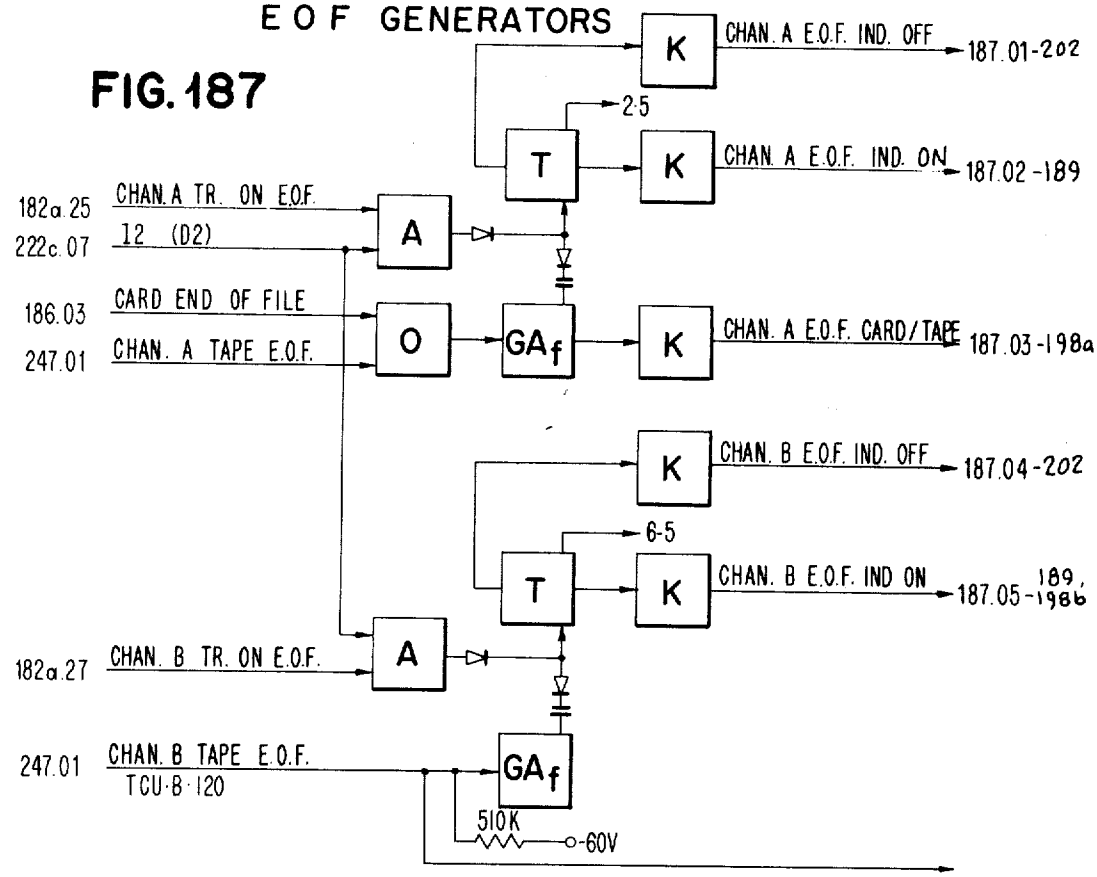
FIG. 184




CHANNEL A & B TAPE CHECK INDICATORS
TRA ON DTUC A REDUN. CHK.
182a.18
I2 (D2)
222c.07
A
68K
33
261.01
RD/WR ERROR
I
Tx
K
N-B-1
CHAN. A TAPE CHK. TGR. ON
185.01-189
CH. A TAPE CHK.
CH. C TAPE CHK.
CH. E TAPE CHK.
CH. B TAPE CHK.
185.09-189
CH. D TAPE CHK.
CH. F TAPE CHK.
CHAN. B TAPE CHK. TGR. ON
N-D-1
TRA. ON DTUC B REDUN. CHK.
182a.22
I2 (D2)
222c.07
FIG. 185
FIG. 186
198a.02
RESET CLOCK GATE
165a.06
IND. I ON (A)
163b.02
WC≠0(CHAN A)
195a.04
DATA REG A LDD
O
K0
RESELECT CARD MACHINE
186.01-178
SS
CARD E.O.R.
186.02-196a, 223
E-1
Tk
Ik
PRI
CARD E.O.R. SET
PRI
CARD E.O.R. RESET
39K
200K
CARD E.O.F.
186.03-187
A-1
PRI
CR. E.O.F. SET
PRI
CR E.O.F. RESET
191b.27
+140 MAN. RESET
CARD EOR/EOF & RESELECT

E O F GENERATORS

FIG. 187



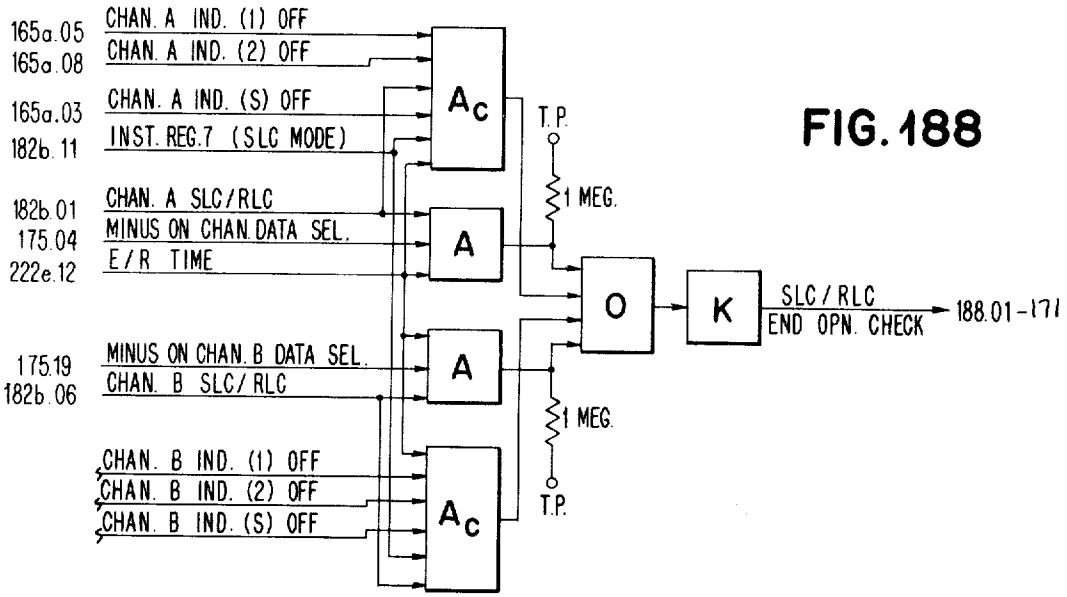


FIG. 188

SLC/RLC END OPERATION CHECK

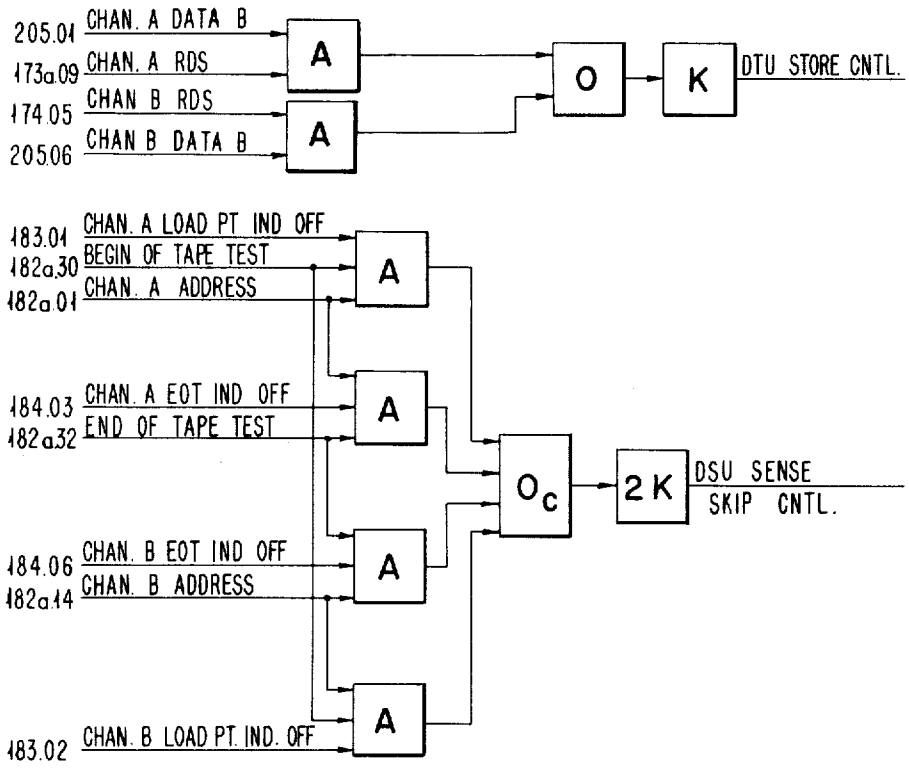
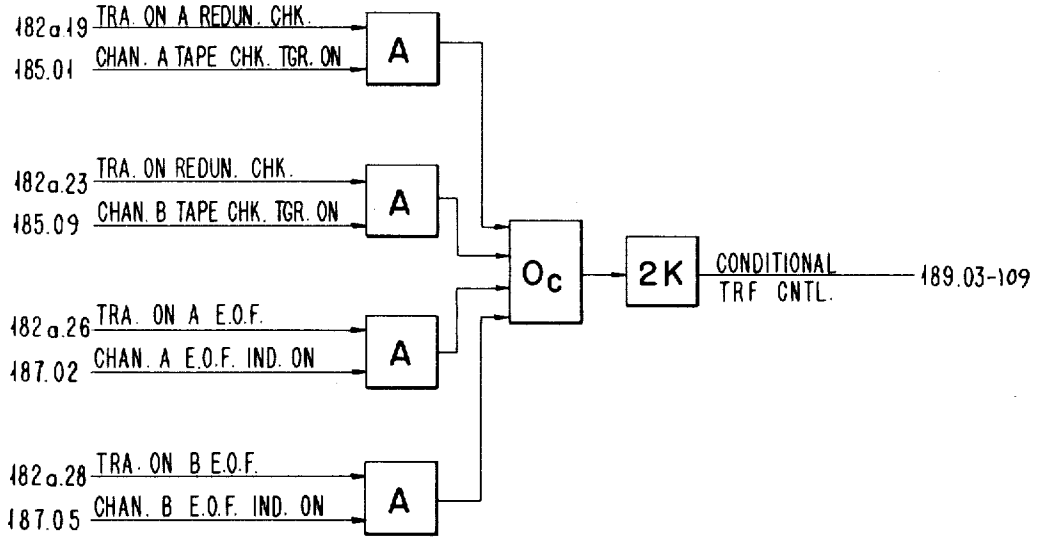


FIG. 189



DS STORE SKIP & COND. TRANSFER CNTL'S

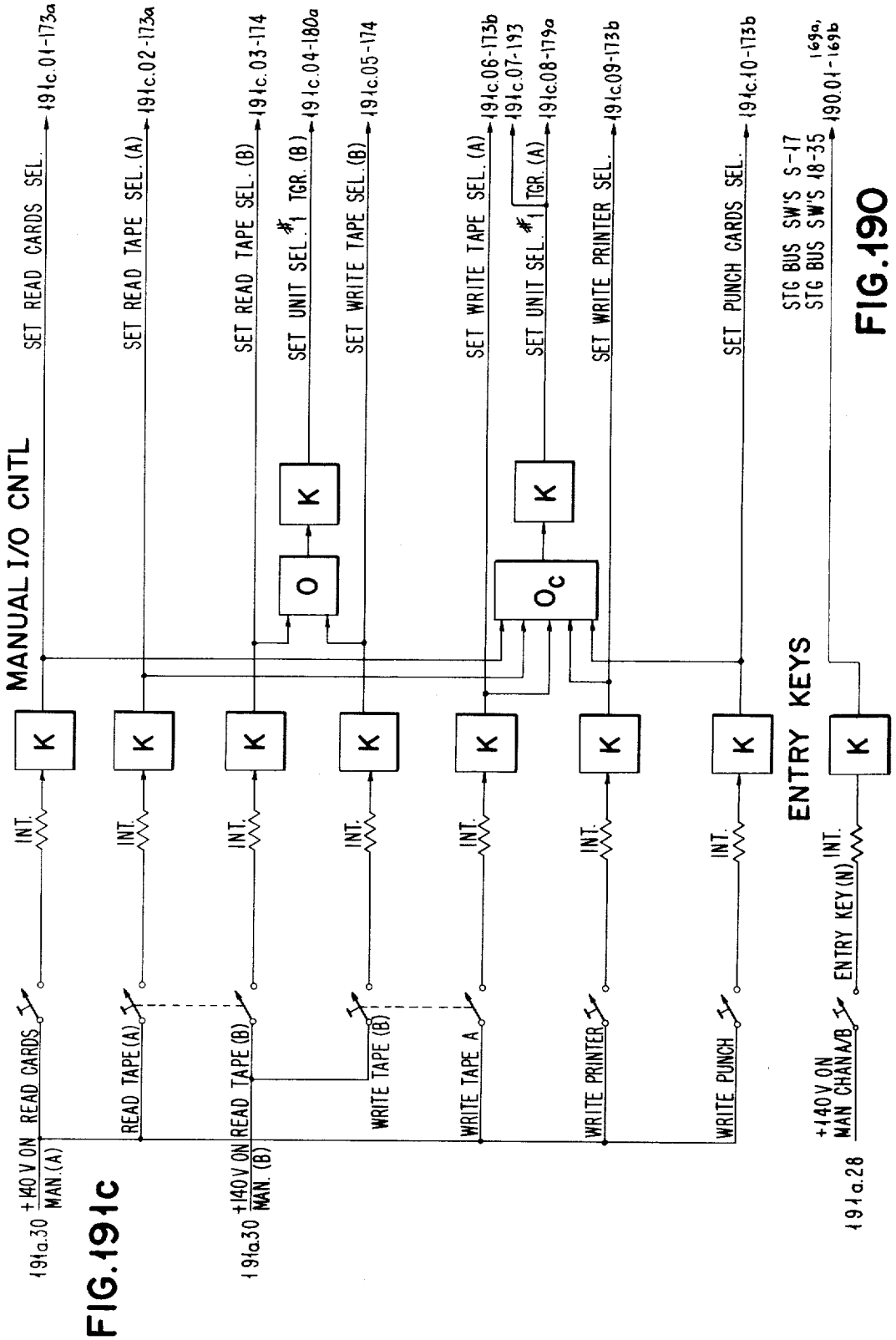


FIG.191c

FIG.190

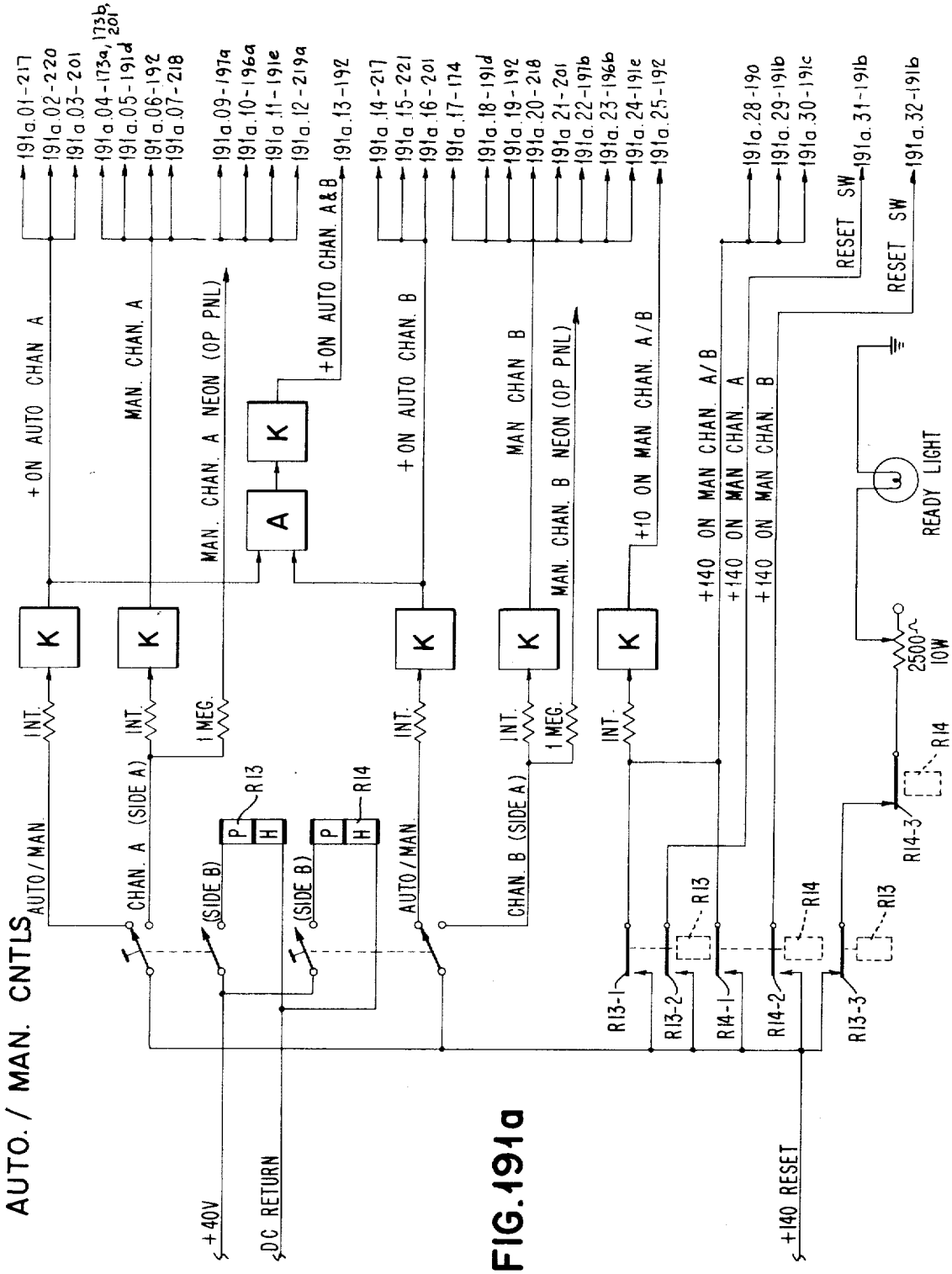

AUTO. / MAN. CNTLS
AUTO/MAN
CHAN. A (SIDE A)
(SIDE B)
INT.
1 MEG.
K
A
P
H
R13
R14
+40V
DC RETURN
+ON AUTO CHAN A
MAN. CHAN. A
MAN. CHAN. A NEON (OP PNL)
+ON AUTO CHAN. A&B
+ON AUTO CHAN. B
MAN CHAN B
MAN. CHAN. B NEON (OP PNL)
+10 ON MAN CHAN. A/B
+140 ON MAN CHAN. A/B
+140 ON MAN CHAN. A
+140 ON MAN CHAN. B
+140 RESET
R13-1
R13-2
R14-1
R14-2
R13-3
R14-3
RESET SW
2500Ω 10W
READY LIGHT
191a.01-217
191a.02-220
191a.03-201
191a.04-173a, 173b, 201
191a.05-191d
191a.06-192
191a.07-218
191a.09-197a
191a.10-196a
191a.11-191e
191a.12-219a
191a.13-192
191a.14-217
191a.15-221
191a.16-201
191a.17-174
191a.18-191d
191a.19-192
191a.20-218
191a.21-201
191a.22-197b
191a.23-196b
191a.24-191e
191a.25-192
191a.28-190
191a.29-191b
191a.30-191c
191a.31-191b
191a.32-191b

FIG.191a

FIG. 191b. MANUAL CONTROL

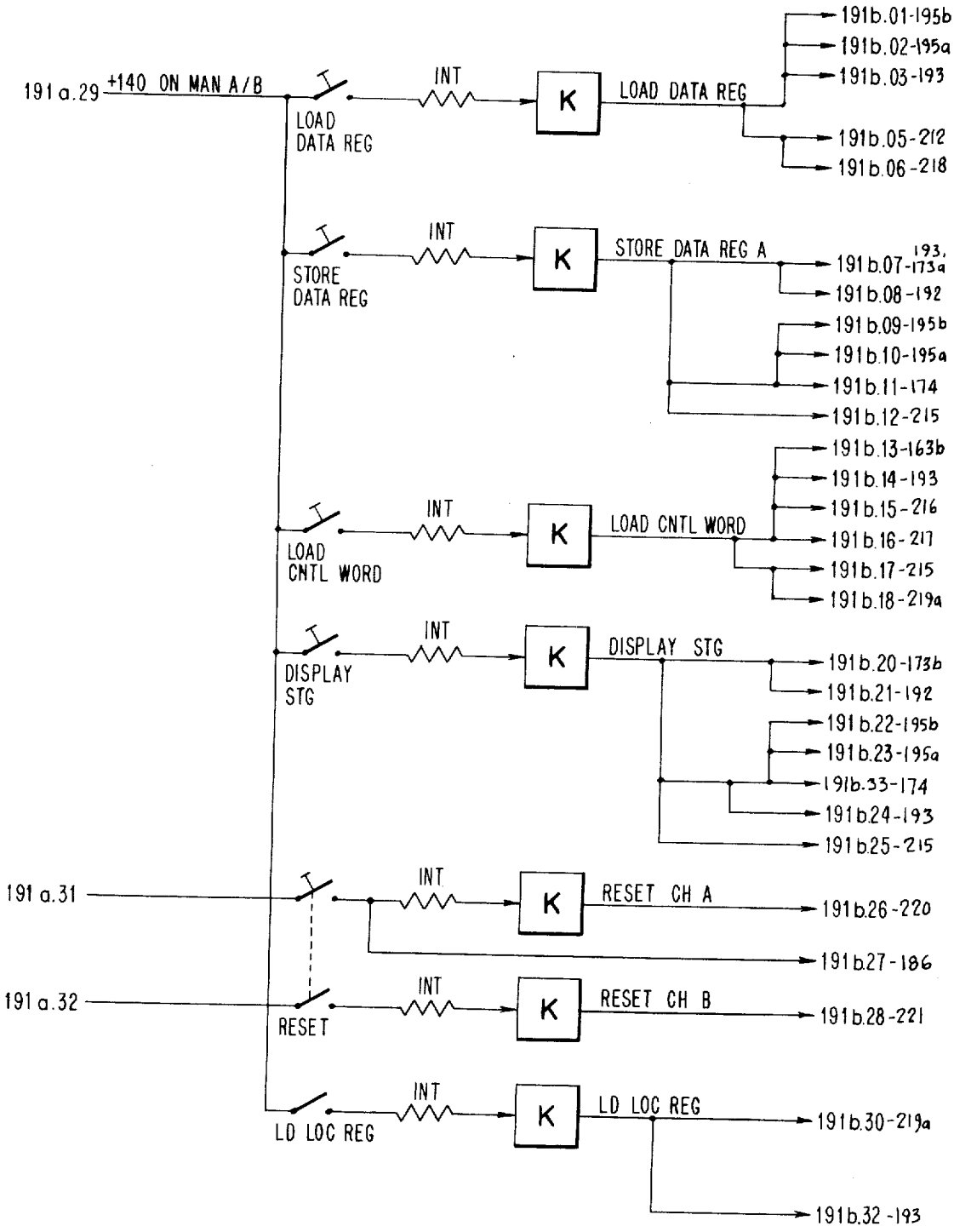
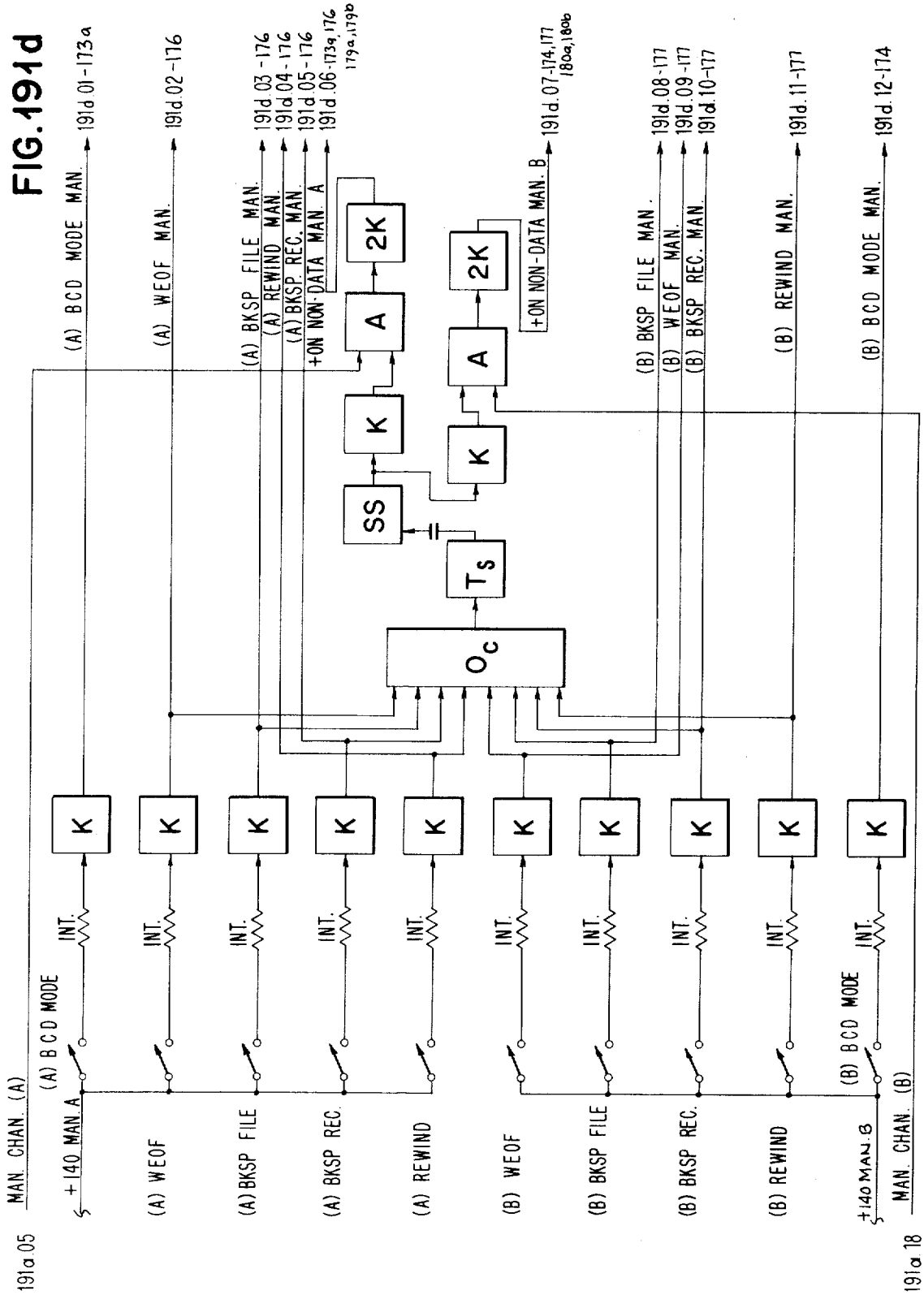


FIG. 191d


MAN. CHAN. (A)
191a.05
(A) B C D MODE
+140 MAN. A
(A) WEOF
(A) BKSP FILE
(A) BKSP REC.
(A) REWIND
(B) WEOF
(B) BKSP FILE
(B) BKSP REC.
(B) REWIND
+140 MAN. B
MAN. CHAN. (B)
191a.18
INT.
K
O_C
T_S
SS
A
2K
(A) B C D MODE MAN.
191d.01-173a
(A) WEOF MAN.
191d.02-176
(A) BKSP FILE MAN.
191d.03-176
(A) REWIND MAN.
191d.04-176
(A) BKSP. REC. MAN.
191d.05-176
+ON NON-DATA MAN. A
191d.06-173a,176
179a,179b
+ON NON-DATA MAN. B
191d.07-174,177
180a,180b
(B) BKSP FILE MAN.
191d.08-177
(B) WEOF MAN.
191d.09-177
(B) BKSP REC. MAN.
191d.10-177
(B) REWIND MAN.
191d.11-177
(B) B C D MODE MAN.
191d.12-174

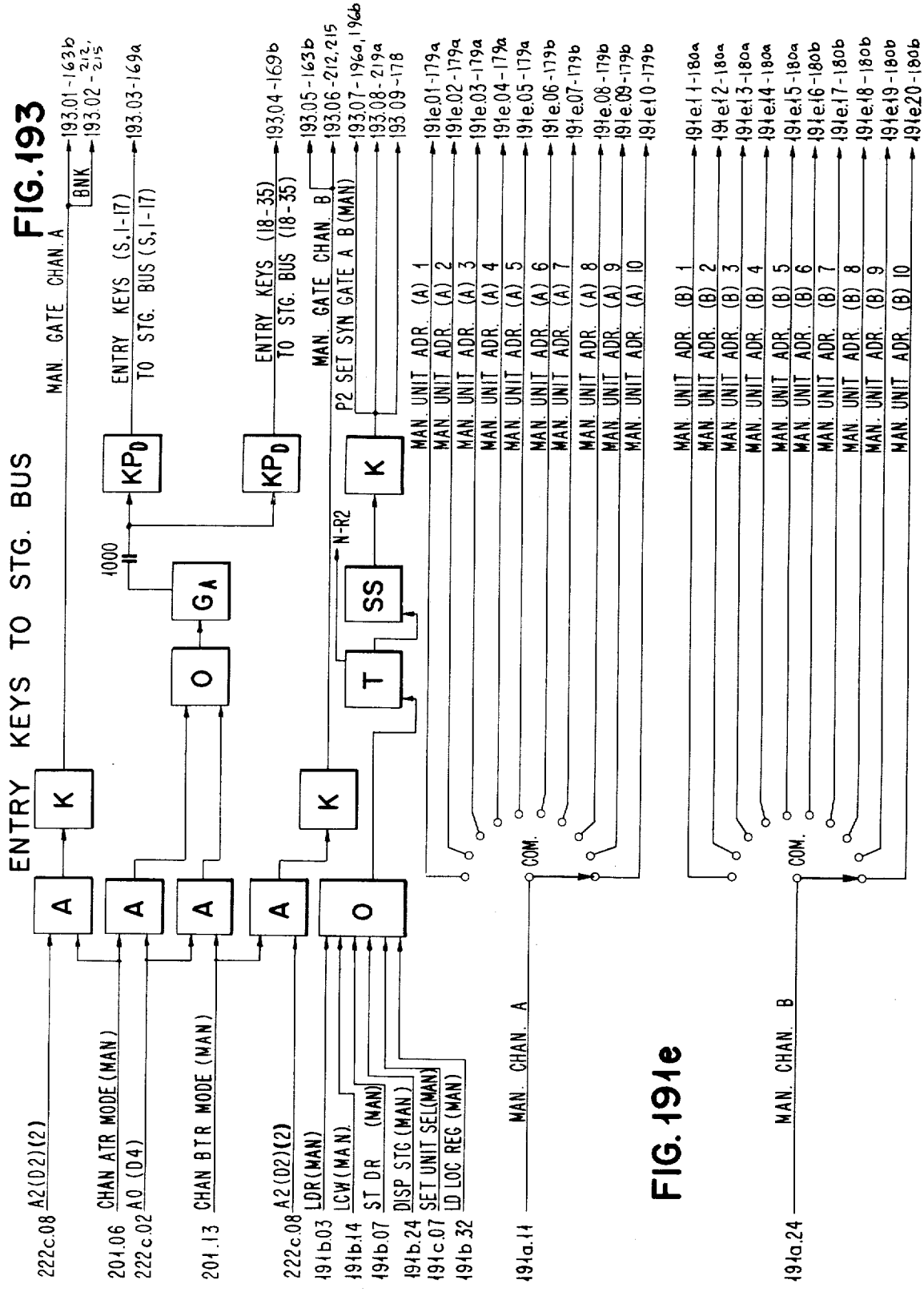


FIG. 193

FIG. 191e

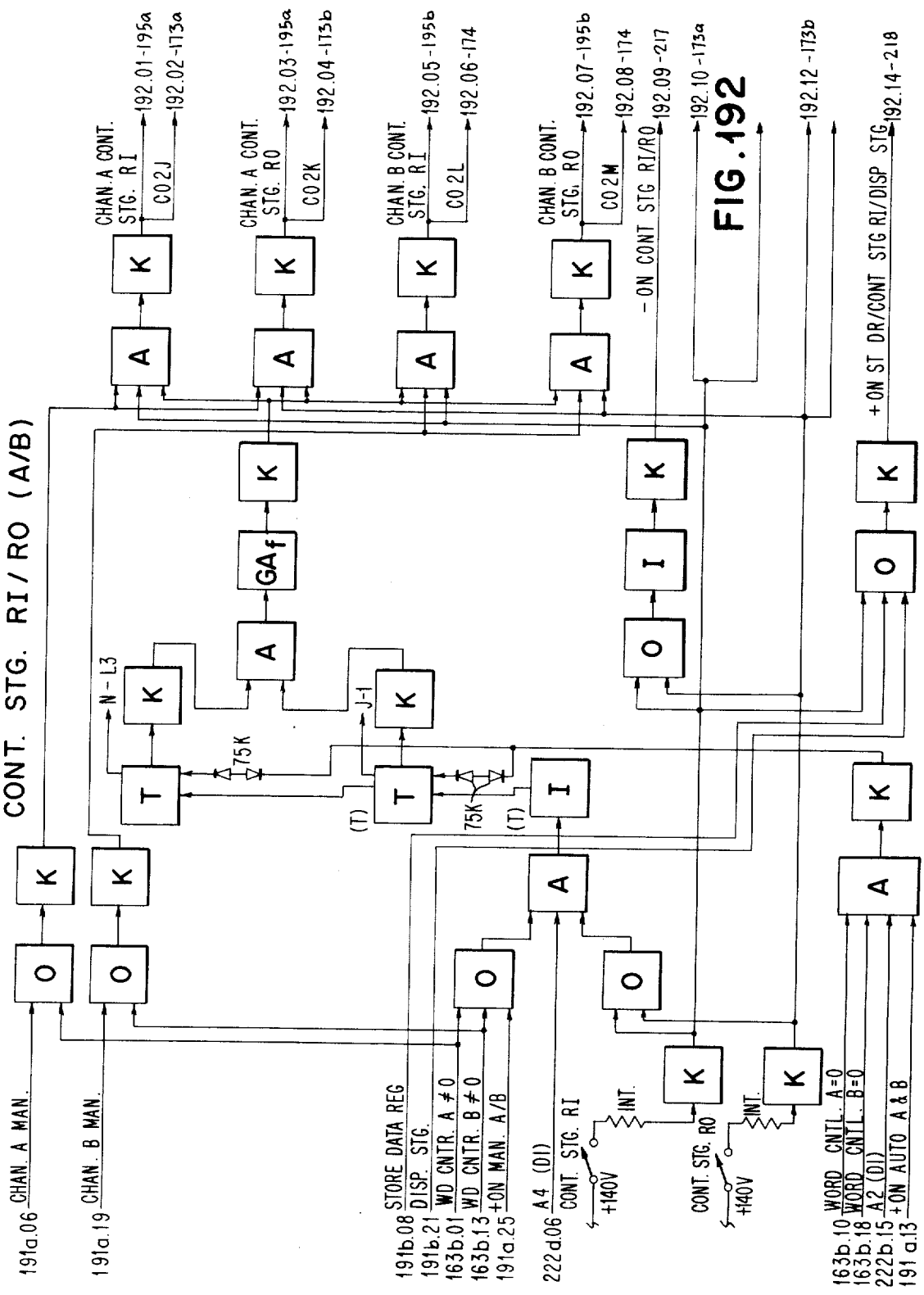
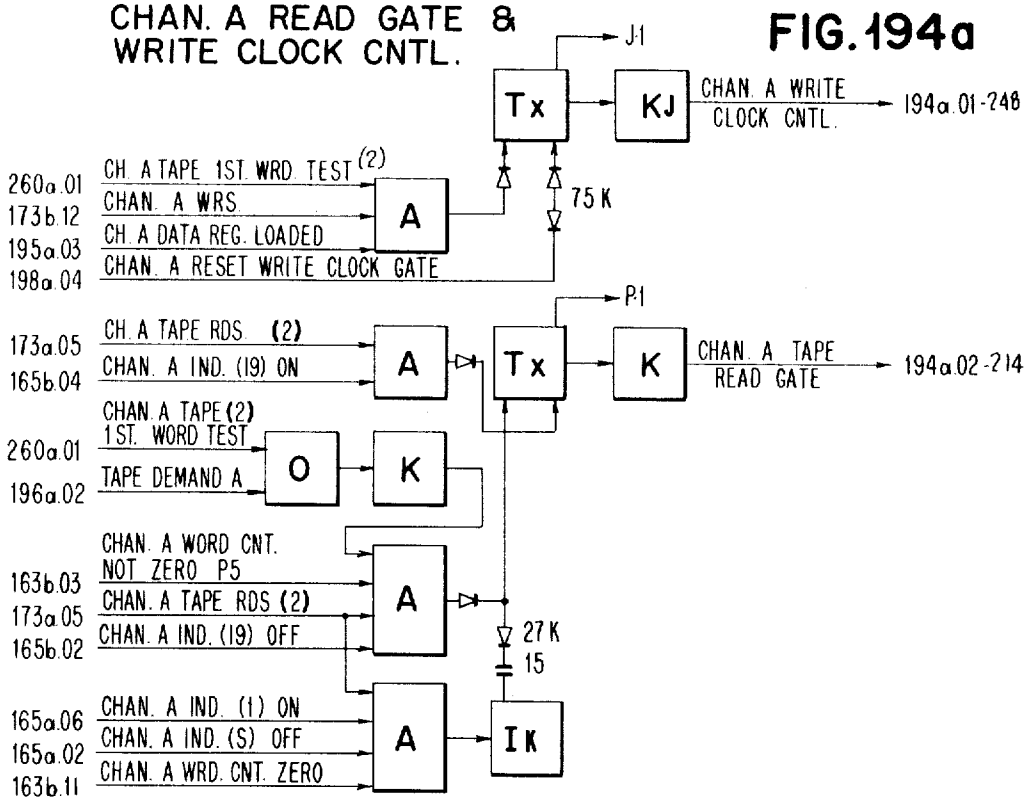

CONT. STG. RI / RO (A/B)
191a.06 CHAN. A MAN.
191a.19 CHAN. B MAN.
191b.08 STORE DATA REG
191b.21 DISP. STG.
163b.01 WD CNTR. A ≠ 0
163b.13 WD CNTR. B ≠ 0
191a.25 +ON MAN. A/B
222d.06 A4 (D1)
CONT. STG. RI
+140V
INT.
CONT. STG. RO
+140V
INT.
163b.10 WORD CNTL. A=0
163b.18 WORD CNTL. B=0
222b.15 A2 (D1)
191a.13 +ON AUTO A & B
CHAN. A CONT. STG. RI
192.01-195a
CO2J
192.02-173a
CHAN. A CONT. STG. RO
192.03-195a
CO2K
192.04-173b
CHAN. B CONT. STG. RI
192.05-195b
CO2L
192.06-174
CHAN. B CONT. STG. RO
192.07-195b
CO2M
192.08-174
-ON CONT STG RI/RO
192.09-217
192.10-173a
192.12-173b
+ON ST DR/CONT STG RI/DISP STG
192.14-218
N-L3
J-1
75K
75K
(T)
(T)

FIG. 192

CHAN. A READ GATE & WRITE CLOCK CNTL.

FIG. 194a



CHAN. B READ GATE & WRITE CLOCK CNTL.

FIG. 194b

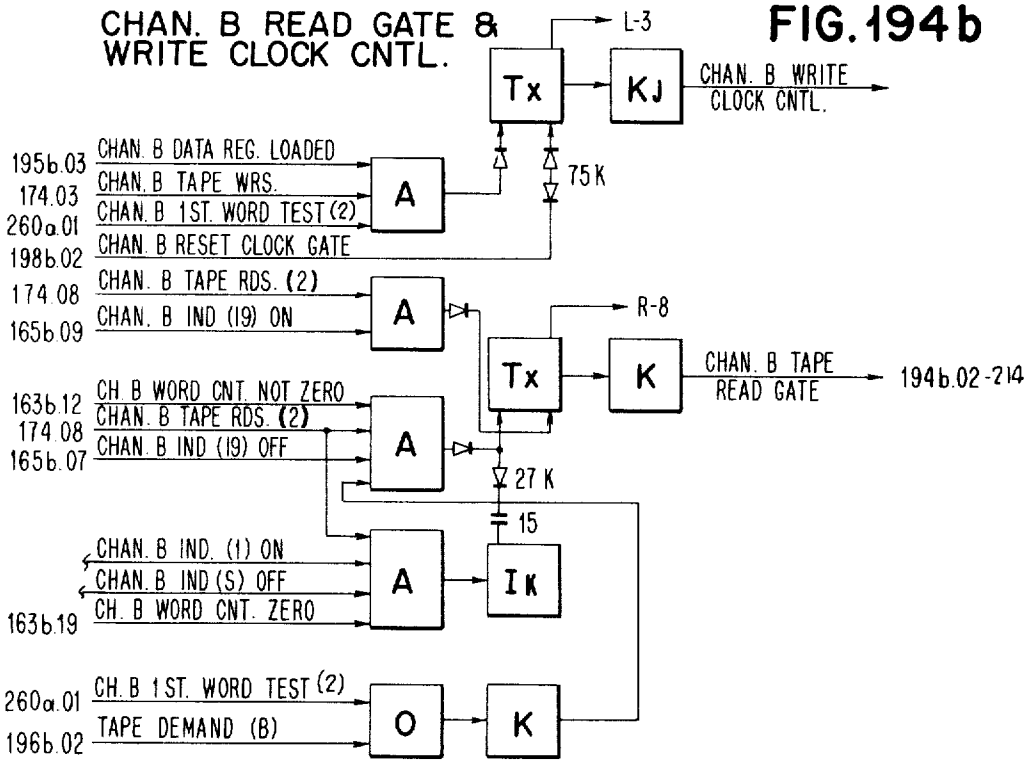
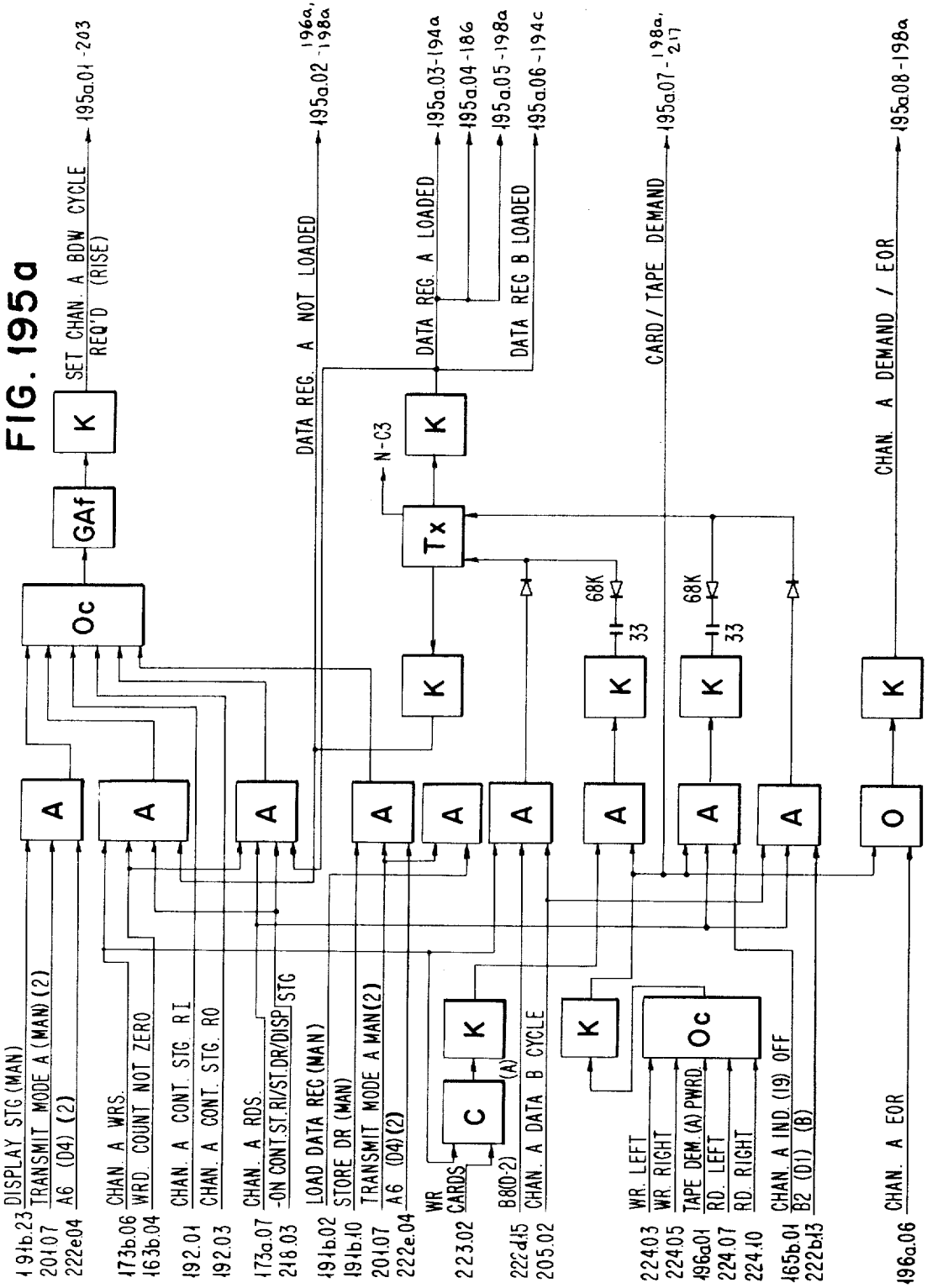


FIG. 195a



DATA REG. A LOADED & SET CHAN. A BDW CYCLE REQ'D.

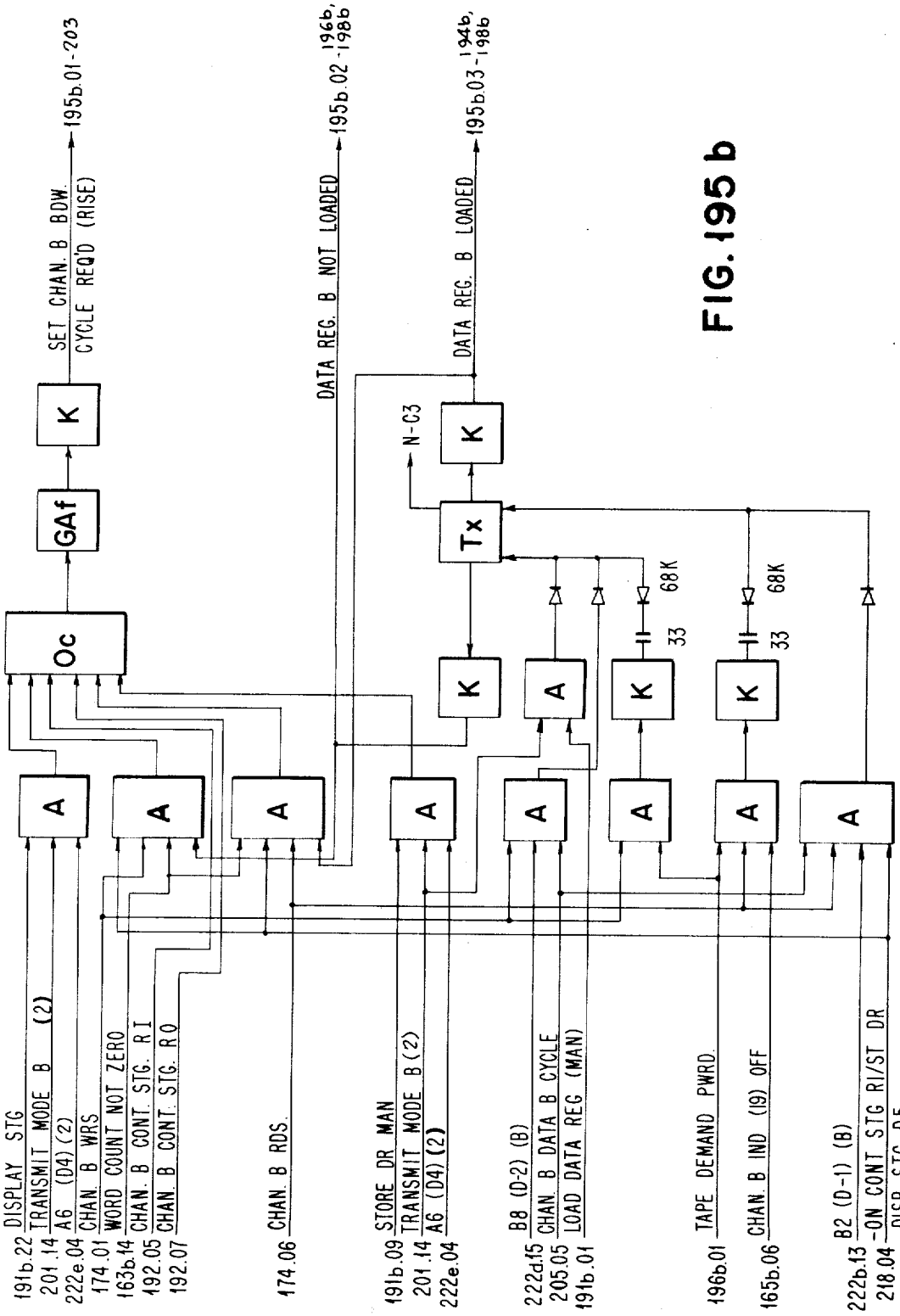


FIG. 195b

DATA REG. B LOADED & SET CHAN. B BDW CYCLE REQ'D.

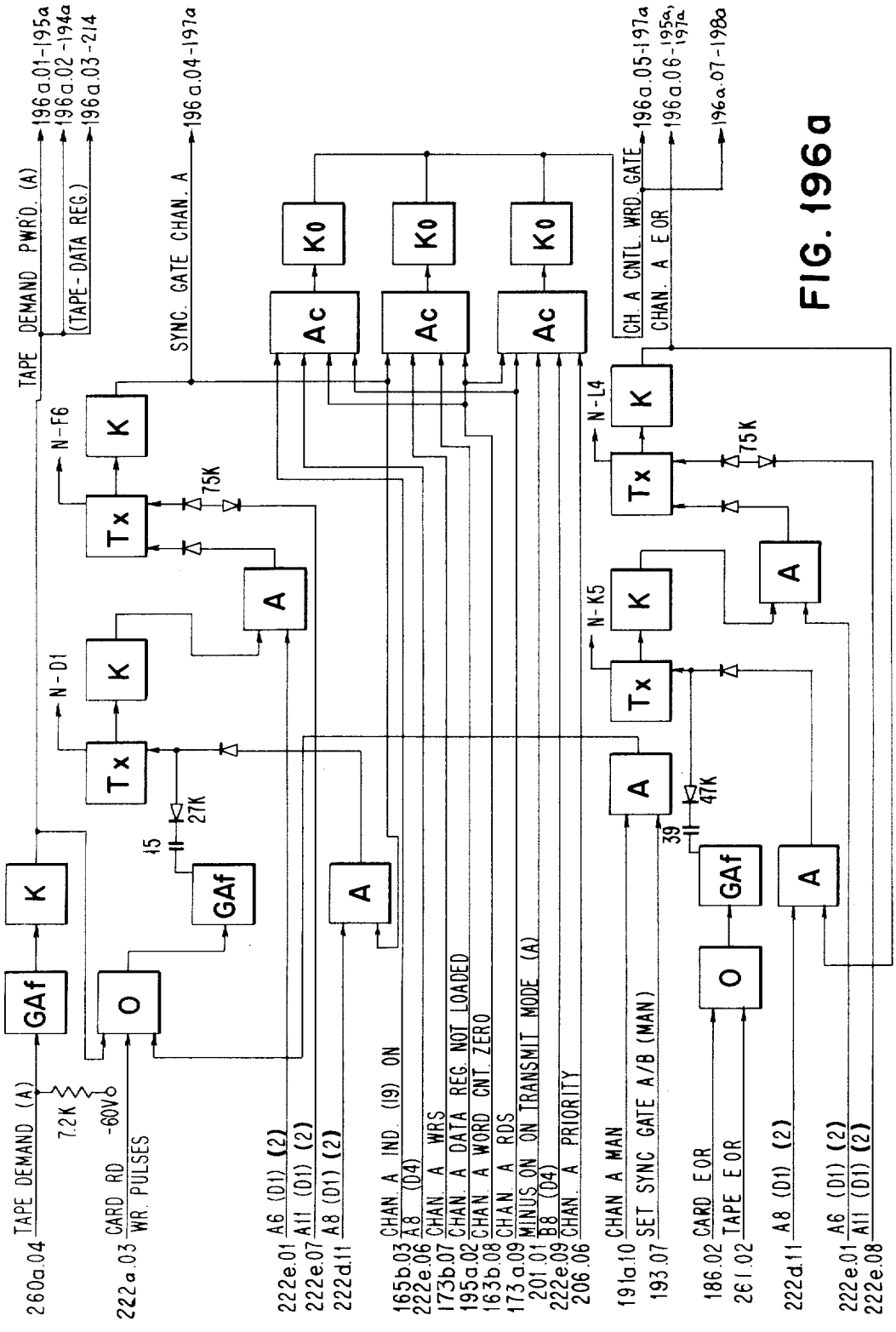


FIG. 196a

CHAN. A CNTL. WORD GATE & E OR SYNCHRONIZING

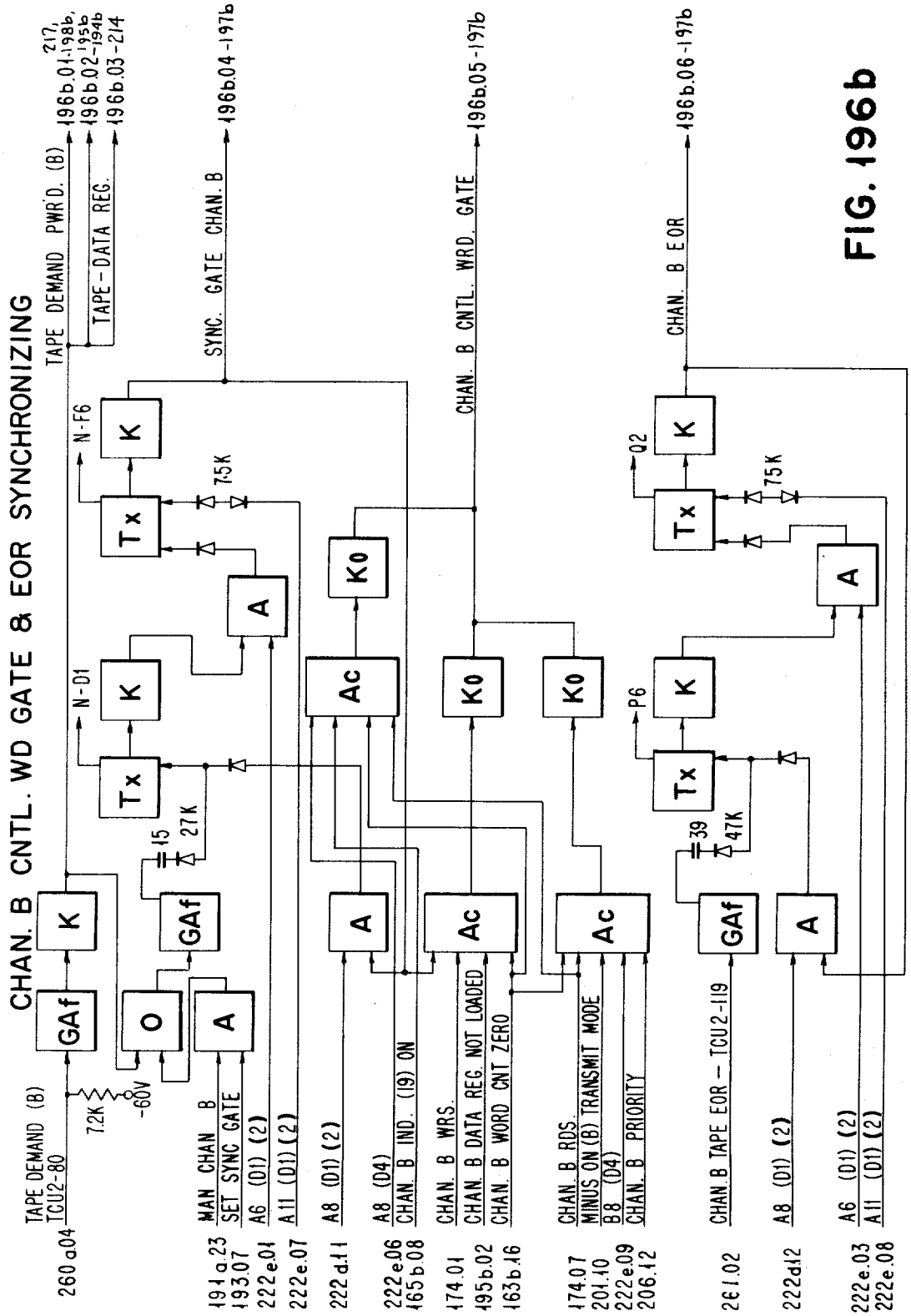

CHAN. B CNTL. WD GATE & EOR SYNCHRONIZING
TAPE DEMAND PWR'D. (B)
196b.01-198b, 217,
196b.02-195b
196b.03-214
TAPE-DATA REG.
SYNC. GATE CHAN. B
196b.04-197b
CHAN. B CNTL. WRD. GATE
196b.05-197b
CHAN. B EOR
196b.06-197b
TAPE DEMAND (B)
TCU2-80
260 a.04
7.2K
-60V
GAf
K
O
A
Tx
Ac
K0
15
27K
39
47K
75K
N-D1
N-F6
P6
Q2
MAN CHAN B
SET SYNC GATE
191 a.23
193.07
A6 (D1) (2)
222e.01
A11 (D1) (2)
222e.07
A8 (D1) (2)
222d.11
A8 (D4)
CHAN B IND. (19) ON
222e.06
165b.08
CHAN. B WRS.
CHAN. B DATA REG. NOT LOADED
CHAN. B WORD CNT ZERO
174.01
195b.02
163b.16
CHAN. B RDS.
MINUS ON (B) TRANSMIT MODE
B8 (D4)
CHAN. B PRIORITY
174.07
201.10
222e.09
206.12
CHAN B TAPE EOR — TCU2-119
261.02
A8 (D1) (2)
222d12
A6 (D1) (2)
A11 (D1) (2)
222e.03
222e.08

FIG. 196b

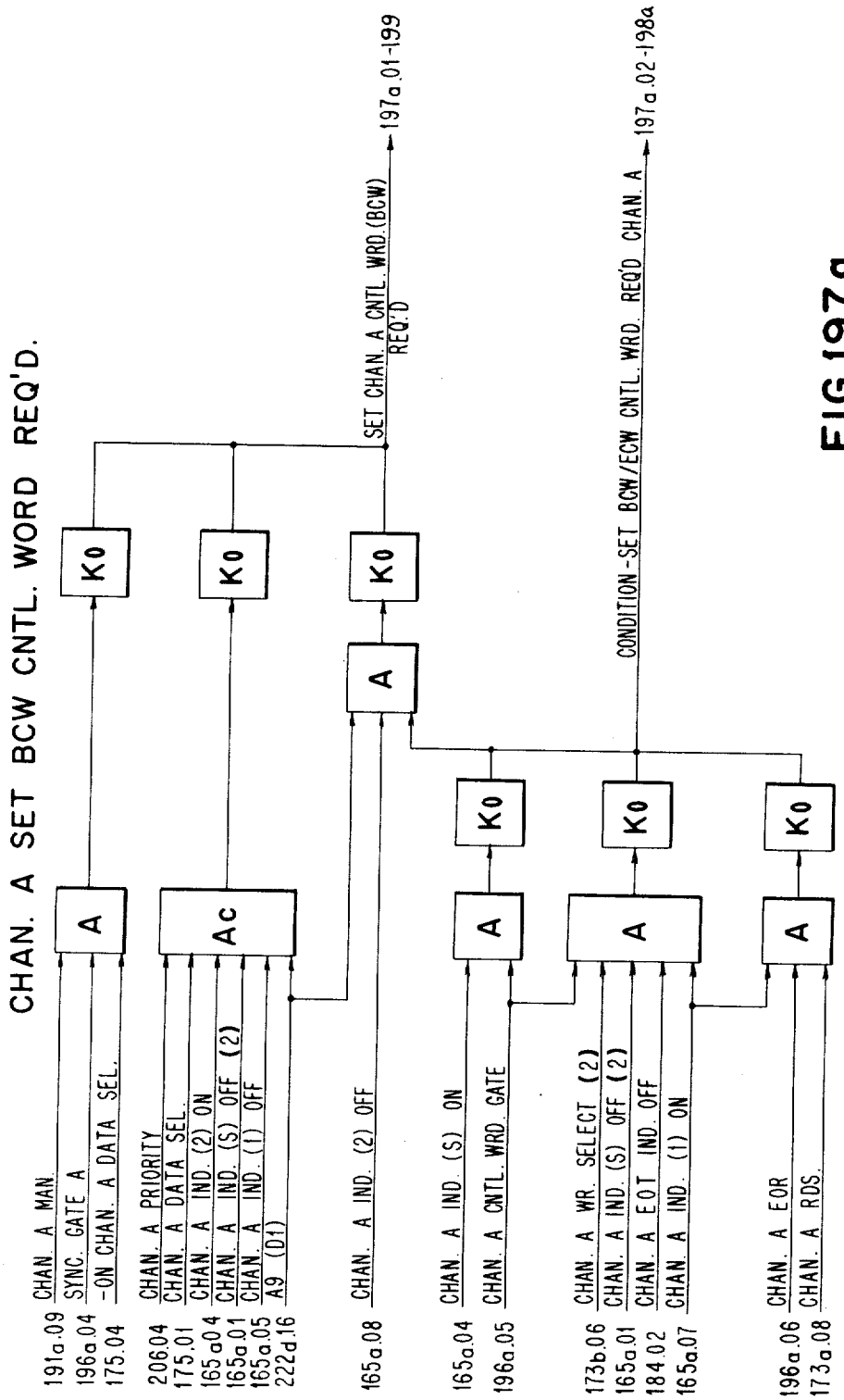

CHAN. A SET BCW CNTL. WORD REQ'D.
191a.09 CHAN. A MAN
196a.04 SYNC. GATE A
175.04 -ON CHAN. A DATA SEL.
206.04 CHAN. A PRIORITY
175.01 CHAN. A DATA SEL.
165a04 CHAN. A IND. (2) ON
165a.01 CHAN. A IND. (S) OFF (2)
165a.05 CHAN. A IND. (1) OFF
222d.16 A9 (01)
165a.08 CHAN. A IND. (2) OFF
165a.04 CHAN. A IND. (S) ON
196a.05 CHAN. A CNTL. WRD. GATE
173b.06 CHAN. A WR. SELECT (2)
165a.01 CHAN. A IND. (S) OFF (2)
184.02 CHAN. A EOT IND. OFF
165a.07 CHAN. A IND. (1) ON
196a.06 CHAN. A EOR
173a.08 CHAN. A RDS.
A
Ac
K0
SET CHAN. A CNTL. WRD. (BCW) REQ'D
197a.01-199
CONDITION-SET BCW/ECW CNTL. WRD. REQ'D CHAN. A
197a.02-198a

FIG.197a

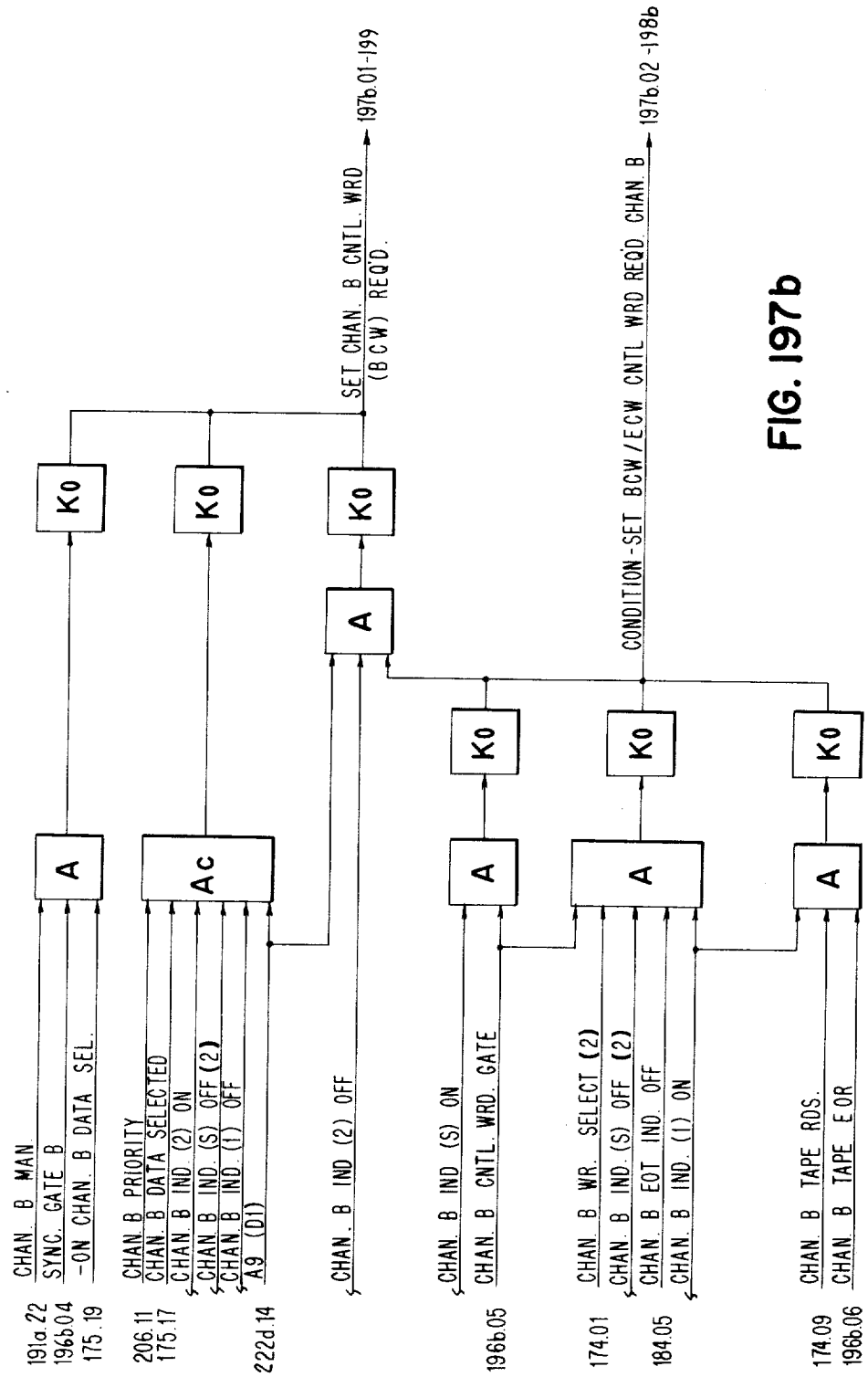

CHAN. B SET BCW CNTL. WORD REQ'D.
CHAN. B MAN
SYNC. GATE B
-ON CHAN. B DATA SEL.
191a.22
196b.04
175.19
A
K0
CHAN B PRIORITY
CHAN. B DATA SELECTED
CHAN. B IND (2) ON
CHAN. B IND. (S) OFF (2)
CHAN. B IND. (1) OFF
A9 (D1)
206.11
175.17
222d.14
Ac
K0
CHAN. B IND (2) OFF
A
K0
SET CHAN. B CNTL. WRD (BCW) REQ'D.
197b.01-199
CONDITION-SET BCW/ECW CNTL WRD REQ'D. CHAN. B
197b.02-198b
CHAN. B IND (S) ON
CHAN. B CNTL. WRD. GATE
196b.05
A
K0
CHAN. B WR. SELECT (2)
CHAN. B IND. (S) OFF (2)
CHAN. B EOT IND. OFF
CHAN. B IND. (1) ON
174.01
184.05
A
K0
CHAN. B TAPE RDS.
CHAN. B TAPE E OR
174.09
196b.06
A
K0

FIG. 197b

FIG. 198a. (SHEET 1 OF 2) CHAN A SET ECW CNTL WRD REQ'D & DATA DISCONNECT

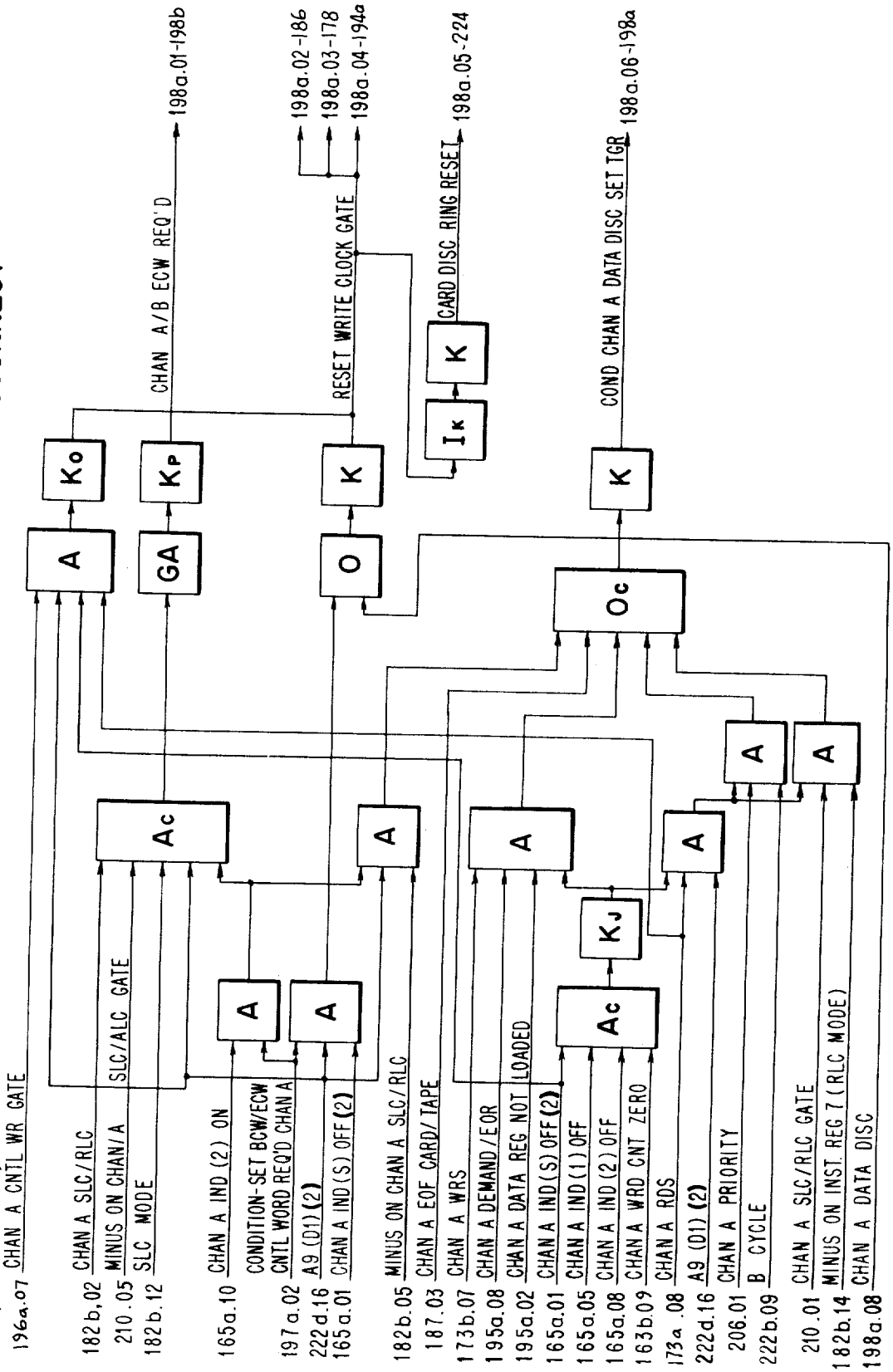


FIG. 198a. CHAN A SET ECW CNTL WRD REQD & DATA DISCONNECT
(SHEET 2 OF 2)

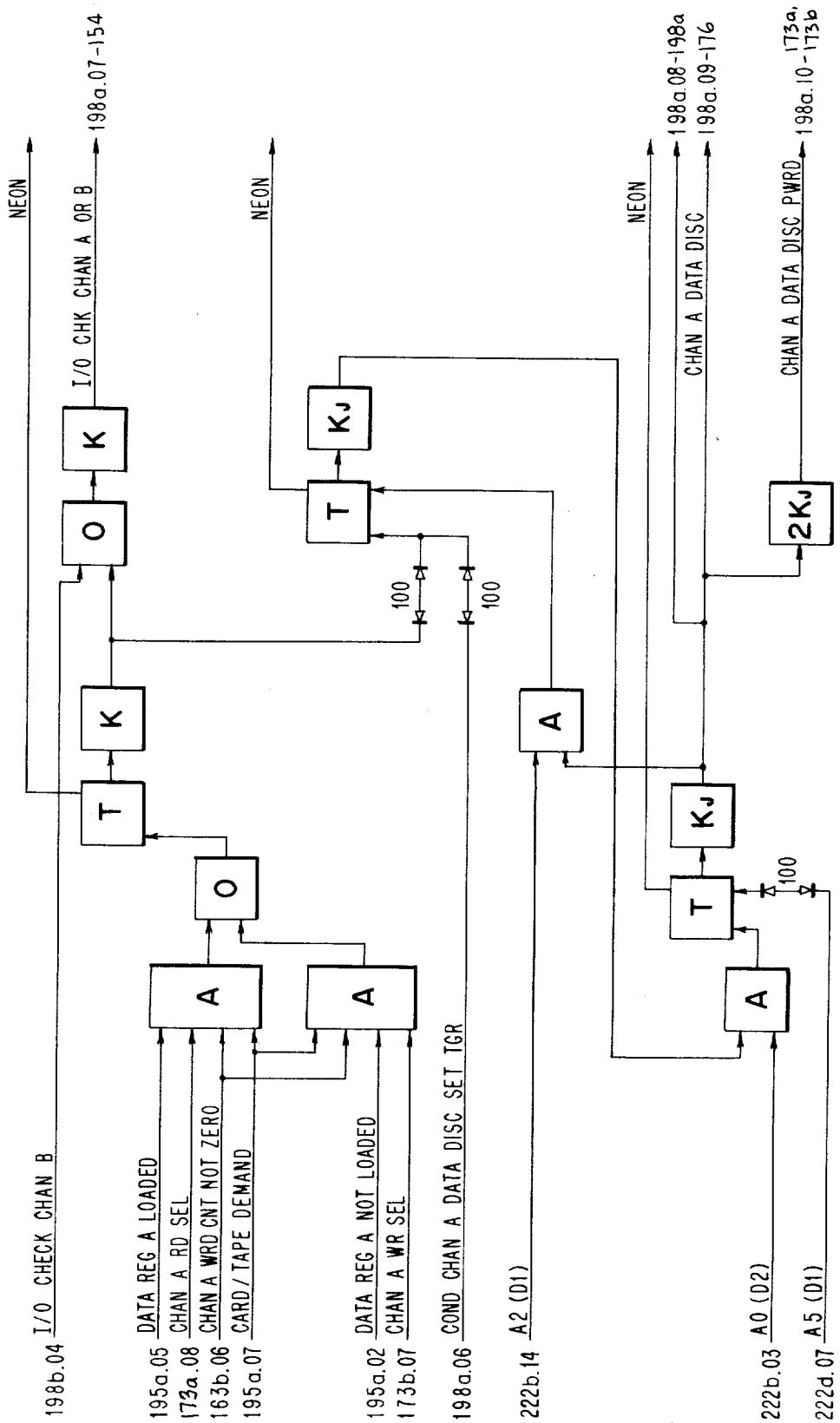


FIG. 198b. (SHEET 1 OF 2) CHAN B SET ECW CNTL WRD & DATA DISCONNECT

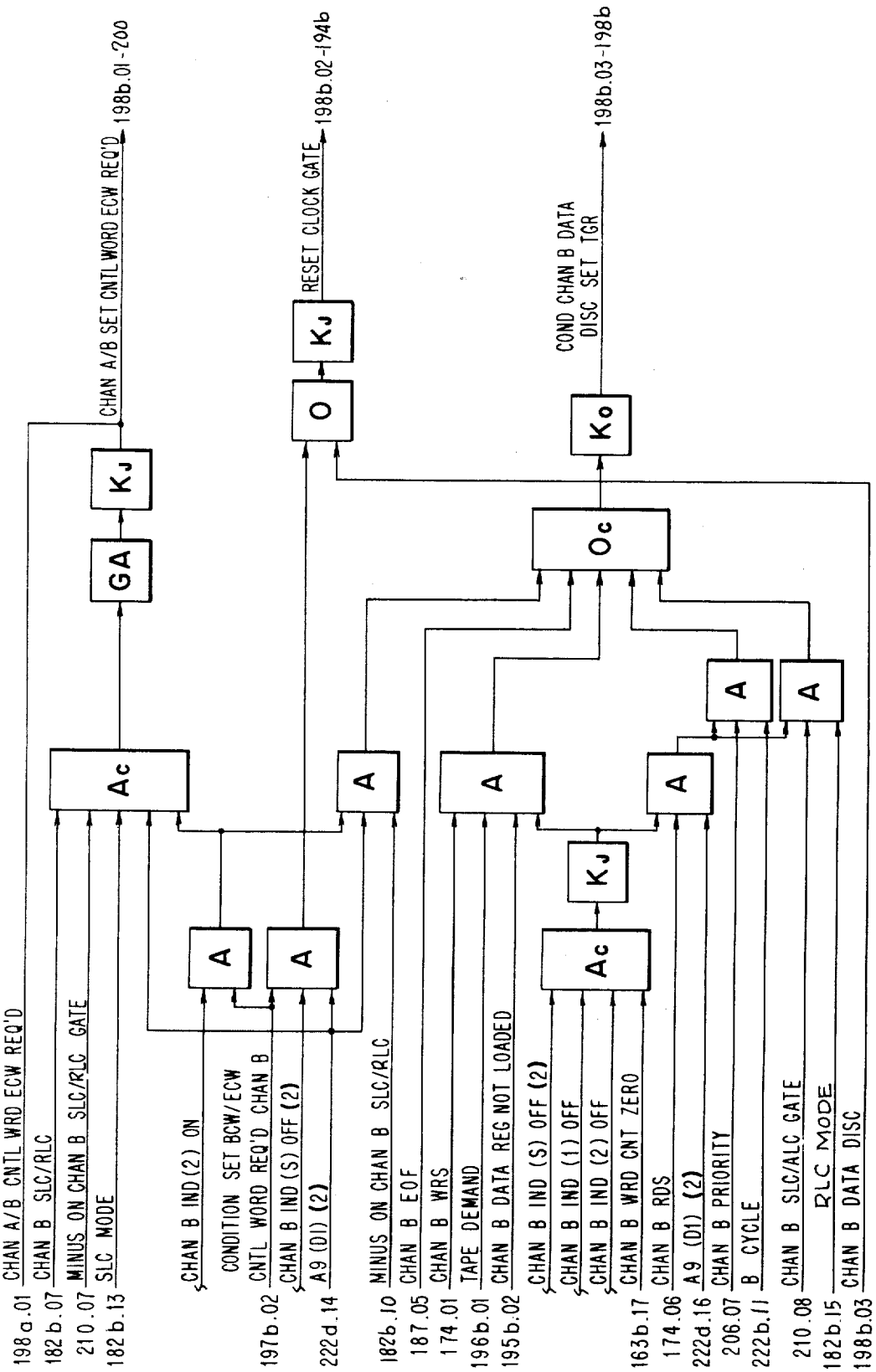
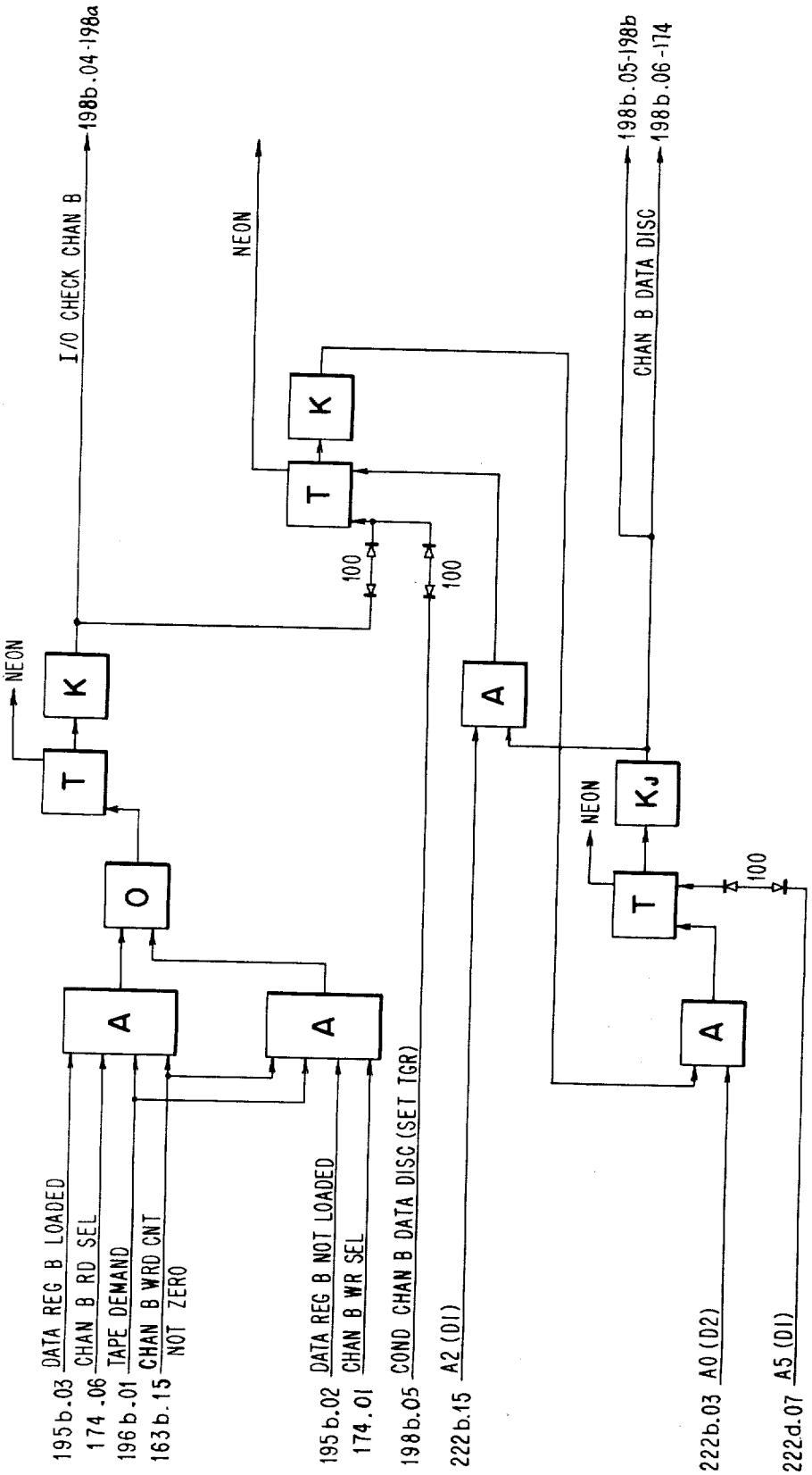


FIG. 198b.
(SHEET 2 OF 2)

CHAN B SET ECW CNTL WRD & DATA DISCONNECT



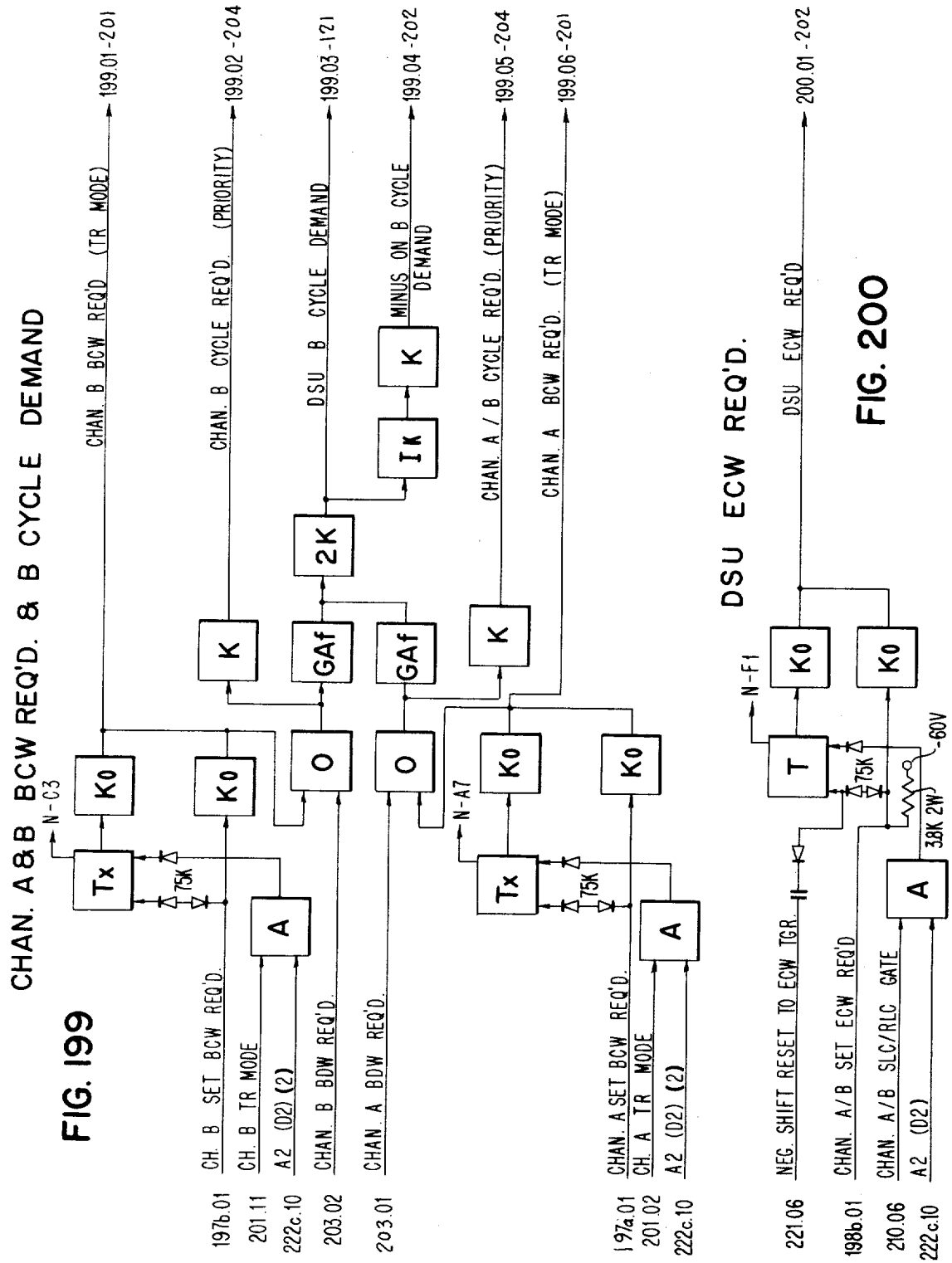
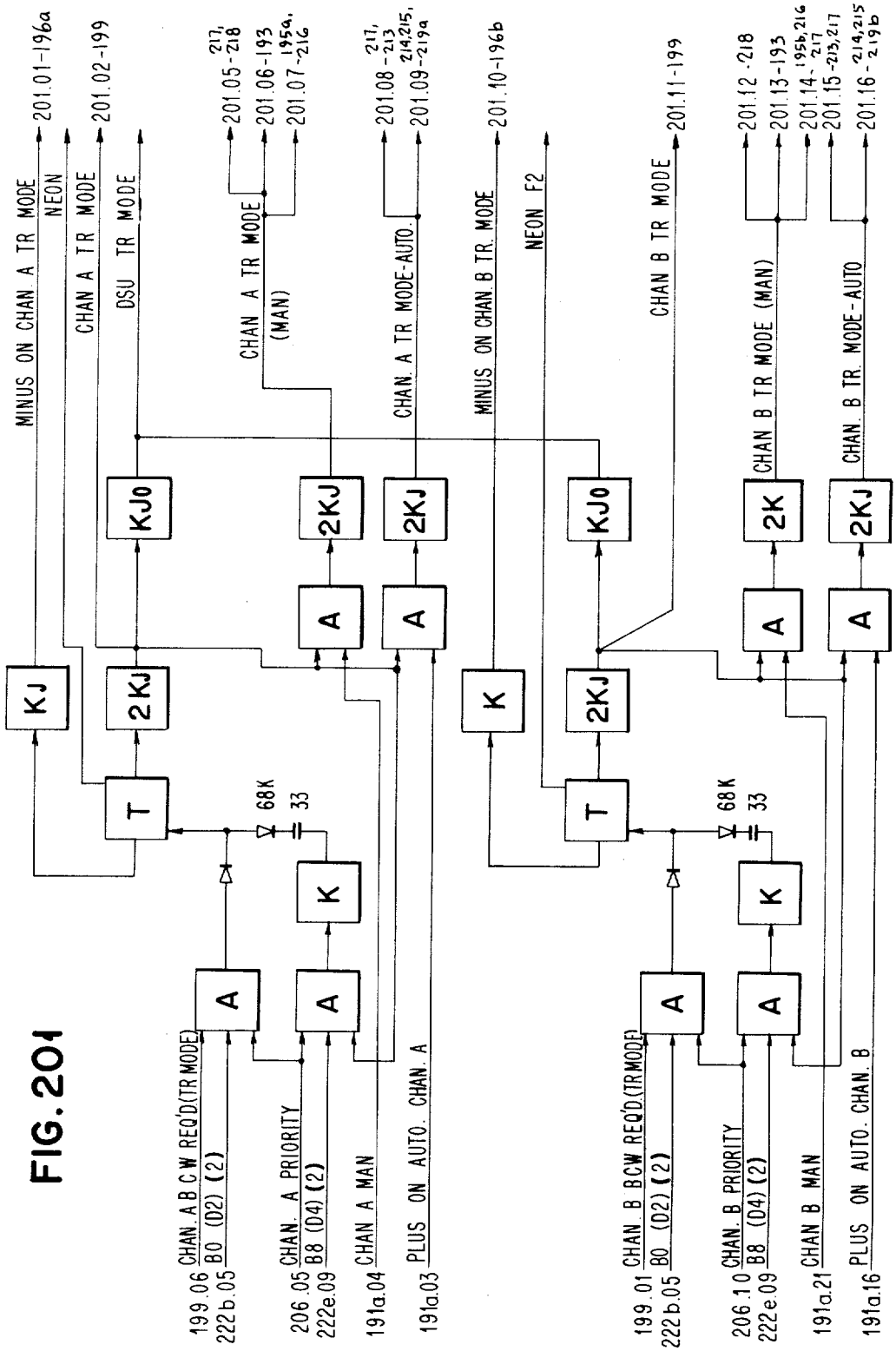


FIG. 199

FIG. 200

FIG. 204

CHAN. A & B TRANSMIT MODE TGRS.



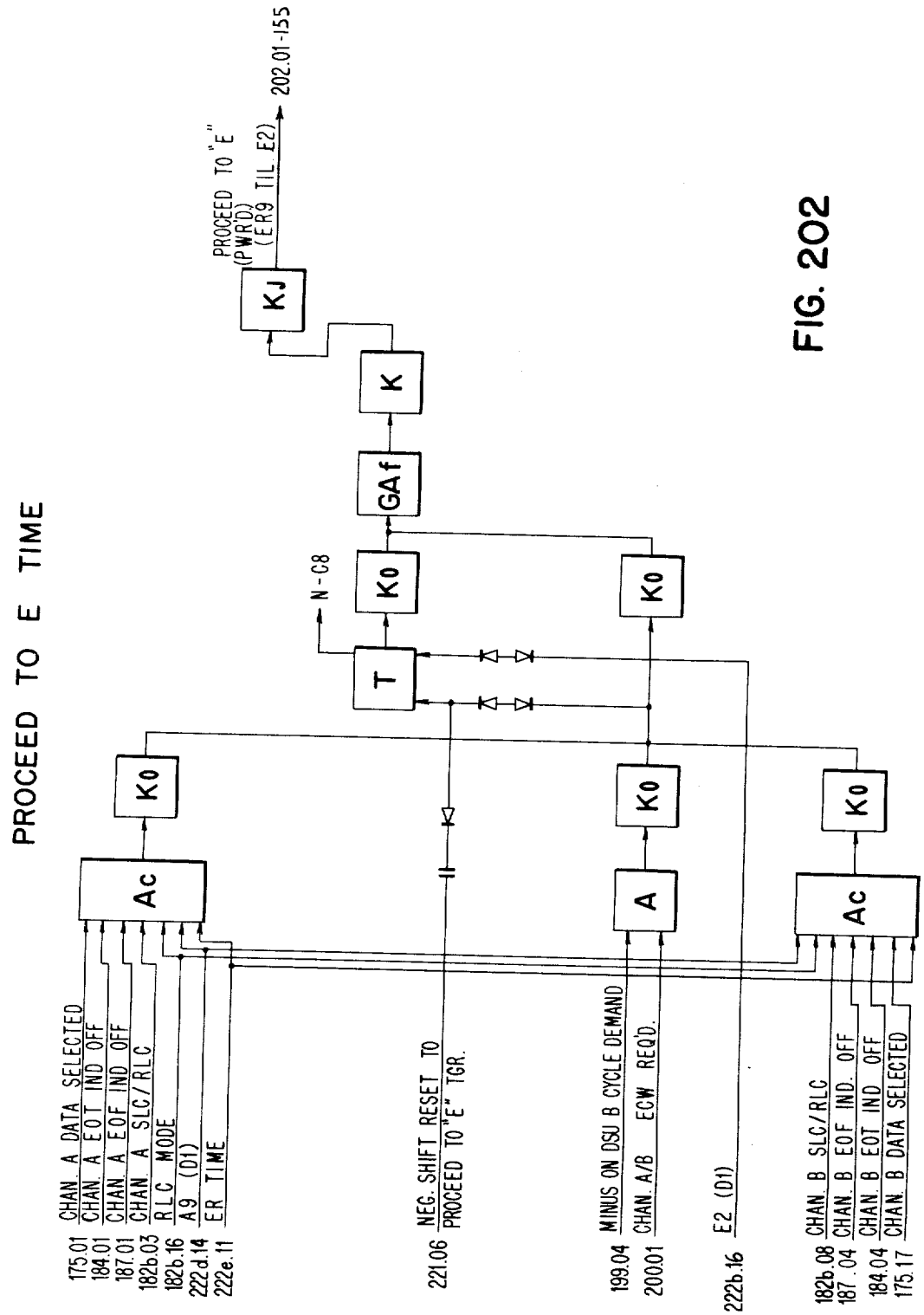

PROCEED TO E TIME
175.01 CHAN. A DATA SELECTED
184.01 CHAN. A EOT IND OFF
187.01 CHAN. A EOF IND OFF
182b.03 CHAN. A SLC/RLC
182b.16 RLC MODE
222d.14 A9 (D1)
222e.11 ER TIME
Ac
K0
221.06 NEG. SHIFT RESET TO PROCEED TO "E" TGR.
T
N-C8
K0
GAf
K
KJ
PROCEED TO "E" (PWRD) (ER9 TIL E2)
202.01-155
199.04 MINUS ON DSU B CYCLE DEMAND
200.01 CHAN. A/B ECW REQ'D.
A
K0
222b.16 E2 (D1)
K0
182b.08 CHAN. B SLC/RLC
187.04 CHAN. B EOF IND. OFF
184.04 CHAN. B EOT IND OFF
175.17 CHAN. B DATA SELECTED
Ac

FIG. 202

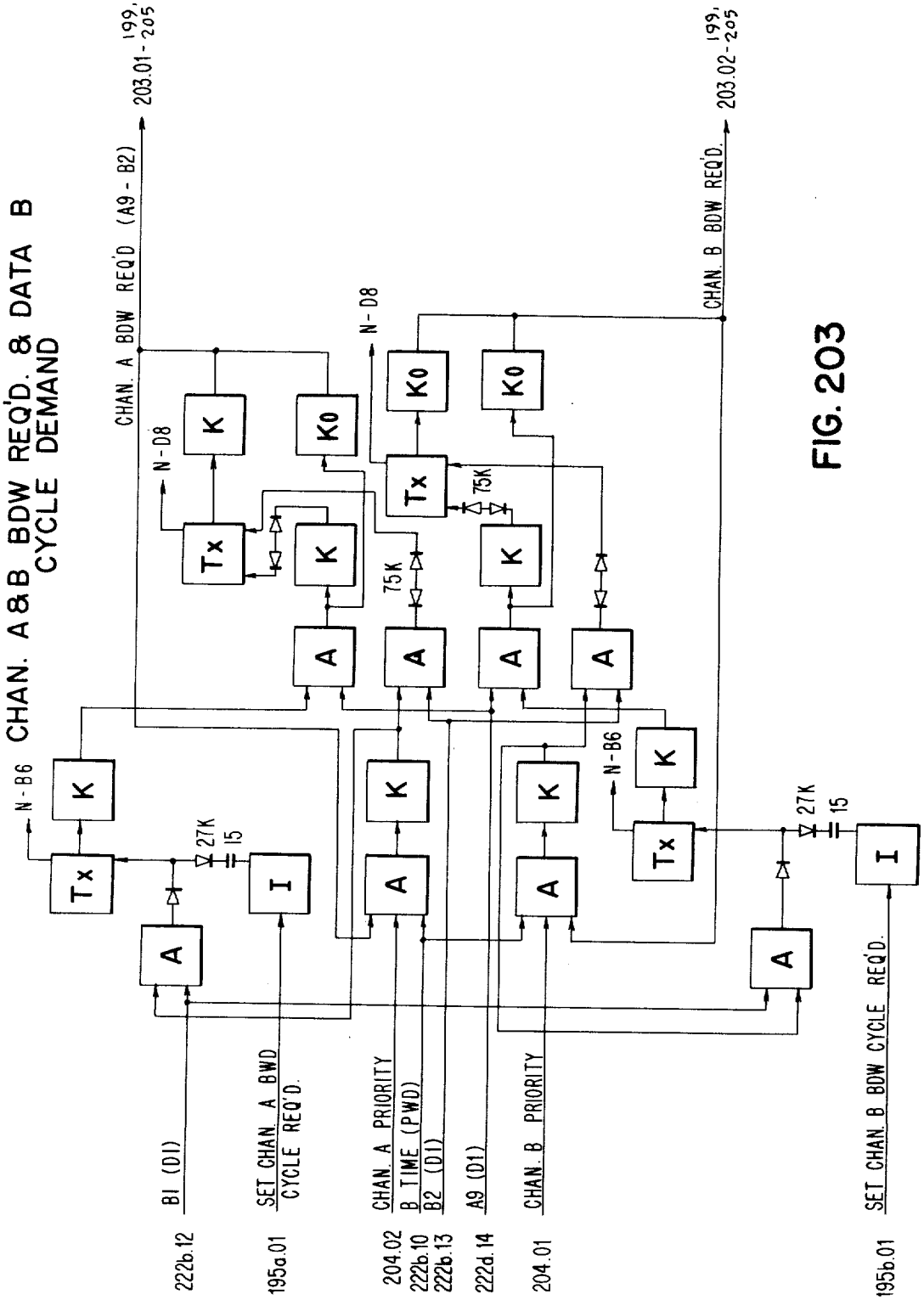

CHAN. A&B BDW REQ'D. & DATA B CYCLE DEMAND
N-B6
K
Tx
27K
15
I
A
B1 (D1)
222b.12
SET CHAN. A BWD CYCLE REQ'D.
195a.01
CHAN. A BDW REQ'D (A9-B2)
203.01-199,205
N-D8
K
Tx
K0
75K
A
CHAN. A PRIORITY
204.02
B TIME (PWD)
222b.10
B2 (D1)
222b.13
A9 (D1)
222d.14
CHAN. B PRIORITY
204.01
CHAN. B BDW REQ'D.
203.02-199,205
SET CHAN. B BDW CYCLE REQ'D.
195b.01

FIG. 203

CHANNEL & DSU PRIORITY REQ'D.

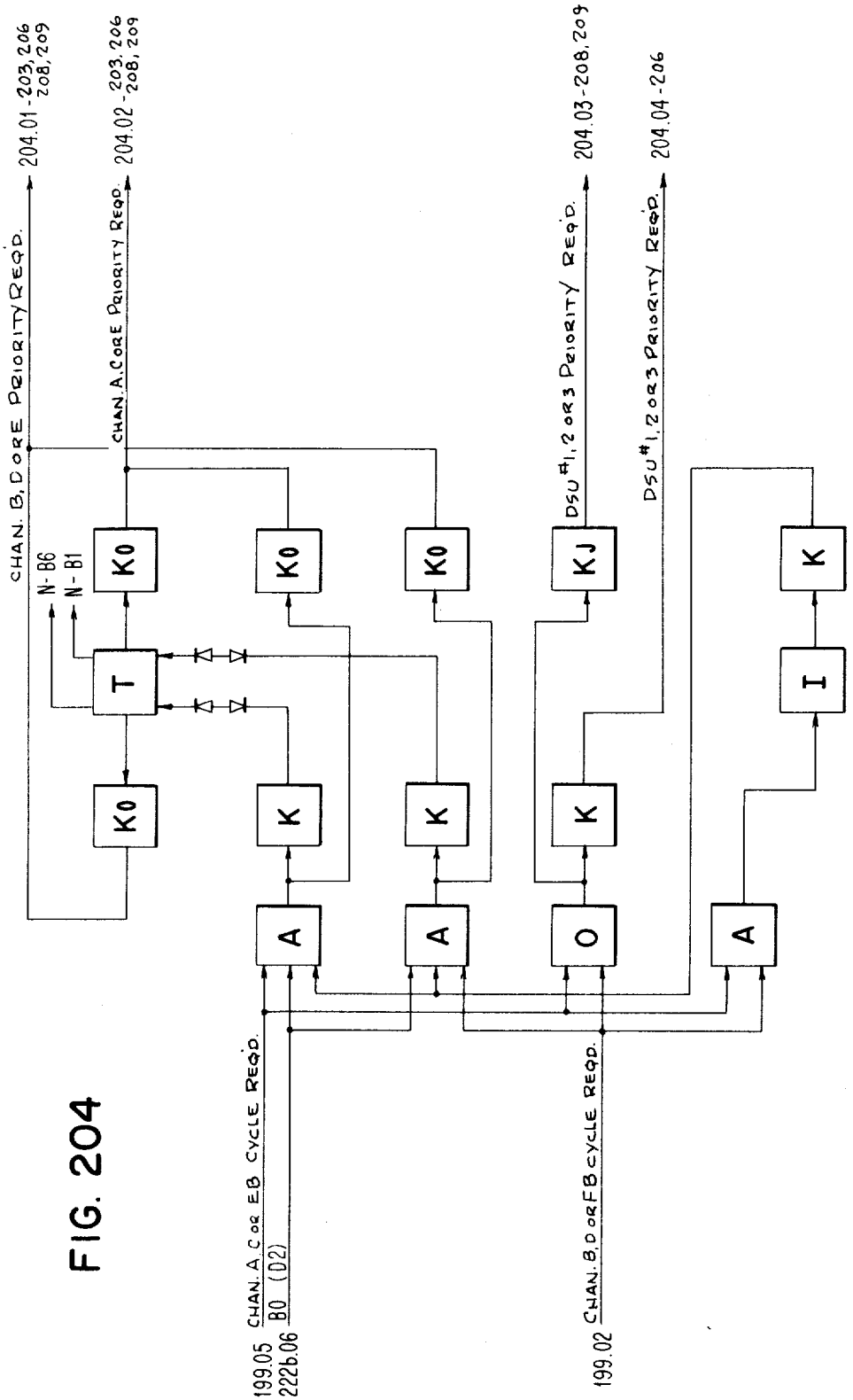


FIG. 204

CHANNEL A&B DATA B CYCLE TRIGGERS

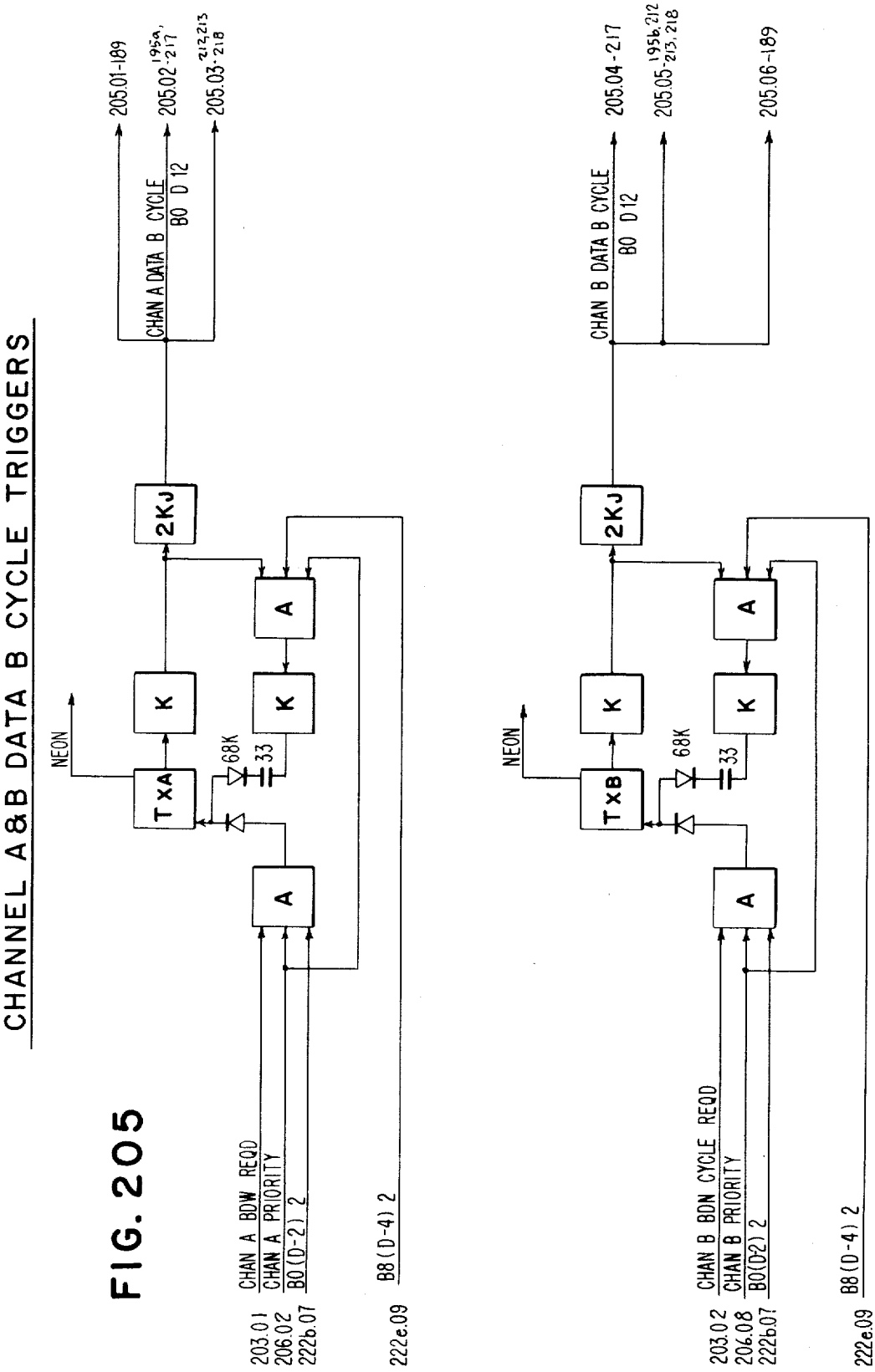


FIG. 205

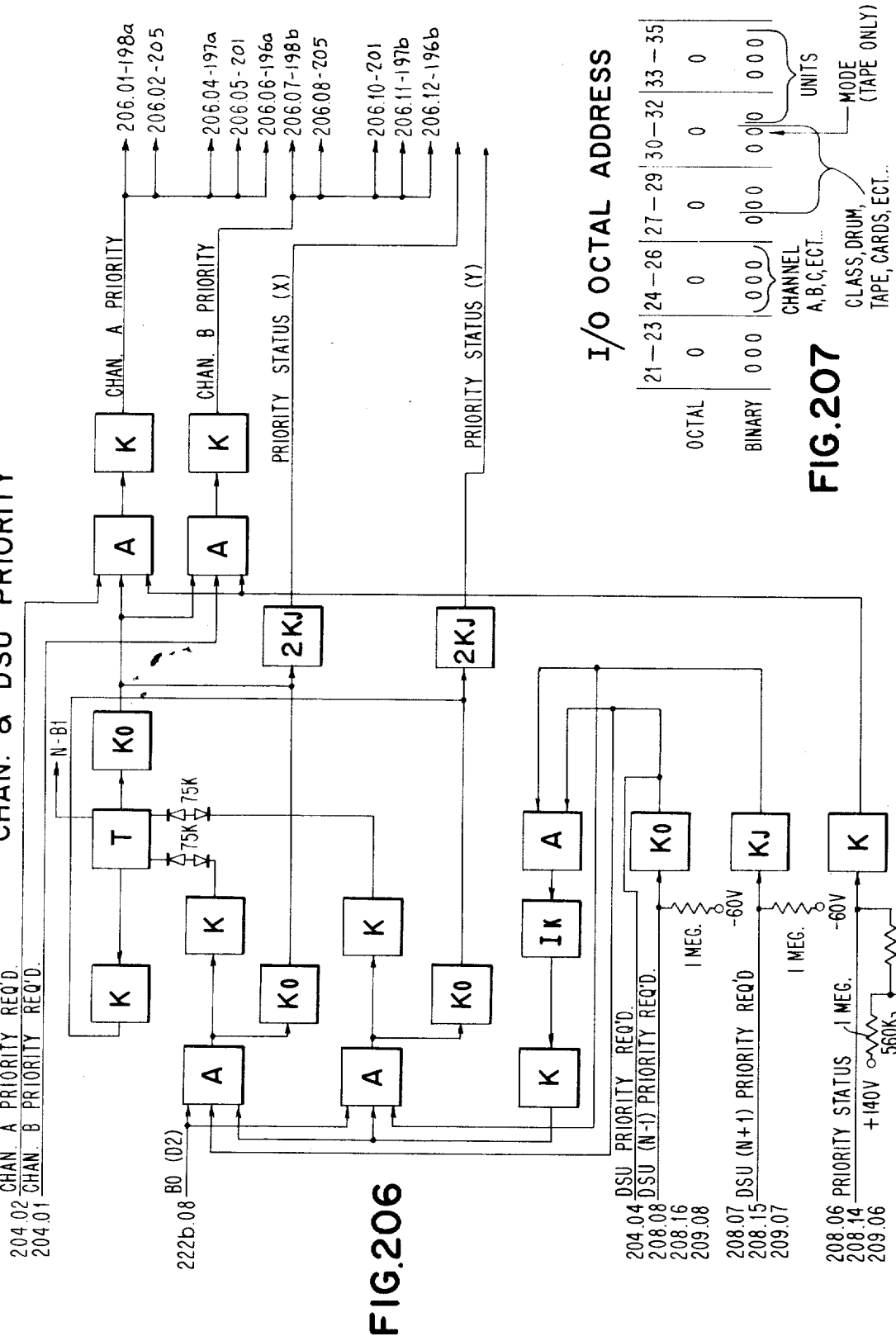


FIG.206

I/O OCTAL ADDRESS

	21–23	24–26	27–29	30–32	33–35
OCTAL	0	0	0	0	0
BINARY	000	000	000	000	000

CHANNEL A,B,C,ECT...

CLASS, DRUM, TAPE, CARDS, ECT...

UNITS

MODE (TAPE ONLY)

FIG.207

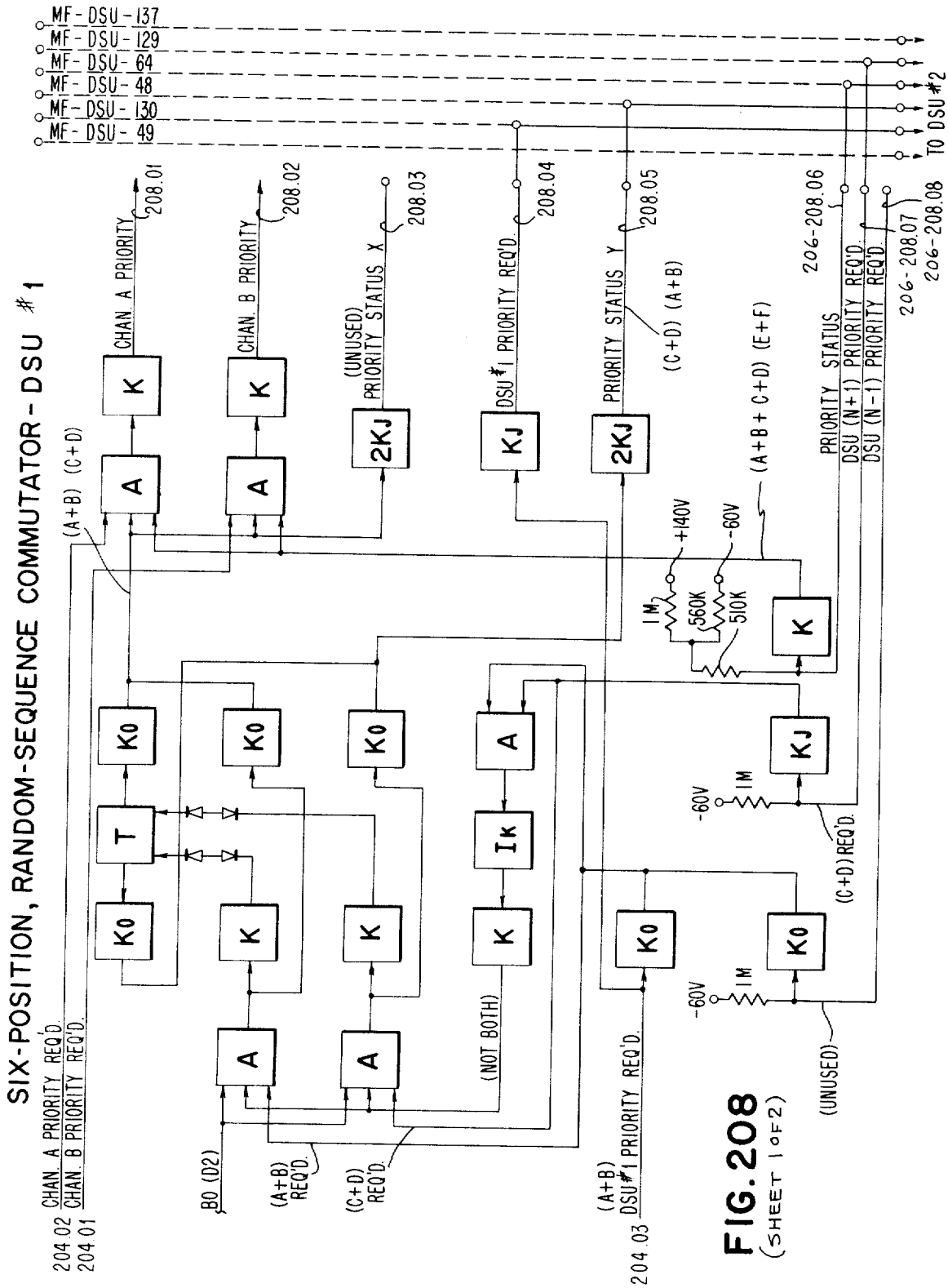


FIG. 208
(SHEET 1 OF 2)

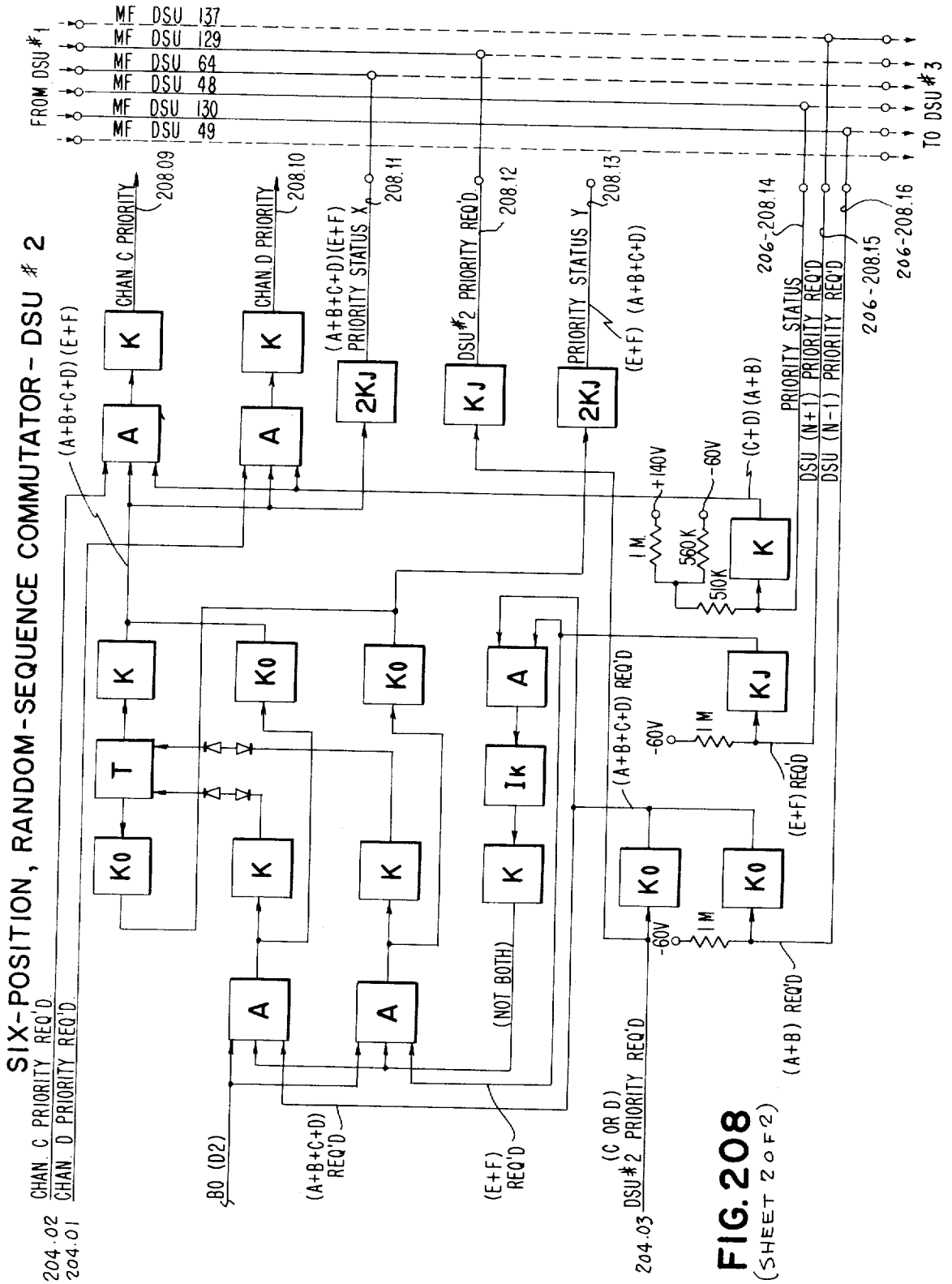


FIG. 208
(SHEET 2 OF 2)

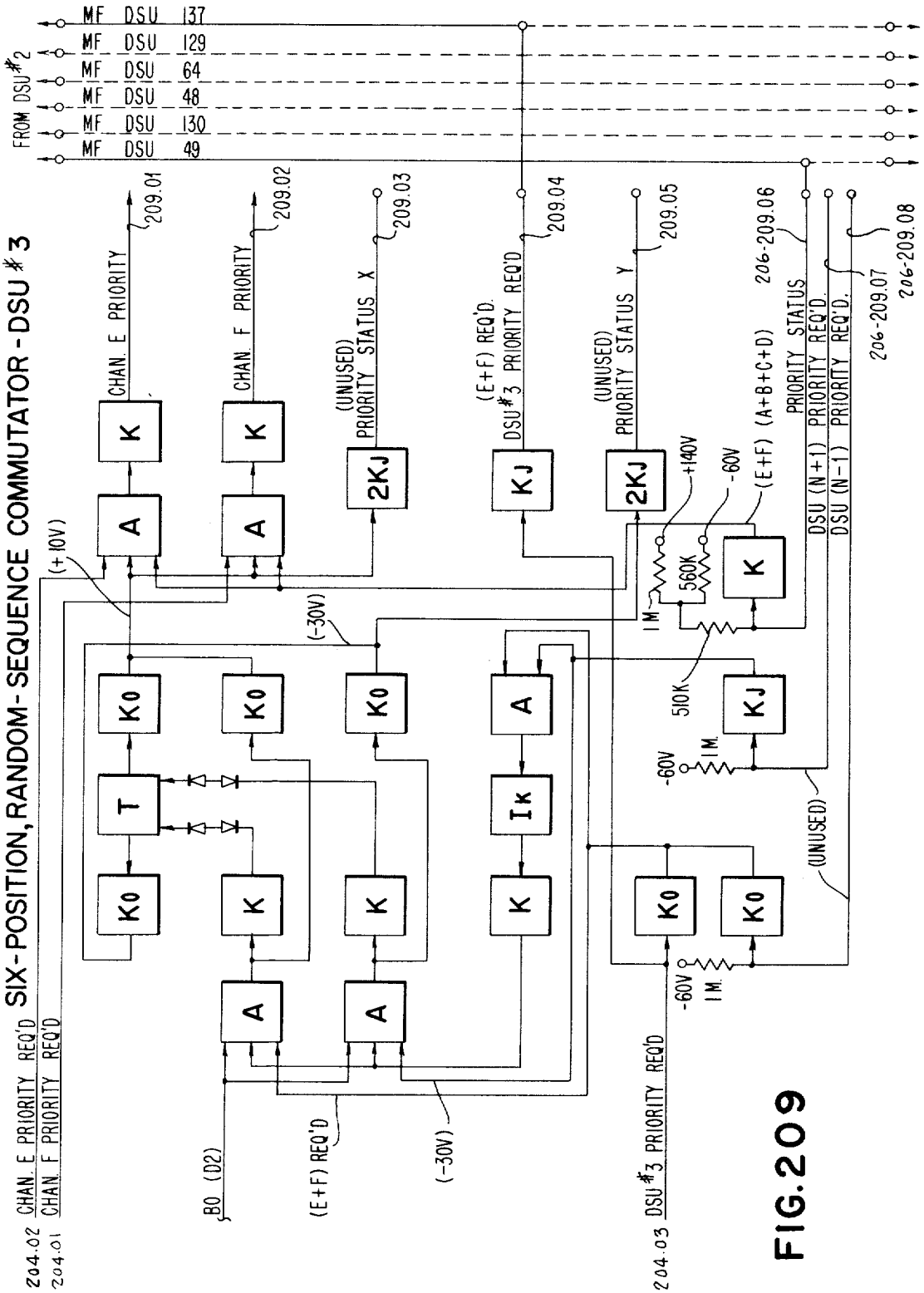

SIX-POSITION, RANDOM-SEQUENCE COMMUTATOR - DSU # 3
FROM DSU #2
MF DSU 137
MF DSU 129
MF DSU 64
MF DSU 48
MF DSU 130
MF DSU 49
CHAN. E PRIORITY
CHAN. F PRIORITY
(UNUSED) PRIORITY STATUS X
(E+F) REQ'D. DSU #3 PRIORITY REQ'D
(UNUSED) PRIORITY STATUS Y
PRIORITY STATUS DSU (N+1) PRIORITY REQ'D. DSU (N-1) PRIORITY REQ'D.
(E+F) (A+B+C+D)
209.01
209.02
209.03
209.04
209.05
206-209.06
206-209.07
206-209.08
(+10V)
(-30V)
+140V
-60V
1M
560K
510K
B0 (D2)
(E+F) REQ'D
204.02 CHAN. E PRIORITY REQ'D
204.01 CHAN. F PRIORITY REQ'D
204.03 DSU #3 PRIORITY REQ'D
(UNUSED)

FIG.209

FIG. 210

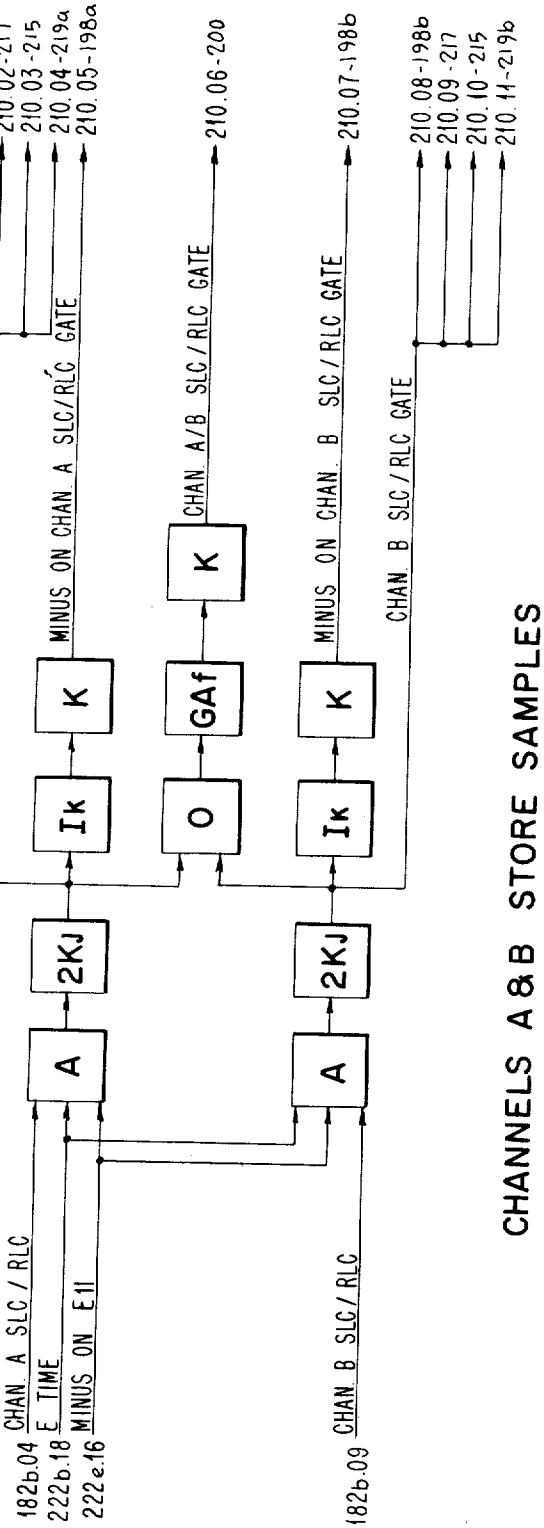
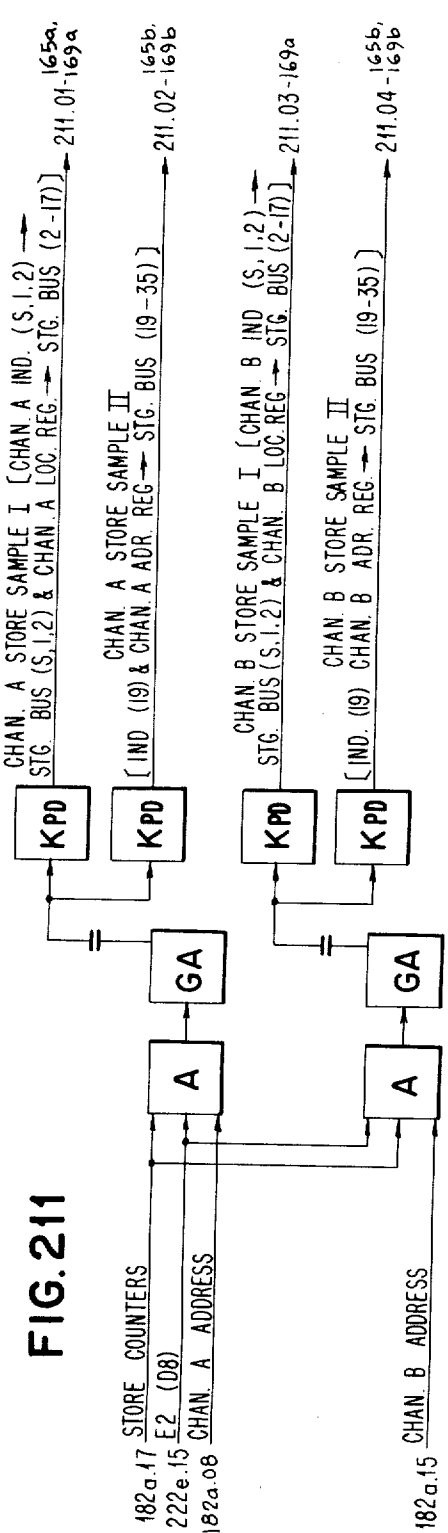


FIG. 211



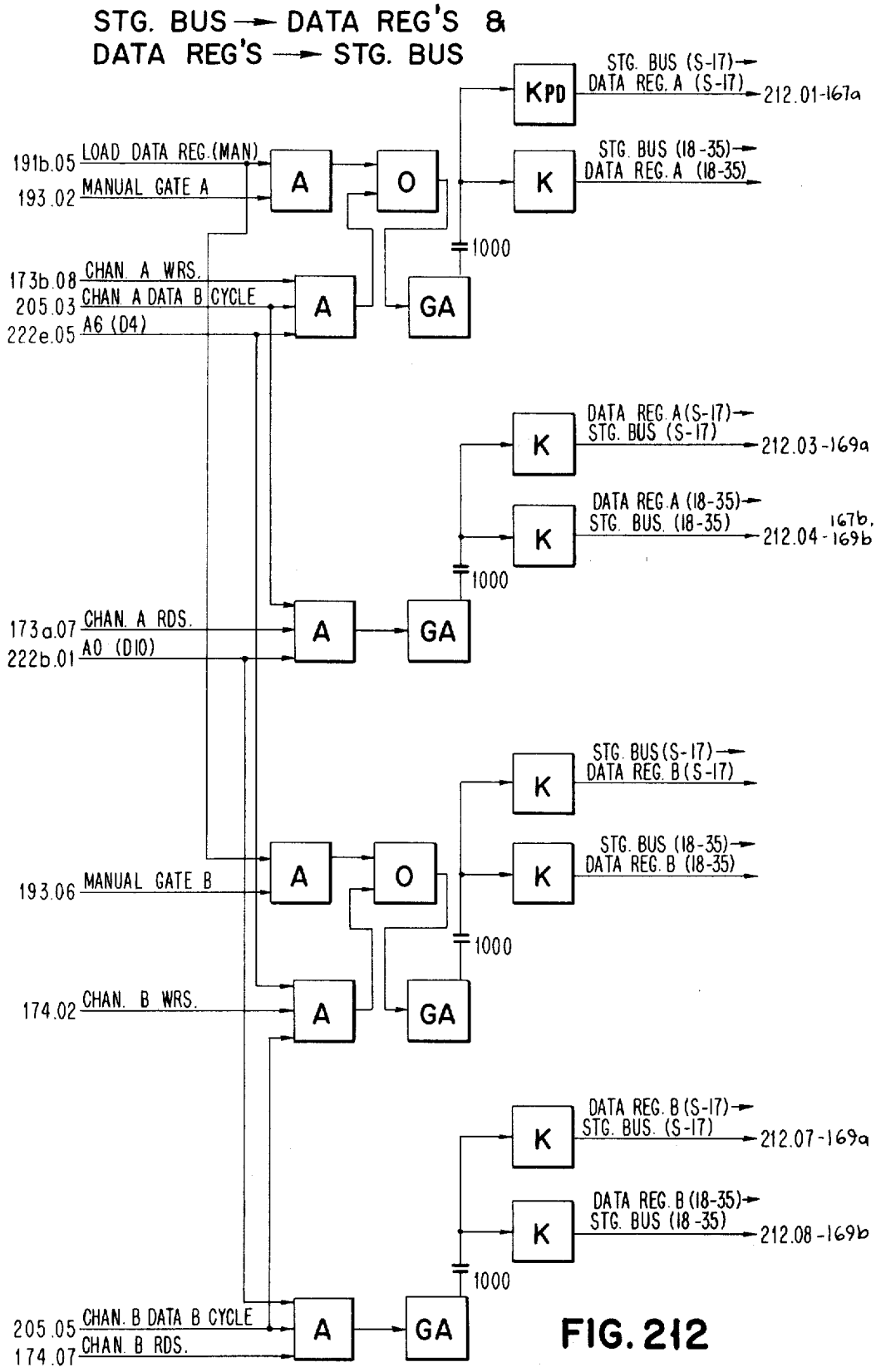
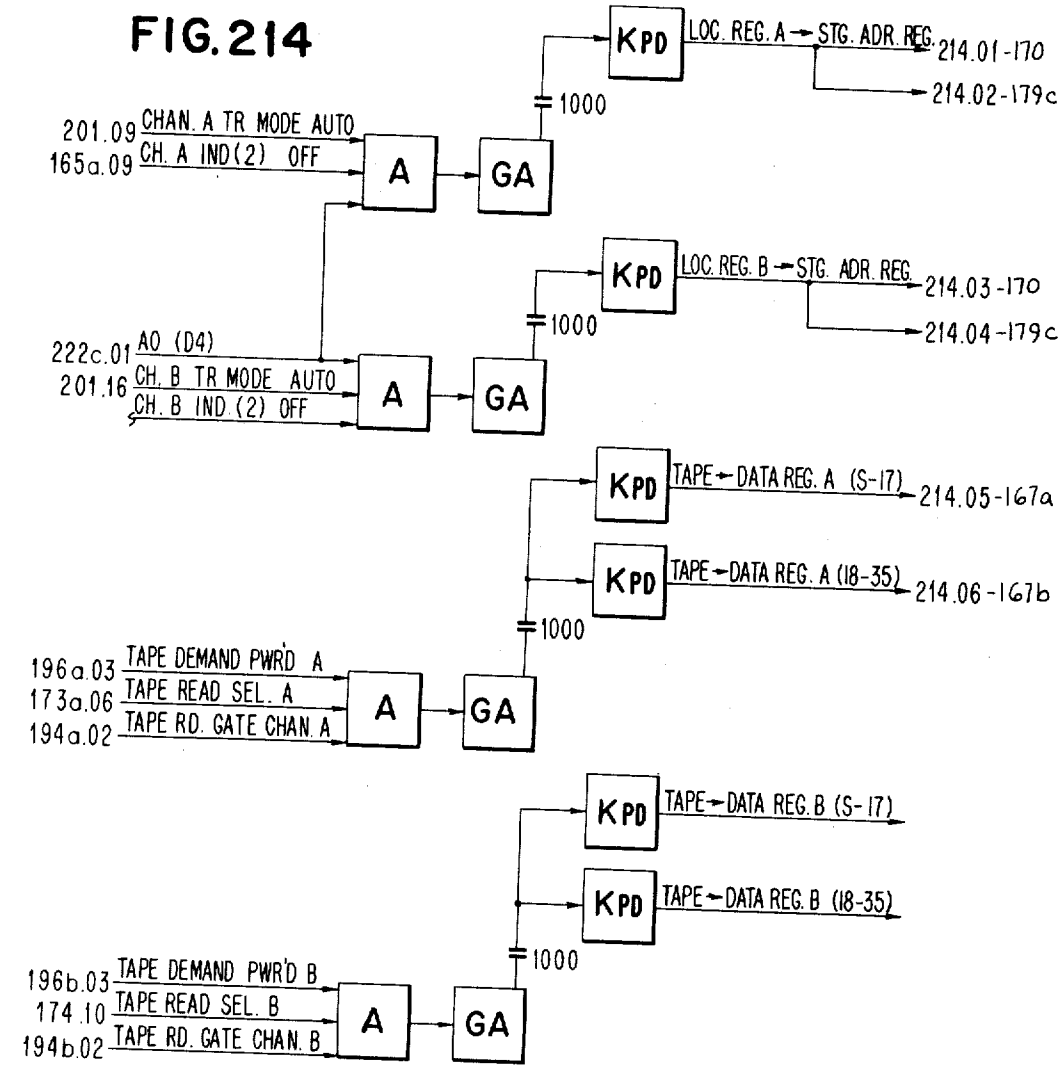

STG. BUS → DATA REG'S &
DATA REG'S → STG. BUS
191b.05 LOAD DATA REG.(MAN)
193.02 MANUAL GATE A
A
O
KPD
STG. BUS (S-17)→
DATA REG. A (S-17)
212.01-167a
K
STG. BUS (18-35)→
DATA REG. A (18-35)
1000
173b.08 CHAN. A WRS.
205.03 CHAN. A DATA B CYCLE
222e.05 A6 (D4)
A
GA
K
DATA REG. A (S-17)→
STG. BUS (S-17)
212.03-169a
K
DATA REG. A (18-35)→
STG. BUS. (18-35)
212.04-167b, 169b
1000
173a.07 CHAN. A RDS.
222b.01 A0 (D10)
A
GA
K
STG. BUS (S-17)→
DATA REG. B (S-17)
193.06 MANUAL GATE B
A
O
K
STG. BUS (18-35)→
DATA REG. B (18-35)
1000
174.02 CHAN. B WRS.
A
GA
K
DATA REG. B (S-17)→
STG. BUS. (S-17)
212.07-169a
K
DATA REG. B (18-35)→
STG. BUS (18-35)
212.08-169b
1000
205.05 CHAN. B DATA B CYCLE
174.07 CHAN. B RDS.
A
GA

FIG. 212

LOC. REG'S → STG ADR. BUS TAPE → DATA REG'S

FIG. 214



ADDRESS REG. → STG. ADDRESS REG.

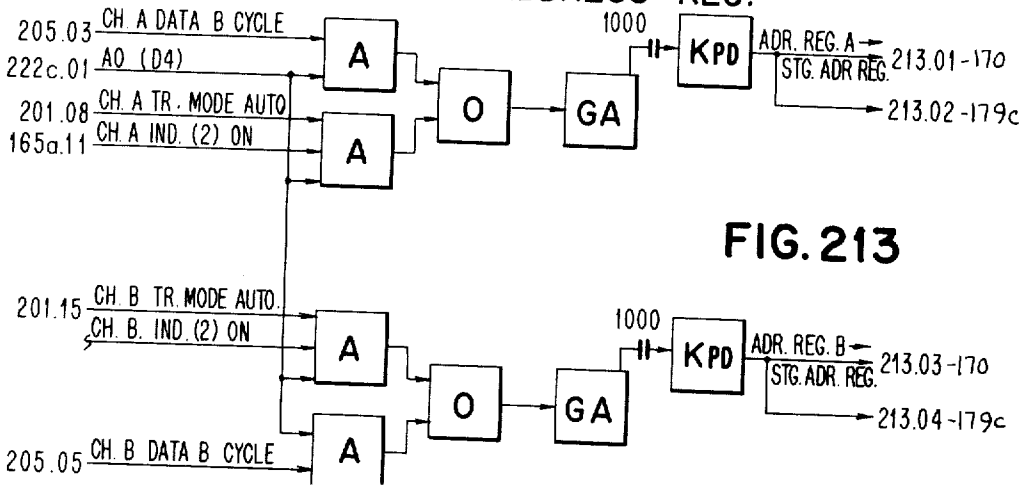
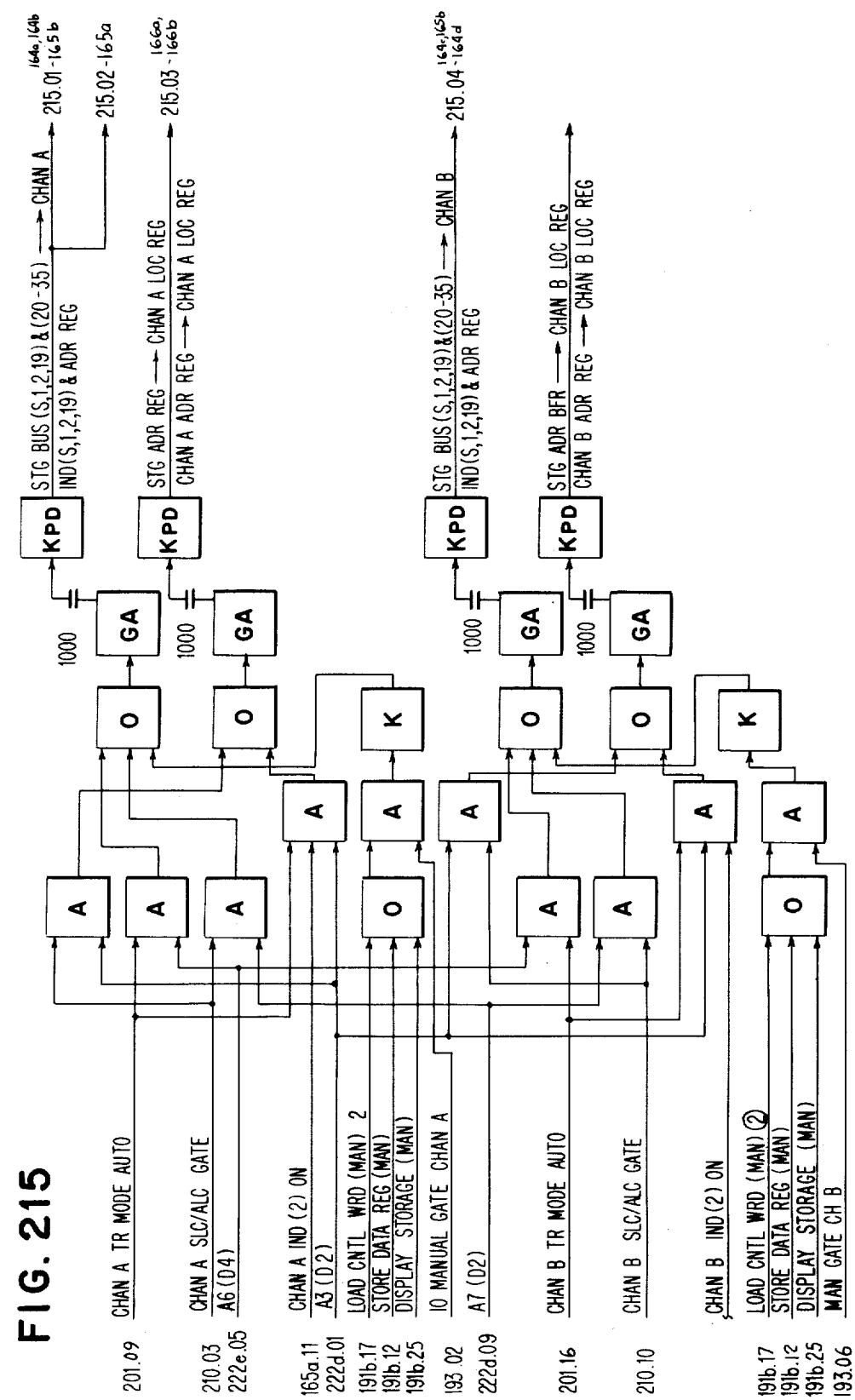


FIG. 213

FIG. 215

STORAGE BUS - CONTROL REGISTERS



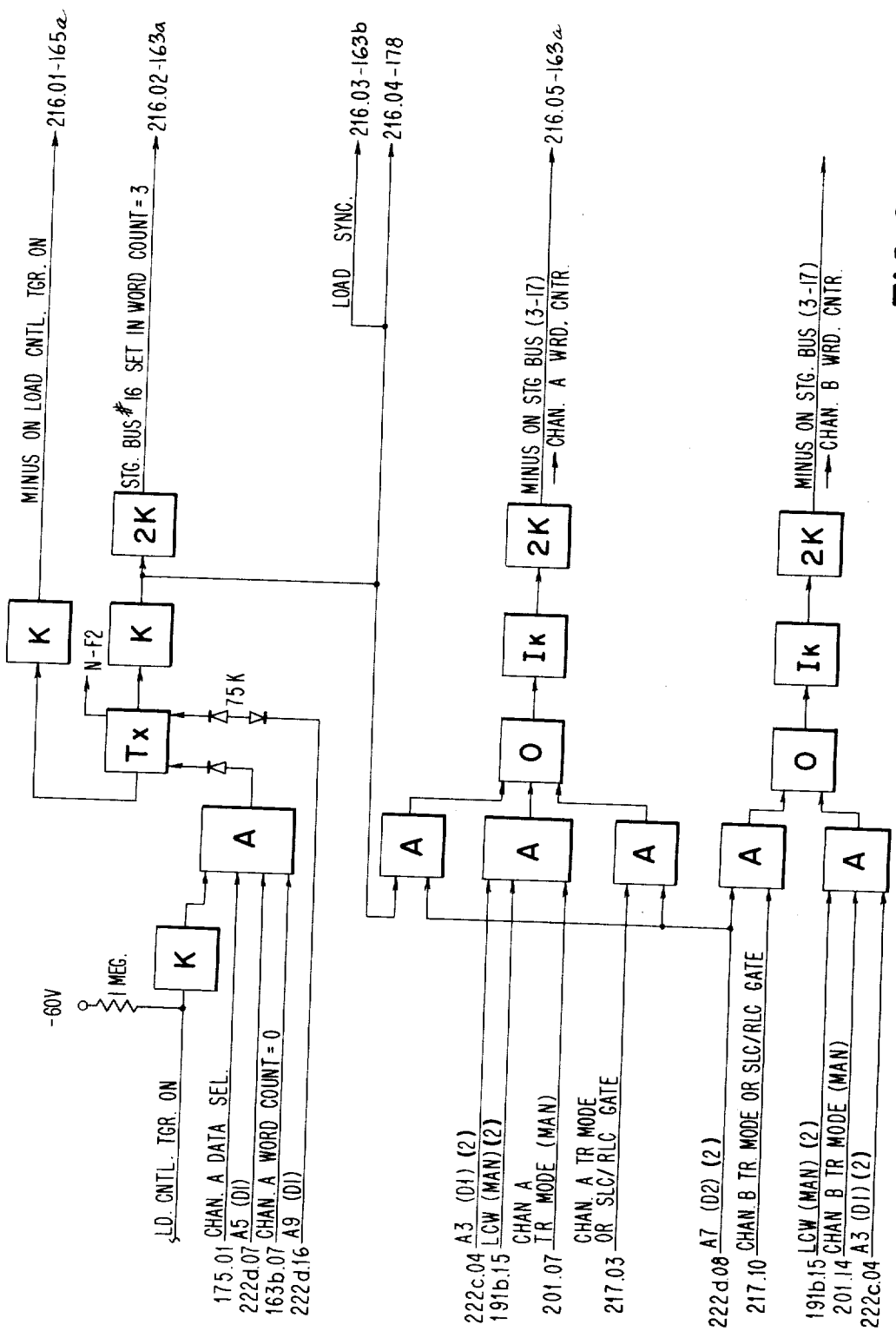

STG. BUS (3-17) → WORD CTRS. & LOAD CNTL. TGR.
MINUS ON LOAD CNTL. TGR. ON
216.01-165a
STG. BUS #16 SET IN WORD COUNT = 3
216.02-163a
LOAD SYNC.
216.03-163b
216.04-178
MINUS ON STG BUS (3-17)
→ CHAN. A WRD. CNTR.
216.05-163a
MINUS ON STG. BUS (3-17)
→ CHAN. B WRD. CNTR.
K
K
2K
2K
2K
Tx
N-F2
75 K
-60V
1 MEG.
A
A
A
A
A
O
O
Ik
Ik
LD. CNTL. TGR. ON
175.01 CHAN. A DATA SEL.
222d.07 A5 (D1)
163b.07 CHAN. A WORD COUNT = 0
222d.16 A9 (D1)
222c.04 A3 (D1) (2)
191b.15 LCW (MAN) (2)
CHAN A
201.07 TR MODE (MAN)
CHAN. A TR MODE
217.03 OR SLC/RLC GATE
222d.08 A7 (D2) (2)
217.10 CHAN B TR MODE OR SLC/RLC GATE
191b.15 LCW (MAN) (2)
201.14 CHAN B TR MODE (MAN)
222c.04 A3 (D1) (2)

FIG. 216

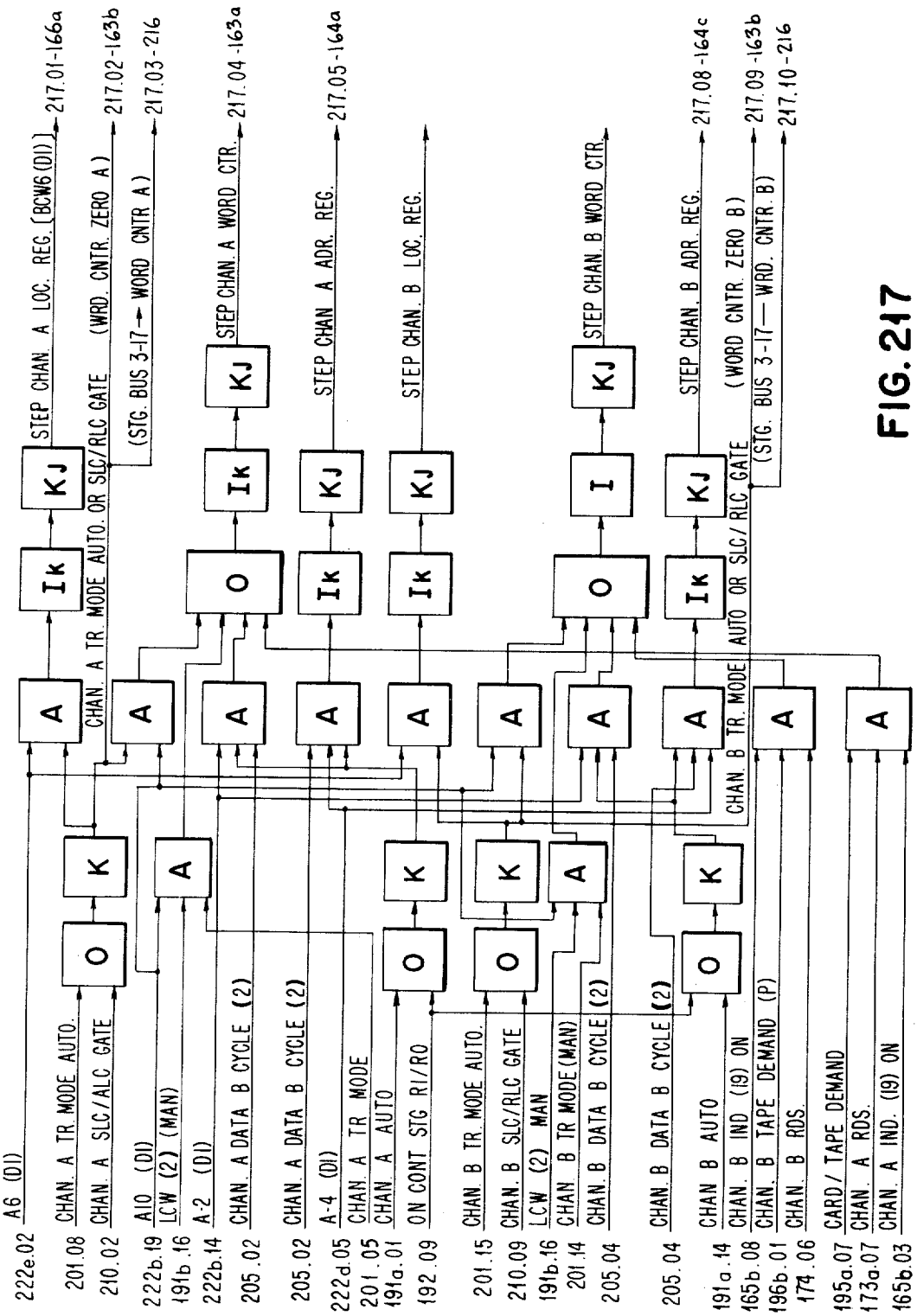

STEP CONTROL REGISTERS
222e.02 A6 (D1)
201.08 CHAN. A TR. MODE AUTO.
210.02 CHAN. A SLC/ALC GATE
222b.19 A10 (D1)
191b.16 LCW (2) (MAN)
222b.14 A-2 (D1)
205.02 CHAN. A DATA B CYCLE (2)
205.02 CHAN. A DATA B CYCLE (2)
222d.05 A-4 (D1)
201.05 CHAN. A TR. MODE
191a.01 CHAN. A AUTO
192.09 ON CONT STG RI/RO
201.15 CHAN. B TR. MODE AUTO.
210.09 CHAN. B SLC/RLC GATE
191b.16 LCW (2) MAN
201.14 CHAN. B TR MODE (MAN)
205.04 CHAN. B DATA B CYCLE (2)
205.04 CHAN. B DATA B CYCLE (2)
191a.14 CHAN B AUTO
165b.08 CHAN. B IND (19) ON
196b.01 CHAN. B TAPE DEMAND (P)
174.06 CHAN. B RDS.
195a.07 CARD / TAPE DEMAND
173a.07 CHAN. A RDS.
165b.03 CHAN. A IND. (19) ON
CHAN. A TR. MODE AUTO. OR SLC/RLC GATE
CHAN. B TR. MODE AUTO OR SLC/RLC GATE
STEP CHAN. A LOC. REG. (BCW6 (D1))
217.01-166a
(WRD. CNTR. ZERO A)
(STG. BUS 3-17→ WORD CNTR A)
217.02-163b
217.03-216
STEP CHAN. A WORD CTR.
217.04-163a
STEP CHAN. A ADR. REG.
217.05-164a
STEP CHAN. B LOC. REG.
STEP CHAN. B WORD CTR.
STEP CHAN. B ADR. REG.
217.08-164c
(WORD CNTR. ZERO B)
(STG. BUS 3-17— WRD. CNTR. B)
217.09-163b
217.10-216
A
O
K
Ik
KJ
I

FIG. 217

FIG. 218

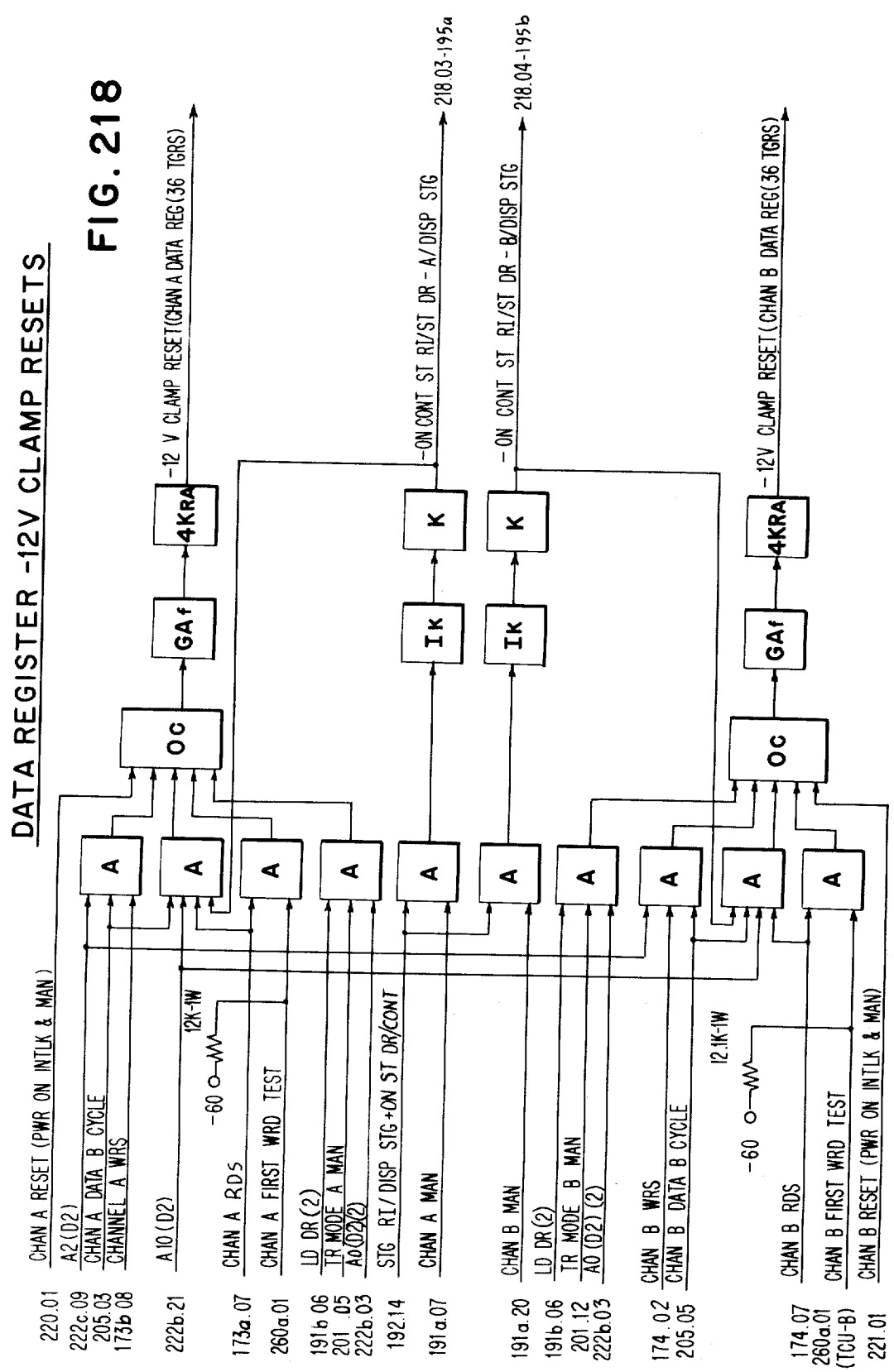
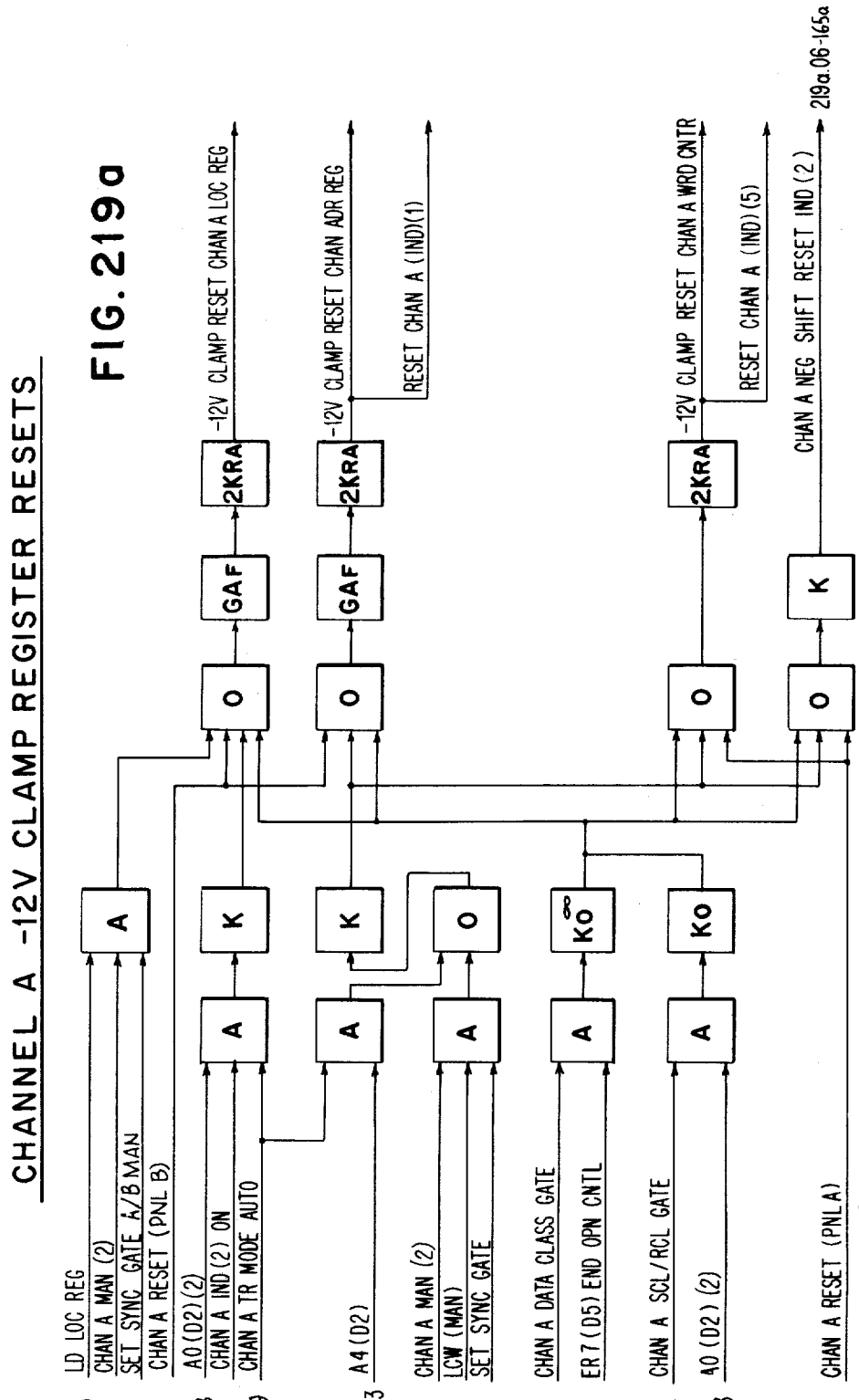

DATA REGISTER -12V CLAMP RESETS
CHAN A RESET (PWR ON INTLK & MAN)
A2(D2)
CHAN A DATA B CYCLE
CHANNEL A WRS
A10(D2)
12K-1W
-60
CHAN A RDS
CHAN A FIRST WRD TEST
LD DR(2)
TR MODE A MAN
A0(D2)(2)
STG RI/DISP STG+ON ST DR/CONT
CHAN A MAN
CHAN B MAN
LD DR(2)
TR MODE B MAN
A0(D2)(2)
CHAN B WRS
CHAN B DATA B CYCLE
12.1K-1W
-60
CHAN B RDS
CHAN B FIRST WRD TEST
CHAN B RESET (PWR ON INTLK & MAN)
A
Oc
GAf
4KRA
Ik
K
-12 V CLAMP RESET(CHAN A DATA REG(36 TGRS)
-ON CONT ST RI/ST DR - A/DISP STG
-ON CONT ST RI/ST DR - B/DISP STG
-12V CLAMP RESET(CHAN B DATA REG(36 TGRS)
220.01
222c.09
205.03
173b.08
222b.21
173a.07
260a.01
191b.06
201.05
222b.03
192.14
191a.07
191a.20
191b.06
201.12
222b.03
174.02
205.05
174.07
260a.01
(TCU-B)
221.01
218.03-195a
218.04-195b

FIG. 219a


CHANNEL A -12V CLAMP REGISTER RESETS
LD LOC REG
CHAN A MAN (2)
SET SYNC GATE A/B MAN
CHAN A RESET (PNL B)
A0 (D2) (2)
CHAN A IND (2) ON
CHAN A TR MODE AUTO
A4 (D2)
CHAN A MAN (2)
LOW (MAN)
SET SYNC GATE
CHAN A DATA CLASS GATE
ER 7 (D5) END OPN CNTL
CHAN A SCL/RCL GATE
A0 (D2) (2)
CHAN A RESET (PNL A)
-12V CLAMP RESET CHAN A LOC REG
-12V CLAMP RESET CHAN ADR REG
RESET CHAN A (IND) (1)
-12V CLAMP RESET CHAN A WRD CNTR
RESET CHAN A (IND) (5)
CHAN A NEG SHIFT RESET IND (2)
A
K
A
O
GAF
2KRA
Ko
191b.30
191a.12
193.08
220.01
222b.03
165a.11
201.09
222d.03
191a.12
191b.18
193.08
171.02
172.04
210.04
222b.03
220.05
219a.06-165a

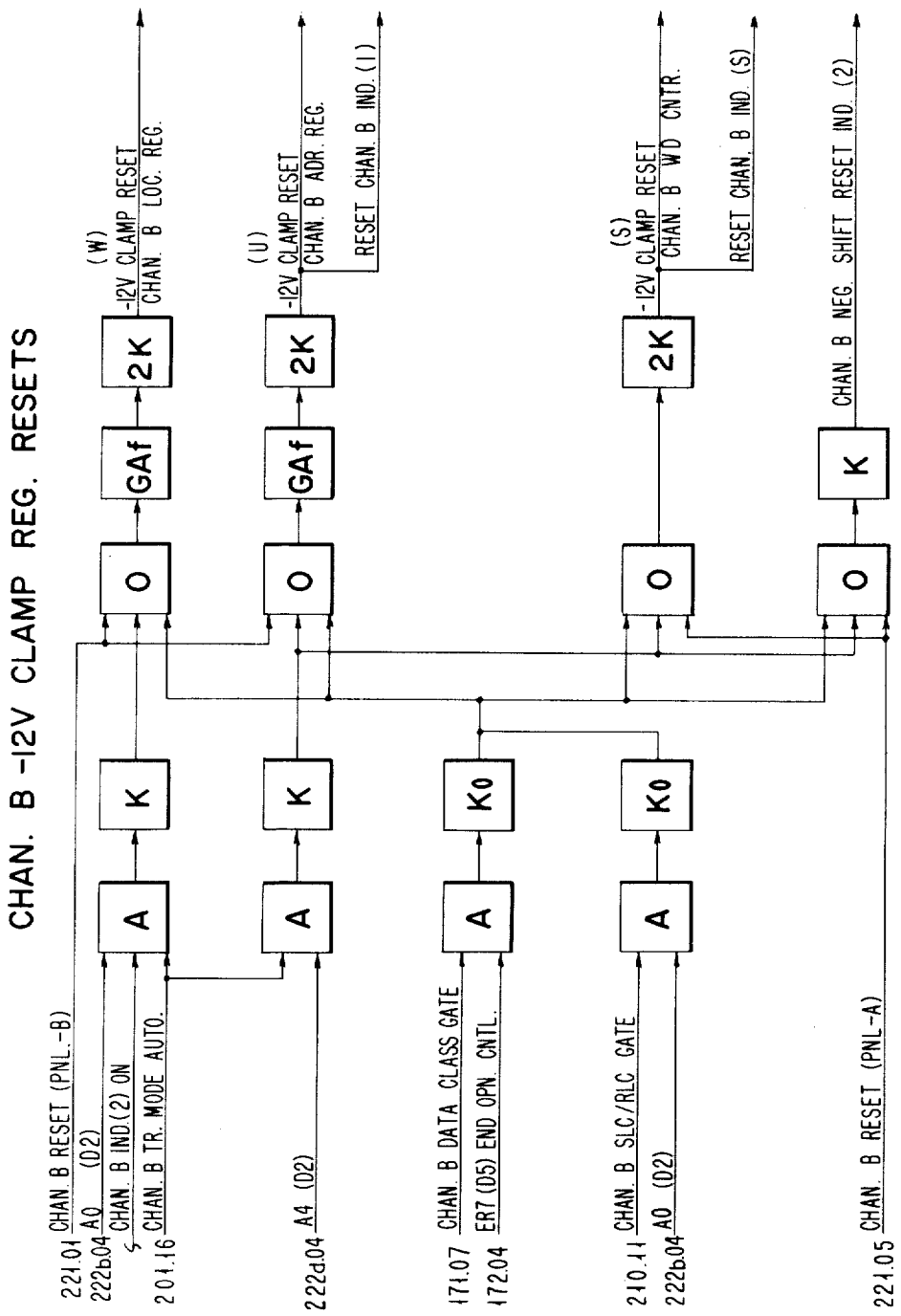

CHAN. B -12V CLAMP REG. RESETS
221.01 CHAN B RESET (PNL.-B)
222b.04 A0 (02)
CHAN. B IND.(2) ON
201.16 CHAN. B TR. MODE AUTO.
222d.04 A4 (02)
171.07 CHAN. B DATA CLASS GATE
172.04 ER7 (D5) END OPN. CNTL.
210.11 CHAN. B SLC/RLC GATE
222b.04 A0 (02)
221.05 CHAN. B RESET (PNL-A)
A
K
Ko
O
GAf
2K
K
(W)
-12V CLAMP RESET
CHAN. B LOC. REG.
(U)
-12V CLAMP RESET
CHAN. B ADR. REG.
RESET CHAN. B IND. (1)
(S)
-12V CLAMP RESET
CHAN. B WD CNTR.
RESET CHAN. B IND. (S)
CHAN. B NEG. SHIFT RESET IND. (2)

FIG. 219b

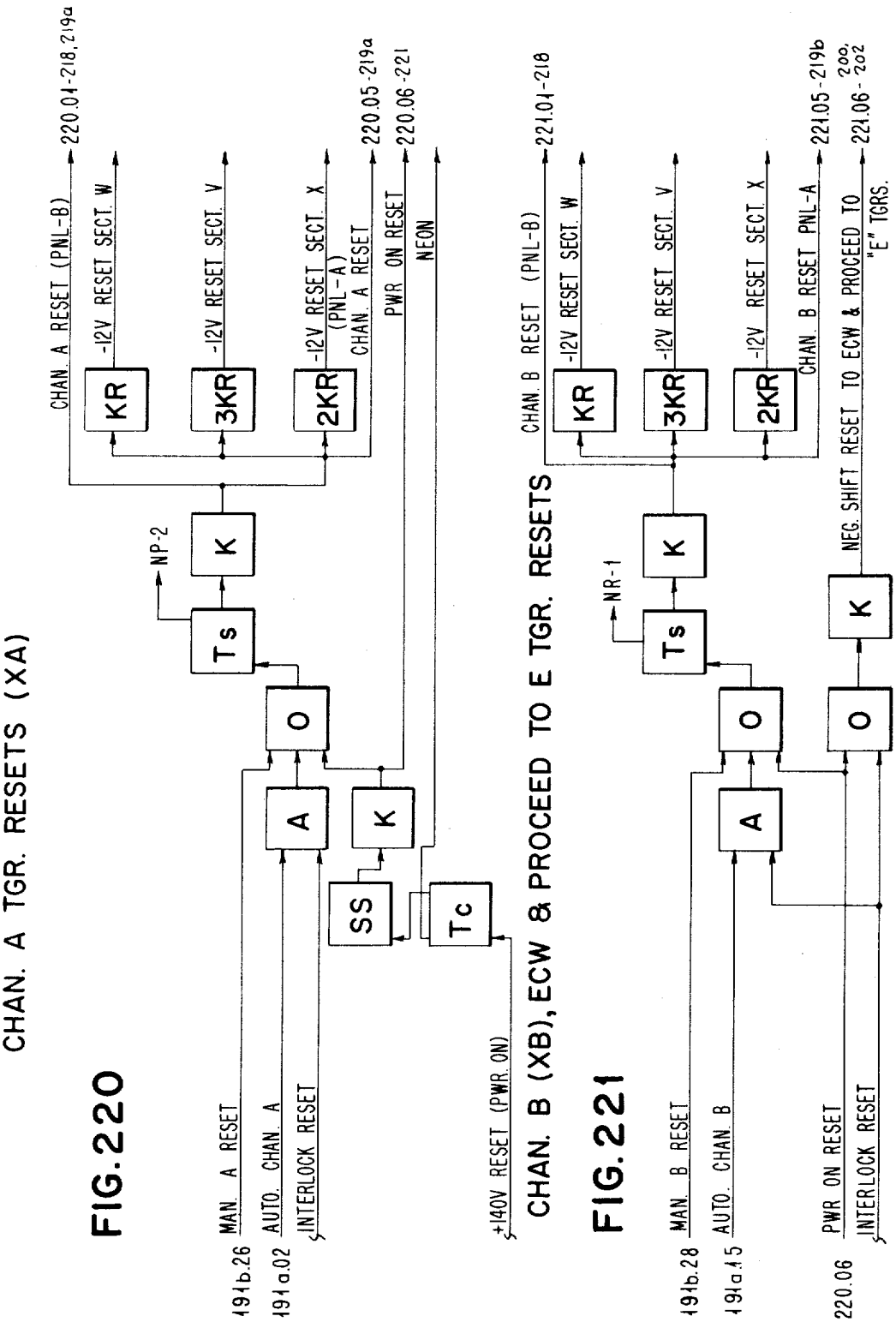

CHAN. A TGR. RESETS (XA)
FIG. 220
CHAN. A RESET (PNL-B)
220.04-218, 219a
-12V RESET SECT. W
-12V RESET SECT. V
-12V RESET SECT. X
(PNL-A)
CHAN. A RESET
220.05-219a
PWR ON RESET
220.06-221
NEON
KR
3KR
2KR
NP-2
K
Ts
O
A
K
SS
Tc
191b.26 MAN. A RESET
191a.02 AUTO. CHAN. A
INTERLOCK RESET
+140V RESET (PWR. ON)
CHAN. B (XB), ECW & PROCEED TO E TGR. RESETS
FIG. 221
CHAN. B RESET (PNL-B)
221.04-218
-12V RESET SECT. W
-12V RESET SECT. V
-12V RESET SECT. X
CHAN. B RESET PNL-A
221.05-219b
NEG. SHIFT RESET TO ECW & PROCEED TO "E" TGRS.
200, 202
221.06-
NR-1
191b.28 MAN. B RESET
191a.15 AUTO. CHAN. B
220.06 PWR ON RESET
INTERLOCK RESET

FIG. 222 a

CARD CONTROL PULSE GENERATOR

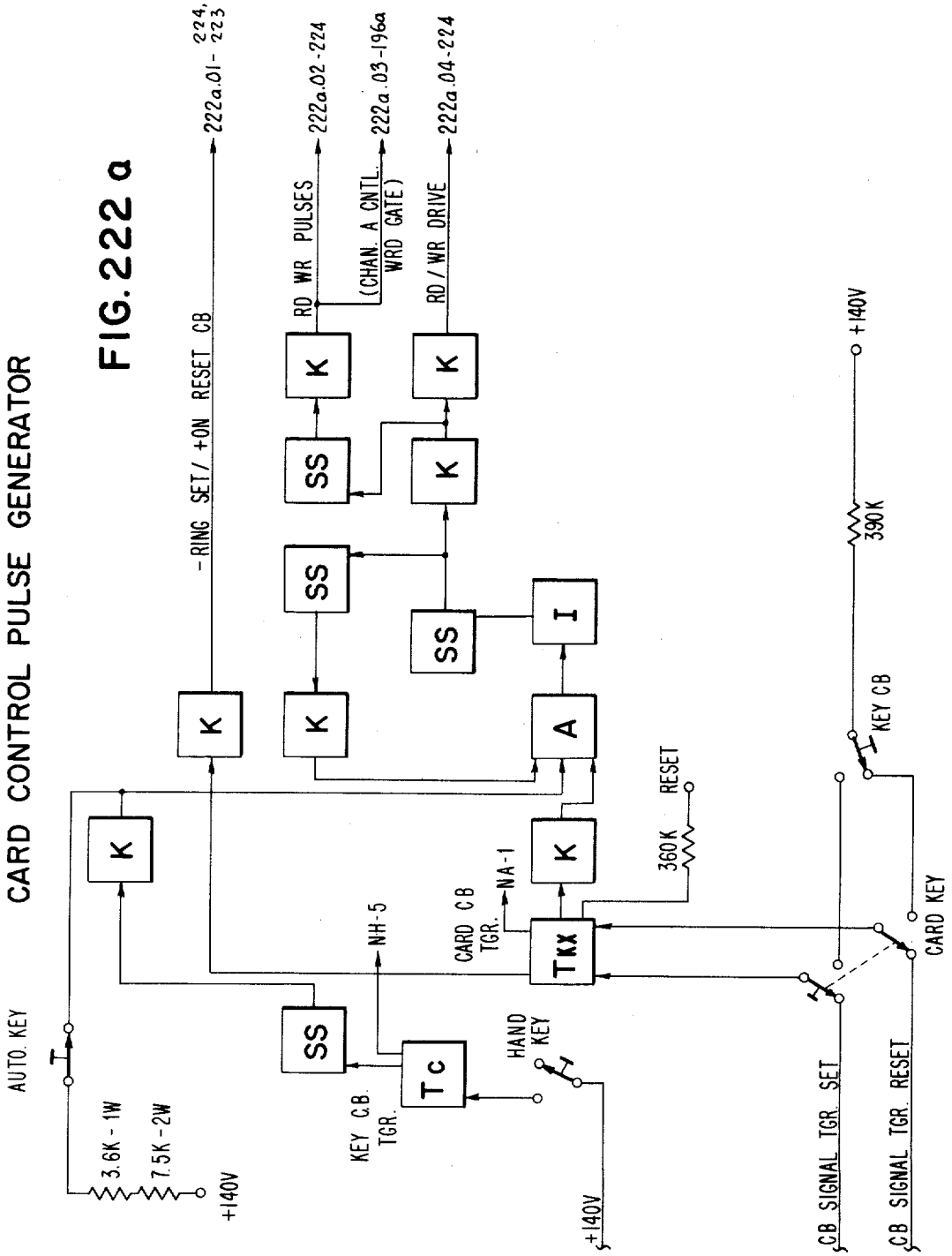
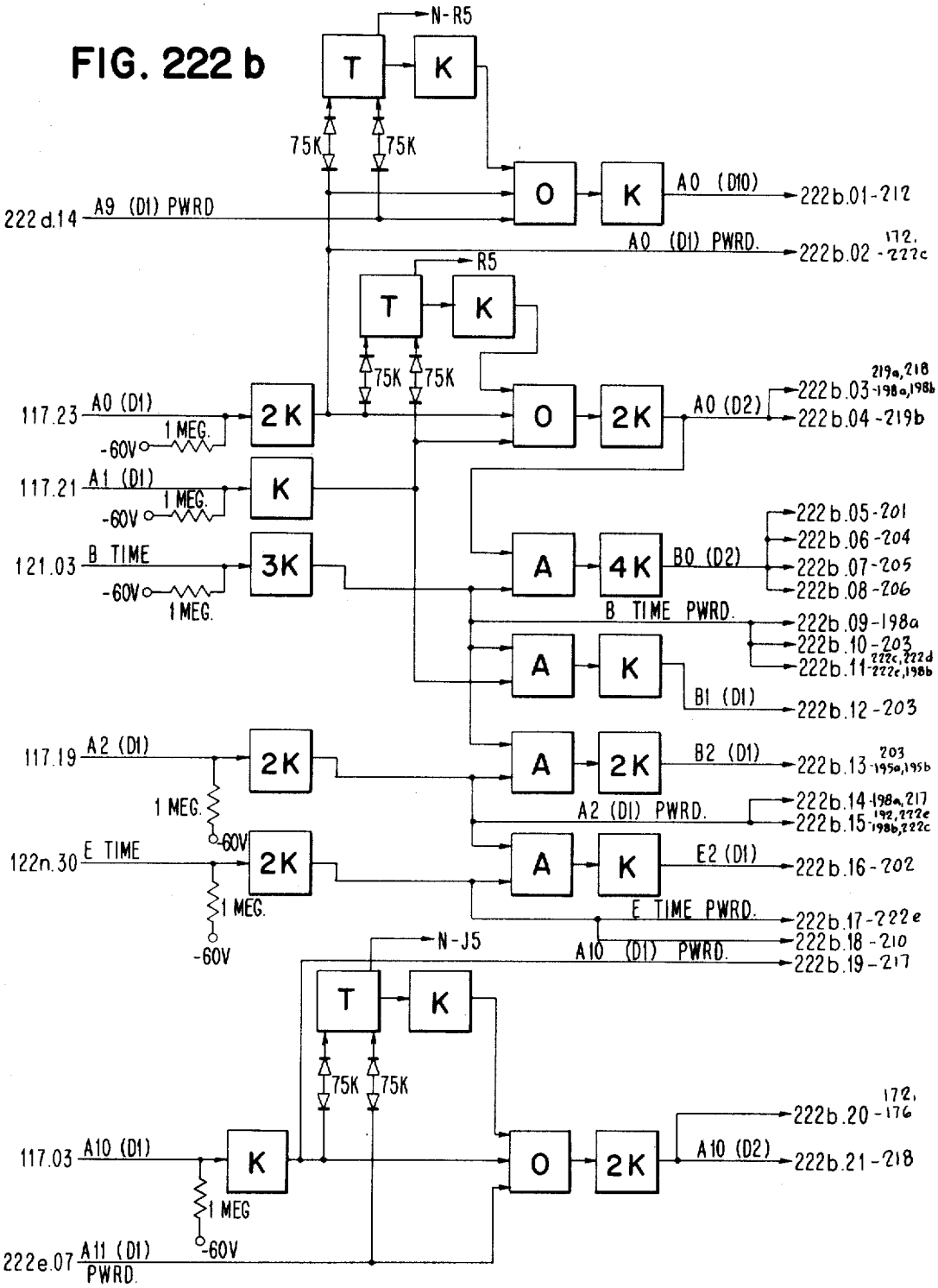


FIG. 222 b



PULSE GENERATORS

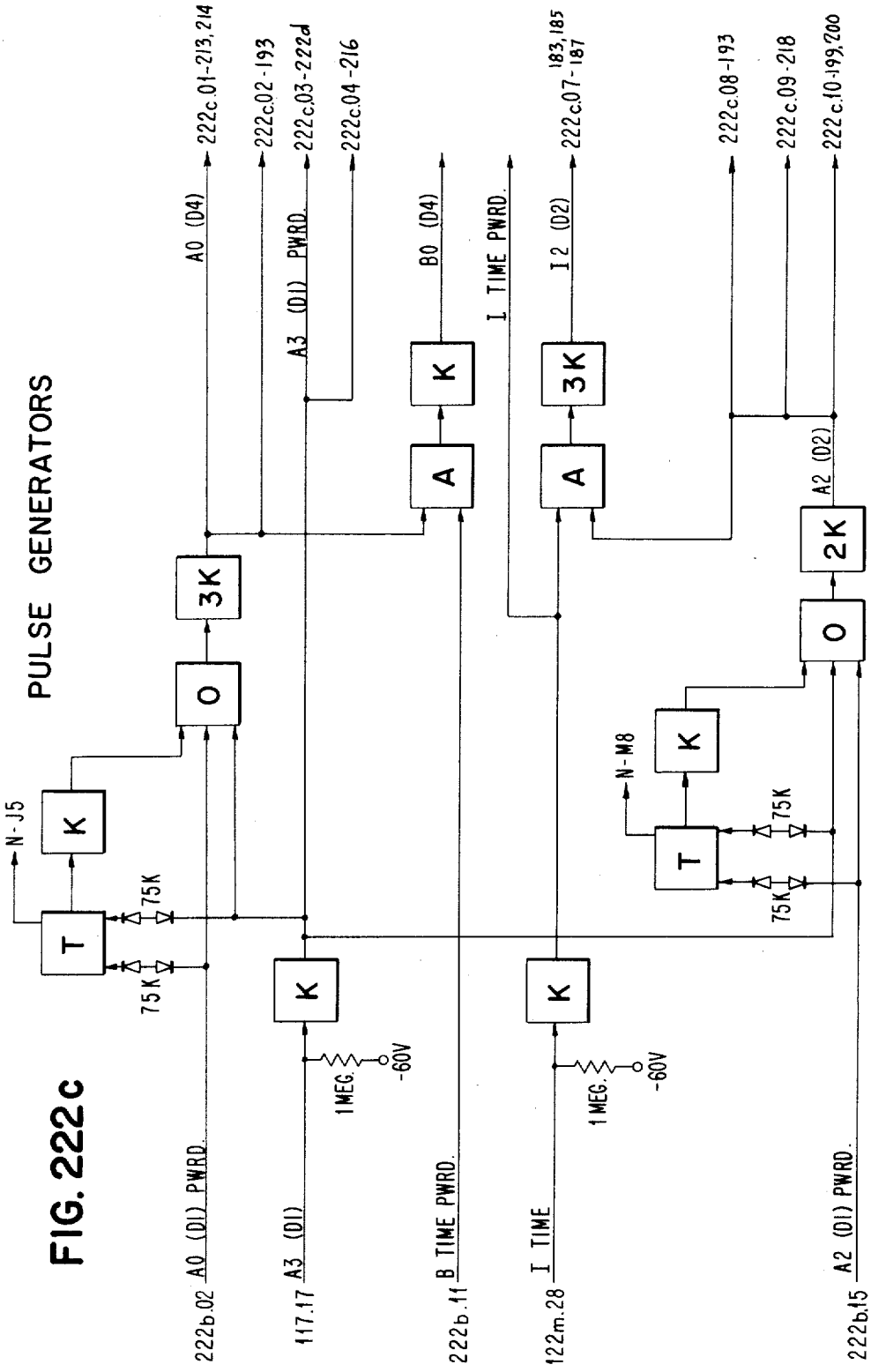

PULSE GENERATORS
N-J5
T
K
75K
75K
O
3K
A0 (D4)
222c.01-213,214
222c.02-193
222c.03-222d
222c.04-216
A3 (D1) PWRD.
A0 (D1) PWRD.
222b.02
A3 (D1)
117.17
K
1MEG.
-60V
B0 (D4)
K
A
B TIME PWRD.
222b.11
I TIME PWRD.
I2 (D2)
222c.07-183,185
3K
A
K
1MEG.
-60V
I TIME
122m.28
N-M8
T
K
75K
75K
222c.08-193
222c.09-218
222c.10-199,200
O
2K
A2 (D2)
A2 (D1) PWRD.
222b.15

FIG. 222c

PULSE GENERATORS

FIG. 222d

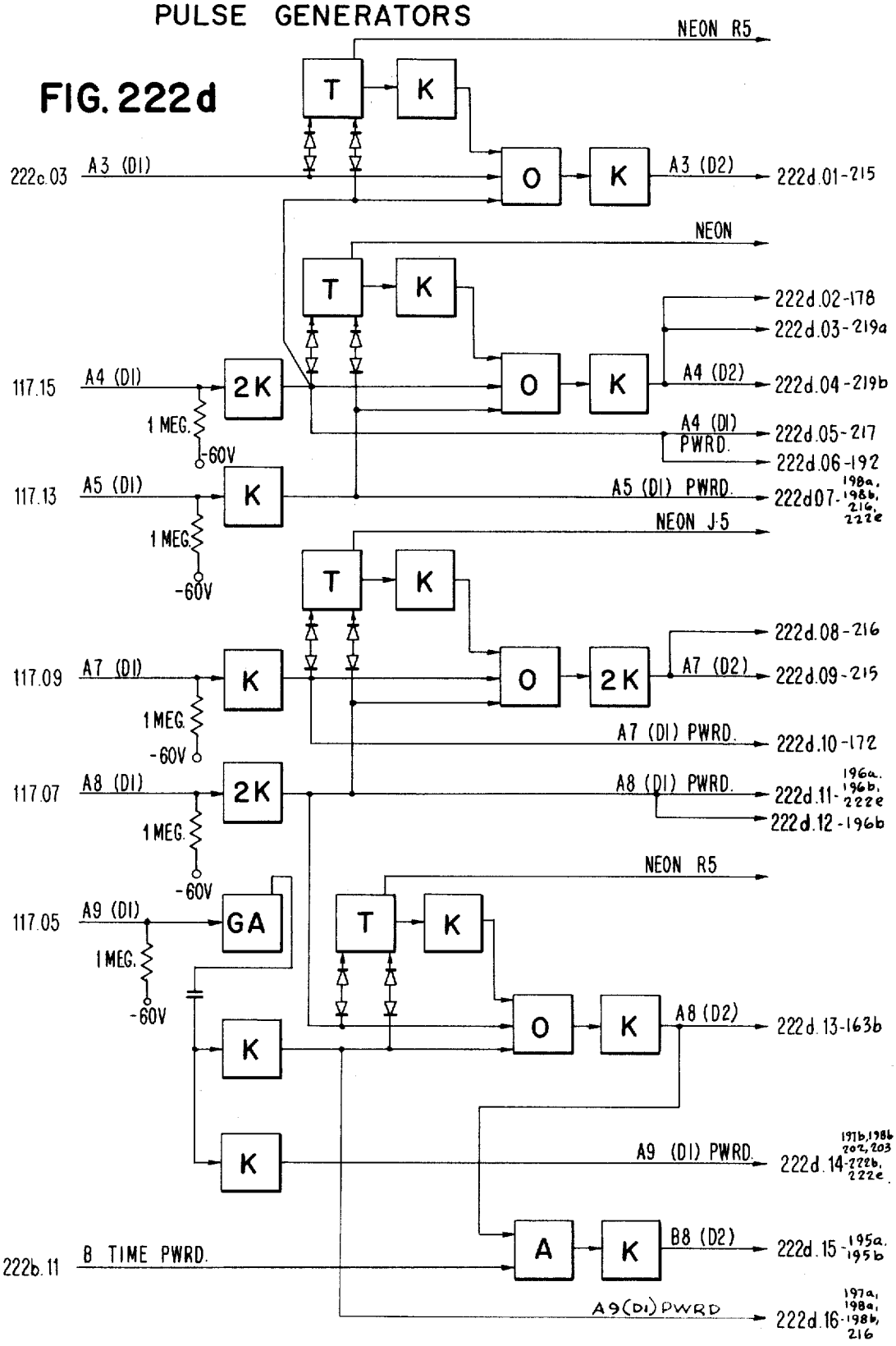
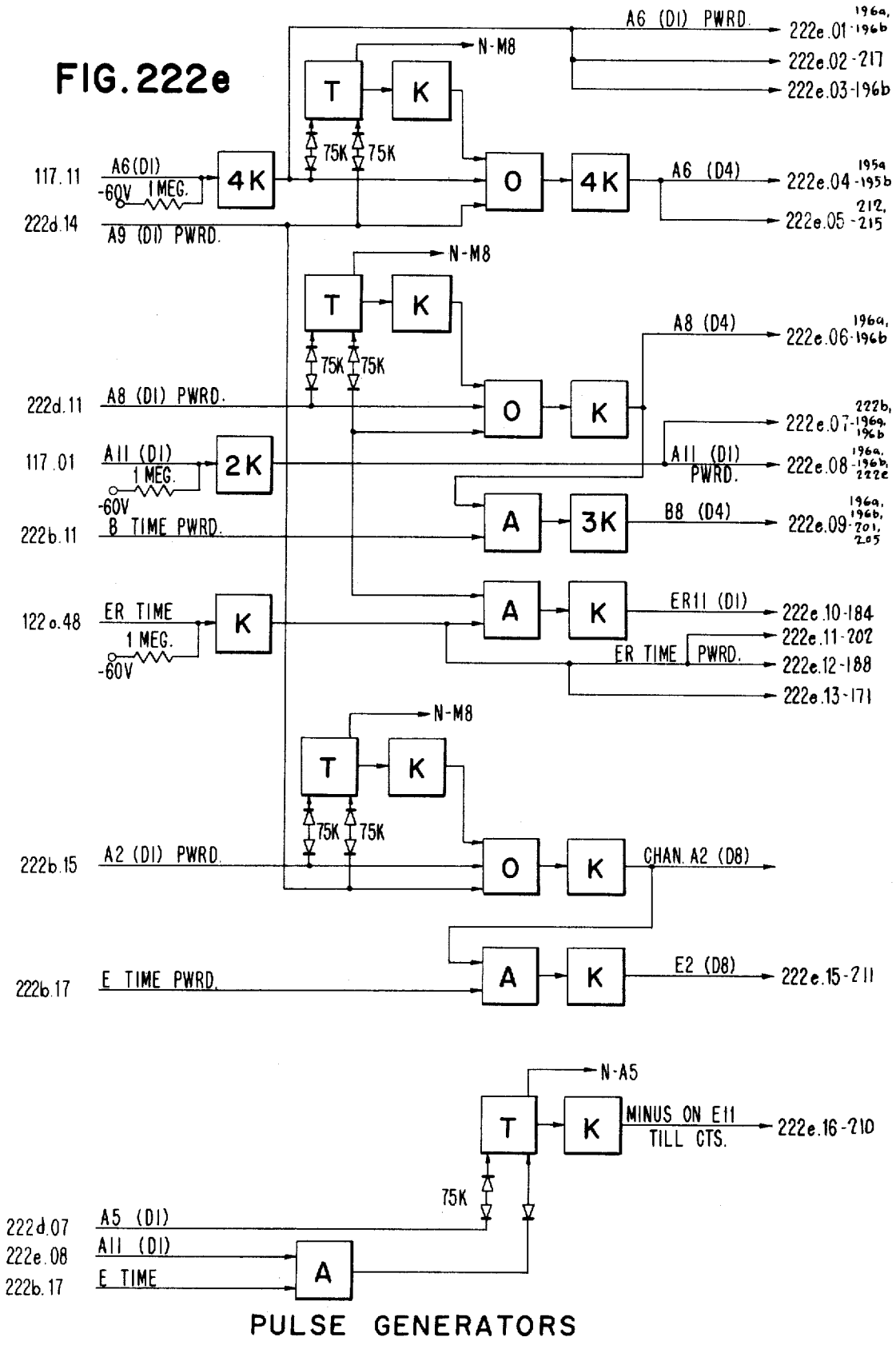


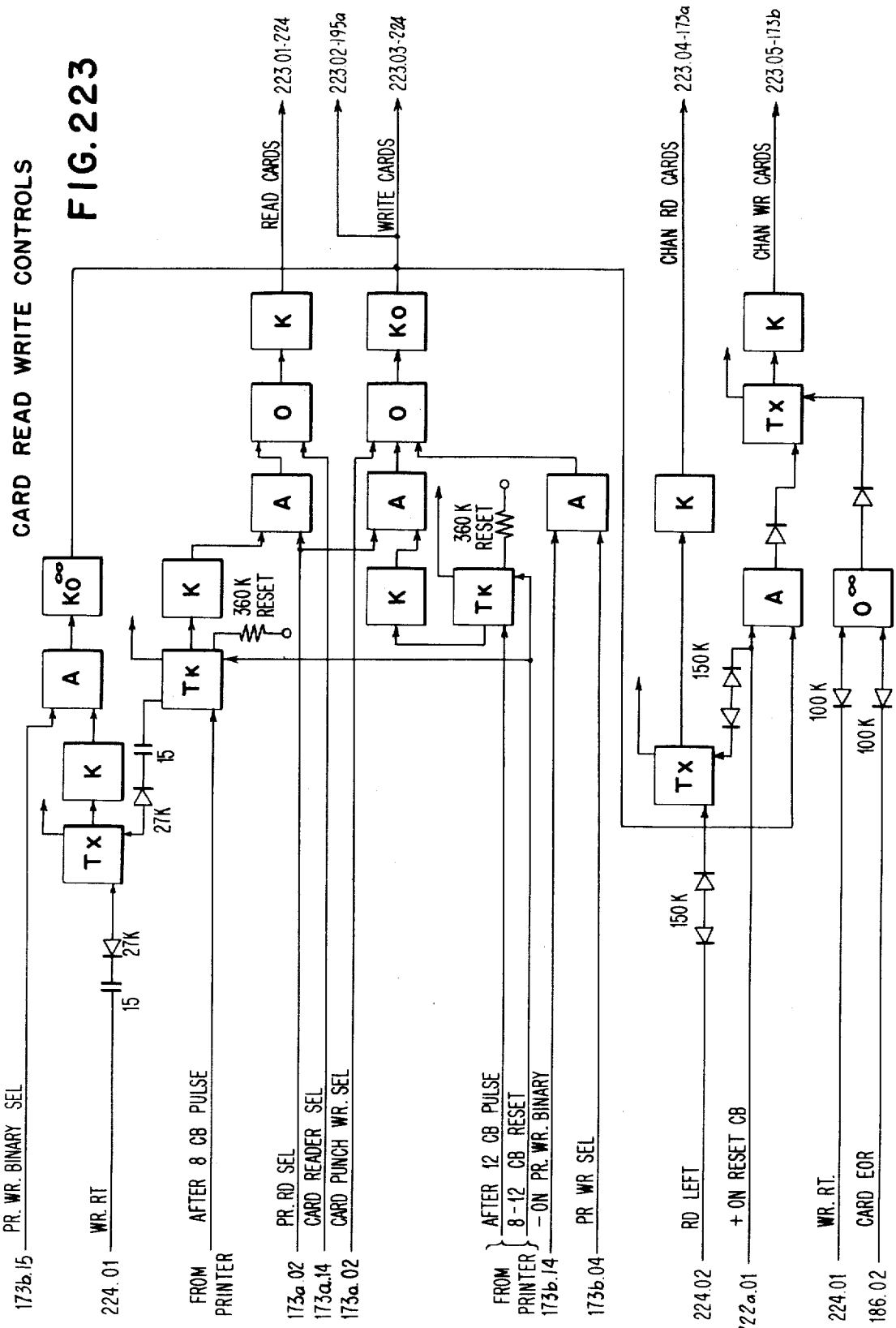
FIG. 222e



PULSE GENERATORS

FIG. 223

CARD READ WRITE CONTROLS



CARD CONTROL RING

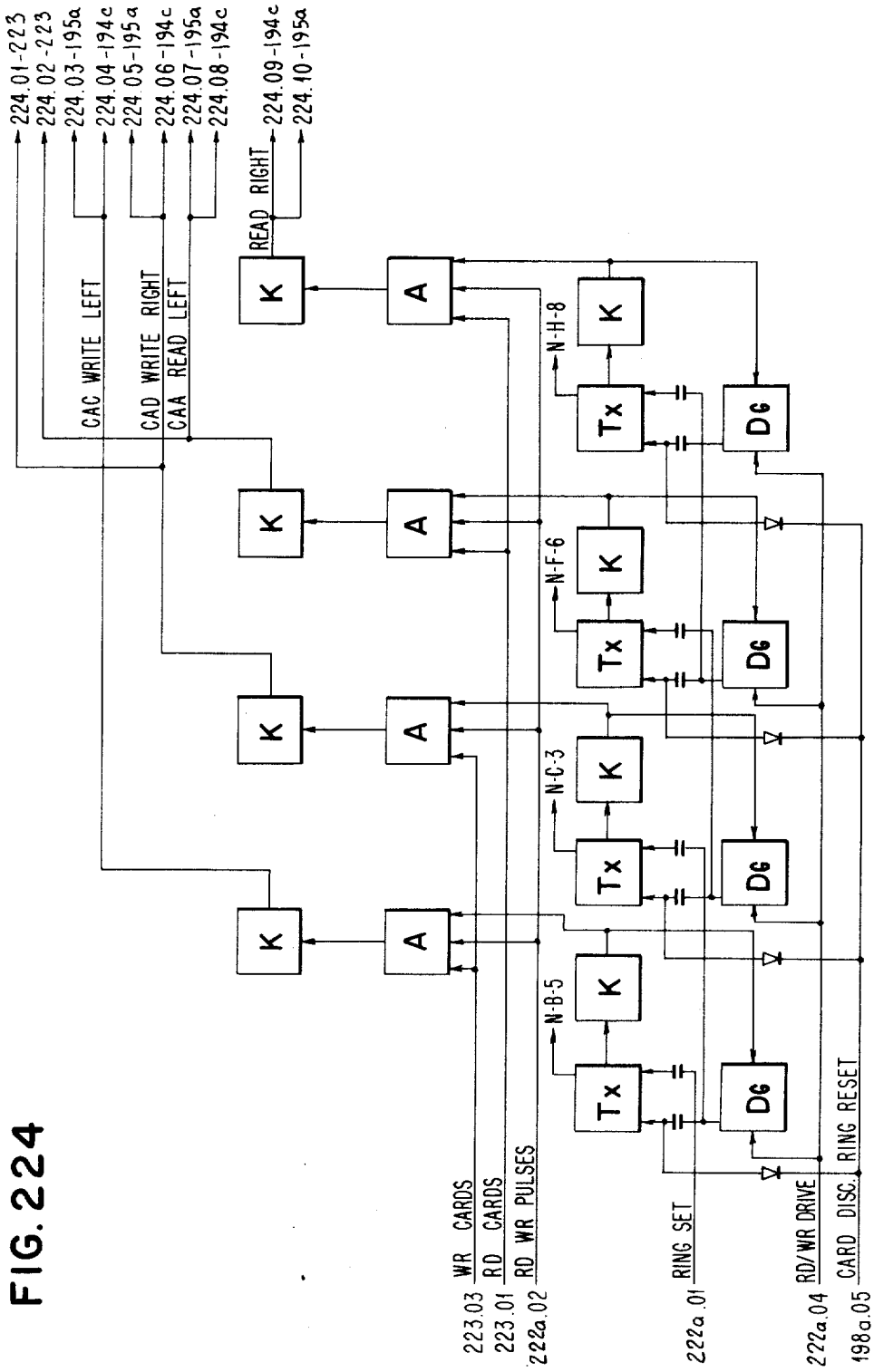


FIG. 224

TAPE SHIFTING REGISTER S THRU 29

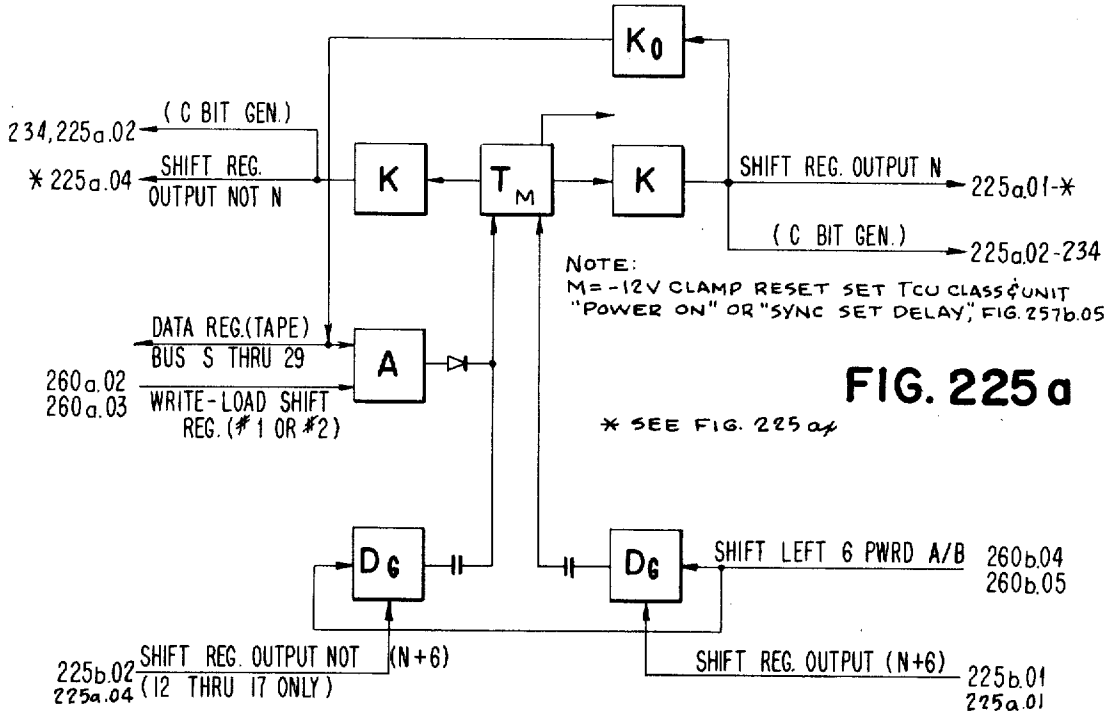


FIG. 225a

TAPE SHIFTING REGISTER 30 THRU 35

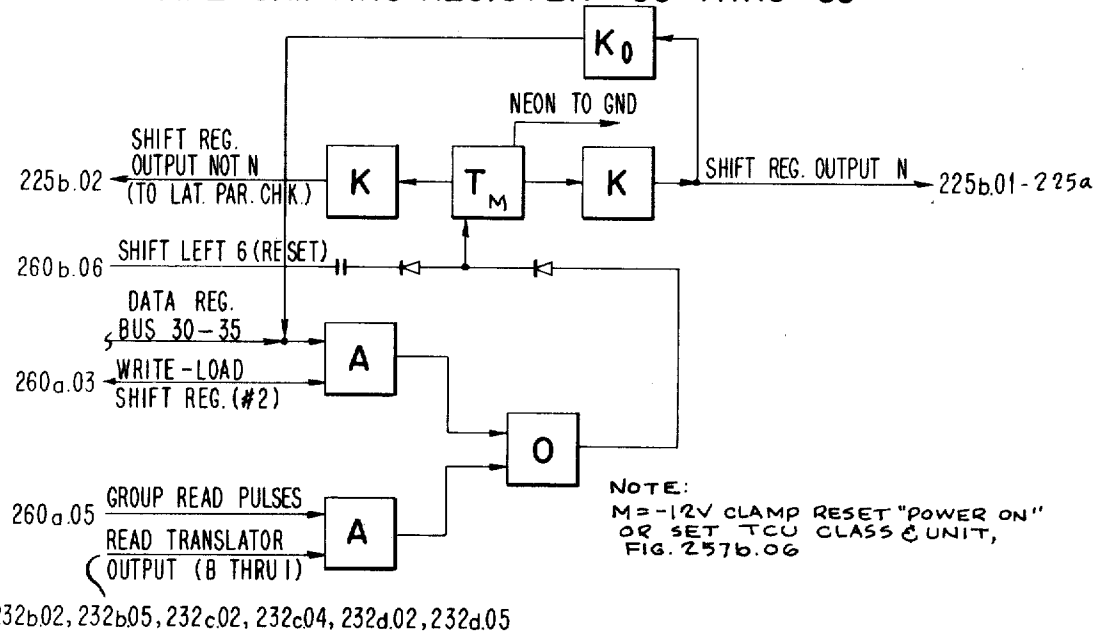


FIG. 225b

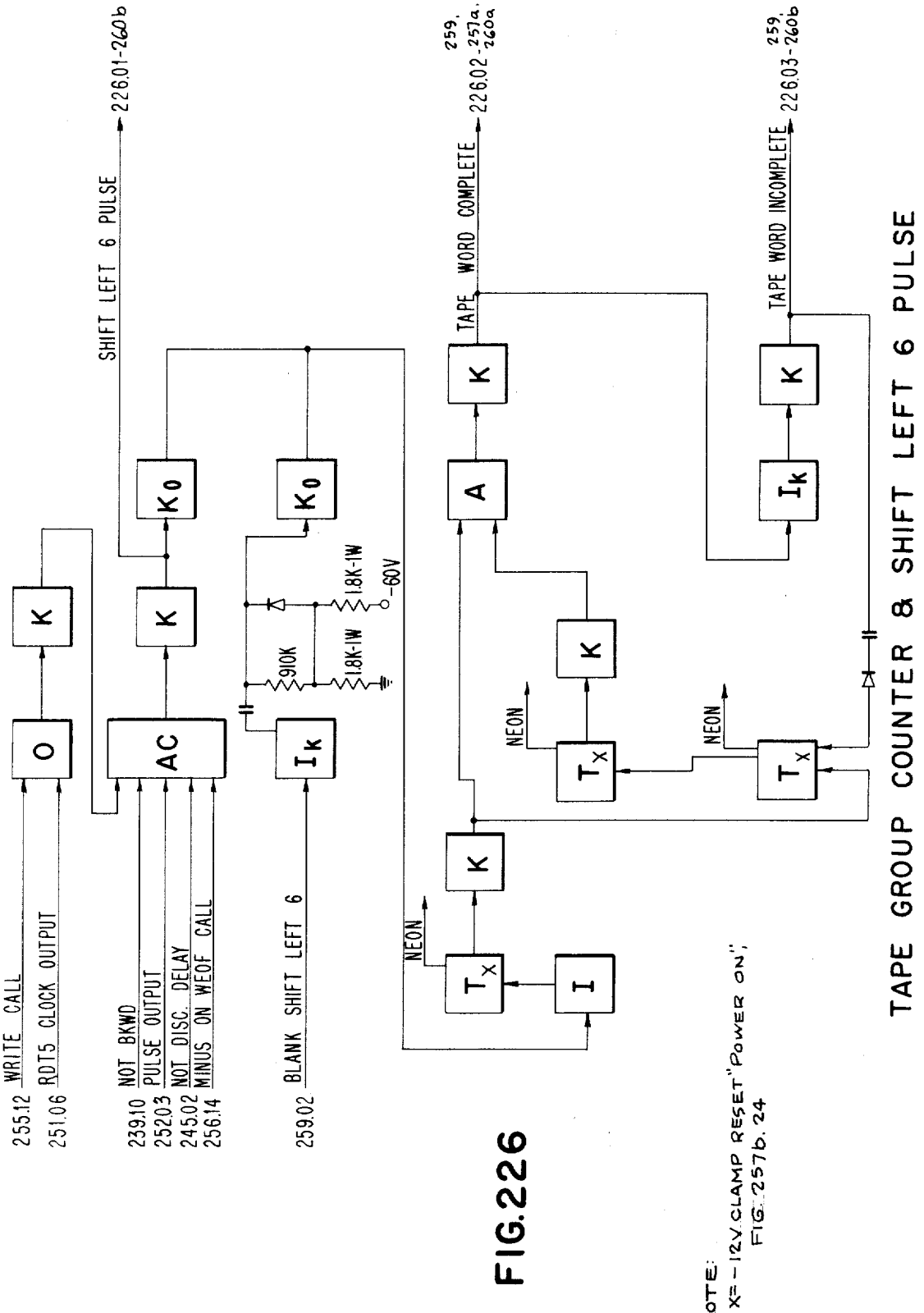

TAPE GROUP COUNTER & SHIFT LEFT 6 PULSE
SHIFT LEFT 6 PULSE
226.01-260b
TAPE WORD COMPLETE
259, 226.02-257a, 260a
TAPE WORD INCOMPLETE
259, 226.03-260b
255.12 WRITE CALL
251.06 RDTS CLOCK OUTPUT
239.10 NOT BKWD
252.03 PULSE OUTPUT
245.02 NOT DISC. DELAY
256.14 MINUS ON WEOF CALL
259.02 BLANK SHIFT LEFT 6
910K
1.8K-1W
1.8K-1W
-60V
NEON
NEON
NEON
K
O
AC
K_0
K_0
I_k
A
I_k
T_x
T_x
T_x
I
NOTE:
X = -12V CLAMP RESET "POWER ON"; FIG. 257b. 24

FIG.226

WRITE BUS (C)

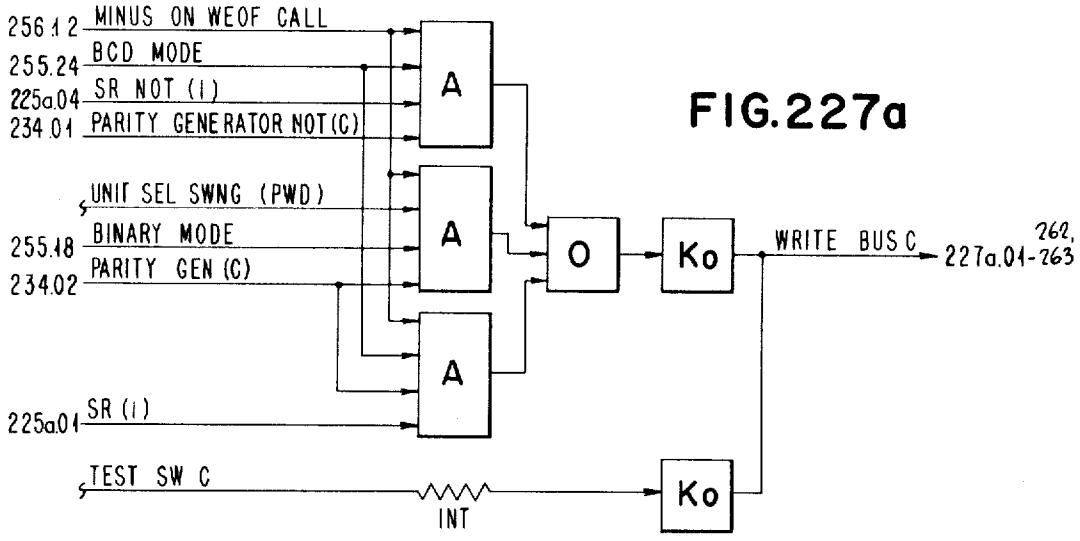


FIG.227a

WRITE BUS (B),(A)

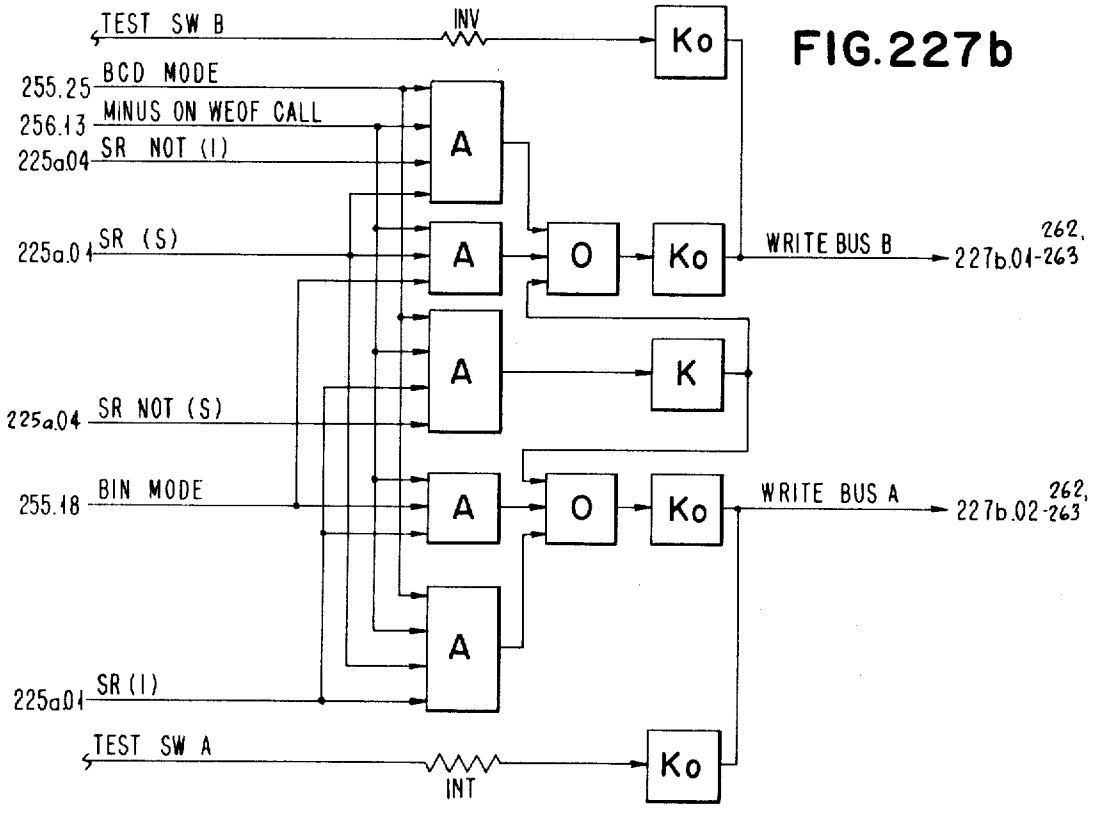


FIG.227b

WRITE BUS (8), (2)

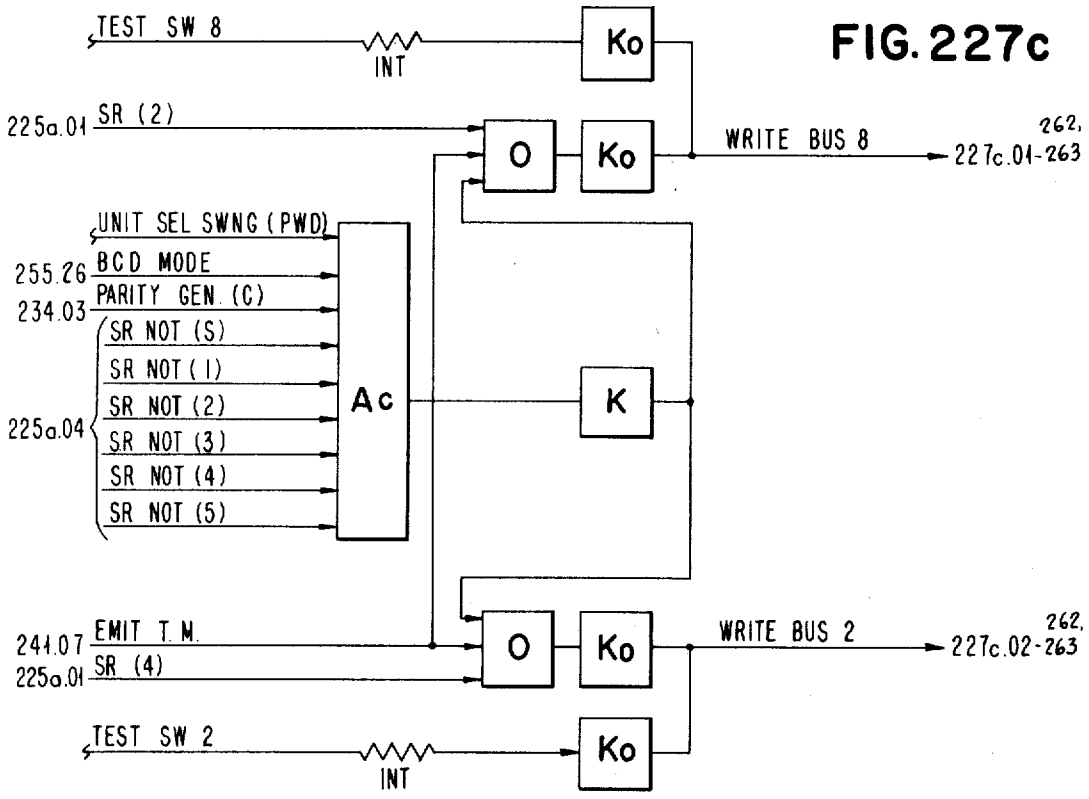


FIG. 227c

WRITE BUS (4), (1)

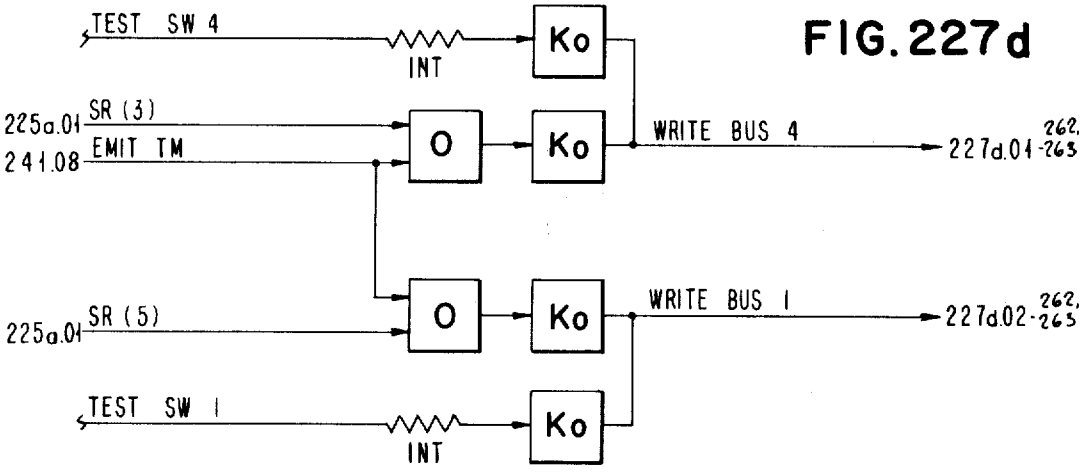
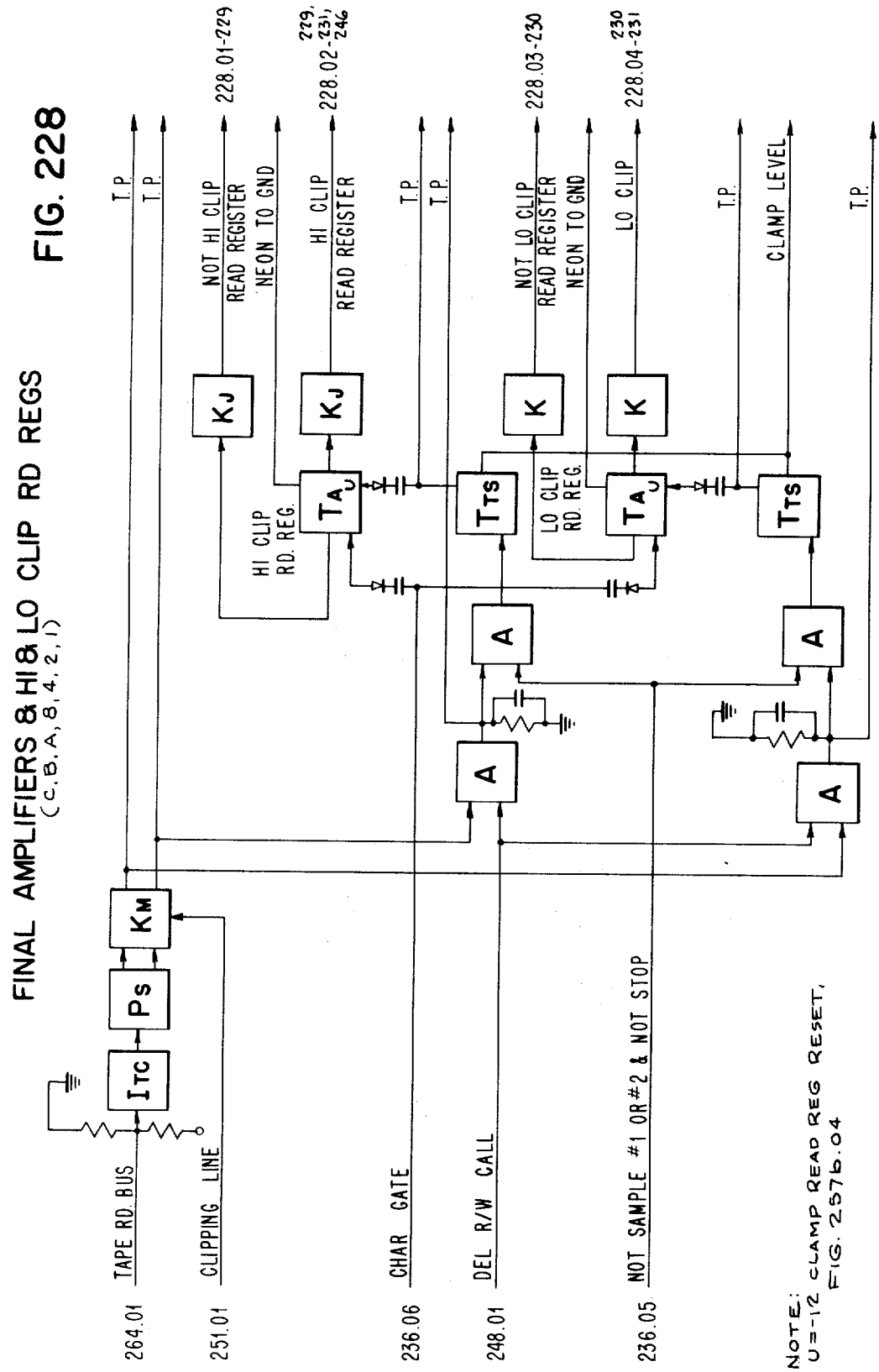


FIG. 227d

FIG. 228


FINAL AMPLIFIERS & HI & LO CLIP RD REGS
(C, B, A, 8, 4, 2, 1)
T.P.
T.P.
NOT HI CLIP
READ REGISTER
NEON TO GND
228.01-229
HI CLIP
READ REGISTER
228.02-229, 231, 246
T.P.
T.P.
NOT LO CLIP
READ REGISTER
NEON TO GND
228.03-230
LO CLIP
228.04-230 231
T.P.
CLAMP LEVEL
T.P.
KJ
KJ
K
K
HI CLIP RD. REG.
LO CLIP RD. REG.
TAU
TTS
TAU
TTS
A
A
A
A
KM
PS
ITC
TAPE RD. BUS
CLIPPING LINE
CHAR GATE
DEL R/W CALL
NOT SAMPLE #1 OR #2 & NOT STOP
264.01
251.01
236.06
248.01
236.05
NOTE:
U=-12 CLAMP READ REG RESET,
FIG. 257b.04

HI CLIP LATERAL PARITY CHECKER

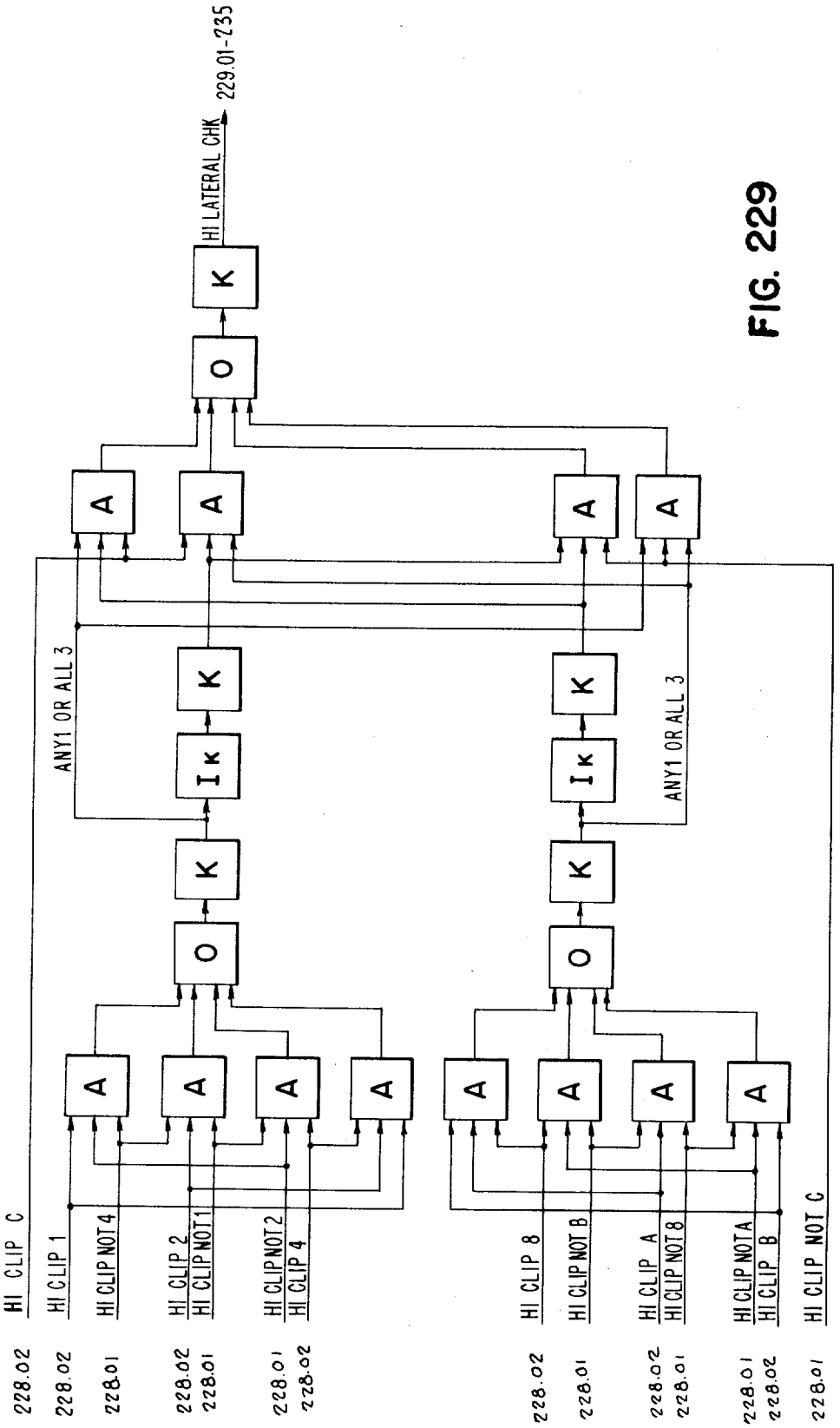
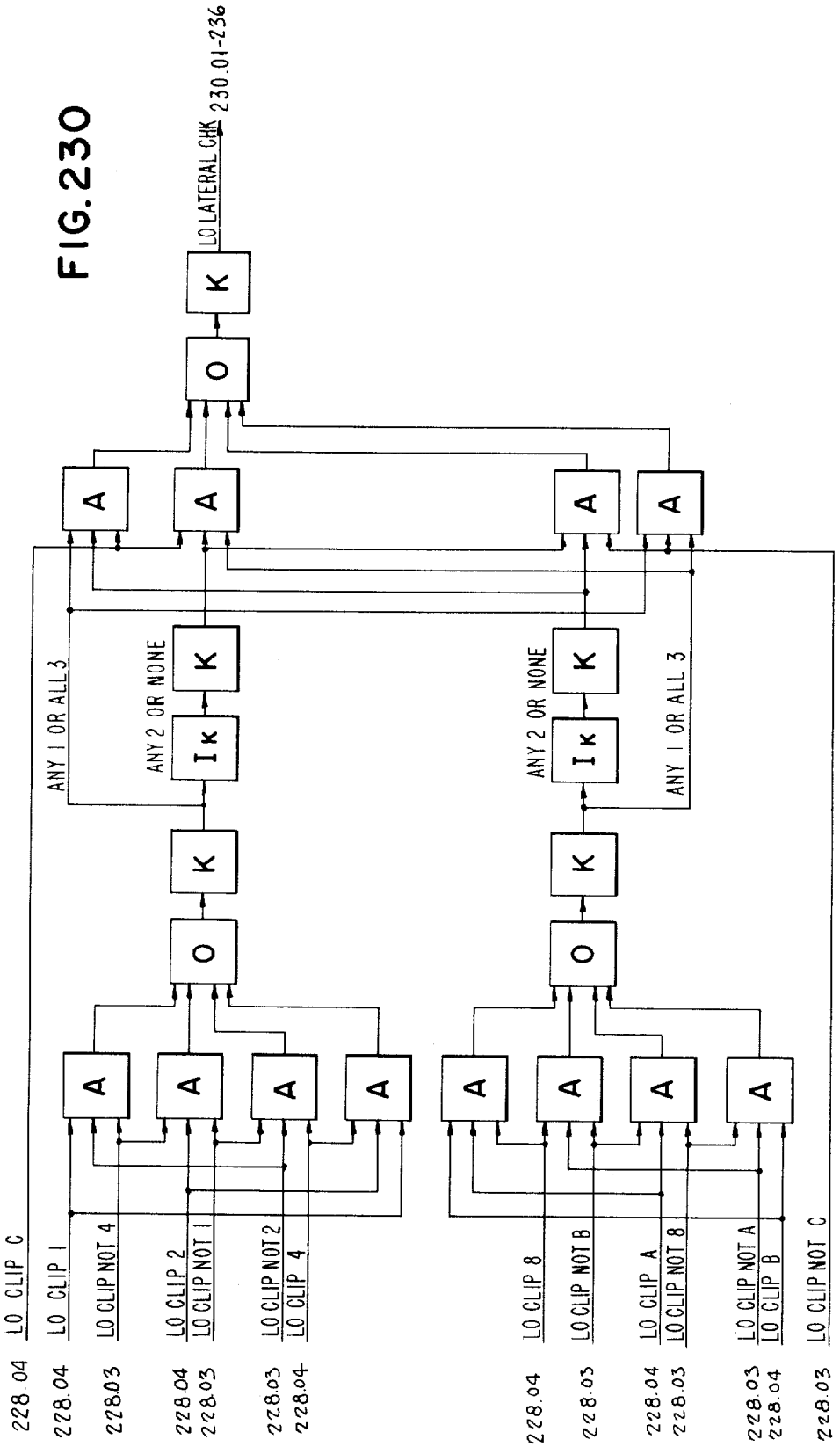


FIG. 229

FIG. 230

LO CLIP LATERAL PARITY CHECKER



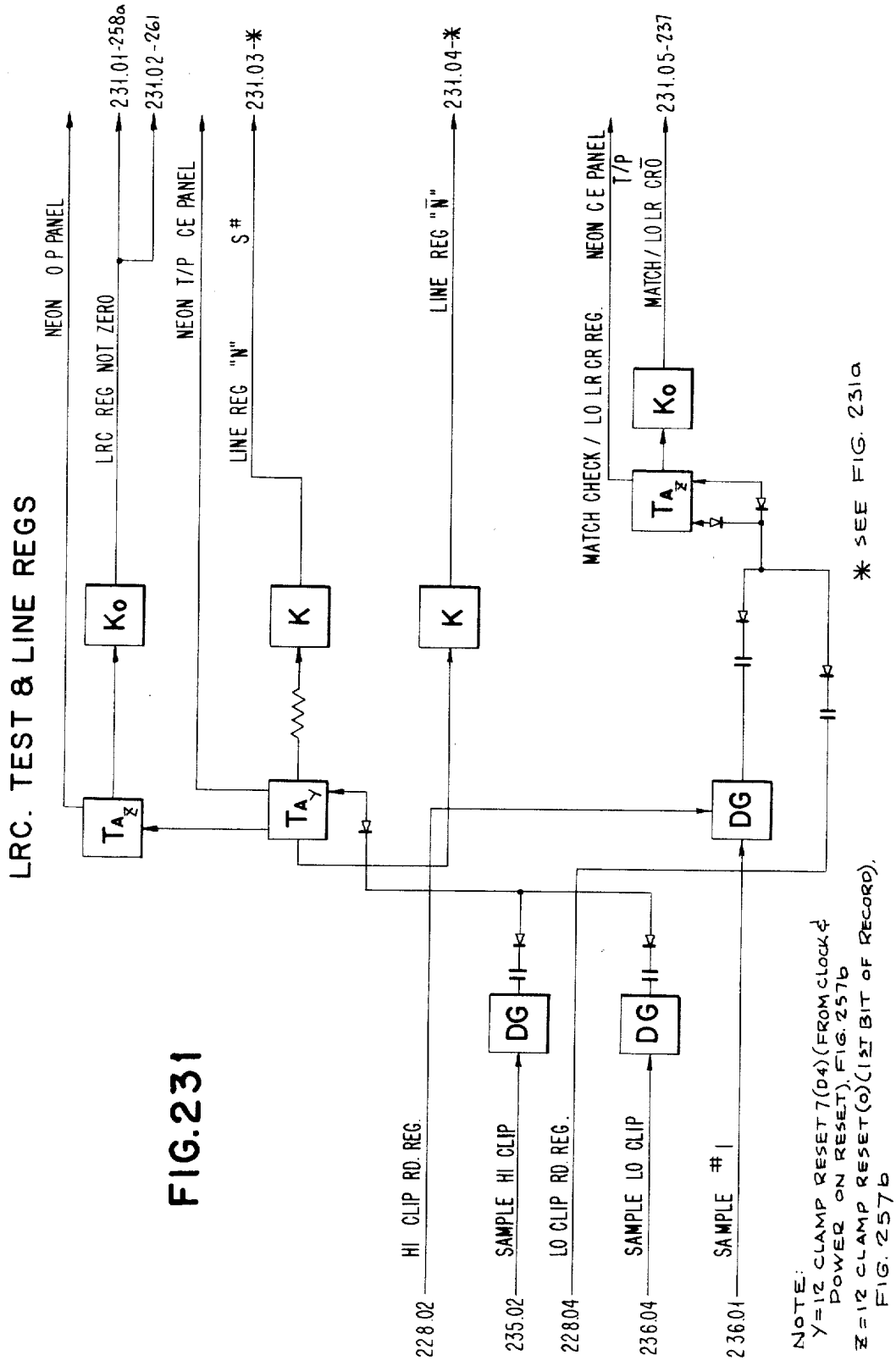
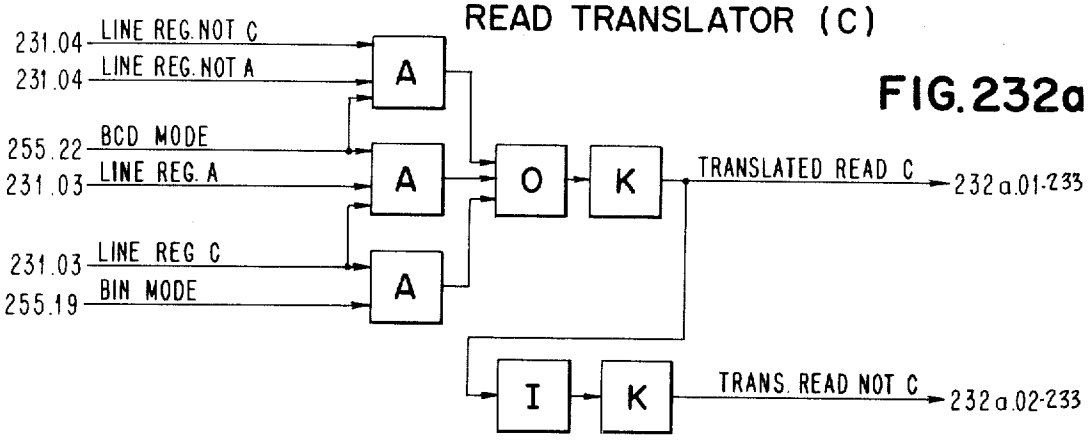

LRC. TEST & LINE REGS
NEON O P PANEL
LRC REG NOT ZERO
231.01-258a
231.02-261
NEON T/P CE PANEL
LINE REG "N" S#
231.03-*
LINE REG "N̄"
231.04-*
MATCH CHECK / LO LR CR REG
NEON C E PANEL T/P
MATCH / LO LR CRŌ
231.05-237
Ko
K
K
Ko
TAz
TAy
TAz
DG
DG
DG
HI CLIP RD. REG.
228.02
SAMPLE HI CLIP
235.02
LO CLIP RD. REG.
228.04
SAMPLE LO CLIP
236.04
SAMPLE #1
236.01
* SEE FIG. 231a
NOTE:
Y=12 CLAMP RESET 7(04)(FROM CLOCK POWER ON RESET), FIG. 257b
Z=12 CLAMP RESET(0)(1ST BIT OF RECORD), FIG. 257b

FIG.231

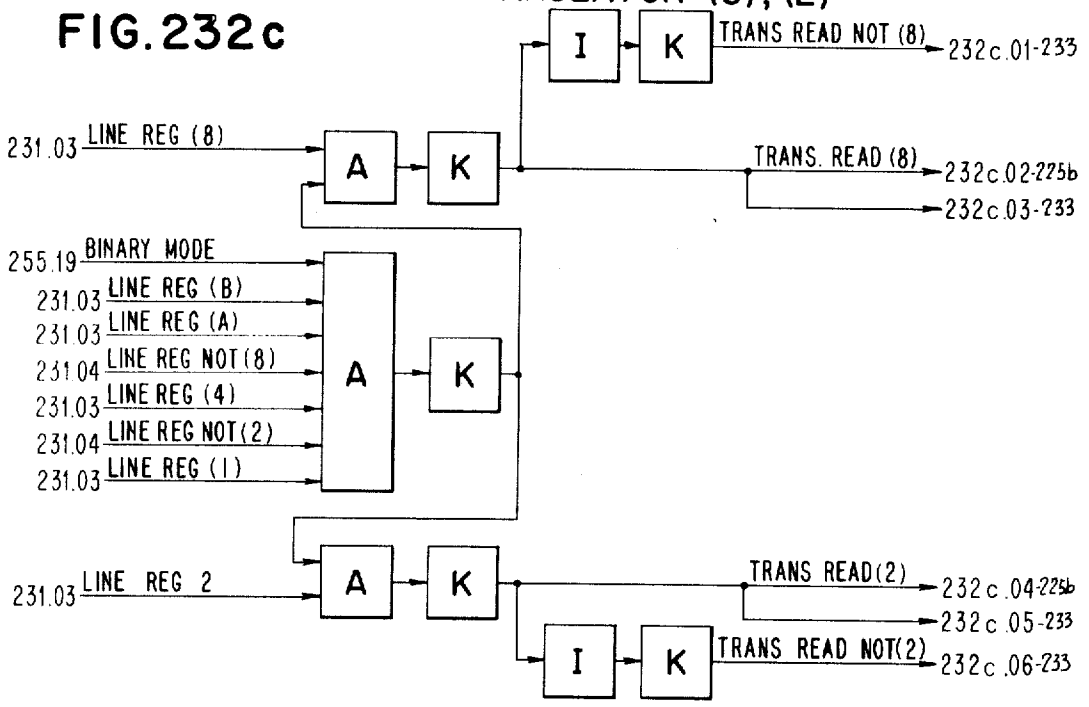
READ TRANSLATOR (C)

FIG. 232a



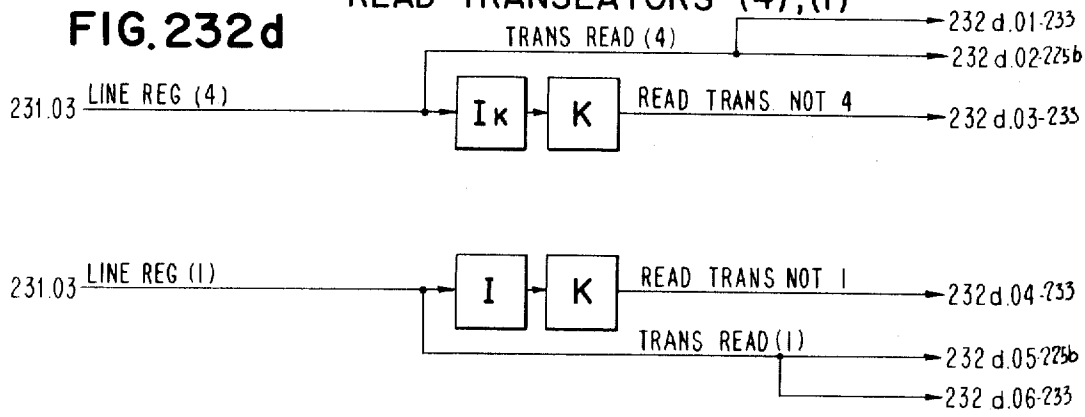
READ TRANSLATOR (8), (2)

FIG. 232c



READ TRANSLATORS (4), (1)

FIG. 232d



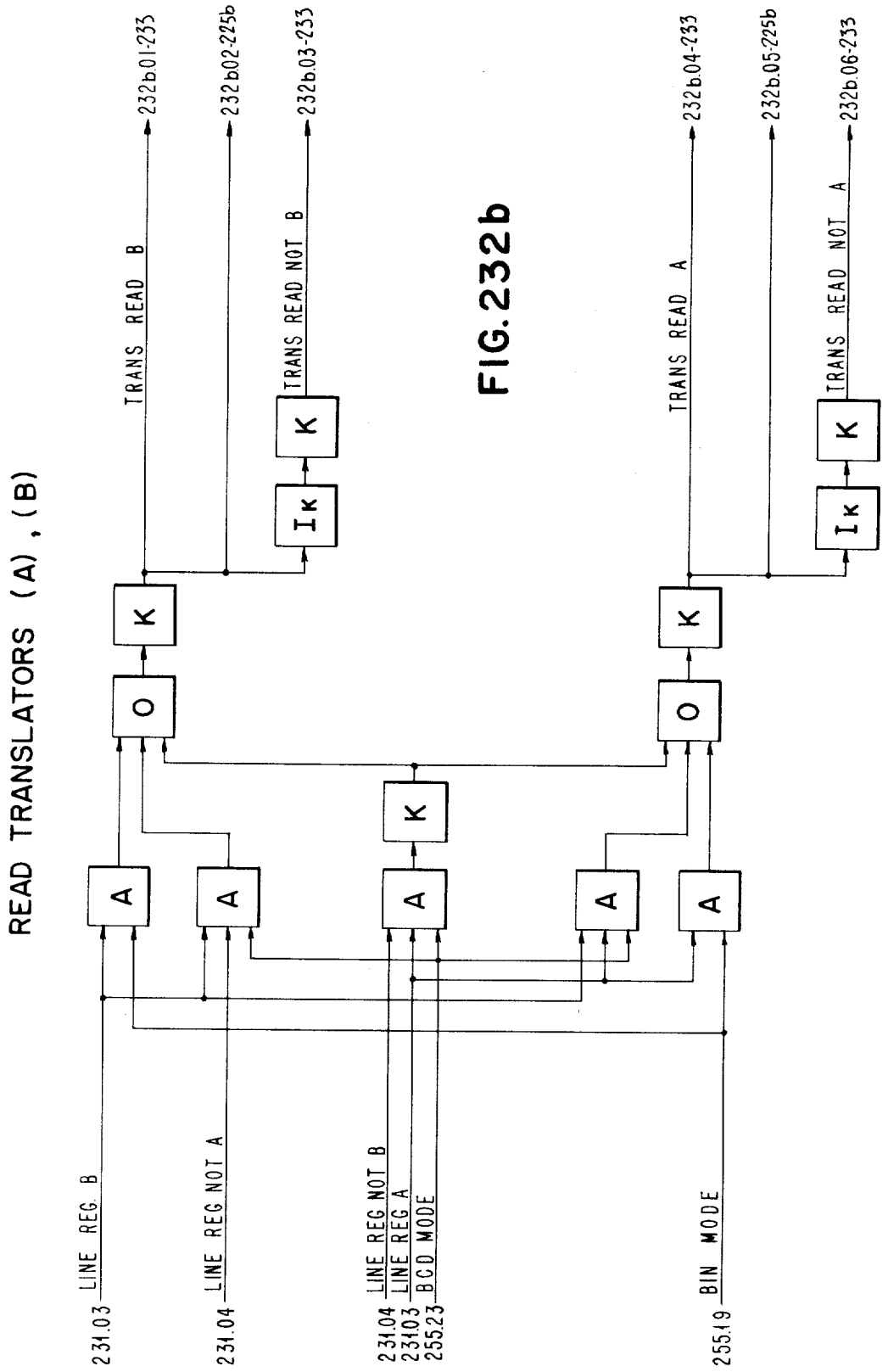

READ TRANSLATORS (A), (B)
231.03 LINE REG B
231.04 LINE REG NOT A
231.04 LINE REG NOT B
231.03 LINE REG A
255.23 BCD MODE
255.19 BIN MODE
A
K
O
Ik
TRANS READ B
TRANS READ NOT B
TRANS READ A
TRANS READ NOT A
232b.01-233
232b.02-225b
232b.03-233
232b.04-233
232b.05-225b
232b.06-233

FIG.232b

LATERAL PARITY CHECKING

FIG. 233

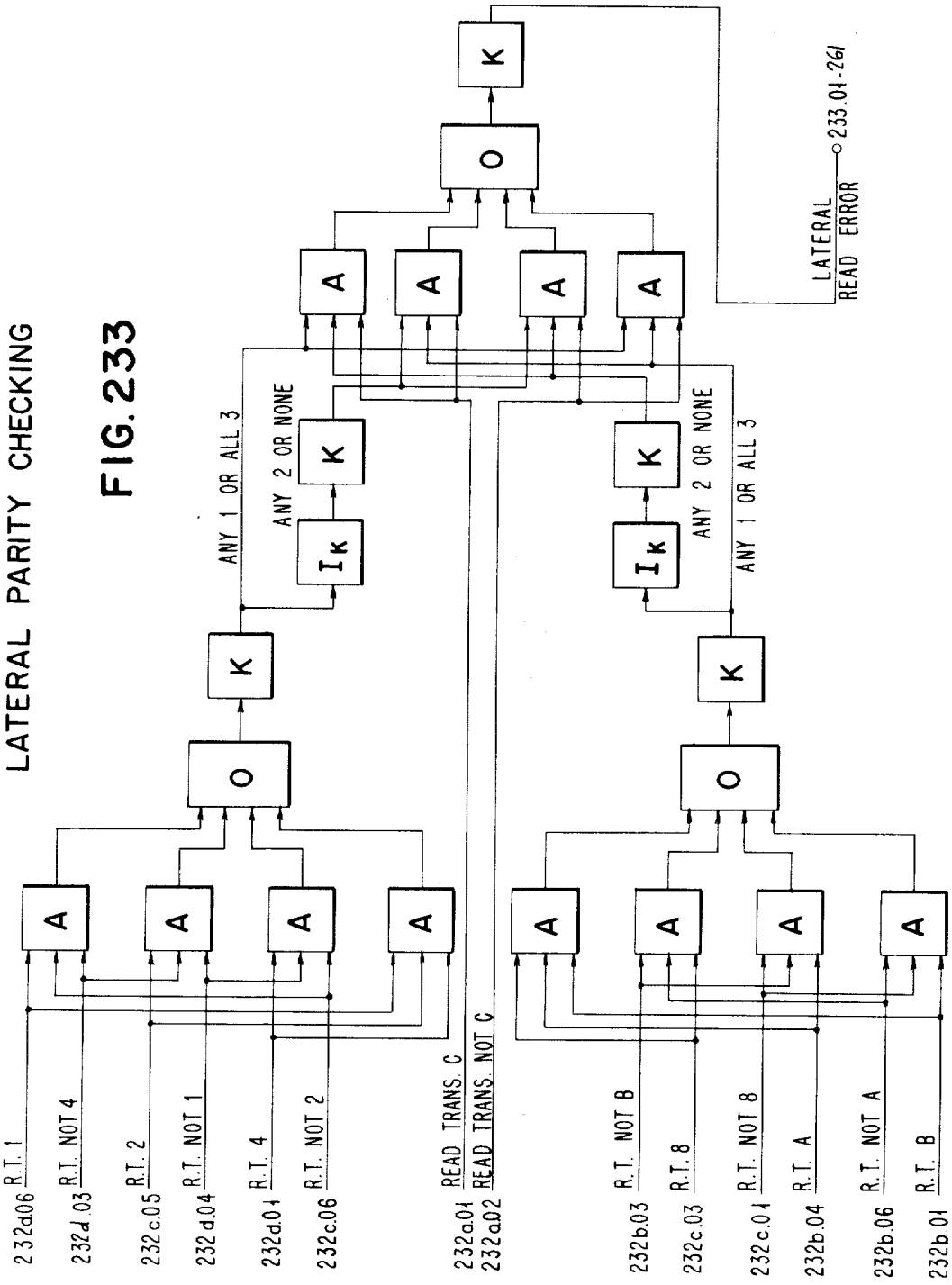
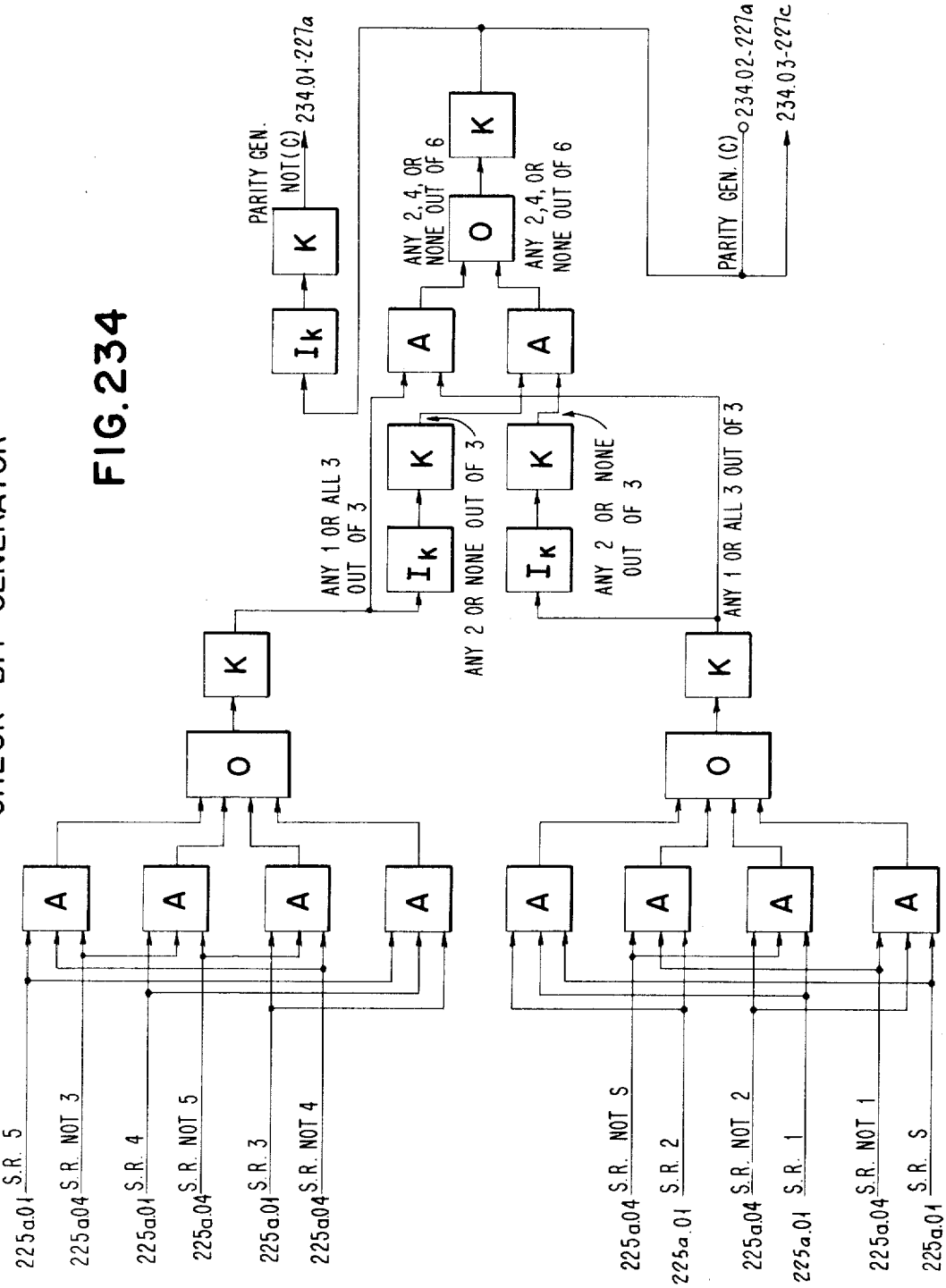


FIG.234

CHECK BIT GENERATOR



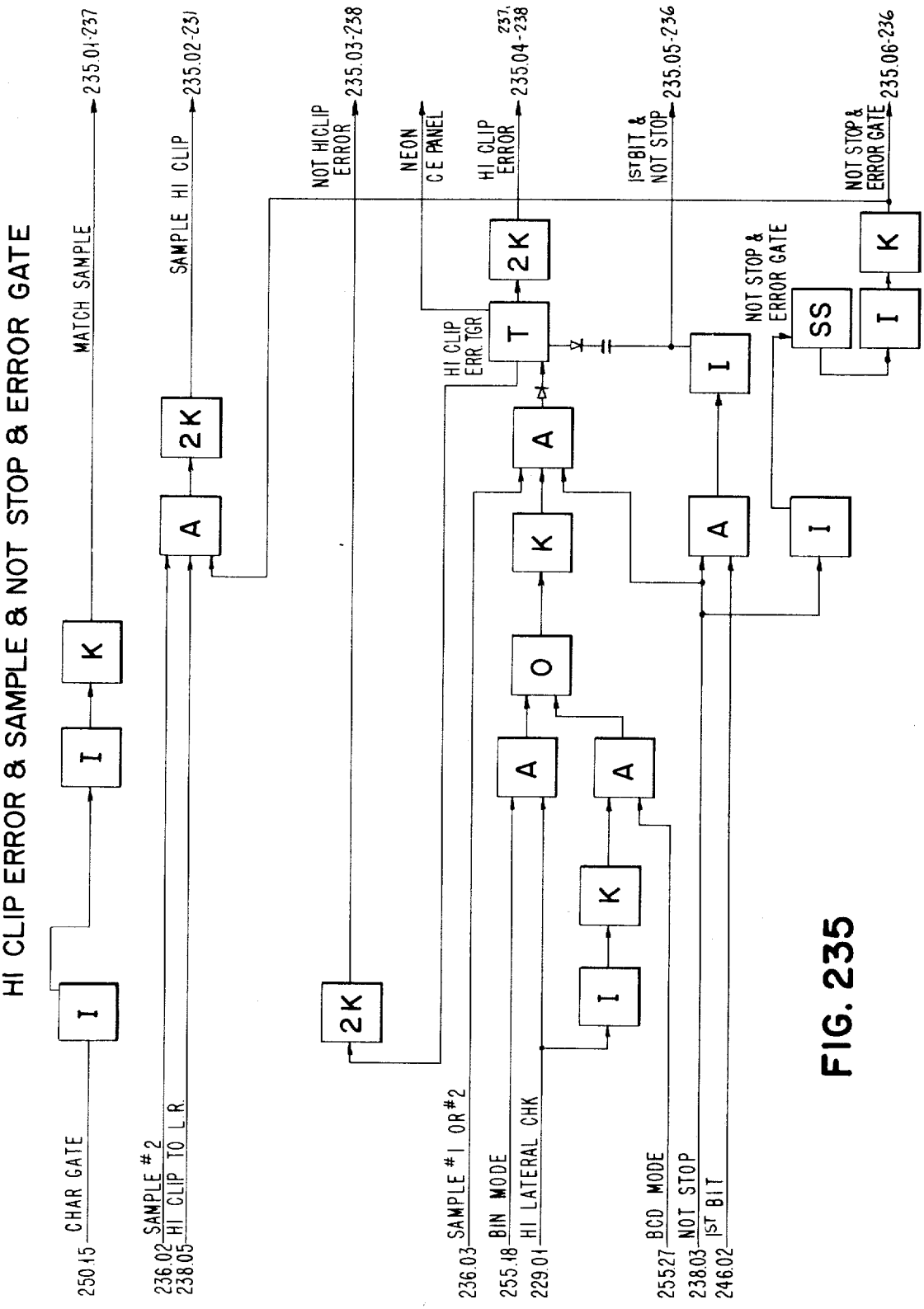

HI CLIP ERROR & SAMPLE & NOT STOP & ERROR GATE
250.15 CHAR GATE
I
I
K
MATCH SAMPLE
235.01-237
236.02 SAMPLE #2
238.05 HI CLIP TO L R
A
2K
SAMPLE HI CLIP
235.02-231
2K
NOT HI CLIP ERROR
235.03-238
NEON C E PANEL
236.03 SAMPLE #1 OR #2
HI CLIP ERR TGR
T
2K
HI CLIP ERROR
235.04-237, 238
255.18 BIN MODE
229.01 HI LATERAL CHK
A
A
O
K
A
K
I
I
255.27 BCD MODE
238.03 NOT STOP
246.02 1ST BIT
A
I
1ST BIT & NOT STOP
235.05-236
NOT STOP & ERROR GATE
SS
I
I
K
NOT STOP & ERROR GATE
235.06-236

FIG. 235

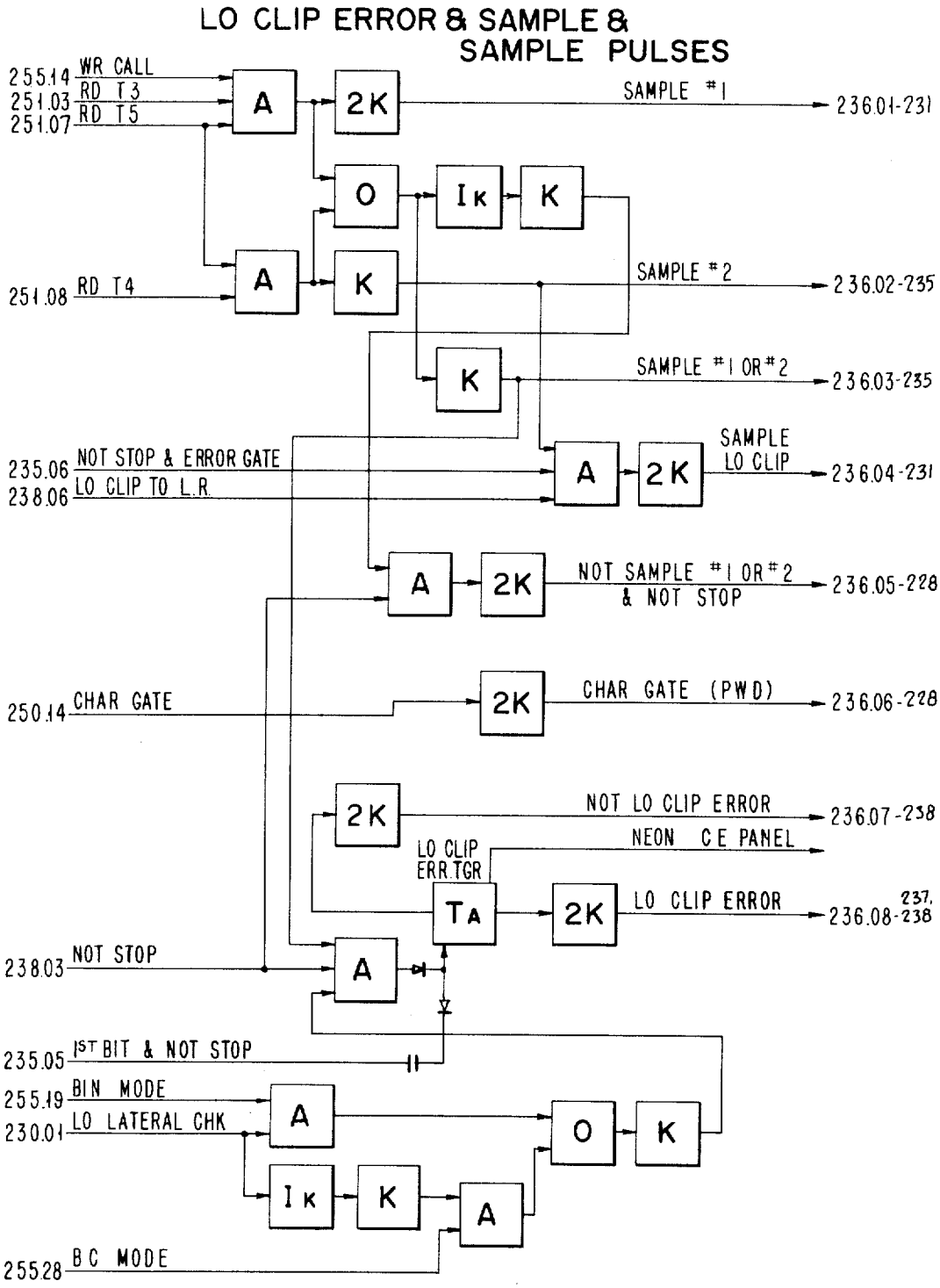

LO CLIP ERROR & SAMPLE & SAMPLE PULSES
255.14 WR CALL
251.03 RD T3
251.07 RD T5
A
2K
SAMPLE #1
236.01-231
O
IK
K
251.08 RD T4
A
K
SAMPLE #2
236.02-235
K
SAMPLE #1 OR #2
236.03-235
235.06 NOT STOP & ERROR GATE
238.06 LO CLIP TO L.R.
A
2K
SAMPLE LO CLIP
236.04-231
A
2K
NOT SAMPLE #1 OR #2 & NOT STOP
236.05-228
250.14 CHAR GATE
2K
CHAR GATE (PWD)
236.06-228
2K
NOT LO CLIP ERROR
236.07-238
NEON CE PANEL
LO CLIP ERR.TGR
TA
2K
LO CLIP ERROR
236.08-237, 238
238.03 NOT STOP
A
235.05 1ST BIT & NOT STOP
255.19 BIN MODE
230.01 LO LATERAL CHK
A
O
K
IK
K
A
255.28 BC MODE

FIG. 236

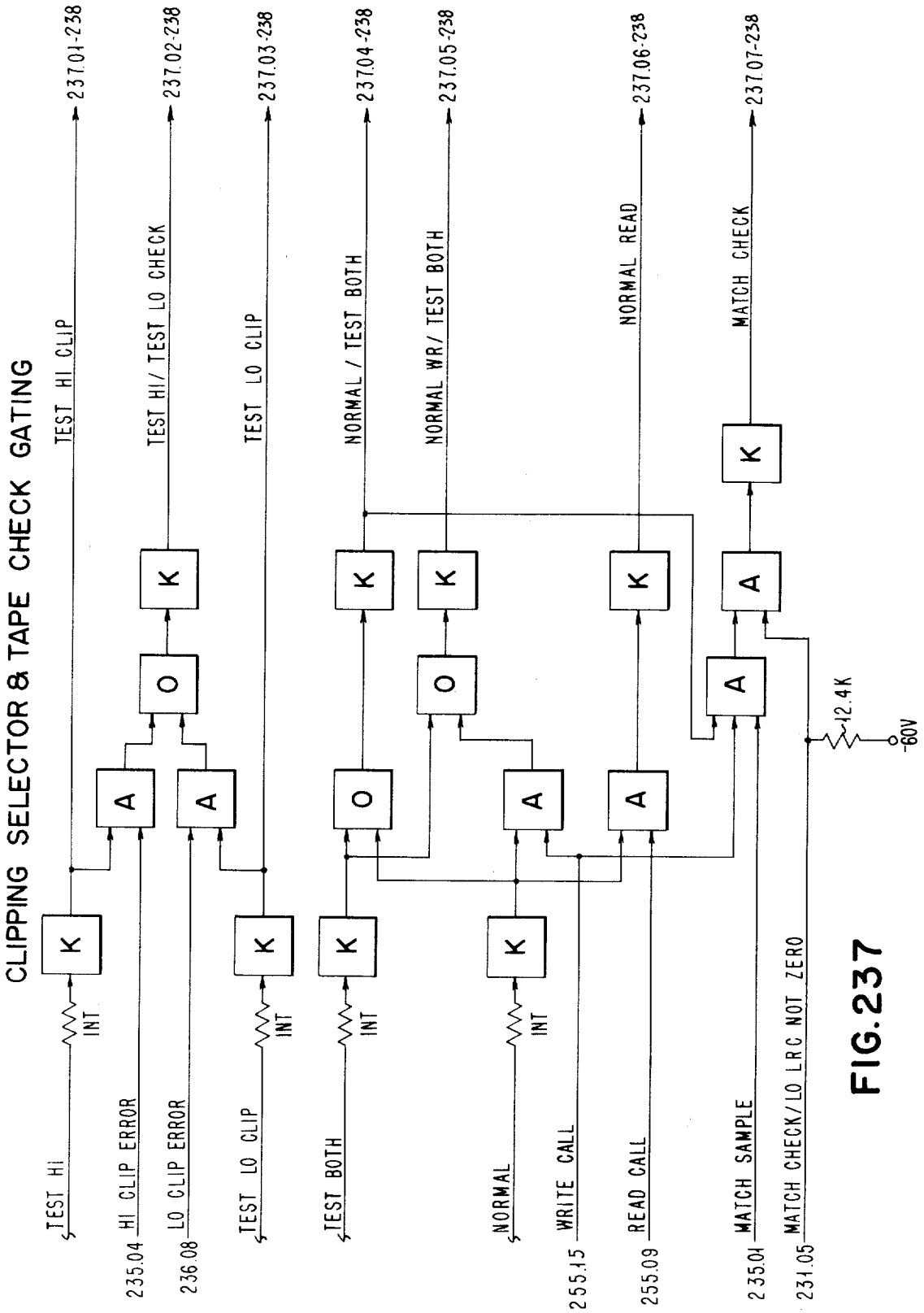

CLIPPING SELECTOR & TAPE CHECK GATING
TEST HI CLIP
237.01-238
TEST HI/ TEST LO CHECK
237.02-238
TEST LO CLIP
237.03-238
NORMAL / TEST BOTH
237.04-238
NORMAL WR/ TEST BOTH
237.05-238
NORMAL READ
237.06-238
MATCH CHECK
237.07-238
K
A
O
INT
12.4K
-60V
TEST HI
235.04 HI CLIP ERROR
236.08 LO CLIP ERROR
TEST LO CLIP
TEST BOTH
NORMAL
255.15 WRITE CALL
255.09 READ CALL
235.01 MATCH SAMPLE
231.05 MATCH CHECK/LO LRC NOT ZERO

FIG.237

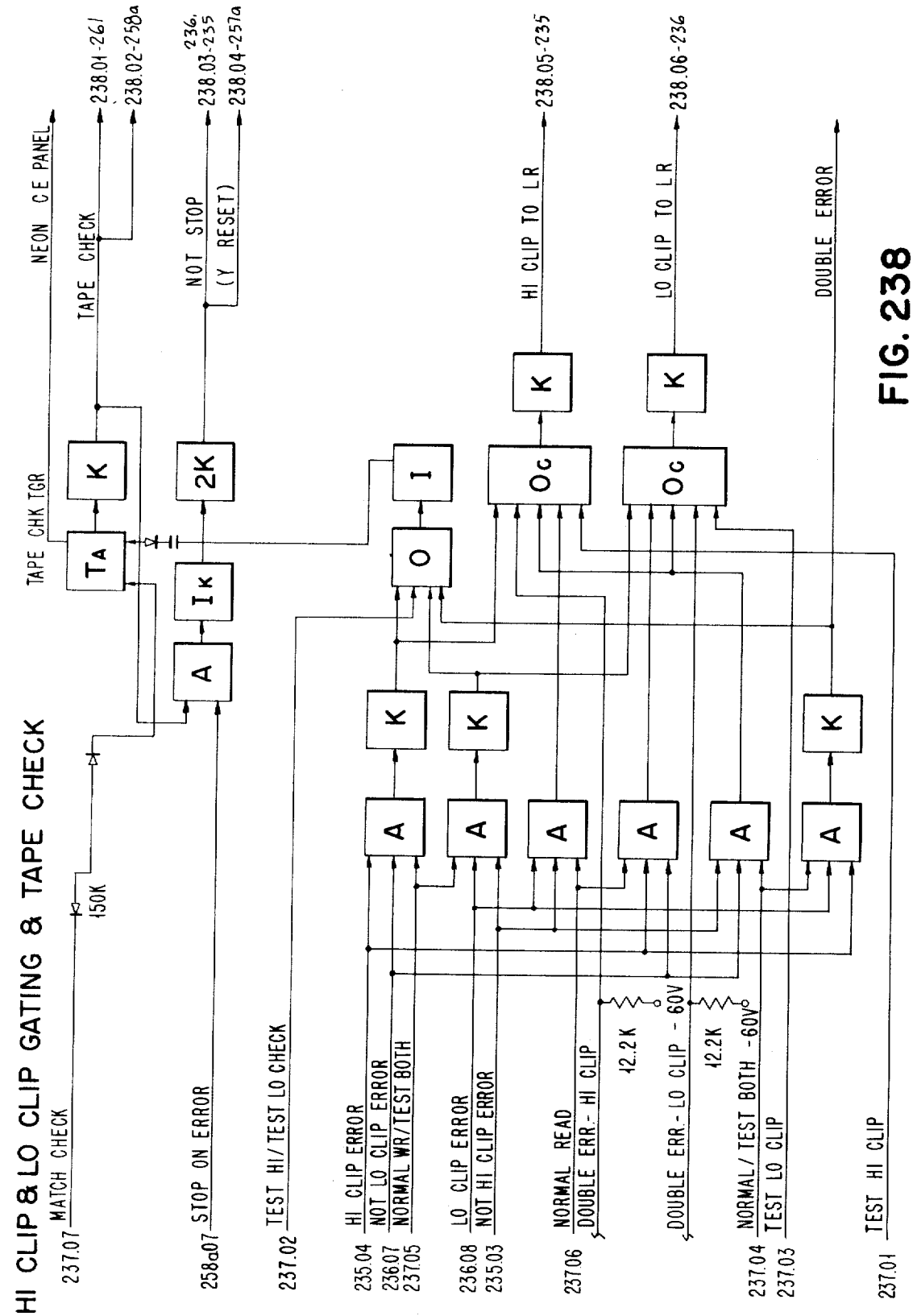
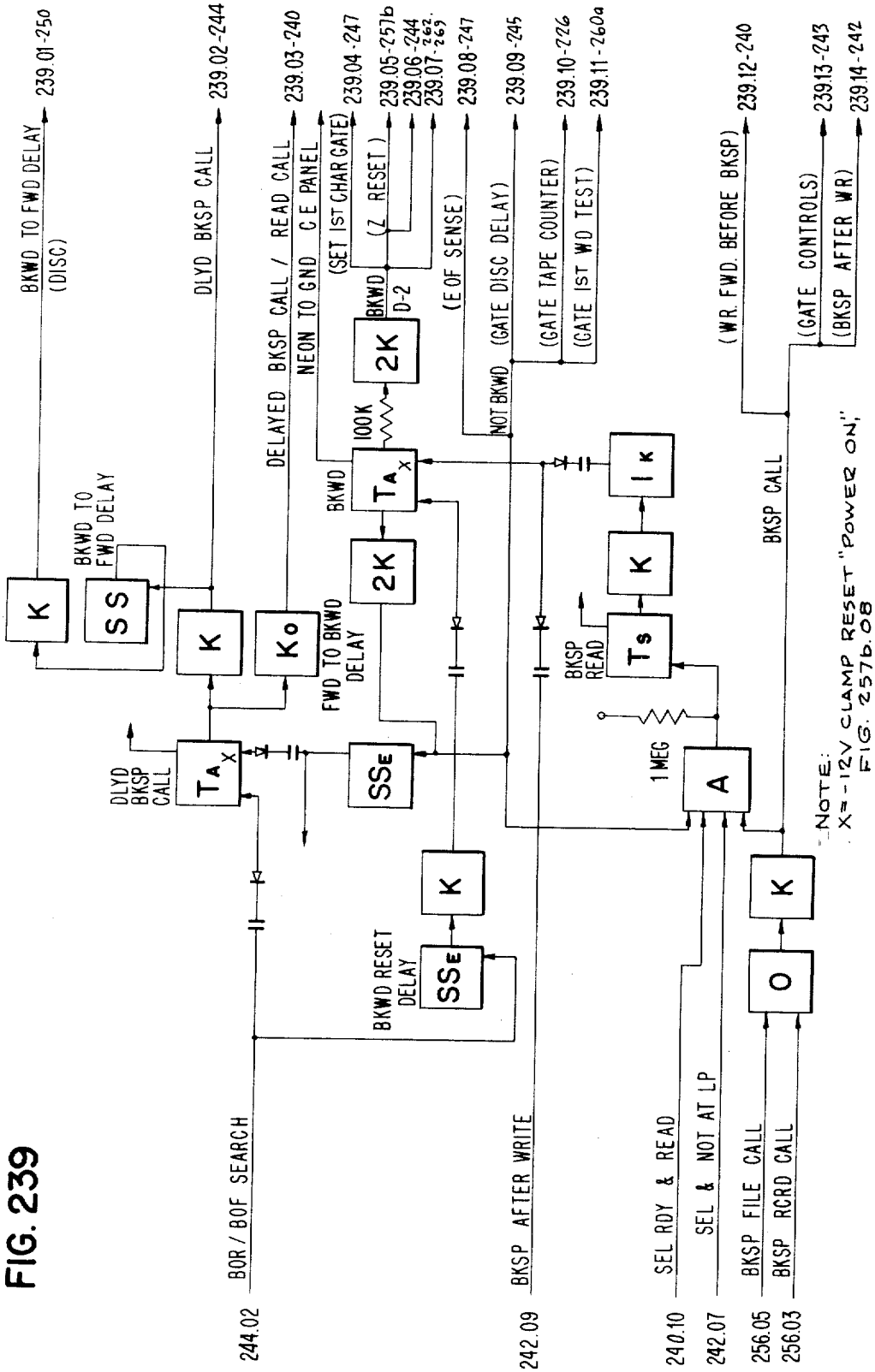

HI CLIP & LO CLIP GATING & TAPE CHECK
NEON C E PANEL
TAPE CHK TGR
TAPE CHECK
NOT STOP
(Y RESET)
238.01-261
238.02-258a
238.03-235
238.04-257a
238.05-235
238.06-236
HI CLIP TO LR
LO CLIP TO LR
DOUBLE ERROR
MATCH CHECK
STOP ON ERROR
TEST HI/TEST LO CHECK
HI CLIP ERROR
NOT LO CLIP ERROR
NORMAL WR/TEST BOTH
LO CLIP ERROR
NOT HI CLIP ERROR
NORMAL READ
DOUBLE ERR - HI CLIP
DOUBLE ERR - LO CLIP
NORMAL/TEST BOTH
TEST LO CLIP
TEST HI CLIP
150K
12.2K
12.2K
-60V
-60V
237.07
258a07
237.02
235.04
236.07
237.05
236.08
235.03
237.06
237.04
237.03
237.01
TA
K
IK
A
2K
I
O
Oc

FIG. 238

FIG. 239


BACK SPACE CONTROL
BKWD TO FWD DELAY
(DISC)
239.01-250
DLYD BKSP CALL
239.02-244
DELAYED BKSP CALL / READ CALL
239.03-240
NEON TO GND C E PANEL
(SET 1ST CHAR GATE)
239.04-247
(Z RESET)
239.05-257b
239.06-244
239.07-263
(E OF SENSE)
239.08-247
(GATE DISC DELAY)
239.09-245
(GATE TAPE COUNTER)
239.10-226
(GATE 1ST WD TEST)
239.11-260a
(WR. FWD. BEFORE BKSP)
239.12-240
(GATE CONTROLS)
239.13-243
(BKSP AFTER WR)
239.14-242
BKWD TO FWD DELAY
BKWD TO FWD DELAY
FWD TO BKWD DELAY
BKWD RESET DELAY
BKSP READ
BKSP CALL
DLYD BKSP CALL
100K
1 MEG
BKWD
D-2
NOT BKWD
K
SS
Ko
2K
TAx
SSE
Ts
1K
A
O
BOR / BOF SEARCH
BKSP AFTER WRITE
SEL RDY & READ
SEL & NOT AT LP
BKSP FILE CALL
BKSP RCRD CALL
244.02
242.09
240.10
242.07
256.05
256.03
NOTE:
X = -12V CLAMP RESET "POWER ON"
FIG. 257b.08

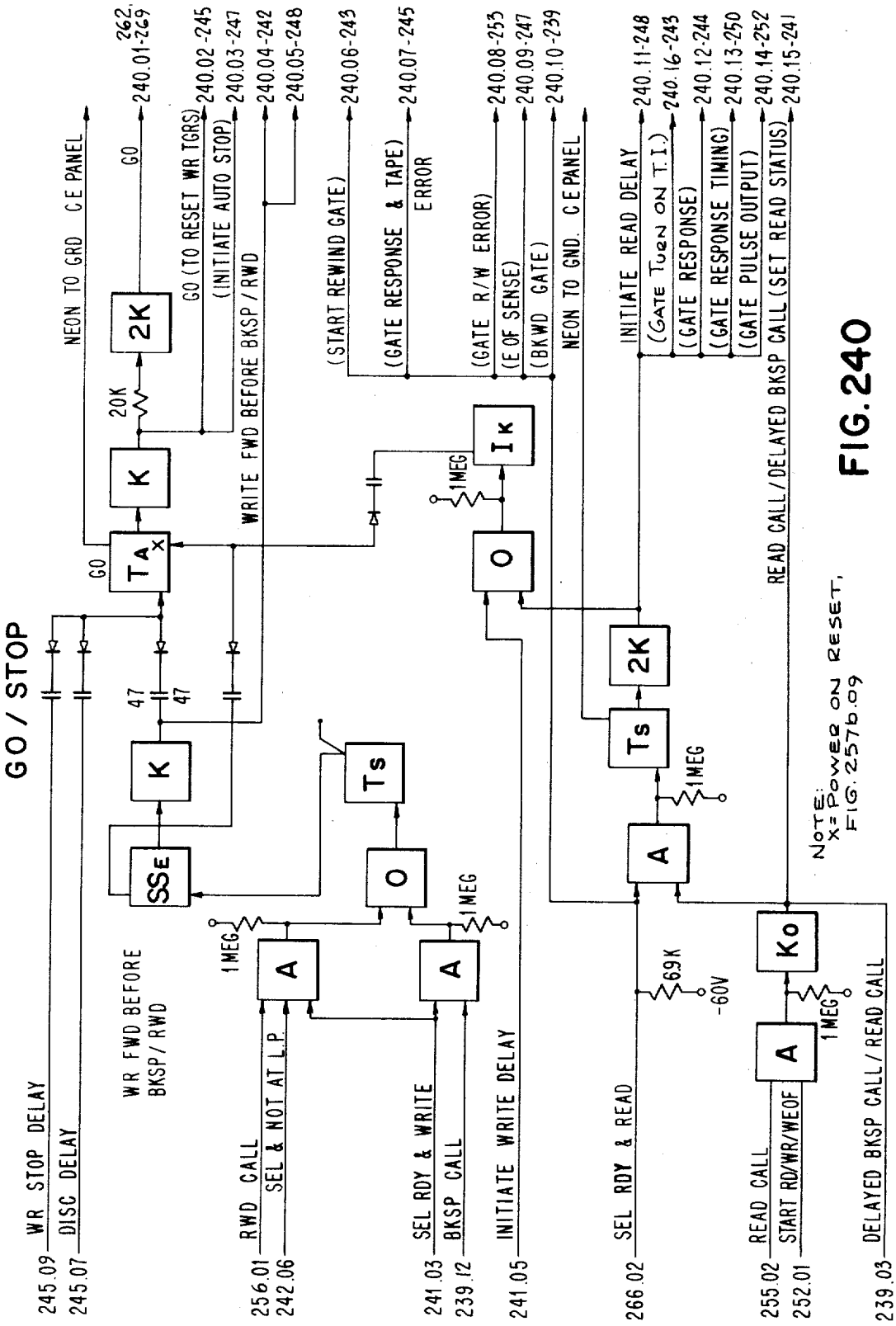
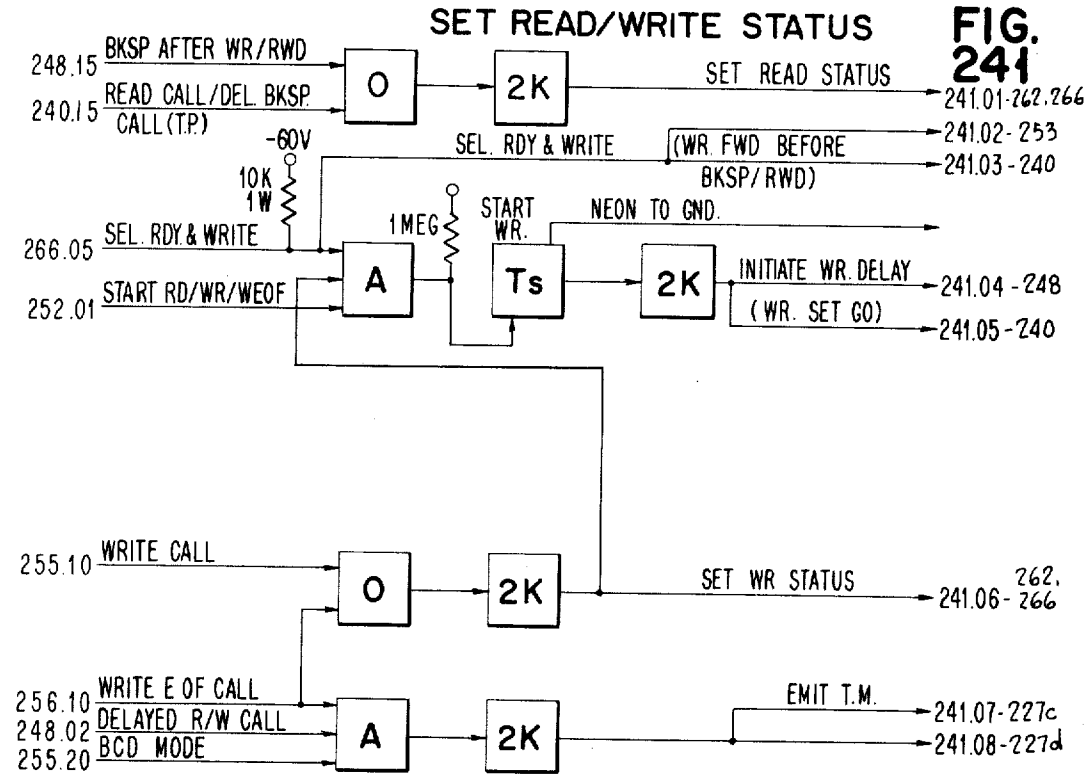

GO / STOP
245.09 WR STOP DELAY
245.07 DISC DELAY
WR FWD BEFORE BKSP / RWD
256.01 RWD CALL
242.06 SEL & NOT AT L.P.
241.03 SEL RDY & WRITE
239.12 BKSP CALL
241.05 INITIATE WRITE DELAY
266.02 SEL RDY & READ
255.02 READ CALL
252.01 START RD/WR/WEOF
239.03 DELAYED BKSP CALL / READ CALL
NEON TO GRD C E PANEL
GO
WRITE FWD BEFORE BKSP / RWD
GO (TO RESET WR TGRS)
(INITIATE AUTO STOP)
(START REWIND GATE)
(GATE RESPONSE & TAPE)
ERROR
(GATE R/W ERROR)
(E OF SENSE)
(BKWD GATE)
NEON TO GND. C E PANEL
INITIATE READ DELAY
(GATE TURN ON T.I.)
(GATE RESPONSE)
(GATE RESPONSE TIMING)
(GATE PULSE OUTPUT)
READ CALL / DELAYED BKSP CALL (SET READ STATUS)
240.01-269
240.02-245
240.03-247
240.04-242
240.05-248
240.06-243
240.07-245
240.08-253
240.09-247
240.10-239
240.11-248
240.16-243
240.12-244
240.13-250
240.14-252
240.15-241
262
20K
2K
K
47
47
TAx
SSE
A
Ts
O
Ik
Ko
1MEG
69K
-60V
NOTE:
X = POWER ON RESET,
FIG. 257b.09

FIG. 240


SET READ/WRITE STATUS
FIG. 241
248.15 BKSP AFTER WR/RWD
240.15 READ CALL/DEL. BKSP CALL (T.P.)
O
2K
SET READ STATUS
241.01-262.266
-60V
SEL. RDY & WRITE
(WR. FWD BEFORE BKSP/RWD)
241.02-253
241.03-240
10K 1W
1MEG
START WR.
NEON TO GND.
266.05 SEL. RDY & WRITE
252.01 START RD/WR/WEOF
A
Ts
2K
INITIATE WR. DELAY
(WR. SET GO)
241.04-248
241.05-240
255.10 WRITE CALL
O
2K
SET WR STATUS
241.06-262, 266
256.10 WRITE E OF CALL
248.02 DELAYED R/W CALL
255.20 BCD MODE
A
2K
EMIT T.M.
241.07-227c
241.08-227d

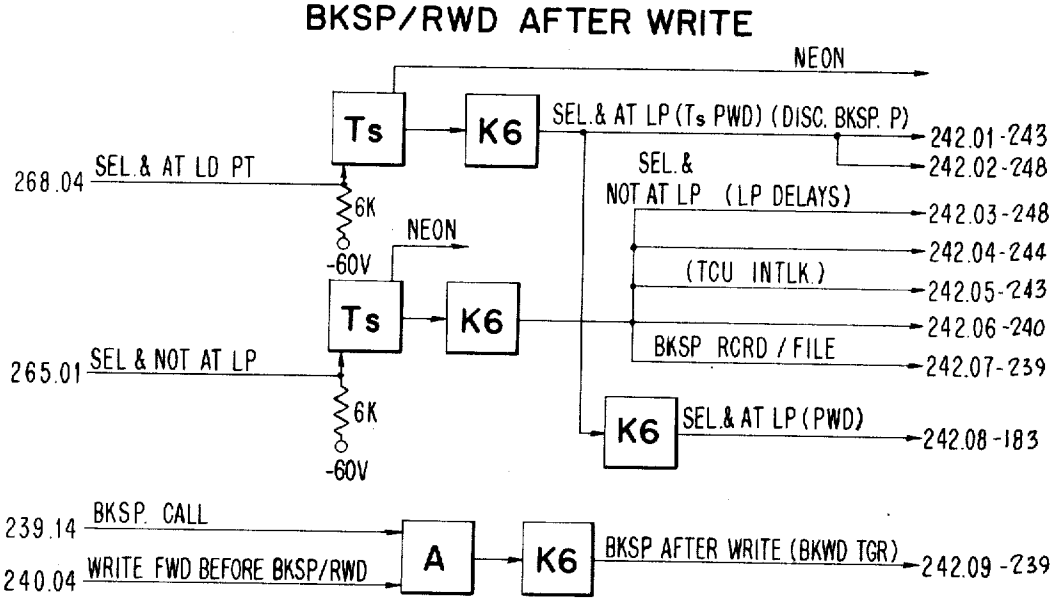

BKSP/RWD AFTER WRITE
NEON
Ts
K6
SEL.& AT LP (Ts PWD) (DISC. BKSP. P)
242.01-243
242.02-248
268.04 SEL.& AT LD PT
6K
-60V
NEON
SEL.& NOT AT LP (LP DELAYS)
242.03-248
242.04-244
(TCU INTLK.)
242.05-243
242.06-240
BKSP RCRD / FILE
242.07-239
265.01 SEL & NOT AT LP
6K
-60V
K6
SEL.& AT LP (PWD)
242.08-183
239.14 BKSP. CALL
240.04 WRITE FWD BEFORE BKSP/RWD
A
K6
BKSP AFTER WRITE (BKWD TGR)
242.09-239

FIG.242

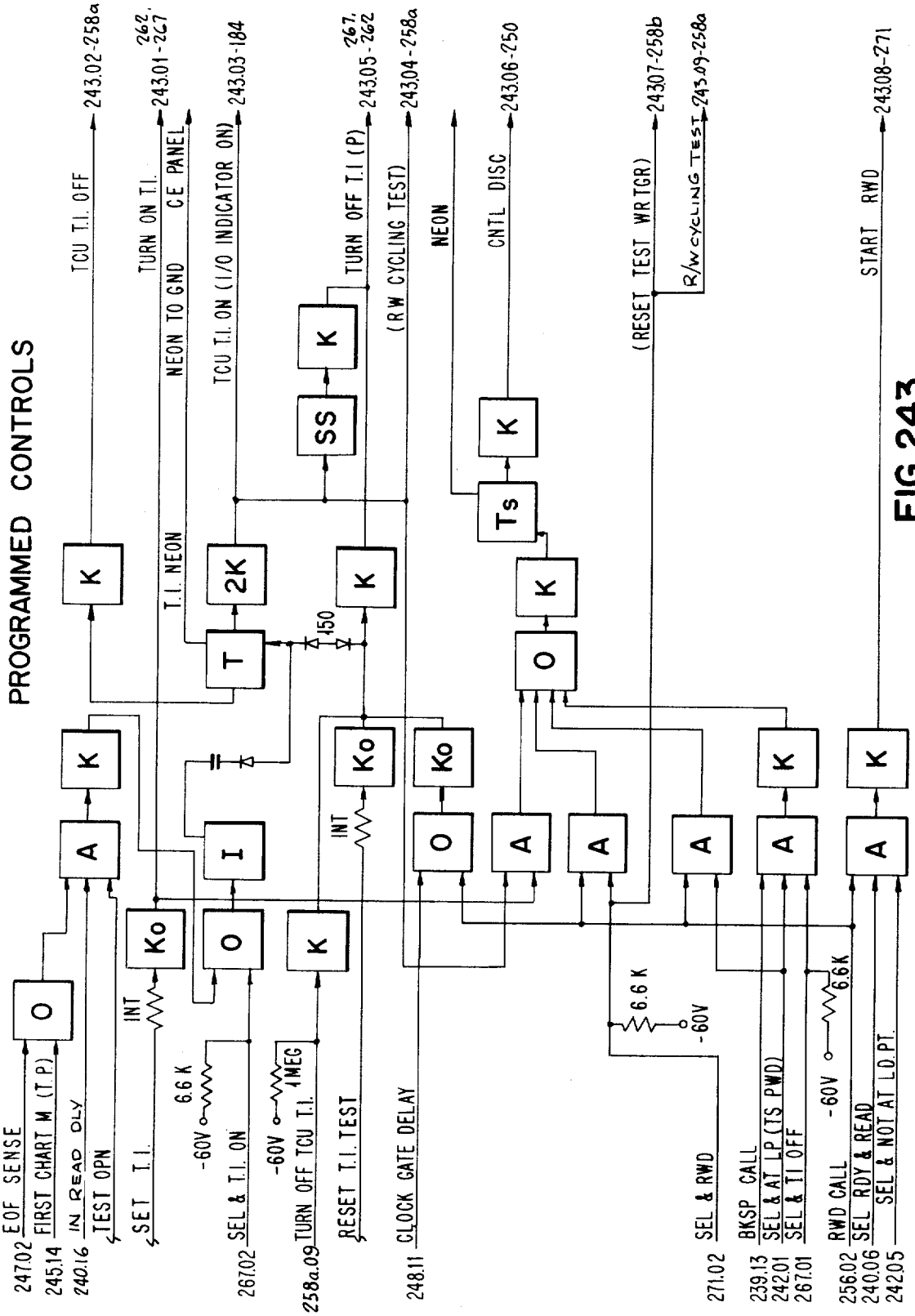

PROGRAMMED CONTROLS
247.02 EOF SENSE
245.14 FIRST CHART M (T.P.)
240.16 IN READ ONLY
TEST OPN
SET T.I.
INT
6.6 K
-60V
SEL & T.I. ON
267.02
-60V
1MEG
258a.09 TURN OFF TCU T.I.
RESET T.I. TEST
INT
248.11 CLOCK GATE DELAY
150
T.I. NEON
NEON TO GND
TCU T.I. ON (I/O INDICATOR ON)
TURN OFF T.I (P)
(R W CYCLING TEST)
NEON
CNTL DISC
(RESET TEST WR TGR)
R/W CYCLING TEST
START RWD
TCU T.I. OFF
TURN ON T.I.
CE PANEL
243.02-258a
243.01-262, 267
243.03-184
243.05-262, 267
243.04-258a
243.06-250
243.07-258b
243.09-258a
243.08-271
6.6 K
-60V
271.02 SEL & RWD
239.13 BKSP CALL
242.01 SEL & AT LP (TS PWD)
267.01 SEL & TI OFF
6.6 K
-60V
256.02 RWD CALL
240.06 SEL RDY & READ
242.05 SEL & NOT AT LD PT.
K
A
O
I
Ko
T
2K
SS
Ts

FIG.243

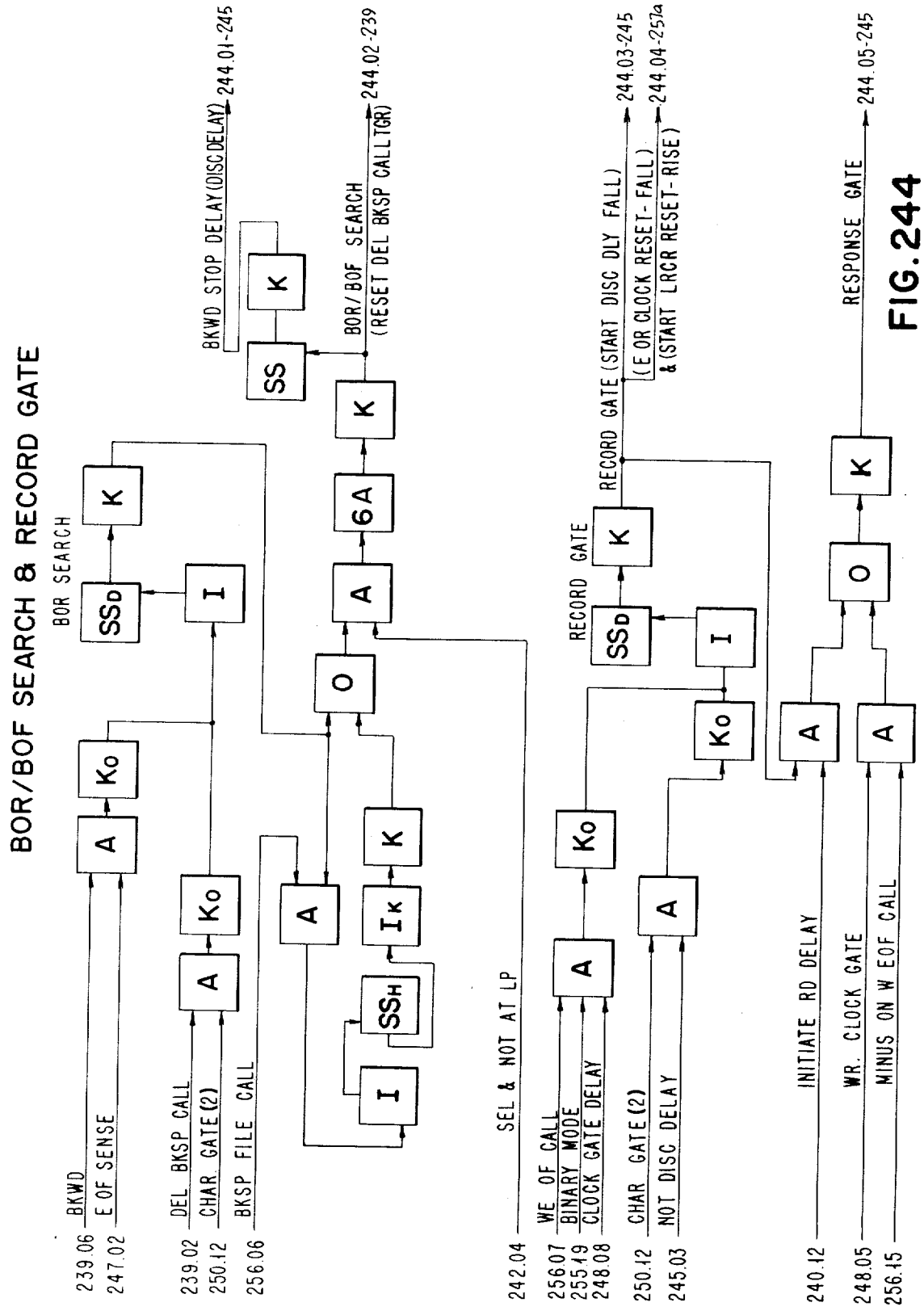

BOR/BOF SEARCH & RECORD GATE
BOR SEARCH
BKWD
E OF SENSE
239.06
247.02
DEL BKSP CALL
CHAR GATE (2)
BKSP FILE CALL
239.02
250.12
256.06
SEL & NOT AT LP
242.04
WE OF CALL
BINARY MODE
CLOCK GATE DELAY
256.07
255.19
248.08
CHAR GATE (2)
NOT DISC DELAY
250.12
245.03
INITIATE RD DELAY
240.12
WR. CLOCK GATE
MINUS ON W EOF CALL
248.05
256.15
BKWD STOP DELAY (DISC DELAY)
244.01-245
BOR/BOF SEARCH
(RESET DEL BKSP CALL TGR)
244.02-239
RECORD GATE (START DISC DLY FALL)
(E OR CLOCK RESET-FALL)
& (START LRCR RESET-RISE)
244.03-245
244.04-257a
RESPONSE GATE
244.05-245
RECORD GATE
A
Ko
SSD
I
K
O
6A
SSH
Ik

FIG. 244

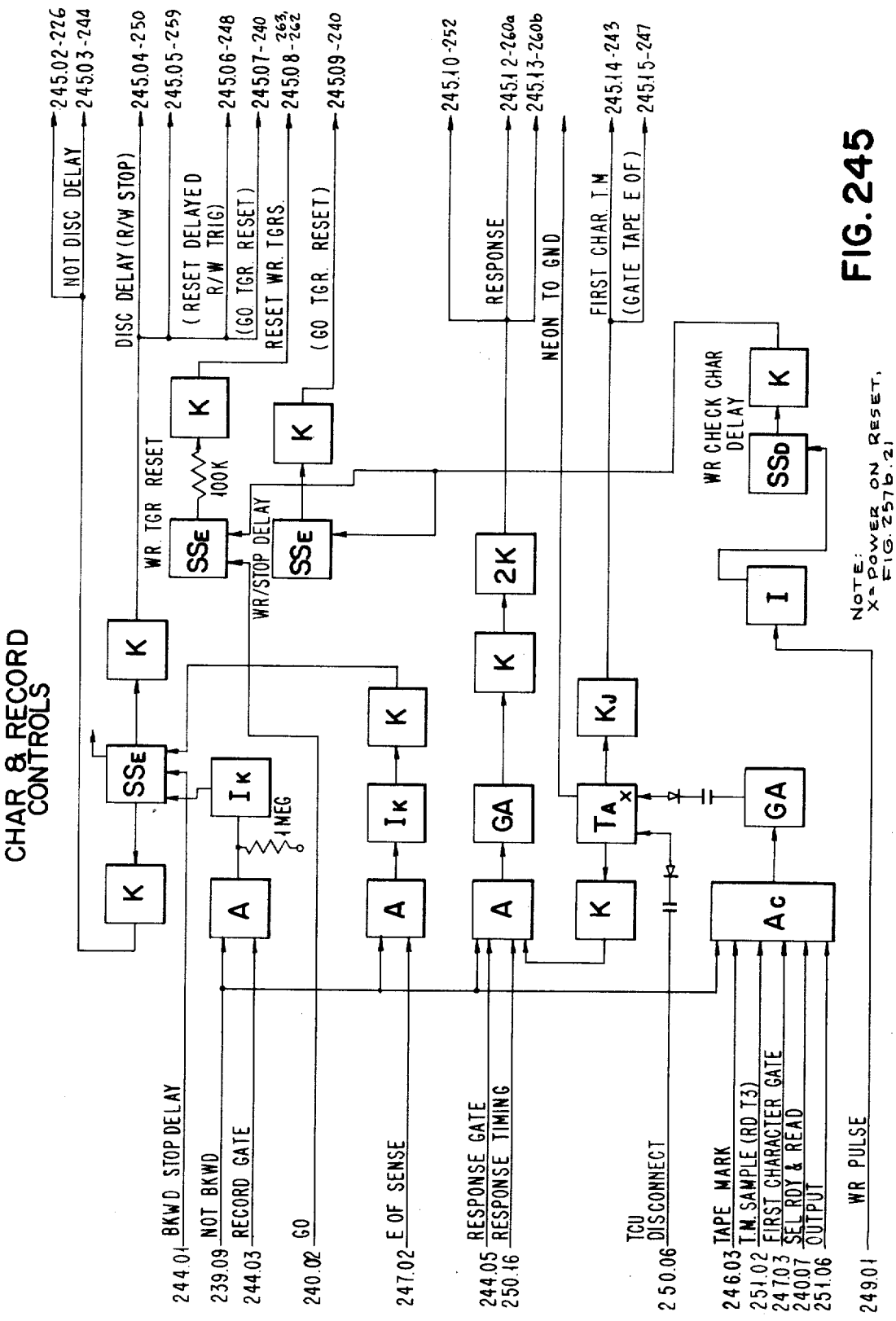

CHAR & RECORD CONTROLS
245.02-226 NOT DISC DELAY
245.03-244
245.04-250 DISC DELAY (R/W STOP)
245.05-259 (RESET DELAYED R/W TRIG)
245.06-248 (GO TGR. RESET)
245.07-240 RESET WR. TGRS.
245.08-263, 262
245.09-240 (GO TGR. RESET)
245.10-252 RESPONSE
245.12-260a
245.13-260b NEON TO GND
245.14-243 FIRST CHAR. T.M.
245.15-247 (GATE TAPE E OF)
WR. TGR RESET
WR/STOP DELAY
WR CHECK CHAR DELAY
100K
1MEG
K
SSE
SSD
I K
A
GA
2K
KJ
TA X
Ac
I
244.01 BKWD STOP DELAY
239.09 NOT BKWD
244.03 RECORD GATE
240.02 GO
247.02 E OF SENSE
244.05 RESPONSE GATE
250.16 RESPONSE TIMING
TCU
250.06 DISCONNECT
246.03 TAPE MARK
251.02 T.M. SAMPLE (RD T3)
247.03 FIRST CHARACTER GATE
240.07 SEL RDY & READ
251.06 OUTPUT
249.01 WR PULSE
NOTE: X = POWER ON RESET, FIG. 257b.21

FIG. 245

TAPE MARK MATRIX & 7-WAY "OR"

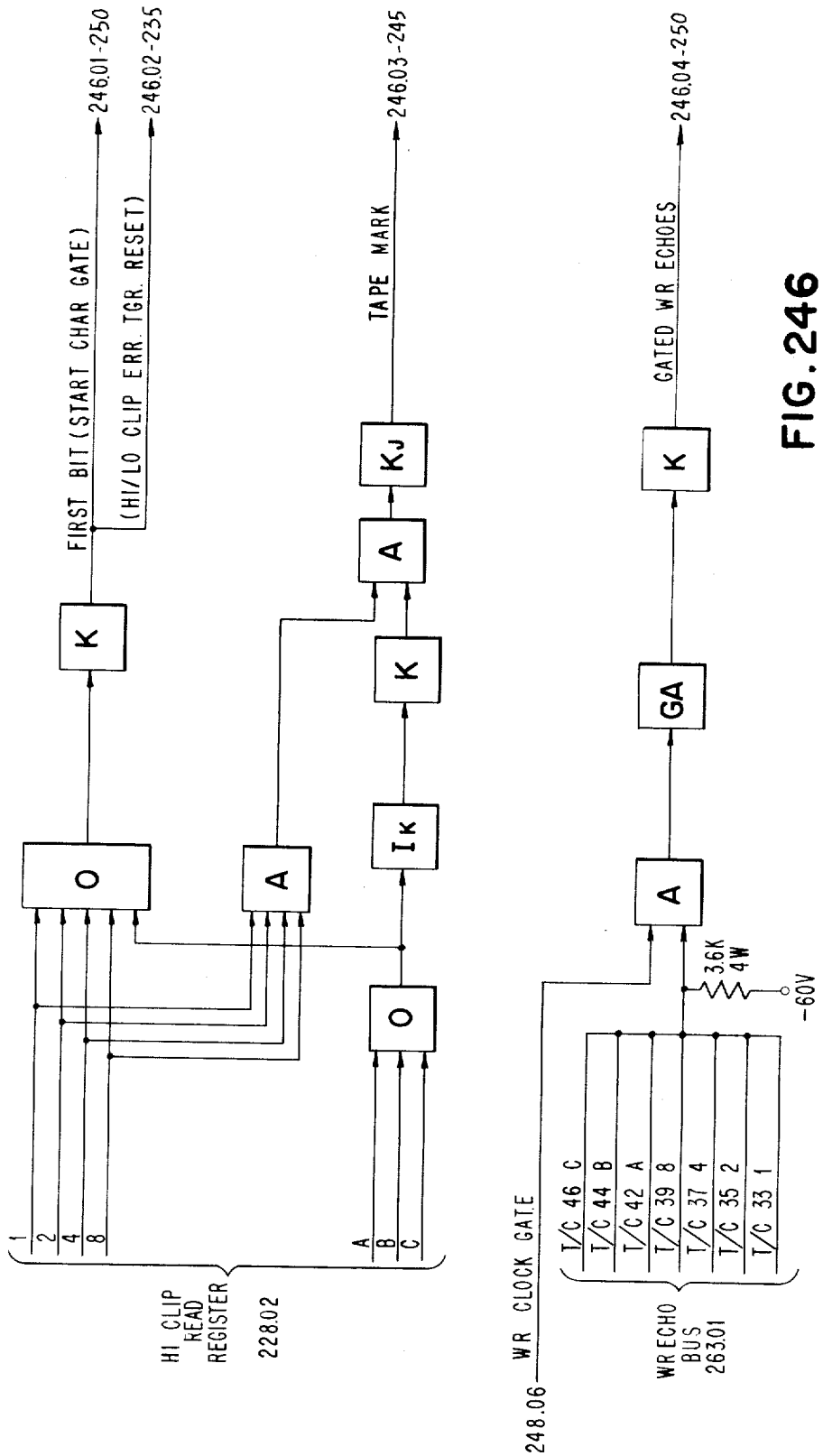


FIG. 246

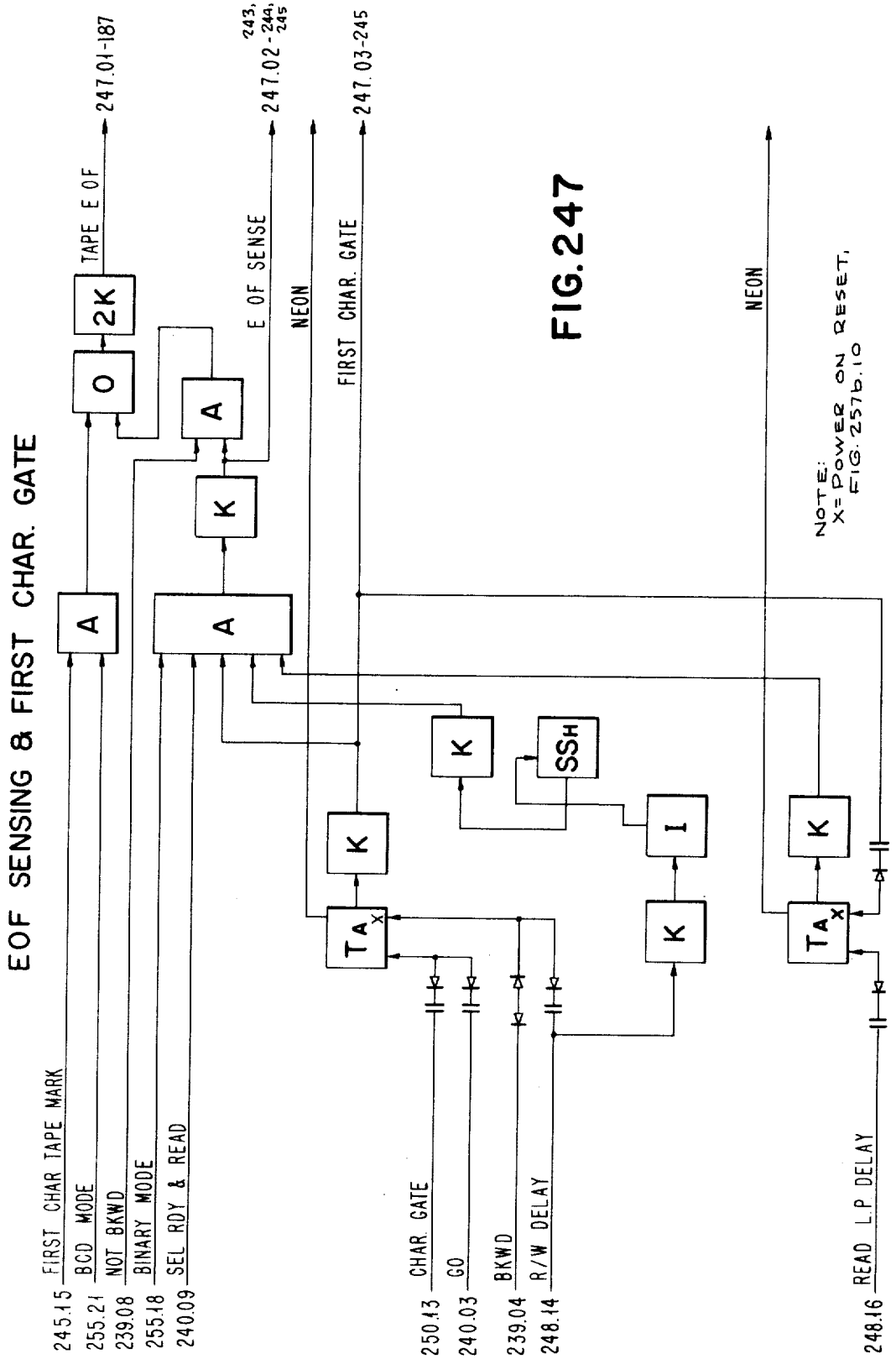

EOF SENSING & FIRST CHAR. GATE
245.15 FIRST CHAR TAPE MARK
255.21 BCD MODE
239.08 NOT BKWD
255.18 BINARY MODE
240.09 SEL RDY & READ
250.13 CHAR. GATE
240.03 GO
239.04 BKWD
248.14 R/W DELAY
248.16 READ L.P DELAY
A
O
2K
TAPE E OF
247.01-187
A
K
E OF SENSE
243, 244, 245
247.02-
NEON
FIRST CHAR. GATE
247.03-245
K
SSH
I
K
TAX
K
TAX
K
NEON
NOTE:
X=POWER ON RESET,
FIG. 257b.10

FIG.247

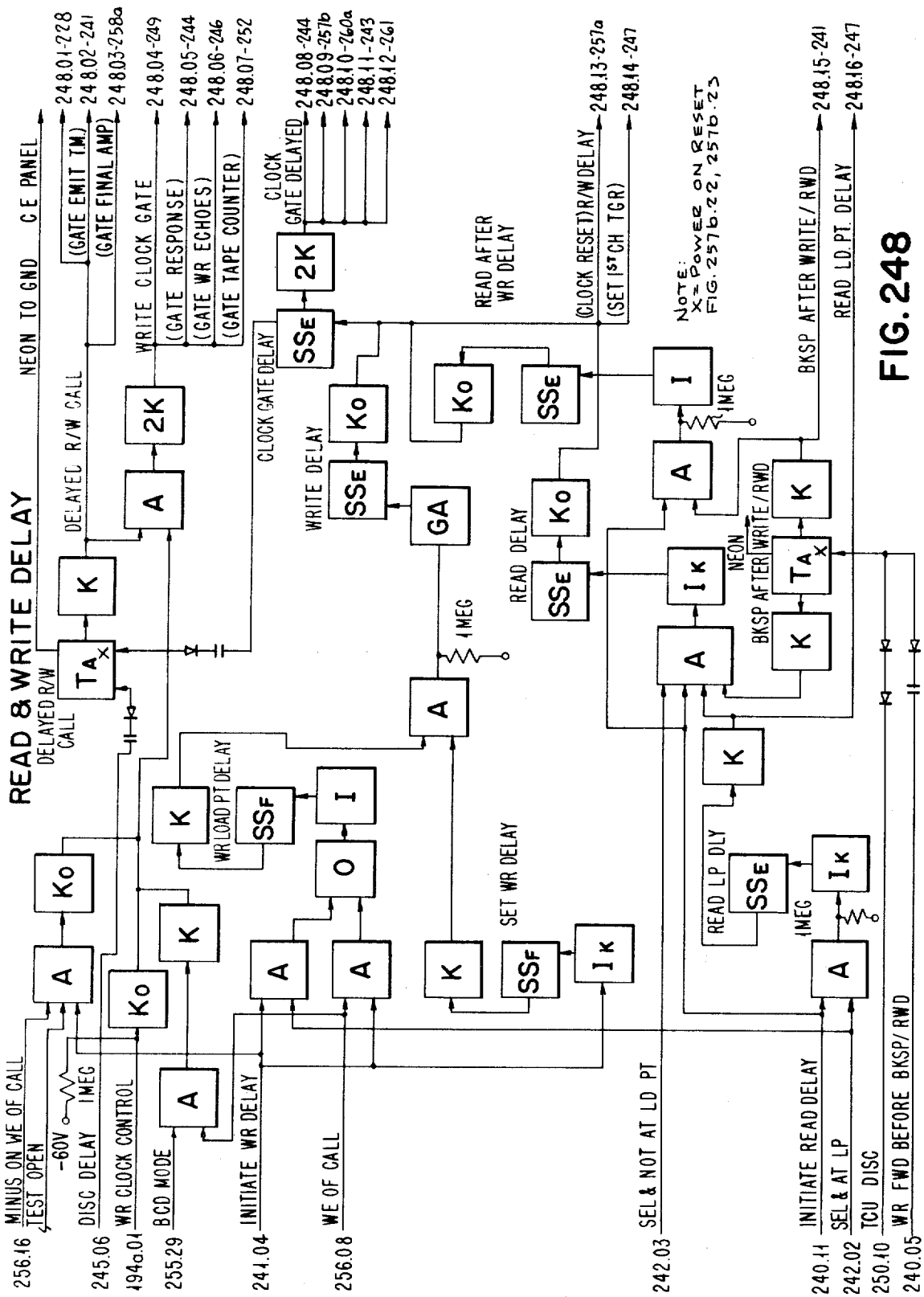

READ & WRITE DELAY
NEON TO GND C E PANEL
DELAYED R/W CALL
WRITE CLOCK GATE
CLOCK GATE DELAY
CLOCK GATE DELAYED
(GATE EMIT TM.)
(GATE FINAL AMP)
(GATE RESPONSE)
(GATE WR ECHOES)
(GATE TAPE COUNTER)
248.01-228
248.02-241
248.03-258a
248.04-249
248.05-244
248.06-246
248.07-252
248.08-244
248.09-257b
248.10-260a
248.11-243
248.12-261
248.13-257a
248.14-247
248.15-241
248.16-247
WRITE DELAY
READ AFTER WR DELAY
READ DELAY
SET WR DELAY
WR LOAD PT DELAY
INITIATE WR DELAY
(CLOCK RESET) R/W DELAY
(SET 1ST CH TGR)
BKSP AFTER WRITE/RWD
READ LD. PT. DELAY
READ LP DLY
BKSP AFTER WRITE/RWD
NEON
1MEG
-60V
TEST OPEN
MINUS ON WE OF CALL
DISC DELAY 1MEG
WR CLOCK CONTROL
BCD MODE
INITIATE WR DELAY
WE OF CALL
SEL & NOT AT LD PT
INITIATE READ DELAY
SEL & AT LP
TCU DISC
WR FWD BEFORE BKSP/RWD
256.16
245.06
194a.01
255.29
241.04
256.08
242.03
240.11
242.02
250.10
240.05
Note:
X=Power on Reset
FIG. 257b.22, 257b.23

FIG. 248

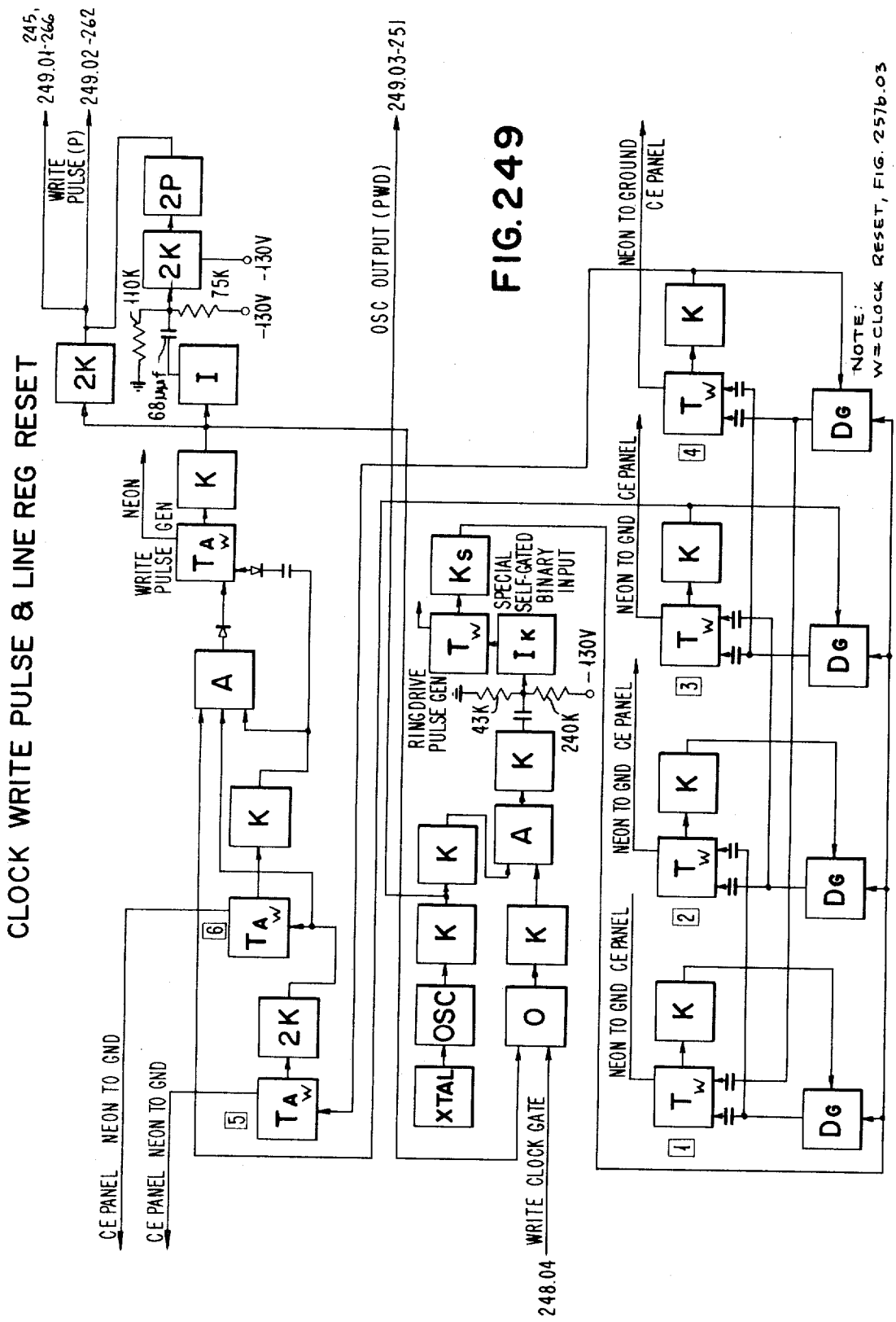

CLOCK WRITE PULSE & LINE REG RESET
249.01-245, 266
249.02-262
249.03-251
OSC OUTPUT (PWD)
WRITE PULSE (P)
2K
2P
110K
68μμf
75K
-130V
-430V
I
K
A
TA w
TW
DG
OSC
XTAL
O
Ks
Ik
RING DRIVE PULSE GEN
43K
240K
SPECIAL SELF-GATED BINARY INPUT
NEON GEN
WRITE PULSE
NEON TO GROUND CE PANEL
NEON TO GND CE PANEL
CE PANEL NEON TO GND
WRITE CLOCK GATE
248.04
NOTE: W=CLOCK RESET, FIG. 257b.03

FIG. 249

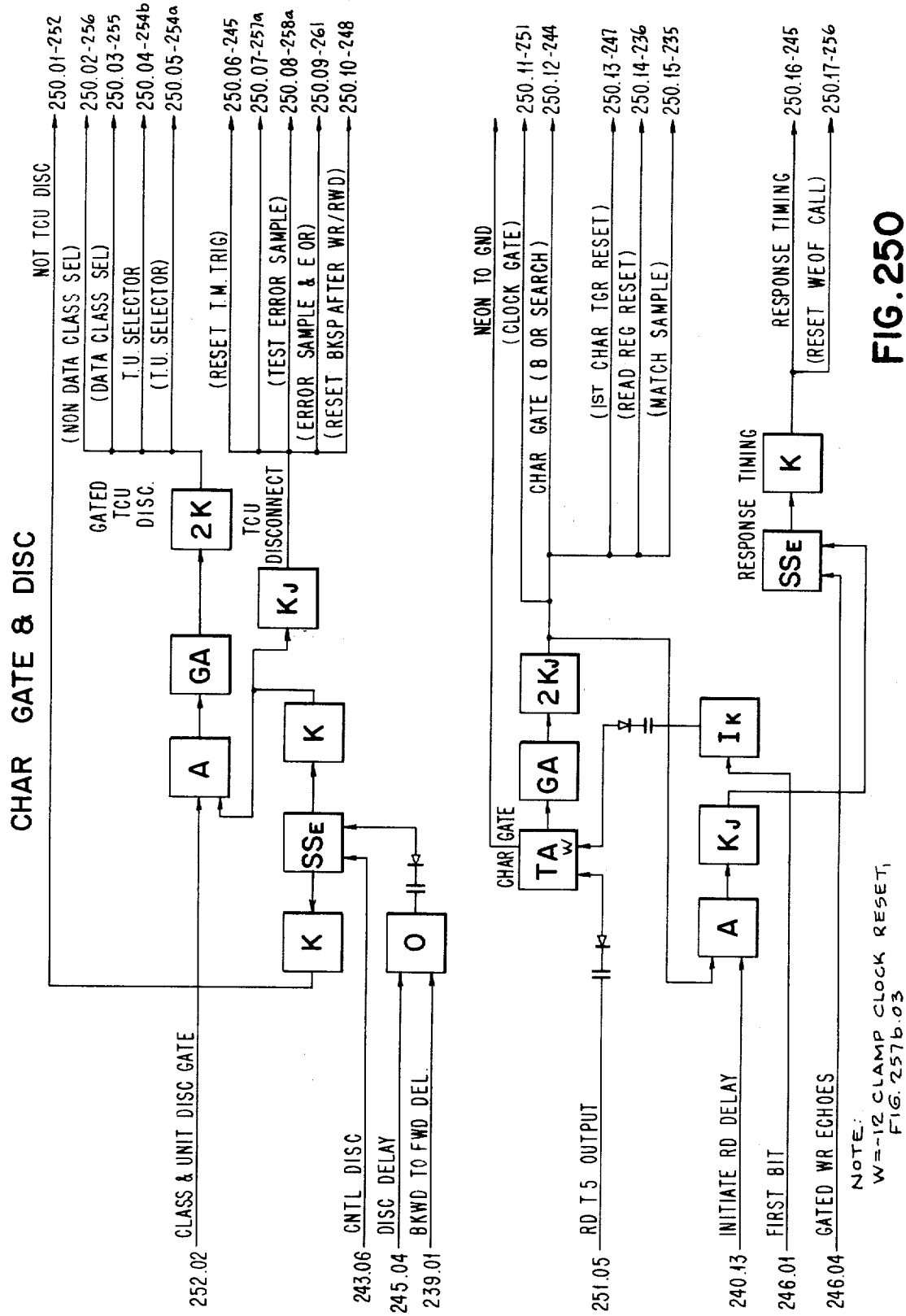

CHAR GATE & DISC
NOT TCU DISC
250.01-252
(NON DATA CLASS SEL)
250.02-256
(DATA CLASS SEL)
250.03-255
T.U. SELECTOR
250.04-254b
(T.U. SELECTOR)
250.05-254a
(RESET T.M. TRIG)
250.06-245
(TEST ERROR SAMPLE)
250.07-257a
(ERROR SAMPLE & E OR)
250.08-258a
(RESET BKSP AFTER WR/RWD)
250.09-261
250.10-248
GATED TCU DISC.
TCU DISCONNECT
2K
A
GA
KJ
K
SSE
K
O
CLASS & UNIT DISC GATE
252.02
CNTL DISC
243.06
DISC DELAY
245.04
BKWD TO FWD DEL.
239.01
NEON TO GND
(CLOCK GATE)
250.11-251
CHAR GATE (B OR SEARCH)
250.12-244
(1ST CHAR TGR RESET)
250.13-247
(READ REG RESET)
250.14-236
(MATCH SAMPLE)
250.15-235
CHAR GATE
TA W
GA
2KJ
IK
A
KJ
RESPONSE TIMING
SSE
K
RESPONSE TIMING
250.16-245
(RESET WEOF CALL)
250.17-256
RD T 5 OUTPUT
251.05
INITIATE RD DELAY
240.13
FIRST BIT
246.01
GATED WR ECHOES
246.04
NOTE:
W=-12 CLAMP CLOCK RESET,
FIG. 257b.03

FIG. 250

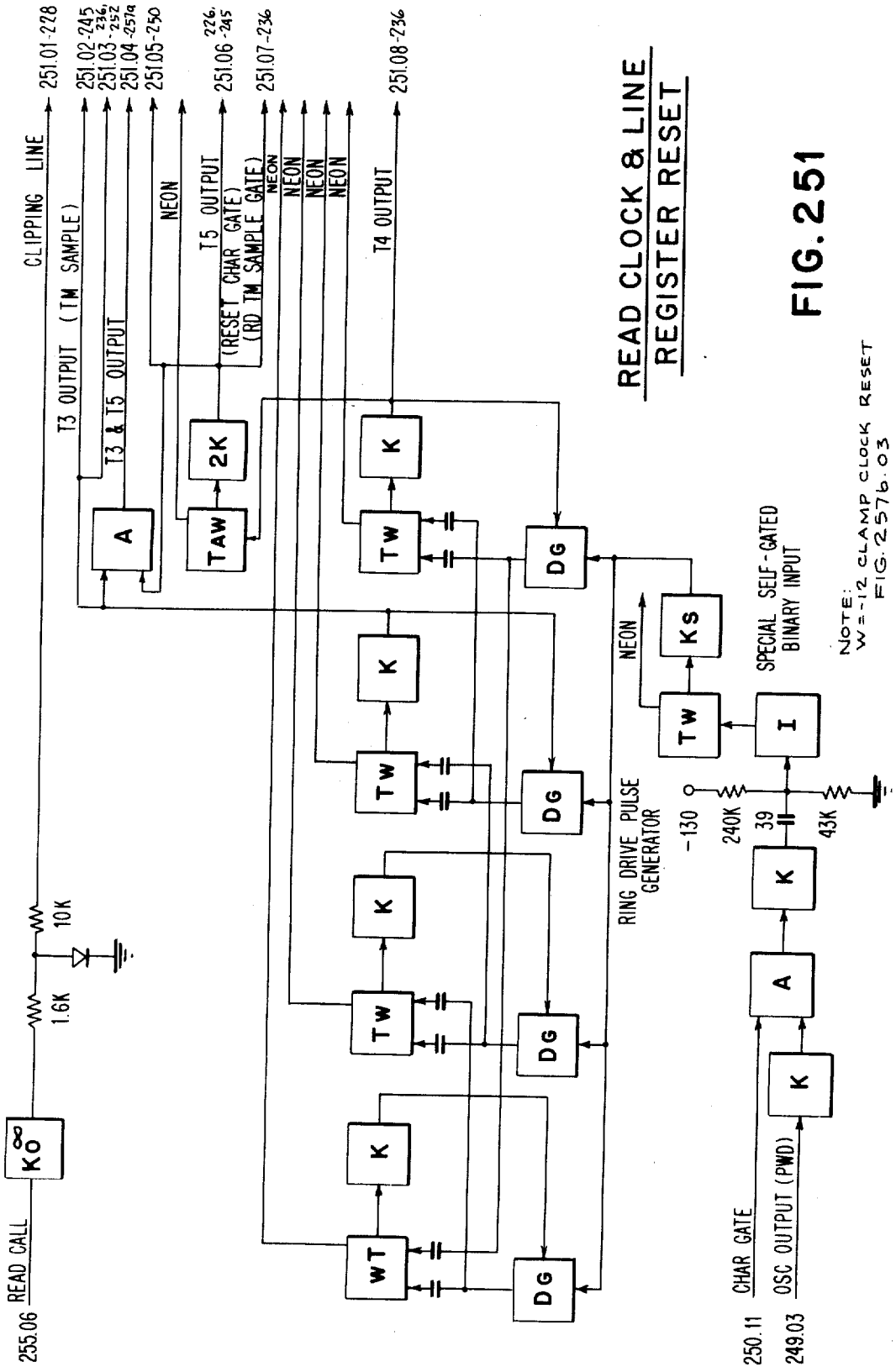
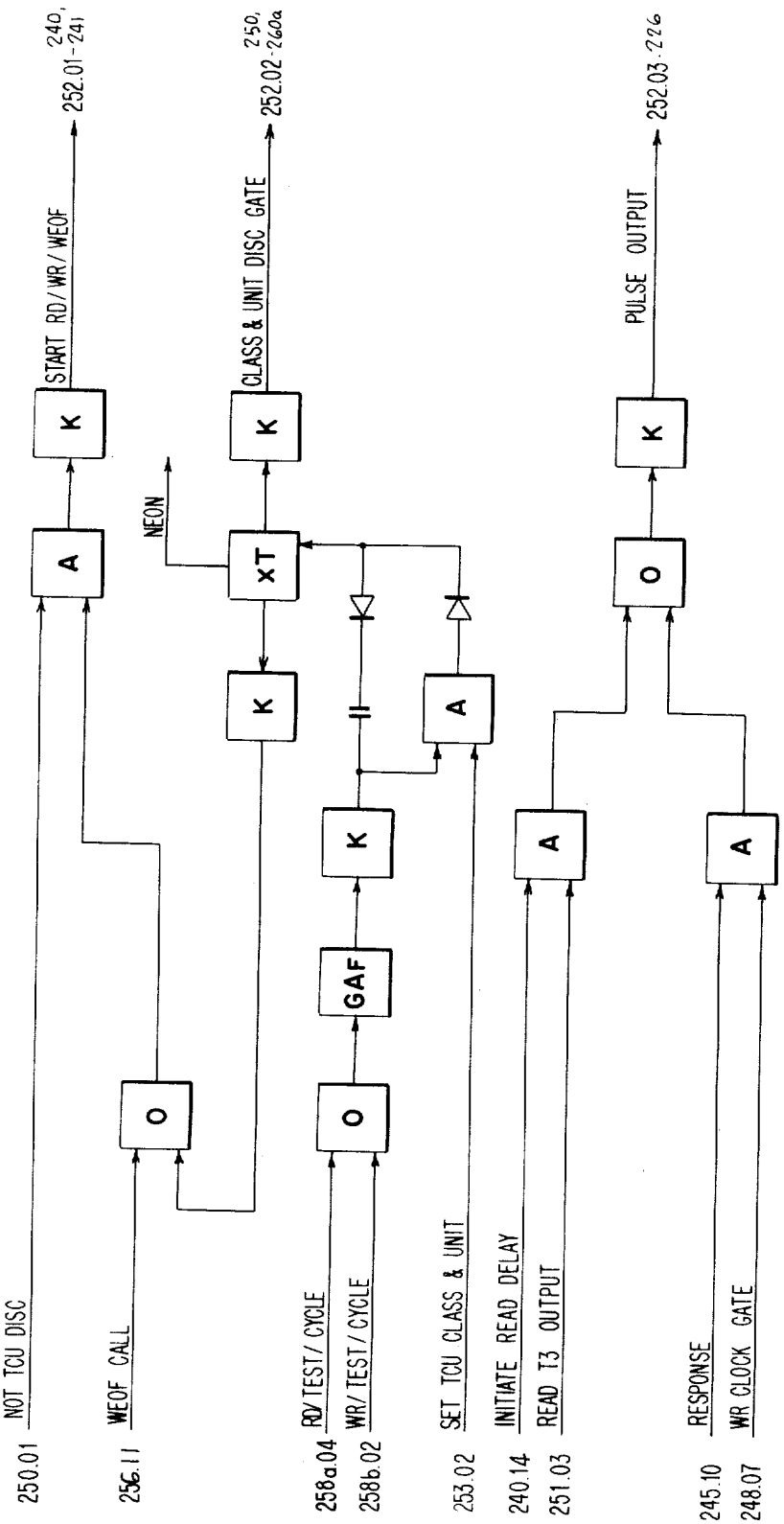
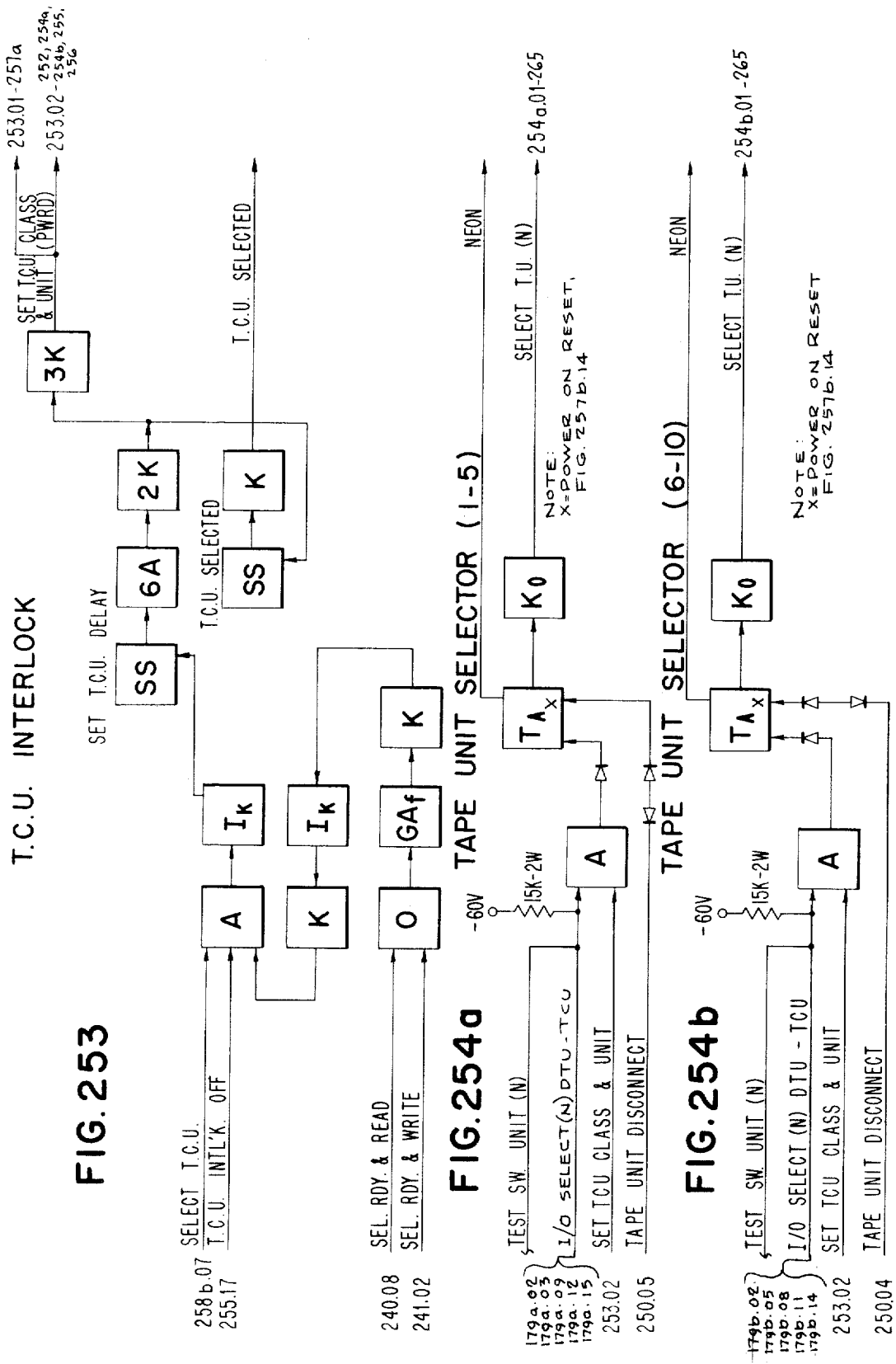

READ CLOCK & LINE REGISTER RESET
CLIPPING LINE
251.01-228
T3 OUTPUT (TM SAMPLE)
251.02-245
T3 & T5 OUTPUT
251.03-234, -252
NEON
251.04-257a
251.05-250
T5 OUTPUT
(RESET CHAR GATE)
(RD TM SAMPLE GATE)
251.06-226, -245
NEON
251.07-236
NEON
NEON
NEON
T4 OUTPUT
251.08-236
READ CALL
255.06
10K
1.6K
RING DRIVE PULSE GENERATOR
-130
240K
39
43K
NEON
SPECIAL SELF-GATED BINARY INPUT
CHAR GATE
250.11
OSC OUTPUT (PWD)
249.03
NOTE:
W=-12 CLAMP CLOCK RESET
FIG. 257b.03

FIG. 251

FIG. 252


CLASS & UNIT DISC. GATE & START RD/WR/WEOF
250.01 NOT TCU DISC
256.11 WEOF CALL
258a.04 RD/TEST/CYCLE
258b.02 WR/TEST/CYCLE
253.02 SET TCU CLASS & UNIT
240.14 INITIATE READ DELAY
251.03 READ T3 OUTPUT
245.10 RESPONSE
248.07 WR CLOCK GATE
A
O
K
GAF
XT
NEON
START RD/WR/WEOF
252.01-240,241
CLASS & UNIT DISC GATE
252.02-250,260a
PULSE OUTPUT
252.03-226


T.C.U. INTERLOCK
SET T.C.U. DELAY
SELECT T.C.U.
T.C.U. INTL'K. OFF
258b.07
255.17
SEL. RDY. & READ
SEL. RDY. & WRITE
240.08
241.02
T.C.U. SELECTED
SET T.C.U. CLASS & UNIT (PWRD)
253.01-257a
253.02-252, 254a, 254b, 255, 256
3K
2K
6A
SS
K
A
I_K
O
GA_f
FIG. 253
TAPE UNIT SELECTOR (1-5)
NEON
SELECT T.U. (N)
254a.01-265
NOTE: X=POWER ON RESET, FIG. 257b.14
K_0
TA_x
-60V
15K-2W
TEST SW. UNIT (N)
I/O SELECT(N) DTU-TCU
SET TCU CLASS & UNIT
TAPE UNIT DISCONNECT
179a.02
179a.05
179a.09
179a.12
179a.15
253.02
250.05
FIG. 254a
TAPE UNIT SELECTOR (6-10)
NEON
SELECT T.U. (N)
254b.01-265
NOTE: X=POWER ON RESET FIG. 257b.14
K_0
TA_x
-60V
15K-2W
TEST SW. UNIT (N)
I/O SELECT (N) DTU - TCU
SET TCU CLASS & UNIT
TAPE UNIT DISCONNECT
179b.02
179b.05
179b.08
179b.11
179b.14
253.02
250.04
FIG. 254b

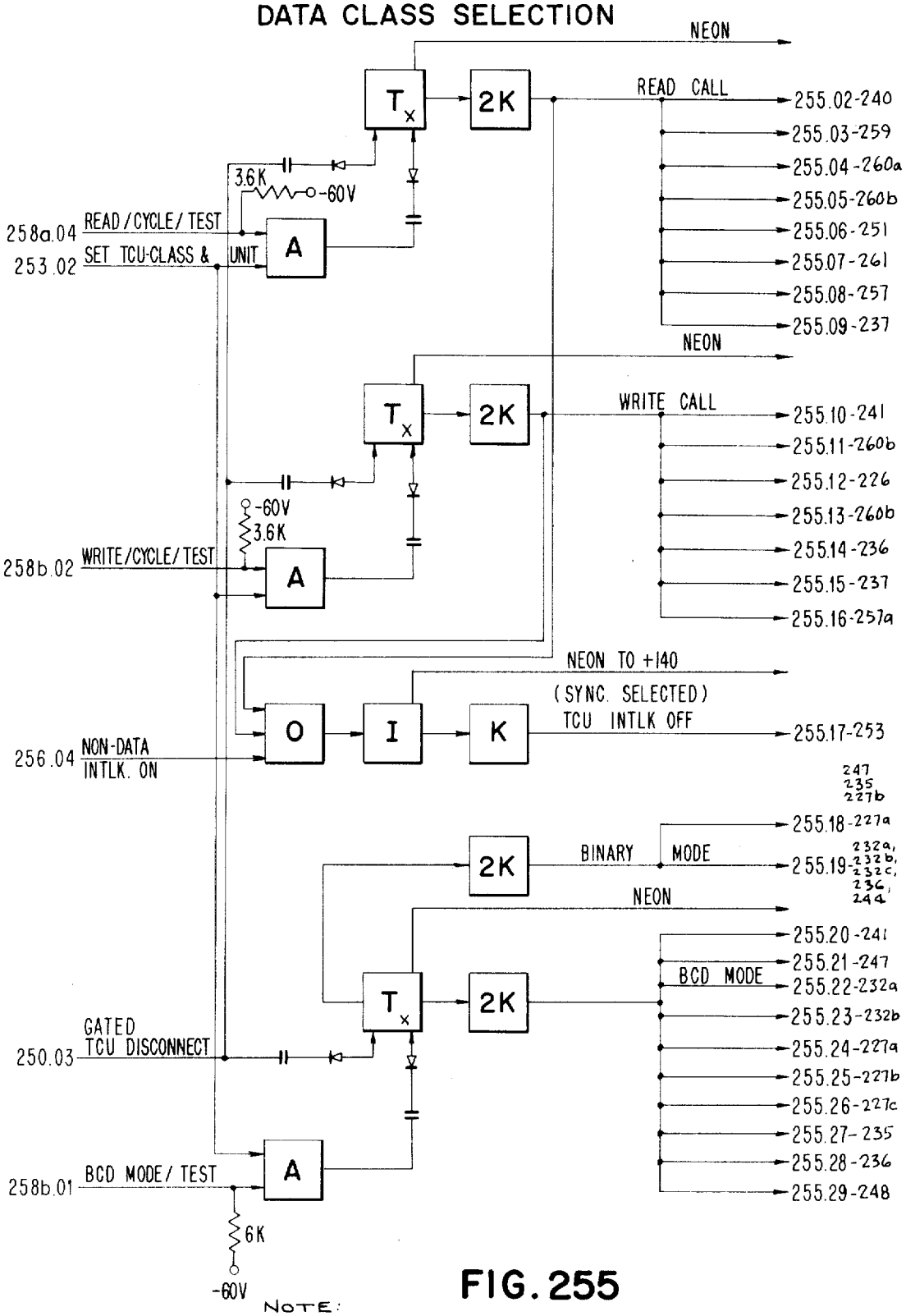
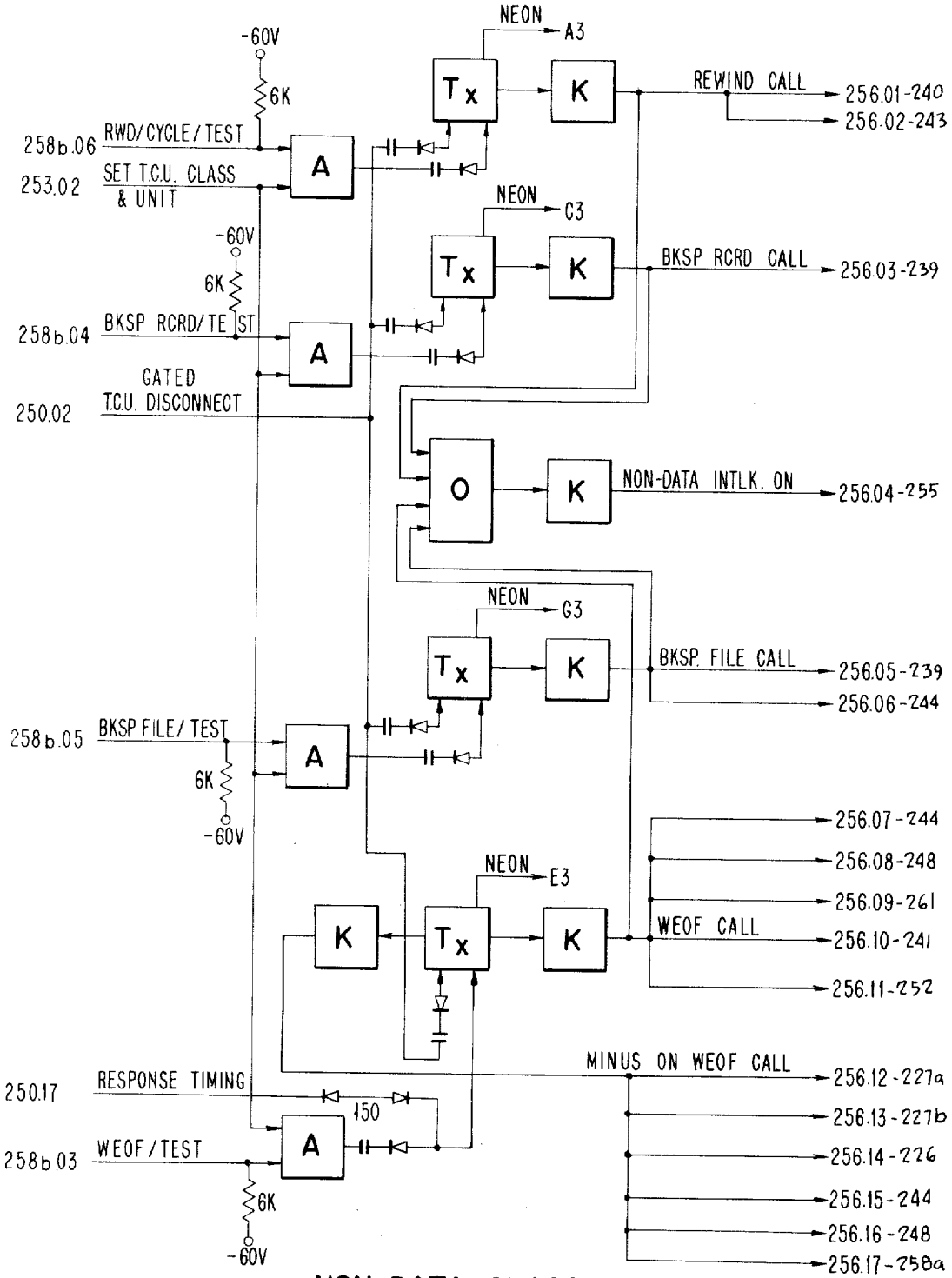


FIG. 255

NOTE:
X = POWER ON RESET
FIG. 257b.15, 257b.16, 257b.17



NON-DATA CLASS SELECTION

NOTE:
X = POWER ON RESET
FIG. 257b.07, 257b.18, 257b.19, 257b.20

FIG. 256

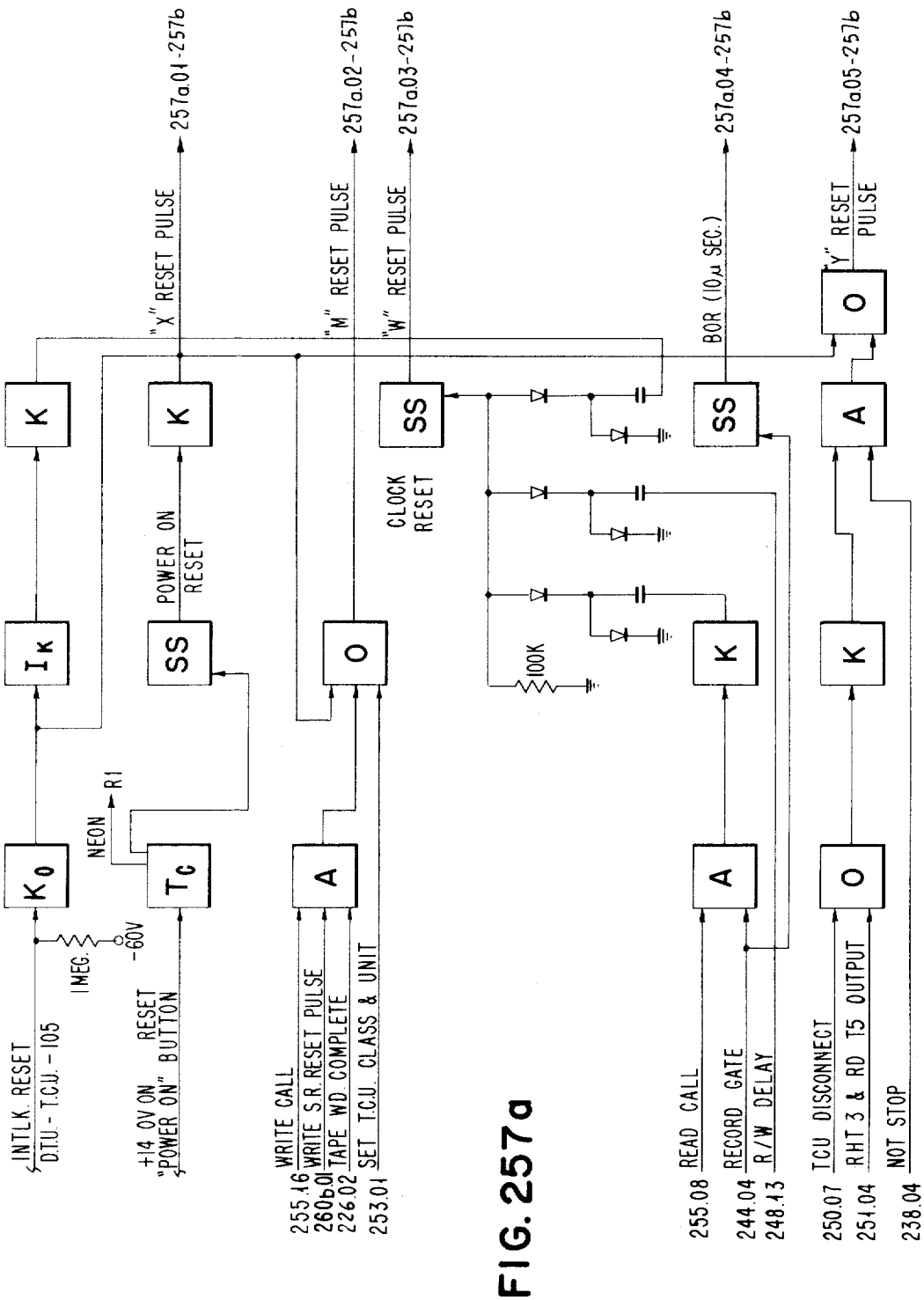

-12V CLAMP RESET PULSE GENERATORS
INTLK. RESET
D.T.U. - T.C.U. - 105
+14.0V ON
"POWER ON" BUTTON
RESET
1 MEG.
-60V
NEON
R1
WRITE CALL
255.16
WRITE S.R. RESET PULSE
260b01
TAPE WD. COMPLETE
226.02
SET T.C.U. CLASS & UNIT
253.01
POWER ON RESET
CLOCK RESET
100K
"X" RESET PULSE
257a01-257b
"M" RESET PULSE
257a02-257b
"W" RESET PULSE
257a03-257b
BOR (10μ SEC.)
257a04-257b
"Y" RESET PULSE
257a05-257b
READ CALL
255.08
RECORD GATE
244.04
R/W DELAY
248.13
TCU DISCONNECT
250.07
RHT 3 & RD T5 OUTPUT
251.04
NOT STOP
238.04
K0
Tc
IK
K
SS
O
A

FIG. 257a

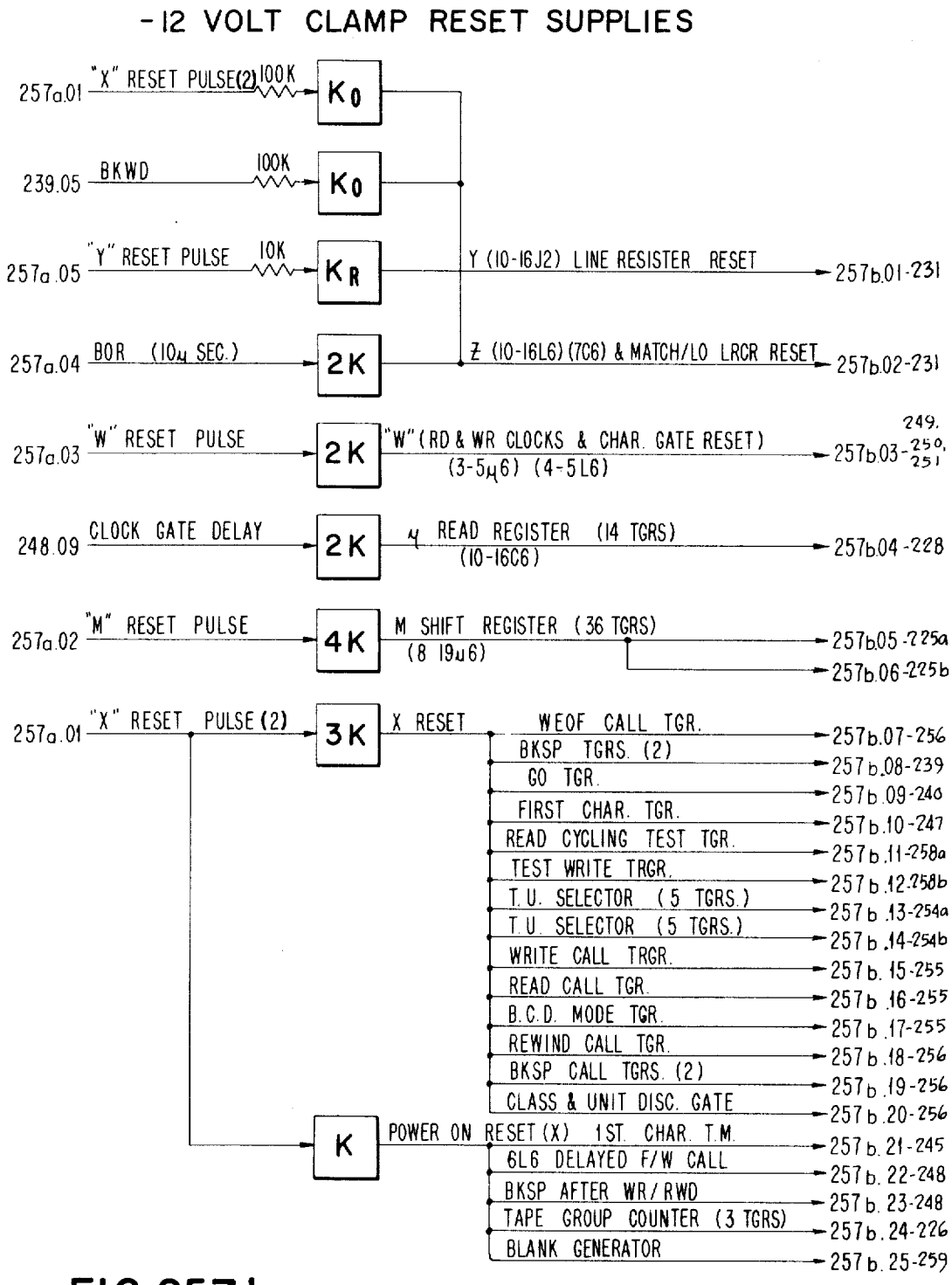
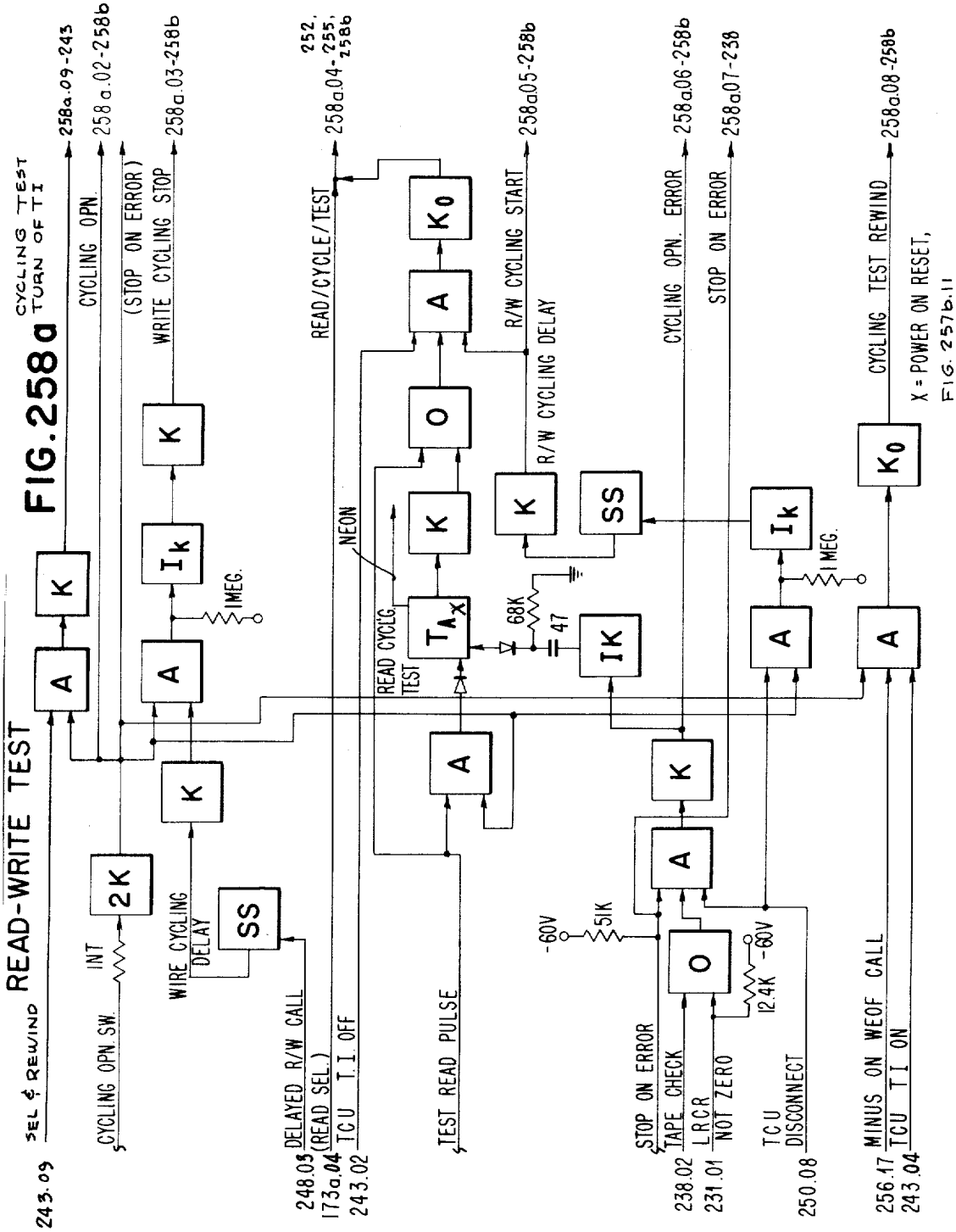
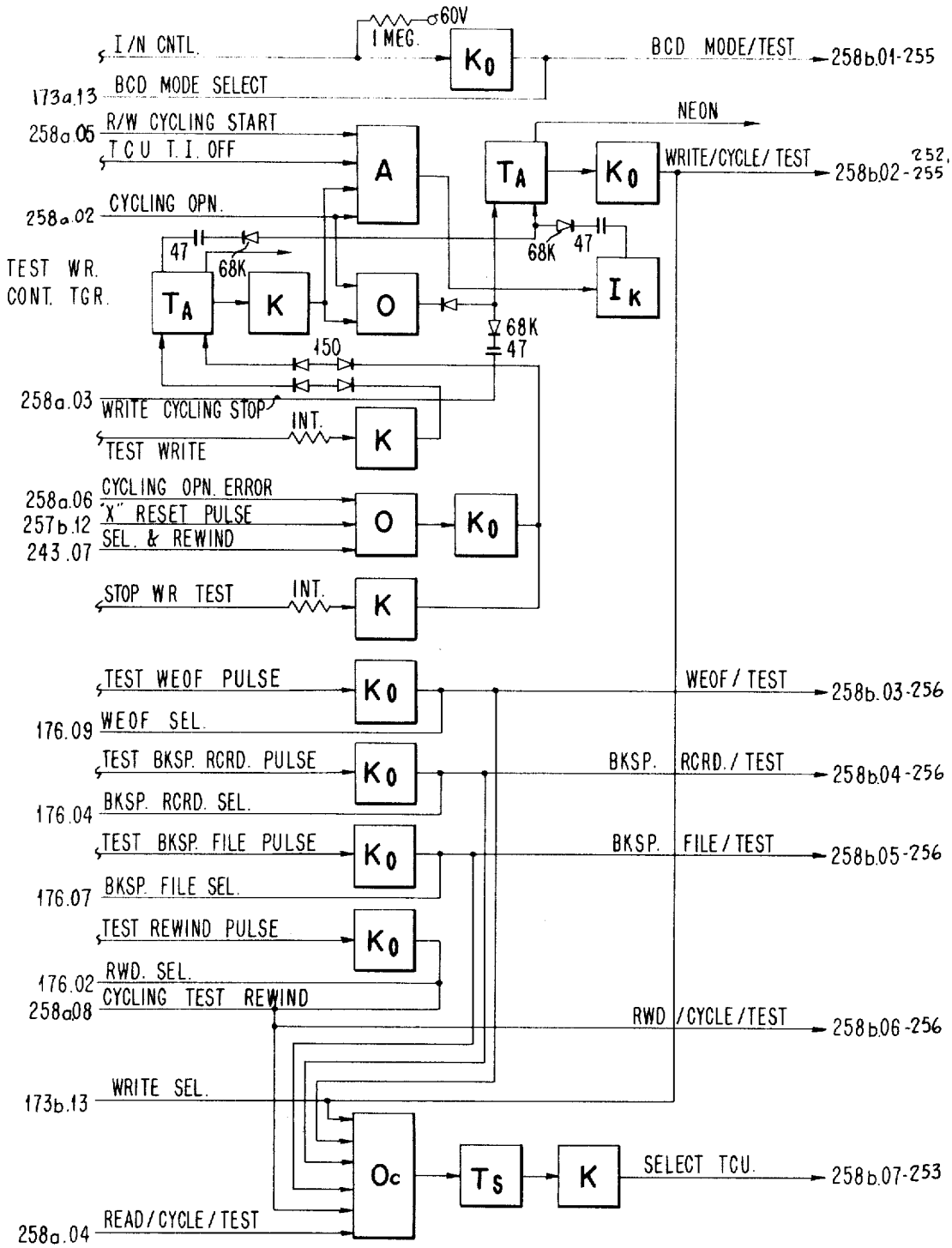

-12 VOLT CLAMP RESET SUPPLIES
257a.01
"X" RESET PULSE(2)
100K
K0
239.05
BKWD
100K
K0
257a.05
"Y" RESET PULSE
10K
KR
Y (10-16J2) LINE RESISTER RESET
257b.01-231
257a.04
BOR (10μ SEC.)
2K
Z (10-16L6) (7C6) & MATCH/LO LRCR RESET
257b.02-231
257a.03
"W" RESET PULSE
2K
"W" (RD & WR CLOCKS & CHAR. GATE RESET)
(3-5μ6) (4-5L6)
249.
257b.03-250, 251
248.09
CLOCK GATE DELAY
2K
4 READ REGISTER (14 TGRS)
(10-16C6)
257b.04-228
257a.02
"M" RESET PULSE
4K
M SHIFT REGISTER (36 TGRS)
(8 19μ6)
257b.05-225a
257b.06-225b
257a.01
"X" RESET PULSE (2)
3K
X RESET
WEOF CALL TGR.
257b.07-256
BKSP TGRS. (2)
257b.08-239
GO TGR.
257b.09-240
FIRST CHAR. TGR.
257b.10-247
READ CYCLING TEST TGR.
257b.11-258a
TEST WRITE TRGR.
257b.12-258b
T.U. SELECTOR (5 TGRS.)
257b.13-254a
T.U. SELECTOR (5 TGRS.)
257b.14-254b
WRITE CALL TRGR.
257b.15-255
READ CALL TGR.
257b.16-255
B.C.D. MODE TGR.
257b.17-255
REWIND CALL TGR.
257b.18-256
BKSP CALL TGRS. (2)
257b.19-256
CLASS & UNIT DISC. GATE
257b.20-256
K
POWER ON RESET (X) 1ST. CHAR. T.M.
257b.21-245
6L6 DELAYED F/W CALL
257b.22-248
BKSP AFTER WR/RWD
257b.23-248
TAPE GROUP COUNTER (3 TGRS)
257b.24-226
BLANK GENERATOR
257b.25-259

FIG. 257b


FIG. 258a
CYCLING TEST TURN OF TI
READ-WRITE TEST
SEL & REWIND
243.09
CYCLING OPN. SW.
INT
2K
WIRE CYCLING DELAY
SS
DELAYED R/W CALL
248.03
(READ SEL.)
173a.04
TCU T.I. OFF
243.02
A
K
IMEG.
CYCLING OPN
258a.09-243
(STOP ON ERROR)
WRITE CYCLING STOP
258a.02-258b
258a.03-258b
READ CYCLG. TEST
NEON
TEST READ PULSE
68K
47
IK
READ/CYCLE/TEST
252.
258a.04-255, 258b
O
R/W CYCLING START
R/W CYCLING DELAY
258a.05-258b
-60V
51K
STOP ON ERROR
TAPE CHECK
238.02
L.R.C.R.
231.01
NOT ZERO
12.4K
-60V
T.C.U. DISCONNECT
250.08
CYCLING OPN. ERROR
258a.06-258b
STOP ON ERROR
258a.07-238
MINUS ON WEOF CALL
256.17
TCU T.I. ON
243.04
CYCLING TEST REWIND
258a.08-258b
X = POWER ON RESET,
FIG. 257b.11



READ / WRITE TEST

FIG. 258 b

BLANK GENERATOR

FIG. 259

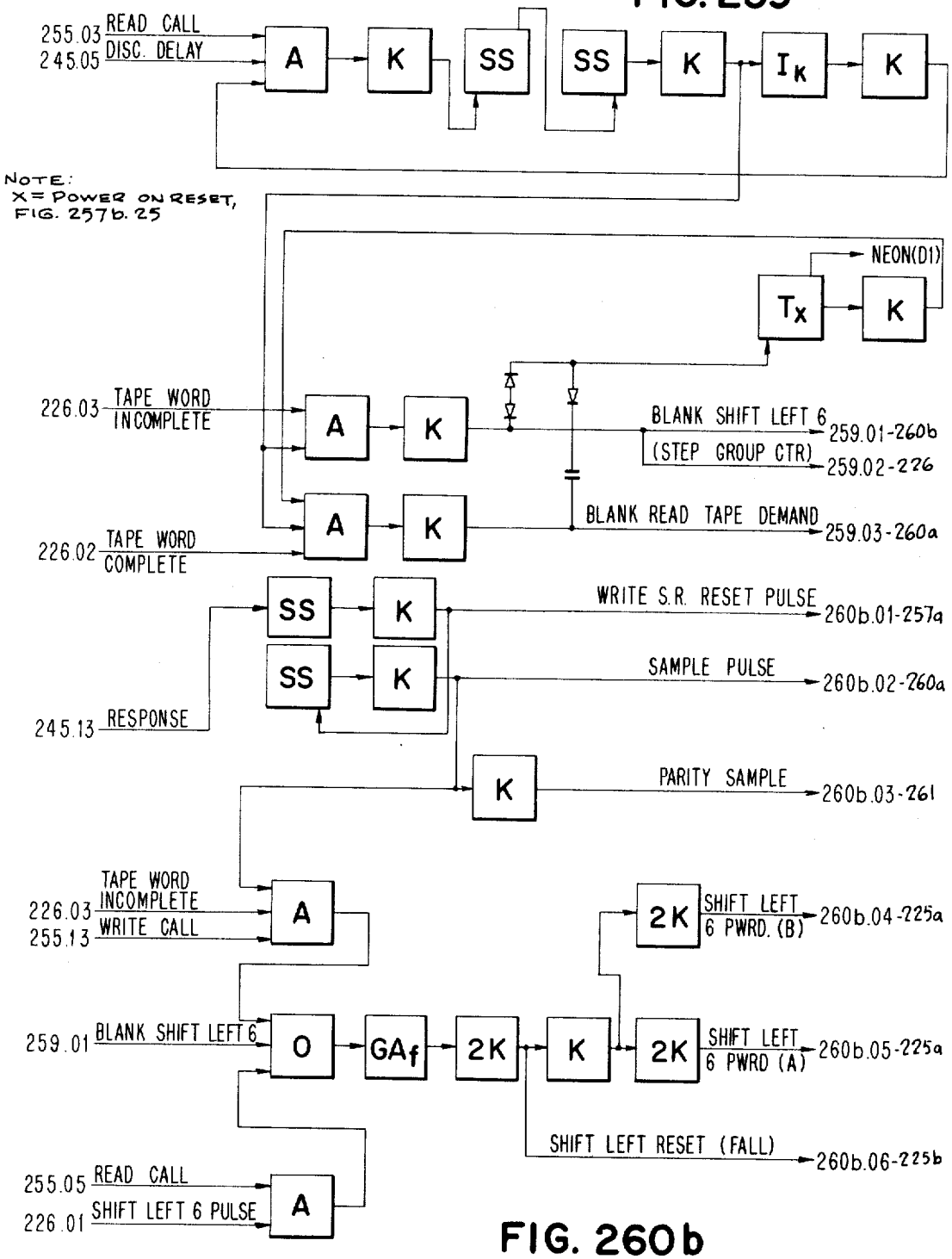


FIG. 260b

SHIFT REGISTER CONTROLS 2

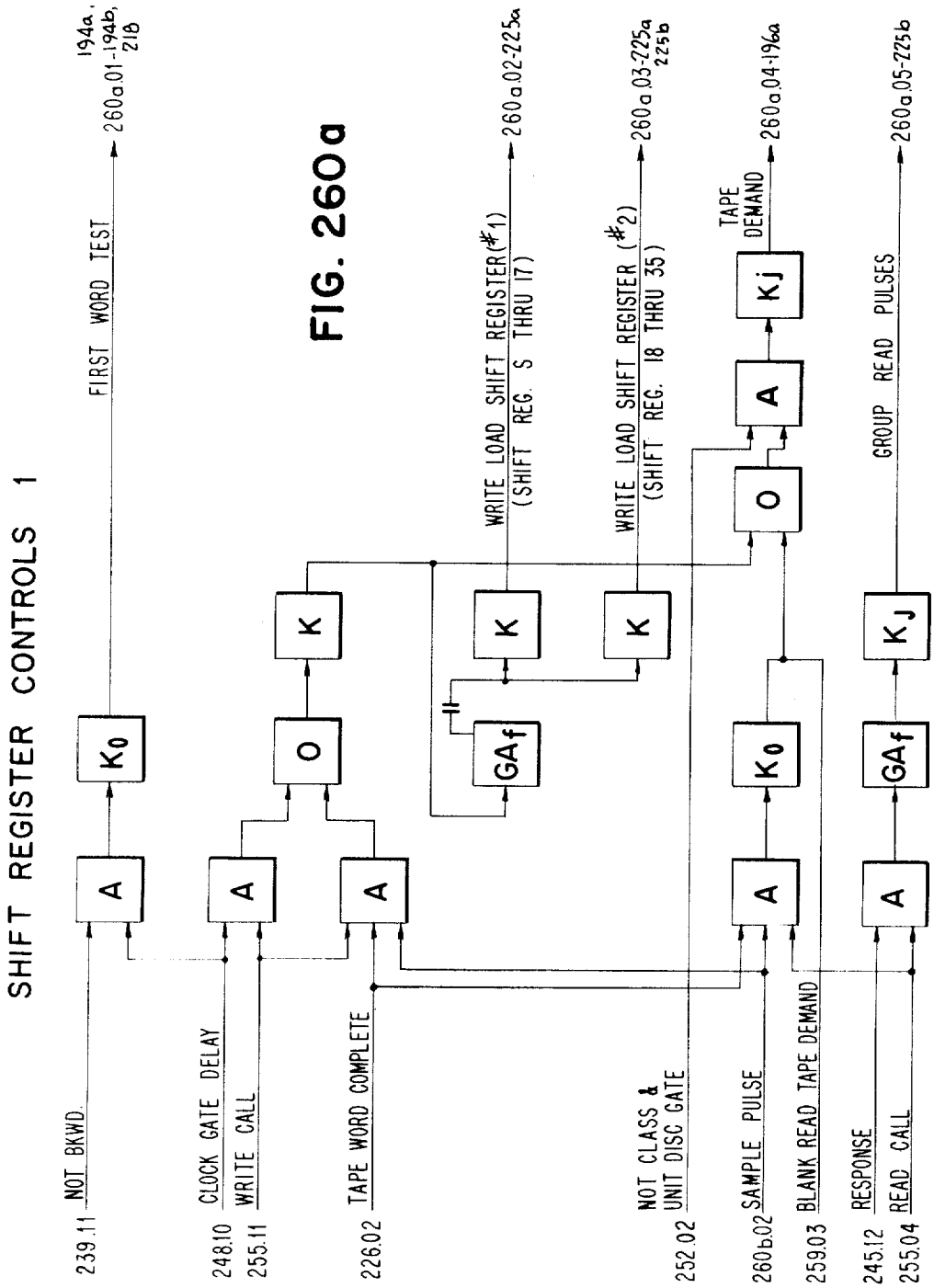

SHIFT REGISTER CONTROLS 1
239.11 NOT BKWD.
248.10 CLOCK GATE DELAY
255.11 WRITE CALL
226.02 TAPE WORD COMPLETE
252.02 NOT CLASS & UNIT DISC GATE
260b.02 SAMPLE PULSE
259.03 BLANK READ TAPE DEMAND
245.12 RESPONSE
255.04 READ CALL
A
K0
O
K
GAf
KJ
Kj
FIRST WORD TEST
194a, 260a.01-194b, 218
WRITE LOAD SHIFT REGISTER (#1) (SHIFT REG. 5 THRU 17)
260a.02-225a
WRITE LOAD SHIFT REGISTER (#2) (SHIFT REG. 18 THRU 35)
260a.03-225a 225b
TAPE DEMAND
260a.04-196a
GROUP READ PULSES
260a.05-225b

FIG. 260a

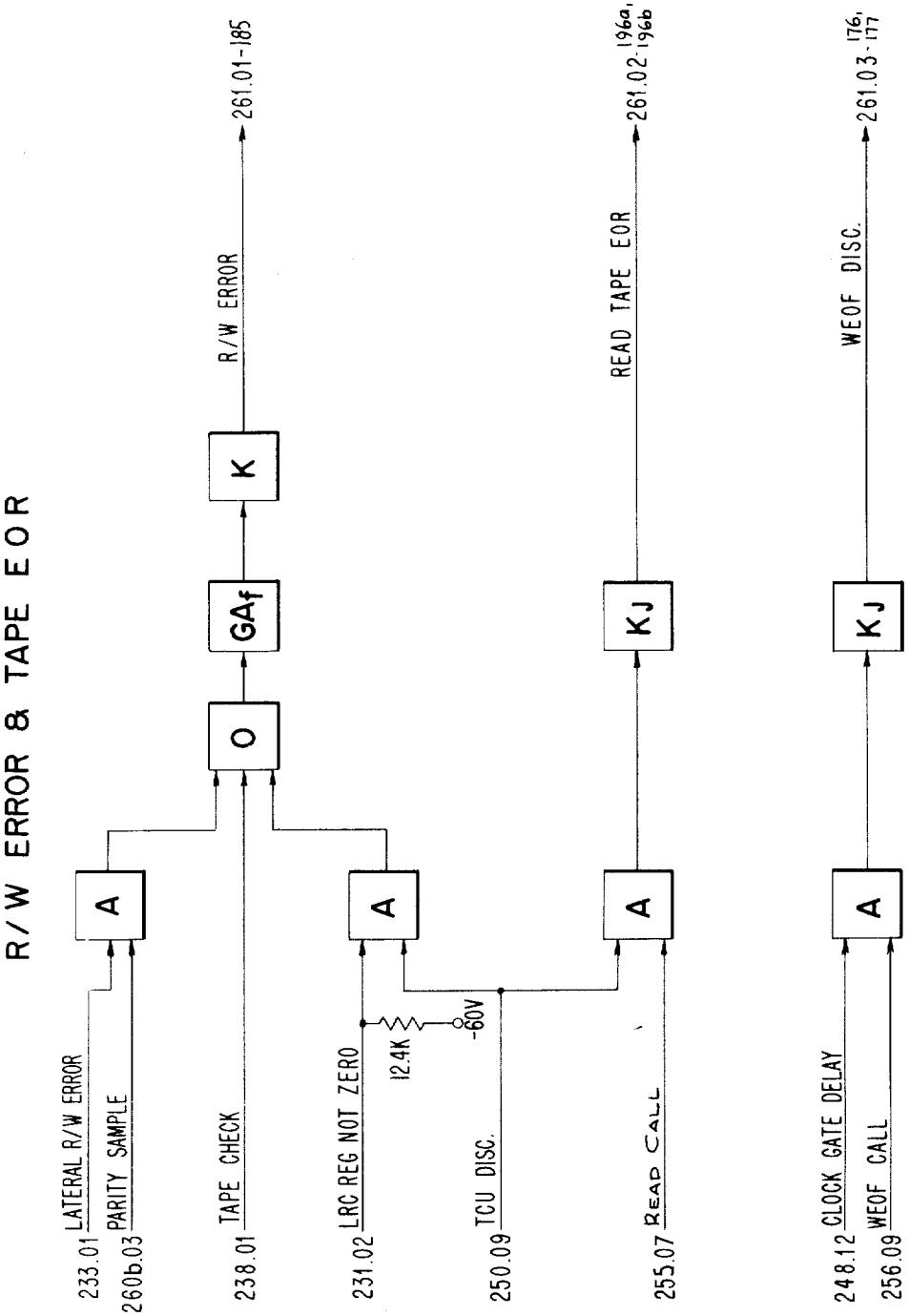
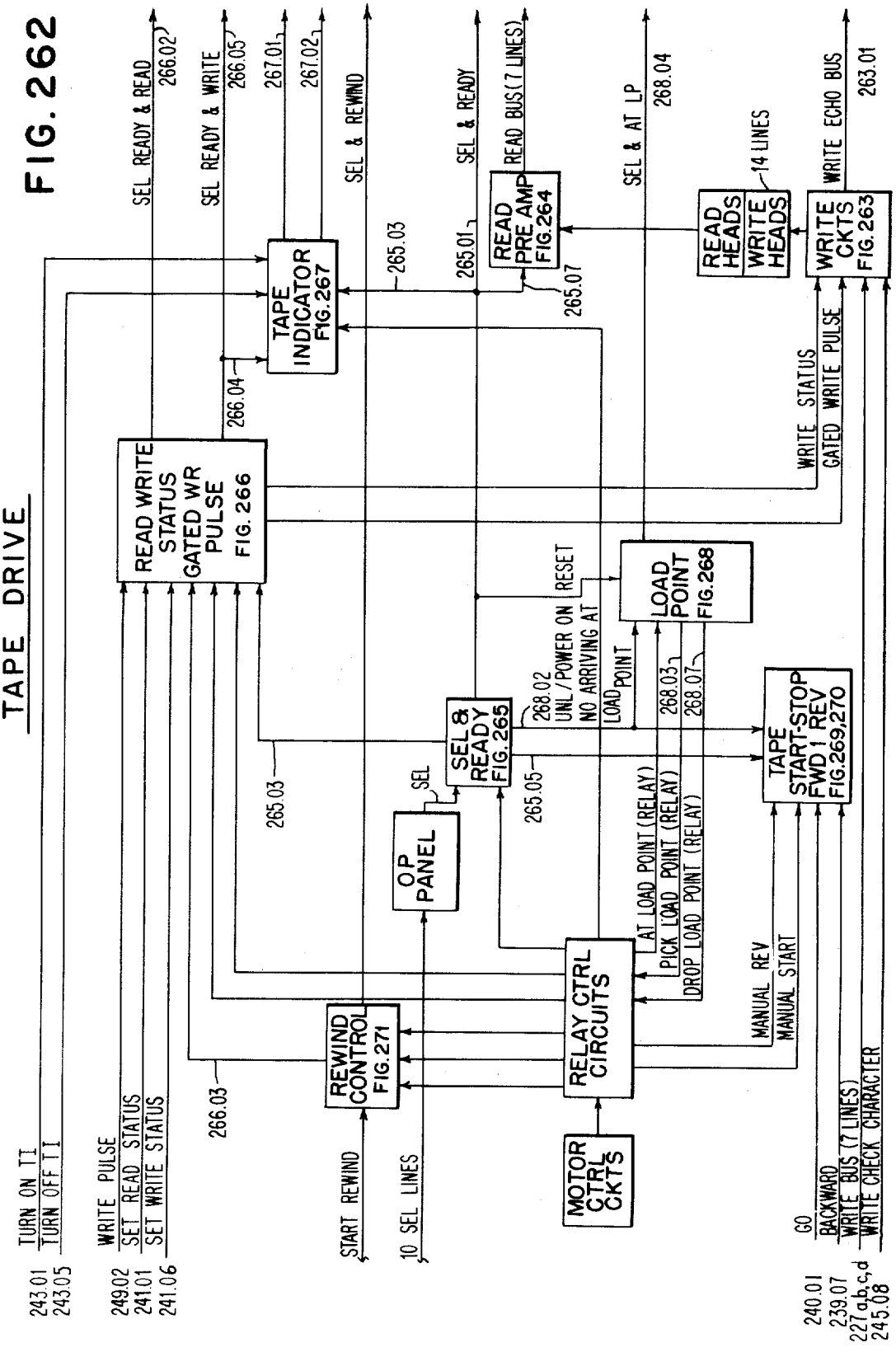
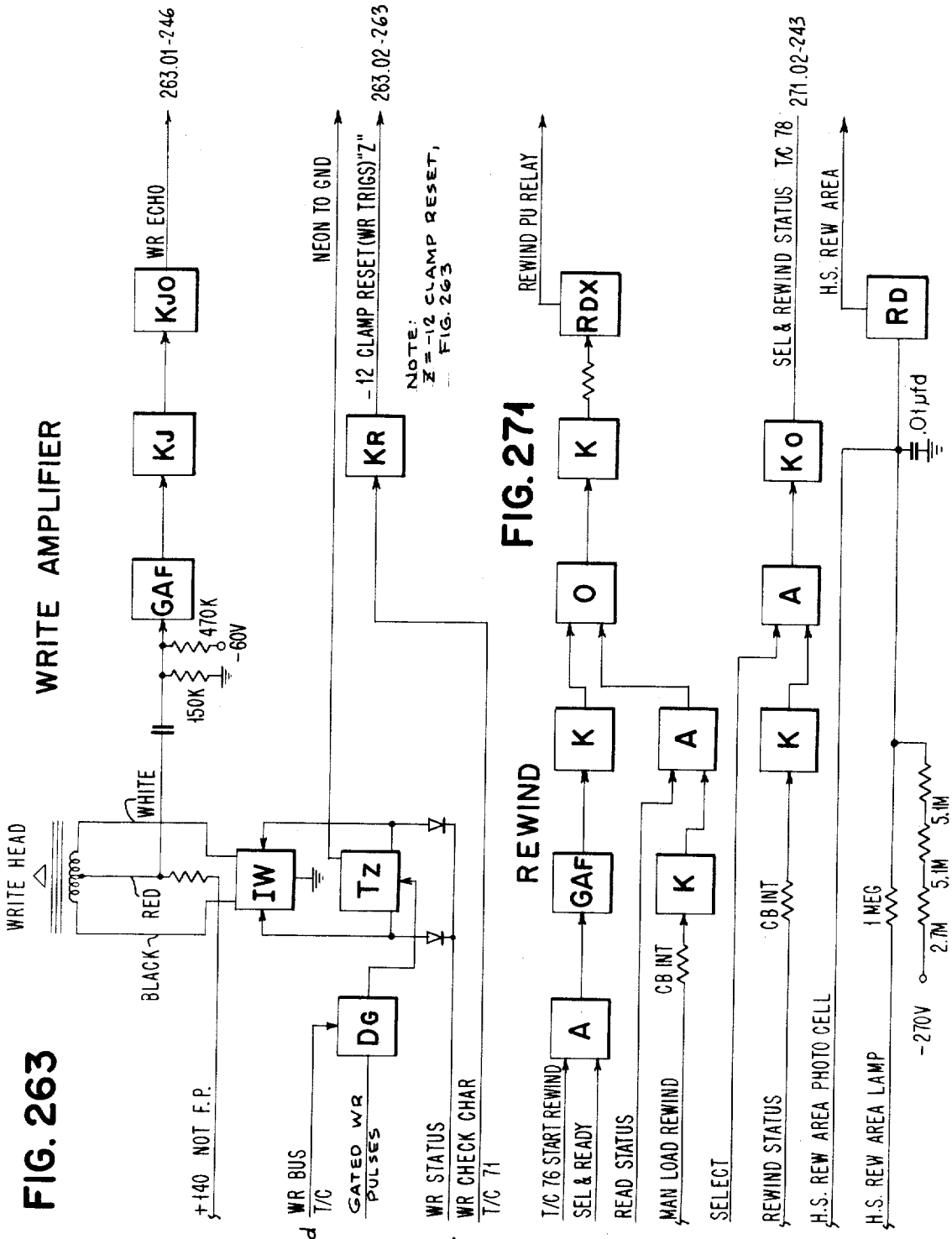
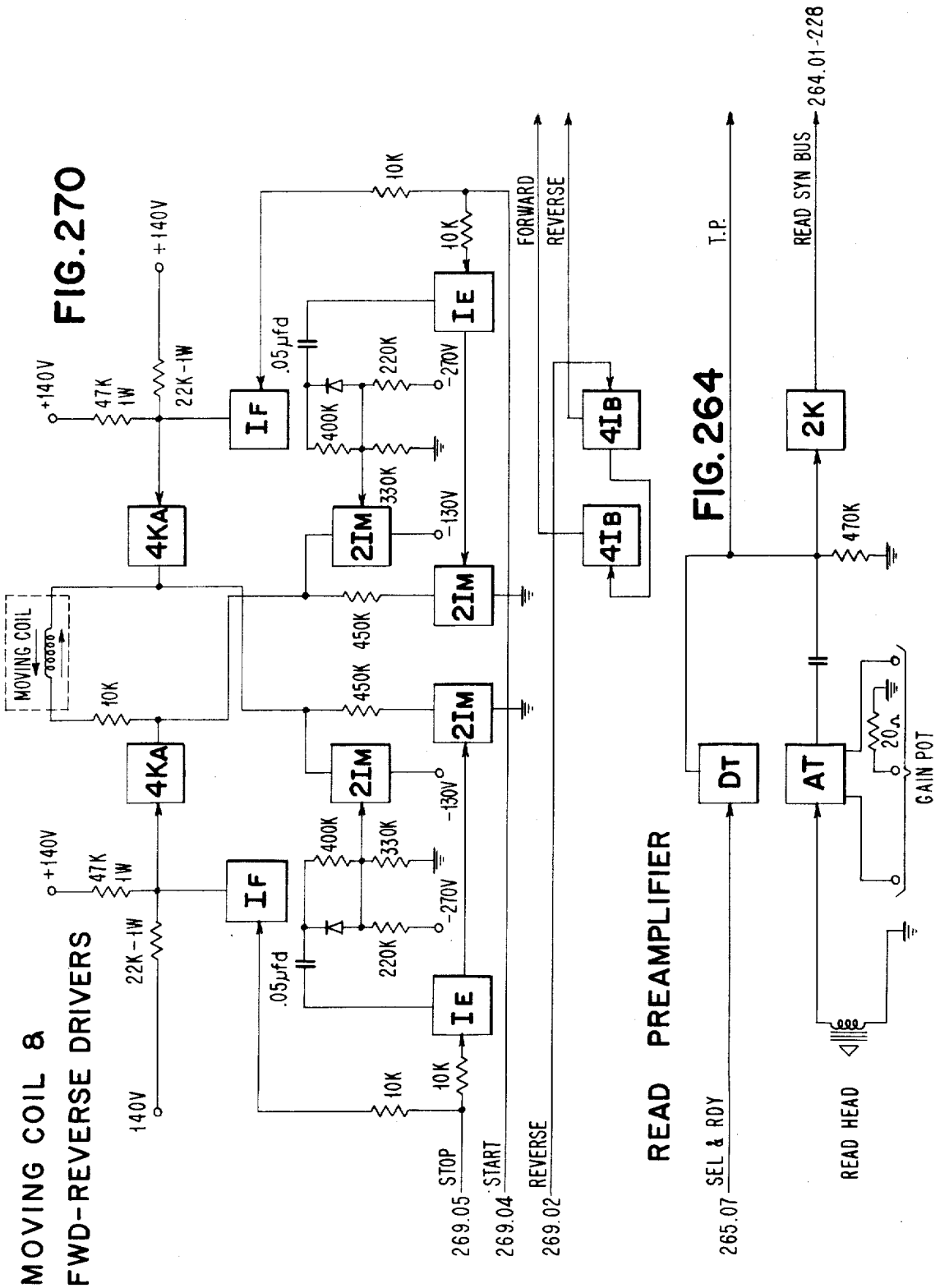

R/W ERROR & TAPE EOR
233.01 LATERAL R/W ERROR
260b.03 PARITY SAMPLE
238.01 TAPE CHECK
231.02 LRC REG NOT ZERO
12.4K
-60V
250.09 TCU DISC.
255.07 READ CALL
248.12 CLOCK GATE DELAY
256.09 WEOF CALL
A
O
GAf
K
KJ
R/W ERROR
261.01-185
READ TAPE EOR
261.02-196a, 196b
WEOF DISC.
261.03-176, 177

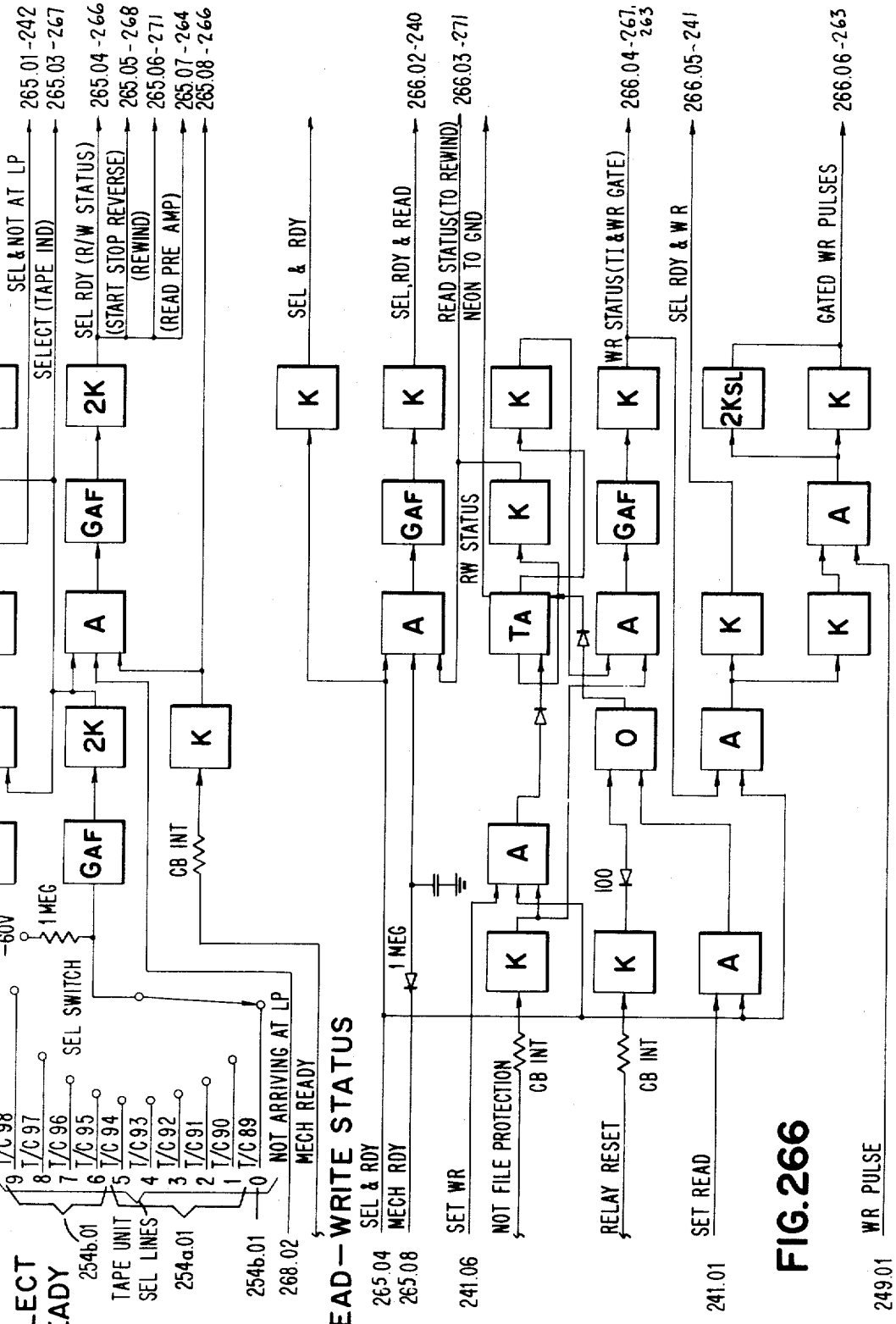
FIG. 261

FIG. 262


TAPE DRIVE
TURN ON TI
TURN OFF TI
243.01
243.05
WRITE PULSE
SET READ STATUS
SET WRITE STATUS
249.02
241.01
241.06
START REWIND
10 SEL LINES
266.03
REWIND CONTROL FIG. 271
READ WRITE STATUS GATED WR PULSE FIG. 266
266.04
SEL READY & READ
266.02
SEL READY & WRITE
266.05
267.01
267.02
TAPE INDICATOR FIG. 267
SEL & REWIND
265.03
265.01
SEL & READY
READ PRE AMP FIG. 264
READ BUS (7 LINES)
265.07
SEL & AT LP
268.04
READ HEADS WRITE HEADS
14 LINES
WRITE CKTS FIG. 263
WRITE ECHO BUS
263.01
WRITE STATUS
GATED WRITE PULSE
OP PANEL
SEL
SEL & READY FIG. 265
265.03
265.05
268.02
UNL/POWER ON
NO ARRIVING AT
LOAD POINT
RESET
LOAD POINT FIG. 268
268.03
268.07
AT LOAD POINT (RELAY)
PICK LOAD POINT (RELAY)
DROP LOAD POINT (RELAY)
RELAY CTRL CIRCUITS
MOTOR CTRL CKTS
TAPE START-STOP FWD 1 REV FIG. 269, 270
MANUAL REV
MANUAL START
GO
BACKWARD
WRITE BUS (7 LINES)
WRITE CHECK CHARACTER
240.01
239.07
227a,b,c,d
245.08


WRITE AMPLIFIER
WRITE HEAD
WHITE
RED
BLACK
IW
TZ
DG
GAF
KJ
KJO
KR
150K
470K
-60V
+140 NOT F.P.
WR BUS T/C
227a,b,c,d
GATED WR PULSES
266.06
WR STATUS
WR CHECK CHAR T/C 71
266.04
245.08
WR ECHO
263.01-246
NEON TO GND
-12 CLAMP RESET(WR TRIGS)"Z"
263.02-263
NOTE: "Z"=-12 CLAMP RESET, FIG. 263
FIG. 263
REWIND
A
GAF
K
O
K
RDX
REWIND PU RELAY
T/C 76 START REWIND
SEL & READY
243.08
265.06
READ STATUS
266.03
A
K
CB INT
MAN LOAD REWIND
SELECT
268.05
A
K
KO
CB INT
REWIND STATUS
SEL & REWIND STATUS T/C 78
271.02-243
H.S. REW AREA
H.S. REW AREA PHOTO CELL
RD
.01μfd
1 MEG
2.7M
5.1M
5.1M
-270V
H.S. REW AREA LAMP
FIG. 271


MOVING COIL & FWD-REVERSE DRIVERS
FIG.270
MOVING COIL
+140V
47K 1W
22K-1W
140V
4KA
IF
IE
2IM
4IB
10K
.05µfd
400K
330K
220K
450K
-130V
-270V
FORWARD
REVERSE
STOP
START
269.05
269.04
269.02
READ PREAMPLIFIER
FIG.264
T.P.
READ SYN BUS
264.01-228
DT
AT
2K
470K
20Ω
GAIN POT
SEL & RDY
265.07
READ HEAD


SELECT READY
TAPE UNIT SEL LINES
254b.01
254a.01
254b.01
268.02
NOT AT LP
T/C 98
T/C 97
T/C 96
T/C 95
T/C 94
T/C 93
T/C 92
T/C 91
T/C 90
T/C 89
NOT ARRIVING AT LP
MECH READY
CB INT
-60V
1 MEG
SEL SWITCH
K
A
2K
GAF
IL
SEL LITE
SEL & NOT AT LP
SELECT (TAPE IND)
SEL RDY (R/W STATUS)
(START STOP REVERSE)
(REWIND)
(READ PRE AMP)
265.01-242
265.03-267
265.04-266
265.05-268
265.06-271
265.07-264
265.08-266
FIG.265
READ—WRITE STATUS
SEL & RDY
MECH RDY
265.04
265.08
SET WR
241.06
NOT FILE PROTECTION
CB INT
RELAY RESET
CB INT
SET READ
241.01
WR PULSE
249.01
SEL & RDY
SEL, RDY & READ
READ STATUS(TO REWIND)
NEON TO GND
RW STATUS
TA
O
100
WR STATUS(TI & WR GATE)
SEL RDY & W R
GATED WR PULSES
2KSL
266.02-240
266.03-271
266.04-267, 263
266.05-241
266.06-263
FIG.266

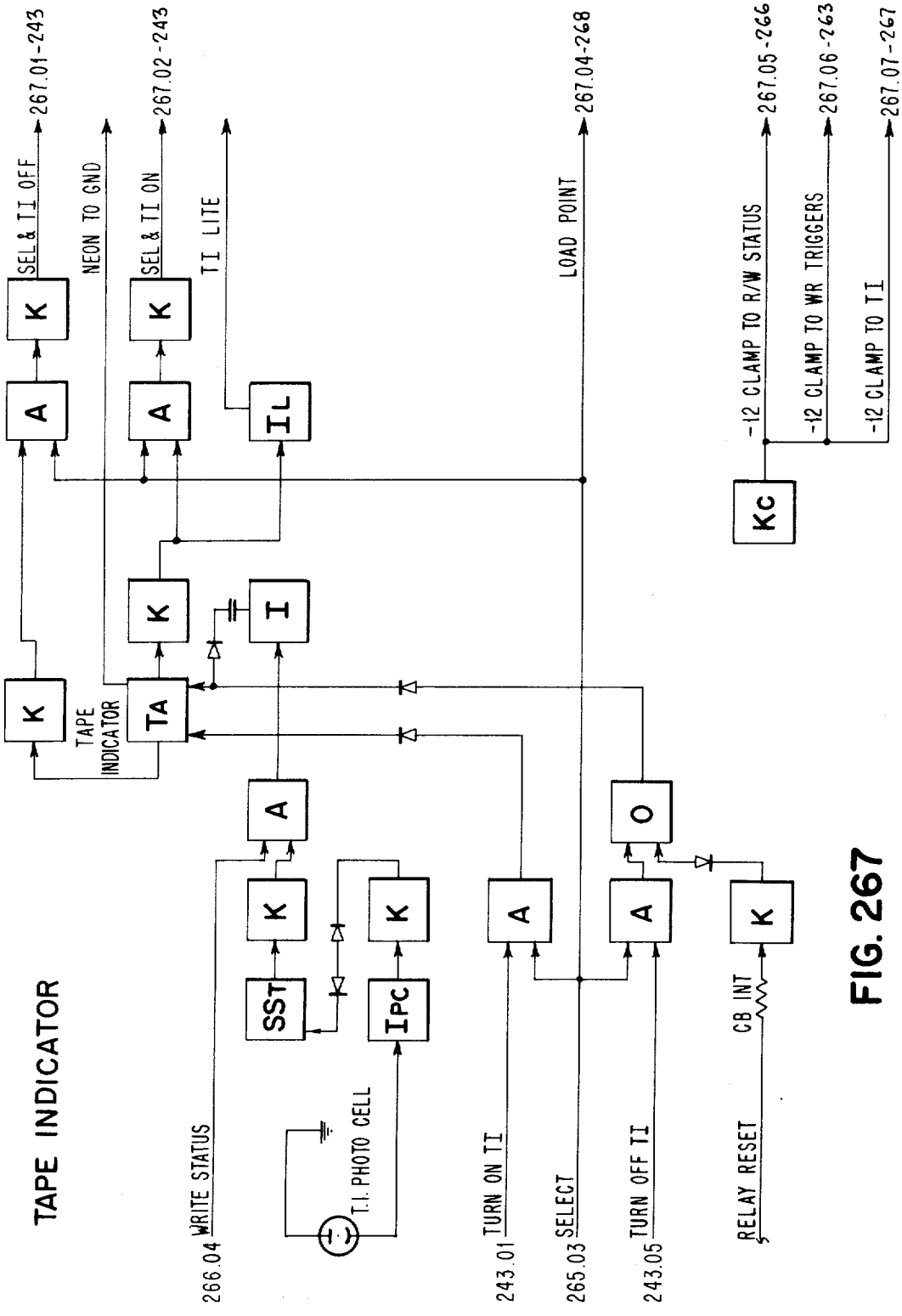
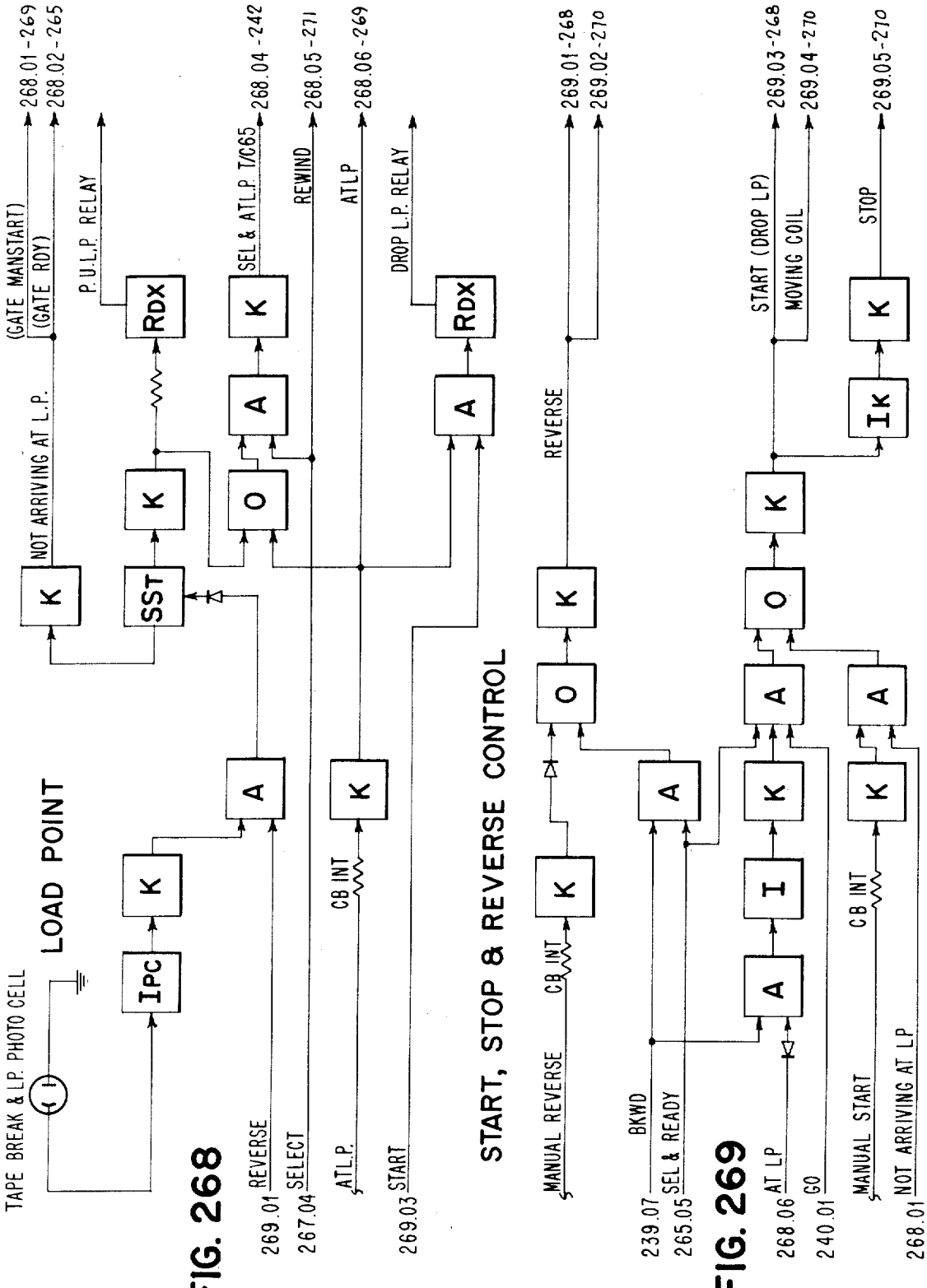

TAPE INDICATOR
266.04 WRITE STATUS
T.I. PHOTO CELL
243.01 TURN ON TI
265.03 SELECT
243.05 TURN OFF TI
RELAY RESET
CB INT
TAPE INDICATOR
NEON TO GND
TI LITE
LOAD POINT
-12 CLAMP TO R/W STATUS
-12 CLAMP TO WR TRIGGERS
-12 CLAMP TO TI
SEL & TI OFF
SEL & TI ON
267.01-243
267.02-243
267.04-268
267.05-266
267.06-263
267.07-267
K
A
TA
I
IL
SST
IPC
O
KC

FIG. 267


LOAD POINT
TAPE BREAK & L.P. PHOTO CELL
IPC
K
A
269.01 REVERSE
267.04 SELECT
CB INT
K
ATL.P.
269.03 START
NOT ARRIVING AT L.P.
K
SST
K
RDX
P.U.L.P. RELAY
(GATE MANSTART)
(GATE RDY)
268.01-269
268.02-265
O
A
K
SEL & ATL.P. T/C65
268.04-242
REWIND
268.05-271
ATLP
268.06-269
DROP L.P. RELAY
RDX
A
FIG. 268
START, STOP & REVERSE CONTROL
MANUAL REVERSE
CB INT
K
O
K
REVERSE
269.01-268
269.02-270
239.07 BKWD
265.05 SEL & READY
A
A
I
K
O
K
START (DROP LP)
MOVING COIL
269.03-268
269.04-270
268.06 AT LP
240.01 GO
A
A
K
IK
K
STOP
269.05-270
MANUAL START
CB INT
268.01 NOT ARRIVING AT LP
FIG. 269

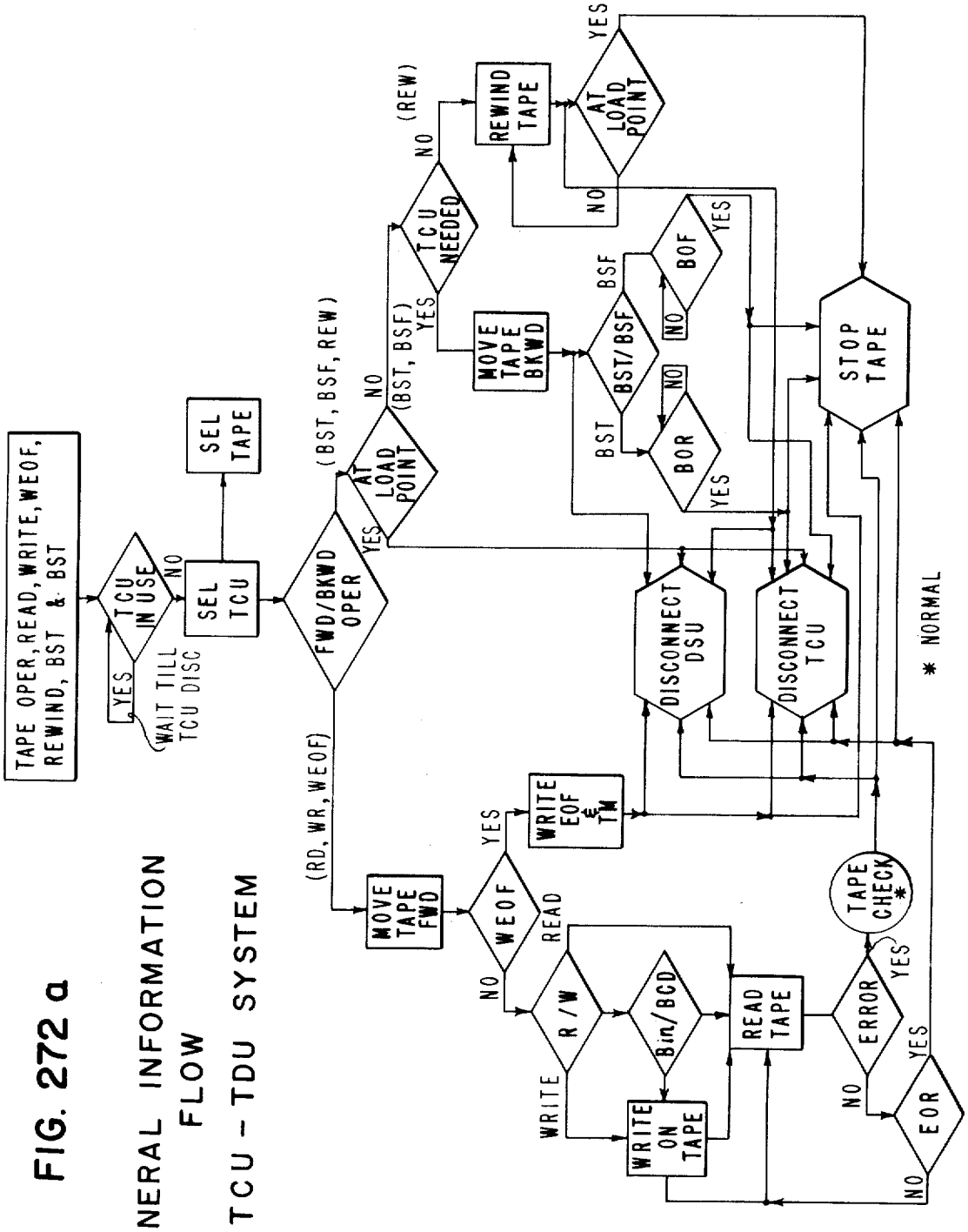


FIG. 272 a

GENERAL INFORMATION FLOW

TCU - TDU SYSTEM

GENERAL INFO FLOW TCU

FIG 272b

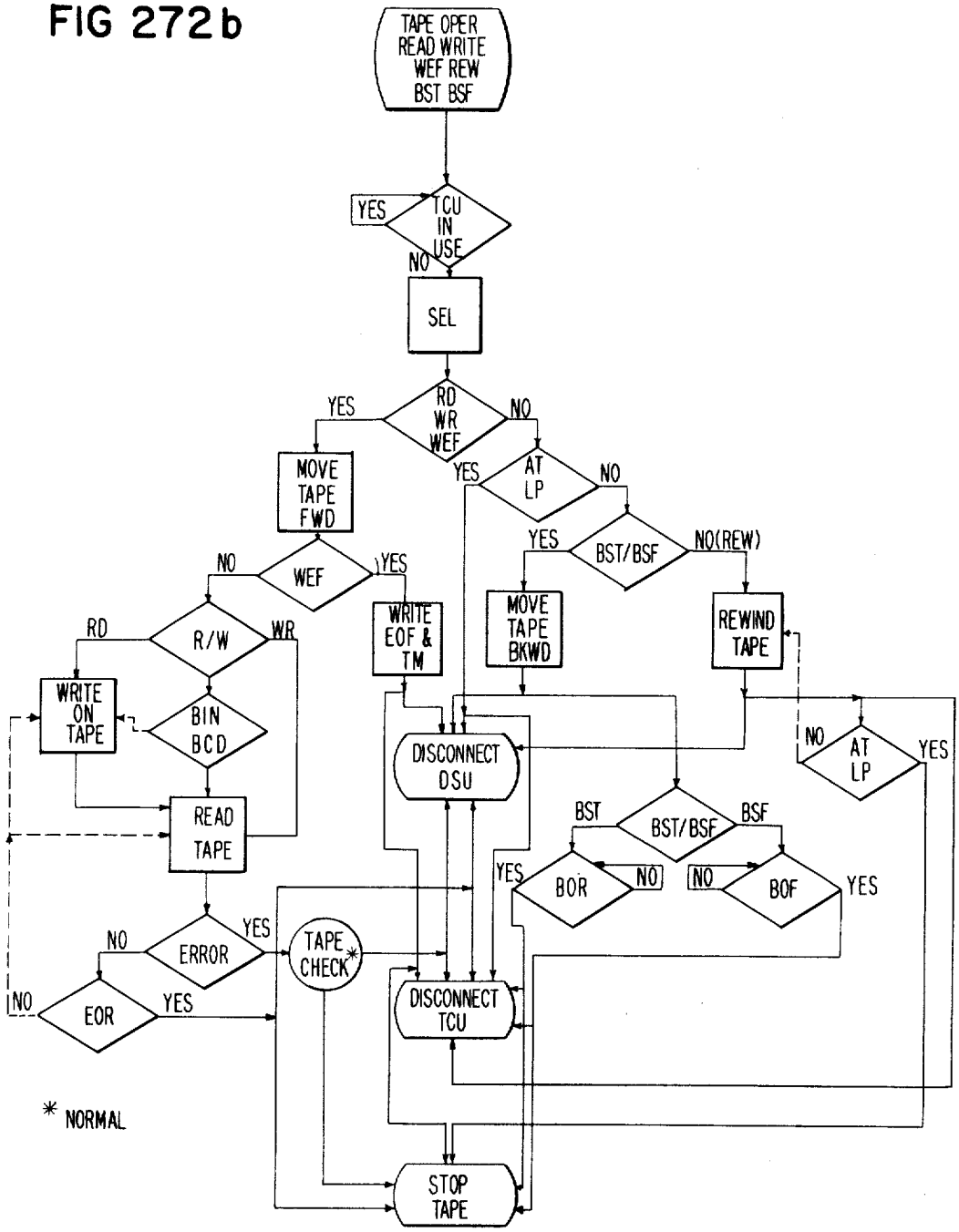


FIG. 273

DATA PROCESSING SYSTEM INCLUDING 3 DSU's

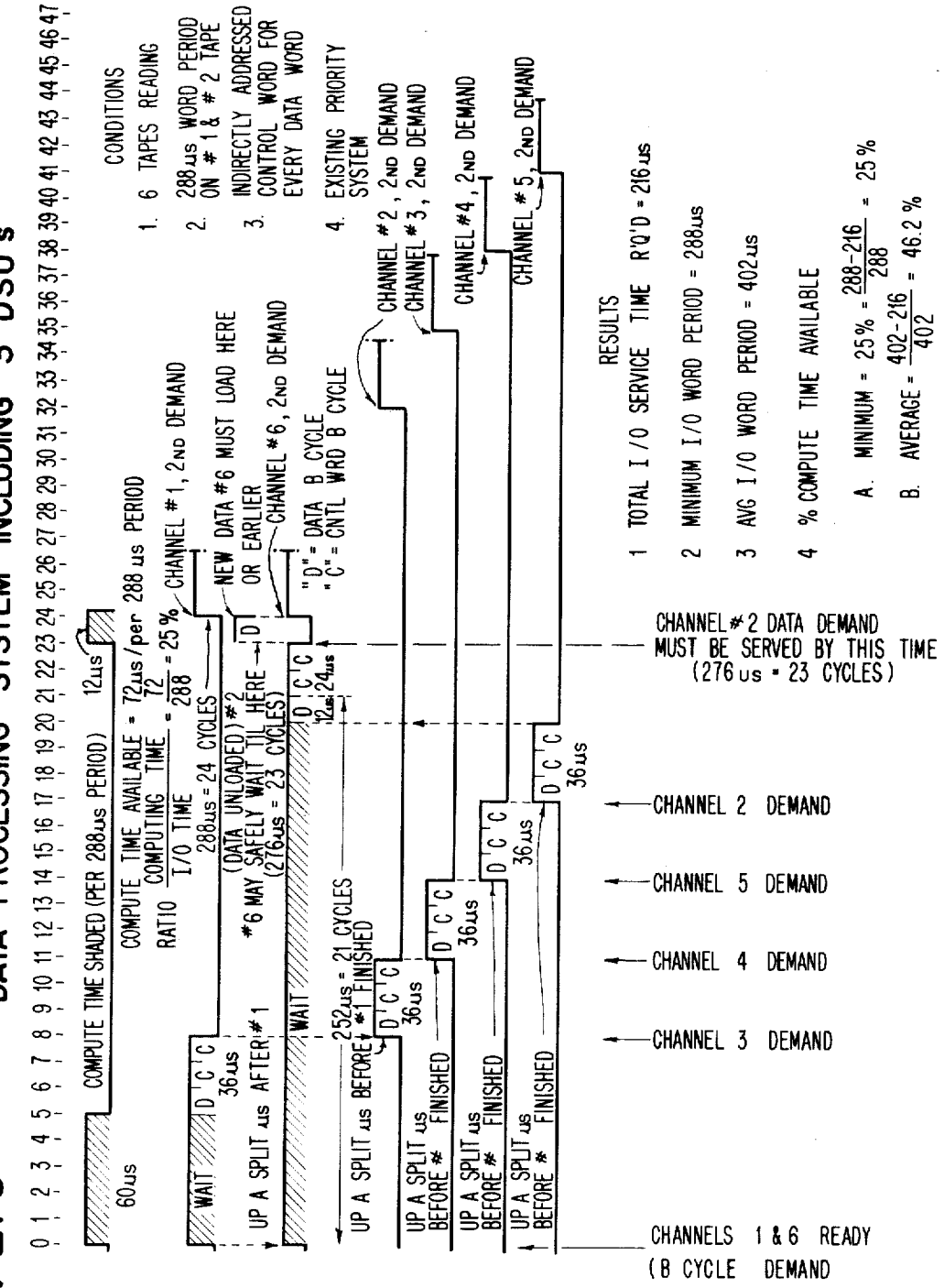
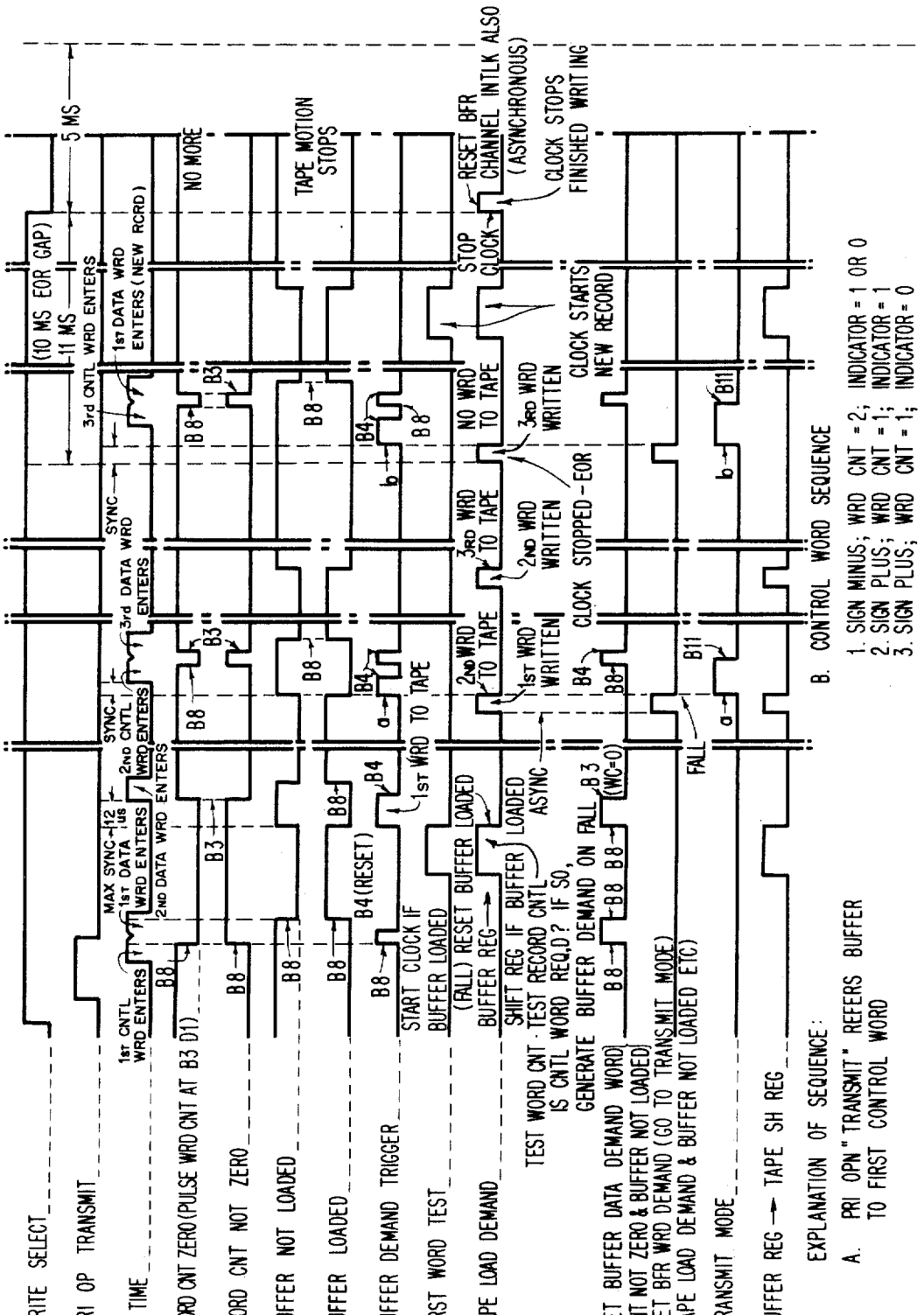


FIG. 274

DSU TIMINGS - TAPE WRITING



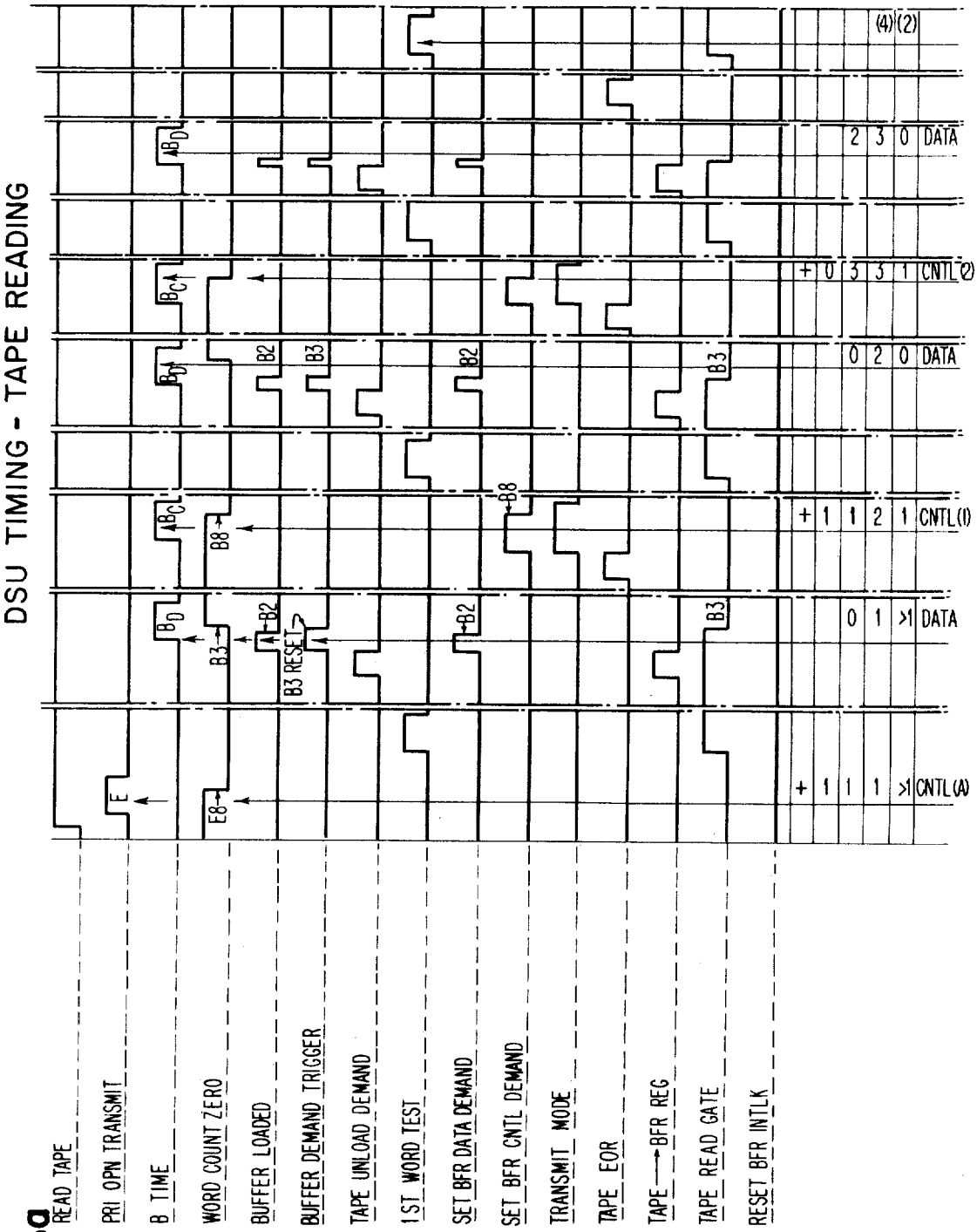
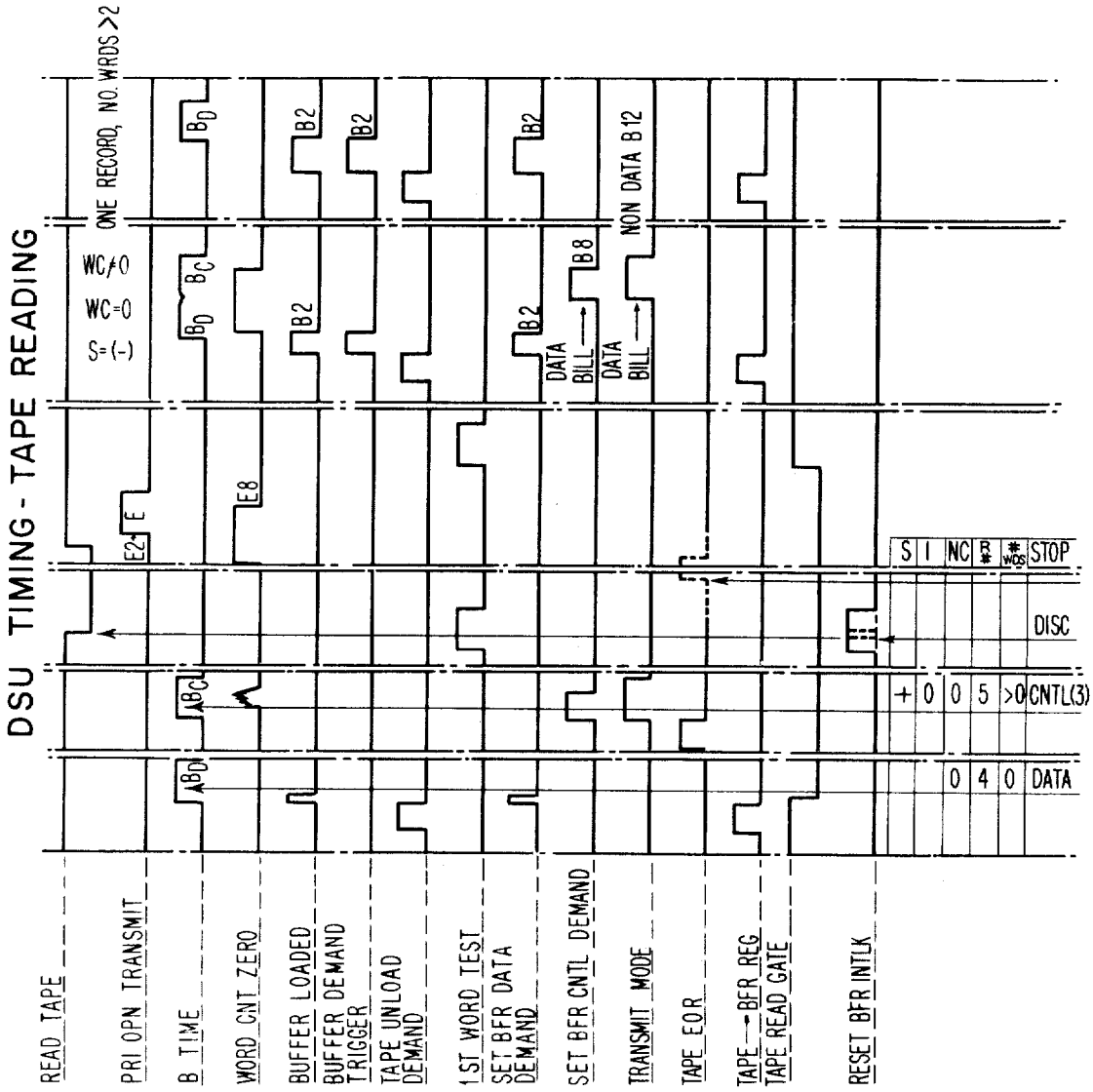

DSU TIMING - TAPE READING
READ TAPE
PRI OPN TRANSMIT
B TIME
WORD COUNT ZERO
BUFFER LOADED
BUFFER DEMAND TRIGGER
TAPE UNLOAD DEMAND
1ST WORD TEST
SET BFR DATA DEMAND
SET BFR CNTL DEMAND
TRANSMIT MODE
TAPE EOR
TAPE ⟶ BFR REG
TAPE READ GATE
RESET BFR INTLK
E
E8
B3
B2
B3 RESET
B8
B2
B3
B2
B8
B3
(4) (2)
2 3 0 DATA
+ 0 3 3 1 CNTL(2)
0 2 0 DATA
+ 1 1 2 1 CNTL(1)
0 1 >1 DATA
+ 1 1 1 >1 CNTL(A)

FIG.275a

FIG. 275b


DSU TIMING - TAPE READING
READ TAPE
PRI OPN TRANSMIT
B TIME
WORD CNT ZERO
BUFFER LOADED
BUFFER DEMAND TRIGGER
TAPE UNLOAD DEMAND
1ST WORD TEST
SET BFR DATA DEMAND
SET BFR CNTL DEMAND
TRANSMIT MODE
TAPE EOR
TAPE → BFR REG
TAPE READ GATE
RESET BFR INTLK
ONE RECORD, NO. WRDS >2
WC≠0
WC=0
S=(-)
E2
E
E8
B2
DATA BILL
B8
NON DATA B12
S I NC R * WDS STOP
DISC
+ 0 0 5 >0 CNTL(3)
0 4 0 DATA

DATA SYNCHRONIZER

This invention relates to data processing systems and more particularly to a system for synchronizing the transfer of data with a central processing unit between magnetic core storage and input-output devices by means of a data synchronizer device.

The data synchronizer is a multi-channel input-output unit controlling device with the ability to transmit information asynchronously between input-output (I/O) devices directly to a shared storage device. It is in effect an input-output sub-calculator of the stored program type and multiplexer having at least two channels, each of which may automatically execute a series of instructions previously placed in storage by the main computer including automatic programming branching facilities for each individual channel. While performing independent dual channel operation with the data synchronizer, simultaneous calculation continues without logical interruption in the computer or central processing unit. The data synchronizer is a buffer which receives information in an asynchronous manner from input-output devices and essentially synchronizes with the main flow of real time in the central processing unit in order to accomplish a synchronized storage of information in memory and receives information asynchronously from core storage and transmits it to I/O devices at a fixed synchronous rate. Another important feature of the data synchronizer is the ability of each information channel to provide the option of synchronous, concurrent operation with the computer in either processing or interpretation of information.

One of the most important features of time multiplexing operations is the fact that when a large number of relatively slow input-output devices require access to memory or to any other synchronous device, the first unit which requires service is the one which must pay the price in time to synchronize. This device may have to wait a maximum time slightly less than one machine cycle in order to synchronize. However, if other input devices are waiting, they need not resynchronize. This is important because it shows the difference between attempting to run one very high speed input-output device and the running of several slower input-output devices and multiplexing them. The advantage lies in the fact that single fast units require synchronization for each and every reference to core storage, but the use of several slower I/O units with multiplexing operations requires only one synchronization with storage if one or more of the other units are awaiting service. Therefore, the absolute maximum theoretical rate of data transmission between input-output units and memory may be made to match the speed of the calculator.

Using the Data Synchronizer Unit (DSU), the operator need only provide an instruction or control word specifying the starting address in storage of the series of commands to be executed by that Data Synchronizer Channel and upon receipt of this information the Data Synchronizer assumes complete control of the input-output process and the main program proceeds in the Central Processing Unit without logical interruption as the input-output units move information into and out of Storage.

Associated with each DSU channel is a Buffer Register having as a function the holding of the word being read until a reference to Storage can be obtained or alternately to hold the word being written until the Input-

Output device is ready to receive it. Also, each channel has a Word Counter used to hold the number specifying the record length and to signal the DSU when the prescribed number of words has been read or written. Furthermore, there is an Address Counter associated with each channel having the function of keeping track of the storage addresses being used during data transmission. Another counter, referred to as the Location Counter, has the function of storing an address which may be used at the end of a DSU operation for a reference to memory at the address specified in the Location Counter. At this new address, the DSU obtains a new control word or instruction and automatically initiates operations specified by the new control word.

Two instructions are required to operate an Input-Output unit through the Data Synchronizer. The first is a Select Instruction which selects the Input-Output device to be used, the DSU channel to be used, and specifies whether the Input-Output device is to read or write. The other instruction required is called a Load Channel Instruction which causes the previously stored control word to be read out of storage into the DSU's Word Counter and Address Counter. The address part-plus-1 of the Load Channel Instruction is placed in the Location Counter. At the conclusion of the transmission of the Load Channel Instruction, the Central Processing Unit is free to return to its program and the DSU has been provided with all the information necessary to initiate and control the specified Input-Output operation.

After the DSU has received the control information and after the selected Input-Output device has been set in motion and is at the proper speed, the DSU channel becomes synchronized with the Input-Output device. When the Input-Output device is ready to receive or transmit a full word from or to the DSU, it signals the DSU and the 36 bit register is either loaded by the Input-Output device in the case of reading or is unloaded to the Input-Output device in the writing operation. At this time, a request for a storage cycle is initiated by the Data Synchronizer Unit. If the instruction being executed at this time in the Central Processing Unit cannot provide such a cycle, the DSU waits until that instruction is complete to interrupt the CPU program when it causes the Central Processing Unit to insert the required memory cycle between two successive instructions. Now, during the DSU initiated memory cycle, the Data Register contents are either stored in, or read from, memory at the address specified by the DSU channel's Address Counter. The Word Counter is stepped down by 1 and the Address Counter is stepped up by 1, this preparing the DSU for the next word to be read or written. This process is repeated once for each word of the Input-Output record and continues until the word counter reaches zero or until an End of Record indication is received. The operator has an option to use a special bit in the control word to specify whether the Word Counter reaching 0 or End of Record indication causes termination of the operation. Furthermore, the operator has the option by means of a second special control bit in the control word of either disconnecting at this point or of causing the DSU to automatically return to Storage at the address specified by the Location Counter previously mentioned. Accordingly, by use of one Select and one Load Channel instruction and a table of control words stored in Memory, the operator has the ability to cause the read-

ing of a file of records from Input-Output devices and to scatter the words in a record or the records themselves or both throughout Core Storage in any sequence specified. While writing, the operator has the ability to cause the writing of a number of words or records or both sequentially that are not stored sequentially in Storage.

The DS Buffer Register receives information in an asynchronous manner from an Input-Output device and effectively synchronizes with the flow of real time in the Central Processing Unit in order to accomplish a synchronous storage of information in Memory. When writing, the converse is true. A synchronous movement of data between Core Storage and a Data Synchronizer Channel is accomplished and then the Input-Output device extracts the information from the Buffer Register in an asynchronous manner at any later time. The Buffer Register is at all times synchronized with the I/O device when writing, however.

It is an object of this device to speed up the rate of data transmission by means of multiplexing the processes to a point where the system and data flow rate nearly match the rate of calculation without the necessity for logical interference with the Main Calculator.

It is another object of this invention to provide a plurality of independent channels for information flow which may transmit data simultaneously in either direction and in any combinations thereof between a primary Storage device and Input-Output devices while the calculator is computing.

It is another object of this invention to provide apparatus for information scattering or block data transmission to any degree from one word to massive blocks requiring the capacity of a memory system.

It is another object of this invention to provide data handling apparatus which is universally compatible with input-output devices.

It is another object of this invention to provide control apparatus for program supervision of input-output devices to any degree desired either on a word by word basis or block basis.

It is another object of this invention to provide apparatus for permitting input-output devices to make reference to Core Storage without logical interference with the Central Processing Unit.

It is a still further object of this invention to provide an apparatus having the ability to store a plurality of consecutive instructions concerning input-output device control in each channel without logical delay to the calculator.

It is a still further object of this invention to provide apparatus including a sub-computer having automatic access to Core Storage for both data and data handling instructions where the Central Processing Unit is only required to provide the data transmitting program to Primary Storage, initiate Input-Output operation by selecting a free channel of the apparatus, and supplying that channel with information as to the location in Memory where subsequent instructions may be extracted by that channel.

It is another object of this invention to provide for picking or selecting a predetermined word, words, or records from a file while reading the file.

It is another object of this invention to provide a priority system for switching a plurality of data synchronizer channels to core storage for servicing each as required by multiple operation of the channels.

It is an object of this invention to provide an improved multi-channel data controlling device with the ability to transmit data asynchronously between input and output units of various types directly to storage.

It is another object of this invention to provide an improved multi-channel device, each channel being capable of independent operation without logical interference with each other during the bilateral transfer of data through the channels.

It is another object of this invention to provide a data handling device having at least two independent channels and multiplexing controls for receiving data from a number of independent sources and for arranging and transmitting the data in sequential order in the time domain to a shared storage device.

It is another object of this invention to provide apparatus for the synchronous distribution of data from a common storage device at one speed to a plurality of storage devices at another than the one speed.

It is another object of this invention to provide an improved data handling device for coordinating the collection of data which is presented in random fashion from a number of individual sources in a storage device in serial fashion.

It is another object of this invention to provide an improved data handling device for controlling the collection of data which is presented in random fashion from a number of individual sources in a storage device in a synchronous fashion.

It is another object of this invention to provide improved data handling apparatus including data channels connecting a number of storage devices with a common or shared storage device, such storage device being adapted to store instructions and data, and each channel having means for receiving program information from the storage device and performing an iterative program to transfer data through the channels including circuits for coordinating the passage of data between the several channels.

It is another object of this invention to provide improved data processing apparatus including a first stored program computer, a storage device for storing instructions and data, a number of individual Input-Output devices, and data handling apparatus coupling the Input-Output devices with the storage device and including calculator circuits for computing addresses for reference to the storage device including circuits for performing operations in response to the instructions effective to control the passage of data through the data handling apparatus.

It is a still further object of this invention to provide a data processing system including data processing apparatus for performing arithmetic manipulation in iterative time increments having circuits for decoding instructions to thereby direct machine operations, a storage device connected to the data processing machine capable of storing instructions and data in successive iterative time increments in selectable locations in response to directions from the data processing machine and capable of serially transmitting the words of instructions or data in response to transmit directions, a group of bilateral transmitting devices having decoding circuits for receiving instructions and providing command signals indicative of particular operations, and groups of selectable Input-Output devices connected

by groups to individual ones of the bilateral data transmitting devices and individually operable when selected for performing operations in response to the command signals to thereby provide data to or receive data from the bilateral data transmitting devices.

It is another object of this invention to provide improved multi-channel data controlling device constructed to transmit data between the input and output units of various types directly to storage in response to the stored program instructions received from the storage device and decoded in the data controlling device.

It is another object of this invention to provide an improved control device including a storage register which is effective while the central processing unit is performing operations to transfer information from a storage array to an Input-Output unit concurrently with the transfer of information from another Input-Output unit to the same storage array.

Another object of this invention is to provide an improved data handling device selectively operable with a plurality of Input-Output devices including means for stacking instructions through the system for sequential operations.

It is another object of this invention to provide an improved data handling device operable with the central processing unit and the central storage unit for transferring information between input-output devices and the storage unit including apparatus providing for the sharing of the storage unit between the central processing unit and the Input-Output devices.

It is an object of this invention to provide improved apparatus for the transmission of data between storage devices which may operate concurrently with the Central Processing Unit processing data or in the concurrent interpretation of instructions with the Central Processing Unit.

It is still another object of this invention to provide improved data handling apparatus for controlling the transfer of data between a shared storage device and input-output units concurrently with independent central processing unit operation.

It is still another object of this invention to provide improved data handling apparatus for use in cooperation with a central processing unit, the data handling apparatus being arranged to control the transfer of data between a shared storage device and input-output units concurrently with independent central processing unit data manipulation and being arranged to share access with the central processing unit.

It is a still further object of this invention to provide improved apparatus including a storage device and at least two program controlled data handling devices for moving data into and out of the storage device.

It is a still further object of this invention to provide data handling apparatus for transferring information between a storage device and input-output devices which may be controlled either by a list of control words previously placed in memory or by manually operable controls.

It is an object of this invention to provide an improved system for establishing priority between a plurality of input-output devices seeking access to a storage device in which the first device seeking access to storage is the first served and all other devices are served before any information is lost.

It is an object of this invention to provide an improved device for establishing priority between a plurality of input-output devices in a random fashion in response to individual requests for access to a storage device.

It is an object of this invention to provide an improved device for establishing priority between a plurality of input-output devices seeking access to a storage device in a logical order as opposed to a sequential selection order.

It is another object of this invention to provide apparatus for reading and checking a file of information and transmitting only portions found in error to the primary storage device.

It is an object of this invention to provide means associated with a central processing unit to test the status of a data transmitting device during iterative data processing operations for either providing instruction or data to the data transmitting device if ready or continuing with the iterative data processing operation if not ready.

It is another object of this invention to provide improved control apparatus in a data processing system which is operative in response to an instruction to test the status of input-output devices and make a decision based on the status to modify the operation of the system in a predetermined manner.

It is a still further object of this invention to provide multi-channel apparatus including at least one input-output device and a control device therefor for each channel in tandem relationship, each having the ability to store a plurality of consecutive instructions concerning input-output device operation in each channel for serial movement and execution of the stored instructions upon completion of each operation of an input-output device.

It is a still further object of this invention to provide in addition to a principal calculator a plurality of control devices, each including arithmetic units for the interpretation of commands, which have automatic access to a shared storage device for both data and data handling commands wherein the principal calculator provides the initial instruction to the control devices concerning the operation to be initiated and the location in storage from which subsequent commands are extracted by the control devices and the control devices operate autonomously thereafter.

It is another object of this invention to provide, in combination with a non- addressed tape, means for picking or selecting a predetermined word, words, or records from a file recorded on tape during the process of reading on tape.

It is another object of this invention to provide a priority system for a plurality of input-output units associated with data synchronizer channels for selecting among a plurality of channels a channel or transmission of data as required during multiple operations of the input-output units.

It is another object of this invention to provide, in combination with a storage device, a data handling device having at least two independent channels and multiplexing controls for receiving data from a number of independent sources and arranging and transmitting the data in sequential order in the channels whereby data are delivered in the desired sequence to the storage device.

It is another object of this invention to provide apparatus for the synchronous distribution of data from a common storage device at one speed to a plurality of storage devices at other than the one speed.

It is an object of this invention to provide improved apparatus included in a data processing system which has data storage devices, control devices therefor, and means for checking the accuracy of data recorded or sensed in the storage devices and indicating the correctness thereof, means for interpreting a transfer instruction and modifying the sequence of operations in response to the indications of correctness of the data recorded or sensed.

It is another object of this invention to provide improved data processing apparatus including a computer, a storage device for storing instructions and data, a plurality of input-output devices, data handling apparatus coupling the input-output devices with the storage device, the data handling apparatus including operation registers for controlling input-output device operation for the passage of data through the data handling apparatus and circuits responsive to a signal from the computer for storing the contents of the operation registers in the data handling apparatus at a predetermined location in the storage device.

In connection with the objects pertaining to the wide difference in speed between input-output devices and high speed electronic data processing equipment such as the Central Processing Unit and Magnetic Core Storage, attention is directed to Digital Computer Programming, D. D. McCraken, Library of Congress Catalog Number : 57-8891, especially pages 9 and 10.

Other objects of the invention will be pointed out in the following description and claims and illustrated in the accompanying drawings, which disclose, by way of example, the principle of the invention and the best mode which has been contemplated of applying that principle.

In the drawings:

FIG. **1** is an overall block diagram illustrating generally the major components comprising the Data Processing System and their interconnections.

FIGS. **2***a* through *eee* form the logical block diagrams of the principal data portions of the Central Processing Unit.

FIG. **2***fff* illustrates how FIGS. **2***a* through *eee* inclusive may be placed to form a composite block diagram of the major data portions of the Data Processing System.

FIGS. **3***a* through **3***k* illustrate the word formats used in the Data Processing System.

FIG. **4** illustrate the data paths of FIGS. **2***a*–**2***gg*.

FIGS. **5***a* through **5***f* illustrate positions of the Storage Register and Storage Register Hold Circuits in logical block form.

FIG. **5***bx* is a table of storage bus input connections to the storage register and outputs from the storage register of FIG. **5***b*, for columns **1–17.**

FIG. **5***fx* is a table of outputs from the storage resister of FIG. **5***f* for columns **21–35.**

FIGS. **6***a* through **6***n* illustrate the Adder and True Complement controls in logical block form.

FIGS. **6***ax*, **6***cx*, **6***dx*, **6***ex*, **6***gx*, **6***hx*, **6***kx* and **6***lx* are tables of Adder outputs and carry inputs for corresponding Adder and True-Complement controls of FIGS. **6***a*, **6***c*, **6***d*, **6***e*, **6***g*, **6***h*, **6***k* and **6***l*.

FIGS. **7***a* through **7***g* illustrate the Accumulator Register in logical block form.

FIGS. **7***bx* and **7***cx* are tables of Accumulator register outputs **P–8** and **9–34** respectively.

FIGS. **8***a* through **8***g* illustrate the Multiplier Quotient Register and its associated hold circuits in logical block form.

FIG. **8***cx* is a table of connections between M Q register columns (**2–5**) of FIG. **8***c* and FIGS. **6***c*, **6***d*, **11***b*, **11***c*, **6***k*, **6***m*, **6***j* and **6***l*.

FIG. **9** illustrates the Index Register in logical block form.

FIG. **10** illustrates the Indicator Trigger Register in logical block form.

FIG. **10***a* is a table of connections between the storage register (FIGS. **5***a*, *b*, *c f*) and storage bus switching (FIGS. **11***a*, *b* and *c*).

FIGS. **11***a*, **11***b*, **11***c* illustrate the Storage Bus Switching, columns S through **35**, in logical block form.

FIG. **12** illustrates the Operators Panel Entry Keys (S through **35**).

FIG. **12***a* is a table of outputs **5–35** of the operator panel entry keys **5–35** of FIG. **12.**

FIGS. **13***a*, **13***b*, **13***c* (two sheets) and **13***d* (three sheets) illustrate positions **1** through **17** of the Instruction Register (Primary Operation Part) in logical block form.

FIGS. **14***a* through **14***d* illustrate the Primary Operation Decoder in logical block form.

FIGS. **15***a* and **15***b* illustrate the Secondary Operation Decoder in logical block form.

FIGS. **16***a* (two sheets) and **16***b* (two sheets) illustrate the Address Register in logical block form.

FIG. **17** (two sheets) illustrates the Instruction Counter in logical block form.

FIG. **18** illustrates the Add and Subtract Execution Control in logical block form.

FIG. **19** illustrates Clear and Add/Subtract Execution Control in logical block form.

FIG. **20** illustrates MPY/MPYR EXEC CNTLS (Multiply Execution Controls) in logical block form.

FIGS. **21***a* (two sheets) and **21***b* (two sheets) illustrate Floating Point Add/Subtract Execution Controls in logical block form.

FIG. **22** illustrates Floating Point Trap Trigger in logical block form.

FIG. **23** illustrates Floating Point Multiply Execution Controls in logical block form.

FIG. **24** (two sheets) illustrates Conditional Transfer Execution and Control in logical block form.

FIG. **25** illustrates Conditional Transfer Controls for Transfer on Low MQ in logical block form.

FIG. **26** illustrates Store Execution Controls in logical block form.

FIG. **27** illustrates Long Left, Logical Left Execution Control in logical block form.

FIG. **28** illustrates Long Right, Logical Right Execution Control in logical block form.

FIG. **29** illustrates OR to Storage Execution Control.

FIG. **30** illustrates AND to Accumulator and to Storage Execution Control.

FIG. **31** illustrates OR to Accumulator Execution Control.

FIG. **32** illustrates Load Index Register Control.

FIG. 33 illustrates Place Address in Index Register Control and Place Decrement in Index Register in logical block form.

FIG. 34 illustrates Transfer with Index Raise Execution Control.

FIGS. 35*a* and 35*b* illustrate Indexing Execution Control in logical block form.

FIGS. 36*a* (two sheets) and 36*b* illustrate Convert Control in logical block form.

FIG. 37 illustrates Exclusive OR to Accumulator in logical block form.

FIG. 38 illustrates Exchange, Transfer Sign Control in logical block form.

FIG. 39 illustrates Test Indicators (Storage) Half Test Indicators in logical block form.

FIG. 40 illustrates Transfer-Indicators (Accumulator) in logical block form.

FIG. 41 illustrates Place Indicators in Accumulator and Reset Indicators from Accumulator in logical block form.

FIG. 42 illustrates Half Indicator Register Controls in logical block form.

FIG. 43 illustrates Multiply and Multiplier, Floating Point Multiply Trigger and Shift/Step controls in logical block form.

FIG. 44 illustrates Place Accumulator in Indicators Load Indicators, Invert Indicators, or Accumulator Indicators in logical block form.

FIG. 45 illustrates Storage and Multiplicand Zero Test in logical block form.

FIG. 46 illustrates Interrupt Control in logical block form.

FIG. 47 illustrates Execution on Control Trigger (T1).

FIG. 48 illustrates Inverter Trigger T2.

FIG. 49 illustrates Index Register (N) Hold Lines Adder to Index Register (N).

FIG. 50 illustrates Adders to Index Register (N) Gating Line Control.

FIG. 51 illustrates Index Register to Adders Gating Line.

FIG. 52 illustrates Index Register Mixing Unit in logical block form.

FIGS. 53*a* and 53*b* illustrate Storage Bus to Storage Register.

FIGS. 54*a* (two sheets) and 54*b* (two sheets) illustrate Storage Register (1–8) to Adder, and Storage Register (9–35) to Adder.

FIGS. 55*a* (two sheets), 55*b*, 55*c* (two sheets) and 55*d* illustrate True Accumulator (Q,P,1–8) to Adders; True Accumulator (9–25) to Adders.

FIG. 56 illustrates Carry to Adder (35) in logical block form.

FIGS. 57*a* and 57*b* (two sheets) illustrate Adder (Q,P,1–8) to Accumulator Adder (9–35) to Accumulator in logical block form.

FIG. 58 illustrates Shift Accumulator Register Left Control.

FIG. 59 illustrates Shift Accumulator Register Right Control.

FIG. 60 illustrates MQ positions S, 1 or 9 to Accumulator 35, 1 to Accumulator 35 Control in logical block form.

FIG. 61 illustrates Plus to Accumulator Register position S control.

FIG. 62 illustrates Minus to Accumulator Register S Control.

FIG. 63 illustrates Storage Register S, 1 through 35 to MQ Register Controls in logical block form.

FIG. 64 illustrates Shift MQ Right Controls in logical block form.

FIG. 65 illustrates Shift MQ Left Controls in logical block form.

FIG. 66 illustrates Clear MQ Register in logical block form.

FIG. 67 illustrates Ring Shift MQ in logical block form.

FIG. 68 illustrates 1 to MQ Register position 35 Control in logical block form.

FIG. 69 illustrates I/O Bus, S through 35, to MQ Register Controls in logical block form.

FIG. 70 illustrates Adders to Accumulator Controls in logical block form.

FIG. 71 illustrates Minus to MQ position S controls in logical block form.

FIG. 72*a* and 72*b* illustrate Accumulator to Storage Bus Controls.

FIG. 73 illustrates Operation Panel Keys to Storage Register Controls.

FIG. 74 illustrates MQ Register S, 1 through 35 to Bus S, 1 through 35 and Storage MQ Register Store Control.

FIG. 75 illustrates Address Switches to Storage Bus 3 through 17, 21 through 35 Control.

FIG. 76 illustrates Clear and Add/AND Control.

FIG. 77 illustrates Minus to Storage Register S Control in logical block form.

FIG. 78 illustrates 35 to Shift Counter Control in logical block form.

FIG. 79 illustrates Step Shift Counter Controls in logical block form.

FIG. 80 illustrates Adder (1) Carry or Accumulator (1 or P) to Overflow Trigger Controls.

FIG. 81 illustrates Ones to Adders Q,P,1 through 8 Controls in logical block form.

FIG. 82 illustrates Carry to Adder Position 8 Controls in logical block form.

FIG. 83 illustrates Floating Point Shift Control in logical block form.

FIG. 84 illustrates Adders 1 through 8 to MQ 1 through 8 in logical block form.

FIG. 85 illustrates Step Floating Point Tally Counter in logical block form.

FIGS. 86*a* and 86*b* illustrate Indexing Operation and Storage Register 18 through 35 to Adders P through 17.

FIGS. 87*a* and 87*b* illustrate Index Register to Adder Controls in logical block form.

FIG. 88*a* illustrates Floating Point Tally Counter.

FIG. 88*b* illustrates Trapping Control in logical block form.

FIGS. 89*a* and 89*b* illustrate Index Register Entry Control Carry One to Adder 16 and Carry One to Adder 17 Controls.

FIGS. 90*a* and 90*b* illustrate Indexing Controls.

FIGS. 91*a* and 91*b* illustrate Adder to Index Register.

FIG. 92 illustrates Electronic Reset of Indicators.

FIG. 93 illustrates Reset Indicators Controls in logical block form.

FIG. 94 illustrates Set Indicators Controls in logical block form.

FIG. 95*a* illustrates Invert Indicators Controls in logical block form.

FIG. **95***b* illustrates Display Indicators.
FIG. **96** illustrates Indicators to Storage Bus Controls in logical block form.
FIG. **97** illustrates complement Indicators to Storage Register Controls in logical block form.
FIG. **98** illustrates Indirect Addressing Controls in logical block form.
FIG. **99** illustrates Instruction Register Pulse Generator in logical block form.
FIG. **100** (two sheets) illustrates Instruction Register Sign, Plus and Minus Controls in logical block form.
FIG. **101** illustrates Shift Counter Pulse Generator 1 in logical block form.
FIG. **102** illustrates Shift Counter Pulse Generator 2 in logical block form.
FIG. **103** illustrates Zero Address Controls.
FIG. **104** illustrates Floating Point Entry to Shift Counter **10** through **17** Controls.
FIG. **105** illustrates Subtract Control in logical block form.
FIG. **106** illustrates Sense Unit Address in logical block form.
FIG. **107** (two sheets) illustrates Advance Instruction Counter in logical block form.
FIG. **108** illustrates Reset Instruction Counter Address Switch to Instruction Counter Control in logical block form.
FIG. **109** illustrates Instruction Counter Transfer Control in logical block form.
FIGS. **110***a* and *b* illustrate Address Switch Input Controls in logical block form.
FIG. **111** illustrates Enter MQ Control in logical block form.
FIG. **112** illustrates the Primary Drive Circuits.
FIG. **113** illustrates a Sign Mixing Controls.
FIG. **114** illustrates the Master Oscillator.
FIG. **115** illustrates the Inverted Sync Generator.
FIG. **116** illustrates the Inverted Clamp Generator and Clock Drive.
FIG. **117** (two sheets) illustrates the Clock.
FIG. **118** (two sheets) illustrates Cycle Timer Control.
FIG. **119** illustrates Cycle Timer Gate Generator.
FIG. **120** illustrates Cycle Timer Output Circuit.
FIG. **121** illustrates B Time Control.
FIGS. **122***a* (two sheets) to *p* illustrate Pulse and Gate Generator Controls.
FIG. **123** illustrates Column Q Carry and Overflow Triggers.
FIG. **124** illustrates Column 9 Carry and Overflow Triggers.
FIG. **125** illustrates Floating Point Overflow Trigger and Floating Point Underflow Trigger.
FIG. **126***a* indicates Adder X Carry Trigger.
FIG. **126***b* illustrates Divide Check Trigger.
FIG. **126***ax* is a table of inputs to FIG. **126***a* from Adder (N) carry output.
FIG. **127** illustrates Floating Point Overflow and Underflow Detection.
FIGS. **128***a* (two sheets), *b* and *c* illustrate End Operation Control.
FIGS. **129***a* and *b* illustrates the Storage Address Register.
FIGS. **130***a* and *b* illustrate the Pulse Generator I and II.
FIG. **130***c* illustrates Timing Pulse Control Circuits.
FIGS. **131***a* and *b* illustrate the Address Decoder Circuit.
FIGS. **132***a* and *b* illustrate the Address Decoder Circuit.
FIG. **133** illustrates Write Driver Select Circuits.
FIGS. **134***a* and *b* illustrate Gate Generator.
FIG. **135** illustrates the X Matrix Switch Write Driver.
FIG. **136** illustrates the X Matrix Switch Read Driver.
FIG. **137***a* illustrates the Y Driver Matrix Switch Layout.
FIG. **137***b* illustrates diagrammatically a Core with certain of its Control Windings.
FIG. **138***a* illustrates diagrammatically the Core Array Layout.
FIG. **138***b* illustrates, in isometric, a Core with Windings.
FIG. **139** illustrates the Y Matrix Switch Write Driver.
FIG. **140** illustrates the Y Matrix Switch Read Driver.
FIG. **141***a* illustrates the X Driver Matrix Switch Layout.
FIG. **141***b* illustrates diagrammatically a Core with certain of its Control Windings as in FIG. **137***b*.
FIGS. **142***a*, *b*, and *c* illustrate the Sense Amplifier, Buffer Register and I/O Switching.
FIG. **143** illustrates the Digit Plane Select Circuits.
FIG. **144** illustrates the Digit Plane Driver Circuits.
FIG. **145** illustrates the Address and Operation Control.
FIG. **146** illustrates the Read/Write Controls.
FIGS. **147***a*, *b*, and *c* illustrate Test Circuits, Test and Reset Controls and the Test Panel Circuits.
FIG. **148***a* illustrates Switch Core Panel and Core Plane Addressing (Octonary).
FIG. **148***b* is a timing chart illustrating the Timing of Magnetic Core Storage in sequence for one cycle from 3 time of a first cycle until 3 time of a second cycle.
FIG. **149** (two sheets) illustrates the Class Decoder.
FIG. **150** (two sheets) illustrates the Unit Selection Matrix.
FIG. **151** illustrates the Input-Output Selection Interlock.
FIG. **152** illustrates the Unit Selector.
FIG. **153** illustrates the Channel Selector.
FIG. **154** illustrates the Interlock Test Skip Control.
FIG. **155** illustrates the Enter Execute Control.
FIG. **156** illustrates End Operation Mixing.
FIG. **157** illustrates Disconnect Synchronizer.
FIG. **158** illustrates MQ Reset and MQ Read-In Circuits.
FIG. **159** illustrates Tape Control.
FIG. **160** illustrates DSU Instruction Decoder.
FIG. **161***a* (two sheets) and *b* illustrates DSU Conditional Transfer Controls.
FIG. **162** illustrates Channel Control.
FIG. **163***a* illustrates DS Word Counter A.
FIG. **163***b* illustrates Word Count Zero Channels A and B.
FIGS. **164***a* and *b* illustrates DS Address Register A (**10**–**17**) and (**2**–**9**).

FIGS. 164*c* and *d* illustrates DS Address Register B (10–17) and (2–9).

FIGS. 165*a* illustrates Channel A Indicators S, 1 and 2.

FIG. 165*b* illustrates Channels A and B Indicators (19).

FIGS. 166*a* and *b* illustrate the Location Register A (10–17) and (2–9).

FIGS. 167*a* and *b* illustrate the Data Register A Trigger S–17 and 18–35.

FIG. 168 illustrates the Thyratron Register (S–17).

FIGS. 169*a* and *b* illustrate DSU Storage Bus Switching columns S–17 and 18–35.

FIGS. 169*ax* and 169*bx* are a table of storage bus connections to registers A and B.

FIG. 170 illustrates DSU Address Switching.

FIG. 170*a* is a table of Location register A, Location register B, Address register A, and Address register B inputs to DSU address switching of FIG. 170.

FIG. 171 illustrates Channels A and B Class Selection Interlock.

FIG. 172 illustrates Channels A and B End Operation Synchronizer.

FIGS. 173*a* and *b* illustrate Channel A Data Class Selection.

FIG. 174 illustrates Channel B Data Class Selection.

FIG. 175 illustrates Data Class Selection Interlock.

FIG. 176 illustrates Channel A Non-data Selection.

FIG. 177 illustrates Channel B Non-Data Selection.

FIG. 178 illustrates Card Machine Selector and Disconnector.

FIGS. 179*a* and *b* illustrate Channel A Unit Selection 1 through 5 and 6 through 10.

FIG. 179*c* illustrates Core Storage Unit Selection (2–737's).

FIGS. 180*a* and *b* illustrate Channel B Unit Selection 1 through 5 and 6 through 10.

FIG. 181 illustrate Printer and Punch Sense Outputs.

FIGS. 182*a* and *b* illustrate Command Decoding.

FIG. 183 illustrates Load Point Indicators.

FIG. 184 illustrates End of Tape Indicators.

FIG. 185 illustrates Channel A and B Tape Check Indicators.

FIG. 186 illustrates Card, End of Record/End of File and Reselect.

FIG. 187 illustrates End of File (EOF) Generators.

FIG. 188 illustrates SLC/RLC End of Operation Check.

FIG. 189 illustrates DS Store, Skip and Conditional Transfer Controls.

FIG. 190 illustrates Manual I/O Control.

FIGS. 191*a*, *b*, *c*, *d*, and *e* illustrate Automatic/-Manual Controls; Manual Control; Manual I/O Control respectively.

FIG. 192 illustrates Continuous Storage Read-In and Read-Out (A/B).

FIG. 193 illustrates Entry Keys to Storage Bus.

FIGS. 194*a*, *b* and *c* illustrate Channel A Read Gate and Write Clock Control Channel B Read Gate and Write Clock Control; and Read and Write Pulses.

FIGS. 195*a* and *b* illustrate Data Register A Loaded and Set Channel A BDW (B Data Word) Cycle Required and Data Register B Loaded and Set Channel B BDW Cycle Required.

FIGS. 196*a* and *b* illustrate Channel A and B Control Word Gate and End of Record Synchronizing Controls.

FIGS. 197*a* and *b* illustrate Channel A and B Set BCW Control Word Required.

FIGS. 198*a* (two sheets) and *b* (two sheets) illustrate Channel A and B Set ECW Control Word Required and Data Disconnect.

FIG. 199 illustrates Channel A and B Binary Coded Word Required and B Cycle Demand.

FIG. 200 illustrates DSU ECW Required.

FIG. 201 illustrates Channel A and B Transmit Mode Triggers.

FIG. 202 illustrates Proceed to E Time.

FIG. 203 illustrates Channel A and B BDW Required and Data B Cycle Demand.

FIG. 204 illustrates Channel and DSU Priority Required.

FIG. 205 illustrates Channel A and B Data B Cycle Triggers.

FIG. 206 illustrates Channel and DSU Priority Controls.

FIG. 207 illustrates I/O Octal and Binary Address.

FIG. 208 (two sheets) illustrates the Six-Position, Random-Sequence Commutator-DSU No. 1 and No. 2, respectively.

FIG. 209 illustrates Six-Position, Random-Sequence Commutator-DSU3.

FIG. 210 illustrates the Channel Register Gate.

FIG. 211 illustrates Channels A and B Store Samples.

FIG. 212 illustrates Storage Bus to Data Registers and Data Registers to Storage Bus.

FIG. 213 illustrates Address Register to Storage Address Register.

FIG. 214 illustrates Location Register to Storage Address Bus and Tape to Data Registers.

FIG. 215 illustrates Storage Bus-Control Registers.

FIG. 216 illustrates Storage Bus (3 to 17) to Word Controls and Load Control Trigger.

FIG. 217 illustrates Step Control Registers.

FIG. 218 illustrates Data Register Minus 12 Volt Clamp Resets.

FIGS. 219*a* and *b*, respectively, illustrate Channel A and B Minus 12 Volt Clamp Register Resets.

FIG. 220 illustrates Channel A Trigger Resets (XA).

FIG. 221 illustrates Channel B (XB) ECW and Proceed to E Trigger Resets.

FIG. 222*a* illustrates Card Control Pulse Generator.

FIG. 222*b*, *c*, *d* and *e* illustrate Pulse Generators.

FIG. 223 illustrate Card Read Write Control.

FIG. 224 illustrates Card Control Ring.

FIGS. 225*a* and *b* illustrate Tape Shifting Registers S through 29 and 30 through 35, respectively.

FIG. 225*ax* is a table of outputs from the tape shifting register of FIG. 225*a*.

FIG. 226 illustrate Tape Group Counter and Shift Left Six Pulse.

FIGS. 227*a*, *b*, *c* and *d* illustrate the Write Bus (C), (B,A), (8,2) and (4,1) Controls respectively.

FIG. 228 illustrate Final Amplifiers and High and Low Clip Read Registers.

FIG. 229 illustrates High Clip Lateral Parity Checker.

FIG. 230 illustrates Low Clip Lateral Parity Checker.

FIG. 231 illustrates LRC Test and Line Registers.

FIG. 231*a* is a table of outputs from the line register of FIG. 231.

FIGS. 232*a*, *b*, *c* and *d* illustrate Read Translator (C), (A,B), (8,2) and (4,1), respectively.

FIG. 233 illustrates Lateral Parity Checking.

FIG. 234 illustrates Check Bit Generator.

FIG. 235 illustrates High Clip Error and Sample and Not Stop and Error Gate.

FIG. 236 illustrates Low Clip Error and Sample and Sample Pulses.

FIG. 237 illustrates Clipping Selector and Tape Check Gating.

FIG. 238 illustrates High Clip and Low Clip Gating and Tape Check.

FIG. 239 illustrates Backspace Control.

FIG. 240 illustrates Go/Stop Control.

FIG. 241 illustrates Set, Read/Write Status.

FIG. 242 illustrates Backspace/Rewind After Write.

FIG. 243 illustrates Programmed Controls.

FIG. 244 illustrates Beginning of Record (BOR)/Beginning of File (BOF) Search and Record Gate.

FIG. 245 illustrates Character and Record Controls.

FIG. 246 illustrates Tape Mark Matrix and Seven-way "OR."

FIG. 247 illustrates End of File Sensing and First Character Gate.

FIG. 248 illustrates Read and Write Delay.

FIG. 249 illustrates Clock Write Pulse and Line Register Reset.

FIG. 250 illustrates Character Gate and Disconnect Controls.

FIG. 251 illustrates Read Clock and Line Register Reset.

FIG. 252 illustrates Class and Unit Disconnect Gate and Start Read/Write/Write End of File.

FIG. 253 illustrates Tape Control Unit Interlock.

FIGS. 254*a* and *b* illustrate the Tape Unit Selector (1-5) and (6-10) respectively.

FIG. 255 illustrates Data Class Selection.

FIG. 256 illustrates Non-Data Class Selection.

FIG. 257*a* illustrates Minus Twelve Volt Clamp Reset Pulse Generators.

FIG. 257*b* illustrates Minus Twelve Volt Clamp Reset Supplies.

FIGS. 258*a* and *b* illustrate Read-Write Test.

FIG. 259 illustrates Blank Generator.

FIGS. 260*a* and *b* illustrate Shift Register Controls One and Two Respectively.

FIG. 261 illustrates Read/Write Error and Tape End of Record Controls.

FIG. 262 is a functional Block diagram of the Tape Drive Circuits.

FIG. 263 illustrates a Write Amplifier.

FIG. 264 illustrates a Read Pre-amplifier.

FIG. 265 illustrates Select Ready Controls.

FIG. 266 illustrates Read-Write Status.

FIG. 267 illustrates Tape Indicator.

FIG. 268 illustrates Load Point.

FIG. 269 illustrates Start, Stop and Reverse Control.

FIG. 270 illustrates Moving Coil and Forward-Reverse Drivers.

FIG. 271 illustrates Rewind.

FIGS. 272*a* and *b* are charts illustrating, respectively, General Flow of Information in TCU-TDU System and General Flow of Information in TCU.

FIG. 273 is a sequence chart for a Data Processing System Including three DSU's.

FIG. 274 is a sequence chart of DSU Timings for a Write Operation on Tape, and

FIGS. 275*a* and *b* when taken together form a sequence chart of DSU Timings for a Reading Operation on Tape.

The convention employed in numbering lines in the logical block diagrams is as follows: from left to right, the first numbers and the letter, if any, to the period or point is the figure number from which the line originated; the next two numbers to the second point refer to the *output* lines (generally numbered according to their positions on the sheet from top to bottom); and the last two numbers, when used, refer to the numerical position of the line with the word S, 1 through 35. Each input line in the block diagram bears the number derived from its point of origin. In the composite drawings, data flows generally into the block at the top and out of the block at the bottom, and control lines which cause the movement of data enter the block from the left.

In FIG. 1, there is shown a data processing system comprising a Central Processing Unit (CPU) **1.10**, a Magnetic Core Storage **1.12**, a Magnetic Drum Storage device **1.14** and a Console **1.16** from which the operator may enter information to the system, monitor certain operations, observe the contents of certain ones of the registers and arithmetic devices comprising components of the CPU and alter programs. Connected to the Magnetic Core Memory **1.12** are three Data Synchronizer Units (DSU1,2,3) **1.20–1**, **1.20–2** and **1.20–3** respectively of substantially identical construction differing only in that their addresses are distinct which provide for the programmed transfer of data throughout the system with priority being established among the separate Data Synchronizer Units for access to the Magnetic Core Storage. Each Data Synchronizer Unit **1.20** may have Input-Output devices which are to be described in relation to the first Data Synchronizer Unit **1.20–1**, it being understood that like equipment is provided for the Data Synchronizers **1.20–2** and **1.20–3.** A Printer **1.24** is connected to channel A of Data Synchronizer **1.20–1** (hereafter designated as **1.20–1A**) and connected to the Printer is a Card Punch **1.26** and a Punched Card Reader **1.28.** A Tape Control Unit (TCU) **1.30–1A** couples a group of eight Tape Units **1.32-1A** through **1.32–8A** to channel **1.20–1A.** A Real Time device **1.34** is connected to channel **1.20–1B** and another Tape Control Unit **1.30–2B** couples the B Channel to Tape Units **1.32–1B** through **8B.** Each Tape Unit in the system, as well as Tape Control Units, in channels of the Data Synchronizers, are to be related to particular addresses hereafter in the discussion of programs in which the instructions designate among other things the type of operation and the address of the device involved.

The Central Processing Unit **1.10** under program control initiates all Input-Output (I/O) operations. Under program control the Central Processing Unit **1.10** may be held in synchronous operation with an In-

put-Output device or may be operated independently, after setting up the Input-Output operation. It also executes Input-Output Testing instructions under program control which are used for conditional testing of the Input-Output devices.

The Magnetic Core Memory **1.12** receives and transmits information between the Central Processing Unit (CPU) and any DSU **1.20** connected to the system. The Data Synchronizers **1.20** are used to control the flow of information and to pass information from the Tape Control Unit **1.20** to the Magnetic Core Storage **1.12** and upon instruction from the Central Processing Unit, information from a selected one of the Data Synchronizers information is processed from or to Core Storage with no further interference with Central Processing Unit operational flow. The Tape Control Unit (TCU) **1.30,** in turn, controls all operations to be executed by the Tape Drive Units **1.32** and each TCU is capable of controlling up to eight Tape Drive Units as shown. All information recorded in or read from the Tape Drive Unit passes through the Tape Control Unit where it is checked for errors, assembled into 36 bit binary words and transmitted to its channel in a Data Synchronizer **1.20.** Each of the Tape Drive Units **1.32** contains a pair of tape reels and each Drive Unit is capable of recording information on tape, reading information previously recorded on tape and performing positioning and control functions on the tape under control of the Tape Control Unit which are necessary to accomplish tape operations.

GENERAL DESCRIPTION OF OPERATION

Data flow through the system is traced with the aid of FIG. **1** where data comprises information which, temporarily, is not an instruction or command, even though, ultimately, it may in some other program routine, be interpreted as an instruction or command or part of either subject to modification by the machine or the program or a combination thereof. Data flows between the CPU **1.10** and the Magnetic Core Memory **1.12,** and the Core Memory **1.12** may receive or supply data to or from a Data Synchronizer Unit **1.20** when required for I/O operation, under which circumstances storage access is under DSU control. Tape data is passed between a selected DSU **1.20** and a selected TCU **1.30** in one or the other direction as the Tape Control Unit requires or supplies it, and the Tape Control Unit furnishes or receives data via busses to its attached Tape Units **1.32.** The particular Tape Control Unit must determine which Tape Unit is receiving or accepting information from the busses. Data is transmitted between the Tape Unit and the Tape Control Unit, in 7 bit information groups, while transmission between all other units is in full word or 36 bit form. One function of the Tape Control Unit is to assemble the 7 bit characters into 36 bit words.

Since the complete Data Processing System of this embodiment may consist of three Data Synchronizer Units **1.20,** each having two separate channels, the resultant system may contain six independent channels, all of which at a given time may be processing data. In so far as reading and writing tape is concerned, all six Tape Control Units may be in operation simultaneously transmitting information some in one direction, some in the other or all in the same direction. Thus, the Data Synchronizer effectively simulates a funnel whereby information from Input-Output units coming at asynchronous times relative to each other and to the synchronous period of the Central Processing Unit **1.10** are brought in and distributed in a linear relationship in the time domain. This is to say, the data are separated into sequential groups by the respective Data Synchronizers **1.20** so that access to the Memory is done on a sequential basis relative to each of the other DSU's and relative to the Central Processing Unit with respect to the Data Synchronizers.

CENTRAL PROCESSING UNIT

The Central Processing Unit **1.10** is basically a high speed electronic Calculator controlled by a program stored in Core Storage with instructions of the single address type. Every function of the machine is under control of such a stored program which allows the machine to execute instructions at the rate of about 40,000 per second. Furthermore, the functions of getting data into the Calculator from Input-Output Devices, Magnetic Core Storage **1.12,** and Magnetic Drum Storage **1.14** or transmission of data from the CPU to these respective devices are controlled by such a stored program. Internally, the Central Processing Unit operates in the pure binary number system but the Input-Output number systems may be the "IBM" code used in punched card systems, the decimal system, or the Binary Coded Decimal System (BCD) to name a few. The information from punched cards may be put on a magnetic tape, the tape may be used as a data source, or results of a computation in the CPU may be transferred to Magnetic Core Storage and then through a Data Synchronizer and Tape Control Unit to a Tape Drive Unit where the data is written on tape and at some later time this data can be read from tape and punched on cards or printed by peripheral equipment. When the capacity of the Magnetic Core Storage is not large enough, Magnetic Drum Storage **1.14** is used to store a supply of larger blocks of information for ready access at frequency intervals. When the amount of storage needed is in excess of the capacities of both Core Storage **1.12** and Magnetic Drums **1.14,** magnetic tapes may be used.

Stored programs may be written and introduced into the Core Storage in a number of ways. The instructions may be punched on cards in the "IBM" code and read into Storage by means of the card reader **1.28,** or they can be punched in cards in the pure binary number system and recorded on tape for entry into the machine therefrom.

It is to be noted that many of the basic elements of the Data Processing System, shown generally in FIG. **1** and more specifically in FIG. **2,** assume two stable states, (as described later) and are therefore particularly suited for the binary system of notation where one specified state is indicative of a binary 1 and the other state is indicative of a binary 0.

The basic unit of information, the word, consists of 36 binary bit positions and may comprise alphabetic, numeric, or symbolic, data or an instruction, or any pattern of 36 bits desired by the programmer for any reason. The layout for the **36** positions of a word is indicated schematically, in FIG. **3***a*, where S refers to the sign position; 1 refers to bit position 1; 2 refers to bit position 2; and so forth. Only when a word comprises numerical data does position S have algebraic significance. Under such usage, with position S containing a 0 the word is positive, and with position S containing

a 1 the word is negative. When a logical operation is performed upon the word, the word is interpreted as a 36 bit signless number.

Individual locations in Magnetic Core Storage and in the Magnetic Drum Unit and individual units, such as Magnetic Tape Units and all other Input-Output units, are identified by a system of numerical addresses. By means of a number contained in the address part of an instruction as described later, it is possible to refer to the information contained in any location in Magnetic Core Storage, the Magnetic Drum Unit or to any I/O unit of the system.

The Central Processing Unit **1.10**, data portions of which are shown in FIGS. **2***a–gg*, (along with instruction portions as described below) comprises a 36 order Storage Register, FIGS.**2***b–d*, comprising 35 orders and a sign order; a 36 order Adder plus one overflow order, FIGS. **2***j–u*; an Accumulator Register, FIGS. **2***x–cc*, of 35 orders plus 2 overflow orders P and Q and a sign order S; a Multiplier Quotient Register, FIGS. **2***dd–gg*, comprising 35 orders and a sign order, three Index Registers, FIGS. **2***f* and *g*, of 15 orders and their associated Index Register Controls, FIG. **2***f* for manipulation of the data contained the rein; an Indicator Trigger Register, FIG. **2***a*, of 36 orders; Storage Bus Switching, FIGS. **2***w–y*, of 36 orders coupled to a Storage Bus, FIG. **2***w–2y*, of 36 orders which is connected to Magnetic Core Storage shown in FIGS. **2***hh–ll*, and Operator's Entry Keys, FIG. **2***e* (FIG. **12**) of 36 orders. Associated with the data portion previously described is an Instruction Register, FIG. **2***h* (FIG. **13**) of 18 positions, S, 1 through **17**. Primary and Secondary Operation Decoders, FIGS. **14** and **15** are connected to the output lines of the Instruction Register, an Address Register, FIG. **2***i*, an Instruction Counter, FIG. **2***v*, and related Storage Address Controls including a Storage Address Register. Information may be placed in Core Storage from either the Accumulator Register of the CPU, its Multiplier Quotient (MQ) Register or its Indicator Register. It is the function of the Storage Bus Switches to switch the contents of the Accumulator Register, the MQ Register or the Indicator Register onto the Storage Busses and into Core Storage under control of certain instructions which require that information be located in Core Storage.

THE ARITHMETIC CONTROL SECTION OF CPU

The function of the arithmetic control section of the CPU is to determine what operations must be performed in the execution of each arithmetic instruction, and to sequence these operations. In order to perform this function, Execution Controls are provided, as illustrated in FIGS. **18** through **51**, for each arithmetic instruction, and arithmetic control mixing circuits or command circuits are also provided as illustrated in FIGS. **52** through **98** which take the information from the execution controls and provide gates or pulses to perform each required operation.

PROGRAM CIRCUITS

The information received from Core Storage by the Central Processing Unit is initially placed in the Storage Register, FIGS. **2***b–d*, prior to being operated upon by the program and arithmetic circuits. The registers and counters used to receive and decode the instructions comprising the program consist of the above mentioned Instruction Register, FIG. **13**, the Instruction Counter, FIG. **17**, the Primary Operation Decoder, FIG. **14**, the Secondary Operation Decoder, FIG. **15**, and related control circuits, FIGS. **99–111**. The Storage Address Register, FIGS. **129***a* and *b*, controls the addressing of the Core Storage Unit and is located in the unit it controls, that is, Magnetic Core Storage **1.12**, illustrated functionally in FIGS. **2***hh–2ii*. Each of the registers and counters is described individually with reference to its function in the overall flow of information and both general and specific timings are set forth later in connection with the receiving and decoding of instructions.

The input information to the execution controls is primarily the output of the Instruction Register, FIG. **13**, which is routed through the Primary Operation Decoder, FIG. **14**, and the Secondary Operation Decoder, FIG. **15**. The decoder output is often mixed with an indication of one of the following conditions to provide conditional operation: (1) whether an overflow has occurred in the Accumulator, (2) whether the carry output from column Q of the Adder is present, (3) whether the carry output from column **6** of the Adder is present, (4) whether the contents of the sign position of the Accumulator Register, the Storage Register or the Quotient Register is negative, or (5) whether the Shift Counter is at 0 or not. (The Shift Counter as described later is used to count E/R (Execute-Route) cycles for a Multiply or a Divide instruction and is also used to count the number of shifts in a Shifting instruction). The command circuits are provided with pulses or gates which circuits become the output command lines or control lines when they are conditioned by the outputs of the execution controls.

The Storage Register, FIGS. **2***b–d*, has inputs **12.01.01** through **12.01.36** to each of its positions S, 1 through 35 from respective ones of positions S, 1 through 35 of the Entry Keys, FIG. **2***e*. The Storage Register also has inputs **11***b*.**03** and **11***c*.**03** to positions 1 through 35 from corresponding outputs of positions 1 through **35** of Storage Bus Switching, FIGS. **2***w–y*. Another set of inputs **10.01S** through **10.01.35** is provided to the Storage Register Positions S, 1 through 35 from the outputs of the Indicator Register, FIG. **2***a*, positions O, 1 through 35. Outputs **5***a*.**04**; **5***b*.**06**; **5***c*.**04**; and **5***f*.**05** are provided from Storage Register, positions S, 1 through 35 to the input of positions O, 1 through 35 of the Indicator Register. Outputs **5***b*.**04** are provided from the Storage Register positions 1, 2, 8 and 9 to *Indexing Controls*, FIG. **90**. Outputs **5***b*.**07** from Storage Register positions 3 through 11 are provided to positions 1 through 9 of the Instruction Register, FIG. **2***h*, with additional lines **5***b*.**07.01** and **5***b*.**07.02** from positions 1 and 2 to the Instruction Register Pulse Generator, FIG. **99**. Furthermore, an additional pair of outputs **5***b*.**07** from Storage Register positions 1 and 2 are sent to the inputs **5***b*.**07.01** and **5***b*.**07.02** of the Instruction Register positions 8 and 9. Outputs **5***a*.**02S**; **5***b*.**03**: **5***c*.**08**; and **5***f*.**08** from Storage Register positions S and 1 through 35 are provided to respective positions S, 1 through 35 of the MQ Register, FIGS. **2***dd–gg*. Outputs **5***b*.**05** from positions 12 and 13 of the Storage Register, FIG. **2***c* are provided to *Indirect Addressing Controls*, FIG. **98**. Outputs **5***b*.**02**; **5***c*.**07**; **5***f*.**07** are provided from positions 1 through 35 of the Storage Register to respective inputs 1 through 35 of the Adder Register. Outputs **5***a*.**01** and **5***b*.**01** from positions S, 1 through 5 of the Storage Register, FIGS. **2***b–2d* are provided to

the inputs of positions 30 through 35, FIG. 2*gg* of the MQ Register. Outputs 5*c*.02; 5*c*.09; 5*f*.06 from positions 19 through 35 of the Storage Register are provided to the inputs of positions 1 through 17 of the Adder. Output 5*c*.01 for S position of the Storage Register 18 is provided to *Ones to Adder*, FIG. 81, Output 5*c*.06 is provided from positions 18 through 20 of the Storage Register, FIG. 2*d*, to *Index Register Hold Lines and Adder Control*, FIG. 49. Outputs 5*f*.01; 5*f*.03 are provided from positions 24 through 26 of the Storage Register, FIG. 2*d* to *Channel Select*, FIG. 153. Output 5*f*.04 from Storage Register positions 24 through 26, FIG. 2*d*, is provided to the Data Synchronizer Instruction Decoder, FIG. 160 and outputs 5*f*.02.24–26 are provided from positions 24 through 26 of the Storage Register to *Sense Unit Address Control*, FIG. 106. Outputs 5*c*.05.18–20 are taken from positions 18 through 20 of the Storage Register and are sent to *Index Registers to Address Gating Line*, FIG. 51.

The Adder Register has positions Q, P and 1 through 35 as previously described and inputs 81.01 through 81.10 are provided to positions Q, P, 1 through 8 from *Ones to Adder Control*, FIG. 81. Inputs 7*g*.01; 7*b*.02; 7*c*:02; 7*d*.02 are provided to positions Q, P and 1 through 35 of the Adder Register from positions Q, P and 1 through 35 outputs of the Accumulator Register, FIGS. 2*x–cc*. Inputs are provided to positions 3 through 17 of the Adder Register, FIG. 2*k–2q*, from positions 3 through 17 of the Index Register Mixing, FIG. 2*f*. Inputs are provided to Adder positions 6 through 17 from Drum Control of Drum Unit 1.14. Inputs 7*c*.03.30–34; 7*c*.03.35 are provided to positions 12 through 17 of the Adder, FIG. 2*k–2q*, from positions 30 through 35, FIG. 4*cc*, of the Accumulator Register, and inputs 8*a*.06; 8*b*.06; 8*c*.03 are provided to positions 12 through 17 of the Adder from positions 1 through 5, FIG. 2*dd*, of the MQ Register. Outputs are provided from the Adder as inputs to positions Q, P and 1 through 35 of the Accumulator Register. Outputs 6*b*.02; 6*c*.01; 6*d*.02; 6*e*.02 are provided from the Adder positions 1 through 8 to the input of positions 1 through 8 of the MQ Register. Outputs are provided from the Adder positions 3 through 17 to the inputs of each of the Index Registers A, B and C, FIG. 9. Outputs are provided from the Adder positions 3 through 17 to the inputs of the Address Register, FIG. 2*i*.

An output is provided from each lower order Adder position, FIGS. 2*i–u*, to the input of each higher order position as illustrated. For example, the carry output 6*h*.03, FIG. 2*u*, of position 34 of the Adder is connected to the input of position 33 of the Adder, the carry output of position 33 of the Adder is connected to the input of position 32 of the Adder, and in like manner similar carry lines are connected through position Q.

Output lines are provided from positions 3 through 17 of the Address Register, FIG. 2*i* (FIGS. 16*a* and 16*b*) as inputs to positions 3 through 17 of the Storage Bus Switches.

Inputs are provided to the Storage Bus Switching, FIGS. 2*w–y* positions S, 1 through 35 from the output of the MQ Register positions S, 1 through 35 and inputs are provided to Storage Bus Switching positions S, 1 through 35 from the outputs of the Indicator Register. An input 71, 01S, FIG. 2*w*, is provided to positions S of Storage Bus Switching from the output of position P, FIG. 2*aa*, of the Accumulator Register. Inputs are provided to the Storage Bus Switching positions 1 through 35 from positions 1 through 35 of the Accumulator Register and there is a connection 7*b*.01P between the output of position P, FIG. 2*aa*, of the Accumulator Register to the input of the S position, FIG. 2*w* of the Storage Bus Switching.

An output 11*a*.04S is provided from position S, FIG. 2*w*, of Storage Bus Switching to *Minus on Storage Register*, FIG. 77. Outputs 11*a*.02; 11*b*.04; 11*c*.04 are provided from the Storage Bus Switching positions S, 1 through 35 to Memory Buffer Register, FIG. 142. Outputs 11*a*.03; 11*b*.01; 11*c*.01 are provided from Storage Bus Switching positions S, 1 through 5, FIGS. 2*w–2x* to position P, 1 through 5, FIG. 2*j–2l*, of the Accumulator Register. Positions P, 1 through 35 of the Accumulator Register have outputs from each lower order position connected to the next adjacent higher order position terminating at the input of position P for the purpose of shifting left. There are outputs from positions Q, P, 1 through 34 of the Adder to the inputs of the next adjacent lower order position terminating with the output position 34 entering as an input of position 35 for shifting right. Position Q of the Accumulator Register has an output 7*g*.02Q to Carry Overflow Trigger, FIG. 123, and another output 7*g*.03Q to 2, Floating Point Overflow/Underflow Detection, FIG. 127. An output line 7*b*.07P is provided from position P of the Accumulator Register to Test Sense Input (not shown in the drawings) and another output 7*b*.08P to Floating Point Overflow/Underflow Detection Controls, position 1 of the Accumulator Register has an output 7*b*.01.01 to Adder 1 Carry to Accumulator Overflow Trigger, FIG. 80. Outputs are provided from the Accumulator Register positions P, 1 through 35 to the input of Storage Bus Switching positions S, 1 through 35 as previously described. Position 9 of the Accumulator Register has two output lines 7*c*.06,08 and 7*c*.07.09 to Column 9 Carry and Overflow Trigger, FIG. 124, and to Floating Point Add/Subtract Execution Controls, FIGS. 21*a* and 21*b*. An output 7*d*.08.35 from position 35, FIG. 2*cc*, of the Accumulator Register is connected to the input of position S, FIG. 2*dd* of the Multiplier Quotient Register, and another output 7*d*.07.35 is connected to position 1 of the MQ, FIG. 2*dd*.

Position S, FIG. 2*dd*, of the MQ Register has an output line 8*a*.06S to *Adder and True Complement Controls*, FIG. 6*k*, an output 8*a*.05S to *Floating Point Shift Control*, FIG. 83, and another output 8*a*.01.S to *SIGN Mixing*, FIG. 113. Position 1 of the MQ Register, FIG. 2*dd*, has an output 8*b*.03.01 to *Floating Point Shift Control*, FIG. 83, has an output 8*b*.02.01 FIG. 83, has an output 8*b*.02.01 to *Multiply Execution Control*, FIG. 20, and an output 8*b*.01.01 to *Sense Unit* Address, FIG. 106; Position 8, FIG. 2*ee*, of the MQ Register has an output 8*d*.01.08 to *Floating Point Shift Control*, FIG. 83. Position 9, FIG. 2*ff*, has an output 8*e*.02.09 to the Floating Point Shift Control, FIG. 83, and an output 8*e*.01.09 that goes to *Floating Point Round*, FIG. 106. Outputs 8*e*.06.34 and 8*f*.03.35 are provided from position 34 and position 35 to *Multiply Floating Point Trigger Shift Step*, FIG. 43. Output lines are provided from positions S, 1 through 35 for entry of the Drum 1.10 in FIG. 1. The output of each lower order position of the MQ Register is connected as an input to the next higher order position, for example, the output 8*f*.01.35 of Position 35, FIG. 2*gg*, is connected to the input of position 34 and so forth in like manner until the final connec-

tion is made between the output position 1 and the input of position S FIG. 2*dd*, of the MQ Register for left shifting. Furthermore, outputs are provided from each higher order position of the MQ Register to each adjacent lower order position beginning with the output 8*a*.04S of position S to the input of position 1 and ending in like manner with connections from the final one of the outputs 8*e*.03.34 to the input of position 35. A single input **68.01**, FIG. 2*gg*, is supplied to position 35 of the MQ Register from *One to MQ* Register, FIG. **68.**

Output lines are provided from positions 3 through 17 of the Address Register, FIG. 2*i*, to positions 3 through 17 of the Instruction Counter, FIG. 2*v*, and outputs are provided from positions 3 through 17 of the Instruction Counter as inputs to positions 3 through 17 of the Address Register. Inputs are provided from Address Reigster, FIG. 2*i*, positions 10 through 17 to the Instruction Register positions 10 through 17. An input is provided to position S of the Storage Register from **3.10.01** Primary Operation Decoder, FIGS. **14***a* through **14***d*.

CONTROL OF DATA FLOW

With reference to the Central Processing Unit, FIGS. 2*a*–*gg*, the flow of data is controlled in the following manner: Operator's Entry Keys S, **1** through **35**, FIG. 2*e*, via cable **12.01**, then in parallel by the individual wires of the cables **12.01S**, **12.01.01**, etc., to the Storage Register positions S, 1 through 35, FIG. 2*b*–*d*, to *Operator Panel Keys to Storage Register Control*, FIG. **73**, which controls entry into positions S, 1 through 35 of the Storage Register, FIGS. 2*b*–*d*, or instead under control of *Complement Indicators to Storage Register*, FIG. **97**; the Indicator Register S, **1** through **35** are fed from the outputs of the Storage Register positions S, 1 through 35 via a cable under control of the *Reset Indicators*, FIG. **93**, (see also FIG. 2*a*) *Set Indicators*, FIG. **94**, or *Invert Indicators*, FIG. **95**, controls. *Electronic Reset of Indicators Control* is also provided in FIGS. **92** (see line **92.01** and 2*a*).

Data may also be transferred from positions **1** through **35** of the Storage Bus Switching, FIGS. 2*w*–*y*, via a cable to respective inputs of the Storage Register, FIGS. 2*b*–*d*, under control of *Storage Bus to Storage Register Control*, FIG. **53.** Data is transferred via cable from positions S, 1 through 35 of the Storage Register, FIGS. 2*b*–*d*, to positions S, 1 through 35 of the MQ Register, FIGS. 2*dd*–*gg*, under control of *Storage Register to MQ Register Controls*, FIG. **63.** Outputs from positions S, 1 through 35 of the Storage Register, FIGS. 2*b*–*d*, are connected to positions P, 1 through 35 of the Adder Register, FIGS. 2*j*–*u*, for entry of data in response to operation of *Storage Register to Adder Control*, FIG. **54.** Data are also transferred between positions **18** through **35** only of the Storage Register, FIGS. 2*c* and *d*, to positions P through **17** of the Adder under control of *Storage Register* (18–35) *to Adder* (*P*–17) *Control*, FIG. **86***a*. Six positions of data (**1**-**5**) contained in positions S, 1 through 35 of the Storage Register, FIGS. 2*b*–*d*, may be entered into positions 30 through 35 of the MQ Register, FIG. 2*gg*, by means of *Convert Controls*, FIG. **36.** The negative of the contents of selected ones of the orders of the Index Register, FIGS. 2*f* and *g*, are provided to positions 3 through 17 of the Adder by means of *Index Register to Adders Gating Line*, FIG. **51.** True outputs of positions Q, P, 1 through 35 of the Accumulator Register, FIGS. 2*z*–*cc*, are transferred to positions Q, P, 1 through 35 of the Adders by means of the *True Accumulator to Adders Control*, FIGS. **55***a* and *b*. The complement of the Accumulator positions Q, P, and 1 through 35 are provided to positions Q, P, 1 through 35 of the Adder under control of *Complement Accumulator to Adder*, FIGS. **55***c* and *d*. Carry output of position P, of the Adder is provided to the input of position 35 of the Adder by means of *Carry to Adder* **35**, FIG. **56.** The contents of positions 3 through 17 of the Adders are supplied to selected ones of the Index Registers, FIGS. 2*f* and *g*, in response to operation of *Adders to Inde x Register Gating Line*, FIG. **50.** The contents of Adder positions 3 through 17 are transferred to the Address Register, FIG. 2*i*, in response to operation of *Address Switch* Input Controls, FIG. **110.** The contents of positions 1 through 8 of the Adders are transferred to positions 1 through 8 of the MQ Register, FIGS. 2*dd*, 2*ee*, in response to operation of the Adders **1**–**8** to MQ **1**–**8** Controls, FIG. **84.** The Contents of the Accumulator positions 30 through 35, FIG. 2*cc*, are transferred to the Adder positions 12 through 17, FIGS. 2*o*–2*q*, in response to operation of *Convert Controls*, FIG. **36.** The contents of positions S, 1 through 5 of the Storage Bus FIG. 2*u*, are entered in positions P, 1 through 5 of the Accumulator, FIGS. 2*aa*–2*bb*, in response of operation of Convert Controls, FIG. **36**, which contents of Storage Bus Switching may be from Accumulator Register, the MQ Register or the Indicator Register as specified by the controls of Storage Bus Switching. Storage Bus Switching, FIGS. 2*w*–*y*, is not a storage device in the sense that a register is and it merely transfers information from the Accumulator Register, the MQ Register and the Indicator Register to the Storage Busses. The contents of the Address Register, positions 3 through 17, FIG. 2*i*, may be placed in positions 3 through 17 of positions 21 through 35 of Storage Bus Switching, FIGS. *w*–*y*, in response to operation of *Address Switches to Storage Bus* **3**–**17** *and* **21**–**35** of FIG. **75.** The contents of the MQ Register may be transferred to the Storage Busses via Storage Bus Switching by means of *MQ Registers S*, **1**–**35** *to Storage Bus S*, **1**–**35** *Control*, FIG. **74.** The contents of the Accumulator may be placed on the Storage Busses via Storage Bus Switching by means of *Accumulator to Storage Bus*, FIG. **72.** The Instruction Register, FIG. 2*h*, is controlled by means of Shift Counter Pulse Generator **1** or Shift Counter Pulse Generator **2**, FIGS. **101** and **102.** Data on the Storage Bus may be entered into the MQ by means of *I/O Bus S*, **1**–**35** *to MQ Register Control*, FIG. **69.** A word from the Drum, FIG. **1.14** may be entered into the MQ Register positions S, 1 through 35 by way of the I/O Bus in response to operation of *I/O Bus, S*, **1**–**35** *to MQ Register S*, **1**–**35**, FIG. **69.** The contents of the Address Register, FIG. 2*i*, may be placed in the Address Register by means of the *Control Address Switch Input*, FIG. **110.**

CONTROL FLOW

There are two general types of control words, namely an Instruction and a Command, both having an operation part and an an address part. For the purposes of explanation an Instruction is defined as a configuration of 36 bits which is decoded by the decoder of the Central Processing Unit for the purpose of controlling an operation to be performed by the Central Processing Unit. This operation, if it be an Instruction for an Input-

Output type of operation, is transmitted to a Data Synchronizer channel. The second type of control word is known as a Command, and is similar to an Instruction except it enters certain registers of the Data Synchronizer Channel (described in detail later) through which it acts like an Instruction and controls that kind of an operation dealing with the transmission of data between a Data Synchronizer Channel and Core Storage. Commands are decoded by the Transmission Register in a DSC. The difference between the two is that Instructions enter and are decoded by the Central Processing Unit whereas Commands enter and are decoded by the Data Synchronizer Channel.

For a better understanding of the operation of the system, control is divided into two sub-control levels, namely, initial control and operational control, Initial control means those control functions necessary to initiate an Input-Output operation and originates in the Central Processing Unit while operational control comprises those control functions necessary to maintain operation once started and to insure a proper completion. For example, during a system operation a Central Processing Unit instruction is needed to initiate any tape operation. Once started, initial control is then passed to the Data Synchronizer conderned, then to the Tape Control Unit, and finally to the Tape Drive Unit selected. Once each unit has satisfied its initial requirement, the control is then held by the units necessary to complete the operation desired. It is seen here, that except for initial operation, the Central Processing Unit is needed in the tape operation for one purpose only, which is to provide the Data Synchronizer Channel access to Core Storage, when such access is needed. For any one tape system (Tape Control Unit and connected Tape Drive Units), this will occur no more frequently than once every 400 microseconds. The Central Processing Unit is otherwise free during this time to pursue its other activities while operational control rests with the Data Synchronizer, the Tape Control Unit and the Tape Drive Unit.

The major function of the operational control is to determine when the other units involved will perform their specific functions to accomplish the given overall operation. The function of the control logic circuits between the Data Synchronizer Unit and the Central Processing Unit is to determine when the Central Processing Unit will provide the Data Synchronizer with access to Core Storage, to store or obtain a word. The function of the control logic circuits between the Tape Control Unit and the Data Synchronizer unit is multiple: (a) It indicates to the Data Synchronizer Unit when the Tape Control Unit has a word ready or needs a word, (b) it indicates when an operation is completed and whether completed by the Data Synchronizer or the Tape Control Unit, and (c) it also indicates the occurrence of special conditions, such as an error. The function of the control logic circuits between the Tape Drive Unit and the Tape Control Unit is to indicate to the Tape Control Unit when the Tape Drive Unit is ready to perform an operation, when it is performing an operation, and when it has completed an operation. In each of the operational control functions, a complete interlock between all units involved is maintained until the operation is complete.

MACHINE TIMING

The fundamental machine cycle of the Central Processing Unit (CPU) is 12 microseconds. One cycle is the duration of Core Storage access time which is the time required by the Central Processing Unit to transmit to or receive a word of information from Core Storage. The time required to transmit information between the Core Storage and any of the Input-Output units via one of the Data Synchronizers is given later when the timing relationship of the Input-Output devices in relation to the basic machine cycles are discussed. The fundamental machine cycles may be Instruction (I) cycles, Execution (E) cycles, Execute-Route (E/R) cycles and B cycles, each of 12 microseconds duration. I cycles are required to make references to Core Storage to obtain Instructions and to distinguish instruction words from data words. Execution (E) cycles are required for the Central processing Unit and the Data Synchronizer Unit to make reference to Memory in order to bring data from Core Storage into the units or to enter words into Storage. E/R cycles are required by the CPU for operations *without* references to Core Storage. B cycles are references to Memory by the Data Synchronizer channel and differ from E cycles only in the manner in which they arise and the fact that the Central Processing Unit may not make reference to Memory during this time. There are particular cycles where references are made to Memory for the Central Processing Unit's purpose, but *Control Word* data is also stored in the Data Synchronizer Channel. Simply stated, the CPU and DSC do have access to Core Storage at the same time for certain instructions during I and E times but, of course, the only time that this is true is when the same information can be used or if it is common to both units.

The timing circuits comprise an Oscillator, FIG. **114**, which oscillates at a frequency of **1** megacycle and provides signals to an Inverted Sync Generator, FIG. **115**. The Inverted Sync Generator provides inverted sync pulses on one output and pulses on another output to the Inverted Clamp Generator and Clock Drive, FIG. **116**, the latter having two outputs, an inverted clamp line and a drive line to the Clock, FIG. **117**. The Clock provides the 12 master timing pulses, labelled Master **A0** through Master **A11** under control of the 1 megacycle oscillator by using a ring of 12 triggers fed by the oscillator in a manner well known in the art. The signals on the Inverted Clamp Line from FIG. **116** and the Inverted Sync Line, FIG. **115**, are special signals required by the Microsecond Delay and Storage Units in the Storage Register, Accumulator Register and MQ Register. The Inverted Synchronizing pulse on line **115.01** is a positive pulse having a duration of approximately 0.3 of a microsecond and the clamp pulse on line **116.01** is a negative pulse having a duration of approximately 0.02 microseconds. Both pulses are repeated at the megacycle rate of the Oscillator, FIG. **114**, and are in phase with each other which is necessary for proper operation of the Microsecond Delay Units as described hereafter. A Cycle Timer Control, FIG. **118**, utilizes inputs from various command controls and operation controls for providing outputs to a Cycle Timer Gate Generator, FIG. **119**, and to Cycle Timer Output Circuits, FIG. **120**. The Cycle Timer Output Circuits provide outputs **120.01**; **120.02** and **120.03** indicative of the type of cycle that the machine is to operate in, that is, whether the cycle shall be an instruction (I) cycle, Execution (E) cycle or Execute-Route (E/R) cycle and one and only one of the outputs indicative of I, E, or

E/R time is up at any time. Each output stays up for a minimum duration of one 12 microsecond clock cycle. The Cycle Timer Control, FIG. **118**, provides instruction signals to the Cycle Timer Output Circuits, FIG. **120**, Go to E Time, labeled **118.01**, Go to E/R Time **118.03**, and Go to I Time **118.14**. Other inputs are provided to the Cycle Timer Gate Generator, FIG. **119**, having outputs Reset Cycle Timer **119.01**, Set Cycle Timer **119.02**, and B Time Control circuits **119.03**. The B Time Control, FIG. **121**, has inputs from the Primary Operation Decoder, Instruction Register and certain other control and timing units for generating outputs concerning B time. A Pulse and Gate Generator, FIG. **122**, generates output signals in response to master timing pulses, type of cycle, and instruction controls.

When the Input-Output units are not being used the Cycle Timer Control follows this sequence: During the last machine cycle pertaining to a previous instruction, a signal is received by the Cycle Timer Control, FIG. **118**, indicating that the previous operation is complete and that the Central Processing Unit is to go to I time control for the purpose of interrogating Core Storage for the next instruction according to usual stored program techniques. When this has been accomplished, at Lead-In Instruction time (around 10 time in I time), the new instruction is decoded. Immediately following the decoding of this instruction, its type of instruction is known as well as whether or not another reference to Core Storage is required. For instance, if the instruction is Add this requires another reference to Storage to Core bring in the data to be added. Therefore, the Central Processing Unit is so controlled that its next machine cycle is an E cycle which provides a reference to Core Storage. In case of a Store instruction, the same would apply, except that this time the references to Core Storage would cause information to be moved from a register in the Central Processing Unit to Core Storage. During execution of some instructions, references to Core Storage may not be required as in the case of multiply, which does not require more than the initial reference to memory to get the multiplicand after which, a series of I/R cycles are required, in order to actually carry out the iterative addition and shifting by the Central Processing Unit in order to perform the multiplication. Only the initial reference to Storage is required.

In addition to the three basic cycles I, E and E/R there is the B (Buffer) cycle referred to previously which results from the inter-action between a Data Synchronizer Channel and the CPU requiring a reference to Storage. B cycles do not provide data simultaneously to the DSU and CPU but frequently data is sent to a DSC simultaneously with control information being sent to the CPU and vice versa.

INSTRUCTION COUNTER

The Instruction Counter, FIG. 2*v*, determines the address in Core Storage involved during an Instruction cycle. In the normal progress of the program, sequential addresses in storage are interrogated during successive I times because the Instruction Counter normally receives a pulse at the end of each operation to step it up 1 so that a succeeding higher numbered address is referred to on the next Instruction cycle. The orders of the Counter are labelled 3 through 17 in order to agree with the corresponding orders of the Address Register, FIG. 2*i*. The loading of the Instruction Counter occurs at the beginning of each Instruction cycle as will later be described and determines the address of the word comprising the next Instruction *except* in those I times following a Halt, a successful Transfer or Branch and in certain operations such as Skip which advances the Instruction Counter more than one to cause skipping of instructions.

INSTRUCTION REGISTER

The Instruction Register, FIG. 2*h*, stores and operates on the information normally received from Magnetic Core Storage as a result of an Instruction cycle until the instruction is completely executed when it is reset during the early part of the next instruction cycle prior to receiving a new instruction. At very **18** time of the Instruction cycle, a one microsecond pulse, (abbreviated D1) (see FIG. 2*h*) causes positions S, 1–9 of the Instruction Register to be reset to 0 and at the same time positions 10 through 17, and the Shift Counter of the Indicator Register, are reset to 1. The layout of the Instruction Register is as follows: Sign in position S,: primary operation, positions 1 through 5; secondary operation, positions 6 through 9; and advance or shift counter data, positions 10 through 17. The information read from the Storage Register, FIGS. 2*b–d*, into the Instruction Register includes the sign, the primary operation part, and the secondary operation part of the Control Word, while positions 10 through 17 of the Instruction Register receive information from the Address Register, FIG. 2*i*.

On a type A instruction (those that contain a prefix), bits 1 and 2 of the Storage Register are read into positions 8 and 9 of the Instruction Register. All B type instructions (those that do not contain a prefix) read positions 3 through 11 of the Storage Register into positions 1 through 9 of the INstruction Register. During the Instruction cycle, the sign bit in the Storage Register is transferred into the S position of the Instruction Register, where it has no algebraic significance but is used only to expand the capacity of the register, and, thus make it possible to decode more instructions.

PRIMARY OPERATION DECODER

Orders 1–5 of the Instruction Register, FIG. **13**, store the primary operation part of the instruction to be performed. The double outputs of each of these orders are analyzed in the Primary Operation Decoder, FIG. **14**, which resolves the five conjugate pairs of signals into one signal on one of 32 possible decoder output lines. Since only 32 outputs are available from the Primary Operation Decoder and 189 computer operations must be provided for, it is necessary to further employ the output of the Primary Operation Decoder by combining it with bits stored in other orders of the Instruction Register to expand the number of instructions over that offered by the Primary Operation Decoder.

SECONDARY OPERATION DECODER

A Sense type instruction has its primary code stored in the primary operation part of the Instruction Register while the *type* of Sense is stored in the secondary operation part. For example, in Read Select 0762, the 7 and the 6 are represented by bits in orders **1** through **5** of the Instruction Register while the 2 is indicated by a binary bit in column 8. Whenever an instruction with a primary operation code 7, 6 is decoded the secondary operation part of the instruction is sampled into the

Secondary Operation Decoder, FIG. **15**, to bring up a secondary operation output of (0,2). On the non-indexable instruction, column 8 and 9 of the decoder contain the prefix which was transferred from columns 1 and 2 of the Storage Register. Like the primary part of the Instruction Register, the secondary part is reset at **18** (DI) and read at **19** time.

ADDRESS PART OF THE INSTRUCTION REGISTER (SHIFT COUNTER)

The eight positions of the address part, FIG. 2*i*, of the Instruction Register form a count-down counter of eight triggers which has a capacity of 255 places. This counter is reset to 1 every **18** (D3) and on a Shift Instruction the number of places to be shifted is placed in the Shift Counter by turning OFF the appropriate triggers at **112** time. The Shift Counter is impulsed every microsecond under a machine cycle gate and as the counter goes to 0, it signals the end of the shifting operation. Similarly, shifting during Multiply, Divide and Floating Point operations are controlled by the Shift Counter.

When using a Sense of an Input-Output Unit Instruction, the Address part of the instruction is read into the Shift Counter at **112** time through the address Switch Controls and the output of the Shift Counter during this type of an Instruction are fed to the Class and Unit Select Matrices, FIGS. **149, 150**, which in turn feed the Class and Unit selectors, FIGS. **151–160.** It is pointed out that the Shift Counter is reset with all triggers ON and that zeros are then set into the counter to set it to its proper setting since the counter is of the count-down type and the normal reset and set of the counter would cause an erroneous carry.

ADDRESS SWITCHES

The Address Switches, FIG. **110**, sample either the Instruction Counter outputs or Adder outputs of positions 3 through 17. In order to store the Index Register in the decrement portion of the Storage Register or to display the effective address, it is necessary to route the Adder outputs 3 through 17 through the Address Switches to the Storage Bus Switches, FIGS. 2*w–y*.

SIGN MIXING CIRCUITS

The Sign Mixer Circuits, FIGS. **113**, combine all the outputs from the sign bits of the Storage Register, FIGS. 2*b–d*, the Accumulator Register, FIGS. 2*z–22*, and the MQ Register, FIGS. 2*dd–gg* to provide signals indicating that the signs are alike or unlike, and also provide signals from the Instruction Register, FIG. 2*h*, indicating when the Address counter reaches the desired count during a Multiply or Divide operation.

SUMMARY OF TIMING CONSIDERATIONS

Every I time the information from Storage is operated on as an Instruction and the location interrogated during the Instruction cycle is selected by the Instruction Counter, FIG. 2*v*. When the End Operation Trigger comes on near the end of the last cycle of the previous operation the contents of the Instruction Counter are gated through to the Address Register, FIG. 2*i*, at I (D1) time. The contents of the Address Register at this time indicate the location in Storage that is to be interrogated for a new Instruction. At I2 (D1) time, the contents of the Address Register are delivered to the Storage Address Register, FIG. 2*hh* (FIG. **129**), of the Core Storage Unit.

When the Storage Address Register has received the address and instruction, it controls the interrogation of the specified location as described later and at I4 3/4 (D 1/2) time transfer its contents to the Storage Bus from **15** to CT **0.5** of next cycle. At 17 (D1) the information on the Storage Busses is transferred into the Storage Register, FIGS. 2*b, c, d*. In preparation for the decoding of this Instruction, the Instruction Register is reset at I8 time. If there is a bit in Storage Register positions 1 or 2 then data in these positions 1 and 2 are transferred to the Instruction Register positions **8** and **9** at I9 (D1). However, if no bit is present in Storage Register positions 1 or 2, then the bits in Storage Register orders 3 through 11 are set into the Instruction Register positions 1 through 9 at I9 (D1) time. Regardless of the condition of orders 1 and 2, the content of the sign (S) position of the Storage Register is transferred into the Instruction Register S position at I9 (D1). The instruction code is thus received by the Instruction Register at I9 time and is decoded by the Primary Operation Decoder, FIG. **14**, from **I9.5** until the succeeding I8 time. The output of the Primary Operation decoder prescribes commands for various arithmetic and logical operations and because of the large number of types of Instructions and the limited capacity of the Primary Operation Decoder, it is necessary to use also outputs **6** through **9** of Instruction Registers along with the outputs of the Primary Operation Decoder for decoding purposes.

The number stored in the Instruction Counter, FIG. 2*v*, is advanced by 1 at I11 (D1) to effect the interrogation of the next sequential Core Storage address during the succeeding I cycle. This is the normal advance and the advance is only suppressed in special cases as stated above. By this time the program circuits have caused the decoding of the Instruction which controls the types of cycles to follow I time and the Instruction Counter is set for the next sequential address.

When the instruction has been completed, a command line End of Operation control, FIG. **128**, is brought up to turn ON the End Operations Trigger, FIG. **118**, at **10** time of the last cycle of the operation which signals the Cycle Timer to proceed to I time and bring out the next instruction.

OVERFLOW AND CARRY TRIGGERS AND CONTROLS

In FIG. **123** there is shown two triggers, one for storing the fact that an Overflow has occurred and the other for storing the fact that a Carry out of column Q of the Adder has occurred. A pair of triggers are used in FIGS. **124**, one for indicating the presence or absence of a carry into position **9** of Adder and another trigger for indicating the carry out of column 9. In FIG. **125**, there is shown a pair of triggers, one for indicating Floating Point Overflow and the other for indicating Floating Point Underflow. There is shown a trigger in FIG. **126** which has an input from a predetermined Adder depending upon the size of Core Storage that is used in the system. In this instance, there is a Carry output from Adder 6 to this trigger. Although Locate Drum Address, LDA, is not used in the explanation of this embodiment of this invention and is not explained in detail, the fact that Locate Drum Address is not used

is pertinent to the extent that the associated controls are down.

In connection with Floating Point Overflow and Underflow detection, circuits of FIG. 127 provide outputs indicative of Floating Point Overflow and Minus on Adder Q sum. In FIGS. 128 *a*, *b* and *c*, there is shown the control circuits for End Operation, Storage End Operation in E R time and End Operation in E time.

WORD FORMAT

FIG. 3*a* shows the layout of a type A instruction. These instructions use positions S, 1 and 2 for an operation code and are characterized by having a 1 in positions 1 and/or 2. All other instructions contain zeros in both positions 1 and 2. Instructions Transfer on Index T1X, Transfer on No Index TNX, Transfer on Index High TXH, Transfer with Index Incremented TXI, and Transfer on Index Low or Equal TXL use positions 3 through 17 as a decrement part, positions 18 through 20 as an index tag, and bits 21 through 35 as an address part. The index tag selects the Index Register, FIGS. 2*f* and 2*g* as the one whose contents are to be modified and tested by the instruction. The decrement contains the modifications or test amount and the address specifies the storage location of the next instruction if the test condition is met. Another of these instructions uses only S, 1 and 2 and bits 3 through 35 have no effect on the execution of the instruction.

The format of a type B instruction is shown in FIG. 3*b*, the shaded part representing the field not used by all type B instructions. These instructions are characterized by having an operation part in S, 1 through 11 (1 and 2 contains 0's), an index tag in 18 through 20 and an address part in 21 through 35 for Shift Instructions. Positions 12 and 13 are used as an indirect address tag by all type B Instructions except non-indexable, shift, input-output, variable multiple and variable divide instructions. Positions 14 and 15 are not used by type B instructions.

FIG. 3c shows the format of the type C instructions. Type C instructions use S, 1 through 9, as an operation part, (and 2 contains 0's), 10 through 17 as a count, 18 through 20 as an index tag and 21 through 35 as an address part. Three of these instructions, Variable Length Multiply (VLM), Variable Length Divide or Halt (VDH) and Variable Length Divide or Proceed (VDP) are indexable and use the index tag for address modification. Convert by Replacement from Accumulator, (CVR), Convert by Replacement from MQ, (CRQ) and Convert by Addition from MQ, (CAQ) are not indexable and use position 20 of the index tag to indicate that the base address of a count cycle is to replace the contents of index register A. The number of convert cycles, the number of bits in the multipler, or the number of bits to develop in the quotient is specified by the count. While the count field has a capacity of 255, a count larger than 47 may cause indirect addressing to take effect on VLM, VDH, VDP but not on Convert Instructions since such a count places bits in positions 12 and 13. Bits through 21 and 35 specify the storage location of the operand or the base address of the first convert cycle.

FIG. 3d shows the format of type D instruction. Type D instructions operate in conjunction with columns 0 through 17 or 18 through 35 of the Indicator Register, FIG. 2*a*. The 18 bit mask used in Sense Indicator instructions is contained in the positions 18 through 35 of the instruction. Positions S, 1 through 11 contain the operation part with 1 and 2 containing zeros. Position S is used to denote whether the left columns (0 through 17) or right columns (18 through 35) positions of the Indicator Register are used in the instruction. If S contains a 1, the left positions are used, and if S contains a 0, the right positions are used.

In FIG. 3*e*, the format of type E instructions is shown. These are defined by plus or minus 0760 in positions S, 1 through 11, do not contain an address part, and use positions 24 through 35 as part of the operation code. Address modification through an index register is specified by positions 18 through 20.

Data Synchronizer operation makes use of three word formats as shown in FIGS. 3*f* and 3*g* and 3*h*. Word formats of FIGS. 3*f* and 3*g* illustrate an instruction word (Control Word) sent to DSC from storage and FIG. 3*h* illustrates a word sent from a DSC to storage. The normal DSC control word specifies the number of words to be transmitted (Word Count) in positions 3 through 17 and specifies the initial storage location in positions 21 through 35 to which data is to be sent or taken from. DSC control is specified by positions S, 1, 2 and 19 and the use of these positions for DSC control are described in detail hereafter. The special DSC control word in FIG. 3*g* is a word which modifies the sequential location of other control words for the Data Synchronizer as described later. Positions S and 1 contain 0's, position 2 must contain a 1 and position 19 contains a zero. Positions 21 through 35 give the location of the next control word to be used by the DSC.

FIG. 3*h* shows the format of an instruction word when a Store DSC instruction is executed. The storage location from which the next control word is taken is specified in positions 3 through 17 (location). The storage address of the next word of data is specified in positions 21 through 35 (Address).

FIG. 3*i* illustrates the layout of a Floating Point instruction. The magnitude of the binary fraction is given by positions 9 through 35 and the sign of the binary fraction is given in position S. The binary characteristic of the fraction (binary exponent + 128) is stored in positions 1 through 8.

In FIG. 3*j*, a Fixed Point instruction is illustrated. In fixed-point arithmetic, the 36 bit word in storage is interpreted as containing a sign in S and a 35 bit magnitude in positions 1 through 35. In logical operations, the word is treated as a 36 bit unsigned quantity.

In FIG. 3*k*, a six character binary coded data (BCD) word format is indicated. It will be discussed in some detail later.

The Central Processing Unit distinguishes between instructions and data information by the type of cycle selected. Words read out of memory, during an instruction cycle, are channeled to the Instruction Register where the stored manifestations of the bits comprise a representation of the instruction. Information read from memory during an execute cycle is always handled as numeric data.

AUTOMATIC ADDRESS MODIFICATION

When an iterative program operates on different items of data during each step of the iteration, it is necessary to change the addresses of instructions which further refer to this data, before each iteration. Without the use of automatic address modification, instruc-

tions which change the addresses of other instructions may constitute a large number of instructions in a given program. When the address of the instruction is brought to the Storage Address Register, it passes first through the Adders and Address Switches. If indexing (address modification) is desired the 2's complement of the amount in one of a chosen of the Index Registers is brought into the Adders at the same time in positions 3–17. The result of this adder operation is that the Address Switches receive the difference between the address and the contents of the selected Index Register and this difference is known as effective address. The execution of the instruction proceeds in the usual manner using the effective address. Each Index Register serves as an accumulator register so that its contents can be increased and decreased by the execution of certain indexing instructions. The Index Register can receive information from either the decrement portion or the address portion of the instructions, from the Accumulator or from the Instruction Counter and it can send information to Adders for address modification, to the Accumulator or to Storage. Selection of an Index Register is made by bits in storage register locations **18, 19** and **20.** Further address modifications may be had by providing bits in positions 12 and 13 in the Storage Register. By means of controls, FIG. **98,** the contents of the address in Core Storage referred to are not added, but instead the address found at this Storage location specifies the location from which data are to be added to the Accumulator. Both of these addresses may be indexed by the same or different Index Registers, each word containing its own tag in positions 18, 19 and 20. Indirect addressing may be used with all indexable transfer instructions and with all other indexable instructions which make a reference to Storage.

MAGNETIC CORE STORAGE ORGANIZATION

Referring now, in general, to FIGS. *2hh* through *ll* and specifically to FIGS. **129** through **147,** the Data Processing System employs a three dimensional Magnetic Core Storage Device and associated storage controls. Outputs from the Address Register, FIG. *2i* and DSU Address Switches, FIG. *2ww*, are provided as inputs to a Storage Address Register shown in FIG. *2hh*, the specific logical contents of which are shown in FIG. **129.** Certain timing pulses are provided to a Pulse Generator shown generaly in FIG. *2jj* and specifically in FIGS. **130***a*, *b* and *c* which provides output signals to the Memory Address Register, FIG. *2hh*. The Memory Address Register provides outputs to an X Address Decoder, FIGS. **131***a* and **132***b*, and to Y Address Decoder, FIGS. **132***a* and **131***b*. Both the X and Y Address Decoders have outputs to respective ones of a pair of Read Bias and Write Gate Mixing Circuits, FIG. **133.** Timing pulses are provided from a Read-Write Gate generator, FIGS. **134***a* and *b*, to the Gate Mixing Circuits; to the X and Y Address Decoders, FIGS. **131***a* and **132***b* and **132***a* and **131***b*, respectively; and to the Read Bias and Write Gate Mixing controls, FIG. **133.** Output lines **133.01** and **133.02** are provided from Read Bias and Write Gate Mixing circuits to the inputs of an X Matrix Switch Write Driver, FIG. **135.** Outputs **131A.01–08** are provided from the X Address Decoder to an X Matrix Switch Read Driver, FIG. **136,** and outputs **131***b***.0.–08** are provided from FIG. **131***b* to Read Bias and Write Gate Mixing Circuits, FIG. **133.** Connections are made via FIG. **135** between Gate Mixing, FIG. **133,** and an X Driver Matrix Switch, FIG. **141***a*. The 64 output lines of this X Driver Matrix Switch are provided as inputs to the Core Array, FIG. **138***a*, each output drives one of 64 X drive lines in the array as indicated in FIG. **138***a* when that driver line has been addressed. Outputs are provided from a Read Bias and Write Gate Mixing, FIG. **133,** to the Y Matrix Switch Write Driver, FIG. **139,** and outputs are provided from the Y Address Decoder to the Y Matrix Switch Read Driver, FIG. **140.** Connections are made according to FIG. **133** between the Address Decoder, FIG. **131***a*, and an Y Matrix Switch, FIG. **139.** Outputs **132A.01–08** are provided as inputs to the Y Matrix Switch Read Driver, FIG. **140,** and connections are made according to FIG. **140** to the Y Driver Matrix Switch, FIG. **137***a*. Sixty-four Y Drive lines of Y Matrix Driver Switch, FIG. **137***a*, are provided to the Core Array, FIG. **138.** Thirty-six digit windings shown in FIG. **138** are provided to inhibit the writing of a 1 in a selected core as will be described in detail later.

Communications with Core Storage from either the Central Processing Unit or Input-Output devices are made through a Sense Amplifier Buffer and Input-Output Switching Register, FIGS. **2–11** (FIG. **142**). Outputs **142A.03**; **142A.04**; **142A.05**; **142B.03**; **142B.04**; **142C.03** and provided to Storage Bus Switching, FIGS. *2w–y* (FIGS. *11b, c, d*) and **36** output lines **142.01** are provided as inputs to a Digit Plane Select Circuits FIG. **143.** Thirty-six outputs of the Digit Plane Select Circuits are provided to a Digit Plane Driver Unit, FIG. **144**; the latter having **36** digit plane dirve outputs which are connected to the Core Array, FIG. **138,** as previously described. With the energization of a selected X and Y line, outputs from cores at the selected address are present at the Sense windings of the Core Array to the input of the Sense Amplifier Buffer and I/O switching, FIG. **142.** Control lines are provided to the Sense Amplifier Buffer and I/O Switching, FIG. **142,** by way of an Address and Operations Control, FIG. **145** and, in turn, by way of Read-Write Control, FIG. **146.** (Adders and operations control are part of CPU) (Inputs to the Adders and Operations Control are from the Central Processing Unit and are shown specifically in FIG. **145**). Inputs are provided to the Test Circuits shown generally as FIGS. **147***a, b* and *c* from the Sense Amplifier Buffer and I/O Switching Register and from the Pulse Generator, FIGS. **130***a* and *b*. An undestanding of the Test Circuits is not necessary for an understanding of the invention. Accordingly, no specific details are mentioned except in those instances where a control line is operated as an incident to the operation of Core Storage.

In FIG, **138,** there is shown a diagrammatical view of a Core Array in which cores are arranged in square arrays such that each core is situated at the junction of two mutually perpendicular single turn windings that are called the X and Y windings. If I is the minimum current necessary to change a core from the "zero" state to the "one" state then if current I/2 is supplied to the single X and a single Y winding, the only core which can change state is the one at the intersection of these two windings. Four windings actually pass through each core and are called the X, Y Digit and Sense Windings as shown in FIG. **138**b. The planes are stacked vertically to form a three dimensional array of **36** planes, each X or Y winding being connected in series with the corresponding X or Y winding in the planes above or below it. Currents of I/2 are applied to one X and one Y winding and a vertical line of cores

is selected at the intersection of the planes at which the X and Y windings lie. The Digit and Sense windings, however, are not connected between the various planes. The process of reading information from the selected vertical line of cores leaves that line of cores of **36** positions in "zero" state and, therefore, to prevent the loss of the information read out it becomes necessary to write "ones" in those cores which has previously contained "ones." This process is accomplished producing magnetizing currents for writing "ones" in the entire line of cores, but whenever a "zero" should appear, an inhibit signal is returned to the plane associated with that digit from the digit winding to cancel a portion of the magnetizing effect which suppresses the writing of a "one" in that plane. More specifically, during the Write cycle the Core Plane Address to be written first receives a Read pulse which changes the full address of **36** positions to "zero. " The Sense winding output is suppressed at the output of the Sense Amplifier which prevents setting the Storage Buffer triggers to the contents of the Address which has been read from. At Write time the Read in sample together with the Storage Bus outputs either turns on the Buffer Triggers for those outputs containing a "one" or leaves it off as in the case of reading a "zero." After the Buffer Triggers have been set, the Write current is setn to all **36** cores of the Address to be written tending to cause all "ones" to be read into that Address. Where "zero" is to be written into a particular core the writing of the "one" is suppressed by the Storage Buffer Lines **142***a*.01S through **142***a*.01.11; **142***b*.01.12; **142***b*.01.23; **142***c*.01.24; **142***c*.01.35 which go to the Digit Plane Select Circuits of FIG. **143** to bring up the Digit Plane Select lines **143.01S** through **143.01.35** to inhibit "ones" from being written into respective planes associated with each Digit Plane Select winding. Since a Write operation is always preceded immediately by a Read operation during any selection of a Memory Address, the selected core is always in a "zero" state when writing starts. To write a "zero" into a core the X and Y windings are each pulsed simultaneously with current of +I/2 and the Digit Plane winding receives an inhibit pulse of −I/2 which results in a net of +I/2 to the core which is insufficient to switch the core from "zero" to the "one" state.

READ AND WRITE OPERATION

A Store Instruction is one that writes the contents or partial contents of a Central Processing Unit Register at an address in Core Storage, specified by the Store Instruction. This is commonly referred to as Writing. Other instructions cause the contents of some Addresses in Core Storage to be read out and sent to the CPU for the purpose of adding, subtracting and so forth, depending upon the instruction, and this is referred to as Reading. For example, the instruction Store +0601 with an Address of 0700 (octal) is assumed to be located at Address 0777 (octal) in Core Storage. The Instruction Counter in the Central Processing Unit, FIG. **2***v*, normally tells the machine where to go in Core Storage during an Instruction cycle and get the next instruction and in this example, contains the Address 0777 (octal) in the positions indicated below;

Instruction Counter Positions	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Contents	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Until **16** time the output of the Instruction Counter feeds the Address Register, FIG. **2***i*, the Central Processing Unit and the contents thereof are transferred into the Address Register at **10** (D1) time. At B time, the contents of the Address Register positions (FIG. **2***i*) 6 through 17 or the contents of the DSU location Register are transferred to the Storage Address Register, FIGS. **2***hh*, located in Magnetic Core Storage. Each position of the Storage Address Register, FIG. **129,** has three outputs, making the total of 36 and is divided into four major divisions as shown schematically in FIG. **148**a: the group of bit positions 6, 7 and 8 comprise the Thousands position; 9, 10 and 11 comprise the Hundreds; 12, 13 and 14 comprise the Tens; and 15, 16 and 17 comprise the Units. Each of these four groups has six outputs **129***a*.01–**129***a*.12 and **129***b*.01–**129***b*.12, labeled 6, $\overline{6}$, 7, $\overline{7}$ and so forth. The Address Decoder, FIG. **132** *b*, decodes positions 6, 7, and 8; Address Decoder, FIG. **131***a*, decodes positions 9, 10 and 11; Address Decoder, FIG. **131***b*, decodes positions 12, 13 and 14; and Address Decoder, FIG. **132***a*, decodes positions 15, 16 and 17. The address contained in the Storage Address Register and placed in the Address Decoders is 0777 (octal) and accordingly, in FIG. **132***a*, Storage Address Register **15** line **129***b*.08 is up; Storage Address Register **16** line **129***b*.10 is up; Storage Address Register **17** line **129***b*.12 is up; Storage Address Register $\overline{15}$ line **129***b*.07 is down; Storage Address Register $\overline{16}$ line **129.09** is down; Storage Address Register $\overline{17}$ line **129***b*.11 is down; and when the Read Gate line **134***a*.02 comes up, Read Address **7** line **132***a*.01 is up since all inputs to its AND circuit are up. In FIG. **131***b*, Storage Address Register **12** line **129***b*.02 is up; Storage Address Register **13** line **129***b*.02 is up; Storage Address Register **14** line **129***b*.04 is up; Storage Address Register $\overline{12}$ line **129***b*.01 is down; Storage Address Register $\overline{13}$ line **129***b*.03 is down; Storage Address Register $\overline{14}$ line **120***b*.05 is down. Address **70** line **131***b*.01 is up since all the inputs are up to its AND circuit. In FIG. **131***a*, Storage Address Register $\overline{9}$ line **129***a*.07 is down; Storage Address Register **9** line **129***a*.08 is up; Storage Address Register $\overline{10}$ line **129***a*.09 is down, Storage Address Register **10** line **129***a* .10 is up; Storage Address Register $\overline{11}$ line **129***a*.11 is down; and Storage Address Register **11** line **129***a*.12 is up. When the Read Gate line **134***a*.03 comes up, an output is provided on Read Address **700** line **131***a*.01, since all the inputs to its AND circuit are up. In FIG. **132***b*, the Storage Address Register **6** line **129***a*.02 is down; the Storage Address Register **7** line **129***a*.04 is down; the Storage Address Register **8** line **129***a*.06 is down; Storage Address Register $\overline{6}$ line **129***a*.01 is up; Storage Address Register $\overline{7}$ line **129***a*.03 is up; Storage Address Register $\overline{8}$ line **129***a*.05 is up. Accordingly, an output is provided on on Address 000 line **132***b*.08 since all of the inputs to its AND circuit are up. The outputs from the Tens and Thousands Decoders, FIGS. **131***b* and **132***b*, respectively, are available as soon as the Storage Address Register is read into at I2 (D1). However, the Units and Hundreds Decoders await a Read Gate pulse on lines **134***a*.02 and **134***a*.03 from the Read and Write Gate Generator before their outputs are up. This allows time to set up the

biasing of the Switch Cores before the Selected Switch Cores are actually transferred. The outputs **131*b*.01** and **132*b*.08** for the Tens and Thousands Address Decoders are sent to read Bias and Write Gate Mixing circuits, FIG. **133**, and here their outputs are logically inverted for providing from each of these circuits seven lines which are up and one which is down. The seven lines that are up from the Read Bias and Write Gate Mixing circuits for the Thousands Address Decoder are sent to the X Switch Core Matrix, FIG. **135**, and the seven lines which are up from the Mixing circuits from the Tens Decoder are sent to the Y Switch Core Matrix, FIG. **139**. As shown in Timing Chart, FIG. **148*b***, both Switch Core Matrices are biased and a Read Gate Line comes up at approximately **13.5** time which allows the Units and Hundreds Address Decoders, FIGS. **132*a*** and **131*a***, to select the correct Switch Core in both the X and Y Matrix.

With reference to FIG. **138**, the Read-Out of a 36 bit word from the 36 sense windings to the Buffer Register, FIG. **142**, is accomplished by the use of Switch Cores shown in FIGS. **137** and **141**. Since each of the 36 Core Planes in the Core Storage Unit is a 64 × 64 Array the Two Switch Core Matrix Panels are used to provide 64 X Drive lines and 64 Y Drive lines as shown in FIG. **138**, at the top of the figure. FIGS. **137*a*** shows an 8 × 8 Switch Core Matrix having 64 Y Drive Address lines which go to the Core Array shown in FIG. **138**. The cores shown diagrammatically in FIG. **137*a*** are each identified by an Address shown thereon and are illustrated in detail in FIG. **137*b***. The Switching Cores have a substantially rectangular hysteresis loop with a Read winding having terminals identified by the numbers 1 and 9, a Write winding having terminals identified as 4 and 6 and a Secondary winding having terminals 7 and 8 with the polarities as indicated by the dots shown in the figure. When the Write winding is energized, the switch core remains magnetized in the state representative of "zero"; and when current is provided to the Read winding, the switch core is magnetized in the opposite sense indicative of a "one". A switch core is said to switch when current is provided in the Read winding sufficient to cause a residual magnetism to change from "zero" to "one". Likewise, sufficient current in the Write winding switches the core from "one" to "zero". A magnetizing force applied through the Write winding has very little effect on the core already magnetized in that direction and a magnetizing force applied to the Read winding has little effect on a core already magnetized in that direction. The Write winding provides the biasing force which, when used simultaneously with a mangetizing force applied on the Read winding, prevents the core from switching due to cancellation of the flux.

The line pairs coming from the Y Matrix Switch Read, FIG. **140**, are related to the Units position, of the Address as previously mentioned, FIG. **148*a***, so that the lines associated with the Units position Address are up and the other seven pairs of lines associated with the Non-Selected Units Address are down. For example, the Read Address 7 line **132*a*.01** is up providing an input to the Matrix Switch Read Amplifier of FIG. **140** bringing up the Read Driver input line to the Matrix Switch Driver, which provides current through the line **104.01**. In FIG. **137*a***, the Matrix Switch Read Driver Address (7) line **140.01** is up which provides current through the series Read coils of the Switch Cores terminals **1** and **9** of Address Cores **77, 67** and so forth through terminals **1** and **9** of Address (07) Switch Core and from the **9** terminal back to the Read Address **7** Feedback line **140.02**. The Read Address Feedback line is returned to the Y Matrix Switch Read Driver of FIG. **140**. In this regard, it is pointed out that current flows from a negative d.c. potential at the cathode to plate of the Matrix Switch Driver through the Read windings in series and through the Feedback line to the cathode of the Matrix Switch Read Amplifier and to ground through the lines **140.03**, shown in FIG. **140**. Since the cathode of the Matrix Switch Driver is at a negative potential of 130 volts essentially positive B+ is provided to the Matrix Switch Driver. Thus, the Read windings of the Switching Cores Address **77, 76, 57, 47, 37,** and **27, 17** and **7** are carrying magnetizing current sufficient to cause a residual magnetism to change the state of from "zero" to "one".

Referring now to FIG. **131*b***, the Tens Address Decoder, Address line **131*b*.01** for Address **70** is up to the Write Driver Select circuits, FIG. **133**, but the Write Gate line **134*b*.03** is not up until about **19** time. However, the Address **70** line is up and inverted to an AND circuit at the more negative level. Even though the Read Bias Gate line **134*a*.01** is up there is no output from the AND circuit since the inverted Address **70** line is down.

With reference to the Address Decoder, FIG. **131*b***, it will be noted that although the **131*b*.01** line is up that the other seven lines **131*b*.02** through **131*b*.08** are down. Accordingly, in the Write Driver Select circuits of FIG. **133**, the output of the Write Driver Select circuits for the Address **70** is down, and the outputs of the Write Driver Select circuits for the Addresses **60, 50, 40, 30, 20, 10** and **0** are up. Therefore, with reference again to FIG. **133**, the Address lines **131*b*.02–08** being down provides outputs which are up from the inverters and the Read Bias Gate line **134*a*.01** is up at **12** near the beginning of the cycle providing outputs on lines **133.01** and **133.02** for Matrix Switch Write Driver lines for the Addresses **60, 50, 40, 30, 20, 10** and **0** as shown in FIGS. **137*a***. In FIG. **137*a***, it will be noted that the Matrix Switch Write Driver Address line **70** is connected to the 4 terminal of the Address **77** core and that the 4 and the 6 terminals are those terminals for the Write coils which are connected in series from the Address **77** core through the Address **70** core. The 6 terminal of the last mentioned core is connected to the Write Address **70** Feedback line as shown. As previously mentioned, the Matrix Switch Write Driver Address **70** line is down and accordingly, current is not provided to the Write coils of the series-connected Switching Coils of Addresses **77–70**. However, current is supplied to the Write coils of the other rows of Address Switching cores by way of the Matrix Switch Write Drive Address **60, 50, 40, 30, 20, 10** and **0** lines as mentioned previously with regard to the Write Driver Select circuits of FIG. **133**. In summation, the Address Switching cores **77, 67, 57, 47, 37, 27, 17,** and **7** have their Read coils energized; the Switching Cores Addresses **67, 57, 47, 37, 27, 17** and **07** also have their Write coils energized; the net effect on the last mentioned cores is that they are not switched, but the Address Core **77** is switched since it has only read current supplied. The Switching Cores **66–60**; **56–50**; **46–40**; **36–30**; **26–20**; **16–10**; and **6–0** receive current through their Write Coils which tends to switch the core from

a "one" to a "zero". However, since the last mentioned cores are already at that state the magnetizing force is ineffective to change that state. The Switching Cores Addresses **76, 75, 74, 73, 72, 71** and **70** have neither the Read nor the Write coils energized so that no change of state takes place. The Switch Core Address **77** has only the Read coil energized as previously described and is switched from "zero" to "one." This change of state from a "zero" to a "one", in effect induces a voltage in the secondary winding which is felt on the Y Drive Address **7** line which goes to Core Plane, FIG. **138,** and provides +I/2. Similarly, the Hundreds Address is decoded, FIG. **131***a*, and provides an input on line **131***a*.**01** to the X Matrix Switch Read Driver, FIG. **136,** to bring up the Read Address **700** Matrix Driver. The Thousands Address Decoder of FIG. **132***b* inverts the Selected output **132b.08** in FIG. **133** to provide one pair of output lines associated with the Address **0000** which is down and seven pairs associated with Addresses **7000–1000** which are up to the X Matrix Switch Core panel, FIG. **141.** Specifically, Matrix Switch Write Driver Addresses **7000, 6000, 5000, 4000, 3000, 2000** and **1000** are up whereas the Matrix Switch Write Driver Address **0** is down and the Switch Core Addresss **0700** is the only core which can change from the "zero" to the "one" state. This change is felt on the X Drive Address **0700** line which provides +I/2 to the Selected X Drive line. Thirty-six cores are acted upon since each X or Y winding is connected in series with the corresponding X or Y windings in the planes above or below it. A Sense winding is threaded through all the cores in each plane so that in FIG. **138** there are two terminals for the Sense winding for each plane and there are two terminals provided to the Sense Amplifier Buffer Register, FIGS. **142***a*, *b* and *c*. More specifically, two terminals from each of the 36 planes are applied to the input of the primary of the transformer, as shown in FIG. **62,** U.S. Pat. Application Ser. No. 592,545, filed July 6, 1956, title: Data coordinator now U.S. Pat. No. 2,960,683 issued Nov. 15, 1960. For each plane having a "**1**" an output is provided from the Sense Amplifier to the AND circuit having two other inputs Read Control **146.03** and Read-Out Sample **130***a*.**07.** For a "1," an output is provided through the OR circuit and Cathode Follower to turn on the Buffer Register Trigger. When a "**0**" is being read, there is no output from the Sense Amplifier and accordingly, the trigger remains in a state indicative of a "zero". Since the Read-Out is destructive and the location (0777) specified by the Address now contains "zero," it is required that the word written out into the Buffer Register be read back into the Address specified (**0777**).

It will now be described how "ones" are written in those cores of Adress **0777** which had previously contained "ones" and which are now contained in the Storage Buffer Register, FIG. **211** (FIGS. **142***a*, *b*, *c*). This operation is accomplished by setting up circuits for writing "ones" in the entire line of cores, but in those positions in which a "zero" should appear, an inhibit signal is returned to those planes associated with the "zero" digits by way of the individually associated Digit Plane windings, which causes suppression of the writing of "ones" in those planes. The timing of the Inhibit Gate is shown in the Timing Chart, FIG. **148***b*. After the Read-Out Operation, the X and Y Switching Cores corresponding to the Address from which the information was read are in the "one" state. That is, they have been switched to provide an output in the Secondary which drives the cores in the Selected vertical line, FIG. **138,** from the "one" to the "zero" state to provide an output from the Sense windings indicative of the values contained in the selected 36 cores. To write the information contained in the Buffer Register back into the Core Array, advantage is taken of the fact that the Switch Cores for the Address Read-Out are now in the "one" state. During Write time all inputs to the Read Windings, FIGS. **136** and **140,** of the Switch Core Matrices, (FIGS. **137** and **141**) are suppressed by a Read Gate lines **134***a*.**02** and **134***a*.**03** (FIGS. **132***a* and **131***a*.). This is to say that the Read Gate provided on the line **134***a*.**02** to the Address Decoder circuit in FIG. **132***a* and the Read Gate provided on the line **134***a*.**03** to the Address Decoder circuit in FIG. **131***a* are down. Accordingly, there will be no output from either the Address Decoder, FIG. **131***a*, or the Address Decoder, FIG. **132***a*. The outputs of the Thousands Address Decoder, FIG. **132***b*, and the Tens Address Decoder, FIG. **131***b*, are not inverted. With reference to FIG. **133,** for example, the Read Bias Gate on line **134***a*.**01** is down which prohibits the passage of the inverted output from the Address line, but the Write Gate on the lines **134***b*.**03** is up which brings the selected one of the Read Bias or Write Address lines which output is provided to the X Matrix Switch Write Driver Address (**0000**) lines of FIGS. **135** and **141.** Similarly, the output of the Tens Address Decoder, FIG. **131***b*, is passed through Read Bias and Write Gate Mixing, FIG. **133,** and is provided as an input to the Y Matrix Switch Write Driver Address (**70**) line of FIGS. **139***a* and **137***a*. With reference now to the Y Driver Matrix Switch, FIG. **137***a*, it will be noted that the inputs from Y Matrix Switch Read Driver, FIG. **140,** are all down and that the only input to the Y Driver Matrix Switch is on the Matrix Switch Write Driver Address **70** from FIG. **139.** Recalling now that the address (**77**) Switch Core was the only one which was changed from the "zero" to the "one" state, it is apparent that the application of current to the Write coil causes the Address Switch core **77** to switch from the "one" to the "zero" state. However, other Switch cores are not affected in this manner since they are already in the "zero" state and the magnetizing force applied is therefore ineffectual to cause a significant voltage in the Sense Output winding or Secondary Output winding. These, of course, are the cores having Addresses **76, 75, 74, 73, 72, 71** and **70.** Accordingly, an output is provided on the Y Drive Address **77** line of FIG. **137***a* to FIG. **138.** Similarly, with reference to the X Driver Matrix Switch, FIG. **141***a*, the inputs from the X Matrix Switch Read Driver, FIG. **136,** are down and the only input from X Matrix Switch Write Driver, FIG. **135,** is provided on the Matrix Switch Write Driver Address (**0000**). It is pointed out that this provides the Write current to the Write coil of Switching Core Address **0700** which is the only core in the X Driver Matrix Switch Array which has been changed from the status of "zero" to "one." Therefore, this core when provided with a Write current in the absence of the Read current switches from "one" to "zero" and the voltage induced in the Secondary winding is provided on the X Drive Address line **0700** to the Core Array of FIG. **138.** Since a current of +I/2 is provided to a selected one of the Y Drive lines and a current of +I/2 is provided to selected one of the X Drive lines shown in FIG. **138** each of the thirty-six cores in the

vertical line selected would normally be switched from the "zero" to the "one" state. However, through the use of the 36 digit plane windings, selected ones of the cores which were normally in the "zero" state prior to reading out will be preserved in the "zero" state in the following manner:

With reference to the Sense Amplifier Buffer Register and I/O Switching, FIGS. **142***a*, *b* and *c*, it will be noted that there is provided a line **142***a*.**01**, **142***b*.**01** and **142***c*.**01** which is Storage Bus Trigger (N) OFF. Accordingly, when each Trigger in The Buffer Register is in the OFF condition as indicated by conduction of the right-hand side of the Trigger, the left-hand side is OFF with the plate at its higher positive potential which is interpreted on the output lines Storage Buffer Trigger (N) OFF as the "OFF" condition, and these outputs are provided from the Buffer Register to the Digit Plane Selector circuits, FIG. **143.** The inhibit Gate comes up at **I8.5** and for each of the 36 positions containing a "zero" in the Buffer Register an output is provided from the Digit Plane Select circuits on selected ones of the lines **143.01.S** through **043.01.35.** The outputs are provided to the Digit Plane Driver in the manner shown in FIG. **144** for driving the Digit Plane windings shown in FIG. **138** for those of the 36 positions containing "zeros." The current provided to the Digit winding is sufficient to cancel the total effect of the current provided to the Y and X Drive lines since I/2 is provided to each of the X and Y Drive lines (which is the current required to switch the core) and the current provided to the Digit Plane winding is sufficient to overcome at least a portion of this current thereby prohibiting the switching of the core from the "zero" to the "one" state on Writing operation. When a word is to be written into Core Storage in response to a Store instruction, the operation proceeds almost as previously described with respect to a Read instruction. However, before a Write pulse can be generated from the Switch Cores, the Switch Cores associated with the selected address must be placed in a Write status and this can be done by causing the proper Switch Cores to first provide a Read current. Therefore, for a Write cycle the Core Plane Address to be written first receives a Read pulse which causes the contents at the Address specified to be all "zeros" in all 36 positions. Output signals will be present on those Sense Windings having a core change from the "one" to the "zero" state but these are suppressed at the output of the Sense Amplifier since the Read-Out Sample line **130***a*.**07** is down. At this time the selected Switching Cores of the X Matrix Switch and the Y Matrix Switch have been switched from the "zero" to the "one" for providing outputs to the Selected vertical line of cores causing them to change from a "one" to a "zero". Information is present on the lines **142***a*.**02**, **142***b*.**02** and **142***c*.**02** from the Storage Bus or in the alternate is present on the DSU Storage Bus **142***a*.**06**, **142***b*.**05**, **142***b*.**04.** When the Read-In Sample signal is provided on the line **130***a*.**05** together with the Write Control signal on **164.02** the trigger is turned ON for those positions having "ones" present at the inputs (that is, having the input lines up).

After the Buffer trigger has been set, the Write current is sent to all thirty-six cores of the Address to be written which causes all "ones" to attempt to read into that Address. Where "zero" is to be written into a particular core the writing of a "one" is suppressed by the Storage Buffer Trigger OFF line **142***a*.**01**, **142***b*.**01** or **142***c*.**01** in the the manner previously described. The Buffer Register triggers are reset by way of the lines **130***b*.**01**, Reset Storage Address Register and Buffer Register between 0.5 and 1.0 time.

COMPONENT CIRCUITS

A detailed description of the principles of operation of a Magnetic Core Storage device may be had in U.S. Pat. application, Ser. No. 592,545, filed July 6, 1956, now U.S. Pat. No. 2,960,683 issued Nov. 15, 1960. A detailed description of a Central Processing Unit of the parallel binary type is described in copending application "Electronic Data Processing Machine" of Jerrier A. Haddad Ser. No. 419,642, filed March 30, 1954, now U.S. Pat. No. 2,974,866 issued Mar. 14, 1961 and includes basic instructions and typical circuits for causing their performance. Especially applicable are FIGS. **1***b*, **1***d*, **1***f* and **1***g*, which correspond generally to devices employed in the present invention. Other operations, particularly those utilizing Input-Output units such as magnetic tapes are disclosed in the copending application, Ser. No. 401,648, Bartelt el al., filed Dec. 31, 1953, now U.S. Pat. No. 2,850,234 issued Sept. 2, 1958 and in copending application, Ser. No. 401,502, of Bartelt el al., filed Dec. 31, 1953, now U.S. Pat. No. 2,921,293 issued Jan. 12, 1960. Further description may be had with reference to similar arithmetic elements in "IBM" Type 701 Computer, by H.D. Ross, Proceedings of the I.R.E. Vol. 41, pages 1287–1294, October 1953.

The Storage Register, Accumulator Register, and Multiplier Quotient Register are composed of microsecond delay units which are storage units having the particular capacity of being able to accept information and transmit information at the same time. These units are described in detail in U.S. Pat. No. Re. 23,699. The Adder and True Complement controls comprise 35 full Adders and two half Adders of the type explained in detail with reference to FIGS. **7***b* and **7***c* of application Ser. No. 419,642 referred to previously. The True Complement controls are those circuits that control the input to the Adders and consist of switching circuits and inverters. The switches control the time of entry of a word into the Adder and also determine whether the digits pass through the Inverter or not. Thus, a word entered into the Adders may be either true or complement. The Indicator register is composed of triggers of the bistable multivibrator type which remain in one or the other of two stable states until forced by external signals to assume the other state. The trigger is said to be ON when its left side is conducting, and therefore its left side is called the "ON side" and the right side is the "OFF side". In this instance, a trigger is said to be storing a 1 when ON and a 0 when OFF. In this embodiment of the invention, circuits are arranged to operate at voltage levels at a −30 volts and a +10 volts. When a line is referred to as being in the Down condition, it is to be assumed that the line is at a −30 volts, and conversely when a line is said to be in the *UP* condition it is to be assumed that the line is at a +10 volts potential.

Circuits employed in the practice of this invention have been designed to function in a 1 microsecond period which has been the usual period employed in similar machines by the assignee of this application since the Type 701 Computer was introduced. Computer

type circuits are used throughout the patent applications to which reference is made and a detailed explanation of the circuits themselves and of the modifications thereof are not considered necessary because of the present state of the art. Throughout the description of operation no reference is made to passive elements such as to cathode followers, level setters and the like. It is obvious that the characteristics of these elements vary and are largely determined not only by the component load but also by the length of conductors coupling one circuit to another.

MAGENTIC TAPE AND DSC ADDRESS SYSTEM

In FIG. **1**, the Core Storage **1.12** is connected to the Tape Units **1.32** by way of the latter's Tape Control Unit **1.30** and the Data Synchronizer Channel **1.20** associated therewith. Similar to separate locations in Core Storage, each Tape Unit, DSC or other Input-Output devices has an address. The combination of two addresses, i.e., the Input-Output device designation and its related DSC designation, specifies a particular Input-Output unit. To start a Tape Unit for reading or writing, a Select instruction must be given. The instruction Read Select (RDS) prepares the tape for a reading operation and the instruction Write Select (WRS) prepares it for writing. If the address of the instruction is used as a five digit octal number, then the first and second low order digits specify the Input-Output unit, the third specifies the class (tape, card, etc.), the fourth digit the data synchronizer channel the third and second, the mode (B-BCD) for tape only, and the highest order digit of the five is not interpreted. The specific numerical addressing system used by the tapes and Data Synchronizer Units is as follows: DSC's A through F are identified by the octal numbers 1 through 6 respectively occupying positions 24 through 26 of the instruction. In the Binary Coded Decimal mode, Tape Drive Units **1** through **8** are identified by the octal numbers 201 to 210 respectively occupying positions 28 through 35 of the Magnetic Tape and DSC Address System Instruction. In the pure Binary mode, Tape Units **1** through **8** are identified by the octal numbers 221 to 230 respectively, occupying positions **28** through **35** of the instruction. An example would be if the instruction RDS 01202 (octal) is executed, Tape Drive Unit **2** indicated by numbers 202 attached to Data Synchronizer Channel A indicated by numbers 01 is selected and started for reading operations in the Binary Coded Decimal Mode indicated by numbers **20.** If the instruction WRS 04221 octal is given, Tape Drive Unit **1** indicated by 221 attached to DSC Channel D indicated by 04 is selected and started for writing in the Binary mode indicated by **22.**

INPUT-OUTPUT CONTROLS

As described previously Input-Output devices may be selected on the basis of their Address to perform a function according to the Instruction given, and where any of the devices have multiple channels, each channel within the device may be selected when the proper instruction is given. FIGS. **149** through **158** are concerned generally with the Selection controls and Instruction controls for a specified Input-Output device. In particular a Class Decoder, FIG. **149,** has for its purpose of decoding of a portion of the Instruction Register positions 10 through 13 as modified by outputs of the Secondary Operations Decoder (FIGS. **15***a*, *b*) to provide outputs according to the class of operation, for example, Tape, Punch, Printer, Sence Printer, and so forth. A Unit Select Matrix, FIG. **150,** has inputs from positions 14 through 17 of the Instruction Register (FIGS. **13***a*, *b*, *c*) with outputs to the various units for their selection according to the code. Thus, according to the address of the unit, it may be selected by the bit configuration in their positions. An I/O Selection Interlock, FIG. **151,** performs an interlock function between Drum Read and Write Select or Not-Drum Read and Write Select. A Unit Selector, FIG. **152,** further decodes the output of the Unit Select Matrix FIG. **150** to provide a specific output for a numbered Input-Output Unit. A Channel Selector, FIG. **153,** provides outputs for the selection of Data Synchronizer Channels A through F according to the Channel address. With reference to FIG. **1,** where three Data Synchronizers are shown, each having two channels, it will be noted that the Channel Selector provides outputs for Channels A through F. An interlock Test Skip Control, FIG. **154,** provides two outputs, the one of primary interest concerning Input-Output End Operation Control. An Enter Execute Control, FIG. **155,** performs an Input-Output function in specifying when to go to Execute type of cycle. An End Operation Mixing Control, FIG. **156,** provides I/O End Operation Control and DSU End Operation. The Disconnect Synchronizer, FIG. **157,** (has for its function a control of Input-Output devices) at the termination of the operation disconnects the devices according to specific timing relations.

As mentioned previously, the only Input-Output device which provides storage directly to the Central Processing Unit and not through Core Storage is the Drum which communicates with the Central Processing Unit by way of the MQ Register, FIGS. 2ee, ff, gg (FIG. **8**). The MQ Reset and MQ Read In Control Circuits, FIG. **158,** control the entry and exit of data from the Drum to various ones of the registers of the Central Processing Unit, by way of the MQ Register and the Input-Output Bus which connects the MQ Register to the Drum Unit **1.14** (FIG. **1**).

FIGS. **159** to **162** disclose circuits for the control of Input-Output devices generally and more specifically the DSU's and Tape Control Units. A Tape Control, FIG. **159,** determines whether the mode of operation will be Binary or Binary Coded Decimal and a DSU Instruction Decoder, FIG. **160,** provides still further decoding of the Instruction to give a Beginning of Tape Test or an End of Tape indication. A DSU Conditional Transfer Control, FIGS. **161***a* and *b*, are decoders to provide specified control signals from the DSU to the Tape Control Unit. A Channel Control, FIG. **162,** provides indications at its output of whether or not channels are in use as the result of inputs from the DSU and TCU.

There are four registers in each DS Channel which control its operation, and are similar in function to the control registers in the Central Processing Unit and they will be described presently. The first command of any DSC program must be sent to the DSC by means of a Reset and Load instruction and the address part of this channel instruction specifies the location in Core Storage containing the DSC command. When this channel instruction is executed in the carrying out of this command, the contents of the location in Core Storage specified by the Reset and Load channel instruction are sent to the four DSC control registers

mentioned above. These control registers, one of which comprises three registers, are as follows:

WORD COUNT REGISTER (WR)

The contents of positions 3 through 17 of any DSC command so selected by the Reset and Load Channel Instruction are loaded into a Word Count Register, FIGS. 2*oo* or 2pp (FIG. 163) of the channel specified. This register specifies the number of words to be transmitted between Core Storage and the Input-Output units selected and also counts. As each word is taken from or entered into Core Storage, the contents of this Word Count Register is reduced by 1. The word counter comprising this register is unique from other registers in that it is a counter which steps down for each word moved and furthermore there is sensing circuitry which determines when the word counter has gone to "0". It is a Nines Complement-plus-one Counter and information is entered in complement form and a "one" is automatically added thereto. Outputs for indicating "zero" are taken from lines 163a.01.

ADDRESS REGISTER (AR)

The contents of positions 21 through 35 of this DSC command selected by Reset and Load Channel Instruction are loaded into an Address Register, FIG. 2*mm* or 2*nn* (FIG. 164). This register specifies the location in Core Storage from which the data word is introduced during writing or to which it is to be entered during reading. The contents of this register are increased by 1 after each transmission of a data word to or from Core Storage. Thus, the Address Register directs the transmission of words into or from consecutive locations of Core Storage. Actually, the Address Register and the Word Count Register may be thought of as two parts of a three part Control Word Register included in each Data Synchronizer Channel, where one part is the word count part of 15 bits mentioned previously, the seconnd part is the address part of 15 bits and the third part of this Control Word Register consisting of the Operation Register (Indicator Triggers), FIG. 2*eee*, whose triggers store the operation codes comprising the 4 bit configuration of positions S, 1, 2 and 19 of the Control Word. This latter Operation Register of Indicator Triggers of which there is one for each DSU Channel is shown generally in FIG. 2*eee* and in detail in FIGS. 165*a* to *c* and is so designated the Operations Register (OR) since it stores the indication of the type of operation. More particuarly, it indicates what is to be done with the data being transferred between Core Storage and the involved Input-Output Unit and is similar to the Instruction Register in the Central Processing Unit. Positions S, 1, 2 and 19 of the DSC command as indicated above are loaded into this register with bit positions S, 1 and 2 providing an indication of eight possible DSC operations, which may be executed during either reading or writing, while position 19 is used only for a reading operation.

LOCATION REGISTER

The second of the four register in each DSC is a Location Register (LR) FIGS. 2*pp* or 2*qq* (FIGS. 166*a–d*) which contains the location of the current DSC command plus 1 and which receives and stores the contents from the Core Storage Address Register, FIG. 2*hh*, and steps plus 1 which is then the address in Core Storage from which subsequent control words will be taken. This stepping occurs each time a control word for the channel is received by the Data Synchronizer Channel. The Location Register in each channel is like a program counter or instruction counter similar to that in the General Processing Unit. In summation, the Word Counter the Address Register and the Indicator Triggers of the Operation Register are concerned with data while the Location Register is concerned with commands. The initial control word is always provided by Reset and Load Channel instruction from the Central Processing Unit but further control words from Core Storage are received by the Data Synchronizer without the Central Processing Unit providing any address or even telling the Data Synchronizer Channel when it should go and get a new one. This control within the Data Synchronizer Channel which is described in detail later depends upon the use of the Indicator Triggers of the Operation Register in conjunction with the word count and also such signals as End of Record or End of File from the I/O Unit.

DATA REGISTER

A Data Register (DR), FIGS. 2*ss* or 2*tt* (FIG. 167) comprises the third register of the DSC and is a 36 bit register similar to the Storage Register (SR) in the Central Processing Unit. Just as the Storage Register serves as a buffer between Core Storage and the Central Processing Unit internal arithmetic devices, the Data Register in the DSC serves as a buffer between Core Storage and Input-Output units. In other words, this is a trigger-buffer register which temporarily stores information from Core Storage or from an Input-Output unit until it may be transmitted to an Input-Output unit or to Core Storage. In the case of tape operations as described later, a Tape Control Unit attached to the channel has a similar register with the exception that the latter is a Shift register for the reasons which will be discussed hereinafter.

THYRATRON REGISTER

A fourth register of a DSC is a Thyratron Register of 36 positions S, 1 through 35, FIG. 2*uu* (FIGS. 168*a* and *b*) and is provided for only one of the channels in each Data Synchronizer, namely, Channels A, C, and E. This register is used for storing data temporarily and controls the punching of the data to be entered in a card by the Punch or controls the data to be printed out by the Printer. Each of the 36 positions has two thyratrons, one for a calculator exit left operation and the other for a calculator exit right operation, making a total of 72 positions for transfer of two 36 bit words in parallel.

DSU STORAGE BUS SWITCHING

Thirty-six positions of DSU Storage Bus Switching, FIG. 2*vv* (FIGS. 169*a* and *b*) are provided for each Data Synchronizer Unit as opposed to 36 Storage Bus Switching positions for each of the two channels of a DSU. Storage bus switching is provided for moving the data which comes in from Core Storage to various ones of the registers of the Data Synchronizer previously described. Fifteen positions of DSU Address Switching are provided corresponding to positions 3 through 17 of the Address Register and are shown in FIG. 2*ww* (FIG. 170). After describing the data paths, the operation of the DSU Address Switching and the DSU Stor-

age Bus Switching will be explained, but, at this time, it suffices to say that DSU Storage Bus Switching receives both instructions and data from Storage, FIG. **211**, and the 15 positions of the DSU Address Switching receive information from the DSU Location Register, FIG. 2*qq* or 2*rr*, and as stated above from the DSU Address Register, FIG. 2*mm* or 2*nn*. By means of this Address Switching, the Data Synchronizer may call upon Core Storage to provide a word located at an address specified by the Address Register in the Data Synchronizer or the Central Processing Unit may control the supply of a word to the Data Synchronizer by sending an address from the Instruction Register in the Central Processing Unit to the Memory Address Register in the Core Storage Unit. Accordingly, both the Central Processing Unit and the Data Synchronizer have access both to the Memory Address Register, FIG. 2*hh*, in Core Storage and to the Sense Amplifier Buffer and I/O Switching Register, FIG. **211**, which is the output of or the input to Core Storage as the case may be.

SELECTION CONTROLS FOR THE DSU

In FIGS. **171** through **181**, Selection Controls are shown which concern Data and Non-Data Class selection and Unit selection for both the A and B Channels. More specifically, FIG. **171** illustrates the controls for Channels A and B Class Selection Interlock; FIG. **172** is the Channel A and B End Operation Synchronizer; FIGS. **173** and **174** are for Channel A and B Data Class Selection respectively; FIG. **175** is the Data Class Selection Interlock Control; FIGS. **176** and **177** are Channel A and B Non-Data Class Selection respectively; FIG. **178** is the Card Machine Selector and Disconnector; FIGS. **179***a* and *b* are Channel A Unit Selectors for one through eight Tape Drive Units; FIGS. **180***a* and *b* are Channel B Unit Selectors for eight Tape Drive Units; and FIG. **181** is the Printer and Punch Sense Outputs.

COMMAND AND INDICATOR CIRCUITS

In FIGS. **182** through **189** logical circuits are shown which illustrate generally the command controls the indicators which modify certain of the BSU operations. More specifically, FIGS. **182***a* and *b* are Command Decoding Circuits; FIGS. **183** and **184** respectively are Beginning of Tape Indicators (Load Point Indicators) and End of Tape Indicators; FIG. **185** is Channel A and B Tape Check Indicators; FIG. **186** illustrates circuits for Tape End of Record (EOR), End of File and Reselect controls; FIG. **187** is the End of File Indicator (EOF) Circuits; FIG. **188** SLC and RLC End Operation Check; and FIG. **189** is the DS Store, Skip and Conditional Transfer Controls.

ENTRY KEYS AND AUTO-MANUAL CONTROLS

FIGS. **190** through **193** disclose the Entry Keys of the Data Synchronizer and the controls for both automatic and manual operation. FIG. **190** illustrates only one of the Entry Keys, of which there are 36 (S, 1–35); FIGS. **191***a*, *b* and *c* illustrate Auto-Manual Controls, Normal Controls, and Manual I/O Controls respectively; FIG. **192** shows circuits for continuous Storage Read-In and Read-Out (Channels A and B); and FIG. **193** illustrates Entry Key to Storage Bus Controls.

READ AND WRITE CONTROLS

FIGS. **194** through **205** are concerned with the controls for reading and writing tape and mode controls for both binary coded words (BCD), binary words and also A and B cycle controls.

FIG. **206** discloses circuits for establishing priority between two channels only. FIG. **207** discloses circuits for binary and octal decoding of a portion of a word. FIGS. **208** and **209** are logical circuits for priority operations among all of the channels.

DATA CONTROL

FIGS. **210** through **224** are concerned with the transfer of data to and from the DSU and control of DSU operations, for example, Storage Bus to Data Registers in FIG. **212**, and Address Register to Storage Address Register, FIG. **213**.

In FIG. **211**, Channels A and B Store Sample Control the transfer of data from the Operation Register and the Location Register to Storage Bus Switching.

In FIG. **212**, Storage Bus to Data Registers and Data Registers to Storage Bus control the flow of data through Storage Bus Switching to Data Registers and vice versa.

In FIG. **213**, the Address Register to Storage Address Register controls transfers of the contents of the selected Address Register to Address Switching, FIG. **170**, and then to the Storage Address Register, FIG. 2hh.

The Control Circuit of FIG. **214** is for the purpose of transferring the contents of the Location Register FIGS. 2*qq* and 2*rr* to the Storage Address Register, FIG. 2hh. The transfer of data from the Storage Bus to the Control Registers, the Operation Register or the Indicator Trigger Register, the Address Register and the Location Register is accomplished by the Storage Bus to Control Register Controls, FIG. **215**. Transfer of the contents of the positions S through 17 only of the Storage Bus to the Word Count Register is controlled by the Storage Bus S through 17 to Word Count Register and Load Control Trigger, FIG. **216**. Step Control Registers, FIG. **217**, provide an output for stepping the specified Word Counter, FIGS. **200**, 2*pp*. The Channels A and B Word Gate and EOR Synchronizing, FIGS. **196***a* and **196***b*, controls the distribution of the word received from Core Storage to the Address Register, the Word Counter, the Indicator Register, and the Data Registers and also controls the flow of data from the DSU to Storage.

BUFFER CYCLES

There are three occasions in which Buffer or B cycles (described later) may be captured from the CPU by a Data Synchronizer channel. The *first* of these is when an instruction is near its completion in the Central Processing Unit and the next step normally would be to go to I time to get the next instruction. However, if a B cycle is required at this time by the Data Synchronizer, the I time will not take place, but is delayed until after a B cycle has been taken by the Data Synchronizer channel. The *second* occasion concerns the gaining of entry to Core Storage by any Data Synchronizer Channel, for a sharing type of action. This is the case where the Central Processing Unit is doing a multiply or divide or similar iterative instruction containing a large number of E/R cycles which do not require reference

to Core Storage by the CPU, and the Data Synchronizer may capture a B cycle simultaneously with an E/R cycle. This means, then, that the Central Processing Unit is not being interrupted either logically or in the time domain and that the DSC is using Core Storage while the CPU is doing some other operation not requiring such use. The *third* occasion involves capturing a B cycle on the part of the Data Synchronizer and is of the interrupt type. Certain instructions in the CPU require frequent and alternate references to Core Storage. The cycle format of such an instruction might be as follows: I, E, E/R, E, E/R, E, E/R, E, E/R and E. In this case, it is not possible to share an E/R cycle because information still remains on the Storage busses during E/R time, and therefore the busses cannot be used by the Data Synchronizer. In operations of this type, it becomes necessary to interrupt or break in between CPU cycles of an entire operation since the sequences are long and data would be lost if the Data Synchronizer waited until the entire operation was executed before interrupting. A B cycle is captured and the continuation of the current instruction in the CPU is interrupted until said B cycle is complete and the Data Synchronizer Channel has been served.

It should be noted that on the first and third occasions described above the calculator is slowed down or interrupted for a finite period of time, on the second occasion described above, the CPU actually shares real time with the DSU and occurs when the CPU does not require reference to Storage. Therefore, the Data Synchronizer may on this second occasion use Core Storage without logical or time interference with the CPU.

MAJOR DSC CONTROL WORDS

There are three types of major control words which may be stored in the Data Synchronizer channel. The words are distinguished by the state of the Indicator bits in positions S, 1, 2 and 19 of the Control Word, FIG. *3h*, which bits are interpreted by the ON and OFF states of the triggers in the Operation Register, FIG. *2eee*. The first of these Control Word types is characterized by the fact that Indicator **2** is not ON. S or 1 both may be ON and Indicator **19** may or may not be ON and the three may be ON or OFF in any combination. In this type of control word, the Indicator S when ON alone describes the following type of operation: With this type of Control Word, any record signals such as End of Record from an Input-Output unit are ignored and the word count exclusively controls how many words are to be transmitted from the Input-Output unit to Core Storage, except, of course, in the event that an End of File (EOF) indicator occurs. In the latter case, an unconditional disconnect of the unit results. Assume that the number of words recorded on tape is greater than the word count, that information flows from the Tape Drive Unit selected, to Core Storage, through this channel, until the word count has been reduced to 0, and that the S indicator is ON. When the word count has been reduced to "0," the Data Synchronizer channel goes directly to the location specified in Storage by its Location Register to bring in a new control word which then enters the Data Synchronizer channel and replaces the contents of the Control Word Register. Tape motion continues and additional data entering from the Tape Unit is directed to positions in Core Storage determined by the *NEW* address of the *NEW* control word. The word count of this new Control Word may be different from that of the previous control word and controls how much information is passed and, furthermore, the new control word may be of a type other than that of the first control word. A variation of the first major type of control word has Indicator 1 ON, Indicator S OFF and indicator 2 OFF. Information from the Tape Drive Unit flows directly to Core Storage from the Data Synchronizer channel until an End of Record (EOR) signal is received from the Tape Drive unit selected. A Signal is then sent to the Data Synchronizer Channel and regardless of the word count, the Data Synchronizer Channel goes to Core Storage for a new control word to replace the current one. Still another variation of control word of the first major type has Indicator **19** ON and Indicators S, 1 and 2 OFF. In the Read status, the word count now specifies the number of words on tape to be read and skipped and *not* transmitted to Core Storage. Briefly, a word count of 5 with Indicator **19** ON and the other Indicators OFF specifies that five words shall be read from tape but not transmitted to Core Storage. In each case, of course, as each word is received from the Tape Drive Unit operated, the word is inhibited from passing to Core Storage and the Word Counter is stepped down one. When the Word Counter goes to 0, the Data Synchronizer Channel goes directly to Core Storage for a new control word to replace the current one. Indicator **19** is ignored when doing a Write operation.

The second major type of control word is the Indirectly Addressed control word of a Transfer Instruction. The bit configuration in the Operation Register, FIG. *2eee*, is as follows: Indicator **2** is ON and all others are OFF. Whenever this type of control word enters the Data Synchronizer Channel, the DSC immediately decodes the command, ignores the word count, looks directly at the address portion of the control word in the Address Register, FIGS. *2mm* or *2nn*, and then returns immediately to Core Storage, at the location specified by the Address Register, for a new control word. The address portion of the new control word is fed into the Address Register and also replaces the contents of the Location Register. Accordingly, this Indirect Address control word is a Transfer instruction because it causes the Data Synchronizer to immediately go back to Core Storage for a new control word specified by the address portion of the previous control word. In order to protect the machine against an operator having failed to provide any control words at all, a control word containing all zeros, when it is entered into the Data Synchronizer channel, causes an abrupt disconnect. The DSU is still synchronized, but it causes a disconnect without any flow of data.

The third major type of control word has an Indicator bit configuration with Indicator **2** ON and at least one other Indicator ON such as **S, 1 or 19.** When these conditions are met the action of the Data Synchronizer is similar to that previously described. Data is transmitted until the word count reaches 0 or until an End of Record (EOR) condition is met as specified by those indicators, other than two, which are ON. However, when the Data Synchronizer finds that it requires a new control word, instead of going directly to Core Storage for that control word at the location specified by its Location Register, it inquires of the Central Processing Unit for a Load Channel instruction. This instruction in the

Central Processing Unit is an instruction which delays the Central Processing Unit until a certain signal is received from the Data Synchronizer channel. Such a signal would be of the type previously described when the word count goes to 0 or End of Record signal occurs with Indicator 2 ON in conjunction with at least one of the other Indicators ON. In this instance, the Data Synchronizer channel causes the Central Processing unit to execute its Load Channel instruction instead of the channel going directly to Storage. The Load Channel instruction then provides a new control word to the Data Synchronizer channel and also provides its location in Core Storage to the Location Register of the Data Synchronizer Channel. This is, therefore, a synchronous transfer type of instruction. The Central Processing Unit is now synchronized with the Data Synchronizer channel to provide the new control word. If, when the Data Synchronizer reaches such a condition and requires a new control word, Indicator 2 is ON and at least one of the other Indicators is ON, and the Central Processing Unit has failed to provide such a Load Channel instruction, the Data Synchronizer Channel causes a disconnect and no further data is transmitted.

The tables to follow indicate DSC operation as prescribed by the Indicators S, 1 and 2 with modification determined by the Indicator 19 which determines if the data will be stored (no bit) or not stored (bit.) The Indicator 19 is ineffective in a writing operation.

TABLE I

DSC Triggers A S	B 1	C 2	DSC C (WR)	Tape EOR	TAPE and CARD READING (Not Read Printer) Operation of DSC
0	0	0	0	no	Disconnect unit from 709, but move I/O unit until it reaches end of record
0	0	0	0	yes	Disconnect unit from 709
0	0	0	≠0	no	Continue transmitting words from I/O unit into memory.
0	0	0	≠0	yes	Ignore End of Record, and continue transmitting words from I/O unit into memory
0	0	1	0	no	Bring control word into DSC from location specified in address part of this control word
0	0	1	0	yes	Bring control word into SDC from location specified in address part of this control word.
0	0	1	≠0	no	Bring control word into DSC from location specified in address part of this control word.
0	0	1	≠0	yes	Bring control word into DSC from location specified in address part of this control word.
1	0	0	0	no	Bring in new control word from location specified by LR.
1	0	0	0	yes	Bring in new control word from location specified by LR.
1	0	0	≠0	no	Continue transmitting words from I/O unit into memory.
1	0	0	≠0	yes	Ignore End of Record, and continue transmitting words from I/O unit to memory.
1	0	1	0	no	If Load Channel instruction is waiting, execute it. If not, disconnect unit from 709 but move I/O unit until it reaches end of record.
1	0	1	0	yes	If Load Channel instruction is waiting, execute it. If not, disconnect I/O unit.
1	0	1	≠0	no	Continue transmitting words from I/O unit into memory.
1	0	1	≠0	yes	Ignore End of Record, and continue transmitting words from I/O unit to memory.
0	1	0	0	no	Read tape without transmitting words to storage. At End of Record bring in control word from location specified by LR.
0	1	0	≠0	no	Continue transmitting words from I/O unit into memory.
0	1	0	≠0	yes	Bring in control words from location specified by LR.
0	1	1	0	no	Read tape without transmitting words to storage. At End of Record, if Load Channel instruction is waiting, execute it. If not, disconnect unit.
0	1	1	0	yes	If Load Channel instruction is waiting, execute it. If not, disconnect unit.
0	1	1	≠0	no	Continue transmitting words from I/O unit into memory.
0	1	1	≠0	yes	If Load Channel instruction is waiting execute it. If not, disconnect I/O unit.
1	1	0	0	no	Bring on control word from location specified by LR.
1	1	0	0	yes	Bring in control word from Location specified by LR.
1	1	0	≠0	no	Control transmitting words from I/O unit into memory.
1	1	0	≠0	yes	Bring in control word from location specified by LR.
1	1	1	0	no	If Load Channel instruction is waiting, execute it. If not, disconnect I/O unit from 709, but move I/O unit until it reaches End of Record.
1	1	1	0	yes	If Load Channel instruction is waiting, execute it. If not, disconnect I/O unit.
1	1	1	≠0	no	Continue transmitting words from I/O unit into memory.
1	1	1	≠0	yes	If Load Channel instruction is waiting, execute it. If not, disconnect I/O unit.

TABLE II

DSC Triggers A S	B 1	C 2	DSC C(WR)	TAPE AND CARD WRITING Operation of DSC
0	0	0	0	Write End of Record Designation and disconnect unit.
0	0	0	≠0	Continue transmitting words from memory to I/O unit
0	0	1	0	Bring control word into DSC from location specified in address part of this control word.
0	0	1	≠0	Bring control word into DSC from location specified in address part of this control word.
1	0	0	0	Bring new control word into SDC from location specified by LR.
1	0	0	≠0	Continue transmitting words from memory to I/O unit.
1	0	1	0	If Load Channel instruction is waiting, execute it. If not, write End of Record and disconnect unit.
1	0	1	≠0	Continue transmitting words from memory to I/O unit
0	1	0	0	Write End of Record indication and bring in new control word.
0	1	0	≠0	Continue transmitting words from memory to I/O unit.

TABLE II-Continued

DSC Triggers			DSC C(WR)	TAPE AND CARD WRITING Operation of DSC
A S	B 1	C 2		
0	1	1	0	Write End of Record indication. If Load channel instruction is waiting, execute it, if not disconnect unit.
0	1	1	≠0	Continue transmitting words from memory to I/O unit.
1	1	0	0	Bring new control word into DSC from location specified by LR.
1	1	0	≠0	Continue transmitting words from memory to I/O unit.
1	1	1	0	If Load Channel instruction is waiting, execute it. If not, disconnect unit.
1	1	1	≠0	Continue transmitting words from memory to I/O unit.

DATA SYNCHRONIZER PRIORITY SYSTEM

The apparatus which causes multiplexing in response to demands from Input-Output devices for access to Magnetic Core Memory **1.12** is known as "The Data Synchronizer Priority System." Stated otherwise, the Priority System determines which of the DSC Channels at any given instant of time is connected to the common Storage Busses or Storage Address Busses. When information is to be passed to Core Storage or is to come from Core Storage to one of the I/O devices, the information is buffered in the associated Data Synchronizer **1.20** for as long as is necessary for data reference to be made for that particular channel. When one of the Input-Output devices sends a signal to the Central Processing Unit requesting access to Core Storage, a signal is also sent to the Priority Units, FIGS. **206, 208, 209,** which are interconnected logically among the Data Synchronizers to determine the sequence of service and insure that any demanding channels which require access to Storage will be served. Each Data Synchronizer Channel is served serially and those not first served, but demanding access to Storage, continue to send a signal to the CPU **1.10** requesting access to Core Storage **1.12** until the demanding channel has been served. The channel which is selected by the Priority System to receive information and to gain access to Core Storage then has the option of making a second reference to Core Storage immediately, if necessary, without being interrupted by either the CPU or other Data Synchronizer channels. This covers the possibility of a single channel requiring three successive references to Storage because it would not be feasible to allow other channels to obtain references to Storage and interrupt a short sequence of operations by a particular channel. After the operating Data Synchronizer channel has satisfied its demands for access to Core Storage, the Priority System is allowed to change to serve another waiting channel. If a single channel, for instance, requires reference to Core Storage, that single channel can gain reference to Core Storage at once except that it may have to wait for synchronizing with the CPU. To summarize, whenever a Data Synchronizer channel requires access to Core Storage, it sends a signal direct to the CPU requesting access thereto and sends another signal to the Priority System.

TAPE CONTROL UNIT

The purpose of the Tape Control Unit, FIGS. *2xx–ccc*, is to provide circuitry for motion controls of the Tape Drive Units and to provide additional buffering of data in the system by means of a **36** bit Shift Register, FIGS. *2xx–aaa* (FIG. **225**), and to provide checking features for ascertaining that the data is read and written correctly. In connection with the Shift Register, there is a Shift Counter, FIG. **226,** which counts to 6 thereby taking six characters in sequence from a Tape Drive Unit reading and storing them serially by six character groups to from a 36 bit word by shifting six characters at a time. When writing, the converse is true. A 36 bit word is shifted six times to provide six characters to the tape in a serial manner. In addition, there are registers to provide storage for commands which can be remembered by the Tape Control unit itself which is an important feature in stacking commands from the Input-Output device back to the Central Processing Unit. As mentioned previously, there are two modes of operation of a Tape Control Unit, Binary Coded Decimal and Binary, and accordingly the Tape Control Unit causes reading or writing in two respective corresponding modes of operation. That is, it can transmit pure Binary information in either direction or it can transmit the Binary Coded Decimal information.

DESCRIPTION OF THE REGISTERS OF THE TAPE CONTROL UNIT

Several seven position registers are used in the Tape Control Unit for processing information through the tape system. The High Clip Register, FIG. *2bbb*, is one of two input registers in the Tape Control Unit of the tape unit and has a primary function of providing buffering action between the Tape Drive Unit and the Tape Control Unit. A secondary function is to compensate for tape skew. The High Clip Register is supplied with signals from the Read Amplifier, FIG. *2dd*, which signals are greater amplitude than a 1.2 volt peak-to-peak amplitude. Signals of lesser amplitude are blocked from entering. The Low Clip Read Register, FIG. *2bbb*, is the other of the two input registers to Tape Control Unit from the Tape Drive Unit and has the primary function of providing buffering action between the Tape Drive Unit and the Tape Control Unit. A secondary function is to compensate for skew. The Low CLip Register is supplied with information from the Read Amplifier that is of greater amplitude than 0.8 of a volt peak-to-peak. Signals of lesser amplitude are blocked from entering.

The Line Register, FIG. *2bbb*, is an input register used to provide buffering action between the Read Registers and the remaining Tape Control Unit logic circuits. The Match Check and Low Longitudinal Redundancy Chec, (LOLRC) Register, FIG. *2bbb* (FIG. **231**), is a dual function register depending upon whether the operation iS Read or Write. On the Read operation, this register reflects the longitudinal redundancy status of the Low Clip Register, FIG. **228.** On Write operations, a bit for bit matching of information contained in the High and Low Clip register occurs and if comparison is correct, all positions of this register will be OFF; if a bit is present in one register (High or Low) and not in the other corresponding position (High or Low), an error signal is available as an output from the Match Check Register. The Longitudinal Redundancy Check Register (LRCR) is the register used to check the longitudinal parity of each recording channel in each record. If each of the seven channels

throughout the entire record was read or written correctly, all positions of this register are OFF. If an error has occurred, it would be indicated by an output from this register. The Shift Register, FIGS. 2*xx*–111, as mentioned previously, is used as a 36 bit input register from the DSU to the TCU, a 36 bit output register from the TCU to the DSU and as a six bit output register from the TCU to the Tape Drive unit when writing and a six bit input register from the Tape Drive to the TCU when reading. The Bit switches are used on test operations to establish the information pattern to be written on tape, and function only on test operations when they replace information normally supplied by the DSU.

Outputs are provided from the Tape Shift Register, positions S, **1** through **5** through the Binary - BCD Translators to the Write Bus, Figures 2*xx* (FIGS. **227***a*, *b*, *c*, and *d*), which may pass the data to one of the several Tape Units. Seven input data lines are provided from one of the several Tape Drive Units, FIG. 2*eee*, to the High and Low Clip Read Register, FIG. 2*bbb* (FIG. **228**). Outputs from the High and Low Clip Register are provided to a High Clip Lateral Parity Checker, FIG. **229,** and the Low Clip Parity Checker, FIG. **230,** which are shown in block form in FIG. 2*ccc*. Additional outputs of High and Low Clip Register are provided to the Lateral Redundancy Check Test and Line Registers, FIG. 2*bbb* (FIG. **231**). Outputs of the LRC Test and Line Register are provided to a Read Translator FIG. 2*aaa* (FIG. **232**) and the Read Translators have outputs to the Lateral Parity Checker, FIG. 2*zz* (FIG. **233**), and another set of outputs to positions **30** through **35** of the Tape Shift Register, FIG. 2*aaa*. In order to provide an odd or even redundancy bit outputs from the Tape Shift Register, outputs from positions S, 1 through 5 are provided to the Check Bit Generator, FIG. 2*xx* (FIG. **234**). The High Clip Lateral Parity Checker, FIG. **229,** provides signals to the High Clip Error and Sample and Not Stop and Error Gate Controls, FIG. **235,** and a Low Clip Lateral Parity Checker, FIG. **230,** provides an output to Low Clip Error and Sample Pulses Circuits, FIG. **236.** Also associated as a High and Low clip Checking feature is the clipping Selector and Tape Check Gating. FIG. **237,** and High Clip and Low Clip Gating and Tape Check, FIG. **238.**

FIGS. **239** through **245** are concerned with control and status of the Tape Control Unit. FIG. **239** illustrates these circuits required for Backspace control. In FIG. **240,** there is shown a Stop and Go control and in FIG. **241,** there is shown the Read and Write Status Controls. Backspace and Rewind after Write, FIG. **242,** is an automatic control which operates in each instance after Write operation. In FIG. **243,** Programmed Controls are shown for testing the status of the Unit. In FIG. **244,** circuits are shown for Beginning of Records, Beginning of File Search and Record Gate. In FIG. **245,** the Character and record Control circuits are shown, and in FIG. **246,** the Tape Mark matrix character Gate Generator and the Seven Way OR circuit are shown, the latter for providing gated write echoes used to generate the 33 microsecond character gate. The End of File (EOF) Sensing and First Character Gate circuits are shown in FIG. **247,** and the Read and Write Delay is shown in FIG. **248.** Reset and disconnect controls are provided in FIGS. **249** through **252** which are Clock Write Pulse and Line Register Reset, Character Gate and Disconnect, Read Clock and Line Register Reset, Class and Unit Disconnect Gate and Start Read/Write or Write End of File respectively. The Interlock circuits of the Tape Control Unit are shown in FIG. **253.**

FIGS. **254** to **256** are devoted to Tape Unit Selection and Data and Non-Data Class Selection. FIGS. **254***a* and *b* are for Tape Unit Selection; FIG. **255,** the Data Class Selector; FIG. **256,** Non-Data Class Selection. In FIGS. **257**a and b, Pulse Generators and Reset Controls are shown and Testing Circuits are shown in FIG. **258***a* and *b*. In FIG. **259,** there is a Blank Generator having inputs of Tape Work Incomplete and Tape Word Complete for a purpose hereafter described, and Shift Register Controls 1 and 2 are shown in FIGS. **260***a* and *b*. Read-Write Error and Tape End of Record Controls are shown in FIG. **261.**

The purpose of the Blank Generator, FIG. **259,** and associated circuitry is to remove the system restriction that only tape records containing an integral multiple of **6** characters (one sixth of a word) can be transmitted from a Tape Drive Unit to Storage via the TCU and Data Synchronizer. The Blank Generator operates automatically when an End of Record has been reached and if the number of characters recorded is not an integral multiple of 6, the Blank Generator automatically shifts the residual character (in excess of the next lower integral multiple of 6) to the high order position of the 36 bit shifting register and fills in any remaining lower orders with binary zeros. Upon completion of such manipulation of the excess characters, the Blank Generator automatically produces an artificial demand signal causing the contents of the 36 bit Shift Register to be transmitted to the DSC Buffer Register just as normal words are transmitted. Such operation automatically occurs only when the TCU is reading in the BCD mode since this is the mode requiring such manipulation.

TCU CLASS OR OPERATION REGISTER

The Write End of Call Trigger, FIG. **256;** Backspace Triggers, FIG. **239;** Go Trigger, FIG. **240;** First Character Trigger, FIG. **247**: Read Cycling Test Trigger, FIG. **258***a;* Test Write Trigger, FIG. **258***b;* Tape Unit Selectors, FIGS. **254***a* and *b;* the Write Call Trigger, FIG. **254***c;* the Read Call Trigger, FIG. **254***c;* the BCD Mode Trigger, FIG. **254***c;* the Rewind Call Trigger, FIG. **254***d;* Backspace Call Trigger, FIG. **254***d;* and Class and Unit Disconnect Gate, FIG. **254***d*, may be thought of as a Register which stores a single operation to be transmitted. Within this register is contained the command that the Tape Control Unit with a particular Tape Unit is to perform an operation such as Read, Write, Rewind, Backspace and so forth. In the case where the Tape Drive unit is given the Rewind command the Tape Drive itself essentially can remember that it is rewinding and disassociates itself from the entire system while it is performing this operation. If a command is sent to a Tape Control Unit for execution and one of the associated Tape drives is rewinding, the command may be executed by the other Tape Drive Units immediately. The only exception is when one Tape Drive is rewinding and another command is received for that particular Tape Drive. The execution of a Rewind causes the Tape drive to immediately disconnect and a second rewind to this Tape Drive is treated as no operation. If the Unit Select Register. is used in connection with the operation command register to remember which particular Tape Unit is to be caused to get up speed and perform a specified command. The DSU channel to which the Tape Unit is attached via its TCU

may initiate a command to the Tape Drive via the TCU and the Tape Control Unit then remembers that command. In some cases, the Tape Control Unit allows a second command to be stored in the Data Synchronizer Channel awaiting execution when the DSU has completed transmission of the previous command to the TCU. This stacking feature is not always complete because when an Input-Output operation appears in the Operation Register of the CPU a specified DSC is tested to see if that channel is in operation. The instruction in the Central Processing Unit can not end operation or allow another instruction to follow in sequence until a signal has been received from the Data Synchronizer Channel specified. In essence then, a command from the CPU enters or awaits and delays indefinitely until the DSC sends a signal back to the CPU telling it to end operation. Thus, in stacking, a possibility exists that a particular Tape drive is rewinding and disassociated from the system, an operation is currently being executed by the Tape Control Unit on another Tape drive, a third operation is being stored in the Operation register of the Data Synchronizer, and still one other operation is being stored by the CPU awaiting execution and entry into the Data Synchronizer Channel. In this instance, the entire Central Processing Unit is delayed and no calculation is taking place. However, by proper programming it is not necessary that the Central Processing Unit be delayed since it has the capacity for testing the Data Synchronizer Channel periodically to determine when the Data Synchronizer is free. Upon ascertaining that the Data Synchronizer is available for another command, it then sends the command to the Data Synchronizer Channel for execution. One important feature of the system, however, is that up to three instructions may be simultaneously in execution while the Central Processing Unit may be acutally doing useful calculations.

In connection with stacking, four important characteristics of the CPU, DSC, TCU, and Tape Drive chain should be pointed out. (1) The Tape Drive Unit has the ability to remember that it is either to execute a rewind or that it is actually executing the rewind. (2). The Tape Control Unit has the ability to remember that it is to execute a tape command and has the ability also to remember that it is to execute a command on a particular one of the Tape Drive Units. (3) The Data Synchronizer channel has the ability to remember first of all that is is executing or is about to execute a command to a Tape Control Unit, including information as to which particular Tape Drive attached to the Tape Control Unit is actually executing a Data Transmitting Instruction to a Tape Control Unit, but in this case it does not remember the Tape Drive Unit which is actually executing an instruction but only the Tape Control Unit which is executing the command. (4) At the same time the Data Synchronizer Channel has the ability to remember one additional non-data transmitting instruction plus information concerning which particular Tape Drive Unit the non-data instruction refers to and this unit may be different from a Tape Drive Unit which is currently transmitting information to or from the units by way of the Data Synchronizer Channel. The CPU has the ability to (a) delay indefinitely the transmission of a command to Data Synchronizer channel if it is busy, where "busy" may be defined as a condition in which either a transmitting or non-transmitting command is still in operation in the Data Synchronizer channel, and (b) to test the status of the Data Synchronizer channel to determine whether or not it is busy without introducing a significant delay in the calculator operations. It is evident at this point that two tape operations may occur simultaneously, a third tape operation is stored in the Data Synchronizer channel awaiting execution and no delay is occasioned in the CPU. The operations that may be stacked thus are as follows: A rewind operation may be in actual operation on a particular Tape Drive, any other tape instruction may be in operation on another Tape Drive, and a third instruction may be stored in the Data Synchronizer channel awaiting execution or transmission to the Tape Control Unit. A typical operation would be as follows: A Tape drive is rewinding, another Tape drive is reading or writing and the Data Synchronizer Channel remembers that it is transmitting information, but it does not know which Tape Unit. In addition, the Data Synchronizer Channel has stored, awaiting execution, a non-data transmitting instruction and a designation for a particular Tape Drive unit which is to execute this non-data transmitting instruction. The CPU is entirely free for calculation and the CPU may periodically test to determine when the Data Synchronizer channel is free from the exceptance of another Input-Output instruction from the CPU through the Data Synchronizer channel. However, if such testing is not necessary the CPU may be attempting to enter or transmit a new instruction into the Data Synchronizer channel and in this case the CPU delays indefinitely until all previous operations in the Data Synchronizer channel have been cleared. Then the CPU transmits the new instruction to the Data Synchronizer allowing the CPU to free itself for other operations. Such operations are possible with all channels in the Data Processing System and the purpose of such stacking is to take advantage of the ability of each of the units in the chain to remember a specific operation, which they are performing or are about to perform with the viewpoint of conserving very valuable high speed CPU time for calculation.

THE TAPE UNIT

As previously mentioned eight magnetic tape units are provided for each Tape Control Unit, each Tape Unit containing a reel of Tape which may be as long as 2,400 Feet. The tape itself is a plastic oxide coated band one half inch wide having information recorded thereon by means of magnetized spots corresponding to binary numbers. A block of words consecutively on a tape is called a record and the amount of information contained in each tape depends on the length of the individual records since there is a certain amount of space between each record to allow for starting and stopping the tape. Reading, writing, and backspacing tape is done at a speed of 75 inches per record. The data transmission rate between magnetic tape and core storage is 2,500 36 bit words per second or 2.5 kilocycles in the Binary Coded Decimal mode. This is equivalent to 15,000 7 bit characters per second in the BCD mode and to 25,000 decimal digits per second in the Binary mode. One reel of tape may hold as many as 960,000 words of information. Between each record on the tape there is a three quarter inch space of blank tape called the End of Record (EOR) or Record gap. A group of records within a tape are called a File and any number of Records may make a File. In addition, there may be one or more files on a tape with each file

separated by an End of File (EOF) gap. An End of File gap is longer than an End of Record gap and may be distinguished thereby.

When reading a tape, the tape unit never stops at any place other than End of Record or End of File gap. A partial record may be read into core storage, however, under program control, but the physical motion of the tape always continues until the read-write heads are positioned over an EOR and EOF gap. Tape is locked in continuous motion until bits have ceased being read for a predetermined period of time. During writing, an End of Record gap may be written while the tape is slowing down from full speed.

However, when the tape stops, an End of Record gap is always written. End of File gaps may also be recognized by the stored program operation while reading a tape and this provides a useful way of separating large quantities of different kinds of information.

Instructions are also available which backspace the tape over a record or file, but no information may be written or read when the tape is moving in the backward direction. Tapes are written or read in the forward direction only but the same tape may be written, backspaced, read, backspaced and written again in that order. Accordingly, a record may be written and then read for checking purpose before writing for the purposes of computation.

Apparatus is provided for continuously reading what has been written and performing checks to determine the accuracy of recording the data. The broad principle of such error checking is disclosed and claimed in U.S. Pat. application Ser. No. 671,834, filed July 15, 1957, Dual Channel Sensing, Hugh A. O'Brien. Although the system will be described briefly here for the purpose of illustration, details may be had by reference to the foregoing application.

Normal rewinding speed of a tape is 75 inches per second if the length of tape to be rewound does not exceed 450 feet and the time of high speed rewind of any reel of tape of the length of 450 to 2,400 feet is nearly constant at about 1 minute. In order to indicate the load point of a physical end of the tape, reflective spots on the tape made of adhesive aluminum strips are photoelectrically sensed to indicate the physical beginning and end of the tape. Briefly, a Tape Unit consists of tape drive mechanism, a sensing mechanism, a writing mechanism, a reel of magnetic tape as previously described, and associated registers and control. A pair of tape reels are provided to hold the tape and are driven intermittently so that a pair of tape loops are formed which are maintained in a vacuum column on either side of the tape sensing device mechanism. Pressure sensitive switches in the vacuum column provide signals for controlling the reel driving mechanism to reel and unreel the tape as fast as the drive mechanism needs it without putting undue stress on the tape. On a rewind operation the tape unit automatically pulls the tape out of the vacuum columns, opens the tape sensing mechanism, retracts the tape driving mechanism so that a direct reel transfer of tape can be effected. The reflective strip at the beginning of the tape is referred to as the load point of the tape or Beginning of Tape while the reflective strip at the end of the tape is hereafter referred to as the Tape Indicator point. Each tape unit is provided with a tape indicator unit which turns on the tape indicator at the physical end of the tape or the End of a File of information. Mechanism and the manner of control of such mechanism is disclosed in U.S. application, Ser. No. 486,832, Tape Feed Machine, Buslik, et al., filed Nov. 15, 1954.

The method of recording information on tape is a non return to zero method. The recording head always magnetically saturates the tape in one polarity or the other. A 0 bit is recorded by continued saturation in the same direction while a "1" bit is recorded by the transition of saturation from one to another direction. During the write operation 7 bits which may be 6 information bits plus the redundancy check bit are recorded laterally across the tape in seven channels. The lateral redundancy check bits are automatically placed on the tape by the TCU to cause an even or odd number of binary "ones" in each lateral row of tape for the Binary Coded Decimal and the Binary mode respectively. Also, at the end of each record written, a longitudinal redundancy check bit is automatically placed by control of the TCU in each of the seven channels to cause an even number of binary "ones," in each channel for that particular record. The longitudinal channel is always an even check for Binary Coded Decimals and an odd check for Binary mode.

Systems Diagram of the Tape Drive Unit are shown in FIG. **262** and the data portion is illustrated in FIGS. **2***ddd*. Seven outputs C, B, A, **8, 4, 2** and **1** are provided to the Write Amplifier, FIG. **263.** Inputs to the High and Low Clip Registers, FIG. **2***bbb* (FIG. **228**) are provided from the Read Head and Read Pre-Amplifiers, FIG. **264.**

Instructions to a TCU for operating a tape unit include: Backspace file (BSF) Backspace Tape (BST), Beginning of Tape Test (BTT), End of Tape Test (ETT), Read Select (RDS), Rewind (REW) Transfer on Data Synchronizer Channel A End of File (TAF), Transfer on Data Synchronizer Channel B End of File (TBF) and similar instructions for other DSU channels, TCF, TDF, TEF and TFF, Write End of FIle (WRF) and Write Select (WRS). Commands to a Tape Drive include Set Read Status, Set Write Status, GO, Backspace and Rewind. Instructions WRS, RDS and WEF may be given either in the Binary or BCD mode. In summation, a three quarter inch blank space on the tape defines the End of Record, and a 3.7 inch blank space, a tape mark followed by its redundancy character, and an End of Record gap defines an End of File of information in BCD. The gap only is used for an EOF in the Binary mode.

The Tape Drive Unit has seven transducer heads for reading tape, each connected to a Read Pre-amplifier (FIG. **2***ddd*) and individual read buses to the Tape Control Unit. Each Tape Unit has seven write transducers coupled to Write Amplifiers (FIG. **2***ddd*) and in turn to individual ones of seven lines of the Write Bus from the Tape Control Unit. In FIG. **262,** various controls, Tape Indicator (FIG. **267**), Read-Write Status and Gated. Write Pulse (FIG. **266**), Rewind Control, FIG. **271,** Select and Ready (FIG. **265**) Motor Control Circuits, Relay Control Circuits, Tape Start Stop and Forward Rewind, FIG. **269** and Load Point, FIG. **268** comprise other significant controls to be discussed hereafter in connection with the descriptions of operation of the DSC, TCU and Tape Drive Units.

FLOW OF DATA

Writing Operation

When in a writing operation, data is transmitted from

Storage (FIG. 2*ll*) to the Data Register (FIG. 2*ss*, 2*tt*) in a particular DS channel, 36 bits at a time, in parallel, during a 12 microsecond period. When a word is moved from Core Storage to a Tape Drive Unit (FIG. 2*ddd*), it is buffered or stored in the Data Register (FIGS. 2*dd*, *tt*) of its channel in the DSU until it is required by the Tape Control Unit. At that time, the entire word of 36 bits is transmitted, in parallel, to the Shifting Register (FIGS. 2*xx–aaa*) in the Tape Control Unit. The access time or time required to actually move this data between the Data Register of the Data Synchronizer and the Shift Register of the Tape Control Unit is on the order of 6 microseconds. The word in the Shift Register is shifted left, 6 bits at a time, and the upper six positions are taken in parallel from the Shift Register and are recorded on the tape. Each time these 6 bits are recorded, the register is again shifted and this continues until the entire word is transmitted and written. Each 6 bit configuration is placed in a Parity Generator (FIG. **234**) which compares and counts the number of bits actually present in the 6 bit configuration and then generates an even or odd parity bit, the seventh bit, to be recorded along with the 6 information bits depending upon the mode of operation, Binary or Binary Coded Decimal.

The information recorded on tape is rad by a Second head or Read Head (FIG. 2*ddd*) on a character by character basis 4 milliseconds after writing, is returned to the Tape Control Unit (FIG. 2*bbb*) which puts it in two channels and each channel is checked in the circuits of FIG. 2*ccc*. If no error has occured in either channel, the contents of the two channels are compared with each other on a bit by bit basis for each character. Even though there are no parity check errors in each character, the comparison of the contents of the two registers is made on a bit by bit basis to determine whether a double error or a double bit drop-out has occurred thus retaining the proper parity in each channel. If the information is not identical, the error indication is set.

RESET AND LOAD CHANNEL TIMING

Once execution of a WRS or RDS instruction has begun in the Data Synchronizer Channel, the Reset Load Channel instruction must supply the DSC with the command before the tape is ready to send or receive the first data word. The time within which the order must be given depends on whether a WRS or RDS is specified and whether the tape is at it load point or not. When the select instruction WRS is given and the tape position is not at Load Point, Reset and Load Channel (RLC) must be given within 4 milliseconds. When the selection instruction WRS is given and the tape position is at the load point, RLC must be given within 40 milliseconds. When the select instruction RDS is given and the tape position is not at load point, RLC must be given within 3 milliseconds. When select instruction RDS and tape position is at load point, RLC must be given within 20 milliseconds. However, when a Reset and Load Channel is not given at all following a Write Select instruction, the tape continues in motion until an End of File Gap is recorded and is checked by the Reading Head. That is to say that no information is recorded, but the tape is erased and the Reading Head carefully reads and checks to see that no information actually is recorded and that no noise is present on the tape. When the Reset and Load Channel instruction is given following a Write Select, but the time allowed after the Write Select and before the Reset and Load Channel is given is exceeded, an End of File Gap is written once again but in addition the Input-Output check light is turned ON which may be interrogated by the CPU under Program Control.

READ SELECT

When a Reset and Load Channel is not given at all following a Read Select, the first record is spaced over and skipped, data is not transmitted, and the tape stops in a position such that a subsequent Read Select is prepared to read the next record. If a Reset and Load Channel following a Read Select is given but in a time exceeding the allowable time, the same result occurs with the addition that the Input-Output check light is turned ON.

DSU CHANNEL PREPARATION FOR A NEXT OPERATION

In a Writing operation, the Data Synchronizer Channel always knows in advance when the last word to be written has been transmitted to the Tape Shift Register of the Tape Control Unit. Since this is so, the DSU is allowed to disconnect and prepare for another operation. The Tape Control Unit, however, still has this last word to be written, or at least a portion of it, since 6 bits are transmitted at a time. Therefore, the Data Synchronizer interlock controls are not reset until the operation has been completed, although the Data Synchronizer Channel has completed its portion of the operation. The Tape Control Unit continues in motion and the Write Clock Gate does not fall until the word has been completely written. Of course, on Reading the converse is true. When the last character has been received and the last word transmitted from the Tape Shift Register of the Tape Control Unit to the Data Register of the Data Synchronizer, the Tape Control Unit senses that the last word is to be transmitted and therefore it proceeds to enter upon an automatic disconnect procedure. The Data Synchronizer still must hold the word until it gains access to Core Storage to unload the word. In this case, the Tape Control Unit is free but the Data Synchronizer Channel is engaged until that word has been finally transmitted to Core Storage. In this case where special control words require that even though the last word in a record on tape is recognized, the tape is not to stop but continue in motion, the word in the Data Synchronizer is transmitted to Core Storage and automatic reselection of the Tape Drive Unit occurs before any speed decrease has occurred in the Tape Drive. The one exception to the preceding sequence of events occurs when Reading, and that is when an End of File condition is sensed by the Tape Control Unit. Then, an uncondition disconnect results of the Tape Control Unit and also the Data Synchronizer Channel which sets an indicator which may be tested at any time when program control from the Central Processing Unit.

GENERAL DISCUSSION OF BINARY AND BINARY CODED DECIMAL MODE OF OPERATION

Two Types of End of File indications may be recorded on tapes. One is for use with the Binary mode, the other is for use in the Binary Coded Decimal mode. A Binary End of File (EOF) is defined as 40 milliseconds of tape movement which is approximately 3.6

inches of blank tape and this condition is detected for each reading of 33 milliseconds of blank tape. A Binary Coded Decimal End of File is defined as 48 milliseconds of blank tape followed by a Tape Mark, the latter being a character with bits in the 1, 2, 4 and 8 channels and no bits in the A, B and C channels and is detected while reading in the BCD mode by the presence of a Tape Mark. The Blank tape preceding the tape mark is ignored because a BCD End of File recorded by certain peripheral equipment is the Tape Mark preceded by an End of Record (EOR) gap. Therefore, it is pointed out that to distinguish between the two codes detection must be based on the tape mark recognization only.

In parallel machines, such as the one described in this application, the use of Binary method of carry checking and information grouping is used which requires that the information be in a binary ascending order or relationship. If information is coded in such a way that binary representation increases in value from numeric 0 to alphabetic A through Z simplified programming results, and therefore, greater speed is achieved in comparison or in sorting operations. On the other hand, in serial computers information is processed in character form and comparision is a direct process by which characters are not compared in a direct Binary numeric value of the character. In this case, speed and ease of programming are obtained by not having to convert numbers and alphabetic characters from Hollerith code to a binary representation. Accordingly, two different methods of parity checking have been developed, one for each of the modes of operation and when processing tape, the tape control unit operates in the Binary mode or the Binary Coded Decimal mode depending upon the code used in the record.

Since any bit configuration is possible in the Binary system, no special characters are allowable. Data is recorded on tape in sets of 6 bits when the seventh bit is an odd parity in the Binary mode or even parity in the Binary Coded Decimal mode. However, it is pointed out that both systems use even longitudinal parity checking which bears no relationship to the code employed.

In addition to End of File condition, there is a Beginning of File Conditions since an instruction is used called "Backspace File." When the tape is backspaced, the Beginning of a File is reached and this condition is defined differently than is the End of File condition. When backspacing over tape the definition of a Beginning of File is as follows: Approximately 33 milliseconds of passage of blank tape which corresponds to about 3, 6 inches of blank tape on an End of File Gap. Of course, an EOF gap must be sensed while moving tape in the backward direction under the execution of a Backspace File Instruction. However, the time period necessary to define the Beginning of File is only 33 milliseconds of blank tape thus providing about 7 milliseconds for a safety factor. In addition, this 33 milliseconds of blank tape must be subsequent to having read at least some binary bits recorded on the tape, which is to say, that should the tape begin to move backward it moves backward over any length of blank tape until it reaches and reads at least some information recorded on the tape which is in the form of bits or changes in the flux polarity. Tape continues in backward motion as long as bits are recorded in any channel on the tape and if at the conclusion of such recorded information, a gap of at least 33 milliseconds of blank tape exists, then the tape stops and a backspace file has been considered executed with the Beginning of File gap being reached. This condition is true regardless whether information is recorded on tape in the binary mode or in the binary coded decimal mode and furthermore, at the conclusion of execution of a Backspace File instruction, tape is positioned such that a subsequent read forward of a tape in the Binary mode produces an End of File and the tape is positioned such as to read the first record in that file on a subsequent Read Forward. In the case of binary coded decimal tape, however, a subsequent Read Forward produces an End of File if selected in the Binary Coded Decimal Reading Mode and tape is positioned such as to read the first record in the file. However, should this tape have a Binary Coded Decimal End of File recorded on it, a Read Forward subsequent to a Backspace file, in the Binary Mode results in an End of File condition and tape is positioned such that a subsequent Rear Forward in the Binary Mode, treats the recorded tape mark as pure binary information and automatically upshifts this one word record in the Shift Counter filling in the blanks (as previously described under Blank Generator) transmitting it to the DSC Buffer Register, FIGS. 2ss-tt, along with a parity check light indication in as much as the tape mark has an even parity and when reading in the Binary Mode a check is made for odd parity.

DOUBLE GAP HEAD IN CHECKING SYSTEM

A double gap electromagnetic transducer, as shown in U.S. application Ser. No. 580,894 filed Apr. 26, 1956, Whitt et al., now U.S. Pat. No. 2,922,231 issued Jan. 26, 1960, is used in the Tape Drive Unit for reading and writing data on tape.

The two gap head provides two logical transducers, one for writing and one for reading. The Reading Head and the Writing Head each containing seven channels or seven transducers completely independent of each other. The Reading Head is spaced three eights of a linear inch behind the Writing Head while tape is moving in the forward direction. This corresponds to 75 inches per second tape motion in 4 milliseconds delay in reading what has been previously written by the Writing Head.

Split channels are provided from the tape Read Head for clipping at two different levels, one high and one low simultaneously and the data in each separate channel is completely parity checked independently and simultaneously. When writing on tape, the data are also read and placed in the two channels for comparison to discover discrepancies. Automatic error rejection is employed when reading if one channel is in error by rejecting error channel and transmitting the channel having the correct parity. In the case where both channels are in error while reading, then in normal operation the channel having the lowest level of clipping is transmitted even though it is in error and an error indicator is set, but when only one channel is in error, the remaining channel containing proper information is transmitted and the error indicator is not set.

In further explanation of checking what is written on tape, it is pointed out that what is written on tape is read back 4 milliseconds later. This information is brought into a final amplifier then split into the two channels previously mentioned of low clipping and high clipping. Each of these channels are parity checked and on the write condition both channels are matched. If an

error occurs, a tape check trigger is turned ON. This matching is accomplished bit by bit in what was previously described as the Match Check Test Register, FIG. 2*bbb* (FIG. 23), which is a seven position Trigger register. The matching result is accomplished by entering what is the High Clipping channel into the set of binary triggers at approximately 4.2 microseconds before the fall of the character gate and then at the fall of the character gate, the data from the Low Clipping channel are put in on to of the high channel information. If no error has occurred the contents of this register is "0", but if any errors have occurred in any one of the bits, it appears as a "one" in this register.

Of the Write operation both channels are parity checked independently and if an error has occurred in either channel a tape check trigger is turned ON and the contents of the channel in error is placed in the Line Register. As information is placed in the Line Register, it is also placed simultaneously in the LRC Register, FIG. 2*bbb*, which keeps a longitudinal check on the information as it is written. At the End of the Record, this register should be at 0 if no error has occurred longitudinally. On the Read operation, the data is parity checked in the High and Low channels independently and if neither one is in error, data from both these channels are simultaneously placed in the Line Register. If either the high channel or the low channel is in error, the opposite channel is placed in the Line Register. Simply stated, if the high channel was in error, the low channel is placed in the line register and no error is indicated, but if both channels are in error a tape check indication is provided and either the high or the low channel is placed in the Line Register depending on the predetermined setting of an error switch. On the Read operation, data are read from the tape to the Final Amplifier and clipping in two channels at two levels is accomplished, then the two channels are parity checked and if either one is correct the information is placed in the Line Register and from there is passed on from Storage when the **36** bit word has been accumulated. The High Clip channel is a relatively insensitive channel and the Low Clip channel is a channel of relatively low sensitivity. The least sensitive channel tends to eliminate large noise pulses and more sensitive channel is capable of reading weak signals. When writing, the clipping levels in each of these channels, although different and distinct, are both simultaneously reduced, or that is to say the sensitivity of the pair of channels, is reduced by about **5%** to compensate for the fact that a freshly written tape immediately re-read **4** milliseconds later produces a very strong signal which is about **5%** greater than the same tape which is read for the second or third time. As previously stated the information read is passed through the final Amplifier and split into two Clipping Channels have different clipping levels and then Data in each separate channel are completely parity checked independently and simultaneously.

When Writing, the two channels are subsequently compared on a bit by bit basis and if incorrect parity exists on either channel or if a bit by bit comparison fails to yield a zero result than an error indicator is turned ON and its status is transmitted to the Data Synchronizer channel. This essentially provides a very stringent signal requirement for operation while writing but in reading, the sensitivity of both channels are each increased by about 5 percent over that employed while writing.

READ OPERATION

Information is read by the same monitoring head as in writing on a character by character basis. Each character passes through a final smplifier and it splits into two channels of High Clipping and Low Clipping, FIG. **228,** and these two channels are parity checked separately in FIGS. **229** and **230.** If either of these channels is correct the correct channel is transmitted to the Line Register which is really an additional buffer register having a capacitor of 7 bits, FIG. **231.** When the character enters the Line Register it is again parity checked to make sure that the proper redundancy is present, odd or even. The character is then loaded into the Shift Register, FIG. 2*aaa*, in the low order positions thereof until a sum of six characters has been received and fills the Shift Register. The Shift Counter, FIG. **226,** keeps track of the number of characters that have been placed in the Shift Register and when this number reaches **6** the Shift Register is known to be full and a signal is sent on line **226.02** to the Data Synchronizer channel to which this TCU is attached. This signal tests the status of the Data Synchronizer channel and if the Data Synchronizer channel is prepared to receive the word, the word is transmitted **36** bits in parallel directly to the Data Register for that DSC, FIGS. 2*rr* or 2*ss*. The word is temporarily buffered in this register until access to Core Storage, FIG. **211,** may be made by the Data Synchronizer channel through its multiplexing system. When connection between the Data Synchronizer and Core Storage is accomplished, a full word of 36 bits in the Data Register is transmitted to the Core Storage at the location specified by the Address Register, FIGS. 2*mm* or 2*nn*, in the Data Synchronizer.

An important fact to emplasize is that when six DSU channels are operating with tape records and operating simultaneously at the rate of 2.5 kilocycles there is always sufficient time for the Data Synchronizer channel to gain access to Core Storage and load and unload a word before another word is ready from the Tape Control Unit. This is indicated by the timing chart of FIG. **273** which will be discussed with reference to the circuits of the Data Synchronizer Unit.

TAPE OPERATIONS

There are eleven instructions designed for use in conjunction with tape operations. They are:

	Operation (Channel A)	Octal Code	Alphabetic Code	Type
1.	Read select	+0762	RDS	Data
2.	Write select	+0766	WRS	Data
3.	Write end of file	+0770	WEF	Non-Data (but executed as though it were a data)
4.	Backspace tape (record)	+0764	BST	Non-Data
5.	Backspace file	−0764	BSF	Non-Data
6.	Rewind	+0772	REW	Non-Data
7.	Transfer on End of File	+0030	TAF	Test

Table – Continued

	Operation (Channel A)	Octal Code	Alphabetic Code	Type
8.	Transfer on +0022 Redundancy Check	TAR	Test	
9.	Beginning of tape test	+0760	BTT	Test
10.	End of Tape test	−0760	ETT	Test
11.	Input-Output check test	+0760 through +0005	IOT	Test

As noted above the instructions are divided into the groups based on type. WRS and RDS are data instructions which are used to transfer data between tape and Core Storage. WEF, BST, BSF and REW are classified as non-data instructions. They are used to position tape in preparation for data operations. The other five instructions TAF, TAR, BTT, ETT and IOT are conditional test instructions. They are used by the program to check the operation for certain conditions. For example, TAF tests to see if the tape in use has sensed an End of File condition. ETT tests to see if the tape in use has reached the physical end of the tape. All of these instructions must originate in the Central Processing Unit. The control then passes to the DSU, then to the Tape Control Unit and finally to the Tape Drive.

READ SELECT (RDS)

The RDS Instruction is used to initiate a tape operation that results in reading information recorded on the tape, check it for redundancy and assemble the characters into 36 bit words. Under additional operational control from the DSU the words are then transmitted to the DSU and from there stored in Core Storage. This operation continues until the DSU signals it has received all the words called for by the program or until some condition, such as an error, indicates that no more reading is possible or practicable. Initial control is established from the Central Processing Unit and once started the control is held by the DSU channel based primarily on the amount of information desired. Combinations of operations may be performed. However, once the signal is given to stop (disconnect) a new RDS instruction is required to initiate the operation again and in some instances resynchronization with the Central Processing Unit is required. The DSU generally decides when the read operation should end. This decision is based upon information received from the program.

WRITE SELECT (WRS)

The WRS Instruction is used to initiate a tape operation that results in writing information on the tape. Under additional operational control from a DSU words are obtained from Core Storage and transmitted in 36 bits through the DSU to the Tape Control unit. The Tape Control Unit divides these words into six characters, establishes and supplies a parity bit for each character if needed and transmits the character to a 729 for recording. Information thus written is read back as previously discussed and parity checked to insure that good information was written. This operation continues until the DSU signals that all the words required by the program have been written or until some condition, such as an error, indicates that no more writing is possible or practical. Initial control is established from the Central Processing Unit and once started the control is held in the DSU based upon primarily the information desired to be written. This is established as a specific number of words to be written. Once the signal is given to disconnect, a new WRS instruction is required to initiate the operation again. If the tape is signalled to stop it will automatically write an End of Record (EOR) as part of the operation. This is inherent in the starting and stopping procedure to the tape system. The DSU generally decides when the write operation ends. This decision is based upon the information received from the program.

WRITE END OF FILE (WEF)

The Write End of File Instruction is used to initiate a tape operation that results in recording an End of File indication on the tape. This is a non-data type of instruction but the DSU is held in operation until completion of the Write End of File instruction. This is done to insure proper recognition of the End of Tape indication if such a condition should occur. Operational Write End of File instruction writes one End of File and disconnects. DSU, TCU and the tape unit all remain in operation until the Tape Control Unit establishes a disconnect after determining that the operation is completed.

BACKSPACE TAPE (RECORD BST)

The BST Instruction is used to initiate a tape operation that results in the tape being moved backward over one record. BST is a non-data type instruction. As soon as the DSU is able to condition the Tape Control Unit for this operation the DSU is disconnected and freed for another use. Backspace control is maintained in the Tape Control Unit until the Beginning of Record is reached. This is an indication that one record has been passed over before going backwards. Special conditions apply when a backspace operation encounters Load Point or an End of File indication. These are discussed in detail later, but is suffices to say at this time that if one of these indications is encountered it is treated as though the beginning of record has been reached and the tape is stopped.

BACKSPACE FILE (BSF)

The BSF Instruction is used to indicate a tape operation that results in the tape being moved backward over one file. BSF is a non-data type of instruction. As soon as the DSU is able to condition the Tape Control Unit for this operation the Data Synchronizer is disconnected and freed for another use. Backspace control is maintained in the Tape Control Unit until the Beginning of File is reached. This is an indication that one file has been passed over backwards. Special conditions apply when the backspace operation encounters both points on End of File indication. If one of these indications is encountered it is treated as though the Beginning of File had been reached and the tape is stopped.

REWIND (REW)

The REW Instruction is used to initiate a tape operation that results in the tape being moved backward to the load point. REW is a non-data type instruction. As soon as the DSU is able to condition the TCU for this operation the DSU is disconnected and freed for other operations. In addition as soon as the Tape Control Unit is able to condition the Tape Drive, the Tape Control Unit is disconnected and freed for other uses. The Tape Drive maintains control of the rewind operation until the tape has reached the load point. If the tape was previously at a Load Point, disconnect occurs immediately. Subsequent rewinds given to a tape unit which is already rewinding or has reached the load point effect an immediate disconnect.

TRANSFER ON END OF FILE (TAF)

The TAF Instruction is used to test the status of the channel A End of File indicator. If the End of File indicator is ON the program is transferred to the address specified and the indicator is turned OFF. If the End of File indicator is OFF the program takes the next sequential instruction. Each DSU channel has one EOF indicator. There are six transfer on End of File instructions, one for each channel, as follows: TBF, TCF, TDF, TEF and TFF. The End of File indicator is turned ON by tape when the tape control unit disconnects on an End of File condition while reading. It can only be turned OFF by the test instruction or by a manual reset operation. The TAF Instruction is executed by the Central Processing Unit asynchronously with the tape operation. The only timing relationship being between the read operation and the test instruction is the sequence in the program in which the test instruction is given. Synchronism is possible only in that the program may be held up until the tape operation is complete. What has been said in regard to the TAF instruction applies equally as well to the same transfer instructions on other channels.

TRANSFER ON REDUNDANCY CHECK

The TAR instruction is used to test the status of the Channel A test check indicator. If the tape check indicator is ON the program transfers to the address specified and turns the indicator OFF. If the tape check indicator is OFF the program takes the next sequential instruction. Each DSU has one tape check indicator, but there are six possible transfer on redundancy check instructions, one for each channel, TAR, TBR, and so forth. The tape check indicator is turned ON when the TCU tape check indicator is turned ON. This is the result of one of a number of error conditions being detected by the Tape Control Unit, which error conditions have been discussed briefly previous to this explanation. The DSU tape check indicator may be turned OFF only by the test instruction or by manual reset. The transfer on redundancy instructions are executed by the Central Processing Unit asynchronously with the tape operation. The only timing relationship between the tape operation and test instruction being the sequence in the program at which the test instruction is given. Synchronism is possible only in that the program may be held up until the tape operation is complete.

BEGINNING OF TAPE TEST (BTT)

The BTT instruction is used to test the status of the BOT indicator in the DSU channel. If the BOT indicator is ON the program takes the next sequential instruction and turns the indicator OFF. If the indicator is OFF the program skips one instruction. Each DSU channel has one BOT indicator and there are six BTT instructions, one for each channel. The BOT indicator is turned ON when a BST or BSF instruction is given to a tape drive unit that is at load point. The indicator can be turned OFF only with the test instruction or with a manual reset operation. The BTT instruction is executed by the Central Processing Unit asynchronously with tape operation. Synchronism is possible only if the program is held up until the tape operation is complete.

END OF TAPE TEST (ETT)

The ETT Instruction is used to test the status of the End of Tape indicator located in the DSU channel. If the End of Tape indicator is ON the program takes the next sequential instruction and turns OFF the indicator. If the indicator is OFF the program skips 1 instruction. Each DSU channel has one End of Tape indicator and there are six ETT instructions, one for each channel. The Data Synchronizer End of Tape indicator is turned ON when the Tape Control Unit tape indicator is turned ON. In the Tape Control Unit, tape indicator is turned ON when the tape drive unit indicator is turned ON. The Tape Drive Unit tape indicator is turned ON when the selected tape unit detects the End of Tape reflective spot which corresponds to the physical End of Tape while executing a Write operation. This may be either a Write or Write End of File operation. The DSU End of Tape indicator can be turned OFF only with the test instruction or by manual reset operation. This instruction is executed by the Central Processing Unit asynchronously with tape operation. Synchronism may be obtained only by programming to hold up the Central Processing Unit until the tape unit has completed a given operation.

INPUT-OUTPUT CHECK TEST (IOT)

The IOT instruction is used to check the status of the Input-Output Check Indicator located in the Central Processing Unit. If the indicator is ON, the program takes the next sequential instruction. If the indicator is OFF, the program skips one instruction. The IO indicator is turned ON if there is a possiblity of input or output data being lost, which occurs when a Reset and Load channel or Load channel instruction is given to a channel that has not been previously placed in operation by a Select instruction. It also occurs due to a channel not getting B time to satisfy its requirement. This would be in the case of a tape unit asking for a word to Write and no word being available or in the case where the tape unit is supplying a word while reading and the previous word in the Tape Control Unit has not been stored. The IOT instruction is executed by the Central Processing Unit asynchronously with the tape operations and synchronism may be obtained only by programming to hold up the Central Processing Unit until the tape unit has completed a given operation.

INSTRUCTION CODES

With reference to the previous chart the instruction codes for tape operations are multipurpose and the data and non-data instructions are similar in their binary make-up. It will be noted that the primary opera-

tion 76 is arranged to set up further decoding in the Secondary class and Unit decoders. The secondary operation is specified as the type of operation to be performed and the address portion of the instruction is used as a combination decoder and address selector. Positions 24 through 26 of the instructions specify the channel to be used 1 through 6. The class address portion specifies the type of I/O device and for tape the mode of operation. For binary mode of operation the class address is $221_8 - 232_8$. For binary coded decimal mode, the class address is $201_8 - 212_8$. This places binary or binary coded decimal mode under control of a bit in position 31 of the instruction word. The unit address specifies which individual unit of the type specified by the class address is to be used. The six select instructions used by the tape system are all decoded in the manner above and only RDS, WRS and WEF specify the mode (Binary or Binary Coded Decimal) of operation. BST, BSF and REW are not affected by mode.

Test instructions may be divided into two categories: Transfer and End of File and Transfer on Redundancy Check or Conditional Transfer instruction. The decoding of these instructions is a function of the sign, primary operation 00 and the combination of bits in positions 7 through 11 of the operation code. The channel to be tested is specified by the operation code and not by any address function. The other category consists of Beginning of Tape Test and End of Tape Test under skip instructions. These instructions are decoded as a +0760 (BTT) and − 0760 (ETT). For these instructions the channel to be tested is specified by the address portion of the instruction and the Input-Output check test instruction is a single test instruction of the skip type. The instruction is decoded as a sensed type (+0760) and has an address of 0005_8. No channel is specified since there is only one indicator located in the Central Processing Unit which is set by any of the channels. TCU and TDU operation is summarized in the block diagrams of FIGS. 272*a* and *b*.

STORE CHANNEL A SCA (+0640)

This instruction causes the contents of the DSC Address Register to be placed in positions 21 through 35 of the Storage Buffer Register (Sense Amplifier Buffer), FIG. 2*ll*; the contents of the Location Register (FIG. 2*gg*) in the DSC to be placed in positions 3 through 17 of the Storage Buffer Register, FIG. 2*ll*; a one to be placed in position S of the Storage Buffer Register if the A (position S) indicator is ON in Channel A; place a one in position 1 of the Buffer Register if the B (position 1) indicator is ON; place a one in position 2 of the Buffer Register if the C (position 2) indicator is ON and place a one in position 19 of the Buffer Register if the position 9 Indicator (FIG. 165*c*) is ON. The contents of the Storage Buffer Register are then placed in Storage at the Address specified in the SCA instruction. The contents of the DSC registers in Channel A are unchanged. If DSC A is not attached when a SCA instruction is given, the SCA is executed as though a DSC were attached having registers containing "zeros" and the location is Storage specified by the address in the instruction is cleared. An SCA instruction may be executed at any time except while the DSC is changing commands. Store Channel B, C, and D, E and F perform a like function and differ only in the operation codes SCB − 0640, SCC + 0641, SCD −0641, SCE + 0642 and SEC − 0642.

LOAD CHANNEL A LCA (+0544)

This instruction contains an address to which reference is made in Core Storage for a DSC Control Word.

If Channel A is selected with a Select instruction, the Address referred to in Storage plus 1 replaces the contents of the Location Register in the DSC A, FIG. 2*gg*, the contents of the positions 3 through 17 of DSC control word replace the contents of the Word Counter, FIG. 2*oo*, and the contents of the positions 21 through 34 of the Control Word replace the contents of the Address Register, FIG. 2*qq*. If position S of the Control Word is a "one," the S indicator (A trigger) is turned ON; if the contents of position "one" of the Control Word is a one, the 1 Indicator (B trigger) is turned ON; if the contents of positions 2 of the control word is a 1, the 2 Indicator (C trigger) is turned ON; and if the contents of position 19 of the Control Word is a "one" the 19 Indicator is turned ON (FIG. 2*eee*). If Channel A is selected but is still executing a Control Word, the Central Processing Unit waits until the Word Count is reduced to "zero" or in the case when a tape is being read while the B trigger (2 Indicator) is ON, the CPU waits until the End of Record is reached before executing the Load Channel Instruction. If Channel A is not selected, the I/O Check Light Indicator is turned ON and the LCA Instruction is interpreted as no operation. What has previously been said regarding the Load Channel Instruction relating to Channel A applies to Channels B, C, D, E and F with the exception that the operation codes are changed as follows: LCB − 0544; LCC + 0545; LCD − 0545, LCE + 0546 and LCF − 0546.

RESET and LOAD CHANNEL A RLA (+0540)

This instruction is the same as the Load Channel A instruction except that the Central Processing Unit does not wait until the word count is reduced to "zero" or until the End of Record is reached before executing the instruction, but executes it immediately upon the End of the decoding cycle. The foregoing explanations of the Address contained in the LCA instruction applies to RLA as well. Reset and Load Channel B, C, D, E and F perform a like function and differ only in that the operation codes are RLB − 0540; RLC + 0541; RLC − 0541; RLE + 0542; and RLF − 0542.

TRANSFER OF DSC A in Operation (TAO + 0060)

If DSC A is in operation when this control word is executed, the CPU takes its next instruction from the Location specified by the address in the control word (TAO) and proceeds from there. If the DSC is not in operation, the CPU takes the next instruction in sequence in the usual manner. The operation of the DSC is not affected. Transfer on DSC B, C, D, E and F operate in a like manner with the operation codes of TBO + 0061; TCO + 0062; TDO + 0063; TEO + 0064; and TFO + 0065, respectively.

TRANSFER ON DSC A Not In Operation (TAN − 0060)

If DSC A is not in operation, the Central Processing Unit takes its next instruction from the location in Storage specified in the control word (TAN) and proceeds

from there. If the DSC is in operation, the CPU takes the next instruction in sequence in the usual manner. The operation of DSC A is not affected. Transfer on DSC B, C, D, E and F operate in like manner with the operation codes of TBN – 0061; TCN – 0062; TDN – 0063; TEN – 0064; and TFN – 0065 respectively.

The following is a summary of the foregoing instructions all of which are indexable and indirectly addressable:

TABLE III

Operation Code Alphabetic	Octal	Instruction
LCA	+ 0544	Load Channel A
LCB	– 0544	Load Channel B
LCC	+0545	Load Channel C
LCD	– 0545	Load Channel D
LCE	+ 0546	Load Channel E
LCF	– 0546	Load Channel F
RLA	+ 0540	Reset and Load Channel A
RLB	– 0540	Reset and Load Channel B
RLC	+ 0541	Reset and Load Channel C
RLD	– 0541	Reset and Load Channel D
RLE	+ 0542	Reset and Load Channel E
RLF	– 0542	Reset and Load Channel F
SCA	+ 0640	Store Channel A
SCB	– 0640	Store Channel B
SCC	+ 0641	Store Channel C
SCD	– 0641	Store Channel D
SCE	+ 0642	Store Channel E
SCF	– 0642	Store Channel F
TAF	+ 0030	Transfer on DSC A End of File
TAN	– 0060	Transfer on DSC A Not in Operation
TAO	+ 0060	Transfer on DSC A In Operation
TAR	+ 0022	Transfer on DSC A Redundancy Check
TBF	– 0030	Transfer on DSC B End of File
TBN	– 0061	Transfer on DSC B Not in Operation
TBO	+ 0061	Transfer on DSC B in Operation
TBR	– 0022	Transfer on DSC B Redundancy Check
TCF	+ 0031	Transfer on DSC C End of File
TCN	– 0062	Transfer on DSC C Not in Operation
TFCO	+ 0062	Transfer on DSC C in Operation
TCR	+ 0024	Transfer on DSC C Redundancy Check
TDS	+ 0031	TRansfer on DSC D End of File
TDN	– 0063	Transfer on DSC D Not in Operation
TDO	+ 0063	Transfer on DSC D in Operation
TDR	– 0024	Transfer on DSC D Redundancy Check
TEF	+ 0032	Transfer on DSC E End of File
TEN	– 0064	Transfer on DSC E Not in Operation
TEO	+ 0064	Transfer on DSC E in Operation
TER	+ 0026	Transfer on DSC E Redundancy Check
TFF	– 0032	Transfer on DSC E End of File
TFN	– 0065	Transfer on DSC F Not in Operation
TFO	+ 0065	Transfer on DSC F in Operation
TFR	– 0026	Transfer on DSC F Redundancy Check

The addresses of the I/O units are as follows:

Component		DSC	Octal	Decimal
Tapes				
	BCD	A	1201-1210	641-648
		B	2201-2210	1153-1160
		C	3201-3210	1665-1672
		D	4201-4210	2177-2184
		E	5201-5210	2689-2696
		F	6201-6210	3201-3208
	Binary	A	1221-1230	657-664
		B	2221-2230	1169-1176
		C	3221-3230	1681-1688
		D	4221-4230	2193-2200
		E	5221-5230	2705-2712
		F	6221-6230	3217-3224
Card Reader		A	1321	721
		C	3321	1745
		E	5321	2769
Card Punch		A	1341	737
		C	3341	1761
		E	5341	2785
Printer				
	Normal	A	1361	753
		C	3361	1777
		E	5361	2801
	Binary	A	1362	754
		C	3362	1778
		E	5362	2802
Drum		Not Used	301-310	193-200
CRT		Not Used	0030	0024

From the preceding description, the effect of the Indicators S, 1 and 2 on the operation may be generalized in the following manner: With reference to Table I, it will be noted that indicators S, 1 and 2 may be considered an octal group where position S corresponds in binary order to the exponent of 2, position 1 corresponds in binary order to the exponent of 1, and position 2 corresponds to the exponent of 0. Accordingly, the command codes for indicators S, 1 and 2 are tabulated with the octal equivalents:

	S	1	2		
IOCD					
0	0	0		I/O with Count Control and disconnect	
TCH	0	0	1	Transfer in Channel	
	0	1	0	I/O of a record and proceed	IORP
	0	1	1	I/O of a record and transfer	IORT
	1	0	0	I/O with count control and proceed	IOCP
	1	0	1	I/O with count control and transfer	IOCT
IOSP	1	1	0	I/O until signal then proceed	
IOST	1	1	1	I/O until signal then transfer	

DSC INDICATORS

Each DSC includes a set of Status Indicators which may be turned on during tape operations. The status of

any of these indicators may be tested through the use of the appropriate test instructions in the stored program, for example, Transfer on Redundancy Check, End of Tape Test (−0760) and I/O Check Test (+0760 . . . 0005). An indicator if ON is automatically turned OFF when tested.

BEGINNING OF TAPE INDICATOR (FIG. 183)

Small strips of adhesive aluminum material are placed a few feet from each end of the tape (as previously mentioned) which are used to indicate the Beginning of Tape (Load Point). Any instruction which attempts to backspace the tape beyond its load point turns ON the Beginning of Tape Indicator in the DSC to which the Tape unit is attached.

The Beginning of Tape Indicators may be turned ON if the tape is at its Load Point and if BST, BSF or REW instruction is given. If the tape is positioned after any record in the first file then three BSF instructions turn the indicator ON. The first BSF positions the tape at the beginning of tape gap near the Load Point. The second BSF returns the tape to its Load Point and the third BSF then turns ON the indicator. If the tape is positioned after the first Record of the first File, then four BST instructions turn the indicator ON. The first BST moves the tape to the beginning of the first record, the second BST positions the tape to the beginning of the tape gap, the third BST returns the tape to its Load Point, the fourth BST turns ON the indicator. To test whether or not a specific Backspace instruction has turned the indicator ON, the instruction is followed by a Channel Delay Instruction and then a BTT instruction. The Channel Delay instruction delays the master program in the SPU until the execution of the Backspace instruction has begun in the DSC. If the tape is positioned at the Beginning of Tape, the Backspace instruction turns ON the indicator as soon as it enters the Tape Control Unit and at the same time the DSC is disconnected. Thus, BTT instruction cannot be executed before the Indicator has been turned ON.

END OF TAPE INDICATOR (FIG. 184)

When the aluminum strips marking the End of Tape is reached during writing, the End of Tape Indicator in the DSC to which the Tape Drive Unit is attached is turned ON. No interruption of the Writing process occurs so that the Writing operation may be completed even though the End of Tape Mark has been passed over. This indicator is never turned ON while reading.

The End of Tape indicator can be turned ON only during the execution of the WRF or WEF instruction and the specified DSC remains in operation after the execution of either of these instructions until the Tape Drive Unit is disconnected. Therefore, the combination of the WRS and WEF followed by Channel Delay and an ETT instruction determines whether or not the End of Tape mark has been passed at any time prior to the writing of the closing End of Record Gap. Should the physical end of tape mark be encountered after the Tape Unit has been disconnected, then the DSC's end of Tape Indicator is turned ON but is not recognized until a succeeding ETT instruction is executed. This situation occurs when an End of Tape Mark follows an End of Record Gap and insures that no more than one record is written following the physical End of Tape mark.

REDUNDANCY CHECK INDICATOR (FIG. 185)

The Redundancy Check Indicator us turned ON at any time during a magnetic tape read or write operation. When ON this indicator signals than an error has occured in the reading or writing of the tape and when reading, the indicator may be turned ON even if information is not being transmitted to Core Storage. For example, if a Tape Drive Unit has been logically disconnected from the system and is merely spacing to the next End of Record Gap, an indicator is turned ON if an error is sensed during this period. Also, in the read status, where the control word has indicator 19 ON and indicators S, 1 and 2 OFF, the word count specifies the number of words on tape to be read and skipped and not transmitted to Core Storage. In this instance the Redundancy Check Indicator is turned ON and may be tested although the words have not been transmitted to Core Storage.

END OF FILE INDICATOR (FIG. 187)

The End of File Indicator in a DSC is turned ON at any time an End of File Gap is encountered during a reading operation. An End of File Gap may be written on a tape at any time by the Write End of File (WEF) instruction. This indicator is not turned ON when an End of File is written. An End of File gap is automatically written after the last record has been placed on tape in a peripherial Card to Tape operation.

PROGRAMMED CHANNEL DELAY

In programming Input-Output operations, it is sometimes desirable to synchronize the testing of the DSC Indicators with the Input-Output process. Load Channel, Store Channel, Transfer in Operation and Transfer Not in Operation Instructions provide flexibility in the master program ability to synchronously control Input-Output operations. One way to hold a master program at a given point consists of placing a Control Word Transfer in Operation at a predetermined location. The master program repeatedly executes the Transfer in Operation instruction until the specified Data Synchronizer Channel is logically disconnected. This is called a Channel Delay. Channel not in Operation may be determined from the following table:

TABLE IV

Select Instruction	Channel in operation Until	Tape Control in Use	Tape Drive Unit In Use Until
RDS	Last Storage Reference has been made	End of Record	End of Record
WRS	Longitudinal Check character is read	End of Record Written	End of Record written
Write End of File (BCD)	End of File gap written	End of File Gap and Tape Mark Written	End of File, Gap and Tape Mark Written

TABLE IV—Continued

Select Instruction	Channel in operation Until	Tape Control in Use	Tape Drive Unit In Use Until
Write End of File (Binary)	End of File gap written	End of File Gap written	End of File gap written
BST	Tape Control and Tape Drive Units Selected	Beginning of Record or File Gap +25 milliseconds	Beginning of Record or File Gap +25 milliseconds
BSF	Tape Control and Tape Unit Selected	Beginning of File Gap +25 milliseconds	Beginning of File Gap +25 milliseconds
REW	Tape Control and Tape Unit Selected	Tape Unit Selected	Load Point

TESTING DSC INDICATORS

During any writing operation, if a Channel Delay instruction is followed by a Transfer on Redundancy Check instruction the master program is delayed until the writing operation is complete before the test is made. When the test is made, all bits including the Longitudinal Redundancy Bits of the last record written are checked. If a record is read by any combination of DSC Commands, for example, an IORP command followed by an IOCD command with a word count of 0, a similar situation prevails. A Channel Delay followed by Transfer on Redundancy Check provides a check on all bits including the Longitudinal Redundancy bits for the last record read. When Word Count control is used to control the reading process, for example, an IOCD with a word count of N words, a Channel Delay followed by a Transfer of Redundancy Check insures that for the N words read the lateral and only the lateral check bits have been checked. When an End of File condition occurs following an RDS, the DSC End of File indicator is turned ON and the reading operation is terminated immediately. Thus, if a Channel Delay instruction is given at some point subsequent to a Read operation and is followed by a Transfer on End of File instruction, the transfer condition is met if the DSC End of File indication is ON. The WEF instruction writes an End of File Gap if executed in the binary mode or writes an End of File Gap plus a Tape Mark if executed in the binary coded decimal mode. The recognition of an End of File then differs depending upon the mode of the RDS instruction being executed when the End of File is reached and, in the binary mode, an End of File condition is met when approximately 33 milliseconds of blank tape has been read and, in the BCD mode, an End of File is determined by the presence of the tape mark.

CPU INTERRUPT OF DSC

Since the Data Synchronizer Channel may operate from a Stored Program autonomously taking instructions from ascending locations in Storage, it is pointed out that the CPU has option at any time to interrupt or alter this preordained set of commands to a Data Synchronizer Channel in a number of ways. One way is to give a Reset and Load Channel Instruction referring to a command in Core Storage of all zeros which causes an immediate disconnect of the channel. Another way is to fail to provide a Load Channel instruction to a DSC before it has disconnected after an operation. Another way is for the CPU to wipe out or destroy the table of Commands in Core Storage to which the DSC is referring which has the effect of providing a disconnect to the Data Synchronizer Channel. Still another way is by the insertion of a special control word, FIG. 3g, within the sequence of DSC control words which sets the Location Register to any arbitrary value. In this instance, if a control word in interpreted which has the C trigger ON (a bit in position 2 causing the Indicator 2 to be ON) and has both the S and 1 Indicators OFF (Bit positions S and 1 both zeros), the Address part of the special control word is interpreted as the location of the next control word replaces the contents of the Location Register, and the control word at the address specified by the Location Register is transmitted from Storage to the Data Synchronizer Channel.

Another way of interrupting a set of commands is by the failing to give a Load Channel instruction. A Load Channel instruction is not executed until the DSC to which it refers has completed the execution of its current operation but if the Load Channel is not waiting when the DSC has completed its operation, the DSC is disconnected. If a Load Channel Instruction is given when the Channel is no longer in operation and has not been selected, an I/O Check Light is turned ON and the CPU proceeds to the next instruction in sequence.

The Load Channel Instruction is a synchronizing type of instruction and instead of causing an abrupt disconnect, alters or transfers the Data Synchronizer Channel sequence of operation from one table of commands in Core Storage to another table of commands in Core Storage specified by the CPU. Thus, complete flexibility is permitted. The use of a Load Channel Instruction as a synchronizing device between the CPU's calculating operations and the Input-Output units asynchronous operations may be carried to the extreme where on every single word transmitted to or from an Input-Output device and Core Storage, the CPU is completely synchronized with DSC by a Load Channel Instruction which provides a command with a Word Count of one, in which case every single word requires a new Control Word and the execution of a synchronous Load Channel Instruction. On the other hand, this extreme situation need not be maintained and any number of words may be transmitted between synchronizing points by means of the Load Channel Instruction. This is solely determined by the CPU providing a command having a Word Count of N.

It may be required during the course of computation to alter or interrupt an Input-Output operation, for example, when the Real Time device of 1.34 of FIG. 1 is used in the system. If a reset and Load Channel Instruc-

tion is given when an Input-Output operation is taking place, a new command is loaded into the DSC immediately from the address specified by the Reset and Load Channel Instruction as set forth previously in the definition of the Reset and Load Channel command. This may be used to change the sequence or to interrupt an Input-Output program. However, if it should be desired to return to the Input-Output operation which was taking place when interrupted, the Reset and Load Channel Instruction may be preceded with a Store Channel Instruction, the latter being effective to store the contents of the Address Register, the contents of the Location Register and the Indicator triggers as S, 1, 2 and 19 in the Address specified in the Store Channel instruction while leaving the contents of these registers unchanged. Following this with a Reset and Load Channel instruction causes these registers to be reset. When it is desired to return to the Input-Output operation, a Reset and Load Channel instruction specifying the Address to which the Store Channel instruction referred, brings into that channel's registers the former contents held when the interruption took place.

CHANNEL STORAGE OF COMMANDS

Any single one of the Input-Output units such as Tape Drive Unit, Card Reader, Printer or Punch may be selected and in operation transmit information in its DS channel at any given time. However, certain non-data transmitting functions concerning tape such as Backspace Record, Backspace File or Rewind may occur simultaneously with a data transmission operation in any given channel. The registers in a Data Synchronizer Channel are divided into general types: Operation and Data Transmission. One type of Operation Register is for the purpose of determining and remembering a class or type of unit; the function to be performed such as reading tape or writing with the printer; and the particular unit in the case of tape such as Tape Drive Unit 1 through 8. The second type of Operation Register is used exclusively for the control and the record keeping of the transmission of information between a selected Input-Output unit and Core Storage. Both types of Operation Registers are completely interlocked with each other, with the Central Processing Unit, and with the Input-Output Units to provide a high degree of versatility. There are three Operation registers of the first type in each channel. The first is the Class Register, FIGS. 173*a* and *b*, which stores the type of Input-Output unit selected and the purpose for which selection is made such as Write Tape, Read Tape, Read Printer and so forth. The second Operation Register is the Units Select Register, FIGS. 179*a* and *b*, which designates which of the units is to be read or written, and the third such register is the Non-Data Select Register, FIG. 176, which stores information that does not pertain to data transmission and generates signals for the purpose of positioning Input-Output units in preparation for the transmission or receipt of information.

The program in Core Storage enters the Central Processing Unit in sequential order where the instructions are decoded, and an instruction line is energized. In a case of an Input-Output operation, the control word refers to a Data Synchronizer Channel so designated by the Address portion of the instruction which determines the Data Synchronizer Channel involved and refers to the operation designated by the operation part of the word which provides the Operation Registers of that channel with information concerning the operation such as writing, reading, backspacing and so forth. It also designates the class, such as tape or card, and finally the unit, such as units 1, 2, 3 through 8. The Operation Registers retain this information and the Data Synchronizer Channel immediately transmits a signal back to the Central Processing Unit permitting the latter to end operations on this particular instruction and then to proceed to the next one, thus leaving the Central Processing Unit completely free to once again make reference to Core Storage to receive the next instruction. As soon as the Operation Registers have been loaded, the Data Synchronizer Channel makes a test of the specified Input-Output units which takes into account the class as well as the function which is to be performed and tests for the availability of the unit. If the unit is not immediately available, the Data Synchronizer Channel continues to store the operation information until the specified Input-Output unit is available at which time information is transmitted, from the Operation Registers to the Input-Output unit to set it in motion and place it in the required status. Certain information taken from the Control Word is not retained in the Data Synchronizer Channel as in the case when the instruction is of the non-data transmitting type (instructions which do not require the use of a DSC for the transmission of data such as Rewind). After such information concerning the function has been transmitted to the Input-Output unit specified, the information is no longer retained. It is pointed out that in the data transmitting type of instruction the DSC's do not retain information as to which unit was previously specified although the Operation Registers retain information pertaining to the class and function after having transmitted such signal to the Input-Output unit involved. When information pertaining to the unit has been transmitted to the unit, a signal is returned to the DSC allowing the Unit Selection Register to be reset. The purpose of this feature is to permit the Central Processing Unit to provide still another instruction to this same DSC provided that such instruction is of the non-data transmitting type, in which case such information previously stored in the Data Synchronizer Channel by the transmitting type of instruction may now be entered and remembered in the Operation Registers leaving the Central Processing Unit free for operations. When the data transmitting type instruction has been sent from the Operational Registers of the DSC and from the latter to an Input-Output unit, the data Synchronizer Channel is now free to immediately receive a second non-data transmitting instruction from the Central Processing Unit and store this information awaiting execution of the previous data transmitting instruction of the DSC. Accordingly, the Central Processing Unit is free to refer to Core Storage for still another instruction. Within a specified period of time following a Select Instruction, the Central Processing Unit must provide another instruction to the Input-Output unit by way of a DSC which conditions the Transmission Registers. If this latter instruction is not received, the Input-Output units selected recognize this fact through their tests and automatically signal the DSC and the latter is disconnected.

Further provision for stacking operations in the data channel is provided. The Tape Unit Selectors, FIGS. 254*a* and *b*, retain the fact that the specified one of the

Tape Units is selected. Data Class Selection triggers, FIG. **255**, retain the class of operation and the mode, for example read, write, binary or binary coded decimal mode. Non-data Class Selection trigger, FIG. **256**, retains the non-data class operation Rewind, Backspace Record, Backspace File, Write End of File and End of Tape.

CHARACTER GATES AND CLOCKS

The first bit of a character from tape is sent from the High Clip Read Register outputs, FIG. **228**, to the seven way OR Circuit of FIG. **246**, where the line **246.10** First Bit (Start Character Gate) line comes up. The First Bit line enters a Character Gate, FIG. **250**, is inverted, and the negative shift turns ON the Character Gate trigger. The outputs of this trigger start the Read Clock, FIG. **251**, in operation. Initially in the Read Clock, Trigger **1** is ON and Triggers **2, 3, 4** and **5** are OFF when the Character Gate line comes up as previously described. The output of a 476 KC Crystal controlled oscillator, FIG. **249**, is provided on the line **249.03** where it is gated by the Character Gate to the inverter to provide a binary input to the Ring Drive Pulse Generator. The first pulse provided by the Pulse Generator turns OFF Trigger **1** by way of its Diode Gate (D_G) since the Diode Gates for T_2, T_3, T_4 and T_5 are blocked by their respective triggers being in the OFF condition. However, the pulse to the Diode Gate associated with Trigger **1** turns T_2 ON in addition to turning T_1 OFF. Turning OFF T_1 provides a bias via the Cathode Follower to its Diode Gate to prevent other input pulses which follow from turning T_2 OFF later in the Clock Cycle. Since T_2 is now ON, the bias applied to its Diode Gate through the Cathode Follower is removed. Accordingly when the next pulse comes through the Ring Drive Pulse Generator, it can reach T_2 and turns the latter OFF, and in addition it is applied to the input of T_3 to turn the latter ON. When T_2 is turned OFF, the bias to its Diode Gate is reapplied through the Cathode Follower so that succeeding pulses during this Character Gate are ineffective to turn T_3 ON. T_3 is now ON and the input from the Cathode Follower to the Diode Gate is more positive due to the right hand plate being up which conditions T_3 for the receipt of a Turn OFF pulse. Additional outputs of T_3 are taken off on the lines **251.02** and **251.03**. Tape Mark Sample (TM SAmple) **251.02** goes to Character and Record controls, FIG. **245**, and to Class and Unit Disconnect Gates and Start Read/Write, Write End of File, FIG. **252**, where it is combined with Initiate Read Delay line **240.13** to provide an output on the line **252.03**. The next successive pulse from the Ring Drive Pulse Generator turns OFF T_3 and at the same time turns ON T_4. The turning ON of T_4 provides a Read T_4 output from the line **251.08** to Low Clip Error Sample and Sample Pulses, FIG. **236**; turns ON T_5; and conditions the Diode Gate associated with T_4 for the next pulse from the Ring Drive Generator. T_5 produces outputs on three lines. Read T_5 output line **251.05** goes to the Character Gate of FIG. **250**, where it is ineffective to turn OFF the Character Gate trigger because the latter requires a negative shift input. Line **251.06** goes to Character Record Control, FIG. **245**, and line **251.07** is provided to the Tape Group Counter Shift Left Six Pulse controls, FIG. **226**. Output line **251.07** is also provided to Low Clip Error and Sample and Sample Pulses, FIG. **236**. T_5 output and T_3 output combine to bring up a line **251.04**. The next pulse from the Ring Drive Pulse Generator turns OFF T_4 since its Diode Gate has previously been conditioned by the fact that T_4 was ON. Also, the same pulse is applied to an input T_1 to turn ON the latter. When T_1 is ON, it biases its Diode Gate for the reception of the next succeeding signal from the Ring Drive Pulse Generator on the same Character Gate Cycle and Triggers **2, 3** and **4** are turned ON in the manner previously described. However, since the output of trigger **4** is a binary input to trigger **5**, this sequence of operations causes T_5 to turn OFF and it is this negative shift on the line **251.05** that turns OFF the Character Gate, FIG. **250**. It is pointed out in review that T_1 was turned OFF at the same time that T_2 was turned ON and then T_3, T_4 and T_5 were turned ON in sequence. T_5 remained ON while T_1, T_2, T_3 and T_4 were turned ON again in sequence. On the fall of T_4, T_5 was turned OFF and the Character Gate was reset. The 476 KC Oscillator has a period of 2.1 microseconds which provides an output of the Ring Drive Pulse Generator of about 2.1 microseconds and each trigger is either turned ON or turned OFF by one of these pulses. Accordingly, the time during the Character Gate that T_1, T_2, T_3 and T_4 are turned ON is 4.2 microseconds, and T_5 is turned ON for a period of 16.8 microseconds, or 4 times the duration that each of the other triggers is ON during the character cycle. Since one Ring Drive Generator Pulse is required initially to turn OFF T_1, the total time of the Character Gate is slightly more than 7½ 4.2 microseconds cycles or approximately 33.6 microseconds. The purpose of the 33 microsecond Character Gate is to provide that all information of that character on tape be read within 33 microseconds. If there has been extreme skew of the tape and this character is not read in 33 microseconds, the Parity Checker of the LRC Check Register, FIG. **231**, indicates an Error and the Indicator Tape Check is turned ON.

Other than providing a measured Character Gate of **33.6** microseconds, the Read Clock provides timed impulses RD T_3, RD T_5, RD T_4 to Low Clip Error and Sample and Sample Pulses, FIG. **236**; an output on Tape Mark Sample line **251.02** to Character and Record Controls, FIG. **245**; and RD T_3 and RD T_5 outputs to the −12 Volt Clamp Reset Pulse Generators, FIG. ***257a***, for providing a Y Reset Pulse which in turn provides Line Register Reset on line ***257b*.01** of the −12 Volt Clamp Reset Supplies, FIG. ***257b***. It also provides the Read T_5 Clock Pulse Output **251.07** to the Tape Group Counter and Shift Left Six Pulse Controls, FIG. **226**; a Read T_3 Output on the line **251.03** to Class and Unit Disconnect Gate and Start Read/Write, Write End of File Control, FIG. **252**. A Character Gate is provided on the Clock Gate Line **250.11** to the Beginning of Record, Beginning of File Search and Record Gate, FIG. **244**, to provide a Record Gate by the way of a Record Gate Single Shot (SS_D) which is a holdover Single Shot with a 150 microsecond output duration. When a pulse is applied to its input, the Single Shot turns ON for 150 microseconds. However, if before the 150 microsecond period is ended another pulse is applied, it causes the Single Shot to stay ON for another 150 microseconds and the Single Shot holds for as long as pulses are applied before the completion of a time duration of 150 microseconds. However, if the Single Shot fails to receive a pulse during a 150 microsecond interval, the Single Shot turns OFF and the Gate which is provided

therefrom is ended. The Character Gate is provided for each group of six bits, and for each word written on tape there are six groups of six bits which calls for six Character Gates per word. In this case, the Single Shot holds over for 150 microseconds and falls at the end of the Record Gate. The falling of the Record Gate Generates a Disconnect Delay Pulse on the lines **245.03 – 245.06** which is 400 microseconds in duration by turning ON the Single Shot SS_E in Character and Record Controls, FIG. **245,** by way of the line **244.01.** The 400 microsecond pulse is sent to the DSU and is used as an early End of Record for telling the DSU that the TCU is going to disconnect. At the end of this 400 microsecond pulse, the TCU generates a Disconnect pulse of 25 microseconds which completely disconnects the Tape Control Unit, resets the Write trigger, and resets the Unit Trigger that was set at the beginning of the Write operation. The fall of the Character Gate line **250.13** provides a negative shift for turning OFF the first Character Gate Trigger which provides an output on the line **247.03** to a Character Record Control, FIG. **245,** where it is combined with Tape Mark Read T_3 Select Ready and Read T_5 output to Not Backward.

WRITE CLOCK GATE

The Write Clock Gate is included in Clock Write Pulse Line Register Reset controls, FIG. **249.** An input pulse is provided on the Write Clock Gate Line **248.04** where it is combined with the output from the **476** KC Oscillator to provide input pulses to the Special Self Gated Binary Input trigger which functions in the manner of the Ring Drive Pulse Generator of the Read Clock. Trigger T_1 is on initially and is cut-off by the first Ring Drive Pulse and, in turn, T_2, T_3, T_4 are turned ON in sequence for duration of 4.2 microseconds. T_5 is turned ON and then T_1, T_2, T_3 and T_4 are turned ON sequentially. The fall of T_4 turns OFF T_5 which has been on for 16.8 microseconds. When T_5 is turned OFF, it turns ON T_6 by way of the latter's binary input. When T_5 turns ON, it is ineffective to turn T_6 ON and when T_3 is next ON, all inputs to the AND circuit are up and the Write Pulse Generator is turned ON. When T_6 is turned OFF by T_5 going OFF, the negative shift turns the Write Pulse trigger OFF. The ON duration of the T_6 is 33.6 microseconds.

The Write Clock Gate **248.04** is controlled by a line **194*a*.01** from the DSU called Write Clock Control. When the DSU receives a tape demand from the TCU and determines that it has no more information to write on tape, the Write Clock Gate comes down stopping the Write Clock. While the Write Clock is generating Write pulses, these pulses are fed by way of the line **249.01** to a Character and Record control, FIG. **245,** as an input Write Pulse to a 275 microsecond Single Shot, Write Check Character Delay, which is a hold-over Type Single Shot of the type that continues to hold over as long as Write Pulses are being generated. At the time that the Write Clock control line falls and Write Pulses are no longer generated, the Single Shot remains ON for **275** microseconds. The Write Stop Delay Single Shot of FIG. **245** is held up by the Write Check Character Delay Single Shot for 3 milliseconds after the last Write Pulse and the Write Stop Delay Single Shot turns OFF the Go line by way of the Go Trigger Reset line **245.08** which is the Write Stop Delay line in FIG. **240.** The dropping of the Go line **240.02** tells the tape to stop and as the tape is slowing down, tape is still being read 4 milliseconds later. However, the decrease in speed is not noticeable and does not affect the reading of the last character written. The fall of the **275** microsecond SS Write Check Character Delay of FIG. **245** provides an output to a 10 microsecond SS_E Write Trigger Reset which brings up the line **245.07** and resets the Write Triggers in the Tape Drive Unit by way of the line **245.07,** FIG. **263.** This resets the Write triggers for the Tape Drive Unit. Resetting of these Write triggers causes bits to be written on tape in any position in which the Write triggers were ON and this process is used to check the characters written on tape because it makes the number of bits written horizontally on tape even.

TAPE GROUP COUNTER AND SHIFT LEFT SIX (FIG. 226)

During Reading, six groups of six bit characters are assembled to form a full word or during Writing, six bit groups are extracted and recorded serially on tape. It is imperative that it be recognized when a full word of six groups is read or written so that operations may proceed with dispatch, and this is accomplished by the Tape Group Counter and Shift Left Pulse Controls of FIG. **226.** When writing on tape, 36 bits are put in the Tape Shift Register in parallel and are taken out six bits at a time from positions S, 1 through 5, FIG. **2*xx*,** and data in this register are shifted six bits at a time to the left to keep filling up these positions with six bit groups. When tape is being read, the word is assembled serially by characters of six bits in parallel in positions 30 through 35 of the Tape Shift Register, FIG. **2*aaa*.** As six bits are received, they are shifted left until the full word is complete.

When doing a Write operation, FIG. **226,** the Write Call line **255.11** of Data Class Selection, FIG. **245,** is up or when doing a Read operation the RD T_5 Clock output line **251.07** is up. One or the other is combined with Not Backward line **239.10,** Pulse Output line **252.03,** Not Disconnect Delay line **245.01** and Minus on Write End of File Call line **256.14** to produce an output Shift Left Six Pulse on line **226.01.** The Pulse Output line **252.03** is brought up while Writing by a signal generated in response to a Write Echo from the Write Amplifier, FIG. **263,** where it will be appreciated an Echo signal is provided on the ine **263.01** for each bit written on the tape. More specifically, a Response line **245.10** and the Write Clock Gate line **248.17** in Class and Unit Disconnect Gate and Start Read/Write/-Write End of File, FIG. **252,** cooperate to provide the Pulse output while Writing. With reference to Read and Write Delay Controls, FIG. **248,** the Write Clock Gate line **248.07** is brought up by the Delayed Read/-Write Call Trigger when set and either the Write Clock Control line **194*a*.01** or the BCD Mode line **255.29** and the Write End of File Call line **256.08.** The Write Clock Control line **194*a*.01** is brought up by the Channel A Write Clock Control Trigger, FIG. **194*a*.** The Delayed Read/Write Call Trigger, FIG. **248,** is set in the following manner: The setting of the Write Call Trigger in the Data Class Selection, FIG. **255,** brings up the line **255.09** and the Start Read/Write/Write End of File line **252.01** is up in FIG. **252** since the Class and Unit Disconnect Gate Trigger if OFF and the Not TCU Disconnect line **250.01** is up. In FIG. **266,** the Select Ready and Write line **266.05** is up from the Read/Write Status Controls in the Tape Drive Unit. Since the lines **266.05,**

252.10 and **255.09** are up in Set Read/Write Control, FIG. **241**, the Start Write Schmidt Trigger (T_S) is set and the lines Initiate Write Delay **241.05** and Write Set Go **241.06** are up, the line **241.06** going to the Go/Stop Controls, FIG. **240**, to turn ON the Go Trigger and the line **241.05** going to Read and Write Delay, FIG. **248**. Since the Select at Load Point line **242.02** is up in FIG. **248** as well as Initiate Write Delay line **241.05**, both conditions of the AND circuit are met and the output of the latter goes up, is inverted, and turns OFF the Write Load Point Delay Single Shot for 40 milliseconds. Furthermore, when the Initiate Write Delay line comes up, its negative shift is felt through an inverter to the Set Write Delay 50 microsecond Single Shot. An input cannot be provided to the 8 millisecond Write Delay Single Shot until the Grounded Grid Amplifier connected thereto receives the output of its input AND circuit. Accordingly, the Write Delay Single Shot is not turned ON for 40 milliseconds. When the Write Delay Single Shot is turned ON, its right hand plate goes positive for **8** milliseconds and at the end of this period the Clock Gate Delay Single Shot is turned ON for **20** microseconds providing outputs on the Clock Gate Delay lines **248.08** through **248.12**. An additional output line is provided to the Delayed Read/Write Call Trigger where is it ineffective to set the trigger until the line falls at which time the trigger is turned ON providing outputs from Delayed Read/Write Call lines **248.01**, **248.02** and **248.03**. An additional output is combined with lines previously described in an AND circuit to bring up Write Clock Gate on the line **248.04**, Gate Response of the line **246.05**, Gate Write Echo on the line **248.06** and Gate Tape Counter on the line **248.06**. The Delayed Read/Write Call Trigger of FIG. **248** stays ON until the Disconnect Delay is provided on the line **245.05**.

The Gate Tape Counter line **248.07** is sent from Read and Write Delay, line **248.02**, to the Class and Unit Disconnect Gate and Start Read/Write/Write End of File, FIG. **252**, to provide the Pulse output on the line **252.03** when the Response line **245.10** is brought up. With reference to Character and Record Controls, FIG. **245**, the response line **245.10** rises in response to Not Backward Response Gate, Response Timing, and First Character Gate Trigger being ON. The line Not Backward **239.06** is up since the Backward Trigger of Backspace Controls, Fig. **239**, is OFF. The Response Gate line **244.05** is up since the Write Clock Gate line **248.05** is up and Minus on Write End of File Call line **256.15** is up because of the Write End of Call Trigger being OFF. The Response Timing line **250.16** is up due to the Gated Write Echo line **246.04** which provides inputs to the Response Timing Single Shot in the Character Gate and Disconnect Controls of FIG. **250**. In FIG. **245**, the Cascaded AND circuit has the Not Backward line **239.06** up as previously mentioned. The Tape Mark line **246.03** is up when the first Tape Mark comes through in response to outputs off the High Clip Read Register, FIG. **228**, once for each six bit character (recalling that what is written is read back 4 milliseconds later by the Read Head). The Tape Mark Sample Read T_3 line **251.02** is up since the Character Gate is provided on line **250.11** to the Read Clock and Line Register Reset, FIG. **251**, by way of the Character Gate Trigger of FIG. **250** which is set by the fall of the First Bit line **246.01**. The first character Gate line **247.03** is up in response to setting of the first Character Gate Trigger, FIG. **247**, by the Character Gate line **250.13** and the Go line **240.04**. The Select Read and Ready line **240.09** and Read T_5 output from the Read Clock, FIG. **251**, are up for the reasons given previously. The conditions for providing an output from a Cascaded AND circuit of Character and Record Controls, FIG. **245**, are such that the First Character trigger is set for the first character and is turned OFF by the Disconnect line **250.06** in response to the Disconnect Controls of FIG. **250**. Actually, the output on the line **245.10** is determined by the Response Timing line **250.16** which in turn is controlled by Gated Write Echoes line **246.04**, the latter providing an input to the Storage Read/Write/Write End of File Controls, FIG. **252**, for each character written.

For providing Pulse outputs on the line **252.03** during a Reading operation, FIG. **252**, the Initiate Read Delay line **240.13** and the Read T_3 output line **251.03** must be up. The Read T_3 output is up as previously described in connection with the Read Clock and Line Register Reset, FIG. **251**. The Initiate Read Delay line **240.13** is up in response to Select and Ready line **266.02**, the Read Call line **255.01** is up for so long as the Read Call Trigger of Data Class Selection, FIG. **255**, is up, and the Start Read/Write/Write End of File line **252.01** is up as previously described. Since a pulse is provided on the line **252.03** for each time that a Read T_3 output is up during a Read operation, it is apparent then that further decoding on the line **252.03** must be done during a Read operation or the count would be improper in the Shift Register. With reference to the Tape Group Counter and Shift Left Six Pulse Controls, FIG. **226**, it will be noted that the Read T_5 Clock output line **251.07** is up for essentially half of the Character Gate time. Accordingly, only one T_3 pulse per character cycle is effective at the output of the Cascaded AND Circuit of FIG. **226** to give a Shift Left Six Pulse on the line **226.01**. The Shift Left Six Pulse is provided to a Tape Group Counter comprising three binary triggers with binary inputs connected to form the Trigger Counter. The counter is reset with all the triggers OFF and the trigger T_1 corresponds to 1, the trigger V_1 corresponds to 2, and the trigger W_2 corresponds to 4. The input pulses from Shift Left Six Circuits are fed to the first stage only. The negative shift of the first pulse turns T_1 ON. The leading edge of the second pulse is ineffective to turn T_1 OFF, but the falling of the second pulse turns T_1 OFF which in turn turns trigger V_1 ON. The leading edge of third pulse does not affect T_1, but the trailing edge turns T_1 ON. The fourth pulse is ineffective to turn T_1 ON, but when it falls, it turns T_1 OFF and T_2 OFF. When T_2 is turned OFF, it turns T_3 ON. The T_1 output is down so even though trigger W_2 output is up, the conditions are not met for an output from the AND circuit and the Tape Word Complete line **226.02** is still down which causes the Tape Word Incomplete line **226.03** to be up by inversion. The fifth pulse is applied as an input to T_1 and its leading edge is inefficient to change the state of the latter but the trailing edge provides a negative shift to turn T_1 ON. At this time, Tape Word Complete line **226.02** comes up. Although only five Shift Left Pulses have come in, five shifts are all that is necessary to complete a word of six characters. The Tape Word Complete line **226.02** goes to Reset Pulse Generator, FIG. **257***a*, where it is combined with a Write Call line **255.15** and a Response line **225.01** to provide an M Reset Pulse on the line **257***a*.**02** which re-

sets the **36** trigger Shift Register by bringing up the lines **257***b*.**05** and **257***b*.**06** in −12 Volt Clamp Reset Supplies. Further, the line **226.02** is used in the Blank Generator, FIG. **259**, and in the Shift Register Controls, FIG. **260***a*, to generate a Tape Demand from the DSU on the line **260***a*.**04** which goes to Channel A Control Word Gate and EOR Synchronizing Controls, FIG. **196***a*.

During the Read operation, it is also possible to read a tape which has been written on some other system in which the six bit characters are not multiples of six. In other words, even groups of six characters are not provided. Therefore, upon reading such a tape an odd number of characters less than six may be read in which case it is necessary to generate some Blank Shift Left Six Pulses in order that the word may be upshifted to fill up the Tape Shift Register. This is accomplished by the Blank Generator of FIG. **259** which causes upshift of the characters to the high order of the Tape Shift Register so that a Tape Word Complete indication may be had.

BLANK GENERATOR (FIG. 259)

The Blank Generator operates automatically when an End of Record has been reached and the number of characters recorded is not an integral multiple of six. The Blank Generator shifts the residual characters in excess of the next lower integral multiple of six to the high order position of the 36 bit Tape Shifting Register and fills in any remaining lower orders with binary zeros. Upon completion of such manipulation the Blank Generator automatically produces an artificial demand signal causing the contents of the **36** bit Shift Register to be transmitted to the DSC Buffer Register just as normal words are transmitted. Such operation occurs only when the TCU is reading in the binary coded decimal mode since in the binary mode this operation would be unnecessary.

With reference to FIG. **259** a Read Call line **255.02** is up as previously described and the line Disconnect Delay **245.04** is only brought up for 400 microseconds after the fall of the Record Gate of FIG. **244.** With reference to the Character and Record Controls, FIG. **245,** the Not Backward line **239.06** is normally up during a Read operation and the Record Gate line **244.03** is up, thus providing a positive output which is inverted and applied to the 400 microsecond Single Shot to hold the latter OFF and prevent a positive output of the Single Shot on the line **245.04.** Immediately upon the fall of the Record Gate line, the 400 microsecond Single Shot turns ON and provides an output of 400 microseconds duration. This pulse is provided on the line **245.04** to the Blank Generator of FIG. **259** where the Read Call line **255.02** is up and the feedback line is up due to the negative output of the 10 microsecond Single Shot which is inverted and fed back to the input. Accordingly, when the Disconnect Delay line **245.04** comes up, the Blank Generator Circuits know that a Read operation is complete and that a Disconnect is being prepared. A 15 microsecond Single Shot is turned ON for 15 microseconds and when it goes OFF it turns on the 10 microsecond Single Shot. The output of 10 microsecond Single Shot is inverted and fed back to the input to cut off the input of 10 microseconds. If the Tape Word Incomplete line **226.03** is up, outputs are provided on the Blank Shift Left Six line **259.01** and the Step Group Counter line **259.02.** The Blank Shift Six line **259.01** goes to the Shift Register Controls, FIG. **260***b*, where outputs on the lines **260***b*.**03**, **260***b*.**04** and **260***b*.**05** are provided. The Step Group Counter line **259.02** is sent to the Tape Group Counter, FIG. **226,** where it is effective to step the Shift Counter by **1.** The Blank Generator Trigger is turned ON and a positive output is combined with the Tape Word Complete line **226.02** and the 10 microsecond Single Shot output to provide an output Blank Read Tape Demand on the line **259.03** and to turn OFF the Blank Generator Trigger if this shift has caused the Tape Word to be complete. The Blank Read Tape Demand line **259.03** goes to the Shift Register Controls **1,** FIG. **260***a*, which provides an output on the Tape Demand line **260***a*.**04** to the Channel AControl Word Gate and EOR Synchronizing Controls of FIG. **196***a* for the purpose of telling the Data Synchronizer to prepare to receive a completed word from the Tape Shift Register. Should this shift be insufficient to complete a tape word, the Tape Word Complete line **226.03** remains down and when the output of the 10 microsecond Single Shot falls a positive input is fed back so that the Blank Shift line **259.10** and Step Group Counter line **259.02** are brought up again if the Tape Word Incomplete line **226.03** is up. Whenever the Tape Group Counter, FIG. **226,** has counted to five the Tape Word is complete and transmission of the word on the Tape Shift Register takes place 36 bits in parallel to a DSC Data Register which it has been conditioned to receive.

WRITE TAPE OPERATION

During an Instruction cycle, a 36 bit control word Write Select is brought from Core Storage into the CPU where it is decoded and found to be an Input-Output instruction involving a Data Synchronizer Channel. The status of the Drum is tested to insure that this is not in operation, and if it is in operation, this DSC instruction is delayed until the Drum operation is complete. Assuming that the Drum is not in operation, the Data Synchronizer channel is selected and the signal Write Tape along with the specified unit is transmitted to the Data Synchronizer channel where a test is made to determine whether or not the Data Synchronizer channel is in use. If the channel is in use, the Calculator is normally (but not always) delayed attempting to enter the Instruction into the Data Synchronizer channel until that channel is free. Assuming that the channel is free, the Write Select is entered into one part of the Operational Register, the Unit is entered into another part, and the Tape Class, BCD or Binary, is entered into still another part of the register although in some cases the function and the class are combined such as Write Tape. In this particular case, they are combined and Write Tape is stored in a single trigger, FIG. **173***a*, the unit is stored in another trigger, FIG. **179***a*, and the mode, Binary or BCD, is stored in still another trigger, FIG. **174.** This information then, having been stored in the DSC Operation Register causes a signal to be generated by the DSC which is returned to the CPU to signal End Operation and proceed to the next Instruction in sequential order. In the meantime, the Data Synchronizer Channel having stored such operational information as Write Tape and Unit immediately selects a Tape Control Unit attached to that channel to determine whether or not it is busy. It is busy, the Data Synchronizer Channel waits until it is not busy. Assuming that the Tape Control Unit is not busy, the

Operation information is transmitted to the Tape Control Unit which accepts the information Write Tape, FIG. **255**, the Unit, FIG. **254**, and the Mode, FIG. **255**. The TCU generates and sends a signal, FIG. **253**, back to the DSC indicating that it has received this information and which would normally cause the Operational Registers to be reset, but since the instruction involves the transmission of information, the Operation Register in the DSC containing the Write Tape information is not reset. The Tape Control Unit now tests the Tape Drive Unit specified, FIG. **272***a*. If this Tape Unit is rewinding, it is not available in which case the Tape Control Unit waits until the rewind has been completely executed and Tape Drive has reached the Load Point at which time the Tape Control Unit selects that Tape Drive, FIG. **265**, sets it into writing status, FIG. **266**, and puts it in motion in the forward direction, FIG. **262**. The Tape Drive Unit is in motion at a predetermined time and subsequently is up to speed at a specified time requiring information in order to properly preserve the format of the material to be written on the tape. Therefore, it is essential that subsequent to a Write Select Instruction the CPU provide another instruction Reset and Load Channel (RLC) within a certain period of time. The CPU may have executed a number of other Instructions prior to Reset and Load Instruction as long as the specified time between the Write Select and the Reset and Load Channel is not exceeded. Assuming the RLC Instruction is provided in the stored program and that the time has not been exceeded, a Reset and Load Channel enters the CPU and is decoded whereupon it is determined that this is a Reset and Load Channel and that it refers to a particular Data Synchronizer Channel. The following operations then take place: The Reset and Load Channel Instruction causes the generation of a signal to test whether or not a previous Select Instruction has been stored in the Operational Registers of the Data Synchronizer Channel. If such information has not been stored in the Operational Registers of the channel or if it has been stored and the time has been exceeded causing information to have been lost through a disconnect, then the Reset and Load Channel is treated as a no-operation as the result of the following sequence: The Data Registers and the Operational Registers in the Data Synchronizer Channels are not disturbed, the Reset and Load Channel Instruction permits End Operation in the CPU, the latter proceeding to the next instruction, and an Input-Output Check Indicator is turned ON indicating that a programming error has occurred, Assuming that the Operations Registers do contain data transmitting information concerning Write Tape, the Reset and Load Channel Instruction causes the DSC to generate a signal directing the CPU to go to E time, which is to say that the CPU is required to make a reference to core Storage at the location specified by the Address portion of the Reset and Load Channel Instruction to bring out a DSC Command. The Address Register, FIG. *2mm*, the Word Counter, FIG. *2oo*, the Location Register, FIG. *2qq*, and the Operation Register, FIG. *2eee*, in the DSC are connected through the Storage Bus Switching, FIG. *2vv*, and the Address Switching, FIG. *2ww*, to the Care Storage Address Register, FIG. **129**, and the Sense Amplifier Buffer and I/O Switching, FIG. **211**, in the Core Storage Unit. The CPU proceeds to E time but instead of bringing the data from Core Storage into the CPU, the data are transmitted to the Data Synchronizer channel in the following manner: The Address specified by the Reset and Load Channel Instruction is placed in the Core Storage Address Register, FIG. **129**, and on the Address Busses **170,01.03** through **170.01.17** from Core Storage. Since the Data Synchronizer Channel Address Switching, FIG. *2ww*, connects these busses to the Location Register, FIG. *2qq*, information which came from the Address part of the Reset and Load Channel Instruction is entered into both the Storage Address Register (FIG. **129**) in Core Storage and also entered in the Location Register, FIG. *2qq* (FIG. **166**), in the Data Synchronizer Channel. In response to the Storage Address Register, FIG. **129**, the contents (DSC Control Word) at the address specified by the Reset and Load Channel Instruction are brought into the Storage Buffer, FIG. **211**, and from the latter into the DSC as follows: The contents of positions S, 1, 2, and 19 are entered into the Operation Register, FIG. *2eee*, in the DSC by means of the controls of FIG. **215**, the contents of positions 3 through 17 of the Control Word is passed by means of the controls of FIG. **216** through the Storage Bus Switching in the DSC and entered into the Word Counter, FIG. *2oo*, which is immediately stepped down one, FIG. **217**, and the contents of positions 21 through 35 of the word is entered into the Address Register, FIG. *2mm*, of the Data Synchronizer Channel by means of the Controls of FIG. **215**. The Location Register is stepped up one, FIG. **217**. Upon completion, the Reset and Load Channel Instruction causes End Operation automatically through means of signals generated in the Central Processing Unit, and the CPU proceeds to the next instruction in sequence. Within the DSC the following status prevails: The Address specified by the Reset and Load Channel Instruction plus one is now stored in the location Register in DSC which is the Address where the DSC Command came from in Core Storage plus one; the Address Register in the Data Synchronizer Channel contains the contents of positions 21 through 35 of the DSC Command referred to in Core Storage; the Word Counter contains the contents of positions 3 through 17 of the DSC Command transmitted from Core Storage minus one; and the Operation Register contains positions S, 1, 2 and 19 of the DSC Command. As soon as these Registers have been loaded with the DSC Command this fact is utilized to determine that sufficient information has been received for the next step in the operation as follows: Since a Write Select operation has been specified, it is essential that the first word of data be immediately taken from Core Storage in preparation for a demand from the Tape Drive Unit (TDU) that it is up to speed and ready to Write. Therefore, as soon as the Operational Registers and the Transmission Registers are loaded, a Data Buffer cycle demand is generated by the Data Synchronizer Channel and a signal is provided to indicate that information is to flow from Core Storage to the Data Synchronizer Channel Data Register. The sequence of operation then is as follows: The Address in Core Storage, FIG. *2ii*, where the information is to come from is specified by the Address Register, FIG. *2mm*, in the Data Synchronizer Channel and the contents of the Address Register are transmitted via Address Switching, FIG. *2ww*, in the Data Synchronizer Channel to Core Storage Address Registers, FIG. **129**, thereby causing selection of the word in Core Storage which is to be written on tape. The Word in Core Stor-

age is put on the Storage Busses, FIG. 2*ll*, which are connected through the Storage Bus Switches, FIG. 2*vv*, in the Data Synchronizer Channel to the Input of the Data Register, FIG. 2*ss*. Information then flows from Core Storage into the Data Register in parallel where it is buffered for an indeterminate period of time awaiting a signal from the TCU to load the Tape Shift Register, FIG. 2*xx*. The DSC tells the TCU that the Data Register is loaded. FIG. **260***a*. When the Tape Drive Unit is up to speed, it provides signals via FIG. **260***a* which causes the Data Register information to be sent to the TCU where it is loaded into the Tape Shift Register, FIGS. 2*xx* to 2*aaa*, 36 bits in parallel, and then broken down into six bit groups and transmitted to the Tape Drive Unit and written on tape.

Approximately every 400 microseconds, the tape has completed the Writing of a full word, and when each word has been transmitted from the Shifting Register, FIGS. 2*xx*–2*aaa*, a signal is generated in the Data Synchronizer Channel indicating that such transmission has taken place and further that now it is the time to refill the Data Register with the next word from Core Storage if multiple words are to be written. Therefore, a signal is generated requiring a Buffer Data Word (BDW) cycle to bring the word to be written from Storage into the Data Register. The generation of a Buffer Cycle demand signal normally depends upon the status of the Word Counter since every time a word is transmitted from Core Storage to the Data Register the Word Counter is stepped down one. Thus, if the Word Counter has not yet reached "zero" and the Operation Register specifies a continuing type of transmission flow indicating that N words are to be written, a signal is sent to Core Storage requiring the transmission of another word as specified by the Address Register. If a data word is to be transmitted, a Buffer Data Word (BDW) B Cycle is required. If a control word is to be transmitted, a Buffer Control Word (BCW) B Cycle is required. If the Word Counter has reached "zero," the contents of the Operation Register, FIG. 2*eee*, in the Data Synchronizer Channel are inspected to determine which of several alternatives take place. Two examples are as follows: (1) When the Word Counter has reached "zero," the Operation Register may specify that a new Control Word is to be taken autonomously by the Data Synchronizer Channel from Core Storage at an Address in Core Storage specified by the contents of the Location Register. (2) Depending upon the contents of the Operation Register a signal may be sent to the CPU for the purpose of determining whether or not a Load Channel Instruction is waiting. The Load Channel Instruction in this instance performs the same purpose as the Reset and Load Channel Instruction did at the initiation of the operation. Operation continues until either the Word Counter reaches "zero," the Operation Register indicates that this is termination of writing, or a new command enters the Data Synchronizer Channel Transmission Register indicating that the operation is complete. The sequence chart of FIG. **274** illustrates Tape Writing Operation where the DSC refers to Storage for Control Words after initialization. Upon completion of a disconnect procedure, which involves the reading of the record by the second head on the Tape Drive Unit and completely parity-checking the record, the Tape Control Unit ultimately reaches a disconnect whereupon it sends a signal to the Data Synchronizer Channel indicating that it is disconnected and permitting the Data Transmitting Registers to be reset. If a non-transmitting instruction has previously been placed in the Operational Registers or stacked on top of the Data Transmitting instruction, this instruction is now automatically executed and entered in the TCU.

The details of the Write Tape Operation, described generally above, follow:

The instruction Write Select (WRS + 0766) is given which translated by the Central Processing Unit, as described below, prepares the system to write information from Core Storage on tape at the Tape Drive Unit specified by the Address in the Control Word. The transfer of information is, of course, through the specified Data Synchronizer Channel. This Write Select instruction is a Type B instruction which contains the octal operation number 766 in binary form in positions 3 through 11 as set forth in the table below, the octal address **1221** in positions 24 through 35 (See FIG. **207**) which signifies DSC A, Tape Unit 1 and operation in the binary mode and the Sign bit in position S. This 36 bit instruction, Write Select, is brought from Core Storage, FIGS. 2*ii* and 2*ll*, and loaded into the Storage Register, FIGS. 2*b*–2*d*. At **19** time positions 18 through 35 of the Storage Register are transferred to the Adder positions P, 1 through 17 by way of the line **998***a*.**08**, and at **110** (D1) positions S, 3 through 11 of the Storage Register comprising the operation part loaded into the Instruction Register positions S through 9 by way of the Storage Register to Instruction Register Controls, FIG. **99**. The operation is decoded from **110.5** until **18** in the Primary Operation Decoder, FIG. **14**, and the Secondary Operation Decoder, FIG. **15**.

It will be remembered that in positions **3** through **8** of this Write Select instruction, the octal number 7 in binary form is in positions 3 through 5, and the octal number 6 in positions 6 through 8. Accordingly, there are "ones" in positions 3 through 7. Accordingly, all of the triggers in the Instruction Register of FIG. **13***a* are ON providing positive outputs on the lines **13***a*.**08**, **13***a*.**16**, **13***a*.**21**, **13***a*.**24** and **13***a*.**27** to the Primary Operation Decoder, FIG. **14***b*. Since the foregoing lines are up, it is apparent from FIG. **14***b*, that an output is provided on the line **14***b*.**07** indicative of the Primary Operation part of the Control Wrod, namely (7,6). This 7,6 output line **14***b*.**07** goes to the Primary Operation Decoder, FIG. **14***b*, where four outputs are provided on the lines **14***d*.**61**, **14***d*.**62**, **14***d*.**63** and **14***d*.**64**. One of these lines **14***d*.**63** goes to the Secondary Operation Decoder, FIG. **15***a*, where it is used to obtain the Secondary Operation portion of the Instruction, namely 6.

Returning once again to the Instruction Register, FIG. **13***c*, as is seen from the table above, there was a 1 in Storage Register position 10 and accordingly the Instruction Register **8** trigger is set for providing an output on the line **13***c*.**25** to the Secondary Operation Decoder, FIG. **15***a*. There was a 0 position 11 of the Storage Register and accordingly the Instruction Register **9** trigger is OFF and an output Minus On Instruction Register **9** is provided on the line **13***c*.**41** to the Secondary Operation Decoder, FIG. **15***a*.

Referring now to positions 6 through 7 of the Instruction Register, FIG. **13***b*, Storage Register position 9 contains a 1 and so the Instruction Register **7** trigger provides an output on the line **13***b*.**42** to Secondary Operation Decoder. Since position **8** of the Storage

Register contains a 0, the Instruction Register **6** trigger contains a 0 and an output Minus on Instruction Register **6** is provided on line **13***b*.**04** to the Secondary Operation Decoder, FIG. **15***a*. As shown in FIG. **15***a*, these lines provide an output on the (0,6) lines **15***a*.**04** and **15***a*.**15**. The Instruction Registers Sign Plus and Minus, FIG. **100**, has a trigger which is set to 0 indicative of a positive sign in the operations code position S of the Storage Register.

In FIG. **171** the Secondary Operation Write line **173.01** is up, lines Minus on Channel A Data Selector **195.03** and Minus on Channel A Non-Data Selector **176.05** are both up since when a Write Select is given as in this instance, the DSC is neither in a data nor a non-data condition, Channel A Address line **182.02** from Command Decoding, FIG. **182***a*, is up, and when E/R line **222***e*.**13** comes up an output on line **171.02** is provided to Channel A Data Class Selection, FIG. **173***a*, a line **171.03** is provided to Channel A −12 Volts Clamp Register Reset, FIG. **219***a*, and the Gate Sync Trigger line **171.06** is brought up to Channels A and B End Operation Synchronizer, FIG. **172**, to set the Sync Trigger. It is pointed out with reference to FIG. **171** that the output lines just mentioned go down immediately upon the selection of the DSC since the instruction will either be data or non-data and one or the other of the lines **175.03** and **176.05** will be down.

The line **15***a*.**04** from the Secondary Operation Decoder is provided to FIG. **15***b* where the lines **15***b*.**09**, **15***b*.**10** and **15***b*.**11** are up indicative of Secondary Operation (0,6) Write. The line **15***a*.**05** in the Secondary Operation is sent to the DSU Channel A Data Class Selection, FIG. **173***b*, which brings up the Secondary Operation Read line **173***b*.**01** and also conditions circuits associated with the Class Selection triggers. The output line **15***b*.**11** is used in the selection of the Drum and the line **15***b*.**10** goes to the Class Decoder, FIG. **149**, where it is used with Minus on Instruction Register **11** line **13***d*.**05**, Minus on Instruction Register **12** line **13***d*.**09** and Instruction Register **10** line **13***d*.**04** to provide a Gate Pulse to bring up the Tape Class Address (2, 0, or 2,2) line **149.17** to the Channel A Data Class Selection controls, FIG. **173***b*, in the DSU where, in turn, the line Tape Class Address line **173***b*.**03** is brought up and the Tape Read and BCD Triggers Controls are conditioned. As shown in FIG. **2***d* in positions 24 through 26 of the Storage Register, lines **5***f*.**03.24** through **5***f*.**03.26** are providing indications of binary "ones" and lines **5***f*.**01.24** through **5***f*.**01.26** are for providing indications of binary "zeros" and these lines are connected to the Channel Selector of FIG. **153** where the Select Channel A line **153.01** is brought up since the Primary Operation (7,6) line is up, the Minus on Storage Register **24** line is up, Minus on Storage Register **25** line is up and Storage Register **26** line is up. The Select Channel A line **153.01** leads to the DSU Command Decoding, FIG. **182***a*. Positions 10 through 17 of the Adder are gated through the Address Register by way of the Adder to Address Switch line **110.04** from I9 to CT1 and outputs are provided from the Address Register on the lines **16***b*.**25.10**, **16***b*.**29.11**, **16***a*.**03.12**, **16***a*.**07,13**, **16***a*.**11.14**, **16***a*.**15.15**, **16***a*.**19.16** and **16***a*.**23.17** to the Shift Counter of the Instruction Register, orders **10** through **17**. Shift Counter **102.04** comes up, FIG. **13***d*, as the result of the I9 until CT1, AO (D1) and Primary Operation (7,6), FIG. **102**. The following lines are up in FIG. **13***d*: line **13***d*.**04**, line **13***d*.**17** and line **13***d*.**34**. The following lines are down: line **13***d*.**05**, line **13***d*.**09**, line **13** *d*.**19**, line **13***d*.**23** and line **13***d*.**27**. These lines provide inputs to the Class Decoder, FIG. **149**, and the Unit Select Matrix, FIG. **150**. In the Unit Select Matrix, FIG. **150**, the Minus on Instruction Register **14** line **13***d*.**19**, Minus on Instruction Register **15** line **13***d*.**23**, Minus on Instruction Register **16** line **13***d*.**27**, and Instruction Register **17** line **13***d*.**34** are up providing an output on the line **150.42** to Channel A Unit Selection **1** through **5**, FIG. **179***a*, where the Unit Select **1** (A) trigger is set by means of the line **150.42**, the line **182***b*.**22** and the line **172.01**.

Referring now to Channels A and B End Operation Synchronizer FIG. **172**, the Gate Sync Trigger line **171.06** is brought up due to the Channels A and B Class Selection Interlock, FIG. **171**, where the Cascaded AND Circuit (A_c) provides the output due to Secondary Operation Write line **173.01**, E/R time **222***e*.**13**, Minus on Channel A Data Class Selected **175.03**, Minus on Channel A Data Class Selected **176.05**, and Channel A Address **182***a*.**02**. In FIG. **14***b*, Primary Operation Decoder, the Primary Operation (7,6) Sense line is up as previously described and an output **14***b*.**61** is sent to the Read/Write Execution Timer for Drum Operations. Another line **14***b*.**62** goes to B Time Control where it is used to set the Go to B Time Trigger if a B Cycle Demand line **199.03** is up. The line **146***b*.**64** is sent to FIG. **102**, Shift Counter Pulse Generator **2**, where it is combined with I9 till CT 1 line **122***j*.**67** and **A0** (D1) line from the Pulse and Gate Generator, FIG. **122***a*, to bring down the Minus on Address Switch 10 through 17 to Shift Counter line **102.04**.

In FIG. **222***b*, the Pulse Generator of Central Processing Unit provides an **A10** (D1) pulse to set the trigger which brings up the line **222***b*.**20**. At A11 (D1) an input pulse is provided on the line **222***e*.**07** which turns OFF the trigger and completes the pulse duration on the line **222***b*.**20** which is sent to the Channels A and B End Operation Synchronizer, FIG. **172**. The Sync Trigger, FIG. **172**, has been set ON by a previous A7 (D1) pulse on the line **222***d*.**10** and the Gate Sync Trigger line **171.06**. Accordingly, the **A10** (D2) pulse of the line **222***b*.**20** is combined with the Sync Trigger output to bring up the line Set I/O Class and Unit (Channel A) line **172.01** which is sent to Channel A Unit Selection **1** through **5**, FIG. **179***a*, and there combined with Unit Address **1** line **150.42** and Channel A Address Gated line **182***b*.**22** to set the Unit Select **1** (A Trigger) as described previously in part.

It is pointed out here that in Command Decoding, FIG. **182***a*, switches are provided which connect those inputs which correspond to the DSU Channel in which the selected unit is employed. For example, using three DSU's, the first DSU has the switch set as shown in FIG. **182***a* for providing Select Channel A to the Grounded Grid Amplifier. A second DSU has the switch set so as to connect Select Channel B to the Grounded Grid Amplifier whereas a third DSU would have the switch set for connecting the line Select Channel E to the Grounded Grid Amplifier. All DSU's are identical and certain switches throughout the system are set for providing the distinct Addresses for the DSU's. In this instance Select Channel A is used and outputs are provided on the lines **182***a*.**01** through **182***a*.**08** with an additional output provided on the line **182***a*.**20**.

With reference to the DSU's Instruction Decoder, FIG. **160**, the Sense (7,6) line is up, the Instruction Register's sign is plus and there is a 1 bit in Storage Register position **26** but the Unit Address is (0,6) instead of (0,0). Since the Unit Address line (0,0) is down the Beginning of Tape Test line is down. It is pointed out that for the Instruction Beginning of Tape Test (BTT + 0760) and End of Tape Test (ETT − 0760) outputs are provided as indicated in this FIG. **160**.

The Tape Write Select Trigger, FIG. **173***a*, is set by way of the Secondary Operation Write line **15***a*.**05**, the Channel A Address line **182.03**, the Set Class and Unit Channel A line **172.01**, and the Tape Class Address line **173***d*.**03**. To set the I/O Class and Unit Channel A Trigger the line **172.02** is sent to Channel A Unit Selection 1 through **10**, FIG. **179***a*, to turn ON the Unit Select **1** A Trigger by way of the lines **150.42**, the Unit Address **1** Channel A Address Gated line **182***b*.**22**, and the line **172.01** just mentioned. Line **182***b*.**22** is provided from Command Decoding, FIG. **182***b*, by way of Channel A Address line **182***a*.**20**. The line **172.01** is also sent to Channel Non-Data Selection, FIG. **176**, where there is an input Channel A Address **182***a*.**04** but since the instruction is a data instruction others of the lines here are ineffective at this time to produce a change in these triggers.

Up to this point Channel A has been selected, the Unit Address has been provided to the DSU and since this is a data type instruction none of the triggers in FIG. **176** are ON. Consequently, the Minus on Channel A Non-Data Selected lines **176.05** and **176.06** are up. In FIG. **175** Class Selection Interlock when the line **176.06** is up and line **175.03** is down due to the Tape Write Select line **173.09**, the line **175.05** is sent to Channel Control, FIG. **162**, where it provides a powered output Channel A in Use on the lines **162.01** and **162.02** to the DSU Conditional Transfer Circuits of FIGS. **161***a* and *b*.

The Binary Coded Decimal Address of Tape Unit **1** in DSU Channel A is **1201** whereas the Binary Address in octal for the same Tape Unit 1 in DSC A is **1221** which is the Address used in this example. Accordingly, if operation is in the Binary System there is a 1 in position 31 of the control word, while if the operation word is in the Binary Coded Decimal system there would be a 1 in position 32 for the control word. In the illustration chosen the Address **1221** signifies DSC A, Tape Unit **1**, operating in the Binary mode, and therefore, there is a "one" in position 31 of the control word which results in a "one" in position 13 of the Adder and also a "one" in the Instruction Register trigger **13**. The line **13***d*.**13** to Tape Control, FIG. **159**, is down and the output BCD line **159.01** to Channel A Data Class Selection, FIG. **173***b*, is down which indicates that operation is in the Binary mode.

With reference to Channel A Data Class Selection, FIG. **173***a*, the line **173***a*.**06** is provided to Channel A Set BCW Control Word Required, FIG. **197***a*, but line **197***a*.**02** cannot be brought up since Channel A Indicator 1 line **165.05** is down because Indicator 1 trigger is OFF. It would be otherwise with a DSC Control Word having an octal 1 in positions S, 1 and 2. Line **173***a*.**06** also goes to Data Register A Loaded and Set Channel A, BDW Cycle Required, FIG. **195***a*. However, an output from this circuit is not available at this time since the Data Register is not loaded. The line **173.07** is provided to Channel A Control Word Gate and End of Record Synchronizer circuits of FIG. **196***a*, where the Channel A Data Register Not Loaded line **195.02** is up since the Data Register is not loaded and the Channel A Word Count **0** line **163.08** is up, but Sync Gate Channel A trigger is not ON at this time.

The DSU has received the instruction Write Select and stores the Write Select in the trigger of FIG. **173***a* and stores the Tape Unit specified by turning ON the trigger of FIG. **254***a* or *b*. The DSU interrogates the TCU on the line **173***a*.**13** and turns ON the Select TCU Schmidt trigger in FIG. **258***b*. If the TCU is not busy as determined by the lines TCU Interlock OFF **255.16** and Select Ready and Write **241.02** in TCU Interlock, FIG. **253**, the pulse enters the Data Class Selection, FIG. **255** and turns On the Write Call Trigger via the lines **253.02** and Write/Cycle/Test **258***b*.**02** and the Tape Unit Selector Trigger, in FIG. **254***a* via the lines **180***a*.**01** and **253.03**. This line **255.26**, in cooperation with line **266.05**, tells whether the TCU is busy or free. A Select TCU signal is generated on the line **258***b*.**07** to the TCU interlock, FIG. **253***b*. With reference to Data Class Selection, FIG. **255**, the line **255.16** is down when either the Read Call or the Write Call lines are up due to the setting of their respective triggers or when the Non-Data Interlock is down. When the Write Call trigger is set by the Write/Cycle/Test line **258.02**, the TCU Interlock line **255.16** is down to the TCU Interlock. But before Class Selection is made in either FIGS. **255** or **256**, the TCU Interlock line **255.16** is up, the Select Ready and Write line **241.02** is down, the Select TCU line **258***b*.**07** is up and the negative shift produced thereby sets the TCU delay **25** microsecond Single Shot. With reference to FIG. **254**, the trigger corresponding to the Tape Unit which is selected is turned ON by way of the line **179***a*.**03** from Channel A Unit Selection **1**, FIG. **179***a*, to the Tape Unit Selector 1 through **5**, FIG. **254***a*.

Summarizing the TCU operation thus far, a Write Select from the DSU to the TCU on the line **173***a*.**13** causes a select TCU and a Write Cycle Test operation. In FIG. **258***b* the Select TCU line **258***b*.**07** sets the TCU Delay and gives outputs on Set TCU Class and Unit and TCU Selected, the latter serving to notify the DSU and the former serving to set the TCU Class and Unit. Tape Unit **1** is selected in FIG. **254***a* which selects a Tape Drive Unit. In FIG. **255**, Data Class Selection, the Set TCU Class and Unit line **253.02** and the Write/Cycle/Test **258***b*.**02** set the Write Call trigger. As soon as the Write Call trigger is turned ON the TCU Interlock Off line **255.16** drops and turns OFF the TCU Interlock Circuits of FIG. **253**.

In Set Read/Write Status Controls, FIG. **241**, the Write Call line **255.09** is up which provides an output Set Write status on the line **241.08** which goes to Read/Write Status, FIG. **266**, in the Tape Drive Unit. In FIG. **266**, the Set Write Status line **241.08** is combined with the Select and Ready line **265.03** and Not File protection which is up to turn ON the Read/Write Status trigger which, in turn, brings up the Write Status (Tape Indicator) line **266.04** and the Select Ready and Write line **266.05** which goes to Set Read and Write Status, FIG. **241**, to initiate Write Delay and pass outputs on the lines **241.03** and **.04**, Write Forward Before Backspace Rewind. In FIG. **266**, the output Gated Write Pulse **266.06** is up to condition the Write Amplifiers, FIG. **263**. With reference to Data Class Selection,

FIG. 255, the line 255.10 is up which goes to Shift Register Controls, FIG. 260*a*, where it is combined in the first instance with Clock Gate Delay and in the second instance with Tape Word Complete and Sample Pulse.

In FIG. 241 the Start Read/Write/ Write End of File line 252.01 is brought up in the following manner: In FIG. 252 the Set TCU Class and Unit line 253.02 and the Write Test Cycle line 258*d*.02 are up to turn ON the Class and Unit Disconnect Gate trigger. The left hand plate of this trigger is up, the line Not TCU Disconnect 250.01 is up thus providing a Start Read / Write / Write End of File signal on the line 252.01. The Class and Unit Disconnect Gate Trigger stays on until the Write / Test / Cycle line 258*b*.02 falls. Now continue with Initiate Write Delay of FIG. 241.

Start Write is initiated with the Write Delay provided on the lines 241.05 to Read and Write Delay, FIG. 248. The Write Delay is introduced for the purpose of leaving the Load Point before beginning to Write on Tape. Assuming that the Tape Drive Unit is not at Load Point then the line 242.02 is up and the Write Load Point Delay Single Shot is turned OFF for 40 milliseconds. The Initiate Write Delay line 241.05 causes the Set Write Delay 50 microsecond Single Shot to turn OFF for 50 microseconds. Since both the Write Load Point Delay Single Shot and the Set Write Delay Single Shot must be ON to set the 8 millisecond Write Delay Single Shot the Write Delay Single Shot is not turned ON until 40 milliseconds after the Write Load Point Delay Single Shot is turned OFF. The 8 millisecond Write Delay Single Shot is turned ON and when it turns OFF the negative shift sets the Clock Gate Delay Single Shot to provide outputs on the lines 248.08 through 248.12 which are up for 20 microseconds. At the fall of the Clock Gate Delay Single Shot the Delay Read/Write Call is turned ON and it remains ON unitl the Disconnect Delay. The Write Clock Gate lines 248.04 to 248.07 remain up as long as the Delayed Read/Write Call trigger is set and the Write Clock Control line 194*a*.01 is up.

Assuming that the machine is not at Load Point then Initiate Write Delay line 241.05 is effective to turn OFF the Set Write Delay 50 microsecond Single Shot which prevents the setting of the Write Delay 8 millisecond Single Shot. At the end of 50 microseconds the Write Delay 8 millisecond Single Shot is turned OFF and operations proceed according to the previous description.

In FIG. 248, Read and Write Delay Circuits, the line 248.10 is up for 20 microseconds and during this time it is used in the Shift Registers Controls 1, FIG. 260*a*, in cooperation with the Not Backward line 239.11 to perform a first word test by bringing up the 260*a*.01 line. The output is provided on 260*a*.01 to the DSU Channel A Read Gate and Write Clock Control, FIG. 194*a*, where it is combined with the Channel A Tape Write line 173*a*.09 and Channel A Data Register loaded line 195*a*.03 to set the trigger for bringing up Channel A Write Clock control line 194*a*.01.

A First Word Test is performed during the Clock Gate Delay of 20 microseconds. Therefore, all the conditions must be met for turning ON the Write Clock Control Trigger, FIG. 194*a*, during this period. It is here that a determination is made of whether or not the Data Register has been loaded. If a Reset and Load Channel instruction has not been given to provide a DSC Control Word which, in turn, loads the Data Register A at this time, then a disconnect results. Assume for the moment that a Reset and Load Channel instruction has been given which refers the DSC to a location in Core Storage from which the DSC Control Word is taken and that the first word to be written on tape has been loaded into the Data Register. Then, the Channel A Write Clock Control line 194*a*.01 is up and the Write Clock Gate is supplied as previously explained and the Write Clock Gate line 248.04 actuates the Clock Write Pulse and Line Register Reset Controls of FIG. 249 in the manner described earlier.

A Reset and Load Channel instruction has an operation code (RLA + 0540) octal and the instruction is of type B as shown in FIG. 3b which has an address portion and operation portion. The operation portion refers to Reset and Load Channel whereas the address portion refers to the initial address in Core Storage at which the DSC control word is to be taken. Channel A has been selected and is awaiting the Reset and Load Channel instruction which is brought from Core Storage and placed in the Storage Register (FIGS. 2*b*–2*d*) positions 3 through 11 which in turn are loaded into positions 1 through 9 of the Instruction Register in the manner previously described. In FIG. 13*a*, the lines 13*a*. 08, 13*a*. 11, 13*a*.21, 13*a*.24 and 13*a*.25 are up since there are "ones" in SR 3, 4, 5, 6 and 17. The Indirect Address Control Trigger OFF line 98.14 is up and the instruction lines just mentioned provide output signals on the (5,4) lines 14*a*.01, 14*a*. 02 which correspond to the tens and hundreds position of the operations code.

The (5,4) line 14*a*.01 goes to Command Decoding, FIG. 182*b*, to indicate Synchronous Load Channel (SLC) or Reset and Load Channel (RLC). The (5,4) line 14*a*.02 goes to Primary Operation Decoder, FIG. 14*d*, to bring up the outputs as shown. The line 14*d*.27 goes to B Time Control, FIG. 121, where it is ANDed with an Instruction Register line 13*b*.49 which is up to provide an output to the OR circuit attached thereto. When the E/R time line and A11 (D1) lines come up (disregarding the share line) the Go to B Time trigger is set provided a B Cycle demand is made on the line 199.03. Since a DSC word must follow the RLA instruction, a B cycle demand follows. The line 121.01 goes to the Cycle Timer Control, FIG. 118. The line 14*d*.28 goes to the Channel Selector, FIG. 153, where Minus on Instruction Register 8 line 13*c*.04 and Minus On Instruction Register 9 line 13*c*.41 combine with Instruction Register Sign Plus line 100.30 to bring up Select Channel A line 153.01 which is directed to the DSU as in the Write Select Instruction. The line 14*d*.29 is connected to the End Operation Control, FIG. 128*a*, where it is ORed into an AND circuit with the lines Indirect Address Control Trigger OFF and E Time to provide an End Operation Control signal on line 128*a*.01. The line 14*d*.30 goes to Enter Execute Controls, FIG. 155, which causes a Go to Execute I/0 line 155.01 to come up when the Proceed to E Control line 202.01 comes up.

With reference to FIG. 14*a*, Primary Operation Decoder, the line 14*a*.01 goes to Command Decoding, FIG. 182*b*, as previously mentioned. The line is combined with Channel A Address line 182*a*.20 to provide an output Channel A Synchronous Load Channel / Reset and Load Channel on the lines 182*b*.01 through 182*b*.04. At this time consider only the line 182*b*.03

which goes to Proceed to E Time Controls, FIG. **202.** With reference to Instruction Register positions 6 through 7, FIG. **13***b*, the Minus on Instruction Register 7 line **13***b*.**37** provides outputs Minus on Instruction Register 7 (RLC Mode) on the lines **182***b*.**17** through **182***b*.**19** in FIG. **128***b*. The line **182***b*.**16** goes to Proceed to E Time in FIG. **202** where it is applied as an input to the Cascaded AND Circuit. At this time Channel A Data Selected line **175.01,** Channel A End of Tape Indicator Off line **184.01,** Channel A End of File Indicator Off line **187.01,** are up so that during an E/R Time are A9 (D1) the Proceed to E Time Trigger is set to provide outputs on the lines **202.01** and **202.02.** The line **202.01** goes to Enter Execute Controls, FIG. **155,** where it combines with Primary Operation **54** line **14***d*.**30** to bring up the Go to Execute I/O line **155.01** which goes to Cycle Timer Controls, FIG. **118.** The Cycle Timer Control, FIG. **118,** has two outputs in response to the Go to Execute signal, namely **118.01** and **118.02.** The Go to E line **118.01** goes to Cycle Timer Output controls, FIG. **120,** where the Set Cycle Timer AO(D1) pulse turns ON the E Time Trigger. With the Cycle Timer Control Trigger OFF an output is provided on E Time line **120.02.** However, the Turn On, Carry Timer, Control Trigger line combines with the Set Cycle Timer AO (D1) line and the negative shift produced thereby turns ON the Cycle Timer Control Trigger to bring up the lines **120.07** and **120.08.** With reference once again to the Cycle Timer Controls, FIG. **118,** the line **118.02** goes to Cycle Timer Gate Generator, FIG. **119,** where at MAO (Di-) the Set Cycle Timer signal is provided on the line **119.02** in response to the MAO (D1) line, While either the Go to E Time Control line or the MAO (D1) line is up the output of the AND circuit connected thereto is negative so the Reset Cycle Timer line **119.01** is up. However, the combination of Go to E Time Control MAO(D1) provides a positive output at the AND circuit and a negative output on the Reset Cycle Timer line. This provides for an Execute Cycle during which time a reference will be made to Core Storage at the address specified in the Reset and Load Channel Instruction to bring in a DSC Control Word.

The line **14***d*.**31** is connected to the Interlock Test Skip Control, FIG. **154,** where it enters an AND circuit as an input with DSU End Operation Control line **156.02** from End Operation Mixing, FIG. **156,** to produce an End Operation signal on the line **154.02.**

During the execution of the Reset and Load Channel Instruction, the contents of the Reset and Load Channel Instruction positions 21 through 35 are put into the Storage Address Register, FIG. **2***d*, and then transferred to the Address Switches of the Address Register, FIG. **2***i*, to the Storage Address Register, FIG. **2***hh*. In the Storage Address Register, FIG. **129,** the triggers are set according to the bit pattern of positions 24 through 35 of the Instruction in positions 6 through 17 respectively, by way of the Address lines **16***b*.**13, 16***b*.**16, 16***b*.**19, 16***b*.**22, 16***b*.**25, 16***b*.**29, 16***a*.**02, 16***a*.**06, 16***a*.**10, 16***a*.**14, 16***a*.**18** and **16***a*.**22.** As described previously, when referring to the Magnetic Core Storage, the setting of these triggers causes the word to be Read from the specified Location in Core Storage via the Sense Amplifier, Buffer and I/O Switching Register, FIG. **211,** (FIG. **142**), and if the Address 0777 octal is used as in the previous example then the lines **129***a*.**01, 129***a*.**03** and **129***a*.**05** are up signifying "zeros" and the lines **129***a*.**08, 129***a*.**10, 129***a*.**12, 129***b*.**02, 129***b*.**04, 129***b*.**06, 129***b*.**08, 129***b*.**10** and **129***b*.**12** are up signifying binary "ones." Then according to the previous description the word at the Location 0777 is brought up into the Sense Amplifier Buffer and I/O Switching which in this instance is to be a DSC Control Word. It is to be noted also that in the Storage Address Register output lines are provided to the Data Synchronizer Address Busses which are connected to the DSU Address Switching of FIG. **2***ww*. It will be noted that the lines **129***a*.**13** through **129***b*.**18** correspond to the lines **170.01.03** through **107.01.17** of DSU Address Switching, FIG. **170.** In this instance the output of DSU Address Switching is the same as in the input. Since these lines are up according to the Address 0777 then the same outputs are also available on the lines **170.02.03** through **170.04.17** to the DSU Location Register A of FIG. **2***qq*. With specific reference to the Location Register A, FIGS. **166***a* and *b*, the Address is loaded into the Location Register by way of the line Storage Address Register to Location Register A **215.03** and Storage Bus to Control Register, FIG. **215,** and the line **215.03** is brought up in this instance by means of the Channel A SLC/RLC Gate Line **210.03** when the A3(D2) line **222***d*.**01** comes up. In this way the Address is loaded into the Location Register A. However it is pointed out that the Address stored in Location Register A, must be the Address to which reference was made plus one in order that a subsequent reference may be made by the DSC for instruction. This is accomplished by stepping the Location Register A by way of the line **217.01.** With reference to the Channel Register Gate, FIG. **210,** the line **210.02** is provided to Step Control Register, FIG. **217,** and when the latter is up and when the A6 (D1) pulse comes up on the line **222***e*.**02** the output of the AND circuit is inverted to the line **217.01** which is sent as a binary input to the Location Register A Address line 17 trigger where it steps the latter one since the Location Register contains 777 octal which is equivalent to 511 decimal and the binary number 111 111 111. The binary number or the binary one applied to the Trigger 17 causes the number to be changed to 1000000000 which is equivalent to 1000 octal or 0512 decimal.

The next steps are, of course, to condition the DSC for receipt of the DSC control word from Core Storage as specified by the Address portion of the Reset and Load Channel Instruction. During the E Cycle which follows, the Address in the RLA instruction is placed in the Storage Address Register, FIG. **2***hh* (FIG. **129**), and the DSC Control Word is brought out of the Storage into the Sense Amplifier Buffer, FIG. **2***ll*, and distributed from there into the DSU Word Counter A, FIG. **2***oo*, the Address Register A, FIG. **2***mm*, and the Operation Register A, FIG. 2eee.

The Control Word which is brought out of Core Storage and placed in the Selected DSC Channel is a normal DSC Control Word as shown in FIG. **3***f* with a word count in positions 3 through 17 which specifies the number of words to be written and an Address in 21 through 25 which specifies the Initial Address from which the word is to be taken and thereafter written on tape. The bit configuration for the Operation Register A is in positions S, 1, 2, and 19 and may be any of these configurations referred to previously. The word count is placed in the DSU Word Counter A and the address is placed in the DSU Address Register A, FIGS. **2***oo*

and 2*mm* respectively. The DSU Word Counter A, FIG. 2*oo*, retains the word count and as each word is written the total count is reduced by one. For each word written the DSU Address Register steps up one so that sequential words are taken from Core Storage and written on tape. The reference that the DSC makes to Storage for the DSC Control Word is made during a B Cycle without logical interference with the Central Processing Unit. After execution of the RLA Instruction, the CPU may take the next instruction from Core Storage in accordance with the output of the Instruction Counter, FIG. 2*v*, and proceed while the DSC autonomously operates writing words on tape. Reference is made to the DSU Timing on Tape Writing, FIG. **274**, which shows where the first DSU Control Word enters and where the first Data Word enters on the following cycle. It is particularly pointed out that the Buffer is loaded when the first Data Word enters DSC which refers to loading of Data Register A in this instance. It is also pointed out that the first Word Test is only completed after it has been determined that the Buffer is loaded. In FIG. 2*ll*, the Storage Buffer Register contains the DSC Control Word. With reference to FIGS. **157***c* and **157***d*, it is pointed out that the DSU Storage Bus merely passes through the Data Register B without control and the lines **167***b*.**02.21**, **167***b*.**02.22**, **167***b*.**02.23** through **167***b*.**01.27**, **167***b*.**04.28** through **167***b*.**04.35** go to the DSU Address Register A which effectively connects the output of the Storage Buffer Register, FIG. 2*ll*, to the DSU Address Register A, FIG. 2*mm*. When the Storage Bus to Address Register A line **215.01** is brought up, the DSU Address Register A is loaded with the address of the DSC Control Word. With reference to Storage Bus to Control Registers controls of FIG. **215**, an output is provided on the line **215.01** in response to the Channel A SLC/ALC Gate line **210.03** and a line A7 (D2) 22*d*.**09**. With reference once again to the Data Register B Triggers, FIGS. **167***c* and **167***d*, the outputs of positions 3 through 17 of the Sense Amplifier, Buffer, I/O Switching, FIG. 2*ll*, are essentially connected to the inputs of the DSU Word Counter A, FIG. **200**. With reference to Storage Bus **3** through **17** to Word Counters Load Control Trigger, FIG. **216**, the Channel A Trapping Mode or SLC/RLC Gate line **217.03** is up and at A7 (D2) the line **222***d*.**08** comes up to provide a negative output on the line Minus on Storage Register **3** through **17** to Channel A Word Counter line **216.05** which goes to the DSU Word Counter A, FIG. **163***a*. As mentioned previously the Word Counters are nines complement plus one counters and the Word Count is entered in complement form and a one is automatically added. Each time that a word is written from Storage a one is added to the Counter until the three position, which is the highest order, goes to "zero". When the negative shift on the Minus on Word Count A0 line **163***a*.**01** turns ON the Word Count Zero Trigger in FIG. **163**b this brings up the lines **163***b*.**07** through **163***b*.**11**. For the time being assume that the DSU Indicator Triggers in positions S, 1 and 2 are "zero" and the Word count is not "zero" which means that the DSC continues to call for the transmission of words from Storage to the Tape Unit. The cycle during which the DSC Control Word was taken from Memory was a Buffer Control Word Cycle whereas the cycle during which the DSC refers to Storage for a data word to be written on tape is a Buffer Data Word Cycle. The distinction between the two is primarily like the one that is applied to the Central Processing Unit between an Instruction Cycle and an Execute Cycle. The DSC in the one instance treats the word as a command and in the other instance as a data word. Since a reference to Core Storage must be made at the address specified in the DSU Address Register A of FIG. 2*mm*, the contents thereof must be passed through the DSU Address Switching of FIG. 2*ww* to the Storage Address Register, FIG. 2*hh*. This is accomplished by the control line **213.01** Address Register A to Storage Address Register shown in FIGS. 2*ww* (FIG. **170**). A bit configuration of the Address is of course retained within the DSU Register A since the read-out is non-destructive. With reference to Address Register a to Storage Address Register, FIG. **213**, an output is provided on the lines **213.01** and **213.02** at AO (D4) time for each time that a Channel A Data B Cycle is taken. In this instance a Data B Cycle has been called for and the line **205.03** is up and an AO (D4) line **222***c*.**01** comes up to transfer the Address Register A to the Storage Address Register. In FIG. **205** Channel A and B Data B Cycle Triggers, the Channel A Data B Cycle Trigger is turned ON with the Channel A Buffer Data Word Required line **203.02** up, the Channel A Priority **206.03** up and the line **B0** (D2) line **222***b*.**07** up. In this instance Channel A Priority is readily established since it has been assumed that none of the other channels are in operation and Channel A BDW Required line is up as a result of taking the Reset and Load Channel Cycle when it follows that at least one reference to Core Storage must be made. Conditions for a Set Channel A Buffer Data Word Cycle requirement are as follows with reference to FIG. **195***a*: A Channel A Write line **173***a*.**06** is up, the Word Count Not Zero line **163***b*.**04** is up, the Minus on Continuous Storage Read-In/Lead/line **218.03** is up since the inputs are down, namely Plus on Continuous Read-In line **192.14** and Channel A Manual line **191***a*.**07** as shown in FIG. **218**. In FIG. **195**a the Data Register A Loaded Trigger is not set. Accordingly, its left hand plate is up which provides another input to the AND circuit associated with the output line **195.01**. Since all the conditions of the AND circuits have been met, Set Channel A Buffer Data Word Cycle Required line comes up. The line **195.01** goes to Channels A and B Buffer Data Word Required and Data B Cycle Demand. FIG. **203**, where the negative shift turns ON the trigger; and at A9 (D1) time, the line 222*d*.**14** turns on the trigger associated with the Channel A Buffer Data Word Required line **203.01**. This output **203.01** is fed back in cooperation with Channel A Priority line **206.03** and B Time line **222***b*.**10**, to turn off the Channel A BDW Trigger at D2 (D1) time when the line **222***b*.**12** is up. The line **203.01** goes to Channel A and B BCW Required and B Cycle Demand, FIG. **199**, where it causes output to be produced on the line **199.03** and **199.05**. The DSC B Cycle Demand line **199.03** goes to B Time Control, FIG. **121**, where it is effective to turn ON the Go to B Time Trigger in cooperation with Carry Timer Control Trigger ON line **120.07** to Go to B Time Line **121.01** to direct the Central Processing Unit to take a B Cycle as pointed out previously. In FIG. **199**, the Channel A B Cycle Required Priority line **199.05** goes to Channel and DSU Priority Required Controls, FIG. **204**, where it turns ON the Channel A Priority Trigger in response to a **B0** (D2) pulse on the line **222***b*.**06**, the Channel B Cycle Required line **199.02** being down. If the lines

199.05 and 199.02 are both up, the Channel A Priority Trigger cannot be turned ON in the manner previously described and both the lines 199.05 and 199.02 are ORed through to Channel and DSU Priority, FIG. 206, and Six Position Random Sequence Commutator, FIG. 208, on the lines 204.03 and 204.04. The Channel A Priority Required line 204.02 goes to FIG. 203 to function in the manner previously described. As shown in DSU Timings for Tape Writing, FIG. 274, the first data word is removed from Storage and loaded into the Data Register A positions S through 35, FIG. 2*ss*, for transfer into the Tape Shift Register, FIG. 2*xx* through FIG. 2*aaa*. In the manner described previously with reference to Magnetic Core Storage the contents of the location in Core Storage specified by the Address is placed in the Storage Buffer Register, FIG. 2*ll*. The outputs 142*a*.06*s* through 142*c*.04.35 for each position of the Storage Buffer Register are conditioned according to the bit configuration within the Storage Buffer Register. These outputs are available from the DSU Bus shown in FIGS. 167*c* and 167*d*. The data word is loaded into the Data Register A by bringing up the Storage Bus of the Data Register A lines 212.01, 212.02. In FIG. 212, Storage Bus to Data Registers and Data Registers to Storage Bus, the Channel A Write line 173*a*.08 is up, the Channel A Data B Cycle line 205.02 is up, and at A6(D4) line 222*e*.05 comes up and provides ouputs on the lines 212.01 and 212.02. The DSC is now prepared for the first Word Test and if the Buffer is loaded the Clock starts in the manner previously described with reference to FIGS. 248 and 249. The Tape Shift Register must now be loaded from Data Register A by bringing up the line 260*b*.02. In Shift Register Controls, FIG. 260*a*, the line DSU Register Loaded comes up when the Data Register A Trigger is set, FIG. 195*a*. The line 195*a*.06 has an input to Shift Register Control 1, FIG. 160*a*. A Clock Gate Delay line 248.10 is up for 20 microseconds while a first Word Test is going on and is combined with the Write Call line 255.10 and the DSU Register Loaded to provide an output Write and Load Shift Register S through 17 and Write Load Shift Register position 18 through 35 on the lines 260*a*.02 and 260*a*.03. This causes the Tape Shift Register, FIGS. 2*xx* through 2*aaa*, to be loaded with the contents of the Data Register A which is the first word to be written on tape. With reference to Data Register A Loaded and Set Channel A BDW Cycle Required, FIG. 195*a*, the Data Register A Loaded Trigger is turned OFF in response to Channel A Write line 173*a*.06 and the Tape Demand line 196*a*.01. Tape Load Demand is shown in the Timing Chart of FIG. 274.

Returning once again to Read and Write status of FIG. 266, the line 266.06 is up to provide a Gate for the outputs of the Tape Shift Register positions S through 5 on the Write Busses. All of the bits, the six bits plus the Redundancy bit in the C position, must be read within the 33 microsecond period, at the end of which the Character Gate Trigger is turned OFF. When writing, all 7 bits are written simultaneously 67 microseconds between groups. In Character and Record Controls, FIG. 245, it will be noted that when the Write Pulse line 249.02 came up, it turns ON the Write Check Character Delay Single Shot for 275 microseconds although the Write Pulse line 249.02 dropped down. Subsequent pulses occurring at intervals less than 275 microseconds will cause Write Check Character Delay Single Shot to return. Immediately prior to the first bit being written when the Write Trigger is turned ON, the Write Check Character Delay 275 microsecond Single Shot being ON, keeps the Write Trigger Reset 10 microsecond Single Shot OFF. At the end of 275 microseconds, the Write Trigger Reset Single Shot comes on for 10 microseconds and provides an output on the line 245.07 to the Write Amplifier, FIG. 263, to reset the Write Triggers.

The first Write Echo occurs very close to the Beginning of the 33 microsecond Gate and when the first echo bit is received, it is sent to the Character Gate and Disconnect Circuits of FIG. 250 where it turns ON the Response Timing Single Shot for 6 microseconds and provides an output on the line 250.16 to Character and Record Controls, FIG. 245, to provide the Response indication referred to previously.

In Character and Record Controls, FIG. 245, when the Write Check Character Delay Single Shot goes OFF, the Write Stop Delay Single Shot is turned ON for approximately 3 milliseconds, providing an output 245.08 to Go/Stop Controls, FIG. 240, to reset the Go Trigger and bring down the lines 240.02 through 240.04. As soon as positions S through 5 of the Tape Shift Register are unloaded, it is necessary to immediately shift left to bring the data in positions 6 through 17 into positions S through 5 of the Tape Shift Register. Accordingly, the line 260*b*.03 is brought up due to the Response line 245.11, Tape Word Incomplete line 226.03, and the Write Call line 255.12. Since the Shift Register Controls have been previously covered, the details concerning the shifting of the remaining six bit groups are not given. When the Tape Word is complete, the next word to be written on tape must be in the Data Register A awaiting immediate transfer to the Tape Shifting Register. Therefore, when Data Register A was unloaded DSU Channel A immediately requested a Buffer Data Word Cycle to bring in the next word from Storage to be written on tape. To bring out the next Data Word from Storage, the DSU Address Register A containing the address in the DSC Control Word plus one must be brought out to the Storage Address Register, FIG. 2*hh*, in response to the Address Register A to Storage Address Register line 213.01. In FIG. 213, the Channel A Data B Cycle line 205.03 is up and at AO (D4) the line 222*c*.01 comes up to cause the contents of DSU Address Register A to be placed in the Storage Address Register. Subsequently, the data word at the location specified by the address is brought out to the Storage Buffer Register, FIG. 2*ll*. The Data Register A, FIG. 2*ss*, is loaded in response to Storage Bus to Data Register A lines 212.01, 212.02. The lines 173*a*.08. 205.02 at A6 (B4) and line 222*e* .05 are up to transfer the contents of the Storage Buffer Register to Data Register A. With reference to the Shift Register Controls of FIG. 260*a*, the DSU Register Loaded line 195*a*.05 is up since the trigger is set by Channel A Write Select, Channel Data B Cycle and the B8 (D2) control line 222.15. The Clock Gate Delay line 248.10 and the Write Call line 255.10 provide an output Tape Demand on the line 260*a*.04 to FIG. 196*a* and also combine with DSU Register Loaded line 195*a*.05 to provide Write Load Shift Register 1 and 2 outputs on lines 260*a*.02 and 260*a*.03. Alternately, the Write Call line 255.10, Tape Word Complete line 226.02, and the Sample Pulse line provide the identical outputs.

READ TAPE

A Read Select Instruction (RDS) comes out of Core Storage, FIG. 2*ll*, and enters the CPU during an I cycle whereupon it is decoded whereby it is determined the operation is Read Tape, that the Drum is not in use, and that the Data Synchronizer Channel referred to is not in use. The Operational Registers in the DSC then transmit operational information to the selected Tape Control Unit, FIGS. 2*xx*–2*cc*, where it is stored in registers in the selected Tape Control Unit in the manner described for the Write operation. The Reset and Load Channel Instruction must be provided within a specified time or the risk of Disconnect is involved. Assuming that the Reset and Load Channel is provided, the transmission of a command is accomplished into the Data Synchronizer Channel in a manner identical with that described for the Write operation with the exception that at the completion of the transfer of the information into the Transmission Registers of the Data Synchronizer Channel, a B cycle is not demanded since this time the data is not to be transmitted from Core Storage to the DSC Data Register, FIG. 2*ss*, but instead the Data Register must await the accumulating of a word to be read from the tape into the Shifting Register, FIGS. 2*xx*–2*aaa*, and to be transmitted to the Data Register.

The Tape Control Unit selects a Tape Drive, determines whether or not it is busy as previously described, and if not busy, the tape is put into Read status and the reel put into motion. When the tape gets up to speed, the head reaches recorded information which is read and transmitted in seven bit groups to the High and Low Clip Registers, FIG. 2*bbb*, the Line Register, 2*bbb*, the Read Translators, FIG. 2*aaa*, and finally in a six bit group to the Shifting Register in the Tape Control Unit. A count is kept of the number of six bit characters transmitted to the Shifting Register and when the count reaches six, indicating the register is full and the 36 bits are available, the 36 bits are transmitted in parallel through the I/O Busses to the Data Register inputs. Upon entering of this information in the Data Register, a signal is sent from the Tape Control Unit indicating that a full word has been received which causes an examination in the Data Synchronizer Channel of the Operation Register, FIG. 2*eee*, and the Word Counter, FIG. 2*ooo*, to determine whether or not this word is to be transmitted to Core Storage. Assuming that the Operation Register and the Word Counter are such that a word is to be transmitted to Core Storage, then and only then, is a signal generated by the Data Synchronizer Channel to Core Storage which signal indicates that the Data Synchronizer Channel Data Register has a word to be transmitted to Storage, that the direction of transmission is from Data Register, FIG. 2*ss*, to Core Storage, FIG. 2*ll*, via the DSU Storage Bus Switch and that the Address Register, FIG. 2*mm*, in the DSU contains the address which is ultimately transmitted through the DSU Address Switching, FIG. 2*ww*, to the Address Busses of Core Storage to select the proper location in Core Storage for the receipt of the word. The word is then stored, the DSU Word Counter, FIG. 2*oo*, is stepped down one, and the Address Register, FIG. 2*mm*, is stepped up one. Such an operation continues until several conditions are met as previously described in the writing operation and these conditions are determined by the contents of the Operation Register and the DSU Word Counter. Assuming that the operation is such that when the Word Counter is reduced to zero, a transmission operation is ended, and the Data Synchronizer Channel generates a signal requiring a B cycle of Storage for the purpose of making a reference to Storage at the location specified by the Location Register to provide the Data Synchronizer Channel with a new Command. Alternately, if autonomous operation is not required as specified by the contents of the Operation Register, FIG. 2*eee*, and Word Counter, a synchronized operation with the CPU may result if a Load Channel Instruction is waiting as previously described in the Write Operation. In any event, either the unit disconnects and the entire operation is ended or a new command is received from Core Storage to replace the contents of the Transmission Registers.

More specifically, once the DSU has received a Read Select instruction and a unit is specified, the DSU tries to enter the information in Tape Control Unit. If the Tape Control Unit is not busy, it accepts this Read Select signal and puts it into one of its Class triggers by turning ON the Read Call Trigger and selects the unit designated from which data are to be read. The TCU also accepts the mode in which it is to read, either BCD or Binary. When this information is stored, the Tape Control Unit generates a signal which is sent back to the DSU saying that it has stored this read operation and interrogates the Tape Drive to see if the latter is ready. If so, it starts the drive in motion and after 5 milliseconds the Tape Drive Unit is ready to Read as the tape is up to speed.

With the tape up to speed, the Final Amplifier is ready to receive information. As tape is passed over the Read Head, signals are generated in response to tape bits which are amplified and then clipped at the High and Low Clip levels. After the clipping process, the signals are entered into the High Clip and Low Clip Register, FIG. **228.** Each of these registers feeds a High Clip, FIG. **229,** and a Low Clip, FIG. **230,** Parity Checker where it is checked to see if the lateral parity is correct. If either of these registers is correct, the TCU accepts this Read information and does not indicate an error. If both are incorrect, the TCU indicates a Read error. Assuming now that both High Clip and Low Clip Registers contain correct information, the information is placed into the Line Register, FIG. **231.** The Line Register feeds the LRC Check Register and the Read Transistor, FIG. **232.** The function of the Read Translator is to translate information into the Binary Mode that has been written on tape in the BCD mode so that it may be processed by the CPU in the Binary mode. If the information was written on tape in the Binary mode, it passes directly through the Translators and enters the Tape Shift Register, FIG. **225,** in a Binary form. The Line Register, FIG. **231,** also feeds another Parity Checker, FIG. **233,** which has the function of seeing that the transmission of information from the High and Low Clip Registers into the LRC Check Registers is then without error. From the Read Translator, FIG. **232,** the information is fed to positions 30 to 35 of the Tape Shift Register, FIG. 225*b*. It is pointed out here that when tape is read, there are seven bits and seven bits are checked in the Parity Checkers, but upon leaving the Read Translator only six bits are provided. The C bit, which is strictly a checking bit, is discarded at this time and the useful information only is stored into

the Tape Shift Register. As information is read in the Amplifiers, a Character Gate is generated as stated in Write operation to see that all bits of a character are read in 33 microseconds. During 33 microseconds, all bits should have been read and if not, an error indication is provided due to the Redundancy Check circuits. The tape continues to move and the second group of seven bits written on tape are encountered. This second group of seven bits is read and after clipping are brought into the Amplifiers and checked as stated previously and passed into the Line Register which feeds the Read Translator. The Read Translators feed positions **30** through **35** again, but before the information is entered into the positions **30** through **35** the Shift Less Six Pulse is provided as previously described, which shifts the information in positions **30** through **35** over to positions **24** through **29** and each succeeding group of six is upshifted six positions as well. Therefore, the original group of six bits that was read from tape is now in positions **24** through **29** of the Tape Shifting Register and the second group of six bits now enters positions **30** through **35.**

The process of reading is continued until the full word is received when positions S through **35** of the Shift Register are filled. Once a full word is received, a Tape Demand signal is generated and sent to the DSU indicating that a full word is ready so it should be taken from the TCU. The DSU having received this Tape Demand signal causes the Tape Shift Register positions S through **35** to be placed in the DSU Data Register.

When there is information in the High and Low Clip Registers and the High Clip Register indicates an error but the Low Clip Register is correct, information is accepted from the Low Clip Register and it is this information which is placed in the Line Register. Therefore, on a Read operation both the High Clip and Low Clip Registers do not have to be correct. The fact that one of them is correct parity wise is enough to satisfy the Tape Control Unit. On Read operation, notice that the Match Check is not performed and also that the LRC Check Register has to be correct.

In FIG. **275**, the DSU timings for Reading operations on tape are shown which indicates the duration of the Read Tape command, the Primary Operation transmission, the various B cycles, the conditions of the Word Counter, the times when the Buffer is loaded in response to Buffer Demands, the times the tape are unloaded, and the first Word Test in each instance. B cycles are identified as to whether or not they are data B cycles or control word B cycles.

The instruction RDS + 0762 is contained in the operation portion of a type B instruction which has zeros in positions 1 and 2 and an address in positions 21 through 35. An example in this instance is an address **1221** used for the purposes of illustration which specifies DSC Channel A, Tape Unit **1**, and Binary Mode. Further details of address decoding may be had with reference to FIG. **207** which illustrates the octal and binary manner in decoding addresses for input-output units. With reference to the Instruction Register, Storage Register **3** output is up, Storage Register **4** output is up, Storage Register **5** output is up, Storage Register **6** output is up, and Storage Register **7** output is up causing the Instruction Register triggers **1** through **5** to be set ON by the Reset Instruction Register pulse on the line **99.01.** This provides outputs on the lines **13***a*.06 through **13***a*.08, **13***a*.14 through **13***a*.16, **13***a*.20, **13***a*.21, **13***a*.24 and **13***a*.27. Storage Register **8** output is down and Storage Register **9** output is down so the triggers for Instruction Register positions **6** and **7** in FIG. **13**b are OFF to bring up the Minus on Instruction Register **6** and Minus on Instruction Register **7** lines. In FIG. **13***a*, Storage Register **10** line is up and Storage Register **11** line is down which brings up the lines **13***c*.24 through **13***c*.26 and the lines **13***c*.27 through **13***c*.53. With reference to the Instruction Register Sign Plus and Minus, FIG. **100,** the Instruction Register sign is plus and the lines **100.01** through **100.41** are up. As shown in the Primary Operation Decoder, FIG. **14***b*, the line (7.6) is up to FIG. **14***d* where the lines **14***d*.61 through **14***d*.64 are up. In FIG. **15***a*, Secondary Operation Decoder, Instruction Register **8** line is up, Minus on Instruction Register **7** line is up, Minus on Instruction Register **9** line is up, Primary Operation (7,6) line is up, and Minus on Instruction Register **6** line is up to bring up the lines **15***a*.01 and **15***a*.02. The line **15***a*.01 goes to Secondary Operation Decoder, FIG, **15***b*, to bring up the lines **15***b*.01 through **15***b*.03 to the Class Decoder, FIG. **149.** Since positions 28 through 35 of the Storage Register have been placed in positions 10 through 17 of the Instruction Register the Minus on Instruction Register **11** line **13***b*.05 is up, Minus on Instruction Register **12** line **13***d*.09 is up, Instruction Register **10** line **13***d*.04 is up, and Secondary Operation (0,6) Write line **15***b*.09 is up to provide an output on the line **149.17** which goes to Channel A Data Class Selection, FIG. **173***b*. In the Unit Select Matrix, FIG. **150,** Minue on Instruction Register **14** line **13***d*.19, Minus on Instruction Register **15** line **13***d*.23, Minus on Instruction Register **16** line **13***d*.27 and Instruction Register **17** lines **13***d*.34 are up to bring up the lines **150.39** through **150.42.** The line **150.42** goes to Channel A Unit Selection **1** through **5,** FIG. **179***a*, to turn ON the Unit Select **1** trigger if the Channel A Address Gated line **182***b*.22 is up and the Set Class and Unit Channel A line **172.01** is up. In the Channel Selector, FIG. **153,** Primary Operation line (7,6) is up, and since positions 24 through 26 of the Storage Register contain the octal one or binary 001, then Minus on Storage Register **24** is up, Minus on Instruction Register **25** is up, and Storage Register **26** is up to bring up the line Select Channel A **153.01.** The line **153.01** goes to Command Decoding, FIG **182**a, where it brings up the line Select Channel A, and, in turn, the lines **182***a*.01 through **182***a*.08 and the line **182***a*.20. The Channel A Address line **182***a*.20 goes to Command Decoding, FIG. **182***b*. In Channel A Data Class Selection, FIG. **173***b*, Secondary Operation Read line **15***a*.05 is now up, the Tape Class Address line **149.17** is up, the Set Class and Unit Channel A line **172.01** is up and the Channel A Address line **182***a*.03 is up which turns ON the Tape Read Select trigger and brings up the lines **173***b*.04 through **173***b*.06. In Tape Control, FIG. **159,** Minus on Instruction Register **13** is down since this position contains the binary one. Therefore, the BCD line **159.01** is down which goes to Channel A Data Class Selection, FIG. **173***b*, and since this lien is down, it does not turn On the BCD trigger, and accordingly the BCD Hold lines **173***b*.12 and **173***b*.13 are down. The line **173***b*.03, Tape Class Address goes to Command Decoding, FIG. **182***b*, where it brings up the line **182***b*.22 to Channel A Unit Selection **1** through **5,** FIG **179***a*. There the trigger is set providing this Channel is not in use. According to Channels A and B Class Selection Interlock, FIG. **171,**

the Secondary Operation Read line is up and Minus on Channel A Data Selected line **175.03** and Minus on Channel A Non-Data Selected line **176.05** are both up when the DSC is either selected for data or selected for non-data. The Channel A Address line **182*a*.02** is up and during ER time the outputs are provided on the lines **171.01** through **171.03** and on the line **171.06.** The line **171.06** then goes to Channels A and B End Operation Sychronizer, FIG. **172*a***, where it is gated with an A7 (D1) pulse on the line **222*d*.10** to turn ON the Sync Trigger. The line **172.01** then goes to Channel A Unit Selection **1** through **5**, FIG. **179*a***, to turn ON the trigger Unit Select One mentioned previously. The line **173*b*.04** goes to Read and Write Test, FIG. **258*a***, and the line **258*a*.05** goes to Class and Unit Disconnect Gate and Start Read/Write and Write End of File, FIG. **252,** where it is combined with Set TCU Class and Unit line **253.02** to cause the right hand side of the trigger to begin conducting. Thus, if Not TCU Disconnect line **250.01** is up, as in this case, then Start Read/Write/-Write End of File line **252.01** comes up. When the Read Test Cycle line **258*a*.05** comes down the negative shift is effective to turn OFF the Class and Unit Disconnect trigger which brings up the line **252.02.** The line **252.01** goes to Go/Stop Control, FIG. **240,** where it is used when the Read Call line comes up to initiate the Read Delay. The line **252.01** goes to Set Read Write Status, FIG. **241,** where it has no effect since this is a Read operation. In Data Class Selection, FIG. **255,** the Read Cycle Test lines, **258*b*.02** sets the Read Call trigger bringing up the line **255.01** through **255.08.** The line **258*a*.05** goes to Data/Non-Data Selection and Test, FIG. **258*b***, to turn ON the Schmitt trigger and bring up the Select TCU line **258*b*.07** which goes to the TCU Interlock, FIG. **253.**

In Data Class Selection Interlock, FIG. **174,** the Tape Read Select A line **173*b*.05** brings up the Channel A Data Select line **175.01** which goes to Storage Bus to Word Counters, FIG. **216,** Proceed to E Time, FIG. **202,** and Channel A Set BCW Control Word Required, FIG. **197*a***, where a decision is made as to whether to take an E cycle or a B cycle when a reference to Storage is to be made. The line **179*a*.03** goes to Tape Unit Selector One, FIG **254*a***, where it turns ON the Select Tape Unit trigger provided the Set TCU Class and Unit line **253.02** is up. In this connection reference is made to TCU interlock, FIG. **253,** where Select TCU line **258*b*.07,** TCU Interlock Off line **255.16** and Select Ready and Read line **240.10** must be down in order to provide a positive output to the inverter. Select TCU line **258*b*.07** is up as previously described and TCU Interlock is OFF so that a negative signal is applied to the 25 microsecond Single Shot. The right hand plate of the Single Shot goes up and brings up the lines **253.01** through **253.03.** The line **253.02** sets the Tape Unit trigger in the manner previously described and the TCU Selected line **253.03** goes to Channel A Non-Data Selection, FIG. **177,** to reset the Non-Data Selection trigger. The line **253.02** goes to Data Class Selection where it is combined with Read Cycle Test **258*b*.02** and at the fall of the latter line, the Read Call trigger is set bringing up the lines **255.01** through **255.08.** A Reset and Load Channel instruction is provided within the time required and gives the DSU the word count and initial address in Core Storage.

In Character Gate and Disconnect controls, FIG. **250,** the first bit line **246.01** comes up in response to the first bit read and the negative shift at the output of the inverter turns ON the Character Gate trigger and brings up the lines **250.11** through **250.15.** The line **250.12** goes to BOR/BOF Search and Record Gate, FIG **244,** where it is combined with Not Disconnect Delay to provide an input to the 150 microsecond Hold-Over Single Shot. This Record Gate Single Shot is held on by the Character Gate for so long as tape is being read and thereafter for 150 microseconds. The rise of the line **244.04** goes to the Reset Pulse Generators, FIG. **257*a***, to start the LRC Reset. The Initiate Read Delay line **240.13** from the Go/Stop Controls, FIG. **240,** in combination with the Record Gate brings up the Response Gate line **244.05** which goes to Character and Record Controls, FIG. **245.** The Gated Write Echoes line **246.04** keeps the Response Timing Single Shot up in FIG. **250** and the output **250.16** goes to Characters and Record Controls, FIG. **245,** to bring up the Response lines **245.09** through **245.12.**

The Character Gate line **250.11** goes to Read Clock and Line Register Reset, FIG. **251,** for starting the Clock as explained previously. Six 6 bit groups are read and then in Shift Register Controls One, FIG. **260*a***, the Tape Demand line **260*a*.04** comes up in response to Tape Word Complete line **260.02,** Sample Pulse line **260*b*.01** and Read Call line **255.03.** The Tape Demand line goes to Channel A Control Word Gate and EOR Synchronizing, FIG. **196*a***, where it is amplified and passed on by way of the lines **196*a*.01** through **196*a*.03.** The line **196*a*.01** goes to Data Register A Loaded and Set Channel A BDW Cycle Required, FIG. **195*a***, and a request is made for a Buffer Data Word cycle when the word count is not zero. When a B cycle is taken, the Channel A Data B Cycle line **205.02,** Channel A Read Select line **174*b*.09,** and B2 (D1) line to turn OFF the Data Register A Loaded trigger since the necessary Buffer Data Word Cycle has been taken and the work transferred to Storage. Group Read pulses are provided on the line **260*a*.05** from Shift Register Controls for so long as the Read Call line is up and the Response pulses are coming in on the line **245.11.** In BOR/BOF Search and Record Gate, FIG **244,** the Record Gate Single Shot provides an output until 150 microseconds after the fall of the last Character Gate. At the end of the 150 microseconds, the Record Gate line **244.03** falls and initiates a Disconnect Delay on the Character and Record Controls of FIG. **245** and this brings up the lines **245.03** through **245.06** for 400 microseconds. The Disconnect procedure results only when the reading operation is complete. Accordingly, if multiple words are to be read from tape the Record Gate of FIG. **244** continues to stay up since it is a Hole-Over Single Shot and receives sequential Character Gate pulses.

BACKSPACE TAPE

In performing Backspace Record, there are two situations to be discussed which involve a Backspace record given after a Write operation and a Backspace Record given after a Read operation. In the first case where a Backspace Record is given after a Write operation, assume that the tape has just read a record and a backspace operation is desired. Now when Backspace Record is given, the Control Unit accepts this Backspace Record and brings up the Backspace Call trigger, FIG. **256,** and also the unit, FIG. **254*a***, which is to backspace. The Read-Write Status trigger in the Tape Drive is sensed to determine that the last operation exe-

cuted on that Tape Drive was a Write operation. Therefore, the fact that it is to perform the Backspace on the Drive that had previously been in the Write Status causes the tape to be moved forward for 12 milliseconds before execution of Backspace. The purpose of moving forward before backspacing is to energize the Read/Write Head 12 milliseconds farther forward on Tape to place noise pulses on Tape before proceeding to go in the backward direction. The Backward trigger brings up the Go line in the Tape Drive which drives the tape up to speed in a backward direction. As this Tape Drive proceeds in the backward direction, Final Amplifiers are gated and a search is made for information on tape. As the Read Head passes over information that has been written, it generates First Bit Gates and Character Gates. The Character Gate is used to pulse a 500 microsecond Hold Over Single Shot and as backspacing continues over information, Record Gates continue to hold over this 500 microsecond Single Shot. When an area of tape is reached where there is no information or there is a beginning of our record, there are no more Character Gates and the Hold Over 500 microsecond BOR Search Single Shot drops down at the end of 500 microseconds after the last Character Gate. The fall of this Single Shot pulse is a 2 millisecond Backward Stop Delay Single Shot. The purpose of this single shot is to insure that the Write Head gets beyond the beginning of this record that is being spaced over. At the fall of this 2 millisecond Single Shot, a Disconnect Delay us initiated and at the fail of a 400 microsecond Disconnect Delay Pulse to Go Trigger is turned OFF and the Backspace Record Call trigger and Unit Select trigger are reset with the pulse that is initiated at the fall of 400 microsecond Disconnect Pulse. If a Read Forward operation was initiated at this time, the Record that has just been backspaced over would be read, the machine would stop at the end of the Record and then be ready to execute another Write instruction. However, if in performing this backspace operation, the Tape Drive had not written forward 12 milliseconds before turning off the Write Triggers in the Tape Drive, an area of tape would be neglected in the next Write operation which would leave noise pulses in the middle of a record gap. However, the fact that the machine spaces forward for 12 milliseconds before backspacing places the noise pulse far enough ahead on tape so that on the next Write operation, the noise pulses are erased by the information that is being written.

When a Backspace Record is given on a Tape Drive that has previously been in the Read Status this situation is more simple than the one given when the Tape Drive had been in the Write status, in that no spacing forward before the Backspace Record is necessary. This is because the Tape Drive is already in the Read Status and it is unnecessary to reset the Write status and generate noise. Therefore, Backspace Record after a Read simply backspaces over the record and continues to search for information generating a BOR search as previously described with the Backspace after Write. If a Backspace Record is given after Write End of File Binary, an attempt is made to backspace over a gap on tape on which there is no information written. In this situation, the Tape Drive moves in the backward direction, a Read delay is generated which sets a 28 millisecond Hold Over Single Shot and turns on the First Character Gate Trigger. As movement continues in a backward direction without receiving a Character Gate, this trigger remains ON, and as the 28 millisecond Single Shot does not receive any Character Gate for this 28 millisecond period, it generates an End of File in the backward direction which turns ON the BOR Search Single Shot. This Single Shot provides a Disconnect procedure described in the Backspace Record after Write operation. Therefore, a Backspace Record given in an area of tape in which there is no information written, causes backspace for approximately 33 microseconds and then a Disconnect.

The Tape Control Unit is able to rewind tape from any area on tape as far back as the load point. In the case where the Rewind is given after a Write, the TCU accepts the Rewind instruction, sets a Rewind Call trigger and the Unit Select trigger causing spacing forward for 12 milliseconds before changing from Write Status to Read status. Again the purpose of the spacing forward is to avoid the effect of noise signals which are generated from changing status. When the tape stops going in the foward direction, it moves in the Rewind direction to the Load point.

Once the TCU is in a Rewind status, it sends a signal to the Tape Drive to set Rewind status. Once this signal has been sensed, Tape Drive sends a signal to the Tape Control Unit affirming the Rewind status by setting the Rewind Call Trigger. The fact that the Tape Drive selected is in the Rewind status and the Tape Control Unit has the Rewind Call Trigger set, disconnects the TCU from the Tape Drive. The Rewind Call trigger is reset and the Unit Select triggeris reset so the TCU is free to accept another instruction from the DSU while this Tape Drive is rewinding. A new instruction entering the Tape Control Unit sets the Class trigger, that is, the Read, the Write, or Backspace, and if the unit attempting to perform this next instruction is not the one that is rewinding it immediately performs this next instruction. If, however, the Tape Drive that is attempting to perform this next instruction is the Tape Drive that has previously been set into a Rewind, the instruction waits in the TCU until this Tape Drive Unit reaches the Load Point. When the Tape Drive reaches the Load Point it becomes ready and the next instruction is performed.

The Rewind Instruction given on a Tape Drive that had previously been in the Read status is the same as the Rewind given on a Tape Drive that has been in the Write status with the exception of the Write Forward for 12 milliseconds before a Rewind. In the case of Rewind after a Read Status, the Write forward is not needed as there is no change in status and no noise pulses are generated on tape. Once the Backspace Record and Rewind instruction in the DSU have been entered into the Tape Control Unit and have set the corresponding triggers in the TCU, a signal is generated which indicates that the TCU has been selected and is sent to the DSU to disconnect the latter. This enables the DSU to receive another instruction while the Tape Control Unit is performing this Backspace Record or Rewind. The TCU has an Interlock which determines whether the TCU has a Read Select stored, a Write Select, or Backspace Record, or if the Tape Drive is selected, is ready and is performing a Write or a Read operation. If either of these cases exists, the instruction being provided from the DSU to the tape Control Unit must wait until this interlock is clear. When the operation is complete, the Read trigger, the Write trigger, the Backspace Record Trigger, and so forth, are reset al-

lowing this interlock to gate the instruction coming from the DSU into the Tape Control Unit.

Backspace File caues a backspace over a group of records referring to one topic and separated by an End of File gap. As in the Backspace Record, the Backspace File can be given after a Read or Write and as in the above Backspace Record discussion, a Backspace File given to a Tape Drive that had previously been in the Write status necessitates tape moving forward for 12 milliseconds before the change of status to insure that noise pulses produced by a change of status are put farther forward on tape. As in a Backspace Record, once the tape has been spaced forward for 12 milliseconds, the Backspace trigger in the TCU is turned ON and places the Tape Drive in a backward status. The tape is brought up to speed in the backward direction and as the tape proceeds in the backward direction, it searches for Character Gates as in Backspace Record and Character Gates continue to provide this Beginning of Record search. However, in the Backspace File the Beginning of Record Search Single Shot fires a Hold Over Single Shot called Beginning of File Search. This single shot is a 30 millisecond single shot and its purpose is to hold over until there is a space on tape where there is no Character Gates for a period larger than 30 milliseconds. Therefore, the Backspace File moves tape in the backward direction over records which produce Character Gates. These Character Gates in turn pulse the Beginning of Record Search Single Shot and as this Beginning of Record Search Single Shot falls once for every record it has backspaced over, it pulses a 30 millisecond Beginning of File Search Single Shot. The latter holds over through any number of records in the backward direction. Therefore, once a backspace takes place over the last record of a File in the backward direction the 30 millisecond single shot holds up for 30 milliseconds and at the end of this period it fires a Backward Stop Delay Single Shot for 2 milliseconds. The purpose of the Backward Stop Delay Single Shot is to insure that the Write head gets beyond the File that is being backspaced over. The Beginning of File Search Single Shot fall turns off the Backward trigger, and the BOR Search Single Shot turns off the Delay Read-Write Call trigger. The Backspace Call trigger being turned off first a Backward to Forward Delay 25 millisecond single shot. The purpose of this single shot is to hold the Interlock in the Tape Control Unit from being reset for 25 milliseconds. This insures that once the Tape Drive has been reset to the forward direction that no new instruction is received in the Tape Control unit for at least 25 milliseconds. This permits the mechanical linkages in the Tape Drive to normalize going from the backward to the forward direction.

WRITE END OF FILE

In Write End of File, the TCU accepts a Write End of File call from the DSU and the Unit which is to write this End of File. It also accepts a signal indicative of either the BCD or Binary Mode. Assume in this case that a Binary End of File is to be written when a WEOF is accepted, it causes the TDU to be brought up to speed and interrogates a 40 millisecond single shot. This 40 millisecond Single Shot in turn fires a 7 millisecond Single Shot while the tape is moving and no information is being written on tape. The 7 millisecond Single Shot generates a sample pulse which pulses the Record Gate once and this Record Gate falls at the end of 150 microseconds and initiates a disconnect procedure and resets the Write End of File Call trigger and Unit trigger. It also turns OFF the Go Line in the Tape Drive allowing the tape to stop. Therefore, a Binary Write End of File just spaces a 47 millisecond gap on tape in which there is no information.

In the Write End of File BCD, however, after the firing of the 40 millisecond and 7 millisecond Single Shots which produce a 47 millisecond gap in tape, a Tape Mark is written which consists of 1, 2, 4, 8 bits on tape. This Tape Mark is written followed by its check character and then the Tape Drive Unit disconnects. Therefore in the Write End of File BCD, there is a 47 millisecond gap followed by a Tape Mark. In Writing this End of File in the BCD Mode, the disconnect procedure is slightly different than the Binary Mode. As the Tape Mark is written the Clock is started to generate a Clock pulse. This Clock pulse fires the Hold-Over 275 microsecond Single Shot and the 400 Single Shot. The Write trigger is reset in the Tape Drive Unit and a 3 millisecond Single Shot is pulsed which turns OFF the Go line. Therefore, the tape is instructed to stop moving. Now, 4 milliseconds after writing the Tape Mark, the Read Head picks up the Tape Mark and generates a Record Gate. The Record Gate falling initiates the disconnect procedure, and resets the Write End of File Call trigger and the BCD Mode trigger and the Unit Select Trigger.

POSITIONING INSTRUCTIONS

Positioning Instructions are Rewind, Backspace Record, and Backspace File. Assume a Rewind Instruction is brought into the CPU during an I cycle and is interpreted as a Rewind Tape Instruction which causes a signal to be generated to test the Data Synchronizer Channel. The Data Synchronizer Channel may be busy with a *Data* Transmission instruction, but if it is not busy also with a *Non-data* transmission instruction, the Non-Data instruction such as Rewind immediately enters into the Data Synchronizer Channel, is stored, and a signal is caused to be sent to the CPU allowing the latter to end operation and proceed to the next sequential instruction. If the Data Synchronizer Non-Data Operational Register is not free, then the CPU delays while awaiting access to this register. Assuming that the register is free, the Non-Data Instruction is entered into the Non-Data part of the Operational Register along with the unit specified into the Unit Register. If the Data Synchronizer Channel is not currently executing a Transmission Instruction, the Non-transmitting Instruction immediately generates a signal to the Tape Control Unit and tests it to determine whether or not it is busy. If it is busy in the execution of a previous instruction, the Data Synchronizer Channel retains this information in the Operation Register indefinitely until the Tape Control Unit is free. When the Tape Control Unit is free, the Operational information Rewind Tape Unit End if is then transmitted to the Tape Control Unit whereupon it is stored in a similar Operational Register and Unit Register in the TCU. When storage occurs in the TCU, a signal is sent therefrom to the DSU to clear the Operational Register of both the Unit and the Operation. Having entered the Tape Control Unit, the Rewind Instruction now tests the specified Tape Unit to determine whether or not it is in use. If it is in use performing a Rewind, the Operation is treated as a "no

operation". The instruction is not executed, the Tape Control Unit Registers are cleared, the interlock is reset and the unit is made ready for accepting any other instruction. Assuming that the tape is not at the load point and, is not rewinding, then the Tape Drive is selected and the Rewind Instruction is stored in a series of relays in the Tape Drive. The Tape Drive disassociates itself from the Tape Control Unit and commences the Rewinding operation and the Tape Control Unit Registers are cleared and made available for the acceptance of any further instructions from the Data Synchronizer Channel. The Tape Drive continues rewinding until the Load point is reached when the Tape Drive reverts to Ready status and prepares itself for the acceptance of any further commands directed to it.

KEEPING A TAPE IN MOTION

Once started, the tape moves at a constant speed until the DSC word register is reduced to zero following a IOCD command. The Tape then continues its motion to about the middle of the end-of-record gap and stops. If the WRS or RDS instruction for the following record has been issued by the main program and is waiting execution when the tape is ready to stop, the new select instruction will be in effect and tape motion will continue at undiminished speed.

Failure to keep a tape in motion may not increase the total running time of the program. Records may be processed on two different tapes attached to the same DSC without loss of time, despite the fact that both tapes will stop at every end-of-record. This is possible because, in crossing an end-of-record gap, the tape unit is always connected to the TCU for a total of 10.5MS regardless of the physical speed of the tape. If the tape stops, the TCU disconnects when the read gap has passed the longitudinal redundancy bits of the last record. The write gap is near the mid-point of the inter-record gap at this time. While the tape is coming to a stop, any second tape attached to the same DSC may be started, as the TCU is free to accept a new select instruction.

If the tape receives a new select instruction while it is slowing, acceleration occurs again. The tape drive is geared so that regardless of the tape unit motion when it begins acceleration, the time taken to reach the beginning of the next record is constant. (Approximately 10.25 and 6.25MS for read and write gaps, respectively.)

Similarly, when a tape is to stop, the time taken to move from the end of the last record to the point on the tape where the TCU disconnects the tape constant (approximately 25 and 4.25MS for the read and write gaps, respectively).

READ CARD OPERATION

The Read Card Instruction enters the CPU whereupon it is transmitted to the Data Synchronizer Channel if the latter is ready to accept it. The Data Synchronizer Channel then selects a Card Reader and puts it into motion and a Reset and Load Channel Instruction as previously described is provided from the CPU within a specified time. This provides information for the Transmission Registers in the Data Synchronizer Channel and thus controls the flow of information from Card Reader via FIG. 2uu into the Data Register and from the Data Register via Storge Bus Switching to Core Storage at an Address specified by the contents of the DSC Address Register. The speed of the Card Reader is such that on the average, a number of milliseconds elapse between the transmission of words to the Data Register, but the maxiumum instantaneous speed is very similar to tape and is approximately 400 microseconds between any two words transmitted from the Card Reader. Therefore, for as far as maximum instantaneous rates of information flow the Card Reader is just as fast as the tape.

WRITE PRINTER OPERATION

A Write Printer Instruction enters the CPU whereupon it is transmitted to the Operational Register of the Data Synchronizer Channel followed in a specified period of time by a Reset and Load Channel Instruction which provides information to the Transmission Registers of the Data Synchronizer Channel. In the Writing operation, as the Transmission Registers are loaded with information, a B cycle is demanded and data is transferred from Core Storage to the Data Register. Here a special case developes. The Data Register places its 36 bits immediately into the high order of the 32 bit Thyratron Register, FIG. **2*uu*** (FIGS. **168*a*** and **6**), whereupon the Data Register is cleared in about 400 microseconds and another reference to Core Storage is made to load the Data Register with a second word. The second word is loaded into the low order of the 72 bit Thyratron Register and the feeding rate of the Printer is slow enough so that the two words spaced roughly 400 microseconds apart are stored in the Thyratron Registre for a number of milliseconds until the Printer reaches a point in its cycle where it accepts the information contained in the Thyratron Register for printing, after which the Thyratron Register is cleared and the cycle repeats itself. This operation continues as previously described for Writing tape until the combination of the DSC Word Counter and Operation Register conditions are satisfied when the operation ends.

LOAD CHANNEL INSTRUCTION

The Load Channel A instruction (LCA) has an Operation code +0544 which is contained in positions S and 3 through 11 of the Storage Register. The Load Channel instruction is a synchronizing type of instruction. That is, if Channel A is selected but is still executing a Control Word, the Central Processing Unit waits until the Word count is reduced to zero or in the case where the tape is being read and the B trigger is ON until the End of Record is reached, before executing the instruction. In terms of decoding it differs from the Reset and Load Channel instruction in the Units position of the octal operation code. Actually the distinguishing part between Load Channel instructions in general and the Reset and Load Channel instruction is that the Load Channel instructions contain a binary 1 in position 9 of the Storage Register whereas position 9 of the Storage Register in the case of Reset and Load Channel Instructions contains a binary 0. With this in mind, reference is made to the Primary Operation Decoder, FIG. **14*d***, where the lines **14*d*.26** through **14*d*.32** are up since this is a Load and Reset Load Channel line. The line **14*d*.26** goes to Cycle Timer Controls, for bringing up the B cycle Interrupt line and for turning on the Cycle Timer Control trigger under certain conditions. The line **14*d*.27** goes to B Time Control, FIG. **121**, where the Instruction Register **7** line **13*b*.49** is up. It is pointed out that the latter line is not up during the Reset and Load

Channel instruction. Therefore, during ER time and at A11 (D1) in response to a B cycle demand on the line **199.03** from the DSU, the Go to B Time trigger is turned ON and the line **121.01** is sent to the Cycle Timer Control. The line **14***d*.**28** goes to the Channel Selector, FIG. **153** where it brings up the Select Channel A line **153.01** in the case of the Load Channel A instruction since the Primary Operation (5,4) line **14***d*.**28** is up, Minus on Instruction Register **8** line **13***c*.**04** is up, and Minus on Instruction Register **9** line **13***c*.**41** is up with the Instruction Register Sign Plus. The Channel Select A line goes to Command Decoding in the DSU, FIG. **182***a*, and Data Class Selection Interlock FIG. **175.** If the Minus on Channel A Data Select line **175.02** is up and the Minus on Channel A Non-Data Selected line **176.06** is up, then the Channel A In Use line to the Central Processing Unit is down. However, if one or the other of the input lines is down then Channel A In Use output line is up to Channel Controls, FIG. **162.** The line **14**d.**29** goes to End Operation, FIG. **128**a, to bring up the End Operation Control line **128***a*.**01** if the IA control trigger is OFF during E time. However, since the Central Processing Unit has found the DSU in use and an Execute cycle is withheld, the End Operation control remains down and the Central Processing Unit waits. The line **14***d*.**30** goes to Enter/Execute, FIG. **155,** where Proceed to E Time Control line **202.01** must be up to provide a Go to Execute signal on the line **155.01.** With reference to Proceed to E Time, FIG. **202,** when the Minus on DSU B Cycle Demand line **199.04** is up then the Channel A/B Execute Cycle Required line **200.01** is up and the Trigger is turned ON to direct the Central Processing Unit to proceed to E time when the DSC may be loaded from Core Storage from the location specified by the address in the Load Channel instruction. The line **14***d*.**31** goes to Interlock Test Skip Control, FIG. **154,** where it is combined with the DSU End Operation Control line **156.02** to bring up the line **154.03.** This line goes to End Operation Mixing, FIG. **156,** and from there to End Operation Controls, FIG. **128.** The line **14***d*.**32** goes to Cycle Timer Control, FIG. **118,** where it is combined with Minus on Go to E time, Trapped Transfer Control, IA Instruction, Store and Trap, **19** until CT**1,** and End operations Trigger Off to cause a Go to ER time control line to come up. The latter causes the Central Processing Unit to take continued ER cycles until the DSC is free.

STORE CHANNEL INSTRUCTION

For the purposes of illustration, Store Channel A instruction SCA +0640 is used although it is understood that there are Store Channel instructions that operate in like manner for Channels B through F. In FIG. **14**d, Primary Operation Decoder, the Instruction Register lines **1, 2, 3, 4** and **5** are up and provide an output to the Primary Operation line (6,4) and also provide an output Store Counters to the DSU Command Decoding, FIG. **182***a*, where it brings up the line **182***a*.**17.** The line **182***a*.**17** goes to Channel A and B Store Samples, FIG. **211,** where it is combined with a Channel A Address line **182***a*.**08** and an E2 (D8) line **222***e*.**15** to provide Store outputs to the Channel A Indicators (FIG. **2***eee*), the Location Register (FIG. **2***qq*) and the Address Register (FIG. **2***mm*) in the location specified in Storage by the address of the Store Channel instruction. However, these last mentioned lines do not come up until E2 (D8) time when the CPU and the DSU share an E cycle. The Primary Operation (6,4) line goes to FIG. **14***d* where it provides outputs on the lines **14***d*.**48** through **14**d.**50.** The line **14***d*.**48** goes to Channel Selector, FIG. **153,** where Minus on Instruction Register **8** line **13***c*.**04,** Minus on Instruction Register **9** line **13***c*.**41,** and Instruction Register Plus along with Primary Operation (6,4) bring up the Select Channel A line **153** to the DSU. The line **14***d*.**49** goes to Address and Operation Control, FIG. **145,** where it brings up the Store Tag Control line **145.05** and the Store Address Control line **145.05,** during E time with the Minus on Store Tag line up. The line **145.05** is fed back to bring up the Store Decrement Control line **145.03** and also the Store Prefix Control line **145.01.** The lines from FIG. **145** goes to Read/Write Controls of FIG. **146** where they bring up the Read/Write Controls for Core Storage in response to DSC Store Control line. The line **14***d*.**50** goes to End Operation Controls, FIG. **128***a*, to call for an End Operation on the line **128***a*.**01** during E time with the IA Control trigger OFF. When the Execute cycle is taken, the contents of the Address Register, the Location Register, the Indicator Trigger Registers are placed in the location in Core Storage specified by the Storage Address Register, FIG. **129,** which contains the address portion of the Store Channel Instruction.

TRANSFER ON DSC IN OPERATION

For the purposes of illustration DSC A will be discussed although the explanation is applicable to the other DSC Channels as well. Transfer on DSC A In Operation (TAO +0060) provides for the operation such that if DSC A is in operation, the Central Processing Unit takes its instruction from the location specified in the Transfer on DSC A instruction itself. The operation of the Data Synchronizer Channel is not effected. If DSC A is not in operation, the calculator proceeds to the next instruction in sequence. In the Primary Operation Decoder, FIG. **14**a, the Instruction Register lines **1, 2, 3, 4** and **5** are up to provide an output on the Primary Operation (0,6) line which goes to the Primary Operation Decoder, FIG. **14***c*, to bring up the lines **14***c*.**20** through **14***c*.**22.** The line **14***c*.**20** goes to Indexing Execution Controls FIG. **35***a*. However, Instruction Register **6** line is down and no output is provided. The line **14***c*.**21** goes to DSU Conditional Transfer, FIG. **161***a*, where the decision is made on whether or not to transfer. Minus on Instruction Register **6** lines, Minus on Instruction Register **7** line, and Minus on Instruction Register **8** line are up and are combined with the Primary Operation **(0,6)** to provide outputs to four AND circuits. Instruction Register Sign Plus line is up, Minus on Instruction Register **9** line is up and if the Channel A is in use, as shown in the previous explanation, conditioned Transfer control lines **161***a*.**01** and **161***a*.**04** are brought up. The lines **161***a*.**01** and **161***a*.**04** go to Conditional Transfer Execution Controls, FIG. **24,** where an output **24.03** is provided to Instruction Counter Transfer Control, FIG. **109.** The line **109.02** goes to Address Register, FIG. **16***a*, to advance the Address Register by 1, the line **109.03** goes to Reset Instruction Counter Address Switch to Instruction Counter, FIG. **108,** where during ER time and at A**10** (D2) the Instruction Counter is reset on the line **108.01.** The line **109.01** goes to Address Switch Input Controls, FIG. **110,** where it is combined with End Operation Trigger On and AO (DI). However, the line **109.01** is down and

therefore suppresses the usual Gated Minus on AO (DI) line **110.05** and Gated AO (DI) line **110.06.** Since the Store and Trap line is down, Trapping Control line is down and the Trapping Mode and Not Transfer line **107.01** status is immaterial, the I9 until CT1 line carries Adder to Address Switch line **110.04** to load the contents of positions 21-36 of the SR (the address of the Transfer Instruction) from the Adders to the Storage Address Register, FIG. **129.** The line **14***c*.**22** goes to Address and Operation Control, FIG. **145,** to Address Switches to Storage Bus, FIG. **75,** to Indirect Addressing Controls, FIG. **98,** and to Address Switch Input Controls, FIG. **110.** The line **14***c*.**22** going to Address Switch Input Controls is combined with Trapping Mode at E6 (D4) to bring up the Instruction Counter to Address Switch Control line **110.01** to cause the contents of the Instruction Counter to be entered into the Storage Address Register, FIG. **129.** If Channel A is in use as indicated by DSU Conditional Transfer Circuits, FIG. **161***a*, then the contents of the Storage Register positions **21** through **35** are placed in positions 3 through 17 of the Adder and are gated through the Address Register to Storage Address Register, FIG. **129,** to cause the Central Processing Unit to take the next instruction from the location specified by the Address part of the TAO instruction. However, if Channel A is not in use and the Conditional Transfer Control lines **161***a*.**01** and **161***a*.**02** are down and the Central Processing Unit proceeds to the next instruction in sequence in the normal manner.

TRANSFER ON DSC A NOT IN OPERATION

In Transfer on DSC A Not in Operation TAM −0060, if the DSC A is not in operation, the Central Processing Unit takes the next instruction from the location specified by the address in the TAM instruction and proceeds from there. If DSC A is in operation, the calculator proceeds to the next instruction in sequence. The instruction TAM differs from the instruction EAO in that the former is negative whereas the latter is positive. Therefore, decoding of the operation part is the same with the exception that Instruction Register Sign Plus and Minus, FIG. **100,** causes the lines **100.01** through **100.41** to be up. With reference to Primary Operation Decoder, the line **14**c.**21** goes to DSU Conditional Transfer Controls, FIG. **161**a. Primary Operation (0,6) line is up, Minus on Instruction Register **6** line is up, Minus on Instruction Register **7** line is up, Minus on Instruction Register **8** line is up to bring up the output of the AND circuit. The output is combined with Instruction Register Sign Minus on Instruction Register **9** line to provide an output Conditional Transfer Control on the lines **161***a*.**01** and **161***a*.**04** if the line Channel A Not in Use is up. This provides the alternate option from the transfer on DSC A in Operation. With the Channel A Not in Use, the calculator takes the next instruction from the location specified by the Address in the TAM instruction and proceeds from there. In this instance, the contents of the Storage Register positions **21** through **35** are placed in positions 3 through 17 of the Adder, are transferred by the controls Adders to Address Switch through the Address Register and into the Storage Address Register, FIG. **129.** On the following E cycle, the contents of the location specified by the Address in the TAM operation is placed in the Storage Buffer Register, FIG. **211,** and transferred from there into the Storage Register, FIGS. 2*b* through 2*d*.

TRANSFER ON REDUNDANCY CHECK (TAR)

In Transfer on DSC A Redundancy Check TAR +0022, if the Tape Check Indicator is ON the calculator takes the next instruction from the location specified by the Address in the instruction and proceeds from there. If the Tape Check Indicator is OFF the calculator proceeds to the next instruction in sequence. With reference to Primary Operation Decoder, FIG. **14**a, Instruction Register line **5** is up, $\overline{4}$ is up, $\overline{3}$ is up, $\overline{2}$ is up, and $\overline{1}$ is up to bring up the Primary Operation **(0,2)** line. In FIG. **14***c*, the Transfer lines **14***c*.**07** through **14***c*.**11** are up. In the DSU Conditional **1** Transfer circuits, FIG. **161***a*, the Primary Operation (0,2) line **14***c*.**11** is up, Minus on Instruction Register **6** line is up, Minus on Instruction Register **7** line is up, and Instruction Register **8** line is up to provide an output Transfer Tape Check on the line **161***a*,**02** which goes to Command Decoding, FIG. **182***a*, to bring up the Transfer on Redundancy Check Channel A lines **182***a*.**18** to **182***a*.**19.** The line **182***a*.**19** goes to DSU Store/Skip and Conditional Transfer Controls of FIG. **189,** the line **182***a*.**18** goes to Channel A and B Tape Check Indicators, FIG. **185,** where it turns OFF the Channel A Tape Check Trigger if the latter is ON at I2 (D2). However, if the Channel A Tape Check Trigger is ON an output is provided on the line **185.01** to DSU Store/-Skip and Conditional Transfer Control, FIG. **189,** where it is combined with Transfer on a Redundancy Check to bring up the Conditional Transfer Control line **189.03** which goes to Instruction Couter Control, FIG. **109** to bring up the Instruction Counter Transfer Control or Store Trap lines **109.02** and **109.03.** The line **109.02** advances the Address Register by 1 and the line **109.03** goes to Reset Instruction Counter Address Switch Instruction Counter **108** where during ER Time at **A10** (D2) the Instruction Counter is reset. The line **14***c*.**10** goes to Address in Operation Control, FIG. **45,** and to Address Switches to Storage Busses, FIG. **75,** as described previously. The line **14***c*.**22** goes to Advance Instruction Counter, FIG. **107,** to Indirect Addressing Controls, FIG. **98,** and to Address Switch Input Controls, FIG. **110.** Since the Tape Check Indicator was ON the Central Processing Unit took the next instruction from the location specified by the Address in the Transfer on Redundancy Check instruction.

TRANSFER ON DSC A END OF FILE

The TAF instruction +0030 turns OFF the EOF indicator if the latter is ON and takes the next instruction from the location specified by the TAF instruction and proceeds from there. If the End of File Indicator is OFF, the calculator proceeds to the next instruction in sequence in the usual manner.

In FIG. **14***a*, the Primary Operation line (0,2) is up to FIG. **14***c* where the lines **14***c*.**07** through **14***c*.**11** are up. The line **14***c*.**11** goes to DSU Conditional Transfer, FIG. **161***a*, where it is combined with Instruction Register **6** line, Minus on Instruction Register **9** line, Minus on Instruction Register **8** line, and Minus on Instruction Register **7** line to bring up the line **161***a*.**03.** This line goes to Command Decoding, FIG. **182***a* where it is combined with Instruction Register Plus line to bring up the lines **182***a*.**25** and **182***a*.**26.** The line **182***a*.**25**

goes to turn OFF the Channel A EOF Indicator if ON at I2 (D2) via line 222c.07.

Previous to the EOF Indicator being turned OFF, the line 187.02 is up to DSU Store, Skip, and Conditional Transfer Controls of FIG. 189. The line 182a.26 goes to FIG. 189 where it combines with the line 187.02 to bring up the line 189.03 to Instruction Counter Transfer Control, FIG. 109. The lines 109.01 through 109.03 function to cause the CPU to refer to the location in Storage specified by the TAF Instruction. The line 109.01 suppresses the line 110.06 in FIG. 110, and the I9 until CT1 line brings up the Adder to Address Switch Control line 110.04.

STORE OPERATION IN GENERAL

It is pointed out that certain of the machine operations are automatic during this general class of operation and that such operations are suppressed on other operations in accordance with the specific instruction. Normally, Storage Bus to Storage Register occurs at I7 (FIG. 53); Storage Register Hold comes down at I7 (FIG. 5e); Storage Register to Adders occurs at I9 (FIG. 86); Adders to Address Switches comes up at I9 (FIG. 110); Storage Register to Instruction Register is up at I10 (FIG. 99); the Store Controls are up at 110.5 (FIG. 145); the Instruction Counter is advanced at I11 (FIG. 107); Address Switch to Address Register is up at E0 (FIG. 110); Accumulator Register to Storage Bus comes up at E6 (FIG. 11a); End Operation Trigger is on at E10 (FIGS. 128b and FIG. 118) and Instruction Counter to Address Switch is up at I10 (FIG. 110).

ARITHMETIC OPERATION IN GENERAL

Normally, the Storage Register to Adder Controls are up at I0 following the last E or E/R cycle (FIG. 54). Set Accumulator Sign is up at E9 (FIG. 61 and 62), Adder to Accumulator is up (FIG. 70 and 57), and End Operation Trigger is on at E10 (FIGS. 118 and 128b).

SETTING OF THE INDICATORS

In Channel A Indicators S, 1 and 2 of FIG. 165a, assume that the triggers are OFF as indicating "zeros" in positions S, 1 and 2 of the DSC Control Word. Accordingly, the lines 165a.02, 165a.03, 165a.05, 165a.08 and 165a.09 are up. The lines 65a.03, 65a.05 and 65a.08 go to SLC/RLC End Operation Check, FIG. 188, where they combine with Channel A SLC/RLC line 182b.01 and Synchronous Load Channel Mode Line 182b.11 to bring up the Synchronous Load Channel/Reset Load Channel End Operations Check line 188.01 to Channels A and B Class Selection Interlock, FIG. 171. Here, the End Operation Check Line keeps the Gate Sync Trigger line 171.06 up and when not at Tape End of Record and the word count is not 0, the DSC continues transmitting words from the Input/Output Unit to Storage. In Channel A Set ECW Control Word Required and Data Disconnect, FIG. 198a, Channel A Indicator S Off line 165a.04, Channel A Indicator 1 Off line 165a.05, Channel A Indicator 2 Off line 165a.08, and Channel A word counter 0 line 165b.09, combine to provide an output which in turn is combined with Channel A Read Select 175b.08 and A9D1 line 222d.16 to provide an output, which, in turn, combines with Channel A Priority 206.01 and B Cycles 1 22b.09 to bring up the Conditional Channel A Data Disconnect set trigger line 198a.06. The latter line is fed back on the same figure to Channel A Data Disconnect line 198.06 to bring up the Reset Write Clock Gate when the word count is 0. The Data Disconnect line initiates a disconnect procedure and the Reset Write Clock Gate is used on a Write Operation only.

When Channel A Indicator 2 is ON and Channel A Indicator S and Indicators 1 are OFF, the operation thus prescribed is to bring a control word into the DSC from the location specified in the Address part of this Control Word. In FIG. 165a, the lines 165a.10 and 165a.11 are up in this instance. In Channel A Set Buffer Control Word Required, FIG. 197a, Channel A Priority 206.04, Channel A Data Selected 197a.01, Channel A Indicator 2 on 165a.10, Channel A Indicator S OFF 165a.01, Channel A Indicator 1 OFF 165a.05 and A9(D1) line 222d.10 set Channel A Control Word Buffer Cycle Word Required line 197a.01. This circuit decides whether to take an Execute cycle or a Buffer cycle. The line 197a.01 goes to Channel A and B BCW Required and B cycle Demand, FIG. 199, where it turns ON the BCW Trigger and brings up the output lines 199.03 through 199.05 and 199.06. The line 199.05 goes to Channel And DSC Priority Required, FIG. 204, where it is effective to turn on the Channel A Priority Required Trigger, if Channel B is not demanding the B cycle at D0 (D2) on the line 222b.06. The line 199.03 DSU B Cycle Demand goes to B Time Control, FIG. 121, where it is effective to turn ON the Go to B Timer Trigger.

In FIG. 198b, the Channel Indicator 2 ON line, in combination with Condition Set BCW Control Word Required, Channel A line brings up the Channel A/B Set Control Word/Execute Control Word Required line 198b.01 if Channel B Synchronous Load Channel or Reset Load Channel, Minus on Channel B SCL/RLC Gate and SCL Mode line 182b.13 is up. This line goes to DSU Execute Cycle Required where it turns ON the DSU ECW Trigger and brings up the line 200.01. The line 200.01 goes to Proceed to E Time, FIG. 202, where if the line Minus on DSU B Cycle Demand line 199.04 is up, the Proceed to E Time Trigger is stepped and an output is provided on the lines 202.01 and 202.02 to the Central Processing Unit. In Enter/Execute Controls of FIG. 155, the Primary Operation (5,4) on the line 14b.30 signifies a Load Channel. The Go to Execute (IO) line 155.01 is up to the Cycle Timer Control, FIG. 118, to bring up the lines 118.01 and 118.02 Go to Execute Time.

In Address Register to Storage Address Register Controls, FIG. 213, the Channel A Indicator 2 ON line 165a.11 is combined with Channel A Transfer Mode line 202.09 to bring up Address Register to Storage Address Register lines 213.01 and 213.02. The line 201.09 is up from Channel A and B Transfer Mode Triggers, FIG. 201, where controls are provided to transmit from the DSC during the Buffer cycle. In Storage Bus to Control Registers, FIG. 215, Channel A Indicator 2 On line 165a.11 is combined with Channel A Transmit Mode line 201.10 and A3 (D2) line 222d.01 to bring up the line 215.03, Storage Address Register Channel A Location Register, Channel A Address Register, Channel A Location Register. In Channel A Clamp Register Reset, FIG. 219a, the Channel A Indicator 2 On line 165a.11 is combined with Channel A Transmit Mode line 201.10 and AO (D2) line 219a.04, to provide an output on line 219a.01 to reset the Channel A Location Register.

Channel A Indicators S and 2 OFF and Channel A Indicator 1 ON signify Input/Output of a Record and Proceed, The Channel A Indicator 1 ON lines **165a.06** and **165a.07** are up. The line **165a.06** goes to Card End of Record, End of File and Reselect, FIG. **186**, where it combines with the Reset Clock Gate line **198.08** to reselect the Card machine by way of the line **186.01** or Indicator 1 On line **165a.06** combines with Word Count Not Zero line **165b.02** and Data Register A Loaded line **195a.04** to bring up the Reselect Card Machine line **186.01** provided the Card End of Record line **186.02** is up. The Channel A Indicator 1 On line **165a.06** goes to Channel A Read Gate and Write Clock Control, FIG. **194a**, where it is combined with Channel A Tape Read line **173b.05**, Channel A Indicator S Off line **165a.02**, and Channel A Word Count Zero line **163b.11** to turn OFF the Channel A Tape Read Gate **194.02** when the word count goes to "zero." The line Channel A Indicator 1 On **165a.06** goes to Channel A Set Buffer Cycle Control Word Required, FIG. **197a**, where during the Write operation with Channel A Indicators S and 2 Off and End of Tape Indicator Off during a Control Word Gate, the Set Channel A Control Word Buffer Cycle Required line is brought up and the Set BCW/ECW Control Word line is up. When reading the same, two lines are energized with Channel A Indicator 2 OFF and Channel A End of Record.

With S Indicator ON and Indicators 1 and 2 ON, the operation signifies an octal 3 or Input/Output of a Record and Transfer. In FIG. **198a**, the condition Set DCW/ECW Control Word Required line **197.02** is only up when Channel A Indicator 1 is ON which is octal 2. Octal 3 code requires both set BCW/ECW Control Word Required and Channel A/B ECW Required line **198a.01** to be brought up by a combination of S OFF and Indicators 1 and 2 ON. The line **197a.02** is brought up during the Read operation with the Channel A Indicator 1 On line and the Channel A End of Record line. In the Write operation, the Channel A Write Select Channel A Indicator S off, Channel A End of Tape Indicator Off, and Channel A Indicator 1 ON bring up the line **197a.02.** The important point is that the line **197a.02** can only be up when S Indicator is OFF and Indicator 1 is ON. Therefore, in FIG. **198a**, the conditioned set BCW/ECW Control Word Required line **187a.02** is combined with Channel A Indicator 2 On to provide the Input-Output of the Record and Transfer, FIG. **198b**. The line **198a.01** provides an output on the line **198b.01** which goes to DSU BCW Required. FIG. **200**, to turn ON the trigger and bring up the line **200.01.**

With Indicator S ON and Indicators 1 and 2 OFF an Input-Output with Count Control and Proceed operation is prescribed. The Proceed operation signified in FIG. **197a**, by the lines Channel A Indicator 2 Off, Channel A Indicator A On, Channel A Control Word Gate where at A9 (D1) the line **222d.16** comes up and provides an output on the Set Channel A Control Word BCW Required. This line calls for a Buffer Control Word. The line **196a.05** is controlled in part by the Channel A Word Count Zero line **163b.08** which provides for an Input operation with Count Control and Proceed.

Inputs-Outputs with Count Control and Transfer is prescribed by Indicator S being ON, Indicator 1 being OFF, and Indicator 2 being ON. Generally, Indicator S being ON provides for Count Controls, whereas Indicator 2 being ON provides for Transfer. The line **65a.04** goes to Channel A Set BCW Control Word Required, FIG. **197a**, where Channel A Word Gate **196a.05**, Channel A Indicator S ON line **165a.04**, Channel A Indicator 2 OFF line **165a.08** and A9(D1) line **222d.16** bring up the Set Channel A Control Word BCW Required line **197a.01.** In FIG. **165a**, the line **165a.10** goes to Address Register to Storage Address Register, FIG. **213**, where it is combined with Channel A Transmit Mode Octal line **201.09** to transfer Adder Register A to Storage Address Register. When the word count goes to 0, a synchronous Load Channel operation is performed provided a Load Channel instruction is waiting. If a Load Channel instruction is not waiting the DSU is disconnected as previously explained.

Input-Output Until Signal Then Proceed (6 octal) refers to transmitting data until either the word count is 0 or End of Record is set and takes the next sequential control word. Indicator S is ON, Indicator 1 is ON, and Indicator 2 is OFF. In FIG. **197a**, with Channel A Indicator 2 OFF line **165a.08** is up with either Channel A Control Word Gate, which depends upon the Word Count Not Zero, or Channel A End of Record **196a.06.** The Set Channel A Control Word BCW Required line **197a.01** is up to cause a Buffer Control Word cycle in response to a B cycle Demand.

Input-Output Until Signal Then Transfer (7 octal) is designated by Indicators S, 1 and 2 all being 1. In FIG. **197a**, Channel A Indicator S On line **165a.04** is up and Channel A Control Word Gate line **196a.05** is up when the word count is **0.** With Channel A Indicator 1 ON and Channel A End of Record Sensed during a Read operation, the line **197a.02** is up. In the first instance, the condition of the line depends upon the Indicator S and in the second instance the condition of the line depends upon the Indicator 1. In FIG. **198a**, the line **197a.02** is combined with Channel A Indicator 2 ON and the conditions here are those imposed by Indicators S, 1 and 2 being ON which provides for a synchronous Load Channel operation if a Load Channel instruction is waiting and the DSU is not disconnected.

The Indicator 19 determines if the data is to be stored or is not to be stored and is effective on the Read operation only. With reference to FIG. **165c**, if a bit is present in Control Word position **19** and the line **167d.06** is up, the Upon the Transfer Storage Bus to Channel A Indicators signal on the line **215.01**, the Schmitt trigger is set to bring up the lines **165c.03** through **165c.05.** In Step Control Registers, FIG. **217**, the Card or Tape Demand line is up, Channel A Read Select line is up, and with Channel A Indicator **19** ON, an output is provided to step Channel A Word Counter which is necessary whether the word is stored or whether the word is not stored. In FIG. **196a**, the Channel A Indicator **19** On line **165c.03**, the AOD4 line **222e.06**, Channel A Read Select line **173b.08**, and the Channel A Word Count Zero line **163b.08** combine to give an output on the Channel A Control Word Gate line **196a.05.** In FIG. **194a**, Channel A Read Gate and Write Clock Control, Channel A Indicator **19** Off line **165c.02** is down and normally this line is up to set the Tape Read Gate trigger. In this instance, the Tape Read Gate trigger cannot be turned ON and furthermore Channel A tape Read Select line **173b.05** is up and Channel A Indicator **19** On line **165c.04** is up to turn the trigger OFF and keep the tape Read Gate line **195a.02** down. Accordingly,

Operation Register, the Address Register and the Location Register through the DSU Storage Bus Switching and DSU Address Switching as previously described. This is a B cycle operation and at 9 time in the Control Word B Cycle which is currently transferring, a control word or command from Core Storage is placed in the Data Synchronizer Channel Operation Registers, Location Register, and Word Counter Register and Address Register. As soon as it has been determined that this is a Transfer, a signal is generated causing the following sequence of events: (1) a new Demand signal is immediately generated requiring another Buffer Control Word B cycle for the Data Synchronizer Channel. The contents of the Location Register of the Data Synchronizer Channel are reset and the information contained in that register destroyed. The contents of the Data Synchronizer Channel Address Register are passed through the Data Synchronizer Channel Address Switching on to the Address Busses to Core Storage and are set into the Core Storage Address Register at 0 time. At 4 time of the following B cycle, these busses are sampled through the Data Synchronizer Channel Address Switching into the Data Synchronizer Channel Location Register and the contents of the Data Synchronizer Address Register are reset and the contents destroyed. As the new control word enters at 9 time, the operation part of the new control word is entered into the Operation Register replacing the Transfer instruction. The word count portion is placed in the Word Counter, the address portion is stored in the Data Synchronizer Channel Address Register and this completes the operation. It should be pointed out at this time that if the second control word is also a Transfer instruction, the previously described process continues.

The purpose of this instruction is to make possible the provision of a table of control words in Core Storage at the end of which a Transfer instruction may be provided which will loop back to the beginning or any other portion of the program and in any other place in Core Storage. This provides a complete branching facility automatically and autonomously on the part of the Data Synchronizer Channel without logical interference or testing or any logical communication whatsoever with the Central Processing Unit. The Central Processing Unit, however, may monitor the status of the Data Synchronizer Channel at any time by means, for instance, of the Store Channel instruction. A Store Channel instruction executed by the Central Processing Unit may provide a facility for determining at any given point in the Central Processing Unit program precisely which control word or Input-Output Output command is currently in process in the Data Synchronizer Channel and further by examining the address part of the current control word may determine how many data words have actually been transmitted. If too large a number of these commands are given and use up the available B cycles between the data words, a disconnect occurs. This provides a means by which the Data Synchronizer Channel and the Tape Control Unit or Input-Output Channel may be programmed to disconnect by default. That is to say that the deliberate introduction of a transfer type of control word having an address part which specifies the actual address in Core Storage of this instruction results in an endless loop of references to the same instruction with the result that a deliberate disconnect may be effected.

With regard to testable Indicators, in the Data Synchronizer Channel, the purpose of providing an End of Tape Indicator is to give the programmer the facility for testing periodically or at will when writing on tape to determine the optimum time to cease writing on that particular reel of tape in order to avoid running off the end of the tape. The facility has been provided for the programmer to avoid this possibility if he so desires or if he considers the quantity of data to be transferred when writing on to the tape may approach the full reel. The purpose in providing a Beginning of Tape Indicator is similar except that in this case we are concerned with Backspacing and Backspace File instructions where we may have an endless loop of Backspace to simulate for instance a Read Backwards on Tape. At the end of each portion of loop, the the programmer is provided through this indicator with a corresponding instruction, allowing it to be determined when the Beginning of Tape has been reached and that further Backspaces or Backspace File Instructions are redundant. An End of File Indicator is provided and a corresponding instruction for the purpose of determining when the End of File has been reached while reading. An End of File while reading is always an unconditioned disconnect, or always results in unconditional disconnect of the Input-Output Unit, its control unit, and the Data Synchronizer Channel to which it is connected. Therefore, it is necessary many times when reading to avoid issuance by the Central Processing Unit and the Stored Program of a further instruction unit it has definitely been ascertained that a complete file has been read. This is purely an optional programming method provided for the programming and he may instead proceed by giving additional Read Select instructions and ignoring End of File indications. For the purpose of counting files or for the purpose of determining which of N files is to be read, the facility of an End of File Indicator and corresponding instruction has been provided.

DEFINITIONS OF SYMBOLS

$A^{I\ MEG}$, A_C, A, AND are AND circuits; A_S is a Slow Amplifier; −AND and −A are OR circuits; A_D is a Drum Amplifier; A_{CS} is a Sense Amplifier; and ATA is a Read Preamplifier.

CF is a cathode follower; CF (infinite), CF^R_{OR}, CF_{OR} (infinite), CF_{OR} are cathode follower OR circuits; CF_T is a tapped cathode follower; CF_{ER} is a cathode follower used for the electronic reset of triggers; CF_M, CF_{OR} (R) are cathode follower OR circuits having the cathode clamped so as not to go below ground; CF_T is a cathode follower with tapped load for reduced output; CG_M is a Clamp Generator; and CPA is a Clamp Power Amplifier.

D is a Microsecond Delay Unit, DG is a Diode Gate; DL is a Delay Line, DPQ is a Digit Plane Amplifier; DPD is a Digit Plane Driver; and DL_H is Delay Line. GA and GAF are Grounded Grid Amplifiers.

K and K_{PP} and Cathode Followers, K_{RA} and KR_A are Reset Cathode Followers; K_O is a Power Cathode Follower OR; K_C is Power Cathode Follower with very small load resistor suitable for low duty cycle use: K_O is Cathode Follower OR; K_J is a Power Cathode Follower; and K_{JO} is a Power Cathode Follower OR.

MV is a Multivibrator; MSAW is a Matrix Switch Amplifier, Write; MSAR is a Matrix Switch Amplifier, Read; and MSD is a Matrix Switch Driver.

normal Read Tape operations occur with the exception that the contents of the Tape Shift Register are not transferred to Data Register A in this instance since in FIG. 214 the Tape Read Gate Channel A line 194a.02 is down.

PRIORITY SYSTEM FOR SIX DSU's

There is no fixed sequence of scanning or commutation among the six channels forcing a particular channel to wait its turn. When a channel requires service to Core Storage, it does not have to wait until its turn comes up necessarily. If no other channels are demanding, it gains immediate access to Core Storage. The priority system is essentially a pyramid of triggers or flip-flops which operate in this fashion. Suppose that all six channels demand access to Core Storage at the same time. When a situation of this type occurs, the status of the priority system allows one, and only one, channel at all times to be positively connected to Core Storage. When all six channels are demanding at the same time, the logic is such that the existing status of the priority system may not be changed, therefore, whatever position the priority system happens to be in, it specifies which channel will first be served. The operation of the Data Synchronizer *priority* system will now be described.

Reference is made to the logical diagrams of FIGS. **204, 206, 208** and **209.**

There are several levels of priority within each DSU. One level of priority determines which of the two DS channels will be served. If both channels are simultaneously demanding service, then the previous history, that is to say, the channel which previously was served relative to the other channel in the same DSU, is the first to be served within the DSU (FIG. **204**). Simply stated, whenever two simultaneous demands occur within a given Data Synchronizer unit no change in status of priority occurs, but since the priority trigger within the DSU has either one status or the other the fact that no change in status occurs immediately indicates that whatever status the priority trigger was in previously (FIG. **204**), is the status it remains in and this determines which of the two channels will first be served. Another level of priority in a three DSU system or a six DSC system is to determine which DSU will be served (FIG. **206**). In each DSU oe trigger settable to one or the other of two states determines whether the associated DSU or an unspecified one of the other two DSUs will be served. The particular DSU of the other two served depends upon which DSU triggers are set. Once again, if a channel in the previously served DSU is demanding service simultaneously with a channel or channels in the other DSUs, then no change in status of this priority trigger will occur. The DSU which was previously served is the first in order of service under the current demand. If channels in the other DSUs demand service and the previously served DSU does not demand service, then the DSU most remote from the Central Processing Unit (CPU) receives priority. In summary, priority of service is random, not fixed, the order in which different DSCs are served varying according to the following rules:

1. Between DSCs in a single DSU, the last DSC to be served is given first priority.

2. Among DSUs, if the last DSU to be served demands additional service, the last DSU to be served is given first priority.

3. Among DSUs, if the last DSU to be served does not demand additional service, the DSU demanding service and most remote from the CPU is given first priority.

Therefore, at any one time a given DSC may have first priority or it may not, depending upon which previous DSC requests were honored. This priority system tends to favor the DSC connected to the fastest I/O unit since a fast data rate results in repeated demands on previously served DSCs (Rules **1** and **2**).

Assume that six tapes are reading, that there is a 288 microsecond word period, that there is an indirectly addressed Control Word for every data word, and that DSC No. **2** of DSU No. **1** was last served. All DSCs of all DSUs simultaneously demand service. DSU No. **1** is selected since it was the last DSU served. Channel 2 is the first served since it had a previous history of being served. Once DSC No. **2** is served DSU No. 1 is reselected and if DSC No. **2** no longer demands service, DSC No. **1** is next served. DSU No. **1** and DSC No. **2** will be reselected repeatedly until DSC No. **2** no longer demands service. The next order of service must be DSU No. **3** since it is the DSU most remote from the CPU. The last channel in DSU No. **3** served was DSC No. **5**, so that Channel 6 cannot be serviced until Channel 5 has been served. Therefore, DSC No. **5** will be repeatedly served until it no longer demands service, at which time DSC No. **6** will be served. Once DSU No. **3** has been completely served, control transfers to DSU No. **2**, even if DSU No. **1** again demands service, because DSU No. **2** is the most remote DSU demanding service. If DSC No. **4** of DSU No. **2** was the last channel in DSU No. **2** serviced, it will have first priority when DSU No. **2** is selected. When the service request of DSC No. **4** has been satisfied DSC No. **3** is finally given priority.

In summary, the simultaneous requests have been satisfied in the following order: DSC No. **2**, DSC No. **1**, DSC No. **5**, DSC No. **6**, DSC No. **4** and DSC No. **8.** The priority order is dependent upon the prior service requests satisfied as specified above. The priority is different if any of those conditions are changed. Thus, the priority is random.

GENERAL

With regard to Data Synchronizer Channel operation making use of the Transfer Command, the Transfer Command has an operation part of bit position number **2** ON and all other bit positions OFF in the operation part. The Word Count portion of the Command is ignored. The Address part of the Command specifies the location in Core Storage not where data is to come from, but instead, where the next Input-Output or Data Synchronizer channel command is to come from. The operation part in this case indicates that this Control Word or command is a transfer and that an immediate reference within the following machine cycle is made by this channel to Core Storage at the location specified by the address part of the Transfer Command. In order to bring into the Data Synchronizer Channel a new Data Synchronizer Channel Command from Core Storage, the procedure is as follows: Assume that the Data Synchronizer Channel has made a demand for a new control word from the Core Storage. The Data Synchronizer Channel in the normal way makes its demands and receives access to Core Storage through the priority system. A new control word is loaded into the

O, $O_{1\ meg}$ and OR are OR circuits; O_C is a Cascaded OR circuit; —OR is an AND; and)SC is a Master Oscillator. R is a Relay Driver (essentially an inverted with a relay coil as a plate load).

SS_F is a Single Slot (fast recovery); ST is a Switch Timer; SS_E is a Single Shot (fast recovery); SS_H is a Single Shot (holdover): SS_D is a Single Shot (short duration); SR is a Switch Reed; SG is a Sync Generator; SC is a Sync Clipper; and SPA is a Sync Power Amplifier.

T is a High Speed Trigger; $T_{W\cdot R}$ is a Write Trigger; T_{KX} is a Key Trigger with reset (X denotes reset); T_K is a Key Trigger; T_T, T_U, T_V, T_W, T_Y, T_{XA} and T_{XB} are Triggers where the subscripts denote different resets; TH is a Thyratron; T_A is a Trigger with particular output dividers; T_S is a Slow Trigger; T_{AXA}, T_{AXB}, T_{AZ}, T_{AW}, T_W, and T_C are Slow Triggers having various output dividers; T_{KA} is a Key Trigger; and T_B is a Schmitt Trigger.

WD is a Write Driver, ${}_xT_{KA}$ and ${}_xT$ are Key Triggers reset off; ${}_xT_D$ is a Key Trigger with a large crossover capacitance; and XTAL is a crystal.

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While there have been shown and described and pointed out the fundamental novel features of the invention as applied to a preferred embodiment, it will be understood that various omissions and substitutions and changes in the form and details of the device illustrated and in its operation may be made by those skilled in the art without departing from the spirit of the invention. It is the intention therefore, to be limited only as indicated by the scope of the following claims.

What is claimed is:

1. A data processing system operable by main instructions comprising, in combination, a storage device for providing a series of said main instructions and control instructions, a plurality of input-output devices independently operable in response to said control instructions, and multi-channel apparatus including a control device for each of said channels in tandem relationship with said storage device and said input-output devices, each of said channels having means to store a plurality of control instructions to be executed consecutively concerning input-output operation, and means for serially moving said control instructions through said channels upon execution of any one operation of said input-output device.

2. A data processing system comprising, in combination, a primary calculator, a plurality of control devices, each including secondary calculating apparatus units for the interpretation of main and control instructions, a shared storage device providing a common information source of data and data handling commands between said plurality of control devices and said primary calculator and the means for communicating said data and data handling commands, and means actuated in response to stimuli from said primary calculator to said storage device to provide initial main instructions to said control devices concerning the type of operation to be performed and the location in the shared storage device from which subsequent control instructions are extracted automatically by the control devices in response to operation of said secondary calculating apparatus.

3. A data processing system comprising, in combination, a device for serially providing address manifestations, an addressable storage device for the storage and transmission of data serially by word in response to said address manifestations, a plurality of input-output devices for receiving and transmitting said data, a plurality of control devices each independently operable in accordance with a separate program directly coupling said input-output devices and said storage device and each adaptable to store and to receive address manifestations and to transmit data, from and to corresponding locations of said storage device in a synchronous manner and to transmit information from and to said input-output devices in an asynchronous manner said control devices adapted to distribute signals representative of words of data serially to and from said storage device and adapted to transmit data signals in parallel, as among said input-output devices, to and from said input-output devices.

4. In a data handling system, apparatus comprising a plurality of selectively operable auxiliary storage devices adapted to receive and store information units in response to read and write signals, a shared storage device adapted to receive and store information units in response to read-in and read-out signals, and bilateral data transmission devices coupling said auxiliary storage devices and said shared storage device and operable in response to predetermined individual programs of control words for providing read and write signals serially to said shared storage device and for providing said read and write signals to said selectively operable auxiliary storage devices according to said predetermined programs.

5. In a data processing unit in combination with a primary storage device having individual information storage locations for receiving and transmitting information in response to read and write signals and a plurality of secondary storage devices individually operable to receive and transmit information in response to said read and write signals, data handling apparatus comprising at least two information transporting channels, each channel having execution means for controlling the passage of information between said primary storage device and said secondary storage devices by providing read and write signals thereto in response to a predetermined program stored therein, and means responsive to said execution means and said read and write signals for arranging and transmitting information in sequential order to said primary storage device so that said information is delivered to destinations determined by said programs in said data handling apparatus.

6. In a data processing system including a shared storage device, a plurality of input-output devices, and means for controlling the passage of information in a plurality of information channels therebetween, a device for establishing priority among said channels comprising a plurality of bistable devices, one for each pair of said channels, means combining indications of the state of said bistable devices, means controlling the state of said bistable devices in response to passage of information through said channels, and means operable in response to combined indications of said bistable devices for establishing priority among said channels.

7. A data processing system adapted to execute a load channel operation in response to an instruction having an operations part and an address part comprising a storage device, an instruction register including means for interpreting instructions and directing corresponding operations, means for storing a program of instructions in said storage device at addresses selectable in a predetermined manner and for reading said stored instructions, a plurality of input-output devices selectable by instruction signals for storing and transmitting data, multi-channel control apparatus adapted to buffer information between said input-output devices and said storage device including operations, address and location registers respectively in each channel and means furnishing signals indicative of said stored information therein, means selecting said input-output devices and said channels of said control apparatus, means reading and transferring said load channel instruction to said instruction register, means operable in response to said instruction register for entering the address part of said load channel instruction plus a predetermined value in said location register of a selected channel and for entering the information from the location specified by said address contained in said load channel instruction in said operations and address registers in said selected channel.

8. A data processing system adapted to execute an input-output control operation in response to an instruction having an operations part, a count, and an ad-

dress, said system comprising a storage device, an instruction register including means for interpreting instructions and directing corresponding operations, means for storing a program of instructions in said storage device at addresses selectable in a predetermined manner and for reading said stored instructions, a plurality of input-output devices selectable by instruction signals for storing and transmitting data, multi-channel control apparatus adapted to buffer information between said input-output devices and said storage device including means storing operation manifestations, said count, and said addresses of locations in said storage device in each channel and for furnishing signals indicative of said stored information, means selecting said input-output devices and said channels of said control apparatus, means reading and transferring an input-output control instruction from said storage device to a selected channel of said control apparatus, means operable in response to operation manifestations in said operation manifestation means to program the transfer of data in said channel, means operable in response to said count stored in said count storing means to control the quantity of data, and means operable in response to said addresses stored in said address storing means to select the data locations in said storage device.

9. In a data processing system adapted to execute a load channel operation in response to an instruction having an operations part and an address, said system comprising a storage device and an instruction register including means for interpreting instructions and directing corresponding operation, means for storing a program of instructions in said storage device at addresses selectable in a predetermined manner and for reading said stored instructions, a plurality of input-output devices selectable by instruction signals for storing and transmitting data, multi-channel control apparatus adapted to buffer information between said input-output devices and said storage device including means storing operation manifestations and addresses of locations in said storage device in each channel and for furnishing signals indicative of said stored information, means selecting said input-output devices and said channels of said control apparatus, means reading and transferring a load channel instruction from said storage device to said instruction register, means transferring a control instruction at the address specified by said load channel instruction to the selected channel of said control apparatus, means under control of said operation manifestations storing means, operable in response to operation manifestations in said control instruction to program the transfer of data in said channel, means under control of said storing addresses of locations, operable in response to said address in said control instruction to select data locations in said storage device, and means delaying the execution of a second of said load channel instructions when provided until the operation specified by said control instruction is complete.

10. A data processing system comprising a storage device, an instruction register including means for interpreting instructions and directing corresponding operations, means for storing a program of instructions in said storage device at addresses selectable in a predetermined manner and for reading out said stored instructions, a plurality of input-output devices selectable by instruction signals for storing and transmitting data, multi-channel control apparatus adapted to buffer information and to transfer said information between said input-output devices and said storage device and adapted to execute a control instruction having an operation part, a count, and an address including means storing manifestations of said operation, said count, and said addresses in each channel and for furnishing signals indicative of said stored control information, means selecting said input-output devices and said channels of said control apparatus, means reading and transferring said control instruction from said storage device to a selected channel of said control apparatus, and execution means for each channel operable in response to manifestations of said operation part in said operation storing means to control the transfer of data in said channel, operable in response to manifestations of said count to control the quantity of data transferred, and means operable in response to manifestations of said address in said address storing means to select the data locations in said storage device.

11. A data processing system adapted to execute a synchronous load channel operation in response to an instruction having an operations part and an address part comprising a storage device, an instruction register including means for interpreting instructions and directing corresponding operations, means for storing a program of instructions in said storage device at addresses selectable in a predetermined manner and for reading out said stored instructions, a plurality of input-output devices selectable by instruction signals for storing and transmitting data, multi-channel control apparatus adapted to buffer information between said input-output devices and said storage device and controlled by buffer instructions having operations and address parts stored in operations and, address registers respectively in each channel, means furnishing signals indicative of said stored information therein and ready signals when an operation is complete, means selecting said input-output devices and said channels of said control apparatus, means reading out and transferring said synchronous load channel instruction to said instruction register, and synchronizing means operable in response to said instruction register and said ready signal from said selected channel for entering the buffer instructions from said address in said storage device into said operations and address registers in said selected channel.

12. A data processing system comprising, in combination, an addressable storage device, a primary computer having access to said storage device for instructions and data, a plurality of input-output devices, a plurality of secondary stored program computers and data transmission devices for receiving and transferring data from and to said input-output devices having access to said storage device for receiving instructions and data and for storing data from said input-otuput devices in accordance with said stored programs and means for establishing priority in response to demands for access to said storage device among said primary computer and said plurality of secondary computers, said priority means favoring previous demands and all demands being satisfied in a predetermined period of time.

13. A data processing system comprising, in combination, a computer, an addressable storage device storing data, channel instructions and further instructions including select and control instructions, a plurality of input-output devices, a plurality of control devices hav-

ing channels coupling said input-output devices to said addressable storage device, means for interpreting said select instructions to render one channel operative to select a chosen input-output device, means interpreting said channel instructions to obtain a control instruction, means controlled by said control instruction for controlling the transfer of data via said selected channel, means controlled by said channel instruction for storing in said selected channel the manifestation of the address of a next control instruction located in said storage means, and means rendered operative upon completion of said transfer of data to render said manifestation of the addresses of a next control instruction effective to select and render operative said next control instruction.

14. A device as in claim **13**, and means for establishing priority of access to said storage device between said computer and said channels, and means controlled by the selected channel operation to grant priority of access to said channel instead of to said computer.

15. A device as in claim **13**, and including means for establishing priority of access to said storage device, among said channels, means conditioned by operation of a chosen channel, and means controlled by said conditioned means rendering said priority means operative to grant access to said chosen channel, in preference to another channel.

16. In combination, a central processing unit controlled by instruction manifestations and operable upon data manifestations, addressable storage means storing manifestations of data, of instructions and of commands, a plurality of input-output devices for receiving and supplying manifestations of data, a plurality of channels for controlling the flow of data manifestations between said storage means and said input-output devices and including means for storing operation control manifestations, and address manifestations of one kind and of another kind, said commands including operation control manifestations and address manifestations designating addresses of data storage locations in said storage means, and said instruction manifestations including address manifestations designating addresses of commands, means controlled by said central processing unit for extracting a manifestation of instruction from said storage means, for selecting a channel and an input-output device, means controlled by said central processing unit for extracting a manifestation of an instruction for initiating operation of said chosen channel, means controlled by an address portion of said last named manifestation for storing manifestations in accordance with said address portion in said address manifestation storing means of one kind, and for selecting a command at the designated address in said addressable storage means and relaying said command to said operation control manifestation storage means, and to said address manifestation storage means of said other kind whereby operation of said selected channel is controlled by said operation manifestation storage means to transfer data to or from said selected input-output unit, and from or to said data address respectively, the addresses of data in said storage means being indicated by said address manifestations of said other kind, and means controlled by said address manifestations of said one kind for selecting a command in said storage means, to control further data transfer.

17. A device, as in claim **16**, and including means in each channel for storing data quantity manifestations, and said commands including a data quantity manifestation, and means controlled by the address portion of said last named manifestation, relaying said data quantity manifestation to said data quantity manifestation storing means, means operating upon said data quantity manifestation to keep track of the amount of data transferred by altering said manifestation to different statuses and means rendered operative by a certain status to render said means, controlled by said address manifestation of said one kind, effective for selecting another command.

18. A device, as in claim **16**, and including means establishing a priority of access to said storage means between said central processing unit and said channels, and means controlling said priority access means to give priority of access to a channel, upon simultaneous demands for access by said central processing unit and said channels.

19. A device, as in claim **16**, and including means establishing priority of access to said storage means between two channels, means controlled by operation of said channels to indicate a present state of operation or of non-operation, respectively, of said two channels, and means controlled by said last indicating means for rendering said priority means effective to grant access to said channel indicating a present state of operation.

20. A device, as in claim **16**, and including means establishing priority of access to said storage means among a plurality of channels simultaneously requesting access, means conditioned selectively by operation of one channel to establish a claim of priority, and means controlled by first and second, associated units in said one channel, for controlling said conditioned means whereby priority among said channels simultaneously requesting access in given to said second associated unit in said one channel, if said first associated unit was immediately previously operative, but no longer requesting access to said storage means.

21. In combination, a computer, a plurality of input-output devices and a shared addressable storage unit, said unit storing manifestations of data, instructions and commands, each of said instructions including an operation part and an address part and each of said commands including a word count part, an operation designating part and an address part, a plurality of channels connecting said input-output devices and said shared storage unit and each including a data register for receiving data manifestations from said input-output devices to be relayed to said storage unit or data manifestations from said storage unit to be relayed to said input-output units, a location register in each said channel for storing manifestations of said instruction address part, a word counter in each said channel for storing manifestations of said command word count part, an address counter in each said channel for storing manifestation of said command address part, an operation register in each channel for storing said command operations part, means controlled by an instruction for selecting a channel and selecting an input-output device, means controlled by an address part of an instruction for storing said address part in said location counter, and for selecting a command in said storage unit, means controlled by said last named instruction operation part for transferring said word count part of said selected command to said word address counter, said word address part of said selected com-

mand to said word address counter and said operation part of said selected command to said operation register, means for stepping said word counter down and said address counter up, said operation part stored in said operation register, controlling the flow of data to said data register, said flow controlling said word counter, said word address counter designating the storage location of data in said storage unit, and means controlled by said word counter, upon termination of said data transfer, to request access to said storage unit, said address stored in said location register selecting the address of the next command stored in said storage unit.

22. A device, as in claim **21**, and including means demanding access to said storage means by said computer and said selected channel and means recognizing both said demands for access, said means granting priority to said channel demand upon simultaneous demand by said computer and said channel.

23. A devive, as in claim **21**, and including means recognizing demands for access by a plurality of channels, and means granting priority to said first selected channel, upon a demand emanating from said channel and another channel.

24. Apparatus for providing service in turn to the individual ones of a plurality of devices arranged into a number of groups, each device operable to request service, means establishing service to an individual device, including: means for recognizing which devices request service and which ones have previously been provided service; means for providing priority of service, as among groups of said devices requesting simultaneous service, to the group having the device being presently serviced; and means for providing priority of service, as among devices requesting service in a group, to the device previously serviced.

25. Apparatus for indicating priority of service among a plurality of input line groups carrying signals representative of service requests, including: a number of bi-stable flip-flops, each settable to a selected one of a first and a second state, and each associated with a different group of said input lines; means operative to permit setting to said first state of selected ones of said flip-flops by service signals on any input line in selected ones of said groups; means operative to permit setting to said second state of selected ones of said flip-flops by service signals on any input line in selected ones of said groups associated with selected others of said flip-flops; means operative to maintain the state of any of said flip-flops when service signals attempt to set said flip-flop to said first and second states substantially simultaneously; gating means associated with each flip-flop responsive to the state of a number of others of said flip-flops; and group-priority indicating output means associated with each flip-flop responsive to said associated gating means and operative by the first state of said associated flip-flop.

26. A device as in claim **25** wherein said gating means is responsive to the first state of said associated flip-flops and to the second state of said other flip-flops.

27. A device as in claim **25** wherein each of said group-priority indicating output means is associated with: a number of line-priority indicating output means corresponding to the number of input lines comprising a group, a selected one of said line-priority means corresponding to the input line carrying a service request being operable when said associated group-priority means is operative.

28. In an electronic data processing apparatus, the combination comprising a plurality of data utilization devices, each of said devices having a separate demand line to indicate when active the readiness of said device to manipulate data, a control means comprising means for addressing a data storage location for data to be manipulated, an addressable data storage means adapted to have data read therefrom or written thereinto in accordance with addresses derived fon said control means, and a traffic control circuit separately connected to each demand line of said utilization devices and said control means to substantially immediately scan all demand lines connected thereto, bypassing all demand lines which are inactive without response therefrom, until an active demand line is sensed and passing separate control signals to said control means for each active demand line sensed.

29. In combination, a plurality of data manipulating devices, a multiple stage traffic control circuit, a data processor, means including said traffic control circuit repetitively scanning all of said devices and connecting each of said data manipulating devices requiring a data manipulation in sequence to said data processor to perform a single data manipulation, an error signal producing circuit, and electronic switching means under control of said error signal producing circuit connected to said traffic control circuit to interrupt said traffic control circuit in at least one stage upon the occurrence of an error in a data manipulation.

30. In combination, a plurality of data manipulating devices, a multiple stage traffic control circuit, a data processor connected to one stage of said traffic control circuit to be activated thereby, means including said traffic control circuit repetitively scanning all of said devices and connecting each of said data manipulating devices requiring a data manipulation in sequence to said data processor to perform a single data manipulation, an error signal producing circuit, an electronic switching means under control of said error signal producing circuit connected to said traffic control circuit to interrupt said traffic control circuit in at least one stage upon the occurrence of an error in a data manipulation.

31. A data manipulating apparatus comprising data supply means having a plurality of data items therein each arranged as a plurality of data words, and an end-of-item indicator separating the respective items, a memory unit having a plurality of separately addressable storage locations to which all of said data is to be transferred, a memory address selector, control means adapted to store address data defining an address in said memory unit, means including said control means activated by each incoming data word to transfer directly the data word unmodified to an address location specified by said address data from said control means, means including said control means modifying the address defining data each time said address data is used, an end-of-item indicator sensing means, and means including said end-of-item sensing means connected to effect modification of the address data in said control means.

32. A data manipulating apparatus comprising data supply means having a plurality of data items therein each arranged as a plurality of data words, and an end-of-item indicator separating the respective items, a

memory unit having a plurality of separately addressable storage locations to which all of said data is to be transferred, a memory address selector, control means adapted to store address data defining an address in said memory unit, means including said control means activated by each incoming data word to transfer directly the data word unmodified to an address location specified by said address data from said control means, means including said control means modifying the address defining data each time said address data is used, an end-of-item indicator sensing means, and means including said end-of-item sensing means connected to effect modification of the address data in said control means, said last-named means comprising memory output sensing means connected to said memory address selector and to said control means.

33. A data manipulating apparatus comprising data supply means having a plurality of data items therein each arranged as a plurality of data words, and an end-of-item indicator separating the respective items, a memory unit having a plurality of separately addressable storage locations to which all of said data is to be transferred, a memory address selector, control means adapted to store address data defining an address in said memory unit, means including said control means activated by each incoming data word to transfer directly the data word unmodified to an address location specified by said address data from said control means, means including said control means modifying the address defining data each time said address data is used, an end-of-item indicator sensing means, and means including said end-of-item sensing means connected to effect modification of the address data in said control means, said last-named means comprising memory output sensing means connected to said memory address selector and to said control means, said control means modifying the data received from said memory output sensing means.

34. Apparatus for arranging a plurality of data words in an addressable main memory comprising a control memory having a plurality of addressable storage positions, a control memory address selector, means connected to said control memory address selector to set a predetermined address therein indicative of an incoming word, a main memory address selector, means including said control memory address selector reading an address for said main memory from said predetermined address in said control memory into said main memory address selector to select a location in said main memory for said incoming word, and means connected to said control memory to modify the main memory address from said predetermined address in said control memory and reinsert said modified main memory address at said predetermined address in said control memory.

35. Apparatus for transferring a plurality of data words relative to an addressable main memory comprising a control memory having a plurality of addressable storage positions, a control memory address selector, means connected to said control memory address selector to set a predetermined address therein indicative of the need for a data word to be transferred, a main memory address selector, means including said control memory address selector reading an address for said main memory from said control memory into said main memory address selector to select a location for said data word which is to be transferred, and means connected to said control memory to modify the main memory address from said predetermined address in said control memory and reinsert said modified main memory address at said predetermined address in said control memory.

36. Apparatus for transferring a plurality of data words relative to an addressable main memory comprising a control memory having a plurality of addressable storage positions, a control memory address selector, means connected to said control memory address selector to set a predetermined address therein indicative of the need of a word to be transferred, a main memory address selector, means including said control memory address selector reading an address for said main memory from said control memory into said main memory address selector to select a location for said word which is to be transferred, means connected to said control memory to modify the main memory address from said control memory and reinsert said modified main memory address at said predetermined address in said control memory, and means connected to said control memory to effect a transfer from said main memory of substitute control data for insertion in said predetermined address in said control memory.

37. In a data processing apparatus, the combination comprising a main memory, said memory being adapted to store data words each at a separately addressable location, a main memory address selector for selecting the address for each data word in said main memory, a control memory having a plurality of addressable storage locations, said control memory being adapted to store control data for said main memory, a control memory address selector, a data transfer circuit, indicating means connected to said last-named circuit to indicate said transfer circuit is conditioned to transfer a data word, means including said indicating means setting an address in said control memory address selector, control memory activating means connected to said control memory to read control data therefrom at a selected address location into said main memory address selector, means including said main memory address selector effecting a direct transfer of data without modification between said transfer circuit and said main memory, and means connected to said control memory to modify the control data read into said main memory address selector.

38. Apparatus for arranging a plurality of data words in an addressable main memory comprising a control memory having addressable storage locations, a control memory address selector, means connected to said control memory address selector to set a first predetermined address therein indicative of a word to be transferred, a main memory address selector, means including said control memory address selector reading an address from said control memory into said main memory address selector to select a location in said main memory for said incoming word, means connected to said control memory to modify the main memory address from said control memory and reinsert said modified main memory address at said predetermined address, word sensing means connected to said main memory to sense the contents of each word transferred, said word sensing means being connected to said control memory address selector to set a second predetermined address therein so that a special address in said main memory will be selected and data at said special

address will be inserted into said first predetermined address in said control memory.

39. In a data processing apparatus, the combination comprising a main memory, said memory being adapted to store data words at separately addressable storage locations, a main memory address selector for selecting the address for each data word in said main memory, a control memory having a plurality of addressable storage locations, said control memory being adapted to store control data for said main memory, a control memory address selector, a data transfer circuit, indicating means connected to said last-named circuit to indicate said transfer circuit is conditioned to transfer a data word, means including said indicating means setting a first address in said control memory address selector, control memory activating means connected to said control memory to read control data therefrom into said main memory address selector, means including said main memory address selector effecting a transfer of data between said transfer circuit and said main memory, means connected to aid control memory to modify the control data read into said main memory address selector, selective data sensing means connected to said data transfer circuit, means connecting said data sensing means to said control memory address selector to set a second address therein, and means including said data sensing means effecting a change of the data in said control memory at said first address.

40. Apparatus for arranging a plurality of data words in an addressable main memory comprising a control memory having a plurality of addressable storage locations, a control memory address selector, means connected to said control memory address selector to set a predetermined address therein indicative of a word to be transferred, a main memory address selector, means including said control memory address selector reading a first address from said control memory into said main memory address selector to select a location for said incoming word, and means connected to said control memory to modify by unity the main memory address from said control memory and reinsert said modified main memory address at said predetermined address in said control memory.

41. In a data processing apparatus, the combination comprising a plurality of data utilization devices, each of said devices being adapted to receive and transmit data, a programmed data processor, a traffic control circuit, demand indicating lines connected from each of said utilization devices to said traffic control circuit, electronic switching means connected to said traffic control circuit to scan substantially immediately all of the demand lines until an active demand line is sensed. said switching means being adapted to lock directly onto only those demand lines in a selected sequence which are active and bypassing without response therefrom those demand lines which are inactive, data storage means, and control means comprising data selecting means connected to be controlled by each utilization device whose demand line is active, said control means being connected to effect a data transfer with respect to said data storage means in accordance with the device in demand.

42. In combination, in a data processing apparatus, a first data manipulation traffic control adapted to scan a plurality of operation demand lines and initiate a control signal and thereby a data manipulation only with respect to each active demand line which is calling for operation, a second data manipulation traffic control adapted to scan a plurality of operation active demand lines and initiate a control signal and thereby a data manipulation only with respect to each active demand line which is calling for operation, a data processor connector to receive control signals from said first and second traffic controls to initiate a control action in said data processor related to a selection made by said second traffic control.

43. In combination, in a data processing apparatus, a first data manipulation traffic control adapted to scan a plurality of operation demand lines and initiate a control signal and thereby a data manipulation only with respect to each active demand line which is calling for operation, a second data manipulation traffic control adapted to scan a plurality of operation demand lines and initiate a control signal and thereby a data manipulation only with respect to each active demand line which is calling for operation, a data processor connector to receive control signals from said first and second traffic controls to initiate a control action in said data processor related to a selection made by said second traffic control, and means to step said second traffic control after a predetermined operation of said data processor when under the control of said second traffic control.

44. In combination, in a data processing apparatus, a first data manipulation traffic control adapted to scan a plurality of operation demand lines and initiate a control signal and thereby a data manipulation only with respect to each active demand line which is calling for operation, a second data manipulation traffic control adapted to sense a plurality of operation demand lines and initiate a control signal and thereby a data manipulation only with respect to each active demand line which is calling for operation, a data processor connected to receive transfer control signals from said first traffic control and data manipulation program orders from said second traffic control to initiate a control action in said data processor related to a selection made by said second traffic control.

45. In combination with a data processor, a plurality of peripheral data handling devices said devices each being adapted to have an output operational demand signal which is active when said device is ready to operate, an operational traffic control having a plurality of control stations, each station of which is connected to one each of said peripheral devices to sense only the active operational demand signals produced by said devices and to bypass without response therefrom those devices having no operational demand signal, a traffic control signal source comprising an electronic switching means connected to said traffic control to step said traffic control from one active demand signal to the next so that each device receives at least one operational control impulse for a predetermined data manipulation after which the traffic control steps substantially immediately to the next active demand signal, and a control circuit connected to be controlled by the output from said traffic control.

46. In combination with a data processor, a plurality of peripheral data handling devices each of said devices having an input buffer and an output buffer, and the buffers of said devices each being adapted to have an output operational demand signal which is active when the associated buffer is ready to operate, an operational

traffic control having a plurality of control stations each independently connected to one each of said buffers to sense active operational demand signals produced by said buffers and to bypass without response therefrom any buffer not having an active operational demand signal, a traffic control signal source connected to said traffic control to step said traffic control from one active operational demand signal to the next so that each buffer receives at least one operational control impulse for a predetermined data manipulation after which the traffic control steps substantially immediately to the next active demand line, and a control circuit connected to be controlled by the output from said traffic control.

47. In a data processing apparatus, the combination comprising a plurality of data utilization devices, each of said devices being adapted to receive and transmit data, a programmed data processor, a traffic control circuit, demand indicating lines connected from each of said utilization devices to said traffic control circuit, electronic switching means connected to said traffic control circuit to scan substantially immediately all of the demand lines, bypassing without response therefrom the inactive demand lines, until an active demand line is sensed, data storage means, control means comprising data selecting means connected to be controlled by each utilization device whose demand line is active, said control means being connected to effect a data transfer with respect to said data storage means in accordance with the device in demand, and clock means producing a traffic control signal connected to said signal means to switch said traffic control circuit from one active demand indicating line to the next active demand indicating line.

48. An on-line data processing system for processing call requests from keysets and the like comprising

a central processing portion, said central processing portion including a computer means and means for receiving said call requests,

a plurality of peripheral units, each of said peripheral units including information storage means and control register means,

said central processing portion also including means responsive to a received call request for directing to said control register means data for controlling the transfer of information between said information storage means and said central processing portion,

and transfer means for each of said peripheral units, said transfer means being controlled by said control data to carry out the transfer of information between the corresponding one of said peripheral units and said central processing portion.

49. A data processing system as set forth in claim **48**, including means at said peripheral units to develop a BID signal indicating that the corresponding peripheral unit is conditioned for a transfer of information,

and means at said central processing portion responsive to said BID signal for inhibiting the operation of said computer means to permit said transfer to take place.

50. A data processing system as set forth in claim **49** further including priority selector means for enabling a predetermined one of said transfer means in accordance with a predetermined priority schedule.

51. In an on-line data processing system for processing call requests comprising

a central processor portion including data storage means,

computer means operable upon data stored in said data storage means,

and means for receiving said call requests and for directing corresponding data signals to said data storage means to be operated on by said computer means;

a plurality of peripheral units for storing inventory information to be processed in accordance with said call requests

each of said peripheral units including control register means,

said computer means being operative in accordance with said call requests to load instructional data in a selected one of said control register means,

said peripheral units further including transfer means responsive to said control register means in accordance with said instructional data for identifying particular inventory information and for effecting a transfer thereof between said data storage means and said inventory storage means.

52. A data processing system as set forth in claim **51** wherein said transfer means further includes synchronizing register means for temporarily storing said identified information.

53. In an on-line data processing system,

a central processor portion,

a plurality of periheral units each including inventory storage means and control register means,

said central processor portion including a computer section and data storage means operable with said computer section,

a plurality of keysets for initiating call requests and for directing said call requests to said central processor portion,

means included at said central processor portion for receiving said call requests and for transmitting transfer instructional data to a selected one of said control register means corresponding to identifying signals contained in the call request,

said control register means including means for addressing said data storage means and said inventory storage means and means for establishing the operational state of said peripheral unit,

and synchronizing register means for receiving digits of inventory information to be transferred between a selected peripheral unit and said data storage means.

54. Data processing system as set forth in claim **53**, including signal means at each peripheral unit for generating a BID signal when that peripheral unit is conditioned to effect a transfer of inventory information,

priority selector means responsive to said BID signals so generated for developing an ALLOW signal individual to one of said peripheral units according to a preset priority schedule,

and means at said peripheral units responsive to the ALLOW signal to carry out the selected data transfer.

55. A data processing system as set forth in claim **54**, including

inhibiting means at said central processor, said inhibiting means being responsive to a BID signal and operative thereby to prevent further operations of said computer section until the data transfer has been effected.

56. An on-line data processing system comprising
a central processor portion and a plurality of peripheral units arranged for operation with said central processor portion,
said central processor portion including data storage means and program control means having a plurality of preset programs,
means for directing call requests to said central processor portion on a random basis,
said central processor portion including means for receiving said call requests on a one-at-a-time basis,
control register means at said peripheral units arranged to receive instructional data defining a particular data transfer operation between the peripheral unit and said data storage means,
said central processor portion including means responsive to signals of a call request for transmitting to said control register means a particular preset program corresponding to said signals of the call request,
synchronizing register means for storing the information to be transferred on a bit basis,
means operative upon said peripheral unit being conditioned to effect a transfer of a bit of inventory information for providing a BID signal,
access providing means responsive to a BID signal for selectively providing communication between one of said peripheral units and said central processor portion according to a predetermined priority schedule,
and means included in said control register means for addressing said data storage means upon access being provided to said one peripheral unit for transferring said bit of inventory information.

57. An on-line data processing system for processing call requests comprising
a central processing portion and a plurality of peripheral units,
said central processor portion including data storage means and program means for containing a plurality of sets of instructional data to be selectively transmitted to a selected one of said peripheral units in response to identifying signals forming part of each request,
each of said peripheral units including inventory storage means and control register means to receive said selected instructional data for independently controlling the transfer of inventory information between said data storage means and said inventory storage means,
synchronizing register means for temporarily storing said inventory information to be transferred,
means for indicating the conditioning of said temporary storing means for the transfer of inventory information, means responsive to said indicating means for selectively providing communication between said one peripheral unit and said central processor portion according to a predetermined priority schedule,
means included in said control register means for addressing said data storage means upon communication being provided to said one peripheral unit,
and means for transferring said inventory information between said temporary storing means and said data storage means as addressed by said addressing means.

58. An on-line data processing system for processing call requests including
a central processor portion having input/output storage means and a plurality of peripheral units, each of said peripheral units including inventory storage means and means for effecting a transfer of inventory information between the inventory storage means and said input/output storage means,
said transfer means including individual programming means for said peripheral unit;
said programming means including control register means having state register means operative for determining the operational state of said peripheral unit,
inventory register means for addressing said inventory storage means,
and processor register means for addressing said input/output storage means;
means forming part of said central processor portion for directing to said control register means program instructions developed in accordance with signals contained in a received call request;
synchronizing register means for effecting the transfer of data between said inventory storage means and said input/output storage means,
and means responsive to said synchronizing register means for determining preferential communication between a particular one of said peripheral units and said central processor portion.

59. A data processing system as set forth in claim 58 further including
means for modifying the instructional data in said inventory register means and said processor register means upon each transfer of data between said input/output storage means and said inventory storage means.

60. An on-line data processing system for processing call requests comprising
means for receiving said call requests on a random basis,
a central processor portion including a data storage means and program control means,
a plurality of peripheral units each having control register means and inventory storage means,
said program control means having a plurality of preset programs and operative upon the receipt of a call request to transmit a particular one of said preset programs to said control register means,
addressing means forming part of said control register means for defining a block of information addresses of said inventory storage means and for defining a block of information addresses of said data storage means,
each of said peripheral units including synchronizing register means for receiving inventory information to be transferred between said data storage means and said inventory storage means,
each of said peripheral units further including means for generating a signal indicative of a transfer condition therefor,
and means responsive to said signals so generated for transferring said inventory information on a preferential basis between a selected one of said synchronizing register means and said data storage means of said central processor portion.

61. An on-line data processing system including

a central processor portion and a plurality of peripheral units and

means for transferring information between individual ones of said peripheral units and said central processor portion,

said transferring means including a priority selector device and circuit means responsive to said priority selector device for interconnecting said central processor portion and said peripheral units,

said priority selector device being responsive to said peripheral units being in a transfer condition and operative to provide access through said circuit means between a selected one of said peripheral units and said central processor portion according to a predetermined priority schedule,

said peripheral units including individual programming means for controlling the transfer of information between said particular one of said perhipheral units and said central processor portion through said circuit means.

62. A data processing system as in claim **61** wherein

said central processor portion and said peripheral units each include storage means between which information is to be transferred,

said individual programming means each including first means for addressing said storage means of said central processor portion and second means for addressing said storage means of said peripheral unit.

63. A data processing system as in claim **62** wherein each of said first and second means is a working storage register adapted to be decremented upon each addressing operation thereby.

64. A data processing system as in claim **61**, wherein

said priority selector device comprises a plurality of input terminals each coupled to one of said peripheral units to receive a BID signal therefrom,

a plurality of output terminals each corresponding to one of said peripheral units

an interconnecting circuit between each input terminal and the corresponding output terminal,

said interconnecting circuits including gate means operable, in response to a higher-priority BID signal, to inhibit the development of an output signal on its output terminal.

65. An on-line data processing system for inventory control purposes comprising

a central processing portion including a computer section and an addressable data storage means,

a plurality of randomly operative keysets for originating any of a number of call requests,

a plurality of peripheral units including means for maintaining current records of inventory information to be processed in response to said radomly received call requests,

said central processing portion including means for individually programming selected ones of said peripheral units in accordance with a received call request,

each of said peripheral units including control register means for storing said programs and means for temporarily storing information to be transferred to and from said central processing portion,

means responsive to the storage state of said temporary storing means for seeking access to said central processing portion,

means responsive to said access seeking means for determining preferential access for a particular peripheral unit according to a priority schedule,

first means responsive to said determining means for transferring inventory information between said temporary storing means of a preferred peripheral unit and said central processor,

and means for inhibiting said computer section of said central processing portion during a transfer of said inventory information.

66. In an on-line data processing system comprising

a central processor portion and a plurality of peripheral units,

each of said plurality of peripheral units including control register means and inventory storage means for inventory statistics,

a plurality of keysets,

said central processor portion being responsive to said keysets on a random basis for transmitting predetermined program instructions to said control register means,

said register means being operative thereby to address said inventory storage means,

temporary storage means,

first means responsive to said control register means for transferring said inventory statistics on a bit basis between said inventory storage means and said temporary storage means,

and second means for controlling the transfer of said bits of said inventory statistics on a preferential basis between said temporary storage means of said perhipheral units and said central processor portion.

67. A data processing system as claimed in claim **66**, wherein

said control register means includes a register stage for indicating the number of data transfer operations to be carried out,

and means responsive to said register stage for stopping further transfer operations after the required number have been completed.

68. In an on-line data processing system,

a central processor portion including means for storing a plurality of preset programs and for receiving a plurality of call requests on a random basis,

a plurality of peripheral equipments associated with said central processor portion

said processor portion being operative in response to an individual call request to direct a predetermined one of said preset programs to a particular one of said peripheral equipments,

said peripheral equipments each including control register means for receiving said predetermined program,

storage means included in each of said peripheral units,

said control register means further including means for storing instructions representing a present address of said storage means,

means responsive to said control register means for addressing said storage means,

and means for decrementing said stored address instructions upon each addressing of said storage means.

69. In an on-line data processing system comprising,

a central processor portion including data storage means addressable on a random basis,

a plurality of peripheral units associated with said central processor portion,

each of said peripheral units including inventory storage means and control register means for independently controlling the operation thereof,

said control register means including means to receive from said central processor portion program instructions developed in accordance with a received call request,

said control register means including first means for addressing said data storage means and second means for addressing said inventory storage means,

means responsive to said control register means for transferring inventory statistics between said inventory storage means and said data storage means,

said transfer means including means operative to modify said control register first and second means upon a transfer being effected

whereby the next address of said inventory storage means of said peripheral unit is identified and the next address of said storage means of said central processor portion is identified.

70. An on-line data processing system comprising

a central processor portion and a plurality of peripheral units,

said central processor portion comprising computer means and randomly accessible first storage means adapted as an input/output device for said computer means,

said peripheral units each including a control register means and a second storage means for storing inventory statistics and the like,

said central processor portion also including means for developing instructional data for effecting the operation of any one of said control register means in accordance with the specific nature of a call request,

said control register means including means for addressing said first and said second storage means in accordance with said instruction data,

and means responsive to said control register means for effecting a transfer of information between said first and second storage means.

71. A data processing system as set forth in claim 70 including means for interrupting the operation of said computer means concurrently with the operation of said transfer effecting means.

72. A data processing system as set forth in claim 71, including means for controlling the operation of said transfer effecting means on a predetermined priority schedule.

73. An on-line data processing system comprising

a central processor portion for processing inventory statistics in accordance with a received call request,

said processor portion including computer means having an addressable input/output storage means,

a plurality of peripheral units for storing inventory statistics to be processed by said computer means and including inventory storage means,

control register means for each of said peripheral units and adapted to be selectively instructed by said central processor portion in accordance with a received call request;

said control register means including first register means for establishing the operational state of said peripheral unit,

second register means defining one address of a group of addresses of said inventory storage means,

and third register means for defining one address of a group of addresses of said input/output storage means;

means controlled by said first register means in accordance with said operational state for effecting a transfer of inventory statistics on a bit basis between consecutive corresponding addresses of said inventory storage means and said input/output storage means;

means operative to modify the instructions contained in said second and third register means upon each addressing of said inventory storage means and said input/output storage means respectively;

and means for controlling the operation of said transfer effecting means on a preferential basis according to a priority schedule.

74. A data processing system as set forth in claim 73 wherein means are included in said control register means for interconnecting said first, second and third registers in a register arrangement.

75. In a data processing system having a central processor portion and a plurality of peripheral units to be provided preferential access to said central processor portion,

each of said peripheral units including means for generating a BID signal,

priority selector means having a plurality of input terminals each assigned a lower order of priority than the preceding input terminal,

a corresponding plurality of output terminals,

each of said input terminals being connected to a predetermined one of said BID signal generating means,

said selector means including logic means interconnecting each input terminal to a corresponding output terminal,

each of said logic means including an inhibit terminal connected to the input terminals of higher assigned priority,

said output terminals being operative to provide communication between the corresponding one of said peripheral units and said central processor portion.

76. A data processing system comprising

a plurality of peripheral data transmitting and receiving devices,

a plurality of channels each adapted to establish an operative relationship with respective ones of said peripheral devices,

a memory subsystem having a unique cell reserved for each of said channels,

said cell containing the indirect address of a memory buffer area,

a general purpose arithmetic subsystem for performing computation upon binary coded data and for receiving both arithmetic and input/output commands from said memory subsystem,

said arithmetic subsystem including means for distinguishing an input/output command and initiating a data exchange between a selected peripheral device and the memory buffer area associated with its channel, and

means responsive to a predetermined command word for providing an operational mode providing a continuous data exchange between a selected peripheral device and memory buffer area independent of said arithmetic subsystem.

77. The data processing system defined in claim **76** comprising

means for inhibiting data transfers between said peripheral devices and said memory subsystem during said operational mode, said means being independent of said airthmetic subsystem.

78. The data processing system defined in claim **76** comprising

means for regulating the flow of data between said memory subsystem and said peripheral data transmitting and receiving devices so that the devices having the highest data rates are automatically afforded the highest priority use of said memory subsystem.

79. In a data processing system, the combination of:

a plurality of peripheral data transmitting and receiving devices,

a plurality of channels each adapted to establish an operative relationship with respective ones of said peripheral devices,

a memory subsystem having a unique cell reserved for each of said channels, and

means operating in conjunction with said channels and said memory subsystem for providing an operational mode wherein one or more of said peripheral devices may continuously exchange data with a selected memory area.

80. In the data processing system defined in claim **79**, means for generating a binary encoded code corresponding to each channel for automatically generating the address of said reserved cell.

81. In the data processing system defined in claim **79**,

means for regulating the flow of data between said memory and said peripheral data transmitting and receiving devices so that the devices having the highest data rates are automatically afforded the highest priority use of said memory.

82. In the data processing system defined in claim **79**,

a general purpose arithmetic subsystem for performing computation upon binary coded data and for receiving both arithmetic and input/output commands from said memory,

said arithmetic subsystem including means for distinguishing an input/output command and subsequently transferring said command to one of said channels after which said arithmetic subsystem is free for performing arithmetic computations and receiving subsequent commands from said memory.

83. In a computer system,

a processor capable of processing data in a plurality of cycles,

said processor including a randomly accessible memory capable of being selectively chosen for access by said processor in any one or more of said cycles,

said processor including means operable in each cycle to provide a processor request signal indicating whether or not the processor requires access to the memory during the next cycle,

said processor also including timing means for initiating a processor cycle and for providing timing signals during each initiated processor cycle,

at least one peripheral unit including means for providing a peripheral request signal requesting access to said memory,

said peripheral unit being capable of randomly accessing said memory independently of said processor to permit data to be transferred therebetween,

the period of a cycle of said processor being relatively small with respect to the period between transfers of data by said peripheral unit,

first control means coupled to said timing means and responsive to said processor and peripheral request signals for inhibiting generation of a new processor cycle when both said processor and said peripheral unit request use of the memory for the same period,

and second control means for initiating access of said memory by said peripheral unit in response to a request for same whenever said processor is not making use of said memory.

84. In a computer system,

a processor capable of processing data in a plurality of cycles,

said processor including a randomly accessible memory capable of being selectively chosen for access by said processor in any one or more of said cycles,

said processor including means operable in each cycle to provide a processor request signal indicating whether or not the processor requires access to the memory during the next cycle,

said processor also including timing means for initiating a processor cycle and for providing timing signals during each initiated processor cycle,

at least first and second peripheral units each including means for providing a peripheral request signal requesting access to said memory,

each peripheral unit being capable of randomly accessing said memory independently of one another and of said processor,

the period of a cycle of said processor being relatively small with respect to the period between transfers of data by a peripheral unit,

first control means coupled to said timing means and responsive to said processor and peripheral request signals for inhibiting generation of a new processor cycle when said processor and at least one peripheral unit request use of the memory for the same period,

second control means for giving one peripheral unit priority over the other for access to said memory,

third control means for initiating access of said memory by a peripheral unit whenever said processor or

the other peripheral unit is not making use of same,

and means cooperating with said first control means for permitting generation of a new processor cycle after access of said memory by a peripheral unit.

85. In a computer system,

a processor capable of processing data in a plurality of cycles,

said processor including a randomly accessible memory capable of being selectively chosen for access by said processor in any one or more of said cycles,

said processor including means operable in each cycle to provide a processor request signal indicating whether or not the processor requires access to the memory during the next cycle,

a processor address register and a processor input-output register cooperating with said memory to permit access of a selected address in said memory in accordance with said processor address register,

at least one peripheral unit including means for providing a peripheral request signal requesting access to said memory,

said peripheral unit also including a peripheral address register and a peripheral input-output register capable of cooperating with said memory in the same manner as said processor address register and said processor input-output register,

the period of a cycle of said processor being relatively small with respect to the period between transfers of data by said peripheral unit,

means for gating said registers so as to permit either the processor or said peripheral unit to access said memory independently of one another,

first control means responsive to said processor and peripheral request signals for inhibiting generation of a new processor cycle when both said processor and said peripheral unit request use of the memory for the same period,

and second control means for initiating access of said memory by said peripheral unit in response to a request for same whenever said processor is not making use of said memory.

86. In a computer system,

a processor capable of processing data in a plurality of cycles,

said processor including a randomly accessible memory capable of being selectively chosen for access by said processor in any one or more of said cycles,

said processor including means operable in each cycle to provide a processor request signal indicating whether or not the processor requires access to the memory during the next cycle,

said processor including processor memory access indicating means for indicating when the processor is using the memory and processor memory request indicating means for indicating whether the processor requests access to the memory during the next processor cycle,

at least one peripheral unit including peripheral request indicating means for indicating when said peripheral unit requests access to said memory,

the period of a cycle of said processor being relatively small with respect to the period between transfers of data by said peripheral unit,

means coupled to said processor memory request indicating means and said peripheral request indicating means for inhibiting generation of a new processor cycle when both said processor and said peripheral unit request access to the memory for the same period,

and means coupled to said peripheral request indicating means and said processor memory access indicating means for permitting said peripheral unit to access said memory independently of said processor when said processor is not accessing the memory.

87. In a computer system,

a processor capable of processing data in a plurality of cycles,

said processor including timing means for initiating a processor cycle and for providing timing control signals during each initiated processor cycle,

said processor also including a randomly accessible memory capable of being selectively chosen for access by said processor in any one or more of said cycles,

said processor including means operable in each cycle to provide a processor request signal indicating whether or not the processor requires access to the memory during the next cycle,

means including processor address means and processor input-output means for cooperating with said memory to permit performance of a memory cycle during which a selected address in memory is accessed in accordance with said processor address means,

said processor further including processor memory access indicating means for indicating when the processor is using the memory and processor memory request indicating means for indicating whether the processor requests access to the memory during the next processor cycle,

at least one peripheral unit including peripheral address means and peripheral input-output means capable of cooperating with said memory in the same manner as said processor address means and said processor input-output means,

the period of a cycle of said processor being relatively small with respect to the period between transfers of data by said peripheral unit,

gating means for gating said address means and said input-output means so as to permit either the processor address and input-output means or the peripheral address and input-output means to access said memory independently of one another,

said peripheral unit also including a peripheral request indicating means for indicating when said peripheral unit requests access to said memory,

means coupled to said processor memory request indicating means and said peripheral request indicating means for inihibiting generation of a new processor cycle when both said processor and said peripheral unit request access to the memory for the same period,

and means coupled to said peripheral request indicating means and said processor memory access indicating means for permitting said peripheral unit to access said memory via said gating means when said processor is not accessing the memory.

88. In a computer system,

a processor capable of processing data in a plurality of cycles,

said processor including a randomly accessible memory capable of being selectively chosen for access by said processor in any one or more of said cycles,

said processor including means operable in each cycle to provide a processor request signal indicating whether or not the processor requires access to the memory during the next cycle,

means cooperating with said memory to provide access thereto in discrete memory cycles each of duration of the same order as a processor cycle,

first indicating means for indicating when said processor is accessing said memory during a processor cycle,

second processor indicating means for indicating when the next cycle of said processor requires access of said memory,

at least one peripheral unit including means for accessing said memory independently of said processor,

said peripheral unit also including peripheral request indicating means,

means coupled to said first processor indicating means and said peripheral request indicating means for permitting said peripheral to access said memory independently of said processor when said processor is not accessing the memory,

the period of a cycle of said processor being relatively small with respect to the period between transfers of data by said peripheral unit,

and means coupled to the first and second processor indicating means and said peripheral request indicating means for inhibiting the performance of the next cycle by said processor when both said processor and said peripheral unit request access to the memory for the same period,

the next processor cycle being inhibited until the peripheral unit completes a memory cycle.

89. For use with a data processing system comprising, in combination, a computer, an addressable storage device storing data, channel instructions and further instructions including select and control instructions, and a plurality of input/output devices, a control device comprising:

channels coupling said input/output devices to said addressable storage device,

means for interpreting said select instructions to render one channel operative to select a chosen input/output device,

means interpreting said channel instructions to obtain a control instruction,

means controlled by said control instruction for controlling the transfer of data via said selected channel,

means controlled by said channel instruction for storing in said selected channel the manifestation of the address of a next control instruction located in said storage means, and

means rendered operative upon completion of said transfer of data to render said manifestation of the address of a next control instruction effective to select and render operative said next control instruction.

90. A control device as in claim **89** including means for establishing priority of access to said storage device between said computer and said channels, and

means controlled by the selected channel operation to grant priority of access to said channel instead of to said computer.

91. A control device as in claim **89** including means for establishing priority of access to said storage device, among said channels,

means conditioned by operation of a chosen channel, and

means controlled by said conditioned means rendering said priority means operative to grant access to said chosen channel, in preference to another channel.

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