

- [54] **TRAFFIC CONTROL SYSTEM**
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[63] Continuation-in-part of Ser. No. 863,309, Oct. 2, 1969, Pat. No. 3,605,084, which is a continuation-in-part of Ser. No. 826,212, May 20, 1969, Pat. No. 3,644,884.
[52] U.S. Cl. **340/41, 340/40, G08g/1/07**
[58] Field of Search **340/35, 37, 40, 41**

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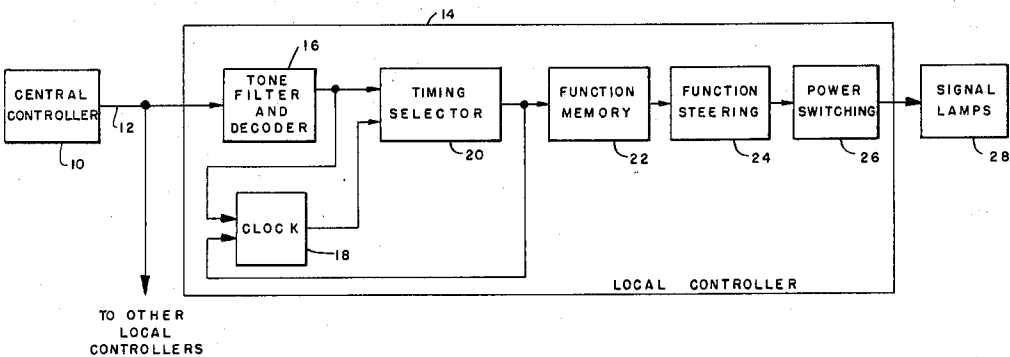
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[57] **ABSTRACT**

A traffic control system in which a plurality of local controllers are connected to a central controller by means of a single communication channel. Each local controller can include a non-volatile memory which stores the desired cycle for that local controller. When it is desired to alter the cycle of a particular local controller, the central controller applies to the communication channel a code signal uniquely associated with that local controller. This enables the selected local controller to respond to subsequent coded signals altering the cycle, while the remaining local controllers do not respond to such commands. By way of illustration, the coded signals may be coded pulses of unique tones.

32 Claims, 7 Drawing Figures



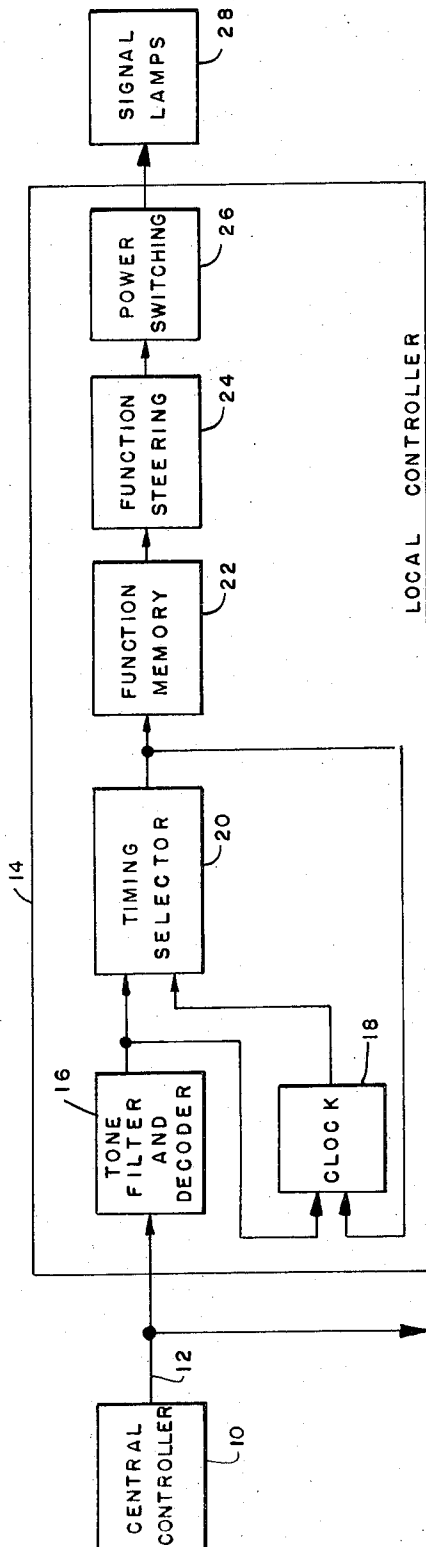


FIG. 1.

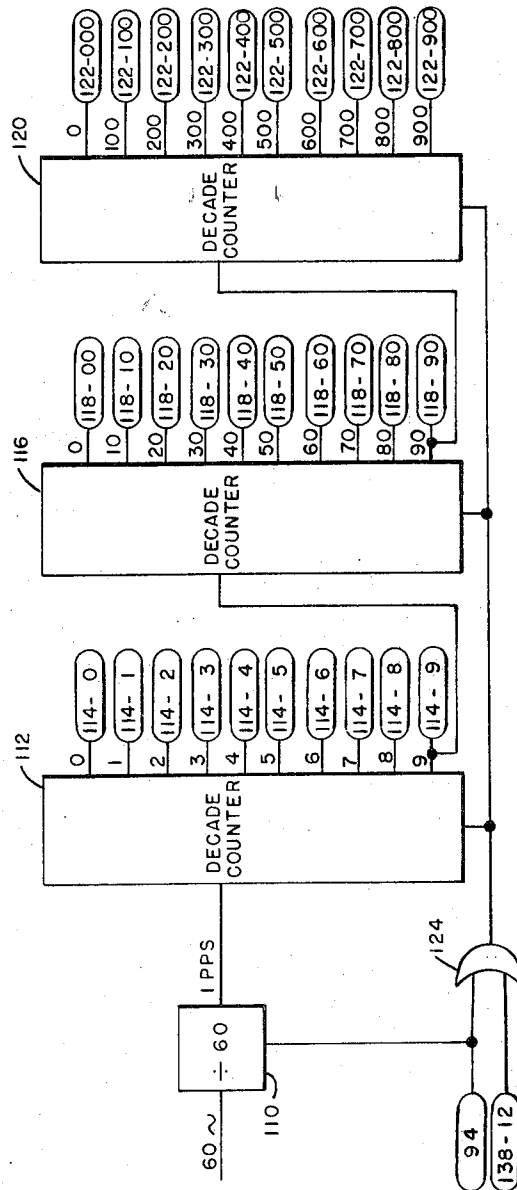


FIG. 3.

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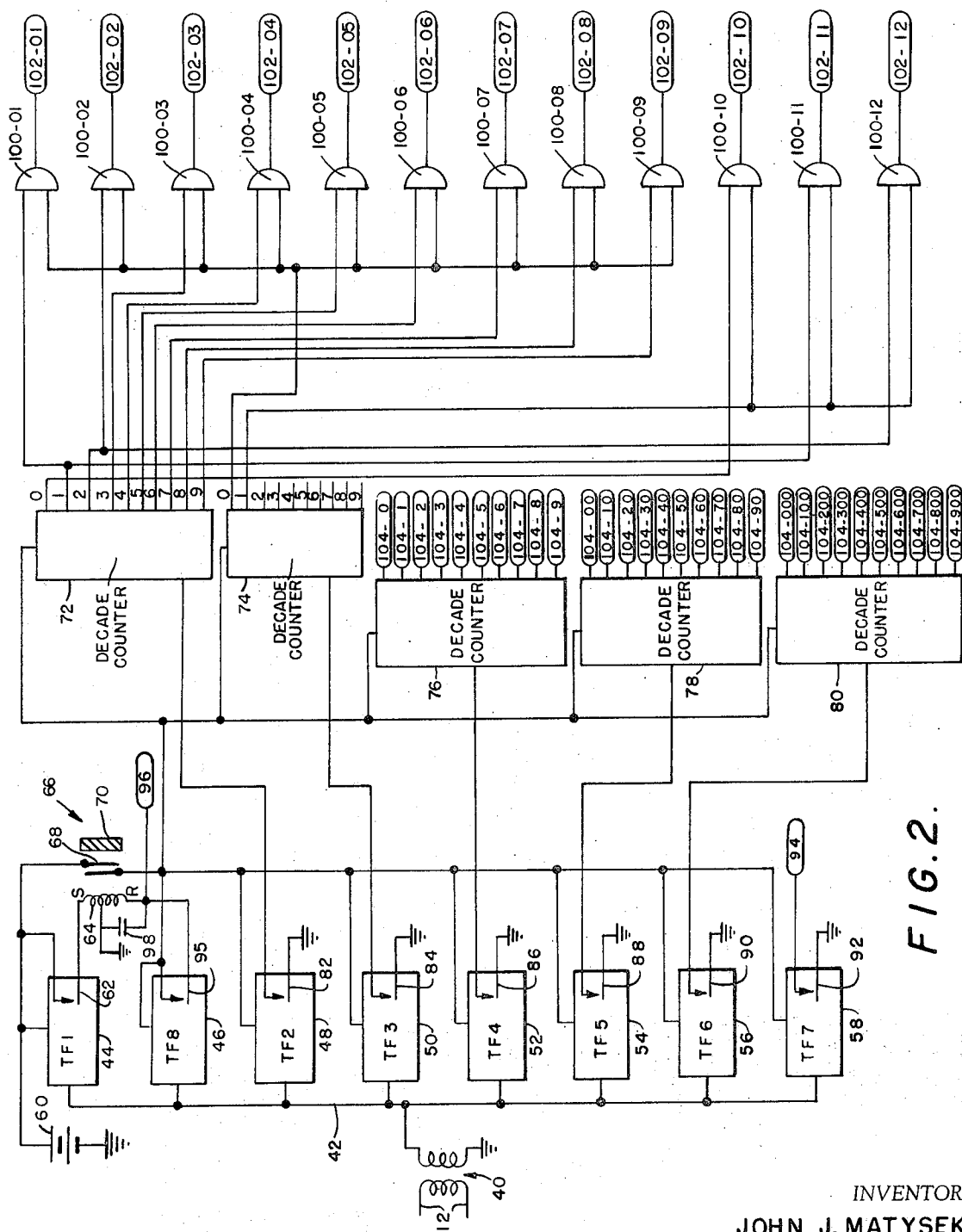


FIG. 2.

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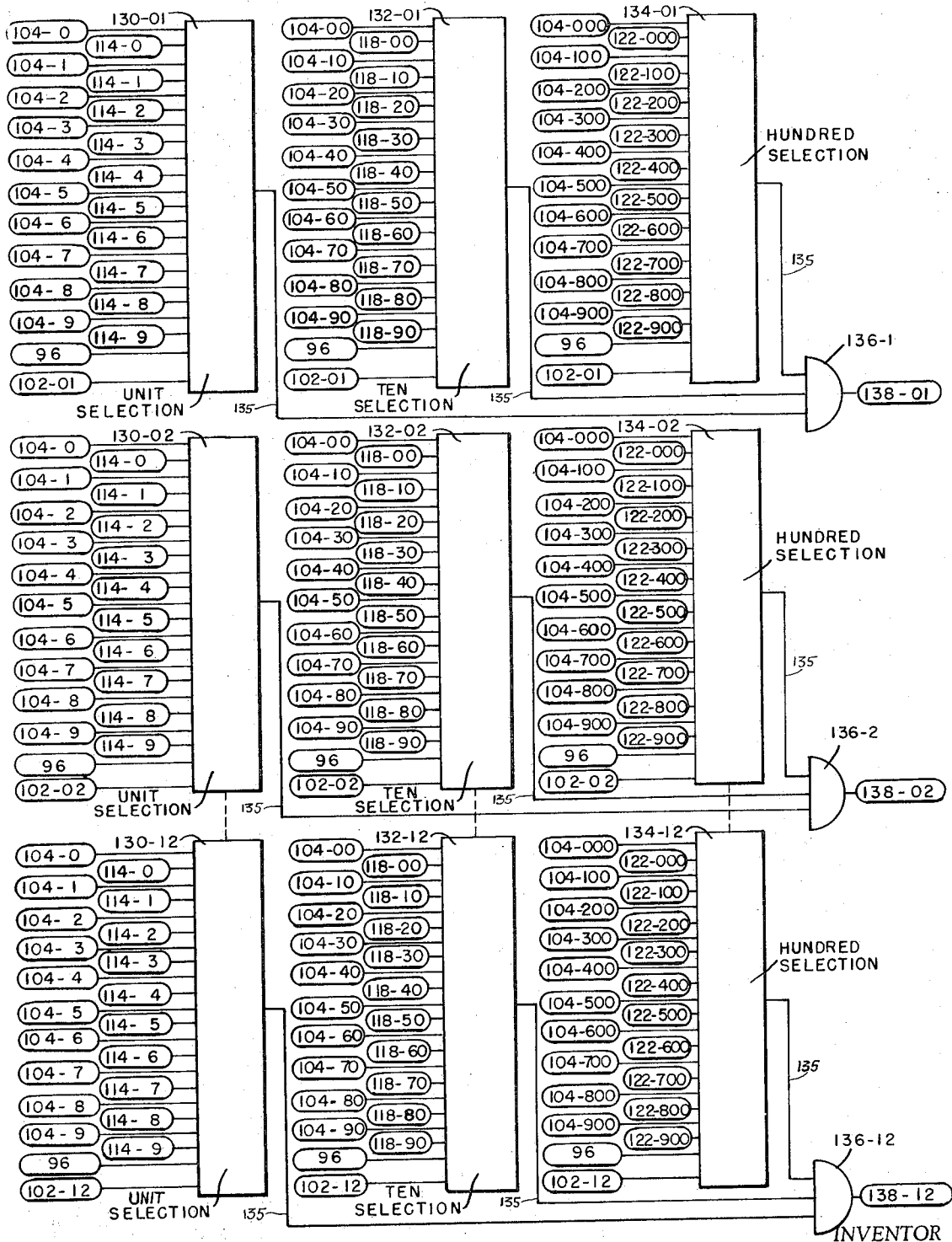


FIG. 4.

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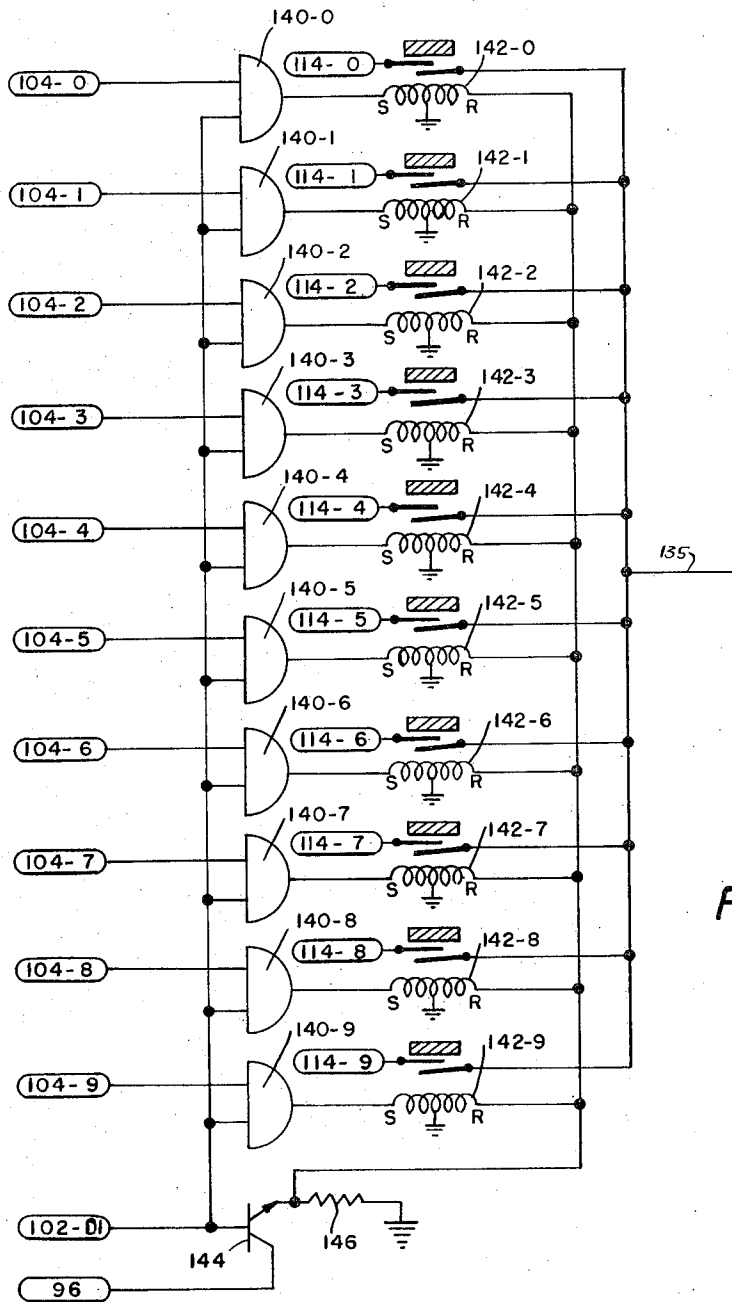


FIG. 5.

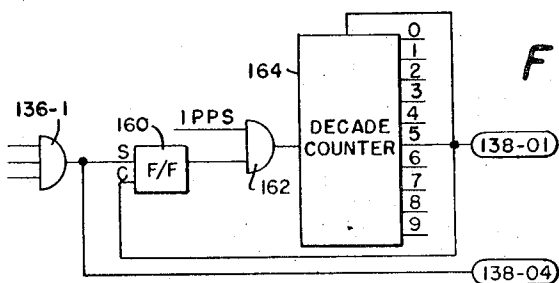


FIG. 7.

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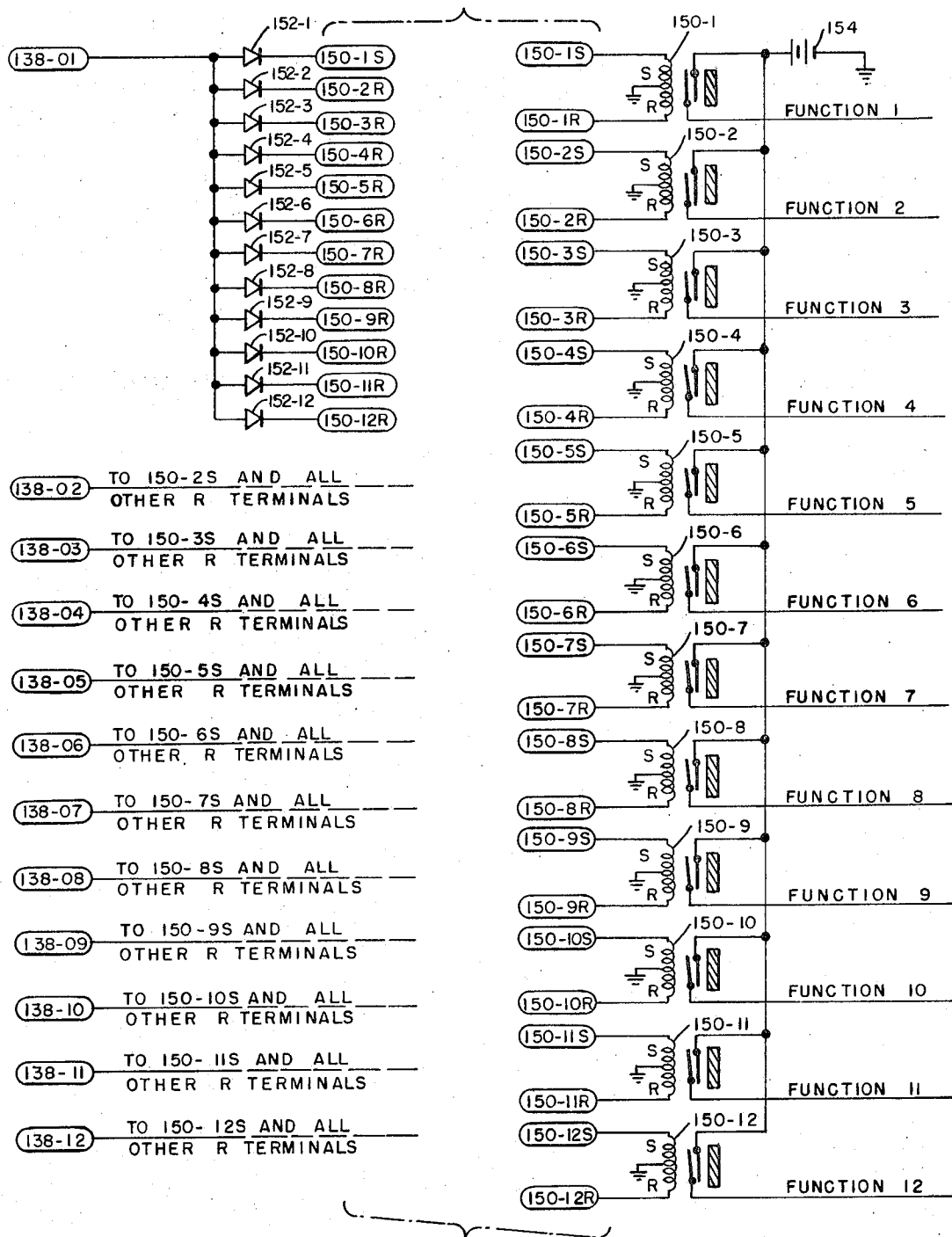


FIG. 6.

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TRAFFIC CONTROL SYSTEM

This application is a continuation-in-part of U. S. Pat. application Ser. No. 863,309 filed Oct. 2, 1969, now U. S. Pat. No. 3,605,084 which in turn is a continuation-in-part of U. S. Pat. application Ser. No. 826,212 filed May 20, 1969, now U. S. Pat. No. 3,644,884.

The present invention pertains to a traffic control system. More particularly, the present invention pertains to a traffic control system including a local controller capable of substantially independent operation for extended periods of time to provide traffic control intervals with a cycle which has been previously directed from a central control location and which can be changed from the central controller as desired without the necessity of visiting the local controller.

In urban areas, it is frequently necessary to have traffic control indicators at numerous intersections to ensure the smooth flow of traffic. Traffic patterns vary from time to time during the course of a day. By way of example, during morning hours such as 7:00 a.m. to 9:00 a.m. traffic might be considerably more heavy in a first direction on a street than in the second opposite direction. Then during evening hours such as 4:30 p.m. to 6:30 p.m. traffic might be considerably more heavy in the second direction than in the first. During the remainder of the day, the traffic might be fairly well balanced in the two directions. To permit optimum traffic flow, therefore, requires that the right-of-way signal indicators at adjacent intersections be sequenced to permit substantially continuous movement in the first direction of the street during the morning peak traffic period or rush hour, and that these signal indicators be sequenced differently to permit substantially continuous movement in the second direction of the street during the evening peak traffic period or rush hour. This requires that the traffic controllers at the intersections have their cycles changed from time to time during the day. These changes at the several controllers at different intersections within the urban areas must take place substantially simultaneously. Consequently, it is not possible for the changes to be made manually, and so the several local controllers are generally connected by control wires to a central controller which is capable of adjusting the cycle for each local controller as desired.

U. S. Pat. applications Ser. No. 826,212 and Ser. No. 863,309 depict traffic control systems in which local controllers are provided which have the capability of having their control cycles altered in response to signals sent over cables from a central control location. However, the traffic control system disclosed in patent application Ser. No. 826,212 utilizes analog timing circuits which might be very precisely adjusted if a series of street intersections is to be sequentially provided with right-of-way. Even a small misadjustment of the timing will, over a number of traffic cycles, result in the right-of-way no longer being provided sequentially. The traffic control system disclosed in patent application Ser. No. 863,309 utilizes digital timing circuitry which is extremely accurate, overcoming the problems of the analogue timing circuit; however, this traffic control system requires that each local controller have continuous communication with the central controller for each command. If this communication is lost, a back-up timer within the local controller can take over, starting operation at a pre-set point in the traffic cycle,

but in such event there is no synchronization of the controllers at consecutive intersections.

The present invention is a traffic control system for controlling right-of-way signal indicators utilizing digital timing circuitry and in which each local controller is able to operate for extended periods of time independent of central control and can have its cycle altered when desired by commands sent from central control to a plurality of such local controllers over a single pair of lines. In accordance with the present invention, each local controller is provided with digital clock circuitry for generating timing signals. Selected ones of these timing signals are gated to generate the desired right-of-way or traffic interval functions. These functions are then steered in the desired cycle to the appropriate right-of-way indicators. A plurality of such local controllers are coupled by a single pair of wires to the central control location. When it is desired to change the control cycle of a local controller, the central controller transmits coded tone signals which are accepted only by the intended local controller. These coded tone signals are then utilized to alter the selection of the timing signals which result in alteration of the traffic interval functions.

These and other aspects and advantages of the present invention are more apparent in the following detailed description and claims, particularly when considered in conjunction with the accompanying drawings in which like parts bear like reference numerals. In the drawings:

FIG. 1 is an overall block diagram of a traffic control system in accordance with the present invention;

FIG. 2 is a block diagram of tone filter and decoder circuitry suitable for use within the local controller of FIG. 1 in accordance with the present invention;

FIG. 3 is a block diagram of a clock suitable for use within the local controller of FIG. 1 in accordance with the present invention;

FIG. 4 is a block diagram of timing selector circuitry suitable for use within the local controller of FIG. 1 in accordance with the present invention;

FIG. 5 is a schematic diagram of one set of selection circuitry suitable for use within the timing selector circuitry of FIG. 4 in accordance with the present invention;

FIG. 6 is a schematic diagram of function memory circuitry suitable for use within the local controller of FIG. 1 in accordance with the present invention; and

FIG. 7 is a block diagram of function generation circuitry suitable for use in a modified embodiment of traffic control system in accordance with the present invention.

FIG. 1 depicts an overall block diagram of a traffic control system in accordance with the present invention. Central controller 10 is connected by line 12 to a plurality of local controllers such as local controller 14. By way of example, line 12 might be a telephone pair. When it is desired to change the cycle of a particular local controller, central controller 10 applies coded tone signals via line 12 to every local controller 14. Within each local controller 14, these coded tone signals are applied to one filter and decoder 16, and only the desired local controller 14 responds by altering its cycle.

Local controller 14 is capable of providing signals to control right-of-way at an intersection of any capacity. If, for example, the intersection includes only two inter-

secting streets, street A and street B, with a right-of-way interval, a clearance interval and a stop interval for each street, then the associated local controller 14 needs to generate only four functions: street A right-of-way; street A clearance; street B right-of-way; and street B clearance. The street A stop interval is provided whenever eight street B right-of-way or street B clearance is present, and, conversely, the street B stop interval is provided whenever either street A right-of-way of street A clearance is present. On the other hand, if a local controller 14 is utilized at a more complex intersection, then that controller 14 must generate more functions. By way of example, if the controller is utilized at an intersection of three streets, some of which are to be provided left turn only intervals and some of which are to be provided walk only intervals, then controller 14 must generate enough functions to provide for each desired interval. As a general rule, the majority of street intersections can be handled by, at most, six intervals necessitating a local controller capable of generating six functions; 90 percent of the street intersections can be handled with a maximum of twelve intervals requiring a local controller capable of generating twelve functions; and the remaining 10 percent of the street intersections may require up to 24 intervals and so a local controller capable of generating 24 functions. FIG. 2 depicts circuitry suitable for use as tone filter and decoder 16 within a local controller 14 capable of generating twelve functions. Additional functions can readily be provided with additional sets of circuitry.

As depicted in FIG. 2, the tone signals on pair 12 received by tone filter and decoder 16 are applied through transformer 40 to line 42 which is connected to the input of each of a plurality of tone filters 44, 46, 48, 50, 52, 54, 56, and 58. Each tone filter 44-58 includes a normally open electrical switch contact which is closed in response to the tone to which that tone filter is tuned. Thus, for example, when the tone one signal, having the frequency to which tone filter 44 is tuned, is applied by pair 12 and transformer 40 to line 42, contact 62 of tone filter 44 closes. Each local controller 14 has its tone filter 44 tuned to a unique frequency so that upon receipt of that unique frequency from central controller 10, only that local controller 14 is enabled to respond to subsequent signals from central controller 10, indicating the change to be made in its traffic interval cycle. The several local controllers 14 can have their tone filters 46 tuned to the same frequencies, their tone filters 48 tuned to the same frequency, their tone filters 50 tuned to the same frequency, their tone filters 52 tuned to the same frequency, their tone filters 54 tuned to the same frequency, their tone filters 56 tuned to the same frequency, and their tone filters 58 tuned to the same frequency.

One side of contact 62 of tone filter 44 is connected to a source of power such as battery 60. In addition, battery 60 is connected to the power input of tone filter 44. When a tone one signal causes contact 62 to close, power from source 60 is applied through contact 62 to the set side of coil 64 of magnetic latching reed relay 66. This current through coil 64 causes the relay contacts 68 to close, and relay magnet 70 maintains those contacts closed after the tone one signal is no longer present so that contact 62 has opened to remove the set current from coil 64.

With contacts 68 closed, power from source 60 is applied to each of the remaining tone filters 46 through 58, thus enabling each of those tone filters to respond to the tone to which it is tuned. Power from source 60 is also applied through contacts 68 to decade counters 72, 74, 76, 78, and 80, resetting each counter and enabling it to respond to pulses applied to its input. With power applied through contact 68, each time tone two is received on pair 12, contact 82 of tone filter 48 closes, applying a pulse to decade counter 72. Similarly, each time tone three is received via pair 12, contact 84 of tone filter 50 closes, applying a pulse to the input of decade counter 74. Likewise, each time tone four is received on pair 12, contact 86 of tone filter 52 closes, applying a pulse to decade counter 76, and each time tone five is received on pair 12, contact 88 of tone filter 54 closes, applying a pulse to the input of decade counter 78. Similarly, each time tone six is received on pair 12, contact 90 of tone filter 56 closes, applying a pulse to the input of decade counter 80. When tone seven is received on pair 12, contact 92 of tone filter 58 closes, applying a pulse to terminal 94, and each time tone eight is received on pair 12, terminal 95 of tone filter 46 closes, applying power from source 60 to terminal 96, to the reset side of coil 64, and to the first side of capacitor 98, the second side of which is tied to ground and to the center tap of coil 64. This charges capacitor 98, following which reset current through coil 64 opens contacts 68. Since magnet 70 is not sufficient to alter the position of contacts 68, these contacts remain open even after the reset current through coil 64 has stopped.

When it is desired to change the cycle of right-of-way intervals provided by a local controller 14, central controller 10 applies via line 12 a pulse of the tone one frequency to which the tone filter 44 is that local controller 14 is tuned. As a consequence, contact 68 within that local controller 14 closes, applying power to tone filters 46-58 of the local controller and enabling those tone filters to respond to the tone two through tone eight signals on pair 12. Since the tone filters 44 in other local controllers 14 are tuned to different tone one frequencies, no other local controller is enabled to respond to the tone two through tone eight signals.

Having enabled the desired local controller 14 by means of a pulse of its tone one signal, central controller 10 then instructs that local controller 14 which function is to have its time of initiation changed with respect to a time zero within the local controller. To do this, central controller 10 transmits by pair 12 a number of pulses of the tone two signal equal to the units digit of that function number and a number of pulses of the tone three signal equal to the tens digit of that function number. Thus, for example, if the time of initiation of function seven is to be changed, central controller 10 applies seven pulses of tone two signal and no pulses of the tone three signal. Likewise, if function eleven is to have its time of initiation changed, then central controller 10 applies one pulse of the tone two signal and one pulse of the tone three signal. Then pulses can be transmitted in either order or simultaneously.

Each decade counter 72-80 has been reset to zero upon the application to it of power from contact 68, and so each decade counter applies a signal on its zero output line. In response to each pulse of tone two signal, contact 82 of tone filter 48 closes and applies a

pulse to decade counter 72. Thus, if seven pulses of tone two signal are received on line 12, decade counter 72 is stepped to apply a signal on its seven output line. Similarly, if one pulse of tone two signal and one pulse of tone three signal are received, contact 82 and contact 84 each close once, and decade counter 72 is stepped to apply a signal on its one output line while decade counter 74 is stepped to apply an output on its one output line.

The outputs of decade counters 72 and 74 are gated by AND gates 100 to provide a signal on an output terminal 102 corresponding with the function number transmitted from central controller 10. Thus, if controller 10 signals that the time of initiation of function one is to be altered, AND gate 100-01 applies a signal to output terminal 102-01 of tone filter and decoder 16. In like manner, if central controller 10 indicates that the time of initiation of one of the other functions two through 12 is to be altered, then the corresponding AND gate 100-02 through 100-12 applies a signal to its corresponding output terminal 102-02 through 102-12.

Central controller 10 then transmits a signal indicating the time with respect to local time zero at which the selected function is to be initiated. To do this, central controller 10 transmits a number of pulses of tone four, tone five, and tone six signals corresponding respectively to the units digit, the tens digit and the hundreds digit of the time. Thus, for example, if a selected interval is to be initiated 137 seconds after local time zero, seven pulses of tone four signal, three pulses of tone five signal, and one pulse of tone six signal are applied. If, of course, the traffic cycle would never have over 99 seconds, then tone six would never be generated, and so tone filter 56 and decade counter 80 could be omitted.

In response to the pulses of the tone four signal, tone five signal, and tone six signal, decade counters 76, 78, and 80, respectively, step to the designated outputs. If, for example, central control 10 indicates that the selected function is to be initiated 137 seconds after local time zero, decade counter 76 steps to apply a signal on its seven output line, decade counter 78 steps to apply a signal on its three output, and decade counter 80 steps to apply a signal on its one output.

Decade counter 76, which indicates the units digit of the time at which the selected function is to be initiated, has its ten outputs connected to output terminals 104-0 through 104-9, respectively, of tone filter and decoder 16. Similarly, decade counter 78, which indicates the tens digit of the time at which the selected function is to be initiated, has its ten outputs connected, respectively, to output terminals 104-00 through 104-90. Likewise, decade counter 80, which indicates the hundreds digit of the time at which the selected function is to be initiated, has its 10 outputs connected, respectively, to output terminals 104-000 through 104-900.

Tone filters 44-58 can be any frequency sensitive switches such as those marketed by Douglas Randall Division of Walter Kidde & Co. under the trademark Fritch. Magnetic latching reed relays suitable for use as relays 66 are likewise available from Douglas Randall Division of Water Kidde & Co. as their Model No. 12CGL1A. Decade counters 72-80 can be any suitable counters such as ten stage shift registers or ring counters. If, as depicted in FIG. 2, less than 20 functions are

to be indicated, with the result that decade counter 74 need be capable of generating only two outputs, then any bistable switching device could be utilized rather than a full decade counter; the example of two-stage shift register or a bistable multivibrator could be utilized.

Within local controller 14 clock 18 generates timing signals for the local controller. As shown in FIG. 3, clock 18 derives power from a locally available source such as a local source of 60 hertz excitation. This 60 hertz signal is applied to dividing circuit 110 which divides the 60 hertz input by 60 to provide a one pulse per second output to decade counter 112. Decade counter 112 has ten output terminals 114-0 through 114-9 and in response to pulses from dividing circuit 110 decade counter 112 applies outputs sequentially to these output terminals. The nine output of decade counter 112 is additionally connected as an input to decade counter 116 which likewise has ten outputs that are connected respectively to terminals 118-00 through 118-90. Decade counter 116 has its nine output connected as an input to decade counter 120 which likewise has nine outputs connected respectively to output terminals 122-000 through 122-900. Decade counters 112, 116, and 120 thus count the one-pulse-per-second pulses from dividing circuit 110. Terminal 94, which is connected to switch 92 of tone filter 58, is connected to one input of OR gate 124, the output of which is connected to the reset input of each decade counter 112, 116 and 120. Terminal 94 is also connected to the reset input of divider 110.

As seen in FIG. 1, tone filter and decoder 16 and clock 18 have outputs connected to timing selector 20, a suitable circuit for which is shown in FIG. 4. As there depicted, a set of time selection circuits is provided for each of the twelve functions which local controller 14 is capable of generating. Thus, unit-selection circuit 130-01, 10-selection circuit 130-01, and hundred-selection circuit 134-01 are provided to select the time at which function one is initiated; unit-selection circuit 130-02, 10-selection circuit 132-02, and hundred-selection circuit 134-02 are provided to select the time at which function two is initiated, etc.

Decade counter 112 has its output 114-0 through 114-9 connected to input terminal 114-0 through 114-9, respectively, of each unit-selection circuit 130-01 through 130-12. Likewise, decade counter 116 has its outputs 118-00 through 118-90 connected to inputs 118-00 through 118-90 of each ten-selection circuit 132-01 through 132-12 within function selector 20, and decade counter 120 has its outputs 122-000 through 122-900 connected to inputs 122-000 through 122-900 of each hundred-selection circuit 134-01 through 134-12.

Decade counter 76 within tone filter and decoder 16 has its outputs 104-0 through 104-9 connected to input terminals 104-0 through 104-9, respectively, of each unit-selection circuit 130-01 through 130-12 within timing selector 20. Similarly decade counter 78 has its outputs 104-00 through 104-90 connected to input terminals 104-00 through 104-90, respectively, of each ten-selection circuit 132-01 through 132-12, and decade counter 80 has its outputs 104-000 through 104-900 connected to input terminals 104-000 through 104-900, respectively, of each hundred-selection circuit 134-01 through 134-12.

Decade counters 76, 78, and 80 apply to the time selection circuits 130, 132, and 134 respectively, signals indicating the time after local time zero at which the selected function is to be initiated. Thus, every unit-selection circuit 130-01 through 130-12 receives as an input the signal on the one activated output line 104-0 through 104-9 of decade counter 76, as determined by the number of pulses of tone four signal received from central controller 10. Every 10-selection circuit 132-01 through 132-12 receives as an input the signal on the one activated output line 104-00 through 104-90 of decade counter 78, as determined by the number of pulses of tone five signal from central controller 10. Likewise, every hundred-selection circuit 134-01 through 134-12 receives as an input the signal on the one activated output line 104-000 through 104-900 of decade counter 80, as determined by the number of pulses of tone six signal. If the time of initiation of one of the functions one through 12 is to be altered, the corresponding AND gate 100-01 through 100-12 is applying a signal through the associated terminal 102-01 through 102-12 to the associated unit-selection circuit 130-01 through 130-12, the associated 10-selection circuit 132-01 through 132-12, and the associated hundred-selection circuit 134-01 through 134-12. Whichever set of time selection circuits 130, 132 and 134 receives signals on its terminals 102 is enabled to alter the time at which it responds to the time signals indicated by decade counters 76, 78, and 80. That alteration takes place upon application to every time selection circuit 130, 132, and 134 of a signal from tone filter 46 through terminal 96. Upon this signal being applied to the terminal 96 of each time selection circuit, the one set of time selection circuits which has been enabled by a signal on its terminals 102 is set to a condition selecting as the time of initiation of its associated function the time after local time zero indicated by the outputs from decade counters 76, 78 and 80. Each of the time selection circuits 130, 132, and 134 is set in this manner to a desired function initiation time.

Each time selection circuit within the twelve sets of time selection circuits has its output connected via an output line 135 as an input to an associated AND gate 136-1 through 136-12. Decade counter 112 of clock 18 applies to each of the unit-selection circuit 130-01 through 130-12 time signals as pulses are applied to that decade counter from divider 110. Whenever a unit-selection circuit 130-01 through 130-12 receives from decade counter 112 a time signal corresponding to the unit digit of the function initiation time to which that unit-selection circuit is set, the unit-selection circuit applies an output to the associated AND gate 136-1 through 136-12. Likewise, upon receipt from decade counter 116 of the respective time signals to which they have been set, 10-selection circuits 132-01 through 132-12 apply outputs to the associated AND gates 136-1 through 136-12 and upon receipt from decade counter 120 of the respective time signals to which they have been set, hundred-selection circuits 134-01 through 134-12 apply outputs to the associated AND gates 136-1 through 136-12. When one of the AND gates 136-1 through 136-12 receives signals on each of its three inputs, it applies a signal to the associated terminal 138-01 through 138-12. The signals in terminals 138-01 through 138-12 indicate that the associated function is to be initiated. In addition, terminal

138-12 is connected to the second input of OR gate 124 within clock 18 to reset the clock.

FIG. 5 illustrates circuitry suitable for use as time selection circuit 130, 132, and 134. In FIG. 5, the input terminals are designated to correspond with those of unit-selection circuit 130-01; however, the circuitry of each time selection circuit 130, 132, and 134 is the same. Each input terminal 104-0 through 104-9 is connected to one input of a corresponding AND gate 140-0 through 140-9. The second input of each AND gate 140-0 through 140-9 is connected to input terminal 102-01. Each AND gate 140-0 through 140-9 has its output connected to the set side of the coil of a corresponding magnetic latching relay 142-0 through 142-9. Each relay 142-0 through 142-9 has its first contact connected to the corresponding input terminal 114-0 through 114-9. Input terminal 102-01 is also connected to the base of NPN transistor 144, the collector of which is tied to input terminal 96. The emitter of transistor 144 is coupled to ground through resistor 146. The emitter of transistor 144 is also tied to the reset side of the coil of each magnetic latching relay 142-0 through 142-9. The second contact of each relay 142-0 through 142-9 is tied to the selection circuit output line 135 which is connected as an input to the associated AND gate 136-1 through 136-12.

When it is desired to alter the cycle of a particular local controller 14, central controller 10 transmits on line 12 the tone one frequency which activates the tone filter 44 within that local controller. Central controller 10 then sends a number of pulses of the tone two signal corresponding with the number of the function which is to have its time of initiation altered. Assume that this is function one. AND gate 100-01 then applies a signal through terminal 102-01 to enable each AND gate 140-0 through 140-9 is unit-selection circuit 130-01, ten-selection circuit 132-01, and hundred-selection circuit 134-01. Central controller 10 transmits a number of pulses of tone four, tone five, and tone six signal to indicate the time at which that function is to be initiated, and the corresponding output terminals 104 of decade counters 76, 78, and 80 apply signals to the associated inputs of time selection circuits 130-01, 132-01, and 134-01. Assume that output terminal 104-5 from decade counter 76 applies a signal to input terminal 104-5 of unit-selection circuit 130-01 in FIG. 5. This signal is applied to AND gate 140-5 which in turn applies a signal to the set side of the coil of magnetic latching relay 142-5 causing the contacts of the relay to close. Central controller 10 then applies a pulse of tone eight signal. This signal causes tone filter 46 to close its contacts 95. As a consequence, a signal is provided through terminal 96 to the collector of transistor 144. Accordingly, a signal is applied to the reset side of the coil of each magnetic latching relay 142-0 through 142-9. This resets whichever relay had previously been set. The signal on the set side of the coil of relay 142-5 overcomes the signal on the reset side of its coil, and so the relay 142-5 contacts remain closed. The current through contacts 95 of tone filter 46 charges capacitor 98 and then resets coil 64 of relay 66, causing contacts 68 to open and returning tone filter and decoder 16 to its quiescent condition in which it provides no output signal and is ready to accept commands to alter the time of initiation of another function. The bias magnet of relay 142-5 maintains the contacts of that relay closed. Thus, each time decade

counter 112 within clock 18 applies a signal on its output terminal 114-5, that signal passes through the closed contacts of relay 142-5 to one input of AND gate 136-1. In like manner, each of the other time selection circuits 130, 132 and 134 applies a signal to the associated AND gate 136 when the respective decade counter 112, 116, or 120 applies a signal on the output terminal corresponding with the set magnetic latching reed relay 142-0 through 142-9 in the selection circuit. The magnetic latching reed relays 142-0 in the unit-selection circuits 130-01 through 130-12, the 10-selection circuits 132-01 through 132-12, and the hundred-selection circuits 134-01 through 134-12 thus act as a non-volatile memory for the initiation times of the functions of local controller 14.

Output terminal 138-12 from AND gate 136-12 is coupled through OR gate 124 to reset decade counters 122, 116, and 120 of clock 18 to return clock 18 to local time zero. Thus, time selection circuits 130-12, 132-12, and 134-12 determine the cycle length for the right-of-way indicators connected to local controller 14. If it is preferred that function one be initiated at the local controller time zero, that can be achieved in any of several manners. For example, the signal from output terminal 138-01 can be utilized to reset clock 18 rather than the signal from terminal 138-12. Then, time selection circuits 130-01, 132-01, and 134-01 are set to the cycle length, which, ignoring switching times, then corresponds with local time zero. Alternatively, an additional set of time selection circuits 130-C, 132-C, and 134-C (not shown) can be provided with output 13 from decade counters 72 and 74 gated to input 102-C thereof to set those time selection circuits to the cycle length, with the output from an associated AND gate 136-C applied through OR gate 124 to reset clock 18.

When it is desired to synchronize the timing circuits 18 in all the local controllers 14, central controller 10 applies the tone one frequencies of all the local controllers to line 12. This enables every local controller 14 to respond to the following commands. Central controller 10 then applies a pulse of tone seven signal which activates the tone filter 58 in every local controller. Consequently, in every local controller, a signal is applied through terminal 94 to clock 18 in which it resets divider 110 and passes through OR gate 124 to reset decade counters 112, 116 and 120. This resets the decade counters to time zero and synchronizes the divider 110 in each of the local controllers to assure that the first output from every divider is at the same time.

As seen in FIG. 1, the output of timing selector 20 is connected to function memory 22. FIG. 6 illustrates circuitry suitable for use as function memory 22. For each of the functions one through twelve which can be accommodated by local controller 14 in this illustrative example, an associated magnetic latching reed relay 150-1 through 150-12 is provided. Thus, when local controller 14 is to provide function one, magnetic latching reed relay 150-1 is in its set condition with its contacts closed; when the local controller 14 is to provide function two, relay 150-2 is in its set condition with its contacts closed, etc. Relay 150-1 has the set side of its coil connected to terminal 150-1S and the reset side of its coil connected to terminal 150-1R. In like manner, each of the other relays 150-2 through 150-12 has the set side of its coil connected to a corresponding set terminal 150-2S through 150-12S and the reset side of its coil connected to a corresponding reset

terminal 150-2R through 150-12R. Within function memory 22, input terminal 138-01 is connected to the anodes of 12 diodes 152-1 through 152-12. The cathode of diode 152-1 is connected through terminal 150-1S to the set side of the coil of magnetic latching reed relay 150-1. The cathodes of diodes 152-2 through 152-12 are connected through terminals 150-2R through 150-12R, respectively, to the reset side of the coils of relays 150-2 through 150-12 respectively. Thus, when a signal is applied to terminal 138-01, relay 150-1 is set and relays 150-2 through 150-12 are reset.

In like manner, input terminal 138-02 is connected through a set of 12 diodes to terminal 150-2S, terminal 150-1R and to terminals 150-3R through 150-12R; input terminal 138-03 is coupled through a set of 12 diodes to terminal 150-3S and to terminals 150-1R, 150-2R, and 150-4R through 150-12R; and each of the other input terminals 138-04 through 138-12 is likewise coupled through an associated set of diodes to the set side of the coil of the corresponding relay 150-4 through 150-12 and to the reset side of the coils of all other relays within function memory 22.

Each of the relays 150-1 through 150-12 has its first contact connected to a source of excitation such as battery 154. The second contact of each relay 150-1 through 150-12 is provided as an output from function memory 22. As seen in FIG. 1, these outputs are applied through function steering circuit 24, which, by way of example, can comprise a diode matrix, to power switching unit 26, which might be a series of power triacs or relays. Power switching unit 26 applies power to signal lamps 28 at the street intersection.

With timing selector 20 in its static condition in which one of the magnetic latching reed relays 140-0 through 140-9 is set in each of the time selection circuits 130, 132, and 134, whenever clock 18 indicates the time at which a function is to be initiated, the associated AND gate 136-1 through 136-12 applies a signal through the associated terminals 138-01 through 138-12 and the associated diode set 152 to set the associated magnetic latching reed relay 150-1 through 150-12 and to reset all the other relays 150-1 through 150-12. The magnets of the relays 150-1 through 150-12 maintain the relays in the condition in which they have been placed by the signal from the terminal 138-01 through 138-12 after that signal ends. Power from source 154 is then applied through the function output line of the one relay 152-1 through 152-12 which is in its set condition to function steering circuit 24. In function steering circuit 24, the power is gated to the power switching devices within power switching unit 26 that control the signal lamps which are to be energized for that function. Thus, by way of example, if local controller 14 is provided at an intersection of two streets requiring only four functions, then the function one signal from function memory 22 might be gated by function steering unit 24 to power control devices within power switching unit 26 that control the street A right-of-way indicator and the street B stop indicator; function two might be gated to power control devices controlling the power to the street A clearance indicator and the street B stop indicator; function three might be gated to devices controlling power for the street B right-of-way indicator and the street A stop indicator; and function four gated to devices controlling the power for the street B clearance indicator and the

street A stop indicator. If local controller 14 is at an intersection requiring more functions, for example, the twelve functions of FIGS. 2-6, then function steering circuit 24 includes a more complex gating capability.

Central controller 10 can be any device capable of providing the necessary tone signals to the local controllers 14. Thus, for example, central controller 10 can be a plurality of tone generators of the desired frequencies under the control of or incorporated within a digital computer or a master programmer. Since commands from central controller 10 are required only when the cycle of a local controller is to be altered, these commands might be necessary only at infrequent intervals, for example, four times a day. Generally, the traffic patterns of different days are similar, and so the same sequence of commands may be utilized each day. Accordingly, it is not necessary that a digital computer be incorporated into the central controller 10. Instead, central controller 10 can include a tape recording of the tone sequences within the more frequently utilized command programs with this tape recording played on line 12 to the local controllers 14 to alter cycles of the local controllers as desired. Several programs of such tone sequences can be recorded on individual tape cassettes with the desired cassette selected to change the program as needed. Alternatively, a single cassette with two-track tape can be utilized, one track having tone sequences recorded thereon and the second track having index numbers. The tones pertaining to a particular local controller 14 can be recorded sequentially if desired. Alternatively, the tone one through tone seven signals can be recorded in parallel or multiplexed and transmitted as one signal, followed by a tone eight signal to terminate operation of tone filter and decoder 16 for a particular location. Tone generators controlled by a patch panel can be utilized with the desired sequence of tones "programmed" into the patch panel prior to activation of the programmer so that the series of tone commands transmitted is determined by the patch panel arrangement.

The number of commands which it is necessary for central controller 10 to transmit to a local controller 14 can be reduced by having some of the function initiation times internally generated within the local controller. Thus, for example, the clearance intervals can be of a fixed duration, and so their generation and timing can be solely accomplished within each local controller 14 without the need for commands from central controller 10. In addition to reducing the number of commands which must be transmitted, this technique also reduces the number of sets of time selection circuitry 130, 132, and 134 which are required. FIG. 7 depicts one manner in which the time of initiation of some functions can be done with the local controller and with no distinct command from central controller 10 for such functions. Using this circuitry to accommodate clearance intervals, central controller 10 applies to the local controller a number of initiation time commands equal to the number of right-of-way intervals, either vehicular or pedestrian, which are to be provided at the intersection at which the local controller is operating. Preferably, each initiation time transmitted by central controller 10 is the initiation time of the clearance interval preceding the associated right-of-way interval. Thus, for example, if the local controller is to be utilized at an intersection of two streets for which only four functions are required, then the time of initiation

of the street A right-of-way interval is determined by a command from central controller 10 indicating the time of initiation of the street B clearance interval and by the circuitry of FIG. 7, and likewise the time of initiation of the street B right-of-way interval is determined by a command from central controller 10 indicating the time of initiation of the street A clearance interval and by the circuitry of FIG. 7.

As seen in FIG. 7, AND gate 136-1, which is within timing selector 20 of FIG. 4, has its output connected to the set input of bistable multivibrator of flip-flop 160 rather than to terminal 138-01. The one output of flip-flop 160 is connected to the first input of AND gate 162 which has its second input connected to the output of frequency dividing circuit 110 within clock 18 to receive the one pulse per second signal therefrom. The output of gate 162 is connected to the input of decade counter 164. Output terminal 138-01 of timing selector 20 is connected to the output terminal of decade counter 164 corresponding to the duration of the phase B clearance interval, illustratively depicted in FIG. 7 as the five output of decade counter 164 to provide a clearance interval of a five second duration. That same output of decade counter 164 is connected to the clear input of flip-flop 160 and to reset decade counter 164. If the local controller is at a two-street intersection requiring four functions, the output of AND gate 136-1 is also connected to output terminal 138-04 of timing selector 20 to provide the signal to initiate the street B clearance interval. Unit-selection circuit 130-01, 10-selection circuit 132-01, and hundred-selection circuit 134-01 are set to the time at which the street B clearance interval is to be initiated. When clock 18 indicates that time, a signal from AND gate 136-1 is applied through 138-04 to function memory 22 of FIG. 6 to initiate that clearance interval signal. This signal from AND gate 136-1 also sets flip-flop 160 which enables AND gate 162 to pass the one-pulse-per-second signals from dividing circuit 110 to decade counter 164. After five seconds a signal on the five output of decade counter 164 clears flip-flop 160 and passes through terminal 138-01 to function memory 22 to initiate the street A right-of-way interval signal. Accordingly, the street B clearance interval is of a duration determined by the selected output of decade counter 164, while the duration of the street A right-of-way interval can be adjusted by altering the time to which time selection circuits 130-01, 132-01, and 134-01 are set. A similar set of circuitry can be utilized for the other clearance intervals to be provided by the local controller. When the local controller is used at an intersection requiring additional clearance intervals, then, of course, additional sets of such circuitry are utilized. The connection from the selected output of decade counter 164 to terminal 138-01 and the clear input of flip-flop 160 can be hard wired or through a patch plug, since this connection is generally fixed for a particular street intersection and would seldom be changed.

FIGS. 1 and 2 illustrate the system of the present invention utilizing frequency coded signals for transmitting interval initiation commands from central controller 10 to each local controller 12. Other types of coded signals could be utilized to convey these commands to the local controllers for storage within the non-volatile memories therein. Thus, by way of illustration, rather than frequency coded signals, pulse coded signals could be utilized with, for example, a first signal portion or

characteristic conveying the signal one through signal eight designation and a second signal portion or characteristic conveying the signal information. Additionally, it is not necessary that the connection from central controller 10 to local controllers 14 be by wire. For example, radio communication would likewise be suitable. A single channel of communication is all that is required.

To provide a simplified traffic control system without non-volatile memory, clock 18, timing selector 20 and, optionally, function memory 22 can be omitted, along with tone filters 52-56 and decade counters 76-80 of tone filter and decoder 16. In such instance the 12 function number outputs from AND gates 100-01 through 100-12 are connected to function memory circuitry or directly to function steering circuitry. This can be function memory circuit 22 depicted in FIG. 6, with output terminals 102-01 through 102-12 connected to input terminals 138-01 through 138-12 of FIG. 6. In such a case, when it is desired to initiate a new function at a particular local controller, the local controller is addressed by a pulse of its tone one frequency, the function number is transmitted as pulses of tone two and tone three signal, and the system is shut off by a pulse of tone eight signal. It would then be possible to apply output terminal 96 from tone filter 46 as an additional input to each AND gate 100-01 through 100-12 so that upon receipt of the tone eight signal the number of the function to be initiated would be transmitted from the associated gate 100-01 through 100-12 while capacitor 98 is charging. This would avoid spurious outputs due to noise or due to stepping of decade counters 72 and 74 at each function change. As an alternative, AND gates 100-01 through 100-12 can have their outputs connected to function steering circuits such as function steering logic 170 depicted in detail in FIG. 6 of United States patent application serial number 863,309, filed Oct. 2, 1969 now U. S. Pat. No. 3,065,084. In this event output terminal 96 of tone filter 46 is not utilized and decade counter 72 and 74 of the present application provide the continuous signals required to maintain energized the solid state switches 172-182 of FIG. 6 in said U. S. Pat. No. 3,065,084.

The latching reed relays depicted in FIGS. 2, 5 and 6 are but one device which could be utilized in the present invention. Other possible devices include magnetic cores and stepping switches which do not require continuous power to maintain a pre-set state. The decade counters could be replaced by ring counters or shift registers or by other suitable counters. Numerous other component interchanges could be made.

It can thus be seen that the present invention provides a versatile traffic control system, including a traffic control system utilizing non-volatile memories within local controllers to permit those local controllers to operate for extended periods of time independent of central control and with no deterioration in programming caused by local or area-wide power failure and yet capable of having the cycles of the local controllers altered as desired by means of commands sent to every local controller over a single transmission channel. Although the present invention has been described with reference to preferred embodiments, numerous alterations and rearrangements could be made, and still the result would be within the scope of the invention.

What is claimed is:

1. A traffic controller responsive to receipt from a central traffic control signal source of relative initiation-time signals and of function indication signals for generating a plurality of right-of-way function signals for steering to right-of-way indicators at street intersections to control right-of-way indications of the indicators, said traffic controller comprising:

a. clock means for cyclically generating timing signals including a local time zero signal indicative of a local time zero and local clock time signals indicative of time with respect to the local time zero;

b. input means adapted for connection to a central traffic control signal source for receipt of coded signals therefrom, said input means including:

1. first switching means including (i) a first terminal adapted for connection to a source of power and (ii) a second terminal, the first switching means responsive to a first received coded signal of a first characteristic, for applying power from the source through the first terminal to the second terminal;

2. second switching means connected to the first switching means second terminal and, while source power is applied to the first switching means second terminal, responsive to a second received coded signal of a second characteristic for generating a function number signal indicated by the second received coded signal and denoting a particular one of the plurality of right-of-way function signals;

3. third switching means connected to the first switching means second terminal and, while source power is applied to the first switching means second terminal, responsive to a third received coded signal of a third characteristic for generating a function initiation time signal indicated by the third received coded signal and denoting the time relative to local time zero at which a right-of-way function signal is to be initiated; and

4. fourth switching means connected to the first switching means second terminal and, while source power is applied to the first switching means second terminal, responsive to a fourth received coded signal of a fourth characteristic for removing source power from the first switching means second terminal;

c. function time selector means including a selection circuit uniquely associated with each of the plurality of right-of-way function signals to be generated by the traffic controller, each selection circuit including:

1. function time memory means connected to the second switching means for receipt therefrom of a function number signal uniquely corresponding with the associated right-of-way function signal, the function time memory means further connected to the third switching means for receipt of a function initiation time signal therefrom, the function time memory means responsive to receipt of the associated function number signal for storing as a function initiation time the time represented by the function initiation time signal; and

2. function initiation means connected to the clock means and to the associated function time memory means and responsive to receipt from said

clock means of a timing signal corresponding with the function initiation time stored in the associated function time memory means for generating a function initiation signal; and

- d. function memory means connected to the function timing selector means for receipt of function initiation signals therefrom and adapted for connection to function steering circuitry, the function memory means responsive to receipt of each function initiation signal for generating an associated right-of-way function signal and terminating any other pre-existing right-of-way function signals.

2. A traffic controller as claimed in claim 1 in which the second switching means includes receiving means for receiving from a central traffic control signal source pulses of the second coded signal and counting means connected to the receiving means for providing as an output a function number signal indicative of the number of received pulses of the second coded signal.

3. A traffic controller as claimed in claim 1 in which the third switching means includes first receiving means for receiving from a central traffic control signal source pulses of the third coded signal and first counting means connected to the first receiving means for providing as an output a function initiation time signal indicative of the number of received pulses of the third coded signal.

4. A traffic controller as claimed in claim 3 in which the second switching means includes second receiving means for receiving from the central traffic control signal source pulses of the second coded signal and second counting means connected to the second receiving means for providing as an output a function number signal indicative of the number of received pulses of the second coded signal.

5. A traffic controller as claimed in claim 4 in which:

- a. the first counting means includes a first plurality of output lines, the first counting means providing each distinct function initiation time signal on a uniquely associated combination of the output lines;
- b. the clock means includes pulse generating means for generating one-pulse-per-second timing pulses and third counting means having a first plurality of output lines for counting the timing pulses and providing an indication thereof, with each distinct indication provided on a uniquely associated combination of third counting means output lines;
- c. each function time memory means comprises a non-volatile memory having a first plurality of memory storage locations, each memory storage location coupled to a unique one of the first counting means output lines, each memory storage location in response to receipt of a function initiation time signal on the associated first counting means output line assuming a first memory state and in response to receipt of a function initiation time signal on a non-associated first counting means output line assuming a second memory state; and
- d. each function initiation means comprising a first plurality of signal switching means, one of said signal switching means uniquely associated with each memory storage location, each signal switching means connected to a uniquely associated third counting means output line, each signal switching means in response to the associated memory stor-

age location being in the first memory state assuming a first switching state providing a function initiation signal path from the associated third counting means output line to the function memory means and in response to the associated memory storage location being in the second memory state assuming a second switching state interrupting the function initiation signal path.

6. A traffic controller as claimed in claim 5 in which at least some of the function initiation means further comprise:

- e. bistable switching means connected to the associated first plurality of signal switching means to assume a first stable state in response to a function initiation signal from the associated function initiation means;
- f. gated pulse counting means connected to the clock means pulse generating means and to the bistable switching means for counting timing pulses when the bistable switching means is in its first stable state and for applying to the function memory means a further function initiation signal in response to counting by the gated pulse counting means of a preset number of timing pulses; and
- g. connecting means connected the gated pulse generating means to the bistable switching means for causing the bistable switching means to assume a second stable state in response to the generation of an associated further function initiation signal.

7. A traffic controller as claimed in claim 5 in which the pulse counting means comprises a plurality of cascaded decade counters.

8. A traffic controller as claimed in claim 1 in which: the first switching means includes a first frequency sensitive switching means responsive to a first tone signal of a first frequency;

the second switching means includes a second frequency sensitive switching means responsive to a second tone signal of a second frequency;

the third switching means includes a third frequency sensitive switching means responsive to a third tone signal of a third frequency; and

the fourth switching means includes a fourth frequency sensitive switching means responsive to a fourth tone signal of a fourth frequency.

9. A traffic controller as claimed in claim 8 in which the second frequency sensitive switching means includes receiving means for receiving from a central traffic control signal source pulses of the second tone signal and counting means connected to the receiving means for providing as an output a function number signal indicative of the number of received pulses of the second tone signal.

10. A traffic controller as claimed in claim 8 in which the third frequency sensitive switching means includes first receiving means for receiving from a central traffic control signal source pulses of the third tone signal and first counting means connected to the first receiving means for providing as an output a function initiation time signal indicative of the number of received pulses of the third tone signal.

11. A traffic controller as claimed in claim 10 in which the second frequency sensitive switching means includes second receiving means for receiving from the central traffic control signal source pulses of the second tone signal and second counting means connected to the second receiving means for providing as an out-

put a function number signal indicative of the number of received pulses of the second tone signal.

12. A traffic controller as claimed in claim 1 in which the clock means includes pulse generating means for generating timing pulses and pulse counting means for counting the timing pulses.

13. A traffic controller as claimed in claim 12 in which the pulse counting means comprises a plurality of cascaded decade counters.

14. A traffic controller as claimed in claim 13 in which each function time memory means comprises non-volatile memory means.

15. A traffic controller as claimed in claim 1 further comprising function steering means connected to the function memory means and adapted for connection to right-of-way indicators for applying energizing signals to right-of-way indicators in response to right-of-way function signals.

16. A traffic controller as claimed in claim 15 further comprising power switching means connected to the function steering means and adapted for connection to right-of-way indicators for switching power to right-of-way indicators in response to energizing signals from the function steering means.

17. A traffic controller as claimed in claim 16 further comprising right-of-way indicators connected to the power switching means for providing right-of-way indications in response to power from the power switching means.

18. A traffic controller as claimed in claim 1 further comprising a central traffic control signal source connected to the input means for application of coded signals thereto.

19. A traffic controller as claimed in claim 18 in which the central traffic control signal source includes a digital computer.

20. A traffic controller as claimed in claim 18 in which the central traffic control signal source includes a tape recording of coded signals.

21. A traffic controller as claimed in claim 1 in which at least some of the function initiation means include: bistable switching means responsive to generation by the associated function initiation means of a function initiation signal for assuming a first stable state;

gated time monitoring means connected to the clock means and to the bistable switching means for monitoring local clock time signals when the bistable switching means is in its first stable state and responsive to the monitoring of a preset local clock time signal for applying to the function memory means a further function initiation signal; and

connecting means connecting the gated time monitoring means to the bistable switching means and responsive to the generation of an associated further function initiation signal for causing the bistable switching means to assume a second stable state.

22. A traffic controller as claimed in claim 1 in which the input means further includes fifth switching means connected to said clock means and, while source power is applied to the first switching means second terminal, responsive to a fifth received coded signal of a fifth characteristic for applying a synchronizing signal to said clock means to reset said clock means.

23. A traffic controller responsive to receipt from a central traffic control signal source of real time signals

commanding initiation of right-of-way functions for generating a plurality of right-of-way function signals for steering to right-of-way indicators at street intersections to control right-of-way indications of the indicators, said traffic controller comprising:

a. input means adapted for connecting to a central traffic control signal source for receipt of coded signals therefrom;

b. first switching means connected to the input means and including (i) a first terminal adapted for connection to a source of power and (ii) a second terminal, said first switching means responsive to receipt by the input means of a first coded signal of a first characteristic for applying power from the source through the first terminal to the second terminal;

c. second switching means connected to the input means and to the first switching means second terminal and, while source power is applied to the first switching means second terminal, responsive to receipt by the input means of a second coded signal of a second characteristic for generating a function number signal indicated by the second received coded signal and denoting a particular one of the plurality of right-of-way function signals;

d. third switching means connected to the input means and to the first switching means second terminal and, while source power is applied to the first switching means second terminal, responsive to receipt by the input means of a third coded signal of a third characteristic for removing source power from the first switch means second terminal; and

e. function memory means connected to the second switching means for receipt of function number signals therefrom and adapted for connection to function steering circuitry, the function memory means responsive to receipt of each function number signal for generating an associated right-of-way function signal and terminating any other pre-existing right-of-way function signals.

24. A traffic controller as claimed in claim 23 in which the second switching means includes receiving means for receiving from a central traffic control signal source pulses of the second coded signal and counting means connected to the receiving means for providing as an output a function number signal indicative of the number of received pulses of the second coded signal.

25. A traffic controller as claimed in claim 23 in which:

the first switching means comprises a first frequency sensitive switching means responsive to a first tone signal of a first frequency;

the second switching means comprises a second frequency sensitive switching means responsive to a second tone signal of a second frequency; and

the third switching means comprises a third frequency sensitive switching means responsive to a third tone signal of a third frequency.

26. A traffic controller as claimed in claim 25 in which the second frequency sensitive switching means includes receiving means for receiving from a central traffic control signal source pulses of the second tone signal and counting means connected to the receiving means for providing as an output a function number signal indicative of the number of received pulses of the second tone signal.

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27. A traffic controller as claimed in claim 23 further comprising function steering means connected to the function memory means and adapted for connection to right-of-way indicators for applying energizing signals to right-of-way indicators in response to right-of-way function signals.

28. A traffic controller as claimed in claim 27 further comprising power switching means connected to the function steering means and adapted for connection to right-of-way indicators for switching power to right-of-way indicators in response to energizing signals from the function steering means.

29. A traffic controller as claimed in claim 28 further comprising right-of-way indicators connected to the

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power switching means for providing right-of-way indications in response to power from the power switching means.

30. A traffic controller as claimed in claim 23 further comprising a central traffic control signal source connected to the input means for application of coded signals thereto.

31. A traffic controller as claimed in claim 30 in which the central traffic control signal source includes a digital computer.

32. A traffic controller as claimed in claim 30 in which the central traffic control signal source includes a tape recording of coded signals.

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