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(54) **Title**: SWITCHING METHOD FOR SWITCHED-MODE POWER CONVERTERS EMPLOYING A BRIDGE TOPOLOGY

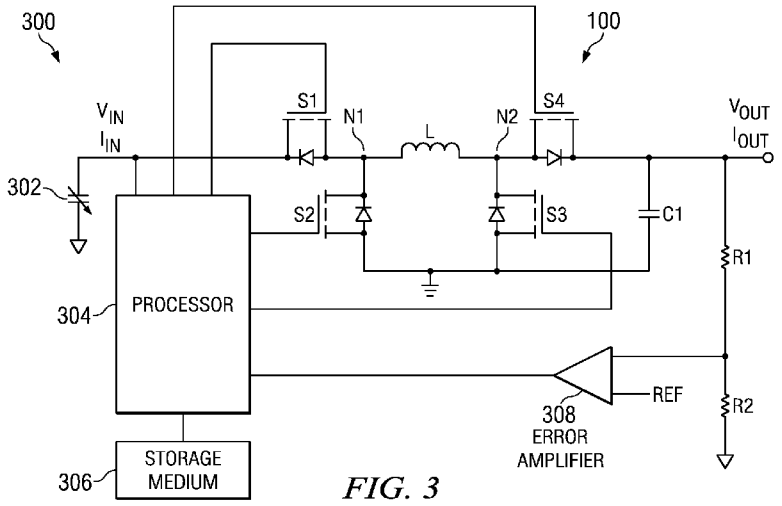

FIG. 3

(57) **Abstract**: Control circuitry (voltage divider (R1, R2), error amplifier 308, processor 304 and storage medium 306) is coupled to input/output terminals for control of a buck-boost switching regulator. The control circuitry uses a compensation function to determine pulse width modulation (PWM) duty cycles for the switching regulator. The switching regulator is controlled to operate in a buck mode when an output of the compensation function is less than the predetermined buck gain; to operate in a bridge mode when the output of the compensation function is between the predetermined buck gain and the predetermined boost gain; and to operate in a boost mode when the output of the compensation function is greater than the predetermined boost gain.

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SWITCHING METHOD FOR SWITCHED-MODE POWER CONVERTERS EMPLOYING A BRIDGE TOPOLOGY

[0001] The invention relates generally to power converters and, more particularly, to power converters using a bridge topology.

BACKGROUND

[0002] There are a number of applications that may need a switching regulator or switched mode power supply to operate in non-inverting buck or boost modes, transitioning relatively seamlessly between the two. Turning to FIG. 1, an example of a bridge 100, which can operate in boost and buck modes can be seen. This bridge 100 is generally an H-bridge, using switches S1 to S4, and an inductor L, which is coupled between the switching nodes of the H-bridge. In buck mode, switches S4 and S3 are closed and open, respectively, while pulse width modulation (PWM) signals are provided to switches S1 and S2. Alternatively, in boost mode, switches S1 and S2 are closed and open, respectively, while PWM signals are provided to switches S3 and S4.

[0003] A problem with bridge 100, however, is that there are some practical constraints that limit the ability to seamlessly transition between the buck and boost modes, namely, on-time and dead-time. Looking to buck mode, for example, switch S1 (or S2) cannot seamlessly reach 100% duty cycle. As can be seen in FIG. 2, switch S2, for example, has a minimum on-time T_{ON} (which is generally dictated by the physics of switch S2), and there is a dead-time T_{DEAD} between a rising/falling edge of the PWM signal for switch S1 and the falling/rising edge of the PWM signal for switch S2. If the total on-time for switch S1 (for example) for a fixed frequency of 1/T (duty cycle in buck mode D_{BU} times the period T) is greater than the period T minus this predetermined constraint period ($D_{BU}*T>T-2T_{DEAD}-T_{ON}$), then the gain ($V_{OUT}/V_{IN}$) of the regulator can deviate from an expected value.

[0004] Some other conventional circuits are described in U.S. Patent Nos. 6,166,527 and 6,037,755 and in U.S. Patent Publ. No. 2009/0039852.

SUMMARY

[0005] An example embodiment of the invention, accordingly, provides an improved switching regulator apparatus. The apparatus comprises a buck-boost switching regulator having an input terminal, an output terminal, a predetermined buck gain, a predetermined boost gain, a predetermined dead-time, and a predetermined on-time; and control circuitry that is coupled to at least one of the output terminal and the input terminal and that controls the buck-boost switching regulator, wherein the control circuitry employs a compensation function to determine pulse width modulation (PWM) duty cycles for the buck-boost switching regulator, wherein the control circuitry includes a processor and a storage medium with a computer program product embodied thereon, and wherein the computer program product includes: computer code for operating the buck-boost switching regulator in a buck mode when an output of the compensation function is less than the predetermined buck gain; computer code for operating the buck-boost switching regulator in the bridge mode when the output of the compensation function is between the predetermined buck gain and the predetermined boost gain; and computer code for operating the buck-boost switching regulator in a boost mode when the output of the compensation function is greater than the predetermined boost gain.

[0006] In accordance with an example embodiment of the invention, the computer code for operating the buck-boost switching regulator in the bridge mode when the output of the compensation function is between the predetermined buck gain and the predetermined boost gain further comprises: computer code for operating the buck-boost switching regulator in a first bridge mode when the output of the compensation function is between the predetermined buck gain and an intermediate value; and computer code for operating the buck-boost switching regulator in a second bridge mode when the output of the compensation function is between the intermediate value and the predetermined boost gain.

[0007] In accordance with an example embodiment of the invention, the buck-boost switching regulator further comprises: a first switch that is coupled between the input terminal and a first switching node; a second switching that is coupled between the first switching node and ground; an inductor that is coupled between the first switching node and a second switching

node; a third switch that is coupled between the second switching node and ground; and a fourth switching that is coupled between the second switching node and the output terminal.

[0008] In accordance with an example embodiment of the invention, the computer code for operating the buck-boost switching regulator in the first bridge mode when the output of the compensation function is between the predetermined buck gain and the intermediate value further comprises: computer code for operating the first switch at a first duty cycle having a value that is the difference between the output of the compensation function and a first constant value; and computer code for operating the third switch at a second duty cycle that is a second constant value, wherein a gain of buck-boost switching regulator, in the first bridge mode, is the product of a third constant and the value of the first duty cycle.

[0009] In accordance with an example embodiment of the invention, the computer code for operating the buck-boost switching regulator in the second bridge mode when the output of the compensation function is between the intermediate value and the predetermined boost gain further comprises: computer code for operating the first switch at a third duty cycle having a fourth constant value; and computer code for operating the third switch at a fourth duty cycle having a value that is the difference between the output of the compensation function and a fifth constant value, wherein a gain of the buck-boost switching regulator, in the second bridge mode, is the product of the fourth constant value and a difference between a sixth constant value and the output of the compensation function.

[0010] In accordance with an example embodiment of the invention, the control circuitry further comprises: a voltage divider that is coupled to the output terminal; and an error amplifier that receives a reference voltage and that is coupled to the voltage divider and the processor.

[0011] In accordance with an example embodiment of the invention, the processor is a digital signal processor (DSP).

[0012] In accordance with an example embodiment of the invention, a method is provided. The method comprises detecting at least one of an input voltage, an output voltage, an input current, and an output current of a buck-boost switching regulator, wherein buck-boost switching regulator includes a predetermined buck gain, a predetermined boost gain, a predetermined dead-time, and a predetermined on-time, and wherein the buck-boost switching regulator includes: a first switch that is coupled between the input terminal and a first switching node; a second switching that is coupled between the first switching node and ground; an inductor that is

coupled between the first switching node and a second switching node; a third switch that is coupled between the second switching node and ground; and a fourth switching that is coupled between the second switching node and the output terminal; operating the buck-boost switching regulator in a buck mode when an output of the compensation function is less than the predetermined buck gain; operating the buck-boost switching regulator in a first bridge mode when the output of the compensation function is between the predetermined buck gain and an intermediate value; operating the buck-boost switching regulator in a second bridge mode when the output of the compensation function is between the intermediate value and the predetermined boost gain; and operating the buck-boost switching regulator in a boost mode when the output of the compensation function is greater than the predetermined boost gain.

[0013] In accordance with an example embodiment of the invention, the step of operating the buck-boost switching regulator in the first bridge mode when the output of the compensation function is between the predetermined buck gain and the intermediate value further comprises: operating the first switch at a first duty cycle having a value that is the difference between the output of the compensation function and a first constant value; and operating the third switch at a second duty cycle that is a second constant value, wherein a gain of buck-boost switching regulator, in the first bridge mode, is the product of a third constant value and the value of the first duty cycle.

[0014] In accordance with an example embodiment of the invention, the step of operating the buck-boost switching regulator in the second bridge mode when the output of the compensation function is between the intermediate value and the predetermined boost gain further comprises: operating the first switch at a third duty cycle having a fourth constant value; and operating the third switch at a fourth duty cycle having a value that is the difference between the output of the compensation function and a fifth constant value, wherein a gain of the buck-boost switching regulator, in the second bridge mode, is the product of the fourth constant value and a difference between a sixth constant value and the output of the compensation function.

[0015] In accordance with an example embodiment of the invention, an apparatus is provided. The apparatus comprises a solar cell; a buck-boost switching regulator having an input terminal, an output terminal, a predetermined buck gain, a predetermined boost gain, a predetermined dead-time, and a predetermined on-time, wherein the input terminal is coupled to the solar cell; and control circuitry that is coupled to the output terminal and that controls the

buck-boost switching regulator, wherein the control circuitry employs a compensation function to determine PWM duty cycles for the buck-boost switching regulator, wherein the control circuitry includes a processor and a storage medium with a computer program product embodied thereon, and wherein the computer program product includes: computer code for operating the buck-boost switching regulator in a buck mode when an output of the compensation function is less than the predetermined buck gain; computer code for operating the buck-boost switching regulator in a first bridge mode when the output of the compensation function is between the predetermined buck gain and an intermediate value; computer code for operating the buck-boost switching regulator in a second bridge mode when the output of the compensation function is between the intermediate value and the predetermined boost gain; and computer code for operating the buck-boost switching regulator in a boost mode when the output of the compensation function is greater than the predetermined boost gain.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] Example embodiments are described with reference to accompanying drawings, wherein:

FIG. 1 is a circuit diagram of a conventional bridge;

FIG. 2 is a timing diagram illustrating constraints of operation of the bridge of FIG. 1; and

FIG. 3 is an example of a system in accordance with an example embodiment of the invention.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0017] FIG. 3 illustrates a system 300 in accordance with an example embodiment of the invention. System 100 generally comprises a bridge 100, solar cell 302, capacitor C1, voltage divider (resistors R1 and R2), error amplifier 308, processor 304, and storage medium 306. Collectively, the voltage divider (R1, R2), error amplifier 308, processor 304, and storage medium 306 generally operate as a control circuitry, while bridge 100 and capacitor C1 generally operate as a buck-boost switching regulator. In operation, an input voltage V_{IN} and input current I_{IN} are provide to the input terminal of the switching regulator from, for example, a solar cell 302 (which may include multiple solar cells coupled in series or parallel to the input terminal) so as to generate an output voltage V_{OUT} and an output current I_{OUT} at the output terminal. The control circuitry measures the output voltage V_{OUT} and the input voltage V_{IN} and generates the

appropriate PWM signals for switches S1 through S4. The error amplifier 308 compares an output from the voltage divider to a reference voltage REF so that the processor 304 can perform correction of the PWM signals. In an alternative arrangement, the error amplifier 308 and voltage divider can be removed, with the functionality being provided by the processor 304. In other alternative arrangements, input current I_{IN}, output current I_{OUT}, or input voltage V_{IN} may be used instead of the output voltage V_{OUT} for correction of the PWM signals. Additionally, the processor 304 may be a digital signals processor or DSP.

[0018] For conventional bridge switching or buck-boost operation, pairs of switches S1/S3 or S2/S4 are switched on and off at about the same time, and the duty cycle D_{BR} is the fraction of the cycle that that switches S1/S3 are on. This switching mode operates generally smoothly through a gain G (ratio of the output voltage V_{OUT} to the input voltage V_{IN}) of 1, but it also dissipates more power than either the buck mode or boost mode. The excessive power dissipation is generally due to there being four active switches (instead of two) and generally due to there being a higher average inductor current I_L than in either the buck mode ($I_L=I_{OUT}$) or boost mode ($I_L=I_{IN}$); namely, the average inductor current I_L is the sum of the input current I_{IN} and output current I_{OUT} ($I_L=I_{IN}+I_{OUT}$).

[0019] A reduction in this average inductor current I_L is possible, however. Assuming that the duty cycles of the buck (for switches S1 and S2) and boost (for switches S3 and S4) sides are independent and assuming that the buck duty cycle D_{BU} (or boost duty cycle D_{BO}) represents a fraction of the switching period T that switch S1 (or S3) is on, the gain G and inductor current IL can be represented as follows:

$$(1) \qquad G = \frac{V_{OUT}}{V_{IN}} = \frac{D_{BU}}{1 - D_{BO}}$$

$$(2) \qquad I_L = \frac{I_{IN} + I_{OUT}}{1 + D_{BU} - D_{BO}}$$

[0020] As shown, the gain G shows that there is a continuum of buck duty cycle D_{BU} and boost duty cycle D_{BO} combinations that will produce a gain G, so long as the relationship between buck duty cycle D_{BU} and boost duty cycle D_{BO} is obeyed (i.e., $D_{BU}=G(1-D_{BO})$). Additionally, it can be seen that a large buck duty cycle D_{BU} and a small boost duty cycle D_{BO} create a substantial reduction in inductor current I_L. Generally, control of the these duty cycles

D_{BU} and D_{BO} is performed or executed by processor 304 through the use of software or a computer program product that is embodied on the storage medium 306 (i.e., flash memory).

[0021] Each bridge (i.e., 100) generally has predetermined characteristics, such as a predetermined dead-time, a predetermined on-time, a predetermined maximum buck gain, and a predetermined minimum boost gain. Each of these characteristics generally contribute to the bridge operational modes; typically, two bridge modes are employed. When an output of a compensation function D (which is generated by processor 304 and used to determine PWM duty cycles) is less then the predetermined maximum buck gain, the switching regulator operates in buck mode, and when the output of the compensation function D is greater than the predetermined minimum boost gain, the switching regulator operates in boost mode. However, when the output of the compensation function D is between the predetermined maximum buck gain and a constant value, the switching regulator operates in an initial bridge mode, where:

(3) $D_{BU}=D-C_1$; and

(4) $D_{BO}=C_2$,

wherein C_1 and C_2 are constant values. Now, applying equations (1) and (2) to equations (3) and (4), the gain G and ratio of the inductor current I_L to the input current I_{IN} for the initial bridge mode are:

(5) $$G=\frac{D-C_1}{1-C_2}$$

(6) $$\frac{I_L}{I_{IN}}=\left(1+\frac{I_{OUT}}{I_{IN}}\right)\frac{1}{1+D-C_1-C_2}$$

[0022] Additionally, when the output of the compensation function D is between a constant value and the predetermined minimum boost gain, the switching regulator operates in an final bridge mode, where:

(7) $D_{BU}= C_3$; and

(8) $D_{BO}=D-C_4$,

wherein C_3 and C_4 are constant values. Now, applying equations (1) and (2) to equations (7) and (8), the gain G and ratio of the inductor current I_L to the input current I_{IN} for the final bridge mode are:

(9) $$G = \frac{C_3}{1 - D + C_4}$$

(10) $$\frac{I_L}{I_{IN}} = \left(1 + \frac{I_{OUT}}{I_{IN}}\right)\frac{1}{1 + C_3 - D + C_4}$$

[0023] In order to further illustrate the operation of bridge modes for system 300, it can be assumed for the sake of illustration for Table 1 that the switching period T, maximum buck gain, minimum boost gain, dead-time, and on-time are 4000ns, 0.9, 1.0292, 150ns, and 133ns, respectively.

Table 1

Mode	**D**	**D_{BU}**	**D_{BO}**	**G**	**I_L/I_{IN}**
Buck	D≤0.9	D	0	D_{BU}	$1/D_{BU}$
Initial Bridge	0.9<D<0.9292	D-0.0292	0.03333	1.0345(D-0.0292)	1/(D-0.0292)
Final Bridge	0.9292<D<1.0333	0.9	D-0.8958	0.9/(1.8958-D)	1.111
Boost	D>1.0333	1	D-1	1/D	1

[0024] In order to realize these bridge modes in processor 304 and storage medium 306, an algorithm is provided that adjusts the boost duty cycle D_{BO} and buck duty cycle D_{BU} in terms of a controller clock cycles (i.e., 1/60MHz=16.67ns). In Table 2 below, the gain G and ratio of the inductor current I_L to the input current I_{IN}, buck duty cycle D_{BU}, and boost duty cycle D_{BO} can be seen for an example of this algorithm.

Table 2

Mode	**D**	**D_{BU}**	**D_{BO}**	**G**	**I_L/I_{IN}**
Buck	210	210	0	0.875	1.143
Buck	211	211	0	0.879	1.137
Buck	212	212	0	0.883	1.132
Buck	213	213	0	0.888	1.127

Buck	214	214	0	0.892	1.121
Buck	215	215	0	0.896	1.116
Buck	216	216	0	0.900	1.111
Initial Bridge	217	210	8	0.905	1.143
Initial Bridge	218	211	8	0.909	1.137
Initial Bridge	219	212	8	0.914	1.132
Initial Bridge	220	213	8	0.918	1.127
Initial Bridge	221	214	8	0.922	1.121
Initial Bridge	222	215	8	0.927	1.116
Initial Bridge	223	216	8	0.931	1.111
Final Bridge	224	216	9	0.935	1.111
Final Bridge	225	216	10	0.939	1.111
Final Bridge	226	216	11	0.943	1.111
Final Bridge	227	216	12	0.947	1.111
Final Bridge	228	216	13	0.952	1.111
Final Bridge	229	216	14	0.956	1.111
Final Bridge	230	216	15	0.960	1.111
Final Bridge	231	216	16	0.964	1.111
Final Bridge	232	216	17	0.969	1.111
Final Bridge	233	216	18	0.973	1.111
Final Bridge	234	216	19	0.977	1.111
Final Bridge	235	216	20	0.982	1.111

Final Bridge	236	216	21	0.986	1.111
Final Bridge	237	216	21	0.986	1.111
Final Bridge	238	216	22	0.991	1.111
Final Bridge	239	216	23	0.995	1.111
Final Bridge	240	216	24	1.000	1.111
Final Bridge	241	216	25	1.005	1.111
Final Bridge	242	216	26	1.009	1.111
Final Bridge	243	216	27	1.014	1.111
Final Bridge	244	216	28	1.019	1.111
Final Bridge	245	216	29	1.024	1.111
Final Bridge	246	216	30	1.029	1.111
Final Bridge	247	216	31	1.033	1.111
Boost	248	240	8	1.034	1.000
Boost	249	240	9	1.034	1.000

[0025] As a result of this configuration, several advantages can be realized. First, there is a relatively seamless transition between buck mode and boost mode, which can be useful for solar applications, where input voltage and input current are generally inflexible. Additionally, the

average inductor current I_L can be reduced, which reduces power losses within the switching regulator.

[0026] Those skilled in the art to which the invention relates will appreciate that modifications may be made to the described example embodiments and other embodiments developed within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a buck-boost switching regulator having an input terminal, an output terminal, a predetermined buck gain, a predetermined boost gain, a predetermined dead-time, and a predetermined on-time; and

control circuitry that is coupled to at least one of the output terminal and the input terminal and that controls the buck-boost switching regulator;

wherein the control circuitry employs a compensation function to determine pulse width modulation (PWM) duty cycles for the buck-boost switching regulator;

wherein the control circuitry includes a processor and a storage medium with a computer program product embodied thereon, and

wherein the computer program product includes:

computer code for operating the buck-boost switching regulator in a buck mode when an output of the compensation function is less than the predetermined buck gain;

computer code for operating the buck-boost switching regulator in the bridge mode when the output of the compensation function is between the predetermined buck gain and the predetermined boost gain; and

computer code for operating the buck-boost switching regulator in a boost mode when the output of the compensation function is greater than the predetermined boost gain.

2. The apparatus of Claim 1, wherein the computer code for operating the buck-boost switching regulator in the bridge mode when the output of the compensation function is between the predetermined buck gain and the predetermined boost gain further comprises:

computer code for operating the buck-boost switching regulator in a first bridge mode when the output of the compensation function is between the predetermined buck gain and an intermediate value; and

computer code for operating the buck-boost switching regulator in a second bridge mode when the output of the compensation function is between the intermediate value and the predetermined boost gain.

3. The apparatus of Claim 2, wherein the buck-boost switching regulator further comprises:

a first switch that is coupled between the input terminal and a first switching node;

a second switching that is coupled between the first switching node and ground;

an inductor that is coupled between the first switching node and a second switching node;

a third switch that is coupled between the second switching node and ground; and

a fourth switching that is coupled between the second switching node and the output terminal.

4. The apparatus of Claim 3, wherein the computer code for operating the buck-boost switching regulator in the first bridge mode when the output of the compensation function is between the predetermined buck gain and the intermediate value further comprises:

computer code for operating the first switch at a first duty cycle having a value that is the difference between the output of the compensation function and a first constant value; and

computer code for operating the third switch at a second duty cycle that is a second constant value, wherein a gain of buck-boost switching regulator, in the first bridge mode, is the product of a third constant and the value of the first duty cycle.

5. The apparatus of Claim 4, wherein the computer code for operating the buck-boost switching regulator in the second bridge mode when the output of the compensation function is between the intermediate value and the predetermined boost gain further comprises:

computer code for operating the first switch at a third duty cycle having a fourth constant value; and

computer code for operating the third switch at a fourth duty cycle having a value that is the difference between the output of the compensation function and a fifth constant value, wherein a gain of the buck-boost switching regulator, in the second bridge mode, is the product of the fourth constant value and a difference between a sixth constant value and the output of the compensation function.

6. The apparatus of Claim 5, wherein the control circuitry further comprises:

a voltage divider that is coupled to the output terminal; and

an error amplifier that receives a reference voltage and that is coupled to the voltage divider and the processor.

7. The apparatus of Claim 5, wherein the processor is a digital signal processor (DSP).

8. A method comprising:

detecting at least one of an input voltage, an output voltage, an input current, and an output current of a buck-boost switching regulator; wherein the buck-boost switching regulator includes a predetermined buck gain, a predetermined boost gain, a predetermined dead-time, and a predetermined on-time; and wherein the buck-boost switching regulator includes:

a first switch that is coupled between the input terminal and a first switching node;

a second switch that is coupled between the first switching node and ground;

an inductor that is coupled between the first switching node and a second switching node;

a third switch that is coupled between the second switching node and ground; and

a fourth switch that is coupled between the second switching node and the output terminal;

operating the buck-boost switching regulator in a buck mode when an output of the compensation function is less than the predetermined buck gain;

operating the buck-boost switching regulator in a first bridge mode when the output of the compensation function is between the predetermined buck gain and an intermediate value;

operating the buck-boost switching regulator in a second bridge mode when the output of the compensation function is between the intermediate value and the predetermined boost gain; and

operating the buck-boost switching regulator in a boost mode when the output of the compensation function is greater than the predetermined boost gain.

9. An apparatus comprising:

a solar cell;

a buck-boost switching regulator having an input terminal, an output terminal, a predetermined buck gain, a predetermined boost gain, a predetermined dead-time, and a predetermined on-time, wherein the input terminal is coupled to the solar cell; and

control circuitry that is coupled to the output terminal and that controls the buck-boost switching regulator;

wherein the control circuitry employs a compensation function to determine PWM duty cycles for the buck-boost switching regulator; and

wherein the control circuitry includes a processor and a storage medium with a computer program product embodied thereon, and wherein the computer program product includes:

computer code for operating the buck-boost switching regulator in a buck mode when an output of the compensation function is less than the predetermined buck gain;

computer code for operating the buck-boost switching regulator in a first bridge mode when the output of the compensation function is between the predetermined buck gain and an intermediate value;

computer code for operating the buck-boost switching regulator in a second bridge mode when the output of the compensation function is between the intermediate value and the predetermined boost gain; and

computer code for operating the buck-boost switching regulator in a boost mode when the output of the compensation function is greater than the predetermined boost gain.

10. The apparatus of Claim 9, wherein the buck-boost switching regulator further comprises:

a first switch that is coupled between the input terminal and a first switching node;

a second switch that is coupled between the first switching node and ground;

an inductor that is coupled between the first switching node and a second switching node;

a third switch that is coupled between the second switching node and ground; and

a fourth switch that is coupled between the second switching node and the output terminal.

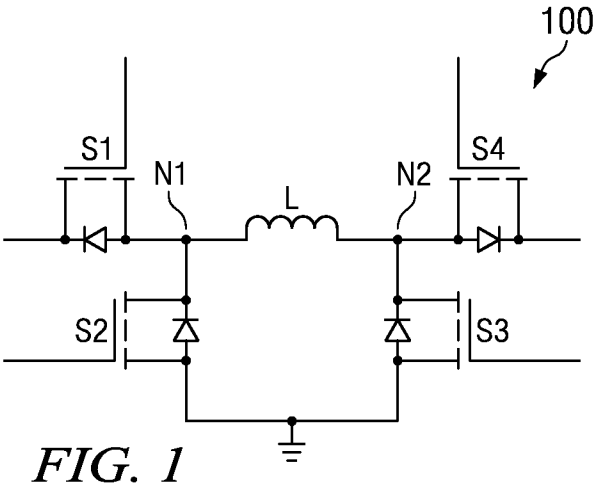

FIG. 1
(PRIOR ART)

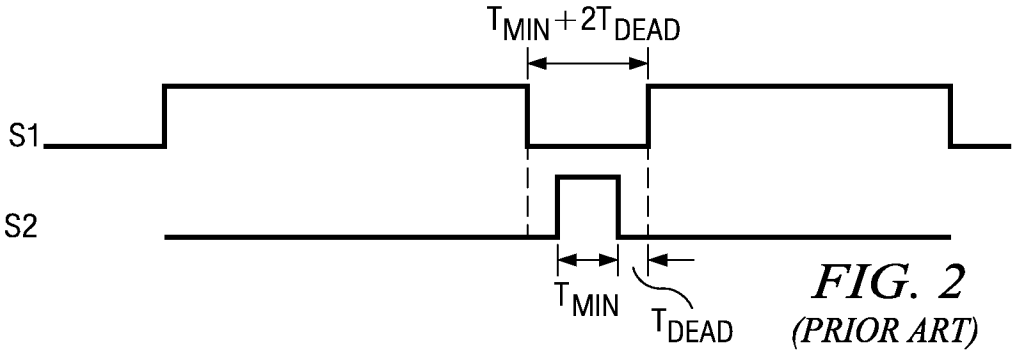

FIG. 2
(PRIOR ART)

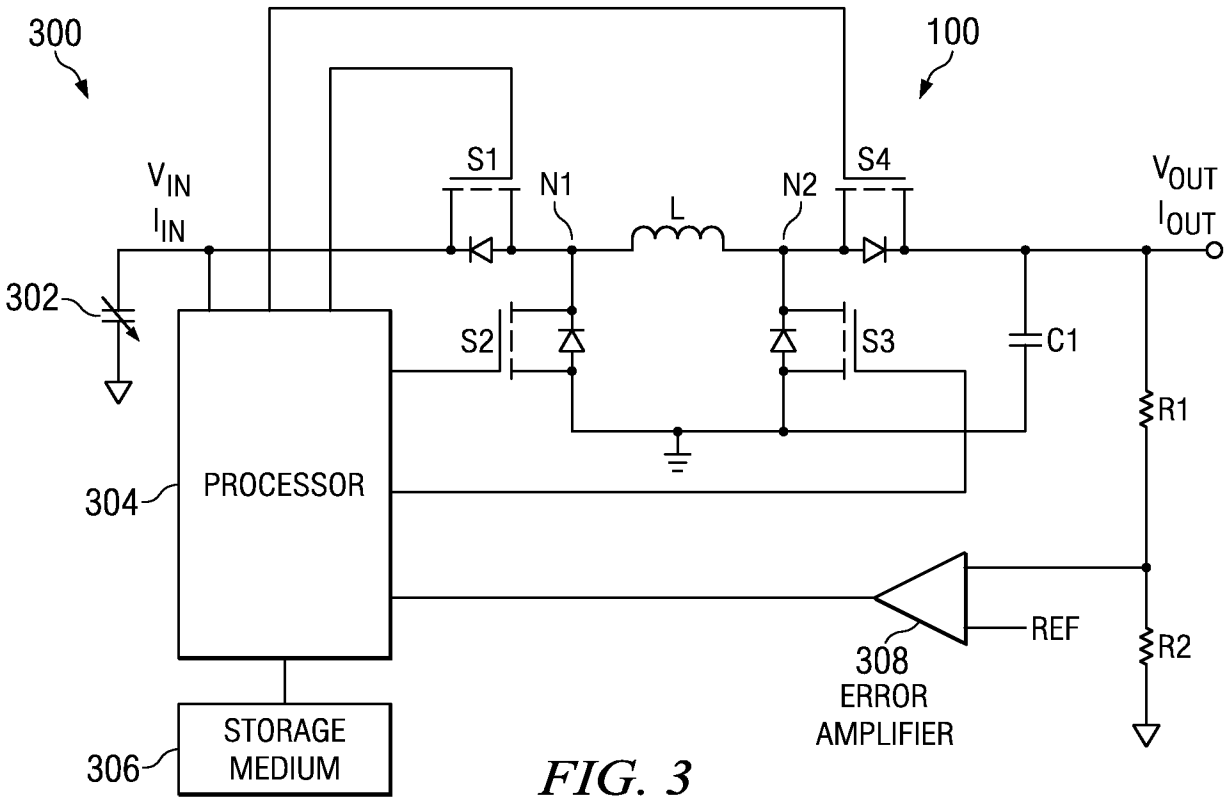

FIG. 3