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Miller

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[54] **ELECTRONIC KEY LOCK HAVING DATA CODED KEY**

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[73] Assignee: **Constellation Science and Technology Corporation,** Oxon Hill, Md.

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[21] Appl. No.: **106,835**

[52] **U.S. Cl.** .....**340/149 R,** 340/149 A
[51] **Int. Cl.** .....**H04q 3/00**
[58] **Field of Search** .....340/149, 149 A

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[57] **ABSTRACT**

An electronic key lock apparatus comprising a digitally coded key which is inserted into a lock apparatus. Upon insertion, the digital code on the key is read and compared with a predetermined digital code. If the code on the key matches the predetermined code, then an output is produced which, through a logic circuit, causes an output signal which will unlock the lock apparatus. If the code on the key does not match the predetermined code, then an unlock output will not be produced, and furthermore, the logic circuit will produce a reject signal which can be used to trigger an alarm device.

**10 Claims, 5 Drawing Figures**

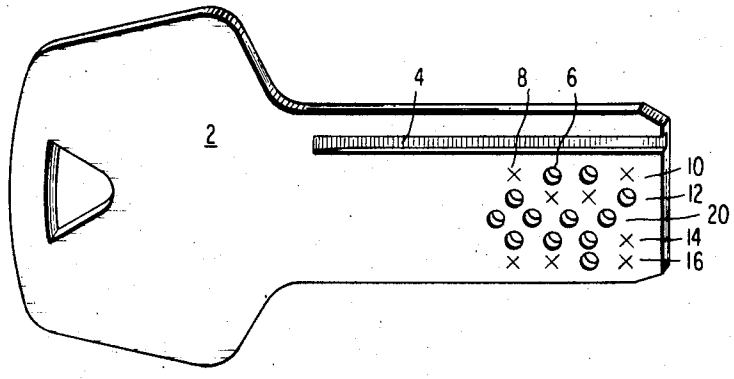
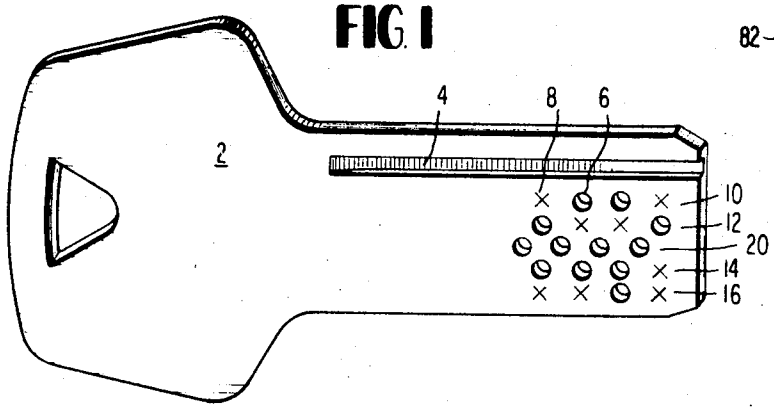


FIG. 1



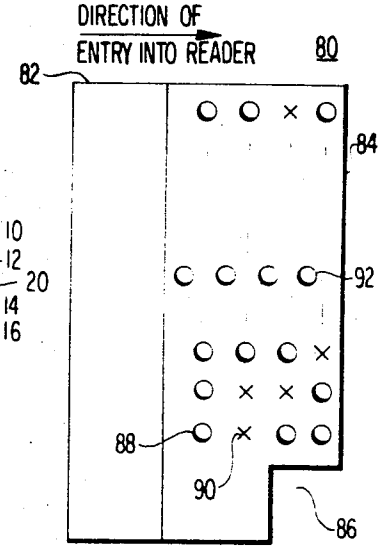




FIG. 5

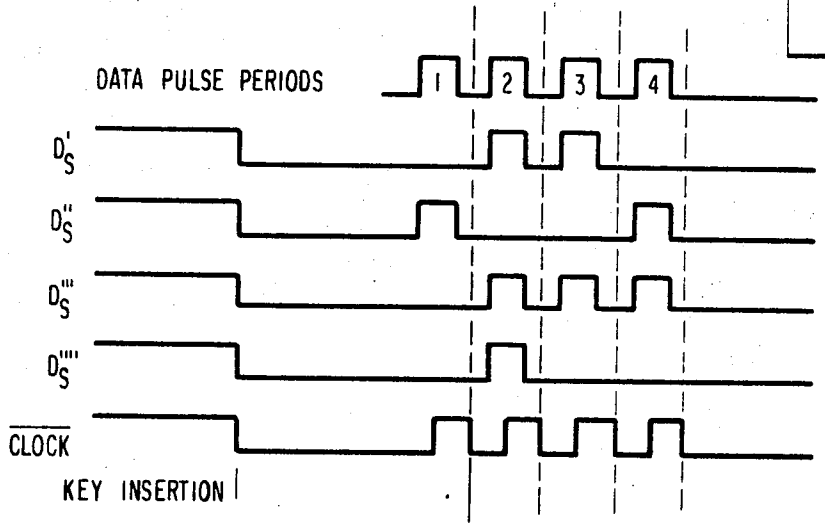



FIG. 3

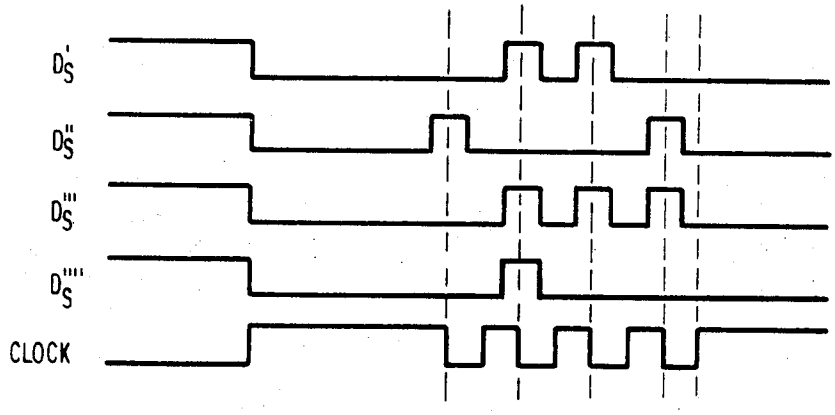
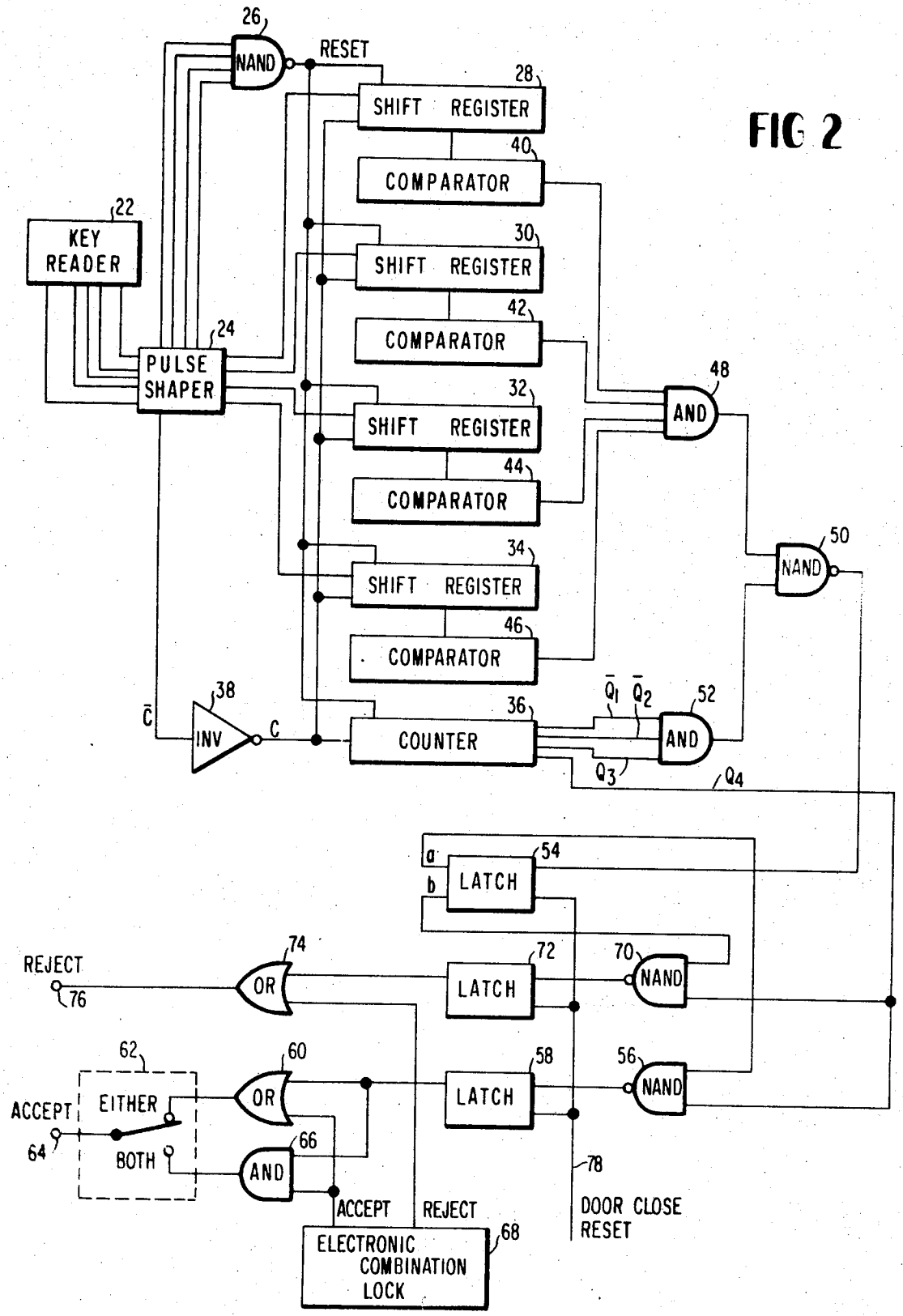



FIG. 4

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ATTORNEYS

FIG 2


26
NAND
RESET
28
SHIFT REGISTER
40
COMPARATOR
22
KEY READER
30
SHIFT REGISTER
42
COMPARATOR
24
PULSE SHAPER
48
AND
32
SHIFT REGISTER
44
COMPARATOR
50
NAND
34
SHIFT REGISTER
46
COMPARATOR
38
$\bar{C}$
INV
C
36
COUNTER
$\bar{Q}_1$ $\bar{Q}_2$
52
AND
$Q_3$
$Q_4$
a
b
54
LATCH
REJECT
76
74
OR
72
LATCH
70
NAND
62
ACCEPT
64
EITHER
BOTH
60
OR
66
AND
58
LATCH
56
NAND
78
ACCEPT
REJECT
DOOR CLOSE RESET
ELECTRONIC COMBINATION LOCK
68

# ELECTRONIC KEY LOCK HAVING DATA CODED KEY

## BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to an electronic key lock apparatus, and more particularly, to an apparatus in which a digitally coded key is inserted into a key lock apparatus such that when the digital code on the key matches a predetermined digital code in the key lock apparatus the apparatus produces an unlock output.

Summary of the Invention

This invention comprises an electronic key lock apparatus which includes a digitally coded key and a lock apparatus. The key is a machined brass plate, keyed at one edge to prevent improper insertion into a reader. An array of holes and non-holes is used to represent the digital code. The lock apparatus comprises an optical reader for reading the digitally coded holes and non-holes on the key. As the key is read, the data thereon is loaded into shift registers. After the key has been read, the data in the shift registers is compared with a predetermined code in a comparator device. If there is a match between the data in each shift register and its corresponding comparator, then the comparator produces an output. The output of all the comparators are applied to a logic circuit which produces an unlock signal if all of the comparators produce an output and the key is withdrawn, and which produces a reject signal if there is no output from at least one of the comparators and the key is withdrawn. The necessity for the withdrawal of the key prior to producing an unlock signal prevents the possibility of leaving the key in the lock after the lock has been opened. The output of a logic circuit can be used to operate a lock mechanism such as that in application Ser. No. 84,085 filed Oct. 26, 1970, by Stephen Paull, and Paul Crafton, and assigned to the same assignee as the instant application. The reject signal can be used to trigger an alarm device if so desired.

The terms key and key means as used herein includes not only metal structures with head and blade positions but also includes any other structure of metal, plastic, paper, etc., having any shape whatsoever, which contains an array of coded data. For example, key or key means includes credit cards, checks, etc. Furthermore, the data may be coded in any conventional manner such as optical, magnetic, etc.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 represents the key used in the preferred embodiment of this invention.

FIG. 2 is a block diagram of the lock apparatus in the preferred embodiment of this invention.

FIG. 3 represents the data pulses for the particular digital code on the key of FIG. 1.

FIG. 4 represents the data pulses from the key of FIG. 1 with inverted clock pulses.

FIG. 5 represents a credit card used in the preferred embodiment of this invention.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 represents a key 2 which consists of a machined brass plate having a slot 4 to prevent improper insertion into a reader. An array of holes 6, and non-holes 8, represented by X's, are located on the key. Each horizontal row 10, 12, 14, and 16 represents a coded word. The fifth row 20 which is offset slightly to the left is the clock pulse row. In reading the data contained in the key, a hole indicates a logic 1 and a non-hole indicates a logic 0.



Referring now to FIG. 2, key 2 is inserted into key reader 22 which comprises optical emitters and sensors for detecting the presence or absence of holes in the data rows and clock row of key 2. The outputs of key reader 22 are applied to pulse shaper 24. Pulse shaper 24 comprises four Schmitt triggers the output of each of which is logic 1 when the output of an optical emitter is detected by its associated optical detector in key reader 22. The output of the four Schmitt triggers is tied to NAND gate 26 whose output is logic 0 when the four inputs are logic 1.

When key 2 is inserted in the key reader 22 all of the optical sensors are interrupted, causing the Schmitt triggers of pulse shaper 24 to produce logic 0 outputs. If any of the inputs to NAND gate 26 drop to zero, then the output of NAND gate 26 changes to logic 1. This enables shift registers 28, 30, 32 and 34, and enables counter 36. When coding key 2, a code cannot be selected in which a vertical column contains more than four holes. If such a code is used then when these holes are detected NAND gate 26 will switch to a logic 0 output. This will reset shift registers 28, 30, 32, and 34, and also counter 36. As the key is then passed through the reader, the light from the emitters will again be interrupted, the output of the Schmitt triggers will drop to logic 0, and the output of NAND gate 26 will return to logic 1, enabling the shift registers 28, 30, 32, and 34. The data subsequently entered into the shift registers will then appear as if the key has just been inserted and when the key is fully inserted the code in the registers will be incomplete.

The data contained in each data row of key 2 will be fed into a respective shift register 28, 30, 32 or 34, when the clock pulse from the clock pulse row of key 2 goes to logic 0. Referring to FIG. 3, it can be seen that when the clock pulses shift to logic 0, the data in the four data rows is also at logic 0. Therefore, only logic 0's would be shifted into shift registers 28, 30, 32 and 34. Therefore, inverter 38 inverts the pulses from the clock row giving an output as shown in FIG. 4. With an inverted clock pulse, when the clock pulses switch to logic 0, either a hole or non-hole is shifted into one of the shift registers.

After the data in each data row of key 2 has been shifted into its corresponding shift register, the data in the shift register is compared with a predetermined code in a corresponding comparator 40, 42, 44 or 46. If there is a correspondence between the data in the shift register and the data wired into the corresponding comparator, the comparator produces a logic 1 output. These outputs are applied to AND gate 48. If there is correspondence between each shift register and its corresponding comparator, then the output of AND gate 48 goes to logic 1 and is applied to one input of NAND gate 50.

As key 2 is inserted, the clock pulses are applied through inverter 38 to binary counter 36. When the key 2 has been fully inserted, counter 36 will register a

count of four and its $\overline{Q1}$, $\overline{Q2}$ and Q3 outputs will all be at logic 1. These three outputs are all applied to AND gate **52** which in turn raises its output to a logic **1** level. The latter signal, coupled with the logic 1 output from AND gate **48**, causes the output of NAND gate **50** to drop to a logic 0.

The output of NAND gate **50** is applied to latch **54**. Output of latch **54** is normally logic 0 and is switched to logic 1 when logic 0 is applied to its input. Output a of latch **54** is applied to NAND gate **56**. When key **2** is withdrawn from key reader **22**, counter **36** advances further to the count of 8. At this point output Q4 of counter **36** is at logic 1 and is applied to the other input of NAND gate **56**. This produces a logic 0 at the output of NAND gate **56**, which is applied to latch **58**. When the input of latch **58** is at logic 0 its output switches to logic 1 and this output is applied to OR gate **60**. This produces a logic 1 output from OR gate **60**. If EITHER/BOTH switch **62** is in the EITHER position, then an ACCEPT output signal is produces at output terminal **64**. If EITHER/BOTH switch **62** is in the BOTH position, then the logic 1 output of latch **58** is applied to one input of AND gate **66**. The other input to AND gate **66** is from an electronic combination lock **68** such as that disclosed in application Ser. No. 884,440 filed Dec. 11, 1969, by John R. Hovey and assigned to the assignee of the instant application. Furthermore, the output of electronic combination lock **68** may also be applied to the other input of OR gate **60** so that an ACCEPT output signal at terminal **64** can be generated by either the operation of the electronic combination lock or by the use of key **2**.

If an improper key is inserted into key reader **22**, then there will be a lack of correspondence between at least one shift register and its corresponding comparator. Therefore, NAND gate **50** will produce a logic 1 output. When this is applied to latch **54**, output a will remain at logic 0 and be applied to one input of NAND gate **56**. When the key is withdrawn, Q4 will be at logic 1, therefore, NAND gate **56** will produce a logic 1 output, latch **58** will not operate, and no ACCEPT output will be produced. However, the logic 1 output from NAND gate **50**, when applied to latch **54**, will produce a logic 1 output from output **b** of latch **54**. This is applied to NAND gate **70**. When the key is withdrawn, $Q_4$ will be at logic 1 and will be applied to the other input of NAND gate **70**. This will produce a logic 0 output which is applied to latch **72**. A logic 0 input to latch **72** will produce a logic 1 output which will operate OR GATE **74**. This will produce a REJECT output at output terminal **76**. This REJECT output signal may be used to trigger an alarm device or to alert a security patrol. OR gate **74** may also be operated by a REJECT output from electronic combination lock **68**.

It can readily be seen, therefore, that if a proper key **2** is inserted into key reader **22** an ACCEPT output will be produced at terminal **64** which can be used to operate a lock mechanism. If an improper key is inserted into key reader **22**, then a REJECT output is produced at output terminal **76**, which can be used to activate an alarm device, or to alert a security patrol.

Door close reset line **78** is connected to a switch (not shown) on the door which the electronic key lock apparatus is used to unlock (not shown). When the door is opened and reclosed the switch closes to provide a negative reset pulse to latches **54**, **72** and **58**, thereby resetting the lock apparatus.

It will be obvious to those with skill in the art that key **2** may be coded in other than optical coding, such as in the preferred embodiment. Furthermore, key **2** need not be coded in a four bit code, but may be coded in any suitable digital code. All that is required is a corresponding increase or decrease in the number or size of the shift registers and comparators.

As discussed above, key **2** may not be coded such that a vertical column contains all holes. This exception to the coding of key **2** may be eliminated by adding another emitter and sensor to reader circuit **22** such that when key **2** is inserted the additional sensor always senses a solid portion of key **2**. As long as the key is within reader **22** there will always be a logic 0 at the input of NAND gate **26**. Therefore, NAND gate **26** will not switch from its logic 1 output until key **2** is withdrawn from reader **22**. Since shift registers **28**, **30**, **32**, and **34** and counter **36** are reset by the switching of NAND gate **26** to logic 0 the shift registers cannot be reset until key **2** is withdrawn. Therefore, the use of the additional emitter and sensor enables the coding of key **2** with a code which has all holes in a vertical column.

The electronic and opto-electronic portion of the electronic key lock reader may be utilized to read digitally coded credit cards or digitally coded paper such as checks. The reader is modified by changing the array of emitters, sensors and shapers to accommodate the code used. In the example shown in FIG. **5**, credit card **80** has an embossed area **82** and a coded area **84**. Corner **86** is cut out from the card in order to insure proper insertion. The coded portion **84** has an array of holes **88** and non-holes **90**, represented by X's. This coding is of the same type as that on key **2** of FIG. **1**. Column **92** which is slightly offset is the clock pulse column corresponding to row **20** on key **2**. When card **80** is inserted into reader **22** in FIG. **2**, in the direction shown by the arrow, the lock mechanism operates in the same manner as described in relation to the insertion of key **2** into reader **22**.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

I claim:

**1.** A key lock apparatus comprising:

a. key means having a digital code thereon;

b. reader means for reading the digital code on said key means as said key means is being inserted;

c. logic circuit means, coupled to said reader means, for comparing said digital code to a predetermined digital code and for producing a first signal when there is a correspondence between said digital code and said predetermined digital code wherein said logic circuit means includes

1. a plurality of shift registers and a corresponding plurality of comparator means;

2. wherein a different portion of said digital code on said key is loaded into each of said shift registers and a different portion of said predetermined digital code is stored in each of said comparator means; and

3. wherein each of said shift registers is connected to its corresponding comparator means such that each of said comparator means produces a first output when the portion of said digital code in each of said shift registers matches the portion of said predetermined digital code in said corresponding comparator means, whereby said first signal is produced when each of said comparator means produces said first output;

4. counter means for producing a second signal when said key has been fully inserted and then withdrawn from said reader means; and

5. first gate means for producing a third signal upon coincidence of said first signal and said second signal whereby an ACCEPT signal is generated upon the occurrence of said third signal which can only occur when said key means is fully withdrawn from said apparatus.

2. The apparatus of claim 1 wherein said key means comprises a plate portion having an array of holes and non-holes positioned thereon which represent said digital code.

3. The apparatus of claim 2 wherein said reader means includes opto-electronic emitters and sensors positioned to be in optical alignment with said holes in said key means and wherein said reader means produces a logic 1 output when the radiation emitted by said optoelectronic emitters is received by said sensors.

4. The apparatus of claim 1 wherein each of said comparator means produces a second output when said digital code in said shift register does not match said predetermined digital code in said corresponding comparator means whereby a reject signal is produced if at least one of said comparator means produces said second output.

5. The apparatus of claim further comprising switch means positioned on a door for resetting said key lock apparatus when said door is opened and then closed.

6. The apparatus of claim 1 wherein said key means has clock pulses encoded thereon and said counter means counts said clock pulses as said key is inserted and as said key is withdrawn.

7. The apparatus of claim 6 wherein said logic circuit means further includes reset means for resetting said shift registers when said key means is fully withdrawn from said lock apparatus.

8. The apparatus of claim 6 further including inhibiting means for preventing the occurrence of said third signal unless said key means has been fully inserted prior to withdrawal.

9. The apparatus as set forth in claim 8 wherein said inhibiting means includes:

a. second gate means coupled to said counter means for producing a first output when said counter means has counted the number of clock pulses indicating that said key means is fully inserted; and

b. third gate means, having one input for receiving said first signal and a second input for receiving the output of said second gate means, for producing an output upon the coincidence of said first signal and the first output of said second gate means.

10. The apparatus of claim 1 further including:

a. combination lock means for producing a fourth signal when the correct combination is inserted into said combination lock means;

b. fourth gate means having a first input for receiving said third signal and a second input for receiving said fourth signal, for producing a fifth signal upon the coincidence of said third and fourth signal; and

c. switch means having a first and second position wherein when said switch means is in said first position an ACCEPT signal is generated upon the occurrence of said third signal and when said switch means is in said second position an ACCEPT signal is generated upon the occurrence of said fifth signal, whereby said ACCEPT signal is generated by either the insertion and withdrawal of the correct key into said reader means or by the insertion and withdrawal of the correct key into said reader means in combination with the insertion of a correct combination into said combination lock means.

* * * * *