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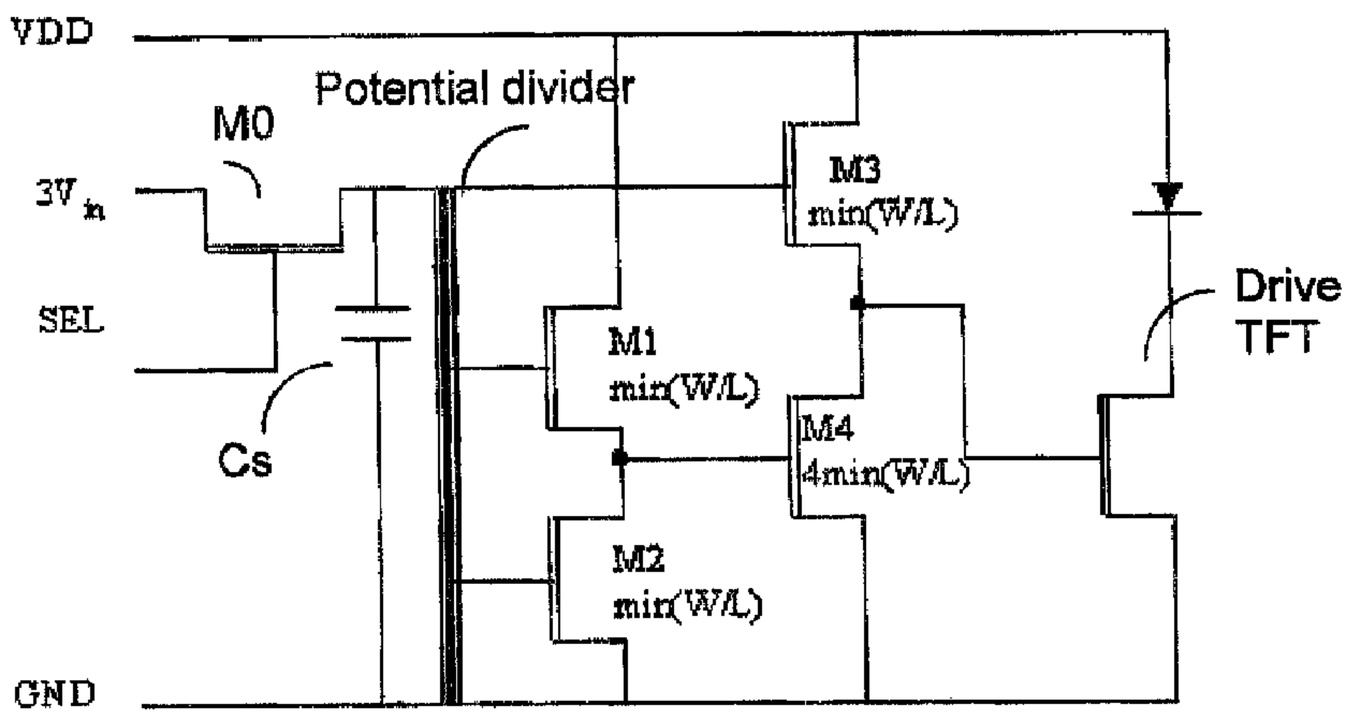
(54) Titre : CIRCUIT DE PIXELS POUR AFFICHAGES AMOLED
(54) Title: A PIXEL CIRCUIT FOR AMOLED DISPLAYS



Schematic of pixel circuit

(57) Abrégé/Abstract:
A pixel circuit for AMOLED displays is provided. The pixel circuit includes active matrix organic light emitting diode (AMOLED) display, a drive TFT for driving OLED and a circuit for compensating for the threshold voltage of the drive TFT. The circuit applies a rising gate voltage to compensate for the rising threshold voltage of the drive TFT.

Abstract

A pixel circuit for AMOLED displays is provided. The pixel circuit includes active matrix organic light emitting diode (AMOLED) display, a drive TFT for driving OLED and a circuit for compensating for the threshold voltage of the drive TFT. The circuit applies a rising gate voltage to compensate for the rising threshold voltage of the drive TFT.

A Pixel Circuit for AMOLED Displays

Field of the Invention

The present invention relates to a circuit for displays, more specifically to a pixel circuit for active matrix organic light emitting diode (AMOLED) Displays.

Background of (and Summary) of the Invention

Amorphous silicon thin film transistors (a-Si:H TFT) are suitable for active matrix organic light emitting diode (AMOLED) display backplanes due to their low leakage, good spatial uniformity, and the possibility of a low temperature process. A 2-TFT voltage driven circuit is the simplest and smallest AMOLED pixel circuit. However, with this circuit, the OLED drive current drops over time due to threshold voltage shifts in the drive TFT. Hence better circuits are required to compensate for the decay in current through the OLED.

There are two main driving principles of AMOLED circuits: Voltage and Current programming. Each drive scheme has unique advantages and disadvantages when used for a-Si or p-Si TFT AMOLED pixel operation, briefly described below.

Current Programmed Circuits

A self-compensating 4-TFT current programmed circuit is developed to overcome time dependent threshold voltage shifts described above and keep the

OLED drive current constant. Figure 1 shows the 4-TFT current-programmed pixel circuit 10, which has been previously published.

Voltage programmed circuits

Figure 2 shows the voltage-programmed pixel circuit 20, which is programmed by charge/discharge [Source: Joon-Chul Goh, Choong-Ki Kim, Jin Jang, "A Novel Pixel Circuit for Active Matrix Organic Light Emitting Diodes," SID 03 Digest]. The circuit 20 has switches Sw1, Sw2 and Sw3, a storage capacitor C_{ST}, an OLED and a drive TFT (DTFT). During the programming stage, the switches Sw1, Sw2 and Sw3 are on, allowing the storage capacitor C_{ST} to charge up to a value of the supply voltage, while maintaining the source of the drive at a voltage corresponding to the data. In order to ensure that the OLED does not have any current through it, the cathode is pulsed to reverse bias the OLED. After the capacitor (and hence the gate of the drive TFT) has been charged to the supply voltage, the signal TNO is turned off. The capacitor now discharges to the value of the data voltage above the threshold voltage of the TFT, hence ensuring immunity to the threshold voltage shift.

Figure 3 shows the voltage-programmed circuit 30, which is programmed by modifying OLED characteristics [Source: Joo-Han Kim and Jerzy Kanicki, " 200dpi 3-a-Si:H Tfts Voltage Driven AM PLEDs," SID 03 Digest]. The circuit 30 has TFT T1-T3 and a capacitor C_{ST}. The programming of the TFT occurs when the SCAN signal goes high during which time the data is fed through the capacitor C_{ST}. The TFT T2 acts as an active resistor and forces the drive transistor to operate in the linear region. Thus when there is a reduction in the OLED current

with time, the drain voltage of the drive transistor, which is seen at node A, increases, thereby increasing the current through the drive. This helps in partial compensation of the threshold voltage shift.

Figure 4 shows the voltage-programmed pixel circuit 40, which is programmed by capacitive coupling [Source: James L.Sanford and Frank R. Libsch, "TFT AMOLED Pixel Circuits and Driving Methods," SID 03 Digest]. Having opposite polarity device terminal voltages has been known to reduce the stress and increase life. Hence the circuit 40 operates by switching polarity across the TFT. The threshold voltage shift compensation takes place in a manner very similar to that of circuit 20. Initially the coupling capacitor is discharged to the threshold voltage of T3. This happens when AZ goes high thus turning on the switching TFT T2. When the row line signal goes high, the data is written onto the capacitor.

Figure 5 shows the pixel circuit 50 of UDC Corp, which is programmed by optoelectronic feedback, and has been previously published. The circuit 50 has three TFTs T_{up}, T_{down} and T_{drive}. The three TFTs T_{up}, T_{down} and T_{drive} form a latch whose state will remain unchanged unless new data enters the pixel through the select transistor. Optical feedback from the OLED to the TFT acting as a photo-detector (T_{up}) ensures that the charge on the storage capacitance maintains a steady current through the OLED.

Table 1 shows the summary of these pixel circuits 10-50.

Table 1 - Summary of Pixel Circuits

	Circuit 10 - 4 TFT current prog. circuit	Circuit 20 – Programmed by charge/ discharge	Circuit 30 – Programmed by modifying OLED characteristics	Circuit 40 – Programmed by capacitive coupling	Circuit 50 – Programmed by optoelectronic feedback
Functionality drawback	Overcompensation due to differential V_T sft. (long term effect)	OLED current instability exists because of TFT in path.	Incomplete compensation (28%)	Assumes perfect OLED with no off current	Sensitive to ambient light
Lifetime Bottleneck	Supply voltage	Auxiliary TFT in the driving path	The Active resistor	Supply voltage	Supply voltage
Layout Area	92620μm^2	92620μm^2	86412μm^2	81562μm^2	92620μm^2
Power/Pixel per prog. cycle	226μW	190μW	168μW	152μW	142μW
No of pins	4	5	4	5	4
Array Level Implication	Slow prog. because of line capacitance	Slow prog. due to capacitance of TFTs in the line	Negligible	Negligible	Negligible
Other Devices	None	Capacitor	Capacitor	Capacitor	OE TFT, Capacitor

Hence, it is desirable to provide a new pixel circuit for AMOLED which meets the following specifications:

- Perfect functionality – **100% threshold voltage shift compensation** – independence from external parameters like temperature, ambient lighting etc.
- **High Lifetime** – in excess of 10000hrs and **stability** for large range of operation

- **Easy programming** – preferably low number of pins, compatibility with environment – hence **preferably voltage programmed**
- **Quick programming** < 60µs
- **Low layout area**
- **Low power consumption**

Summary of the Invention

It is an object of the invention to provide a pixel circuit that obviates or mitigates at least one of the disadvantages of existing systems.

In accordance with an aspect of the present invention, there is provided a pixel circuit for use in a display which includes: an organic light emitting diode (OLED); a pixel driver for driving the OLED, having a drive TFT; and a compensation circuit for compensating for the shift of the threshold voltage of the pixel driver.

Other aspects and features of the present invention will be readily apparent to those skilled in the art from a review of the following detailed description of preferred embodiments in conjunction with the accompanying drawings.

Brief Description of the Drawings

The invention will be further understood from the following description with reference to the drawings in which:

Figure 1 is a schematic diagram showing a 4-TFT current-programmed pixel circuit;

Figure 2 is a schematic diagram showing a voltage-programmed pixel circuit, which is programmed by charge/discharge;

Figure 3 is a schematic diagram showing a voltage-programmed pixel circuit, which is programmed by modifying the OLED characteristics;

Figure 4 is a schematic diagram showing a voltage-programmed pixel circuit, which is programmed by capacitive coupling:

Figure 5 is a schematic diagram showing voltage-programmed pixel circuit, which is programmed by optoelectronic feedback;

Figure 6 is a graph showing Threshold Voltage shift vs. Stress Voltage characteristic;

Figure 7 is a block diagram showing a pixel circuit of the present invention;

Figure 8 is a schematic diagram showing a pixel circuit having 5 transistors;

Figure 9 is a graph showing optimization of power, stability, and area;

Figure 10 is a schematic diagram showing a first embodiment of the pixel circuit of the present invention;

Figure 11 is a graph showing the simulation results of the transfer characteristics of Figure 10;

Figure 12 is a graph showing transfer characteristics of Figure 10;

Figure 13 is a graph showing current vs. time characteristic of Figure 10;

Figure 14 is a graph showing drive current vs. time characteristics of Figure 10; and

Figure 15 is a graph showing drive current vs. time characteristics of Figure 10.

Detailed Description of the Preferred Embodiment(s)

A pixel circuit of the present invention is used in Amorphous-Silicon-based Active-Matrix OLED Displays that is voltage programmed and driven. This design:

- Compensates for the Threshold-Voltage shift in amorphous silicon thin-film transistors;
- Offers sufficient characteristics to drive an OLED pixel; and
- Is able to be fabricated and integrated into an array.

Analysis of Threshold Voltage Shift

Figure 6 shows threshold voltage shift vs stress voltage characteristic for a discrete a-Si TFT. To account for the non-linearity in the threshold voltage shift with time and gate voltage, a convenient empirical equation (1) is used for the design of the pixel circuit.

$$\Delta V_t = A\ [\exp(\alpha V_g) - 1][1-\exp(-\beta t)] \qquad \ldots(1)$$

Where ΔV_t is the threshold voltage shift, V_g is the gate voltage applied, t is the time, α, β and A are constants

At a given instance of time t = T, (1) is the following equation (2) :

$$\Delta V_t = \eta [\exp(\alpha V_g) - 1], \text{ where } \eta = A[1-\exp(-\beta T)]$$

$$= \eta [(\alpha V_g) + (\alpha V_g)^2/2! + (\alpha V_g)^3/3! + \dots] \qquad \dots(2)$$

Ignoring higher powers (as $\alpha << 1$), the following equation (3) is obtained:

$$\Delta V_t = \eta [(\alpha V_g)] = \xi V_g \qquad \dots (3)$$

For relatively low values of the gate voltage, which are well within the practical range of operation.

Principle of Compensation

Figure 7 shows a concept of the pixel circuit of the present invention. The compensation circuit 102 in accordance with an embodiment of the present invention applies a rising gate voltage to compensate for the rising threshold voltage of the drive TFT.

The compensation technique of the present invention is now described in detail. Figure 8 shows a pixel circuit 120 having 5 transistors M1-M4 and Mdrive. If $a/b = (N)^n$, $c/d = (M)^n$ and all the transistors have the same initial threshold voltage, we have the following equations:

Stage 1:

$$N^n (V_{bias1} - V_{To} - V_{o1} - \xi V_{bias1})^n = (V_{in} - V_{To} - \xi V_{in})^n$$

Thus,

$$V_{o1} = (V_{bias1} - \xi V_{bias1}) - (V_{in} - \xi V_{in}) / N + (1/N - 1) V_{To}$$

$$= (V_{bias1} - V_{in}/N) - \xi (V_{bias1} - V_{in}/N) + (1/N - 1) V_{To}$$

V_{T0} is the initial (starting) threshold voltage of the TFTs.

Stage2:

$$M^n (V_{bias2} - V_{To} - V_{o2} - \xi V_{bias2})^n = (V_{o1} - V_{To} - \xi V_{o1})^n$$

Which is the same as,

$$M^n (V_{bias2} - V_{To} - V_{o2} - \xi V_{bias2})^n =$$

$$[\{(V_{bias1} - V_{in}/N) - \xi (V_{bias1} - V_{in}/N) + (1/N - 1) V_{To}\} - V_{To} - \xi \{(V_{bias1} - V_{in}/N) -$$

$$\xi (V_{bias1} - V_{in}/N) + (1/N - 1) V_{To}\}]^n$$

As $\xi << 1$, we have the following reduced form:

$$M^n (V_{bias2} - V_{To} - V_{o2} - \xi V_{bias2})^n =$$

$$[\{V_{bias1} - V_{in}/N + (1/N - 1) V_{To}\} - V_{To} - 2\xi (V_{bias1} - V_{in}/N) - \xi (1/N - 1) V_{To}]^n$$

Thus,

$$V_{o2} = [V_{bias2} - \xi V_{bias2}] -$$

$$[\{V_{bias1} - V_{in}/N + (1/N - 1) V_{To}\} - \xi \{2(V_{bias1} - V_{in}/N) + (1/N - 1) V_{To}\}]/M + (1/M - 1) V_{To}$$

$$= [V_{bias2} - \{V_{bias1} - V_{in}/N + (1/N - 1) V_{To}\}/M] +$$

$$\xi [\{2(V_{bias1} - V_{in}/N) + (1/N - 1) V_{To}\}/M - V_{bias2}] + (1/M - 1) V_{To}$$

For achieving the desired purpose, we want V_{o2} to be of the form ($V_{out} + \xi V_{out}$).

$$[V_{bias2}+ (1/M -1) V_{To} - \{V_{bias1} - V_{in} / N +(1/ N - 1) V_{To}\}/M] =$$

$$[\{2(V_{bias1} - V_{in} /N) + (1/N - 1) V_{To}\}/M - V_{bias2}]$$

Subject to the following constraints, which ensure that, the transistors operate in saturation.

$$V_{bias1} - V_{To} \leq VDD$$

$$V_{bias2} - V_{To} \leq VDD$$

$$V_{in} - V_{To} \leq V_{o1}$$

$$V_{o1} - V_{To} \leq V_{o2}$$

The above conditions rewritten as follows:

1. $[V_{bias2}+ (1/M -1) V_{To} - \{V_{bias1} - V_{in} / N + (1/ N - 1) V_{To}\}/M] =$

   $[\{2(V_{bias1} - V_{in} /N) + (1/N - 1) V_{To}\}/M - V_{bias2}]$

2. $V_{bias1} - V_{To} \leq VDD$

3. $V_{bias2} - V_{To} \leq VDD$

4. $[V_{bias1} (1 + 1/M) - V_{bias2} + V_{To} (1/N +1/MN -2/M - 1)] / (1/N + 1/NM) \leq V_{in}$

5. $V_{in} \leq [V_{bias1} + (1/N) V_{To}] / (1 + 1/N)$

Solving the above set of conditions for different values of N and M, various possible solutions are obtained as shown in Table 2. These solutions form various versions of the general circuit of Figure 8. These solutions are to be optimised for minimum layout area, minimum power consumption and maximum stability.

Table 2 - Solutions for the general circuit

VER	V_{Bias1}	V_{Bias2}	V_{out} (Gate voltage to drive TFT)	Conditions for operation
A1	$2V_{iN}$	$3V_{iN}$	$(V_{iN} + V_{To}) + \xi(V_{iN})$	$V_{To} \leq V_{iN} \leq VDD/3 + V_{To}/3$
A2	$2V_{in}$	$3V_{iN} - V_{To}/2$	$(V_{iN} + V_{To}/2) + \xi(V_{iN} + V_{To}/2)$	$V_{To} \leq V_{iN} \leq VDD/3 + V_{To}/2$
A3	$3V_{iN} - 2V_{To}$	$3V_{iN} - 9/2V_{To}$	$(V_{iN} - 3/2V_{To}) + \xi(V_{iN} - 3/2V_{To})$	$V_{To} \leq V_{iN} \leq VDD/3 + V_{To}$
A4	$7/3V_{iN} - 4/3V_{To}$	$3V_{iN} - 23/6V_{To}$	$(V_{iN} - 5/6V_{To}) + \xi(V_{iN} - 5/6V_{To})$	$V_{To} \leq V_{iN} \leq VDD/3 + 29/18V_{To}$
A5	$7/3V_{iN} - 4/3V_{To}$	$2V_{iN} - 43/18V_{To}$	$2/3V_{iN} - 13/18V_{To} + \xi(2/3V_{iN} - 13/18V_{To})$	$3/2V_{To} \leq V_{iN} \leq 23/6V_{To} \leq VDD/2 + 61/5$
A6	$2V_{iN} - V_{To}$	$3V_{iN} - 7/2V_{To}$	$V_{iN} - 1/2V_{To} + \xi(V_{iN} - 1/2V_{To})$	$V_{To} \leq V_{iN} \leq VDD/3 + 7/6V_{To}$
A7	$2V_{iN} - V_{To}$	$2V_{iN} - 13/6V_{To}$	$2/3V_{iN} - 1/2V_{To} + \xi(2/3V_{iN} - 1/2V_{To})$	$3/2V_{To} \leq V_{iN} \leq 9/2V_{To} \leq VDD/2 + 19/12$
A8	$9/5V_{iN} - 4/5V_{To}$	$3V_{iN} - 33/10V_{To}$	$V_{iN} - 3/10V_{To} + \xi(V_{iN} - 3/10V_{To})$	$V_{To} \leq V_{iN} \leq VDD/3 + 43/30V_{To}$
A9	$9/5V_{iN} - 4/5V_{To}$	$2V_{iN} - 61/30V_{To}$	$2/3V_{iN} - 11/30V_{To} + \xi(2/3V_{iN} - 11/30V_{To})$	$3/2V_{To} \leq V_{iN} \leq 49/10V_{To} \leq VDD/2 + 91/$
A10	$5/3V_{iN} - 2/3V_{To}$	$3V_{iN} - 19/6V_{To}$	$V_{iN} - 1/6V_{To} + \xi(V_{iN} - 1/6V_{To})$	$V_{To} \leq V_{iN} \leq VDD/3 + 25/18V_{To}$
A11	$5/3V_{iN} - 2/3V_{To}$	$2V_{iN} - 53/18V_{To}$	$2/3V_{iN} - 5/18V_{To} + \xi(2/3V_{iN} - 5/18V_{To})$	$3/2V_{To} \leq V_{iN} \leq 53/6V_{To} \leq VDD/2 + 71/3$
A12	$5/3V_{iN} - 2/3V_{To}$	$3/2V_{in} - 4/3V_{To}$	$1/2V_{iN} - 2/3V_{To} + \xi(1/2V_{iN} - 2/3V_{To})$	$2V_{To} \leq V_{iN} \leq 8/3V_{To} \leq 2VDD/3 + 14/9V_{T}$
A13	$11/7V_{iN} - 4/7V_{To}$	$3V_{iN} - 43/14V_{To}$	$V_{iN} - 1/14V_{To} + \xi(V_{iN} - 1/14V_{To})$	$V_{To} \leq V_{iN} \leq VDD/3 + 57/42V_{To}$
A14	$11/7V_{iN} - 4/7V_{To}$	$2V_{iN} - 121/42V_{To}$	$2/3V_{iN} - 3/14V_{To} + \xi(2/3V_{iN} - 3/14V_{To})$	$3/2V_{To} \leq V_{iN} \leq 75/14V_{To} \leq VDD/2 + 153/$
A15	$11/7V_{iN} - 4/7V_{To}$	$3/2V_{iN} - 18/14V_{To}$	$1/2V_{iN} - 2/7V_{To} + \xi(1/2V_{iN} - 2/7V_{To})$	$2V_{To} \leq V_{iN} \leq 24/7V_{To} \leq 2VDD/3 + 82/21$
A16	$3/2V_{iN} - 1/2V_{To}$	$3V_{iN} - 3V_{To}$	$V_{iN} + \xi(V_{iN})$	$V_{To} \leq V_{iN} \leq VDD/3 + 4/3V_{To}$
A17	$3/2V_{iN} - 1/2V_{To}$	$2V_{iN} - 11/6V_{To}$	$2/3V_{iN} - 1/6V_{To} + \xi(2/3V_{iN} - 1/6V_{To})$	$3/2V_{To} \leq V_{iN} \leq 11/2V_{To} \leq VDD/2 + 17/1$
A18	$3/2V_{iN} - 1/2V_{To}$	$3/2V_{iN} - 5/4V_{To}$	$1/2V_{iN} - 1/4V_{To} + \xi(1/2V_{iN} - 1/4V_{To})$	$2V_{To} \leq V_{iN} \leq 7/2V_{To} \leq 2VDD/3 + 3/2V_{To}$

In Table 2, V_{IN}, V_{IN} and V_{in} all represent the input voltage.

Optimization

The range of operation parameter:

This can be defined as 'σ'. As we need at least a 3 V_{To} range to operate the drive,

$$\sigma = 3 - [\mathrm{Max}(V_{in}) - \mathrm{Min}(V_{in})]/ V_{To}$$

The layout area parameter:

This is defined as 'a'.

$$a = \Sigma_{i=1 \text{ to } 4}(W/L)_{M\,i} / \min(W/L)$$

The power consumption parameter:

This can be defined as 'λ'. The power consumed by the compensation circuit 102 is the product of the supply voltage and the current. But the current is dependent on the minimum gate voltage in each stage, which in all the cases is approximately V_{in}. Hence the supply voltage alone decides this parameter. The supply voltage needs to be only as large as the largest bias voltage possible. Hence we define λ as follows:

$$\lambda = \max(V_{bias}) / VDD = \max(V_{bias}) / 10V_{To}$$

To find the optimum circuit we find the minimum value of $P = (a\ \lambda / \sigma)$. Figure 9 shows optimization of power, stability and area (i.e. physical dimensions when it is fabricated) for the 5-transistor pixel circuit of Figure 8. In Figure 9, P=-40 is obtained as minimum value. a, λ, σ are selected to minimize P.

Figure 10 shows the first embodiment of the pixel circuit 100. The pixel circuit 100 has 2 signal lines; 3Vin and SEL. SEL turns on the pixel for programming, and 3Vin is a voltage which represents the desired brightness of the pixel. The pixel circuit 100 also has 2 supply lines, Vdd and GND. The pixel Circuit 100 also contains a storage capacitor Cs and a potential divider, represented by the thick vertical bar.

The pixel circuit 100 of Figure 10 is a 5 TFT voltage programmed, a-Si or p-Si TFT AMOLED pixel circuit.

Programming Time Analysis

Following is a description of the programming of the pixel circuit 100, shown in Figure 10. The SEL signal goes on when the pixel is to be programmed. The data for the pixel (3Vin) is delivered to the pixel, and stored in the capacitor Cs. The SEL signal then goes off. The charge in the capacitor Cs flows through the potential divider, setting up the necessary bias voltages for M1, M2 and M3. Once the bias voltages are set up, transistors M1, M2, M3 and M4 work together to apply a voltage to the gate of the drive TFT, which is equal to Vin plus the threshold voltage shift of the drive TFT.

The threshold voltage shift in M1, M2, M3 and M4 work together to track and compensate for the threshold voltage shift in the drive TFT, by providing the appropriate gate voltage to the drive TFT.

During the programming

$$2.2\ R_{line}\ C_S \leq 32\mu s$$

Where, R_{line} is the line resistance.

For maintaining the charge, we need

$$0.11\ R'\ C_S > 20ms$$

Where R' is the resistance of the potential divider. This can easily be made high by choosing a material with high resistivity such as a-Si:H itself and by controlling the length of the strip.

The circuit was tested using min size TFTs of 66/23.

Figure 11 shows simulation results of the transfer characteristics of Figure 10. The X-axis is the Vin supplied to the first stage. Figure 11 shows the simulation results of the transfer characteristics of Figure 10. Figure 12 shows transfer characteristics of Figure 10. Figure 13 shows current vs. time characteristic of Figure 10. Figure 14 shows drive current vs. time characteristics of Figure 10. Figure 15 shows drive current (Idrive) vs. time characteristics of Figure 10.

According to the present invention, the pixel circuit meets the followings:

Functionality Drawback: None

Lifetime bottleneck: TFT M1 going into linear

Layout area: 109618μm^2

Power consumption:

Dynamic power = 18μW/pixel

Static Power = 167μW/pixel

Total Power consumption per programming = 185μW/pixel

Other devices: Potential divider, capacitor

Number of Signal Lines: 4

Array implications: Negligible

While particular embodiments of the present invention have been shown and described, changes and modifications may be made to such embodiments without departing from the true scope of the invention.

What is claimed is:

1. A pixel circuit for use in a display comprising:

an organic light emitting diode (OLED);

a pixel driver for driving the OLED, having a drive TFT; and

a compensation circuit for compensating for the shift of the threshold voltage of the pixel driver.

2. The pixel circuit according to claim 1, wherein the pixel driver includes a first stage circuit having first and second TFT transistors, and a second stage circuit which is provided between the first stage circuit and the drive TFT and has third and forth TFT transistors.

3. The pixel circuit according to claim 2, wherein the compensation circuit includes a potential divider provided for the first and second stage circuits.

5. The pixel circuit according to claim 3, wherein the compensation circuit further includes a storage capacitor provided parallel to the potential divider.

6. The pixel circuit according to claim 5, wherein a signal line for controlling the charge of the storage capacitor.

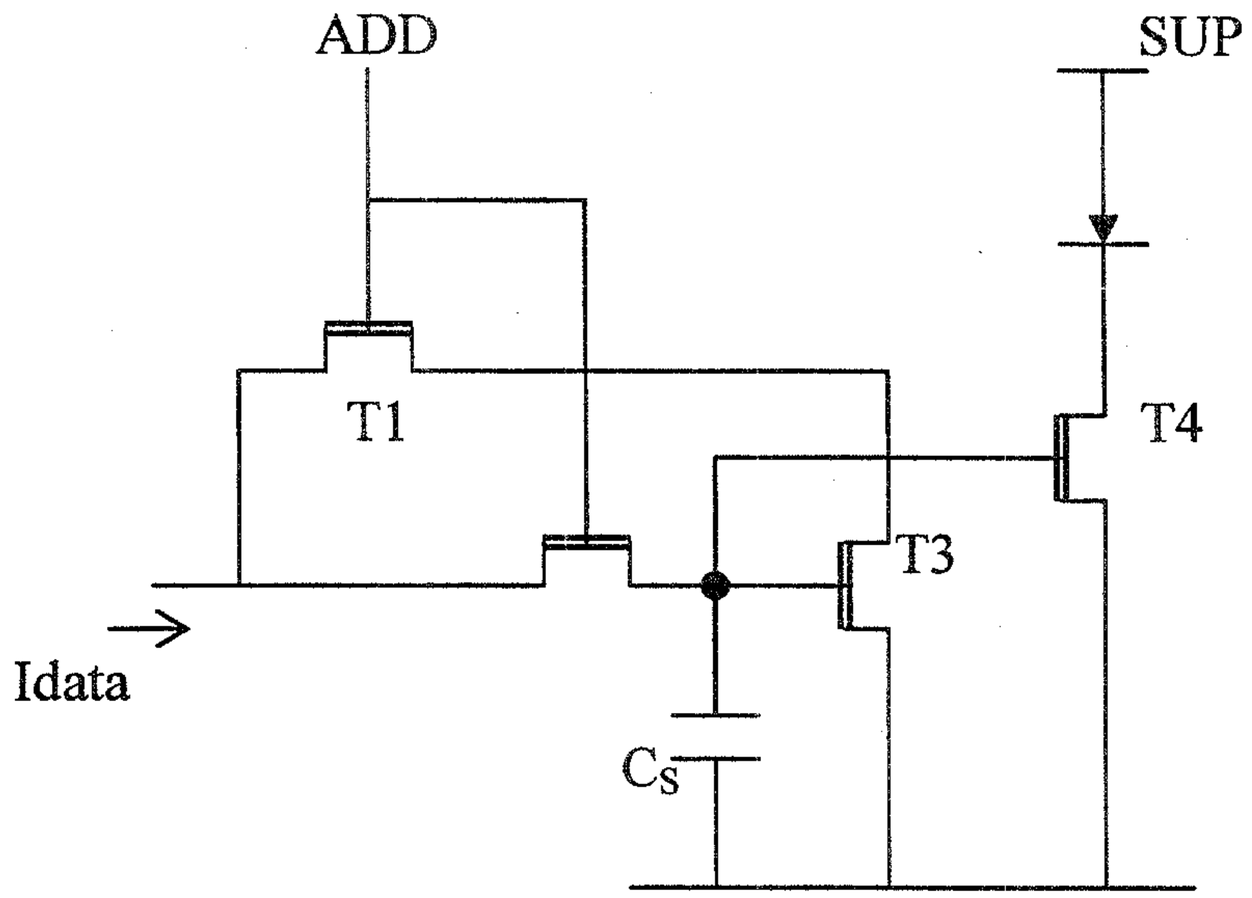


Figure 1 - 4-TFT current-programmed pixel

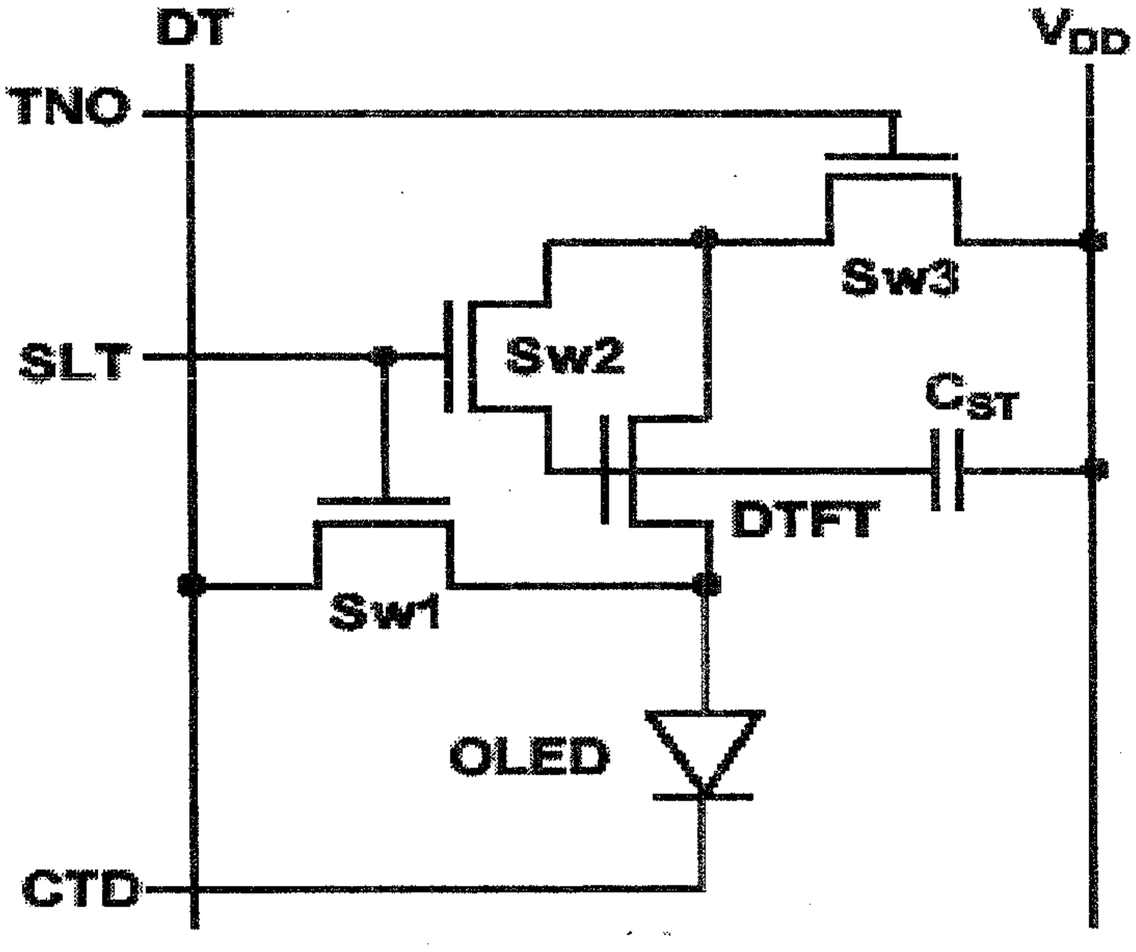


Figure 2 - Voltage-Programmed Circuit – Programming by Charge/Discharge

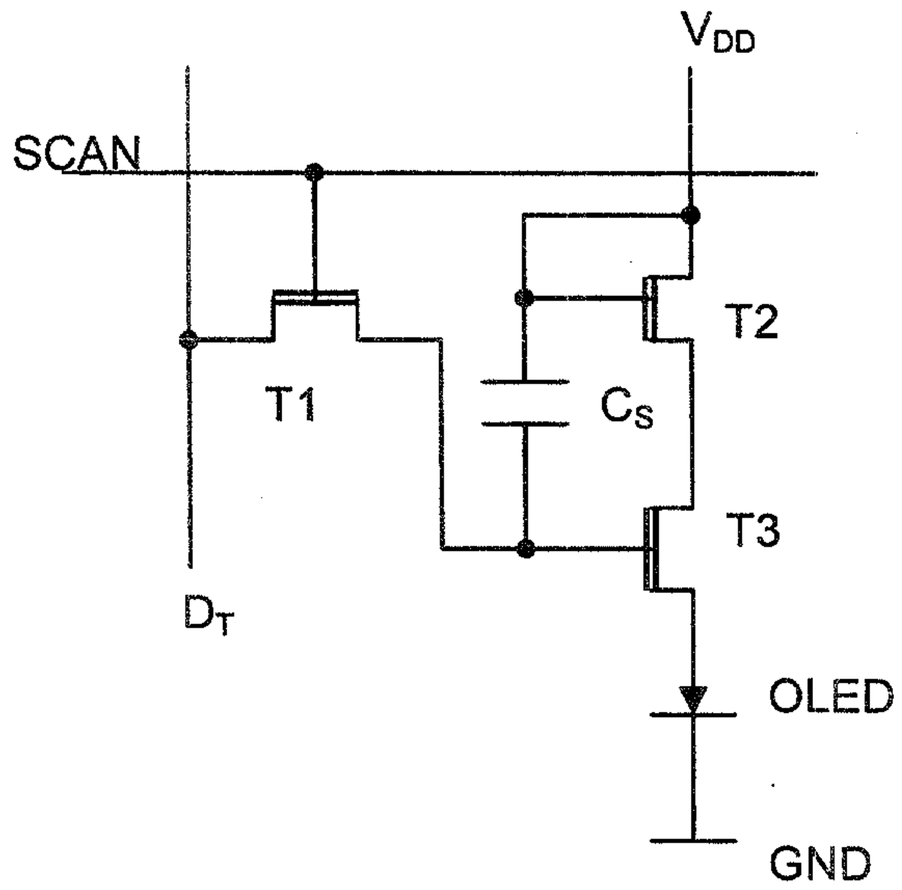


Figure 3 - Voltage-programmed pixel circuit – Programming by modifying OLED characteristics

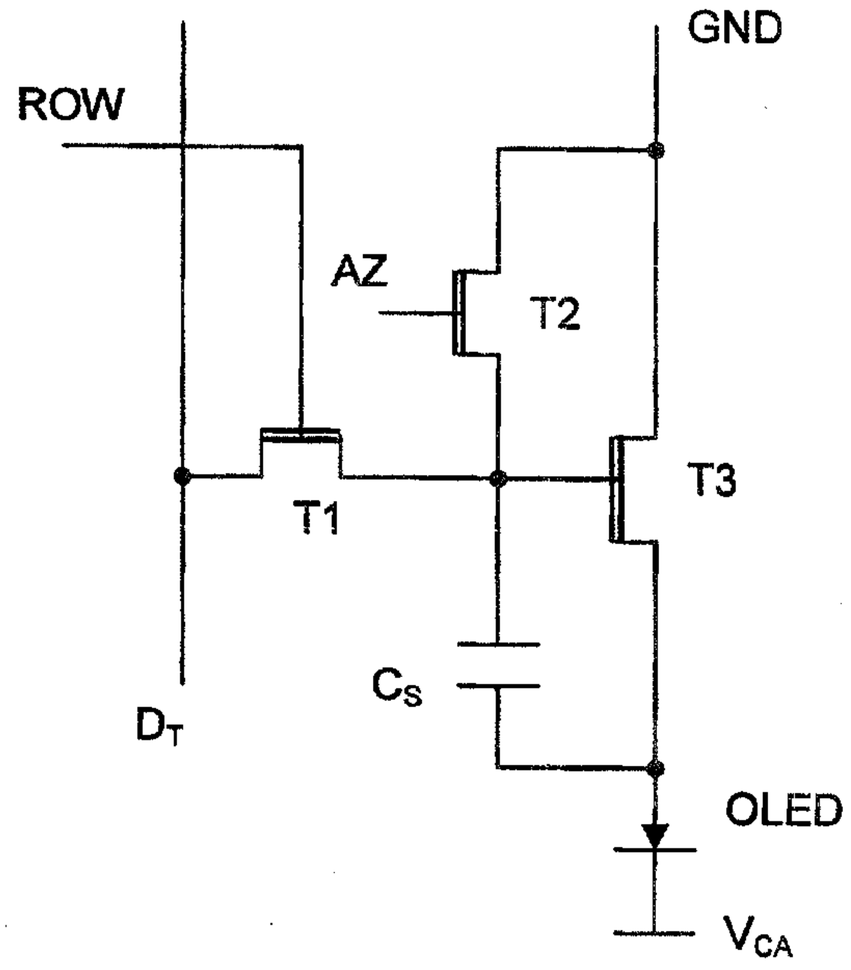


Figure 4 - Voltage-Programmed Circuit – Programming by capacitive coupling

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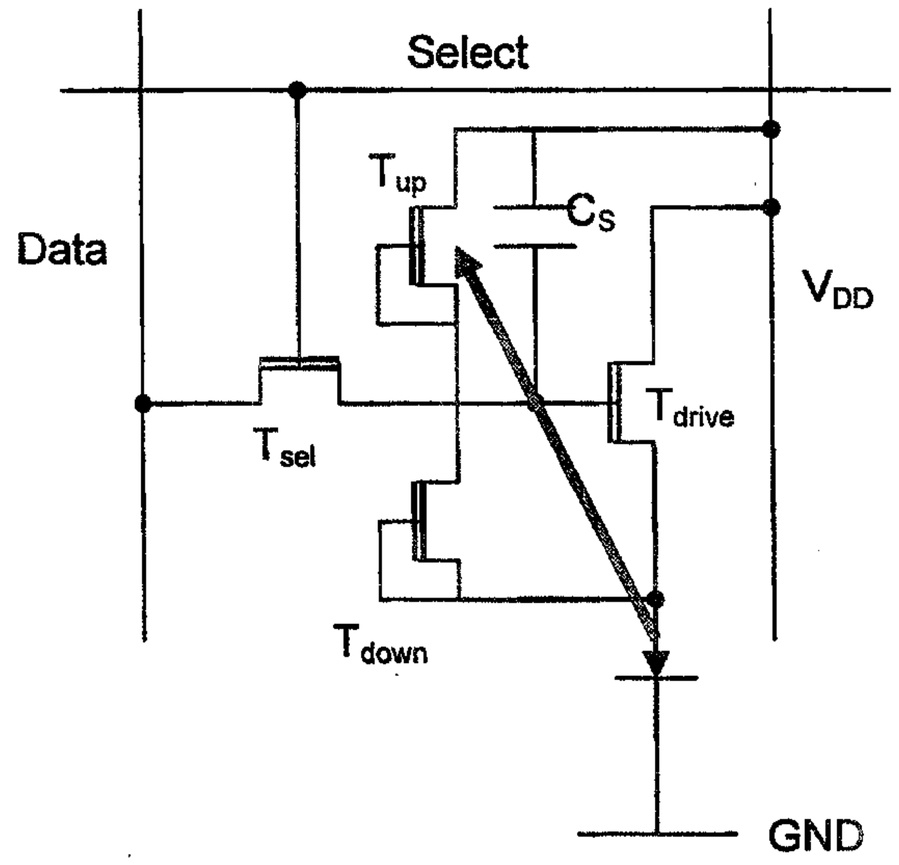


Figure 5 – Voltage-Programmed Circuit – Programmed by Optoelectronic feedback

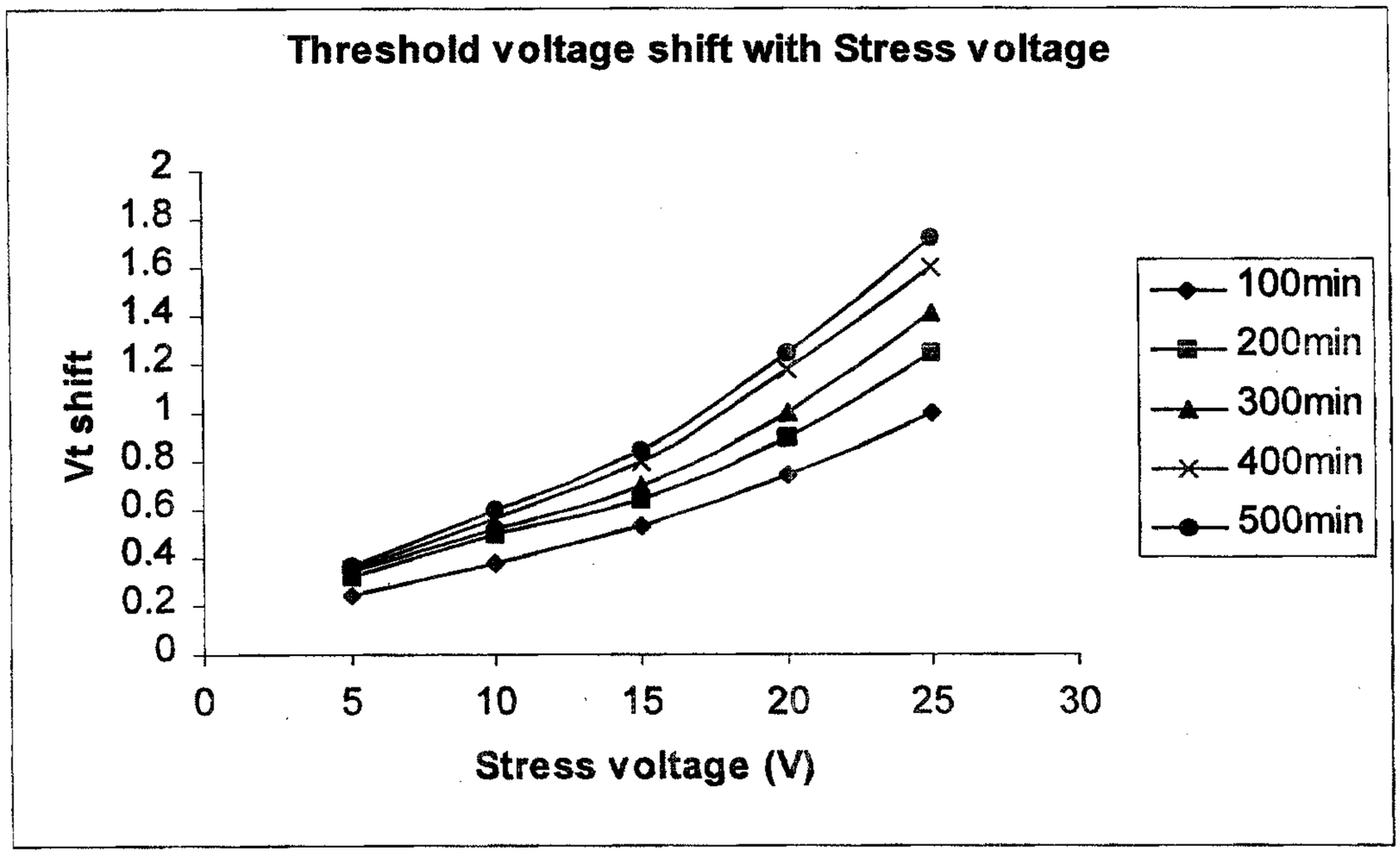


Figure 6 - Threshold Voltage shift vs. Stress Voltage of a discrete a-Si TFT

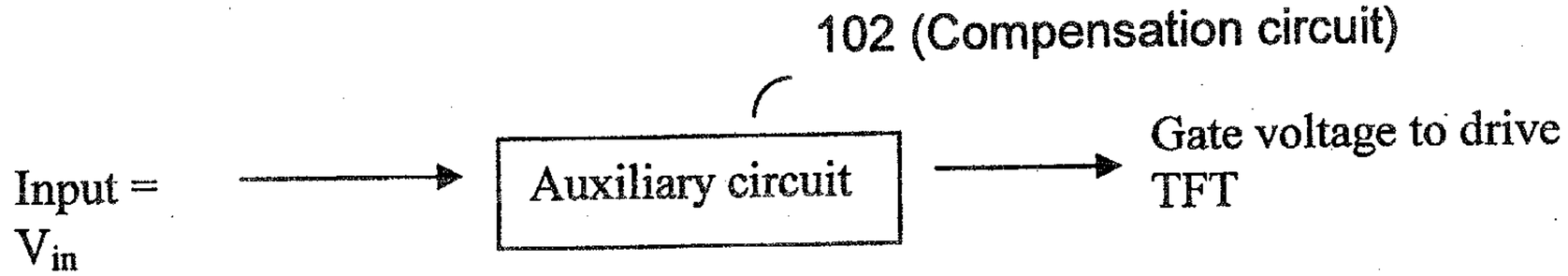


Figure 7 - Principle of compensation

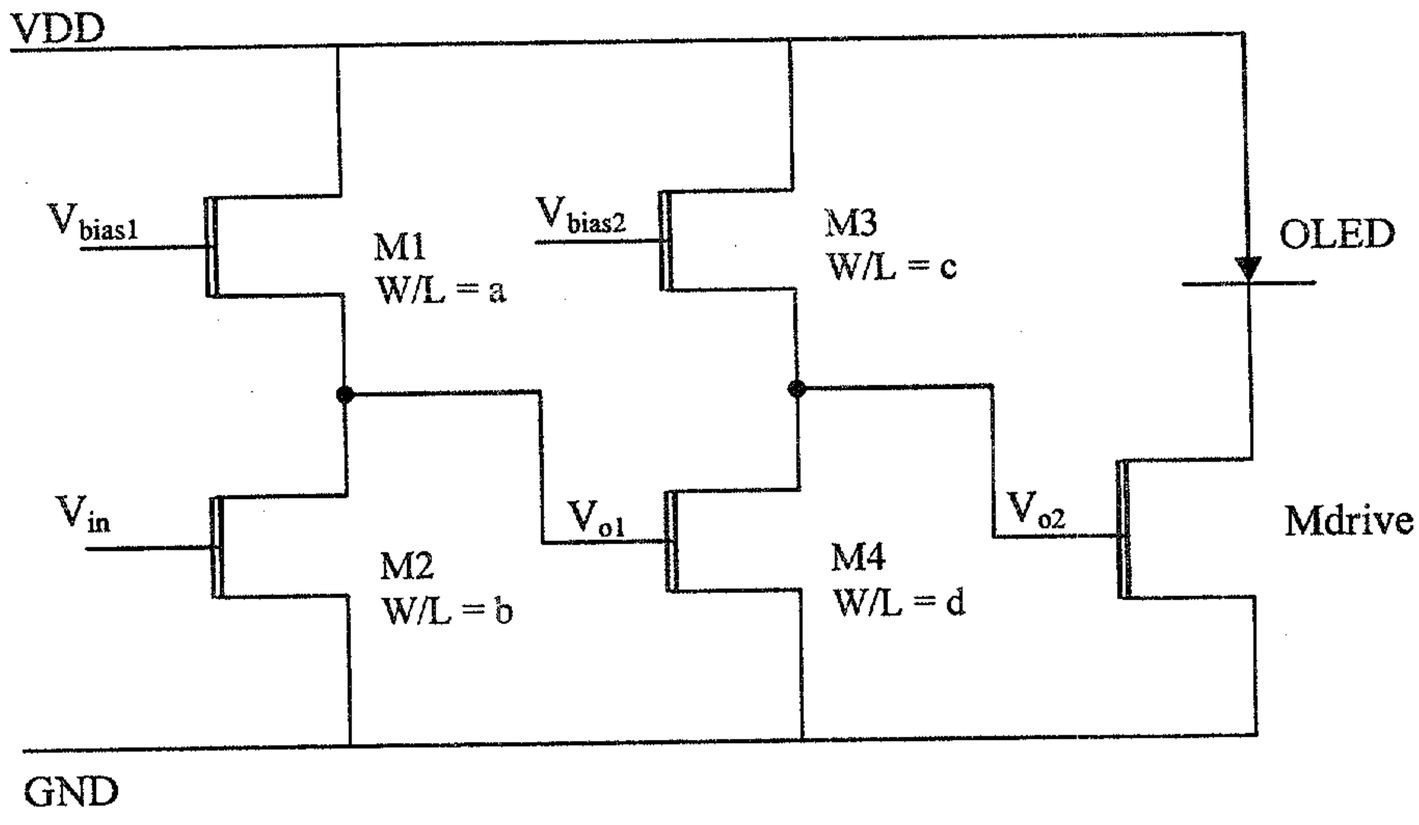


Figure 8 - Schematic of pixel circuit

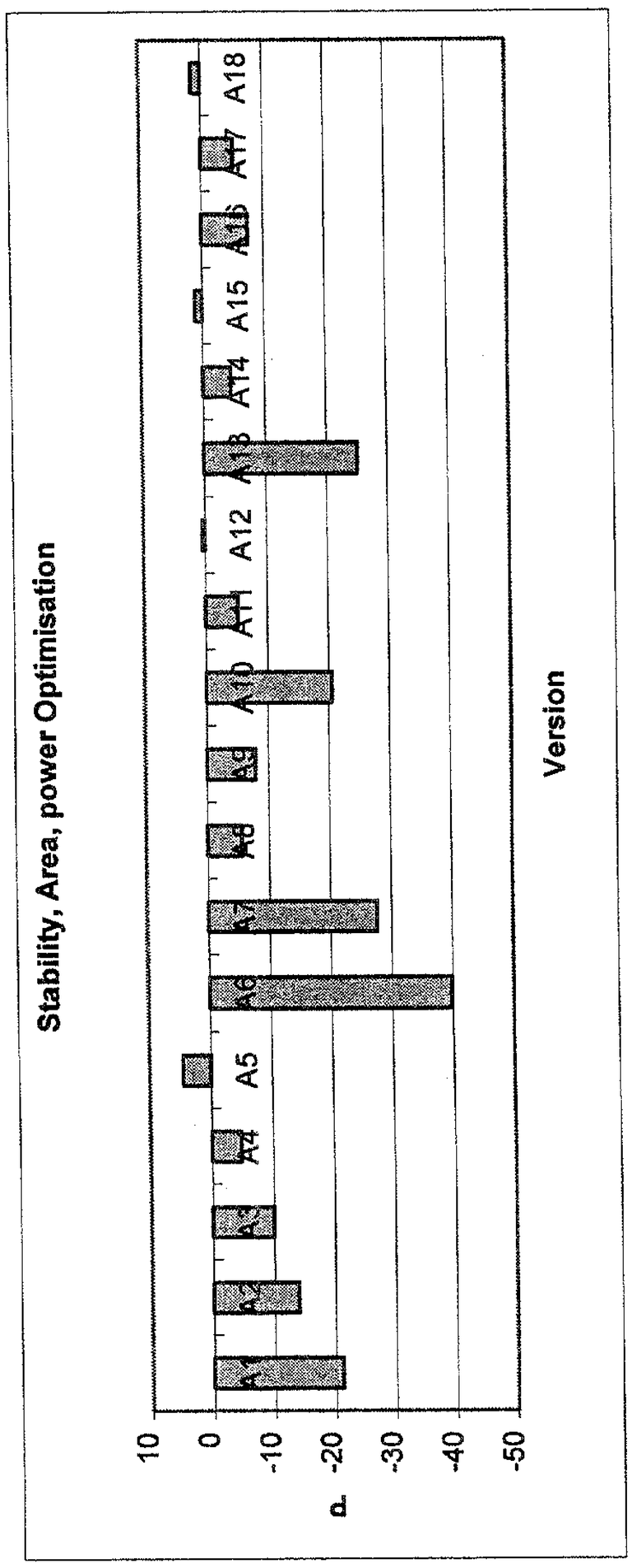


Figure 9 - Optimization of power, stability, and area

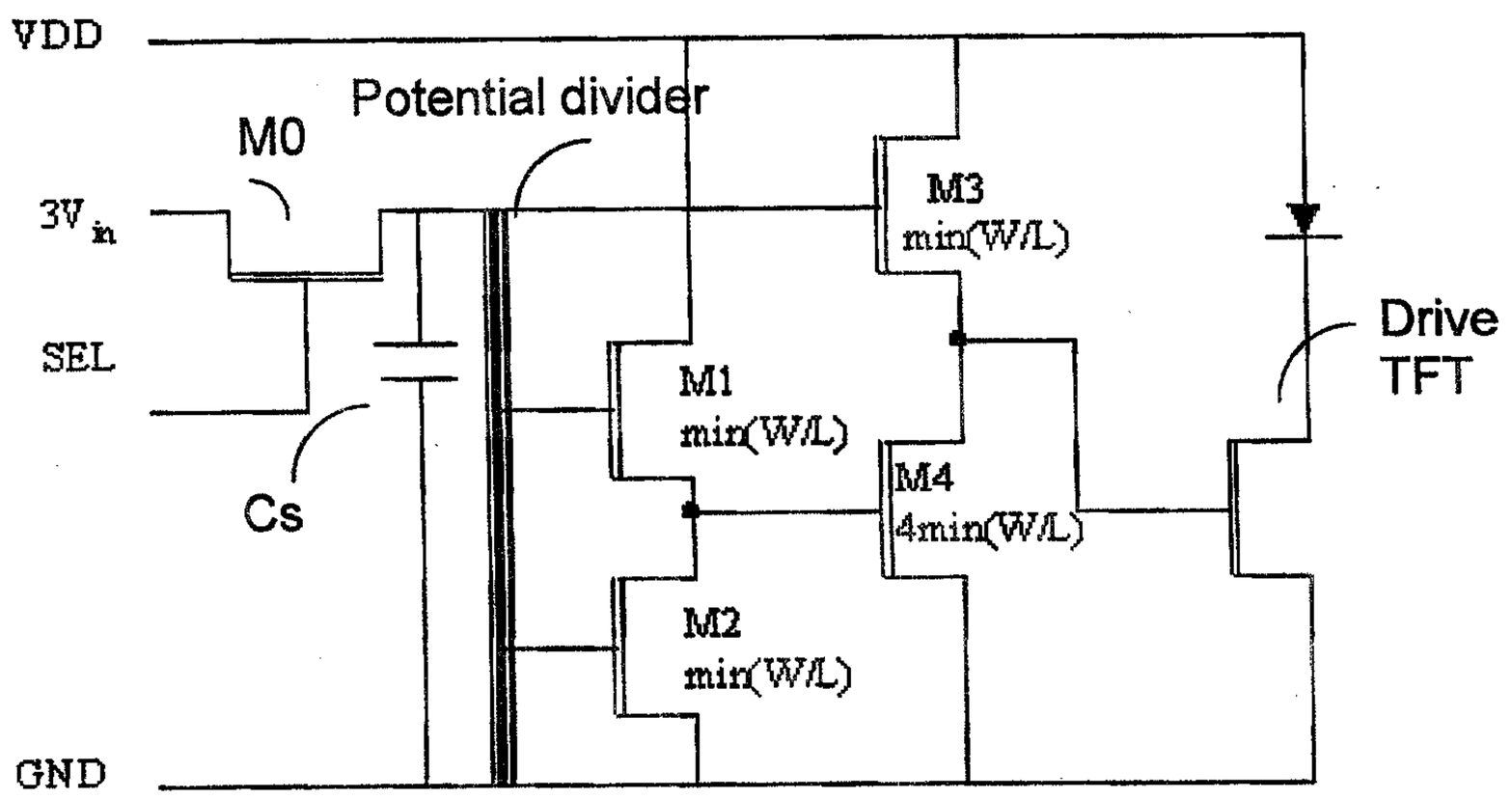


Figure 10 - Schematic of pixel circuit

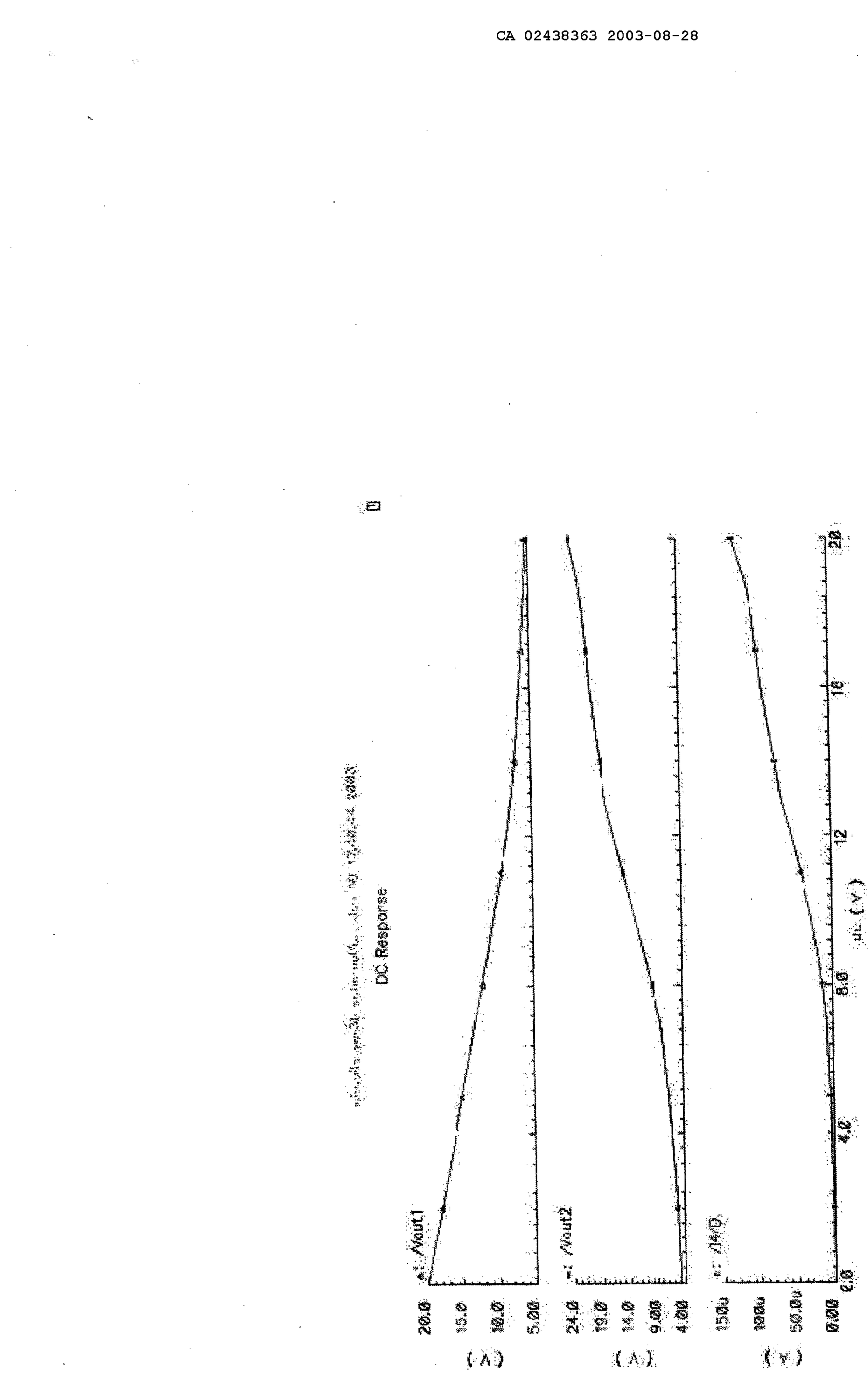


Figure 11 - Simulation of the transfer characteristics. The X-axis is the Vin supplied to the first stage

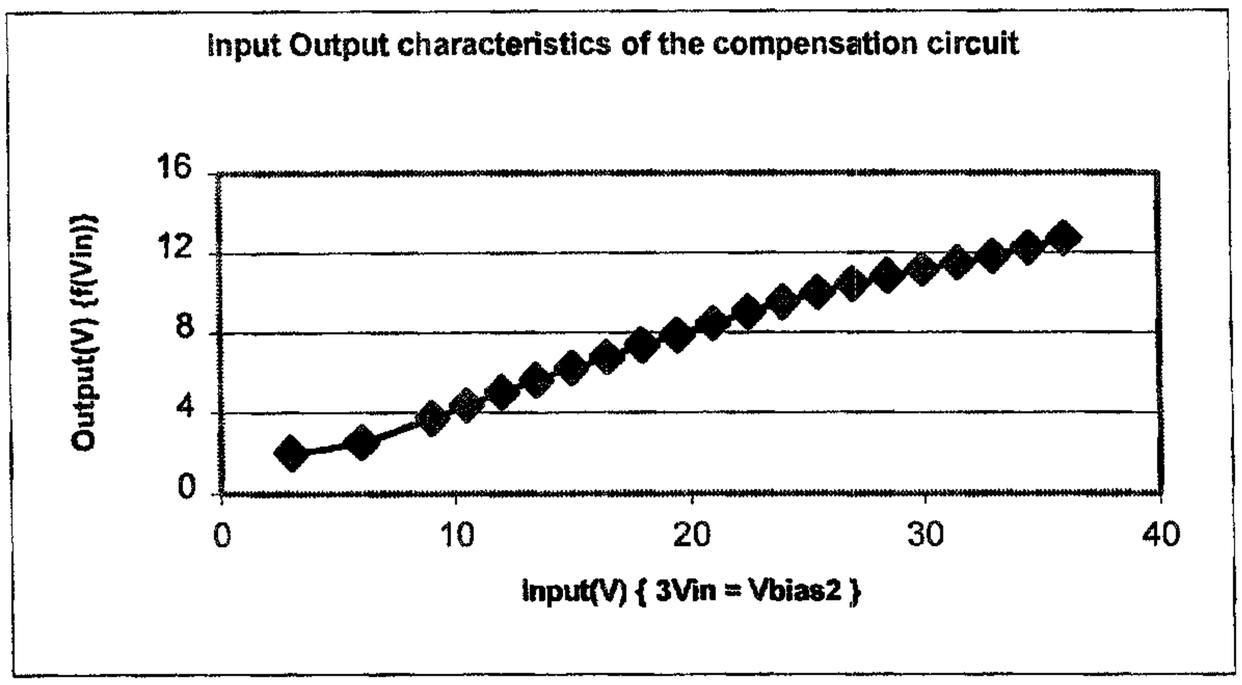


Figure 12 - Transfer Characteristics

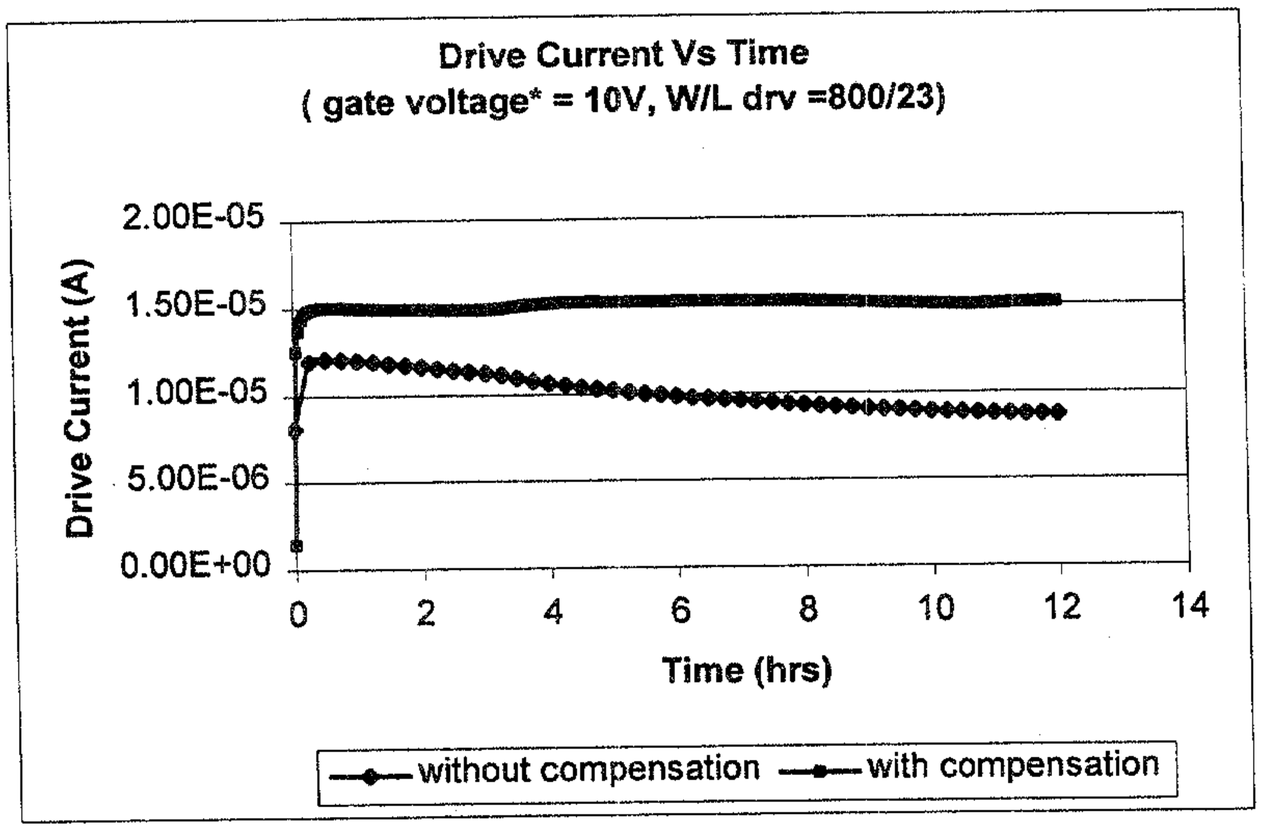


Figure 13 - Current vs. Time

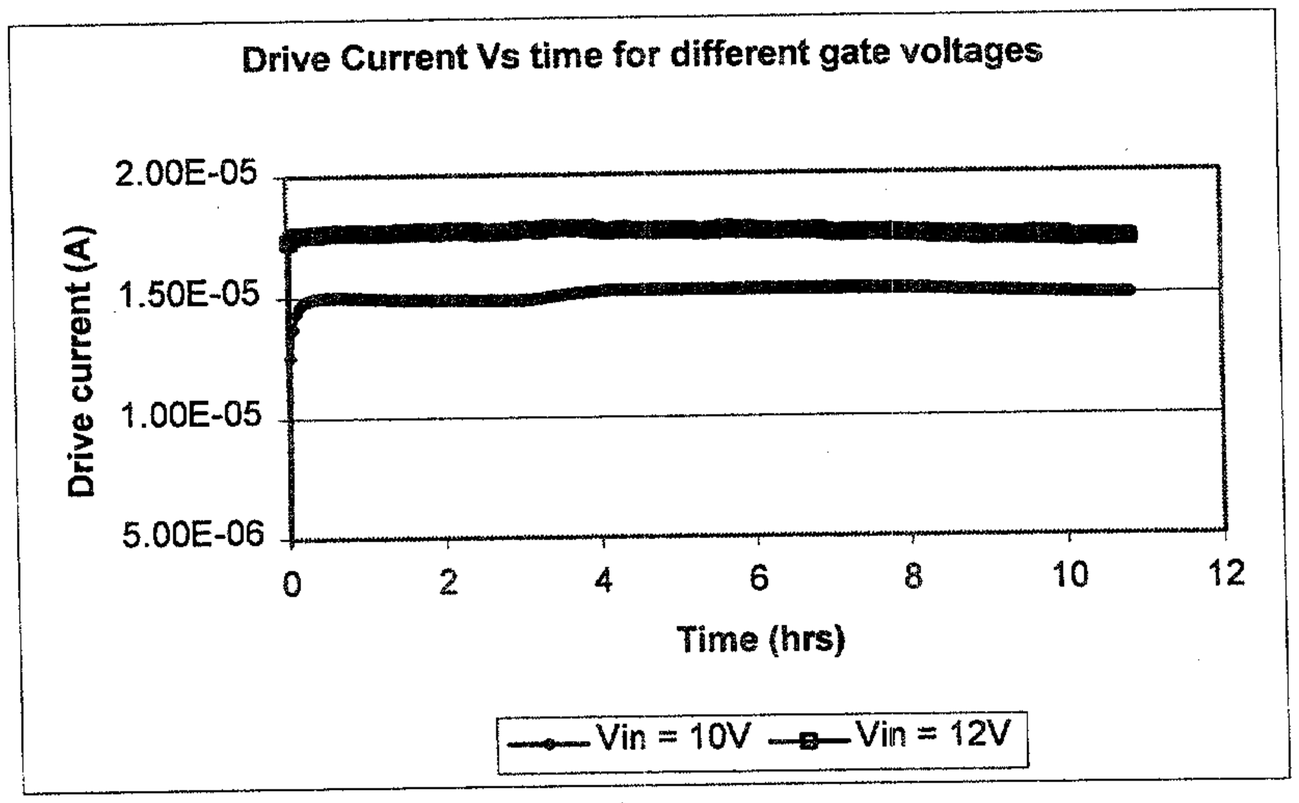


Figure 14 - Drive Current vs. time

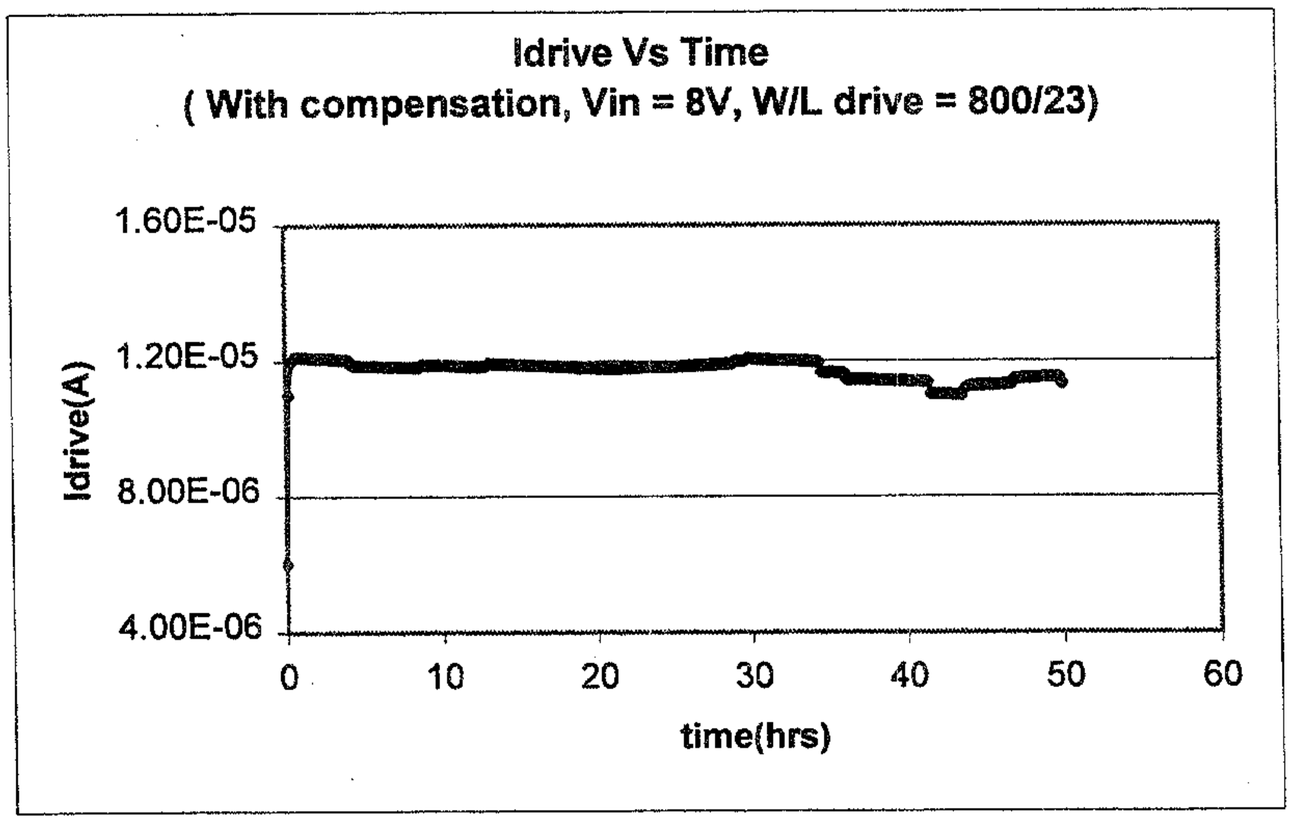
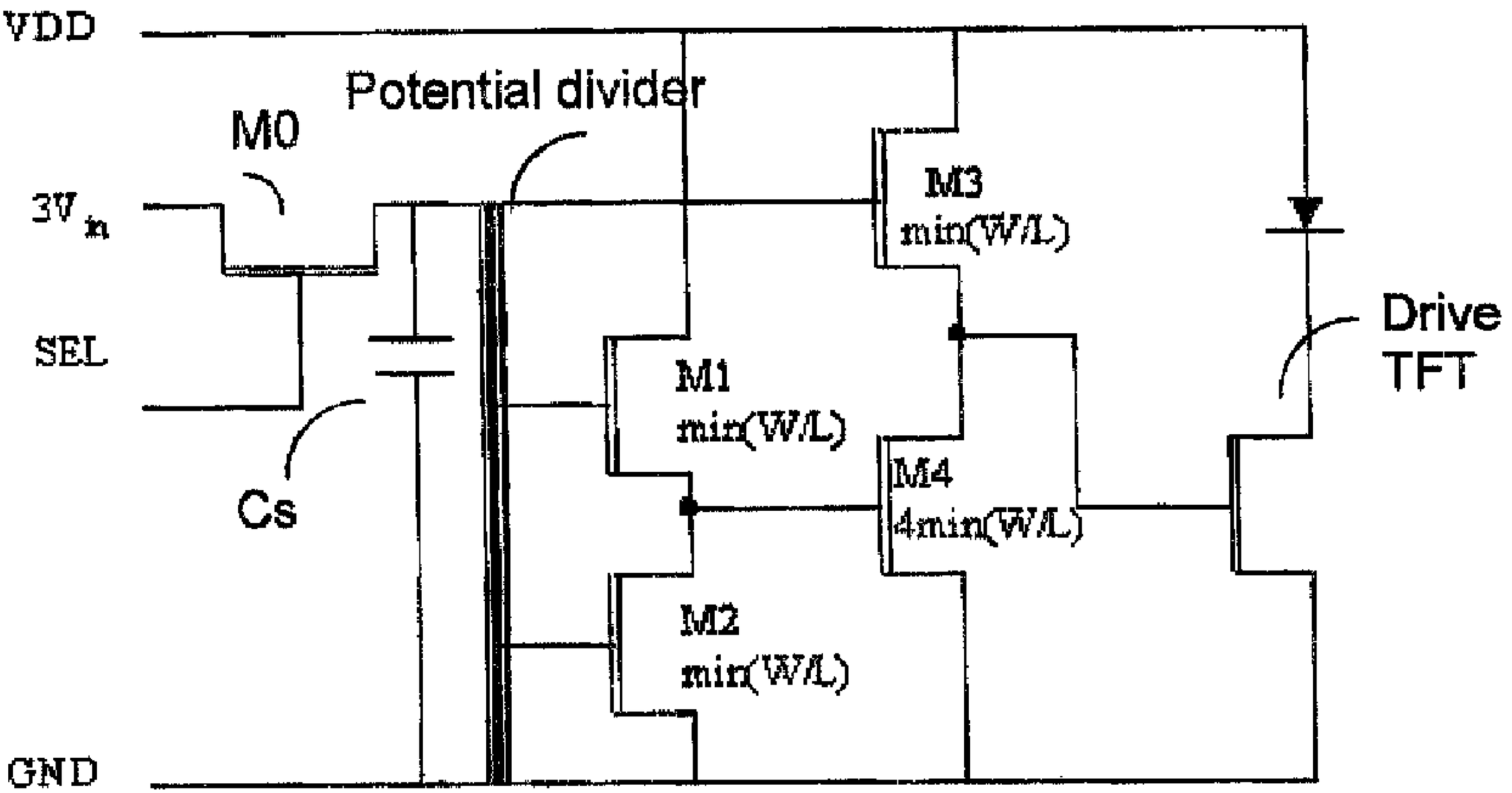


Figure 15 - Drive current (Idrive) vs. time



Schematic of pixel circuit