**Methods and Apparatus for Charge Coupled Device Image Acquisition With Independent Integration and Readout**

Methods and apparatus for image acquisition utilize a charge coupled device having a photosensitive region that responds to an applied transfer signal by transferring charge accumulated on the collection sites to the corresponding readout sites. The non-photosensitive region responds to a read signal, applied independently of the transfer signal, by outputting (e.g., to the host camera or image acquisition system) charges on the readout sites. The methods and apparatus take advantage of the inherent storage capability of the non-photosensitive sites by using them to hold image information pending application of the readout signal, thereby, conserving the host resources.
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METHODS AND APPARATUS FOR CHARGE COUPLLED DEVICE IMAGE ACQUISITION WITH INDEPENDENT INTEGRATION AND READOUT

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Background of the Invention

This application claims the benefit of priority of United States Provisional Patent Application Serial No. 60/050,597, filed June 24, 1997, the teachings of which are incorporated herein by reference and a copy of which is attached hereto as Appendix A.

The invention pertains to image acquisition and, particularly, to the control and readout of images using charge coupled devices. The invention has application in video cameras and other image acquisition devices used in machine vision and in other industrial, research and recreational environments.

Manufacturers of video cameras and other digital image acquisition devices are increasingly reliant on charge coupled devices (CCD's) to capture images for real-time processing. These devices are made up of hundreds or thousands of microscopic semiconductor elements arranged in closely spaced arrays. When the array is exposed to light (or other radiation), each of its constituent elements accumulate an electronic charge proportional to the number of photons that strike it. By focusing a scene on such an array, an electronic image is formed with brighter regions of the scene corresponding to more highly charged elements and darker regions corresponding to less highly charged ones.

Typically, only one-half of the elements in a CCD array are used to collect light. In one prior art design, referred to as the interline transfer CCD, rows (or columns) of photosensitive elements are alternated with rows (or columns) of nonsensitive elements. The latter serve as "conduits" to transfer the electronic charges from the photosensitive elements to an output buffer, or readout register.
The acquisition of an image in a typical CCD array occurs over several phases. To begin, the photosensitive elements are grounded or "reset" to remove all previously accumulated charge. Once this is completed, light (or other energy) from a lens begins to accumulate, forming an image. Since CCD devices are not typically equipped with mechanical shutters, accumulation continues until the charges built-up in each of the photosensitive elements are transferred to the corresponding non-photosensitive elements. The period following the reset and before the transfer is, accordingly, referred to as the integration or shuttering period.

According to prior art image acquisition system designs, once the integration period ends, the charges transferred to the non-photosensitive elements are immediately and quickly shifted across (or down) each row (or column) of non-photosensitive elements to the readout register. From there, they are loaded into to the memory of the host device (e.g., video workstation) into which the CCD has been incorporated.

Another type of prior art CCD array, the full frame CCD, is configured differently from the interline CCD, but is operated similarly. Rather than having interleaved rows of photosensitive and non-photosensitive elements, the photosensitive elements are disposed together on one-half of the array; the latter, on the other half. Once the integration period ends, the charges accumulated in the photosensitive elements are shifted from neighbor to neighbor until they occupy corresponding elements on the non-photosensitive half, whence they are transferred via the readout array to the host memory.

Regardless of which prior art CCD design is used, prior art image acquisition system designs require that memory be dedicated in the host device to receive the image data as it streams from the readout register. Sufficient bandwidth must also be provided on the bus or other communications path to insure that the streaming data is not lost en route to the memory. Still further, because the CCD devices typically operate with their own internal clocks, the host must be designed to accommodate asynchronous transfers from the readout register.
For example, conventional machine vision systems using a CCD camera based upon one of the popular video standards (i.e. RS170 or CCIR) have no control over when the image data is output by the CCD’s, since they are constantly outputting new video information after each vertical blanking interval. In applications that use electronic shuttering, on the other hand, the host must be ready to accept the video information immediately following the termination of the integration period, since there exists no mechanism which would allow the readout of the data to be postponed.

An object of this invention is to provide improved methods and apparatus for image acquisition and, more particularly, improved methods and apparatus using charge coupled devices to acquire images.

Another object is to provide such methods and apparatus as reduce the resources required for, and costs associated with, image acquisition.

Still another object of the invention is to provide such devices and methods as permit greater control of image acquisition.

Yet still another object of the invention is to provide such methods and apparatus as are adapted to use in multicamera environments, e.g., where multiple images must be acquired synchronously or asynchronously.
Summary of the Invention

The foregoing are among the objects attained by the invention, which provides methods and apparatus for image acquisition that take advantage of the inherent storage capability of charge coupled device (CCD) devices. By separating the integration and readout functions of such devices, the invention permits image acquisition apparatus (e.g., video camera) or systems into which they are incorporated (e.g., machine vision systems) to control the flow of image information, e.g., to reduce the bus and memory resources required to carry it, to time its arrival with other information or images, and/or to coordinate its arrival with the availability of processing resources.

Thus, in one aspect, the invention utilizes a charge coupled device that includes a photosensitive region, with photosensitive charge collection sites, and a non-photosensitive region, with non-photosensitive readout sites. The readout sites are coupled directly (e.g., as in an interline format) or indirectly (e.g., as in a frame transfer format) to the charge collection sites. The photosensitive region responds to an applied transfer signal by transferring charge accumulated on the collection sites to the corresponding readout sites. The non-photosensitive region responds to a read signal, applied independently of the transfer signal, by outputting (e.g., to a host camera or image acquisition system) charges in the readout sites.

Unlike prior art acquisition devices, in which initiation of a transfer cycle leads directly to the output of image information from the readout sites, an acquisition device according to the invention executes transfer and readout functions independently. Thus, although the transfer and readout signals may be applied substantially simultaneously (thus, emulating prior art systems), they need not be. By delaying application of the readout signal, image information in the readout sites can be retained until the host is ready to receive it.
The apparatus further includes a control unit that responds to requests, e.g., from a host system, by generating and applying to a head unit signals for acquiring an image. The head unit responds to those signals by acquiring image information output from the CCD and generating a video signal for application to the control unit and/or the host.

Related aspects of the invention provide an image acquisition apparatus as described above in which the acquisition signal generated by the control unit include a shutter pulse that defines at least a duration of charge integration by the CCD, and a readout signal that causes charges on the CCD readout sites to be outputted, e.g., to the head unit. The head unit can respond to such a shutter pulse by applying to the CCD a reset signal that clears its charge collection sites. The head unit can subsequently apply a transfer signal to the charge collection sites, causing them to transfer their charge to the readout sites. Application of the transfer signal can be timed to effect an integration period in accord with that defined by the shutter pulse. The head unit can respond to a readout signal from the control unit by applying to the CCD a read signal that causes the charges to be transferred from the non-photosensitive sites to a readout register, buffer or other store.

Still further aspects of the invention provide an image acquisition apparatus as described above in which multiple head units are provided, each associated with a respective CCD. The control unit of such can apparatus can effect synchronous image acquisition from those head units by applying shutter pulses substantially concurrently to them. Alternatively, the images can be acquired asynchronously via application of shutter pulses at different times. Whether image acquisition is synchronous or asynchronous, the control unit can control image transfer from the head units by applying readout signals to them independently of the application of the shutter pulses. Thus, for example, in response to requests from the host, the control unit can cause images acquired simultaneously by multiple head units to be output to the host memory in any desired order.
In still further aspects, the invention provides methods for image acquisition paralleling operation of the devices and apparatus described above.

Systems in accord with the invention have a many advantages over the prior art. By taking advantage of the inherent storage capability of CCD readout sites and separating their integration functions from the readout functions, the invention provides greater control of, and reduces the resources required for, the image acquisition process. In machine vision, for example, such systems are well suited to those applications which require that the acquisition of images overlap the inspection process. Here, inspection of an image can be completed without diverting processor resources (e.g., memory and bus cycles) to acquisition of a subsequent image. Instead, the host can instruct the control unit simply to acquire the subsequent image and to defer resource-consuming transfers until processing of the prior image is completed.

Moreover, in applications requiring acquisition of multiple images, systems according to the invention can utilize a single video path (e.g. amplifiers, D.C. restoration circuits, anti-aliasing filters, A/D converters) efficiently among multiple head units. For example, a control unit can apply integration pulse signals simultaneously to the multiple head units, yet, apply the readout signals serially so that only a single video path is required to condition the resultant image signals for transfer to the host. This contrasts with prior art image acquisition technology, which would require a unique datapath for each camera head unit.
Brief Description of the Drawings

A more complete understanding of the invention may be attained by reference to the drawings, in which:

Figures 1a - 1b depict charge coupled devices (CCDs) of the type used in practice of the invention;

Figure 2 depicts an image acquisition apparatus according to the invention having a single camera head unit;

Figure 3 depicts a camera head unit utilized in an image acquisition apparatus according to the invention;

Figure 4 depicts a camera control unit utilized in an image acquisition apparatus according to the invention;

Figure 5 depicts the timing of signal generation in an image acquisition of the type shown in Figure 2;

Figure 6 depicts an image acquisition apparatus according to the invention having multiple camera head units;

Figure 7 depicts the timing of signal generation in an image acquisition of the type shown in Figure 6 that acquires multiple images synchronously; and

Figure 8 depicts the timing of signal generation in an image acquisition of the type shown in Figure 6 that acquires multiple images asynchronously.

Detailed Description of the Illustrated Embodiment
With reference to Figure 1a, there is shown a CCD 10 of the type used to practice the invention configured in accord with the interline format. The CCD 10 alternates columns of photosensitive charge collection sites 12 (also referred to as picture elements or pixels) with columns of non-photosensitive (i.e. protected) readout sites 14. In the illustrated embodiment, each charge collection site is coupled to a corresponding (and, typically, adjacent) non-photosensitive site in the conventional manner.

Though there is a one-to-one correspondence between photosensitive and non-photosensitive sites in the illustrated embodiment, other embodiments of the invention may employ other relationships (e.g., four photosensitive sites to one non-photosensitive site, and so forth). The non-photosensitive sites are, moreover, coupled to one another in the conventional manner that permits charge to be output to a readout register 16 and, from there, to other components of the image acquisition system.

With reference to Figure 1b, a CCD 18 of the type used to practice the invention configured in accord with the frame transfer format does not interleave the charge collection 20 and readout sites 22 but, rather, places them on two distinct halves of the device. In this embodiment, the photosensitive and non-photosensitive sites are coupled to one another in the conventional manner (i.e., with some photosensitive sites being coupled indirectly via other photosensitive sites to non-photosensitive sites) in order to permit charge collected in the former to be moved to the latter and, thereafter, to the readout register 24.

In order to produce an image, the CCD's 10, 18 employ three basic cycles. The first, the reset cycle, is used to clear any residual charges from the photosensitive areas, effectively forcing the pixels to black. The next step, the transfer cycle (commonly referred to as the charge transfer interval), moves the charges accumulated since the most recent reset cycle into the non-photosensitive readout
sites. Since the amount of charge accumulated is proportional to the length of time between the reset and transfer cycles, the difference (in time) between these two constitutes an electronic shutter mechanism.

The final step, the readout cycle, is used to move or output the charges to the Camera Head Unit, which combines them with timing information to form an image signal for application to the Camera Control Unit (CCU). This step, requiring a vertical transfer clock sequence, involves moving an entire line of pixels from their protected cells into the readout register. Once there, the pixels are then shifted out serially using a series of horizontal transfer clock cycles at a rate dictated by the Camera Head Unit's (CHU's) internal clock rate. The total number of horizontal clock cycles per line and vertical clock cycles per frame is dictated by the number of rows and columns contained within the CCD.

In the CCD of Figure 1a, the transfer cycle is initiated over line 26 which is coupled to the photosensitive sites 12 (and other elements of CCD 10) in a conventional manner such that application of a transfer signal causes charges accumulated on sites 12 to be transferred to the non-photosensitive sites 14. A readout cycle is likewise initiated by a line 28 such that application of a readout signal causes charges stored on sites 14 to be transferred to the readout register 16. Referring to Figure 1b, CCD 18 is similarly equipped with lines 30, 32 that carry signals for initiating transfer and readout cycles for that device.

The reset cycle of CCD's 10 and 18 can be initiated over further lines (not illustrated) or, preferably, over lines 26, 30, in a conventional manner. Thus, for example, CCD 10 can be arranged such that a reset signal applied to such a line causes any charges accumulated in the photosensitive elements 12 to be cleared.

Unlike prior art image acquisition system, in which initiation of a transfer cycle leads directly to transfer to the readout register of charges accumulated on
photosensitive sites, the illustrated embodiment permits the transfer and readout functions to be executed independently. Thus, although they the transfer and read signals may be sent at substantially the same times or in quick succession (thus, emulating prior art systems), they need not be. By delaying the read signal, the illustrated embodiment permits the accumulated charges (i.e., the image) to be retained in the non-photosensitive sites, e.g., rather than in the readout register 18 or other memory of the acquisition system or its host.

Figure 2 illustrates a video camera or other such single head image acquisition system 33 according to the invention. The system includes Camera Head Unit (CHU) 34 and associated Camera Control Unit (CCU) 36. The system 33 and, specifically, the CCU 36 communicates with a host computer, or other control apparatus (not shown), via a System Bus 38. A lens, through which scenes are focussed on the CCD, is not shown.

The Camera Control Unit 36 services requests for new images by processing commands received from the host (e.g., a host digital data processing system) over the System Bus 38 and, in turn, issues the Shutter_L and Readout_L pulses to the CHU 34, as illustrated. The Shutter_L pulse is used to control the integration time of the Camera Head Unit (CHU). It includes two parts, a first that causes the photosensitive sites in the CCD to clear (or reset) so that acquisition of a new image can begin, and a second that causes image-representative charges on those sites to be transferred to the non-photosensitive sites. The Readout_L signal initiates the readout cycle.

The CHU 34, which includes a CCD, e.g., of the type shown in Figures 1A or 1B, responds to the applied Shutter_L and Readout_L signals for acquiring an image and transmitting it back to the CCU 36, as indicated by the image signal labeled "video." Along with the image signal, the CHU 34 returns a clocking signal,
PCLK, that indicates the timing of the video signal and a data valid signal, DATA VALID_L, identifying that portion of the video signal containing valid image data.

A detailed block diagram of Camera Head Unit (CHU) 34 is illustrated in Figure 3. As shown there, a Decoder 40 is used to synchronize the Shutter_L and Readout_L signals with the Camera Head Unit’s 34 internal clocking and to generate a pulse to the CCD Timing Generator 42 to initiate each of the CCD clock cycles required to create an image and transfer it to the Camera Control Unit (CCU) 36.

More particularly, in response to an applied Shutter_L signal, the Decoder 40 generates a Reset pulse instructing the CCD Timing Generator 42 to clear the photosensitive areas of the CCD, via application of a Reset signal, in preparation for a new integration cycle. In accord with the pulse width of the Shutter_L signal, the Decoder 40 subsequently generates a transfer pulse informing the CCD Timing Generator 42 that the integration cycle has expired and that the charge currently residing in the photo-sensitive areas of the sensor needs to be moved into the non-photo-sensitive readout sites, i.e., via application of a transfer signal to the CCD. Moreover, in response to the Readout_L signal, the Decoder 40 applies to the Timing Generator 42 a Read signal indicating that the Camera Control Unit (CCU) 36 is ready to accept the image and that the sequence of vertical and horizontal transfer cycles required to read the contents of the CCD sensor should be executed.

As noted above, in response to the foregoing, the Camera Head Unit (CHU) 34 transfer the CCD-acquired image to the CCU 36 via a video signal (Video), a pixel clock (PCLK), and a data validation signal (Data Valid_L).

Figure 4 illustrates a Camera Control Unit (CCU) 36 that can be used to support a single head image acquisition system of the type shown in Figures 2 - 3, as well as a multihead system of the type described below. In the illustration, an Acquire Timing Generator 44 processes commands received from the host computer
(not shown) via the System Bus. Since a single Camera Control Unit (CCU) 36 preferably supports configurations with multiple Camera Head Units (CHUs), a set of shutter (Cl Shutter_L ... CnShutter_L) and readout (Cl Readout_L ... CnReadout_L) controls are derived for each potentially installed CHU. Similarly the Acquire Timing Generator 44 accepts the pixel clock (Cl PCLK ... On PCLK), data validation signals (Cl DataValid_L ... CnDataValid_L), and video wave forms (Cl Video ... CnVideo) from each installed CHU.

As shown in the drawing, the CCU 36 includes a video pre-processing circuit comprised of a video multiplexer (Mux) 46 and programmable gain (Gain Adjust) 48. In a preferred embodiment, that gain is set in accord with the ratio of full scale digitizer (A/D) input versus full scale video output from the CHU 34. The programmable gain 48 can also be used to increase the amplitude of the video signal in low light situations where extending the integration time (i.e. the width, in time, of the CnShutter_L pulse) is not an option. Those skilled in the art will, of course, appreciate that the gain can be set and utilized in other ways conventional in the art.

A level correction (D.C. Restoration and Offset Adjust) 50 is provided to eliminate any residual offsets from the video signal. In a preferred embodiment, level correction is set at a value determined in accord with calibration or other training parameters, though it can be set in other ways conventional in the art.

The Acquire Timing Generator 44 is responsible for performing D.C. restoration of the video signal. It achieves this by asserting a Clamp signal, as illustrated, at a point in the video signal where it has been pre-determined that a black level should be present. In a preferred embodiment, that pre-determined point is set in accord with signal characteristics of the CHU 34.

The Acquire Timing Generator 44 is also responsible for producing a clock (AD-CLK) for the analog to digital convertor (A/D) 52, which samples the video signal at
its optimum point to ensure maximum accuracy. In a preferred embodiment, that optimum point is set in accord with signal characteristics of the CHU 42.

Since illustrated Camera Control Unit 36 contains only one video path, the video multiplexer (Mux) 46 is used to select the proper video signal (C0Video ... CnVideo). This is controlled by means of the Camera Head Unit select (CHUSEL) signal which emanates from the Acquire Timing Generator 44, as shown. The CHUSEL signal is also used to select the proper set of pixel clock and data validation signals (C0PCLK ... CnPCLK, C0DataValid_L ... CnDataValid_L).

Digitized image data emanating from the A/D converter 52, as represented by signal ImageData(N-1 :0), is transferred to the host computer via the System Bus 38 under the control of the Acquire Timing Generator 44.

Figure 5 illustrates the timing sequence for image acquisition in the embodiment shown in Figures 2 - 4 involving only a single Camera Head Unit 34. The host computer (not shown) first initializes the CCU’s Acquire Timing Generator 44 for the type of acquire (to wit, single CHU), the integration interval. The host computer also selects a Camera Head Unit (CHU) by setting the CHUSEL signal to the appropriate value (e.g. 0 for CHU 0, 1 for CHU 1, and so forth).

When the Acquire Timing Generator 44 receives a start of integration command from the host computer, it immediately asserts the shutter signal (C0Shutter_L in this example) for the selected Camera Head Unit (CHU). The high to low transition (i.e. leading edge) of the C0Shutter_L pulse is detected by the Decoder located inside the Camera Head Unit 34 (see Figure 3) which then asserts the Reset signal. Upon sensing the Reset signal, the CCD Timing Generator 42 executes the CCD sensor clock sequence required to clear out any charge remaining in the photo-sensitive areas of the CCD sensor.
The integration period is terminated by the low to high transition (trailing edge) of the C0Shutter_L pulse. This edge, when sensed by the Decoder 40, causes it to issue the Transfer pulse which in turn informs the CCD Timing Generator 42 that all of the charge currently residing in the photo-sensitive collection wells needs to be transferred to the corresponding non-photo-sensitive (i.e. protected) readout sites.

Once the charge transfer cycle is complete, the image is ready to be transmitted to the Camera Control Unit (CCU) 36. No further action is taken until the host computer informs the Acquire Timing Generator 44 that it is ready to accept the image. Upon receiving a readout instruction from the host computer, the Acquire Timing Generator 44 asserts the readout signal, C0Readout_L in this example. The high to low transition (i.e. leading edge) of this signal causes the Decoder 40 circuit inside the Camera Head Unit (CHU) 34 to issue a Read strobe. This pulse causes the CCD Timing Generator 42 to commence the sequence of vertical and horizontal clock cycles required to completely transfer the image residing in the readout cells to the Camera Control Unit (CCU) 36 where it is digitized and passed along to the host computer via the System Bus 38.

The data validation signal (C0DataValid_L in this example) is issued by the Camera Head Unit (CHU) 34 and is used by the Camera Control Unit 36 to distinguish between valid and invalid portions of the video signal. The pixel clock (C0PCLK, not shown in this example) ensures that the video signal (C0Video, not shown in this example) is sampled at its’ optimum point to maximize the accuracy of the digitalization process.

Figure 6 shows an image acquisition system 54 according to the invention comprising multiple Camera Head Units CHU0, CHU1, . . . , CHU n and their associated Camera Control Unit (CCU) 36. The CHU’s CHU0, CHU1, . . . , CHU n are constructed and operated identically to CHU 34, discussed above. CCU 36 operates as described above, albeit in a manner intended for controlling multiple CHU’s.
As discussed above, CCU 36 acquires an image in response to requests received from the host via the System Bus 38. In addition to the simple image acquisition sequence described for the single camera head embodiments described earlier, the multihead embodiment of Figure 6 supports synchronous and asynchronous shuttering.

The synchronous shutter mode, illustrated in Figure 7, allows multiple Camera Head Units (CHUs) to start their integration cycles at precisely the same time based upon a single write cycle from the host computer. This mode allows a system requiring multiple views of the same object to precisely control the operation of multiple cameras, resulting in images which are different views of the same object at a single moment in time. An alternative use of this mode could include operating multiple cameras in parallel so that each could capture an image of a different object in parallel, potentially increasing the efficiency of the inspection system.

Referring to Figure 7 multiple shutter pulses (C0Shutter_L ... CnShutter_L) resulting from a single write cycle from the host computer communicating with the Camera Control Unit (CCU) 36 via the System Bus 38. The widths of the shutter pulses, and hence the integration time for each camera, may be identical or of varying lengths, depending upon the illumination conditions for each Camera Head Unit CHU0 - CHUn.

Following the completion of the shutter interval, the image stored in each CCD is then transferred to the host computer via the System Bus 38 under the control of the Camera Control Unit (CCU) 36. More particularly, the host requests an image by instructing the Camera Control Unit (CCU) 36 to assert the readout pulse (C0Readout ... CnReadout_L) for the next image requiring analysis. Since the host initiates the readout process, the order in which images are transferred from the
Camera Head Units CHU0 - CHUn is under host control and need not necessarily be in any particular order nor need it be fixed from one set of acquires to the next.

Each readout pulse (C0Readout_L ... CnReadout_L) causes the CCD Timing Generator 42 located in the corresponding Camera Head Unit CHU0 - CHUn to commence the sequence of vertical and horizontal clock cycles required to completely transfer the image residing in the readout cells of the corresponding CCD to the Camera Control Unit 36, where it is digitized and passed along to the host computer via the System Bus 38. The data validation signals (C0DataValid_L ... CnDataValid_L in this example) are issued by the Camera Head Units CHU0 - CHUn and are used by the Camera Control Unit 36 to distinguish between valid and invalid portions of the video signals transmitted from each CHU. The pixel clock generated by each Camera Head Unit, CHU0 - CHUn, ensures that the video signal is sampled at its optimum point to maximize the accuracy of the digitalization process. The correct video and pixel clock signal are selected via the CHUSEL (Camera Head Unit SELect) signals within the Camera Control Unit (CCU, refer to Figure 4).

With reference to Figure 8, the asynchronous shutter operation of involving multiple Camera Head Units CHU0 - CHUn is shown. This mode allows a single Camera Control Unit 36 to control two or more Camera Head Units in a completely independent manner. The net effect is that each Camera Head Unit CHU0 - CHUn is operating as though it were attached to its own dedicated Camera Control Unit (CCU) 36.

In the illustration, the host initiates integration and readout cycles for each Camera Head Unit (CHU) by writing the appropriate commands to the Camera Control Unit (CCU) 36, via the System Bus 38. The CCU 36, in turn, issues the necessary shutter (C0Shutter_L ... CnShutter_L) and readout (C0Readout_L ... CnReadout_L) pulses. Since the CHUs are operating autonomously, the shutter operation for one CHU may overlap with the shutter or readout operations of the other CHUs, as illustrated in Figure 8.
As with the synchronous shutter mode, the host computer has complete
control over the sequence of shutter and readout cycles for each Camera Head Unit
CHU0 - CHUn via the Camera Control Unit (CCU) 36. The host, accordingly,
determines the order and frequency with which images are acquired from any
particular Camera Head Unit CHU0 - CHUn.

To this end, each readout pulse (C0Readout_L ... CnReadout_L) causes the
CCD Timing Generator located in the corresponding Camera Head Unit (CHU) to
commence the sequence of vertical and horizontal clock cycles required to
completely transfer the image residing in the readout cells to the Camera Control
Unit (CCU) 36, where it is digitized and passed along to the host computer via the
System Bus. The data validation signals (C0DataValid_L ... CnDataValid_L in this
example) are issued by the Camera Head Units (CHUs) and are used by the Camera
Control Unit 36 to distinguish between valid and invalid portions of the video signals
transmitted from each CHU. The pixel clock ensures that the video signal from each
CHU is sampled at its optimum point to maximize the accuracy of the digitalization
process. The correct video and pixel clock signal are selected via the CHUSEL
(Camera Head Unit SELect) signals within the Camera Control Unit (CCU, refer to
Figure 4).

Described above are systems for image acquisition meeting the desired
objects. Those skilled in the art will, of course, appreciate that the illustrated
embodiments are merely examples of the invention and that embodiments
incorporating modifications thereto fall within the scope of the invention. Thus, for
example, it will be appreciated that the CCD configurations shown in Figures 1A -
1B are merely examples of the configurations that may be used with the invention.
By way of further example, it will be appreciated that the specific signals generated
and used within the illustrated embodiment are but examples of those that may be
used in operation of systems according to the invention. In view of the foregoing,
what I claim is:
APPENDIX

to

Patent Application for

METHODS AND APPARATUS FOR CHARGE COUPLED DEVICE IMAGE ACQUISITION WITH INDEPENDENT INTEGRATION AND READOUT
1. Mission Statement

This document contains the framework for a proposed camera architecture with advanced features required by the machine vision industry. The Cognex Digital Camera, henceforth referred to as the CDC, is intended to provide both OEMs and End-User’s with the most cost effective high performance video acquisition sub-system currently available. Our goals are to establish new standards for flexibility, speed, and image fidelity.

The contents of the specification are proprietary and should not be discussed or disclosed to others outside of the immediate working groups. The disposition of efforts between Cognex and the candidate vendor of the camera head assembly is as follows:

- Architecture.............................................. Cognex, Vendor
- Interface Specification................................. Cognex, Vendor
- Camera Head Specification............................. Cognex, Vendor
- Camera Acquire & Control Electronics Specification... Cognex
- Camera Head Design....................................... Vendor
- Camera Acquire & Control Electronics Design......... Cognex
- Camera Head Production.................................. Vendor
- Camera Acquire & Control Electronics Production..... Cognex
2. Architecture

This section contains a description of the proposed architecture for the camera head and controller board.

2.1 Sequential Acquire Model

Figure 1 shows the concept for a system in which a single Camera Acquire and Control Electronics would support sequential acquires from a maximum of four cameras. Alternatively, all four cameras could integrate images simultaneously and then place them in their interline vertical transfer registers where they would be held until readout was initiated.

![Diagram of CDC Block Diagram (PCI Bus Version)](image)

*Figure 1: CDC Block Diagram (PCI Bus Version)*

The video, clock, and camera timing signals are all transmitted differentially to ensure maximum signal integrity in noisy environments. CCD pixel correction is performed within the Camera Head coefficients downloaded from via the Command Interface after an initial cal-
Cognex Digital Camera (CDC) Design Specification

Iibration process has been executed at the factory. Alternatively, the calibration could be executed in the target system facilitating correction for overall system factors such as illumination flatness. The Acquire Timing logic located on the Camera Acquire and Control Electronics is responsible for processing external trigger events and supporting strobe firing.

2.1.1 Functional Description - Camera Head

The Camera Head contains eight functional elements. It should contain a single high density connector and will receive 'clean' regulated power from the Camera Acquire and Control Electronics. The substrate bias voltage (Vsub) should be generated locally. A separate connector for power is acceptable if required to meet performance. The functional elements of the camera head include:

1. **CCD**
   - The core of the camera head is the solid state image sensor. The initial CDC will use a 'medium format' array. The minimum sensor requirements are:
     - Interline technology
     - Square pixels (dx=dy)
     - Support for electronic shutter
     - Minimum horizontal clock rate of 25MHz (target frame rate is 60 frames/second)
     - Support sub-image readout (must be able to discard vertical lines with at least 2x normal readout rate)
     - Multiple resolutions
       - medium (640 pixels x 480 lines)
       - high (1024 pixels by 1024 lines)
     - Single chip color versions also desirable

2. **Vsub**
   - CCD substrate bias voltage generator.

3. **Command Interface**
   - Interprets commands issued by the Camera Acquire and Control module and instructs the CDC or Correction Map to perform specific functions. The minimum command set includes:
     - `Activate(c)` is used to select Camera Head c (c = 0, 1, 2, or 3) for operations which require the camera to transmit either Clock and Dvalid signals (e.g. Transfer(y) and Calibrate(y)) or command data (e.g. CorrectionRead()) to the Camera Acquire and Control Electronics.
     - `Integrate(f)` causes the CCD to be reset, integrated for f(us), then transferred to the interline vertical holding registers. It controls the electronic shutter function. Multiple cameras may be process the Integrate(f) command simultaneously.
     - `Transfer(y)` initiates a readout of the sensor. The first y lines are discarded and not transferred to the Camera Acquire and
Control Electronics. This command allows the CDC to perform Region-Of-Interest (ROI) readout.

- Calibrate() initiates a readout of the sensor but bypasses the Pixel Correction phase. This mode is required to pass the uncorrected data on to the Camera Acquire and Control Electronics where the actual correction values can be determined via special calibration software.

- CorrectionAddr(addr) is a pointer to the next address of the Correction Map to be accessed. It is stored locally in the Command interface upon receipt of this command.

- CorrectionRead() initiates memory read cycle of the Correction Map at the current address. Data is serialized in the Command Interface and transferred back to the Camera Acquire and Control Electronics. The Correction Map address is post incremented (addr++) after the data is read out.

- CorrectionWrite(data) initiates a write to the Correction Map at the current address. The Command Interface performs serial to parallel conversion of the data and executes a memory write cycle. The Correction Map address is post incremented (addr++) after the data is written.

4. CCD Timing

The timing generator is responsible for producing all of the signals required to execute the integration and readout phases of the CCD sensor. The timing generator is also responsible for controlling the correlated double sampling (CDS) sequence within the Video Processor as well as matching the CCD output pixel with the correct gain and level correction factors from the Correction Map.

The timing generator also sends the control signals associated with the image transfer process in RS-422 (differential TTL) format to the Camera Acquire and Control Electronics. The signals include:

- Clock+, Clock- (pixel clock)
- Dvalid+, Dvalid- (Data Valid indicator)

5. Video Processor

Implements correlated double sampling (CDS) noise reduction techniques and provides some minimum signal gain. The resulting video output is differential in order to support cable lengths of up to 5 meters.

6. Pixel Correction

Uses calibration values obtained from the Correction Map to adjust the gain and level of each pixel. This is intended to minimize the fixed pattern noise which results from imbalance in the charge creation process from one collection site to another, differences in the charge transfer efficiency, and other error sources which would result in uneven grey values for an image generated by exposing the sensor to a uniformly illuminated flat field target. The algorithm is fairly simple, consisting of gain and level correction.
Cognex Digital Camera (CDC) Design Specification

\[
\text{Video}(x,y) = G(x,y) \times \text{Pixel}(x,y) + O(x,y)
\]

Where:

- \( \text{Pixel}(x,y) \) is the post CDS pixel voltage
- \( G(x,y) \) is the gain correction factor
- \( O(x,y) \) is the offset correction factor
- \( \text{Video}(x,y) \) is the corrected video voltage

The resolution of \( G(x,y) \) and \( O(x,y) \) are TBD.

7. **Interface Electronics**
   Conditions the digital representation of the CCD sensor timing signals to meet the voltage levels required for proper sensor operation.

8. **Oscillator**
   Provides a stable crystal timing reference for all camera operations and data transfer operations between the Camera Head and the Camera Acquire and Control Electronics.

### 2.1.2 Functional Description - Camera Acquire and Control Electronics

The Camera Acquire and Control Electronics contains 6 functional elements. The module contains a high density connector for communications and supplies 'clean' regulated voltages to the Camera Head. The module is based upon Cognex’s proprietary Vision Module (CVM) concept and can be utilized with the 5900 Video Processor as well as all members of the 8000 family. All signals required to support the CVM electrical interface pass through the CVM Interface Connector. The functional elements of the Camera Acquire and Control Electronics include:

1. **Camera Multiplexer**
   4:1 differential input multiplexer. It allows a single Camera Acquire and Control module to support a maximum of four Camera Heads units.

2. **Amp & Low Pass Filter**
   This video pre-processing is necessary to adjust the video signal to that required by the A/D converter for maximum performance while the low-pass-filter is used to perform classical Nyquist bandwidth limiting to eliminate aliasing.

3. **A/D Converter**
   Flash type device which supports conversion rates up to 30MHz and is TTL compatible.

4. **Acquire Timing**
   Controls the digitization process and generates all the video timing required by the CVM interface based upon the sense of the Clock and Valid signals. Each acquire is 'armed' via the Command Interface so the Acquire Timing knows which camera is active and when a new acquire in commencing.

5. **Command Interface**
   Translates standard CPU type bus structures (e.g. 68060, C80, local PCI bus) into serial command streams for processing by the installed Camera Head assemblies.

6. **DC/DC**
   Used to generate Camera Head supply voltage(s) from local bus...
Cognex Digital Camera (CDC)  

**Design Specification**

Converter references; either +5VDC or +12VDC. The voltage will be the largest required for camera sensor operation and could be further regulated using LDO linear regulators in the Camera Head to reduce noise picked up via the cable.

### 2.1.3 Camera Cable

It is desirable to support a minimum cable length of to 5 meters (approximately 15 feet). This is why the design uses the following formats for transmission of analog video, pixel clock and data validation controls, and command signals. Each set of differential signals will use twisted-pair copper as the transmission medium.

1. **Analog Video**
   - D.C. coupled differential signal with a peak-to-peak level of TBD volts. There are four sets of video signals, each dedicated to a particular Camera Head assembly.
   - For Video+
     
     \[
     V_{\text{black}} = 0.0 \text{ V} \\
     V_{\text{white}} = \text{TBD V}
     \]
   - For Video-
     
     \[
     V_{\text{black}} = \text{TBD V} \\
     V_{\text{white}} = 0.0 \text{ V}
     \]

2. **Pixel Clock and Uvalid**
   - Electrical interface is high performance RS-422 (differential TTL) using transmitters and receivers manufactured by Lucent Technology (formerly AT&T). These parts use pseudo-ECL signal levels for the differential signals and support frequencies up to 100MHz. These signals are tri-stated until a camera is selected (via the Command Interface) allowing them to be bussed between installed Camera Head assemblies and the Camera Acquire and Control Electronics.

3. **Command Interface**
   - Electrical interface is high performance RS-422 (differential TTL) using transmitters and receivers manufactured by Lucent Technology (formerly AT&T). These parts use pseudo-ECL signal levels for the differential signals and support frequencies up to 100MHz. The data portion of this interface is tri-stated until a camera is selected (via the Command Interface) allowing them to be bussed between installed Camera Head assemblies and the Camera Acquire and Control Electronics.

### 2.1.4 CVM Interface

This specification allows Cognex to design video option modules around a standard physical and electrical interface. This allows modules to be shared among multiple vision platforms.
2.2 Physical Dimensions - Camera Head

The goal is to keep the dimensions of the CDC as small as possible. The following dimensions and weight should be used only as guidelines. Cognex is willing to adjust the packaging parameters in the event it yields significant cost savings. Conversely, we do not want to incur additional costs just to reduce the Camera Head assembly to an absolute minimum.

1. Dimensions 22W x 22H x 50D
2. Weight 100g

2.3 Power Dissipation - Camera Head

The maximum power dissipation inside the Camera Head assembly is approximately 2.0W.
1. An image acquisition apparatus comprising:

A. a charge coupled device including a photosensitive region having one or more photosensitive charge collection sites, a non-photosensitive region having one or more non-photosensitive readout sites, the readout sites being coupled any of directly and indirectly to corresponding charge collection sites, the photosensitive region responding to an applied transfer signal for moving charges accumulated on the charge collection sites to corresponding non-photosensitive readout sites, the non-photosensitive region responding to a read signal applied independently of the transfer signal for outputting charges from the readout sites,

B. a head unit, coupled to the charge coupled device, that generates an image signal based on charges output from the readout sites.

2. An image acquisition apparatus according to claim 1, comprising

A. a control unit that responds to requests from a host by generating and applying to a head unit signals for acquiring an image, and

B. the head unit responding to signals applied thereto by the control unit for applying to the charge coupled device (i) a transfer signal for moving charges accumulated on the charge collection sites to corresponding readout sites, and (ii) a read signal causing charges to be output from the readout sites.

3. An image acquisition apparatus according to claim 1, wherein the control unit generates and applies to the head unit at least one of (i) a shutter pulse defining at least a duration of charge integration by the charge coupled device, and (ii) a readout signal that effects output of charges from the readout sites.
4. An image acquisition apparatus according to claim 3, wherein the head unit responds to the shutter pulse for applying to the charge coupled device a reset signal for clearing the charge collection sites and for applying to the charge coupled device a transfer signal for causing charges accumulated on those sites to be transferred to the readout sites.

5. An image acquisition apparatus according to claim 4, wherein the head unit applies the transfer signal to the charge coupled device subsequent to application of the reset signal so as to effect an integration period having a duration in accord with that defined by the shutter pulse.

6. An image acquisition apparatus according to claim 2, wherein the control unit includes a video path that conditions the image signal received from the head unit.

7. An image acquisition apparatus according to claim 6, wherein the video path includes a gain adjustment element that any of (i) adjusts a gain of the image signal received from the head unit, and (ii) increases an amplitude of that image signal.

8. An image acquisition apparatus according to claim 6, wherein the video path includes a level correction element that eliminates residual offsets in an image signal received from the head unit.

9. An image acquisition apparatus according to claim 1, comprising

A. a control unit that responds to a request from a host by generating and applying to a head unit (i) a shutter pulse defining at least a duration of charge integration by the charge coupled device, and (ii) a readout signal that effects output of charges from the readout sites,
B. the head unit responding to the shutter pulse for applying to the charge coupled device a reset signal for clearing the charge collection sites and for applying to the charge coupled device a transfer signal for causing charges accumulated on those sites to be transferred to the readout sites,

C. the head unit responding to the readout signal applied thereto by the control unit for applying a read signal to the charge coupled device for effecting output of charges in the readout sites, and

D. the control unit including a video path that conditions the image signal generated by the head unit from charges output from the readout sites.

10. An image acquisition apparatus according to claim 9, wherein the video path includes

i) a gain adjustment element that any of (a) adjusts gain of the image signal received from the head unit, and (b) increases an amplitude of that image signal, and

ii) a level correction element that any of eliminates residual offsets in an image signal received from the head unit.

11. An image acquisition apparatus comprising:

A. a plurality of head units, each including a charge coupled device, and each that generates an image signal from charges output from readout sites of the respective charge coupled device,

B. each charge coupled device including a photosensitive region having one or more photosensitive charge collection sites, a non-photosensitive region
having one or more non-photosensitive readout sites, the readout sites being coupled to corresponding charge collection sites, the photosensitive region responding to an applied transfer signal for moving charges accumulated on the charge collection sites to corresponding non-photosensitive readout sites, the non-photosensitive region responding to a read signal applied independently of the transfer signal for outputting the charges from the readout sites, and

C. a control unit, that is coupled to the plurality of head units, selectively generates and applies to each head unit signals for acquiring an image.

12. An image acquisition apparatus according to claim 11, wherein the control unit generates and applies to each head unit at least one of (i) a shutter pulse defining at least a duration of charge integration by the respective charge coupled device, and (ii) a readout signal that effects output of charges from the respective readout sites.

13. An image acquisition apparatus according to claim 12, wherein each head unit responds to the shutter pulse for applying to the respective charge coupled device a reset signal for clearing the charge collection sites and for applying to the respective charge coupled device a transfer signal for causing charges accumulated on those sites to be transferred to the readout sites.

14. An image acquisition apparatus according to claim 13, wherein each head unit applies the transfer signal to the respective charge coupled device subsequent to its application of the reset signal to that charge coupled device so as to effect an integration period having a duration in accord with that defined by the shutter pulse applied by the control unit to that head unit.
15. An image acquisition apparatus according to claim 11, wherein the control unit includes a video path that conditions image signals generated by the head units.

16. An image acquisition apparatus according to claim 15, wherein the video path includes

i) a gain adjustment element that any of (a) adjusts gain of the image signal received from the head units, and (b) increases an amplitude of that image signal, and

ii) a level correction element that any of eliminates residual offsets in an image signal received from the head units.

17. An image acquisition system according to claim 11, wherein the control unit has a synchronous mode of operation wherein it applies a shutter pulse signal substantially concurrently to a plurality of head units, and an asynchronous mode of operation wherein it applies shutter pulse signals to a plurality of head units at substantially different respective times.

18. An image acquisition system according to claim 17, wherein the control unit applies readout signals to plurality of head units at substantially different respective times.

19. An image acquisition system according to any of claims 17 - 18, wherein the control unit applies the shutter pulse and readout signals to the head units in accord with one or more requests received from a host.

20. A method of image acquisition using a charge coupled device of the type having
i. a photosensitive region having one or more photosensitive charge collection sites,

ii. a non-photosensitive region having one or more non-photosensitive readout sites, the non-photosensitive readout sites being coupled to corresponding photosensitive charge collection sites,

the method comprising the steps of

A. responding to an applied transfer signal for moving charges accumulated on the charge collection sites to corresponding readout sites, and

B. responding to a read signal applied independently of the transfer signal for outputting the charges in the non-photosensitive readout sites.

21. A method according to claim 20, comprising the step of responding to an applied reset signal for clearing charges on the charge collection sites.

22. A method according to claim 20, comprising the step of utilizing a head unit to generate an image signal based on charges output from the readout sites.

23. A method according to claim 22, comprising the steps of

A. utilizing a control unit to generate and apply to the head unit signals for acquiring an image, and

B. responding, with the head unit, to signals applied thereto by the control unit for applying to the charge coupled device (i) a transfer signal for moving charges accumulated on the charge collection sites to corresponding readout
sites, and (ii) a read signal causing charges to be output from the readout sites.

24. A method according to claim 23, comprising the step of utilizing the control unit to generate and apply to the head unit at least one of (i) a shutter pulse defining at least a duration of charge integration by the charge coupled device, and (ii) a readout signal that effects output of charges from the readout sites.

25. A method according to claim 24, comprising the step of responding, with the head unit, to the shutter pulse for applying to the charge coupled device a reset signal for clearing the charge collection sites and for applying to the charge coupled device a transfer signal for causing charges accumulated on those sites to be transferred to the readout sites.

26. A method according to claim 25, comprising the step of utilizing the head unit to apply the transfer signal to the charge coupled device subsequent to application of the reset signal so as to effect an integration period having a duration in accord with that defined by the shutter pulse.

27. A method according to claim 26, comprising the step of utilizing the control unit to condition the image signal generated by the head unit.

28. A method according to claim 20, comprising the step of utilizing a plurality of head units, each coupled to a respective charge coupled device to generate an image signal based on charges output from readout sites thereof.

29. A method according to claim 28, comprising the step of utilizing a control unit to selectively generate and apply to each head unit a signal for acquiring an image.
30. A method according to claim 29, comprising the step of utilizing the control unit to generate and apply to each head unit at least one of (i) a shutter pulse defining at least a duration of charge integration by the respective charge coupled device, and (ii) a readout signal that effects output of charges from the respective readout sites.

31. A method according to claim 30, comprising the step of utilizing each head unit to respond to an applied shutter pulse for applying to the respective charge coupled device a reset signal for clearing the charge collection sites and for applying to the respective charge coupled device a transfer signal for causing charges accumulated on those sites to be transferred to the readout sites.

32. A method according to claim 30, comprising the step conditioning the image signals generated by the head units with a common video path.

33. A method according to claim 30, comprising the step of applying a shutter pulse substantially concurrently to a plurality of head units.

34. A method according to claim 30, comprising the step of applying shutter pulses to a plurality of head units at substantially different respective times.

35. A method according to any of claims 33 - 34 comprising applying readout signals to plurality of head units at substantially different respective times.
FIG. 4
FIG. 6
FIG. 8

SUBSTITUTE SHEET (RULE 26)
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04N5/232 H04N5/335

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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<td>X</td>
<td>EP 0 777 381 A (CANON KK) 4 June 1997</td>
<td>1,6,9, 20,22,23</td>
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<td>Y</td>
<td>USE 5 506 617 A (PARULSKI KENNETH ET AL) 9 April 1996</td>
<td>1,20</td>
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Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance.

"E" earlier document but published on or after the international filing date.

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified).

"O" document referring to an oral disclosure, use, exhibition or other means.

"P" document published prior to the international filing date but later than the priority date claimed.

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention.

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone.

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"*" document member of the same patent family.

Date of the actual completion of the international search 8 September 1998

Date of mailing of the international search report 16/09/1998

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Authorized officer

Bequet, T
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<td>X</td>
<td>US 4 809 077 A (NORITA TOSHIO ET AL)</td>
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