US008697510B2

(12) **United States Patent**
Bhuwalka et al.

(10) **Patent No.: US 8,697,510 B2**
(45) **Date of Patent: Apr. 15, 2014**

(54) **TUNNEL FIELD-EFFECT TRANSISTOR WITH NARROW BAND-GAP CHANNEL AND STRONG GATE COUPLING**

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(73) Assignee: **Taiwan Semiconductor Manufacturing Company, Ltd.**, Hsin-Chu (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **13/741,086**

(22) Filed: **Jan. 14, 2013**

(65) **Prior Publication Data**

US 2013/0137236 A1 May 30, 2013

Related U.S. Application Data

(62) Division of application No. 12/880,236, filed on Sep. 13, 2010, now Pat. No. 8,354,695, which is a division of application No. 11/828,211, filed on Jul. 25, 2007, now Pat. No. 7,812,370.

(51) **Int. Cl.**

H01L 21/336	(2006.01)
H01L 21/02	(2006.01)
H01L 29/66	(2006.01)

(52) **U.S. Cl.**

USPC **438/197**; 438/306; 438/307; 257/288; 257/192; 257/E29.55; 257/E21.409; 257/E29.068

(58) **Field of Classification Search**

CPC H01L 29/7391; H01L 29/66356; H01L 21/26586; H01L 29/66545; H01L 29/66636

USPC 257/E29.55, 288, 192, E21.409, 257/E29.068; 438/197, 306, 307

See application file for complete search history.

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Primary Examiner — Ha Tran T Nguyen
Assistant Examiner — Thai T Vuong
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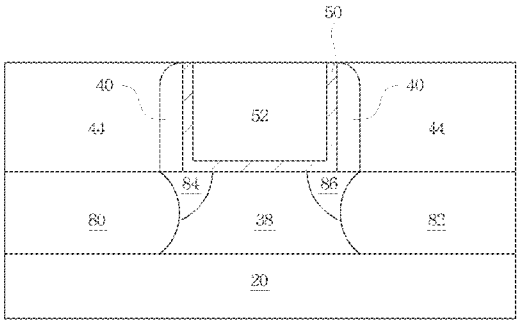
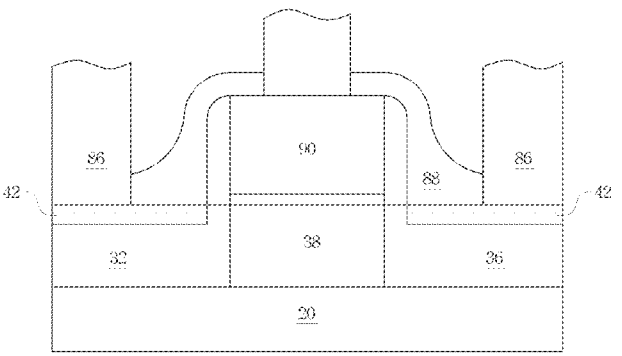
(57) **ABSTRACT**

A semiconductor device and the methods of forming the same are provided. The semiconductor device includes a low energy band-gap layer comprising a semiconductor material; a gate dielectric on the low energy band-gap layer; a gate electrode over the gate dielectric; a first source/drain region adjacent the gate dielectric, wherein the first source/drain region is of a first conductivity type; and a second source/drain region adjacent the gate dielectric. The second source/drain region is of a second conductivity type opposite the first conductivity type. The low energy band-gap layer is located between the first and the second source/drain regions.

20 Claims, 30 Drawing Sheets





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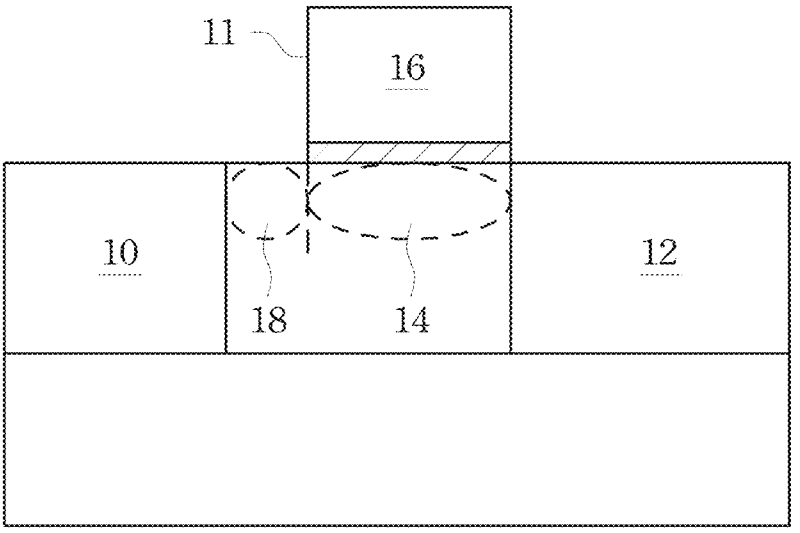

Fig. 1
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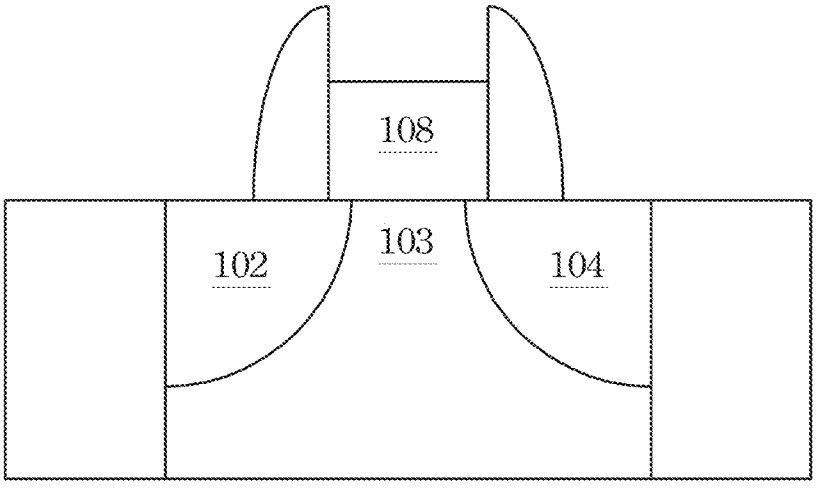
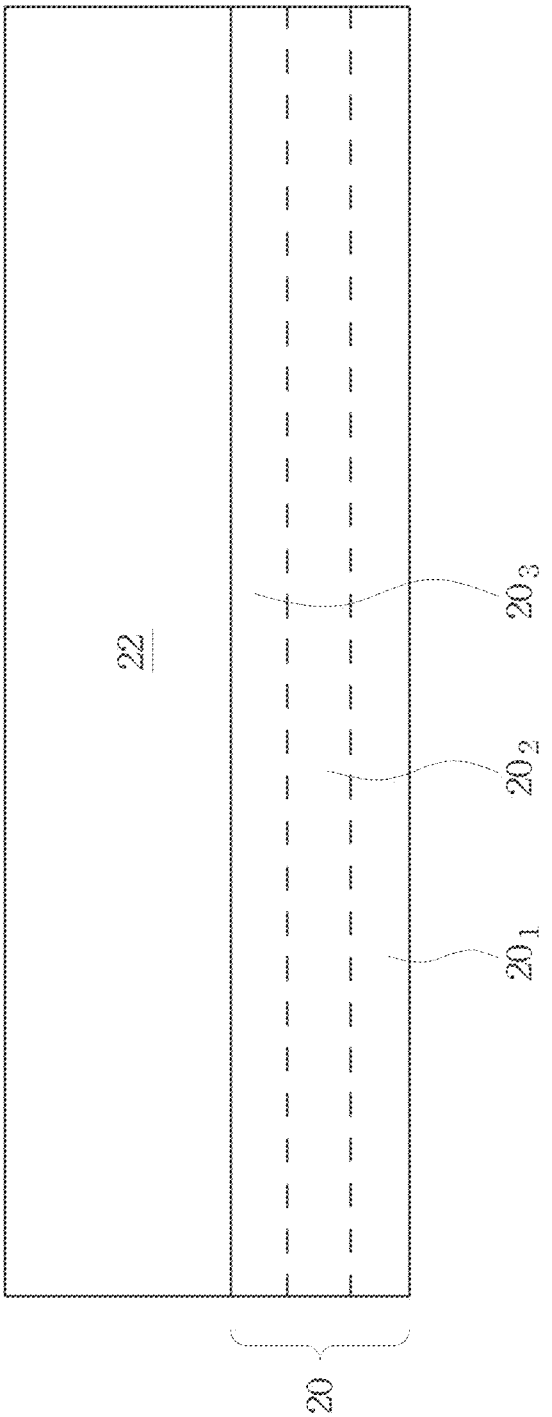


Fig. 2
(Prior Art)



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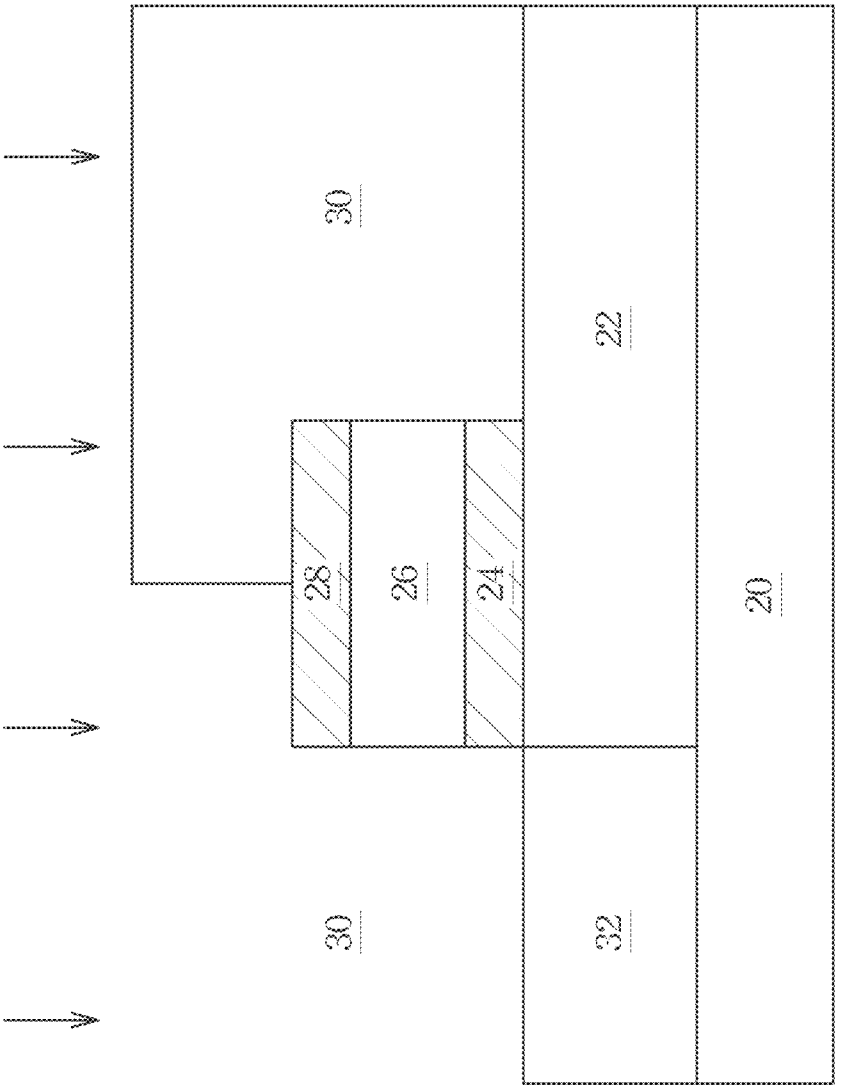


Fig. 4

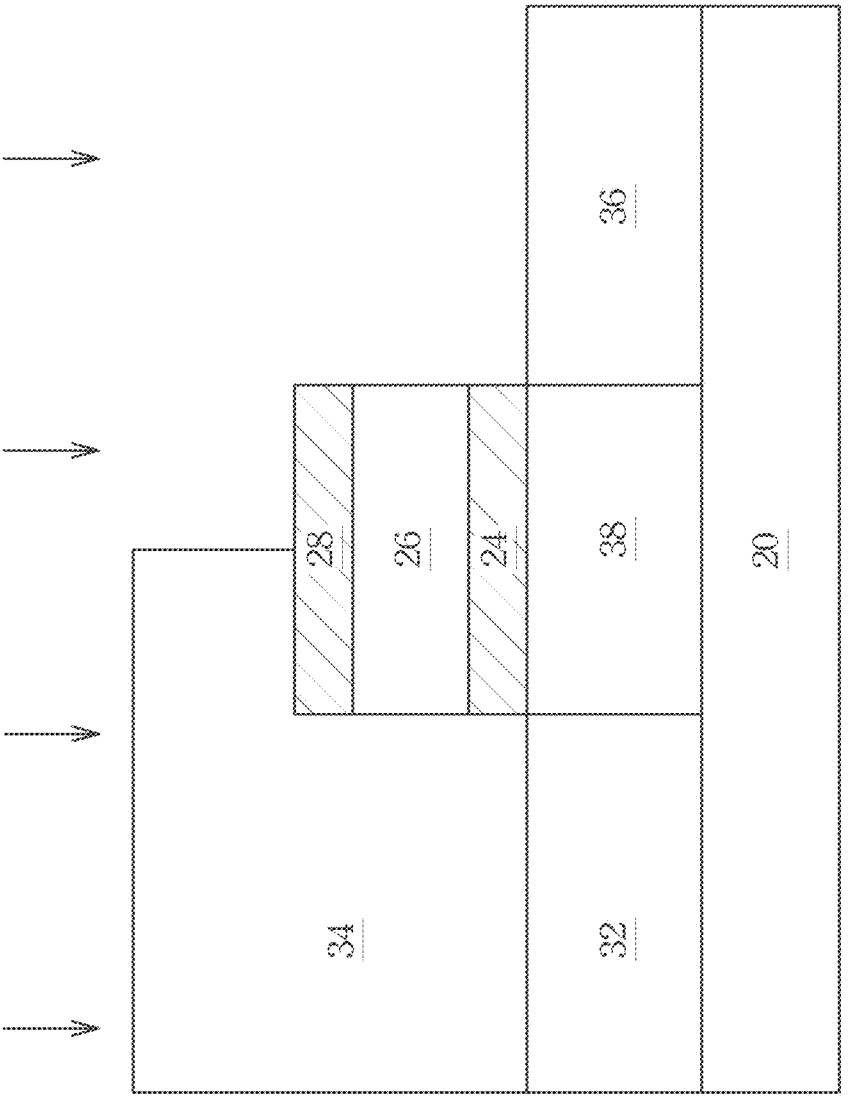


Fig. 5

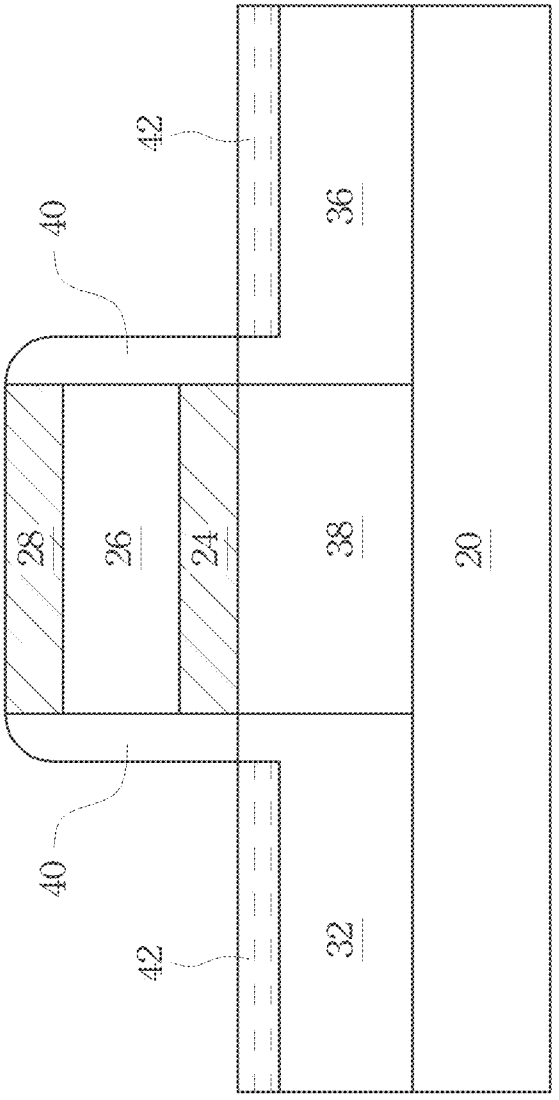


Fig. 6

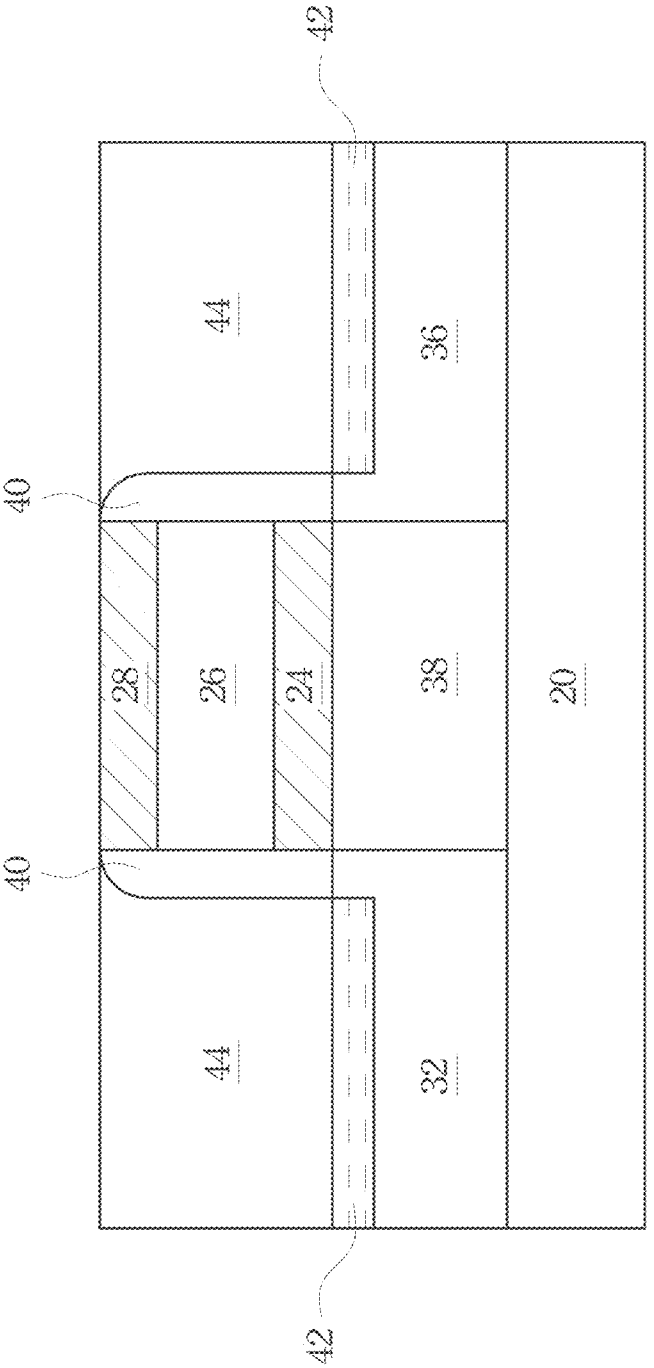


Fig. 7

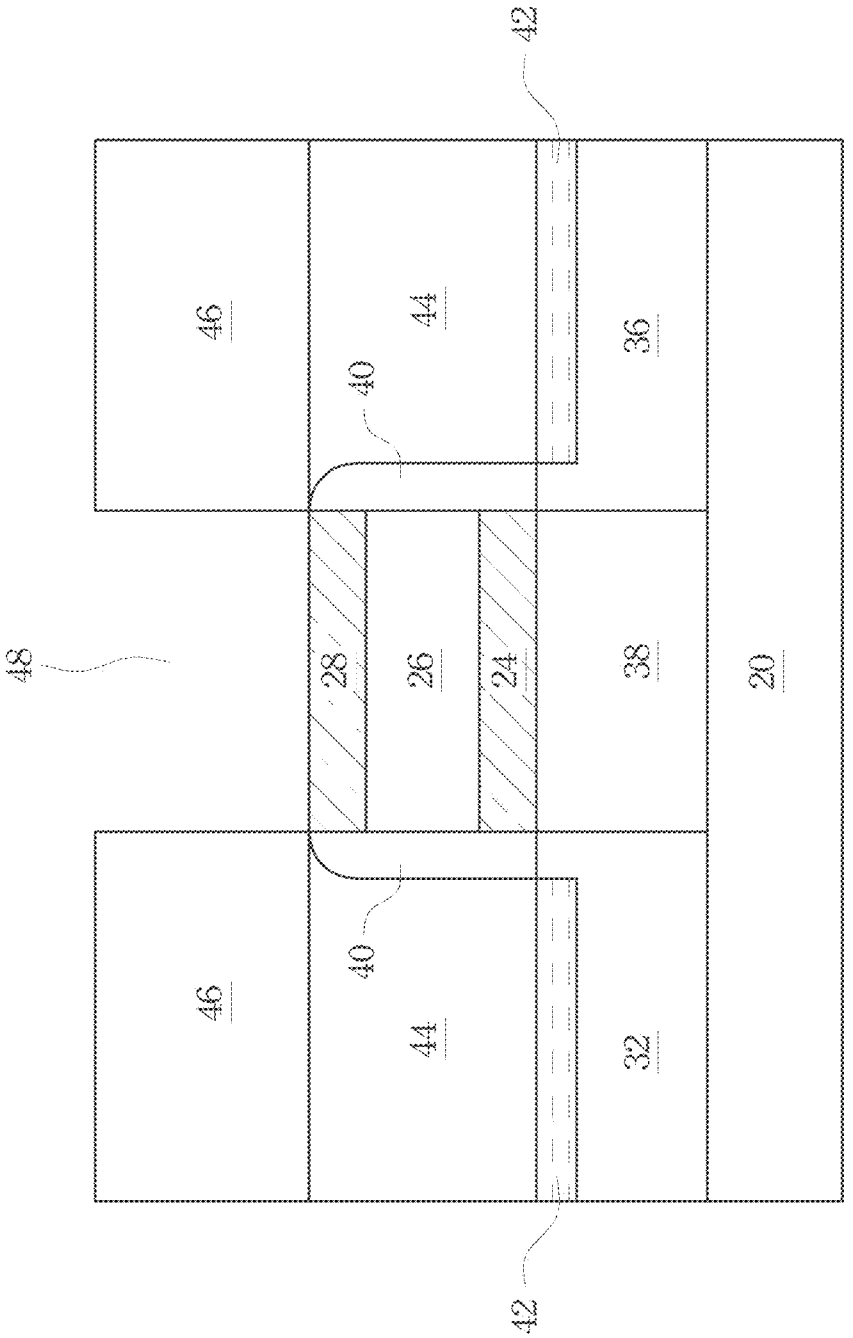
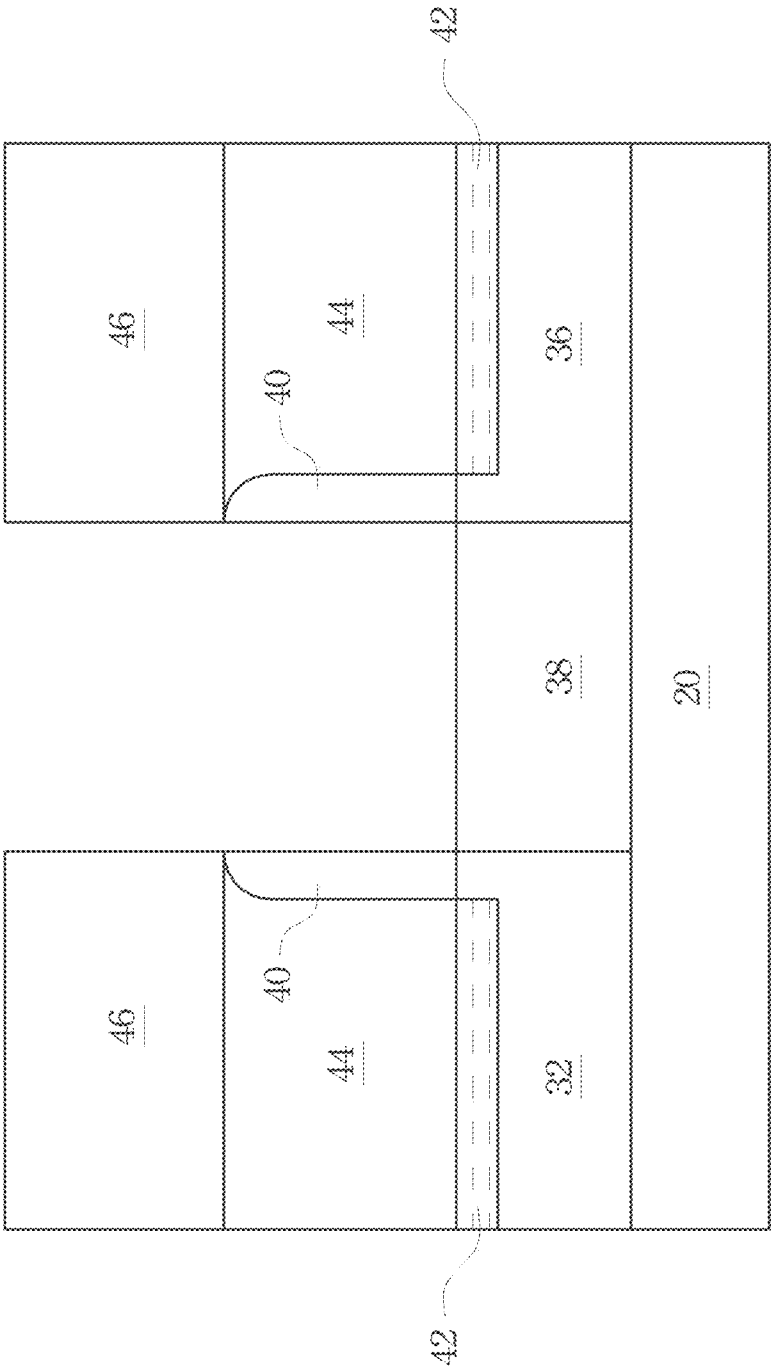


Fig. 8



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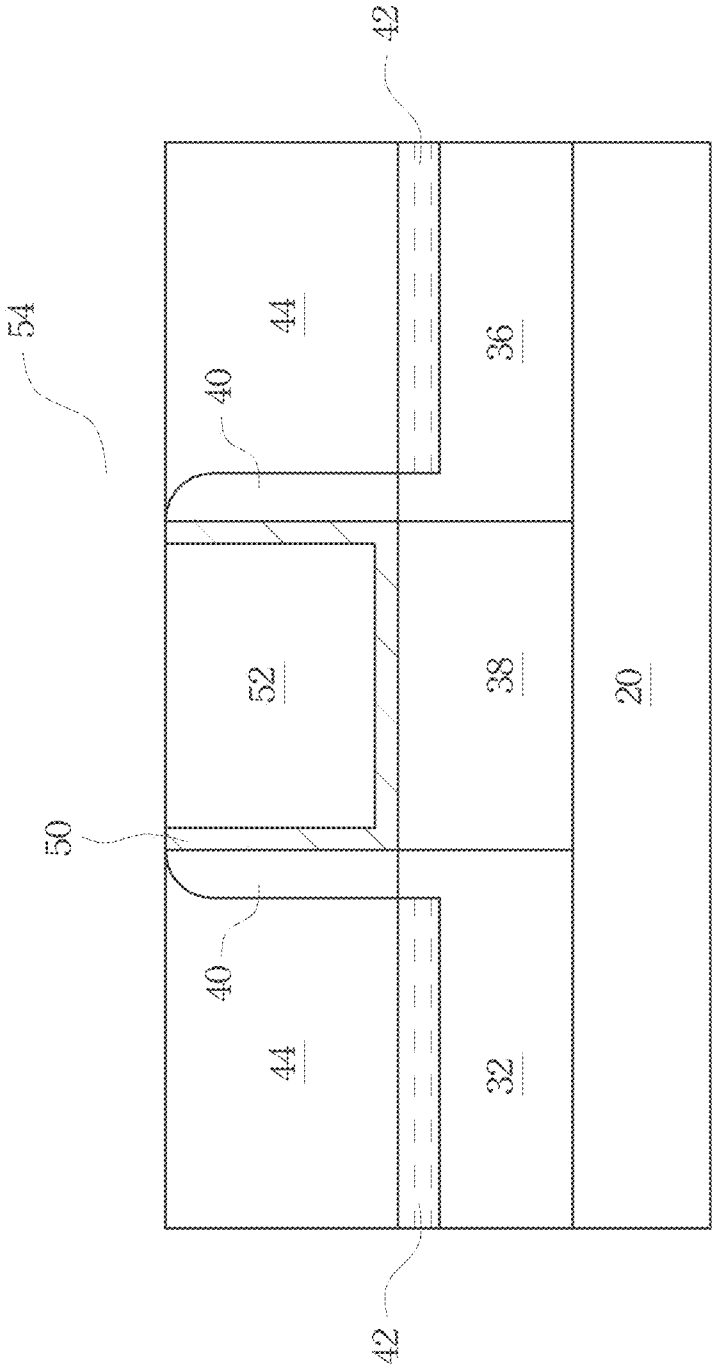

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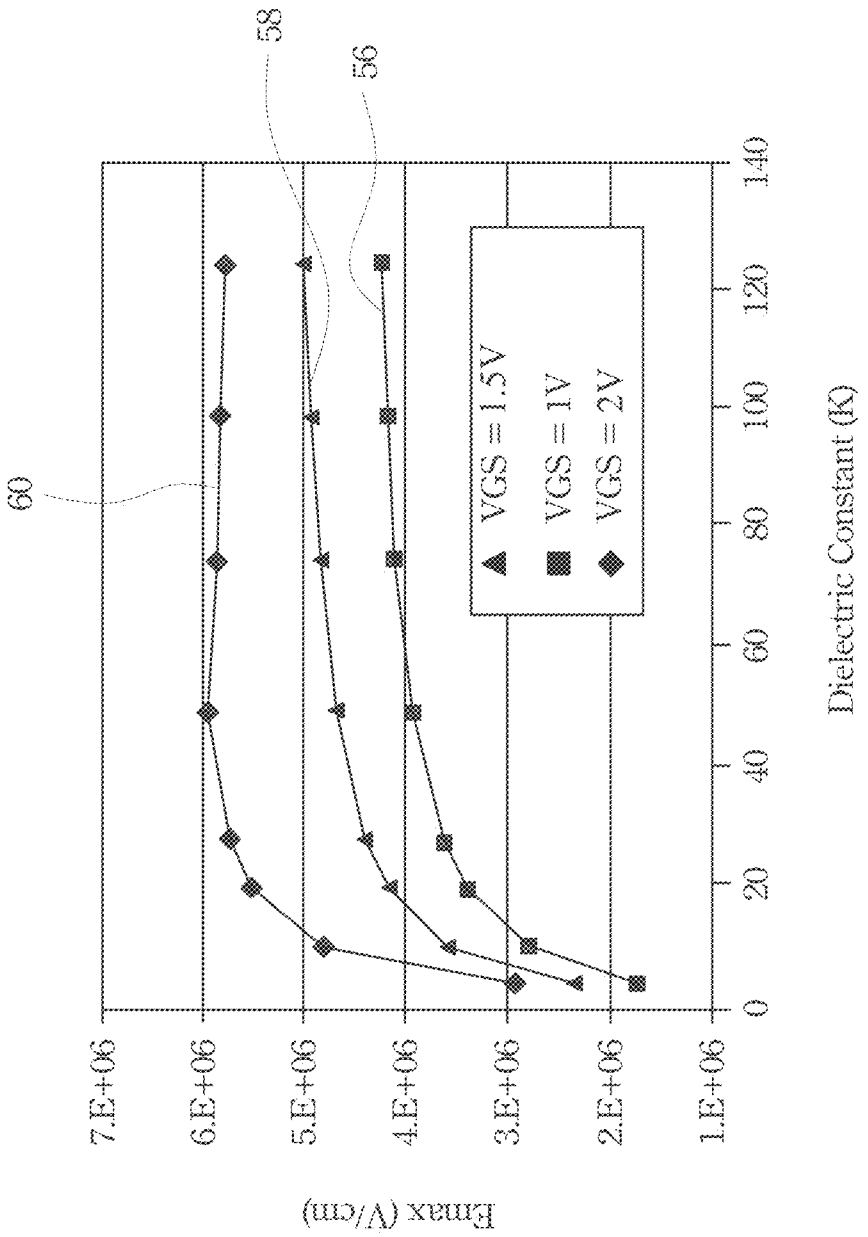

58
56
60
VGS = 1.5V
VGS = 1V
VGS = 2V
7.E+06
6.E+06
5.E+06
4.E+06
3.E+06
2.E+06
1.E+06
Emax (V/cm)
0
20
40
60
80
100
120
140
Dielectric Constant (K)

Fig. 11A

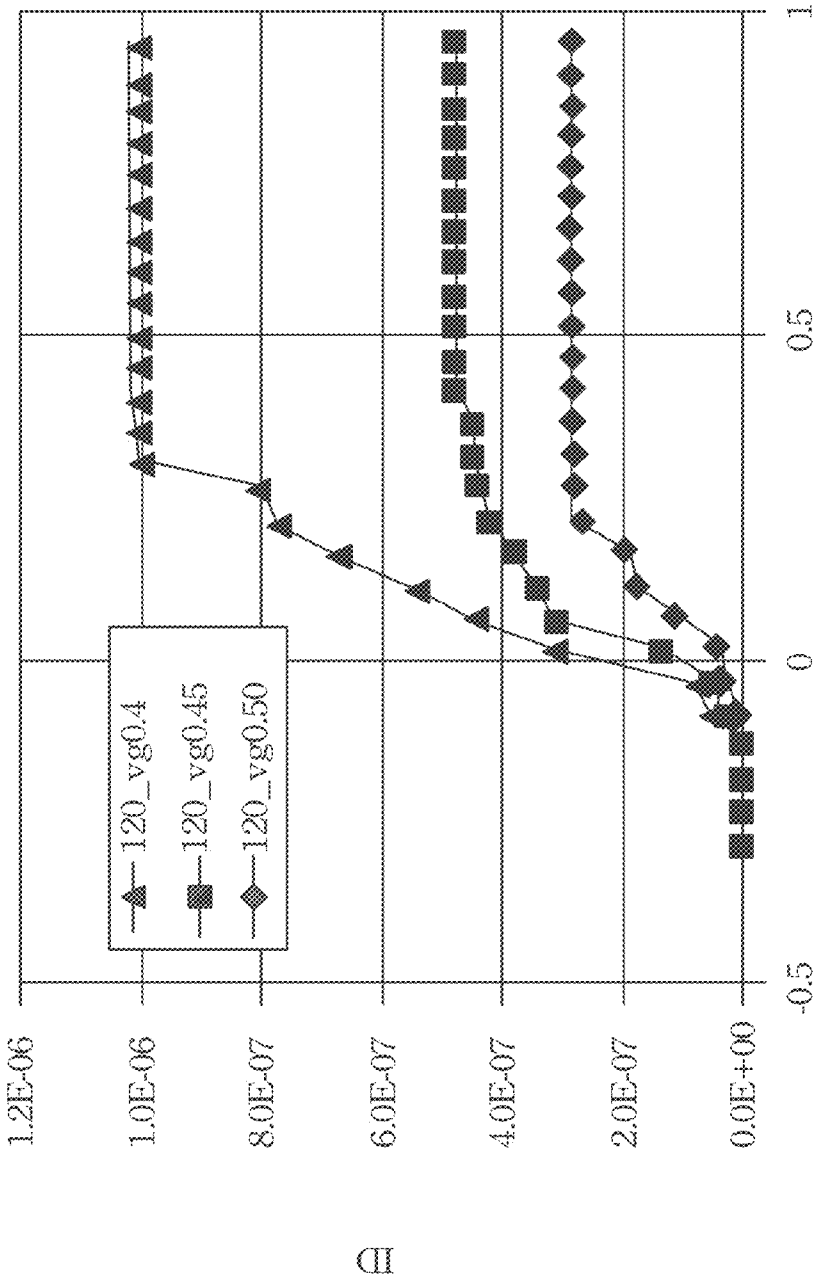

ID
1.2E-06
1.0E-06
8.0E-07
6.0E-07
4.0E-07
2.0E-07
0.0E+00
-0.5
0
0.5
1
VD
120_vg0.4
120_vg0.45
120_vg0.50

Fig. 11B

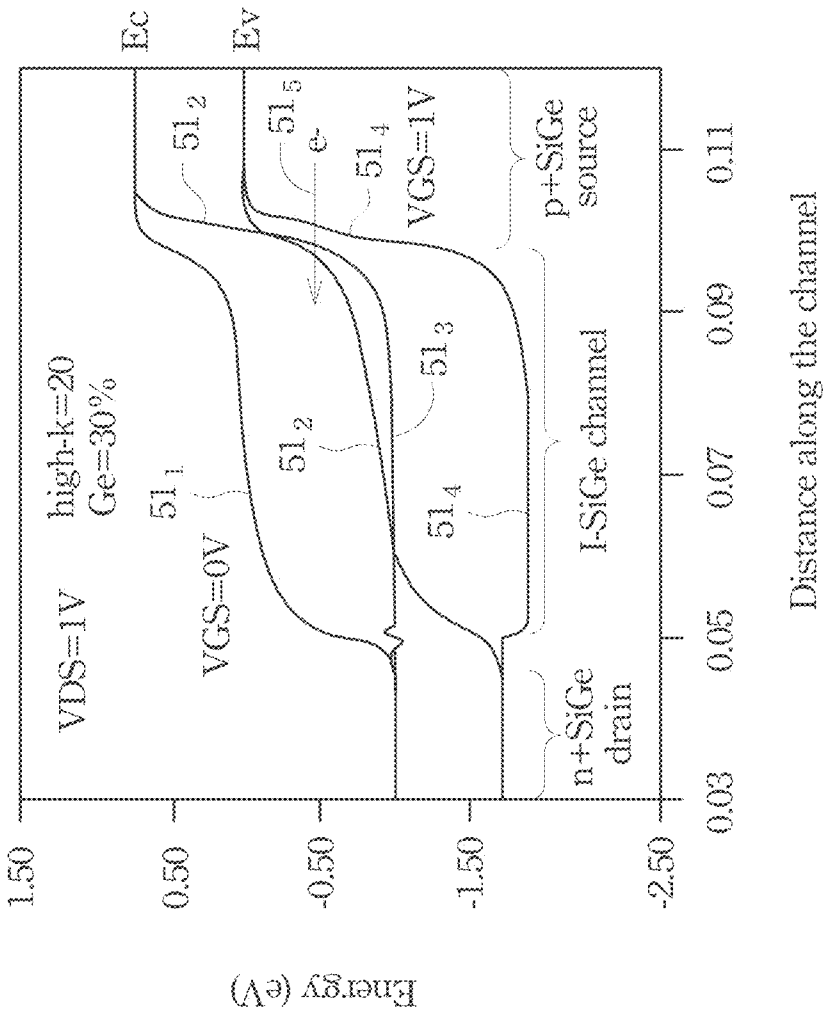

Ec
Ev
VDS=1V
high-k=20
Ge=30%
VGS=0V
VGS=1V
51 1
51 2
51 3
51 4
51 5
e
n+SiGe drain
I-SiGe channel
p+SiGe source
1.50
0.50
-0.50
-1.50
-2.50
0.03
0.05
0.07
0.09
0.11
Energy (eV)
Distance along the channel

Fig. 11C

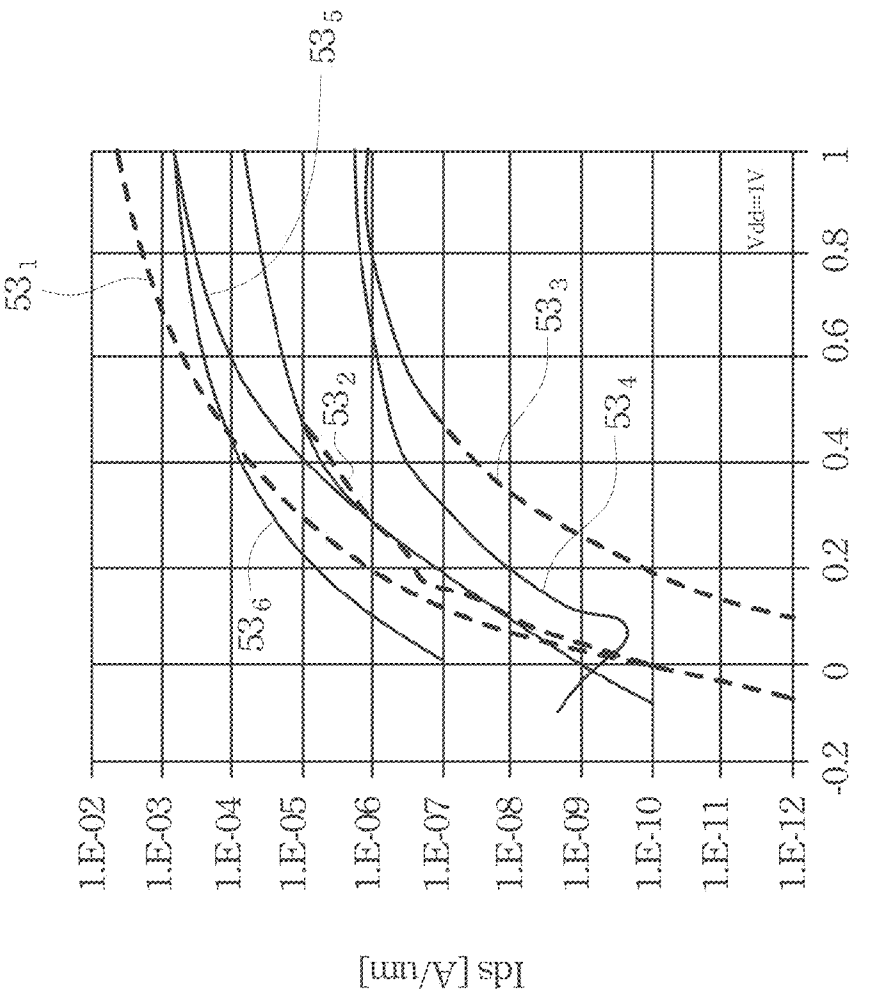

53_1
53_2
53_3
53_4
53_5
53_6
Vds=1V
1.E-02
1.E-03
1.E-04
1.E-05
1.E-06
1.E-07
1.E-08
1.E-09
1.E-10
1.E-11
1.E-12
Ids [A/um]
-0.2
0
0.2
0.4
0.6
0.8
1
Vg [V]

Fig. 11D

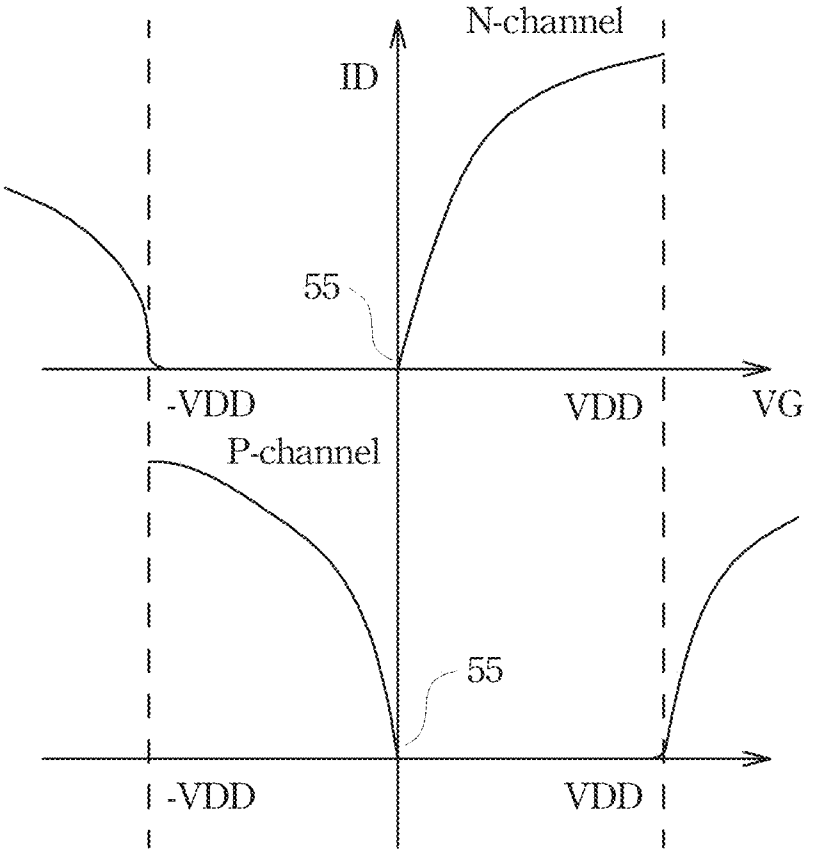
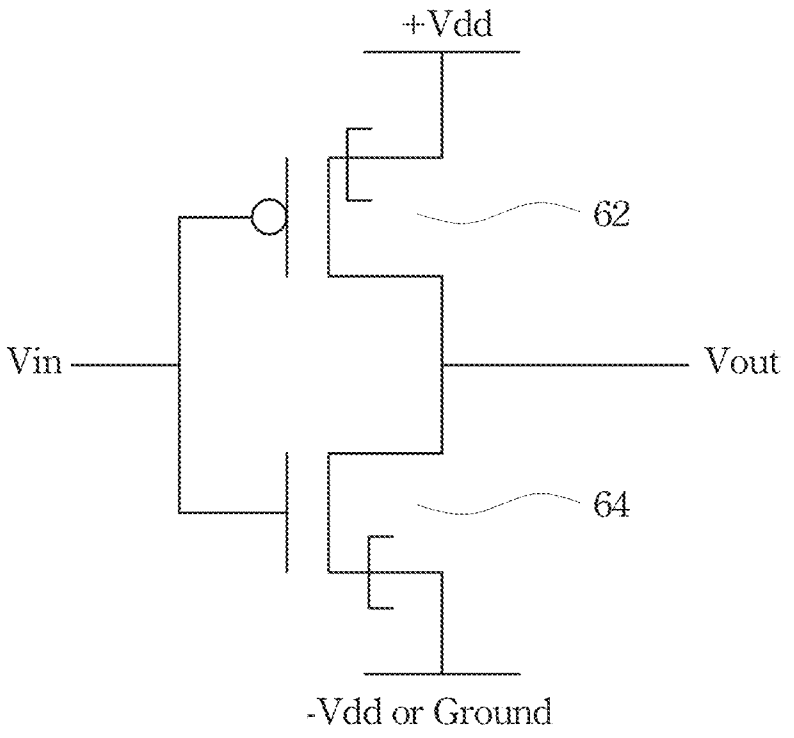


Fig. 12



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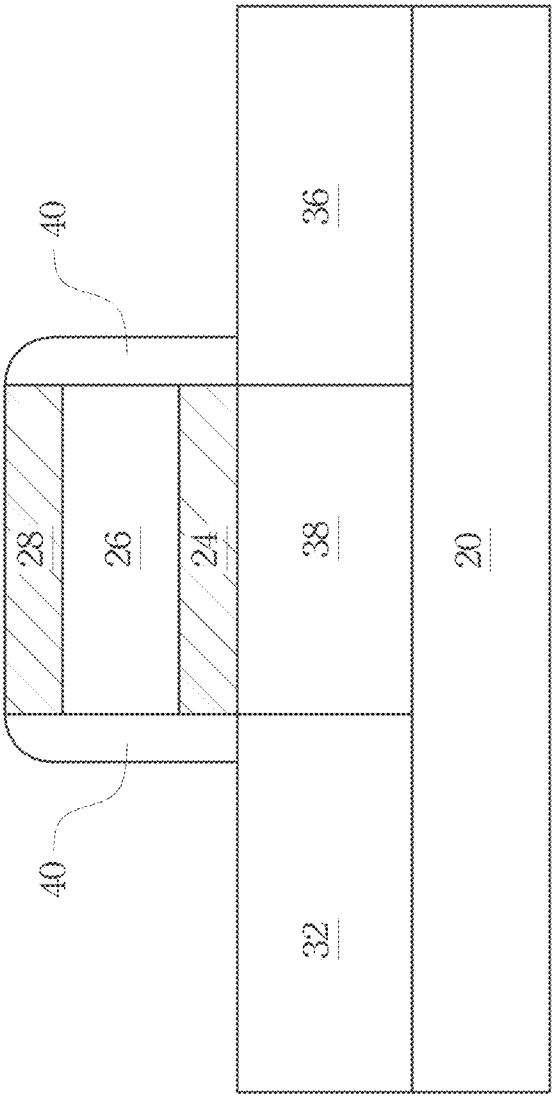


Fig. 14

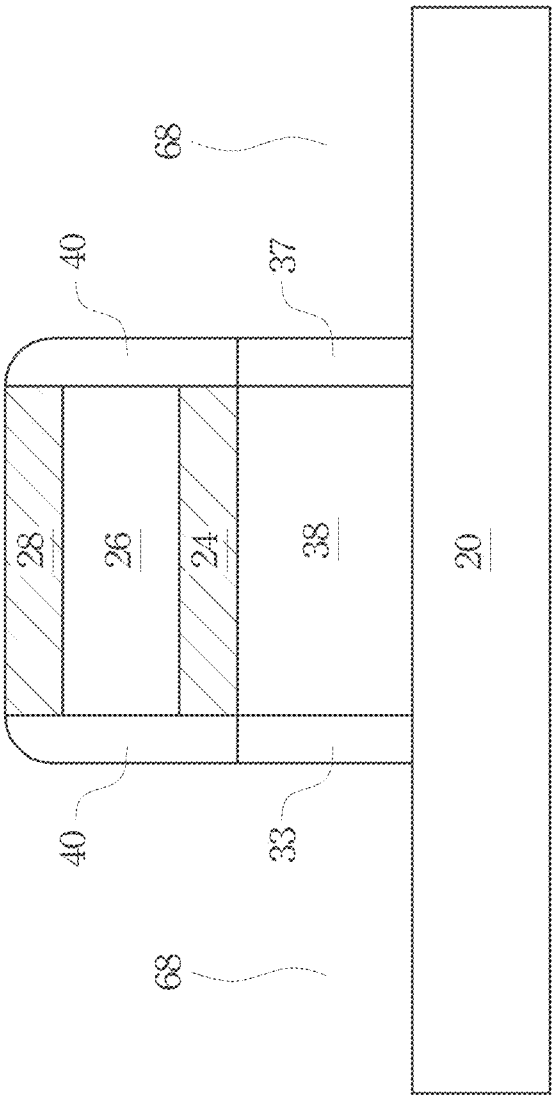
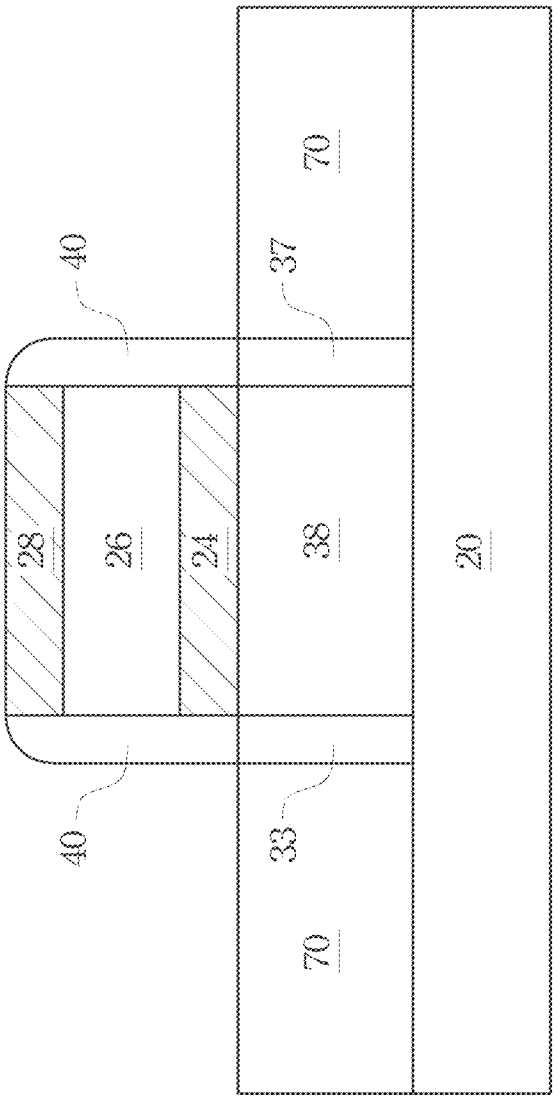


Fig. 15



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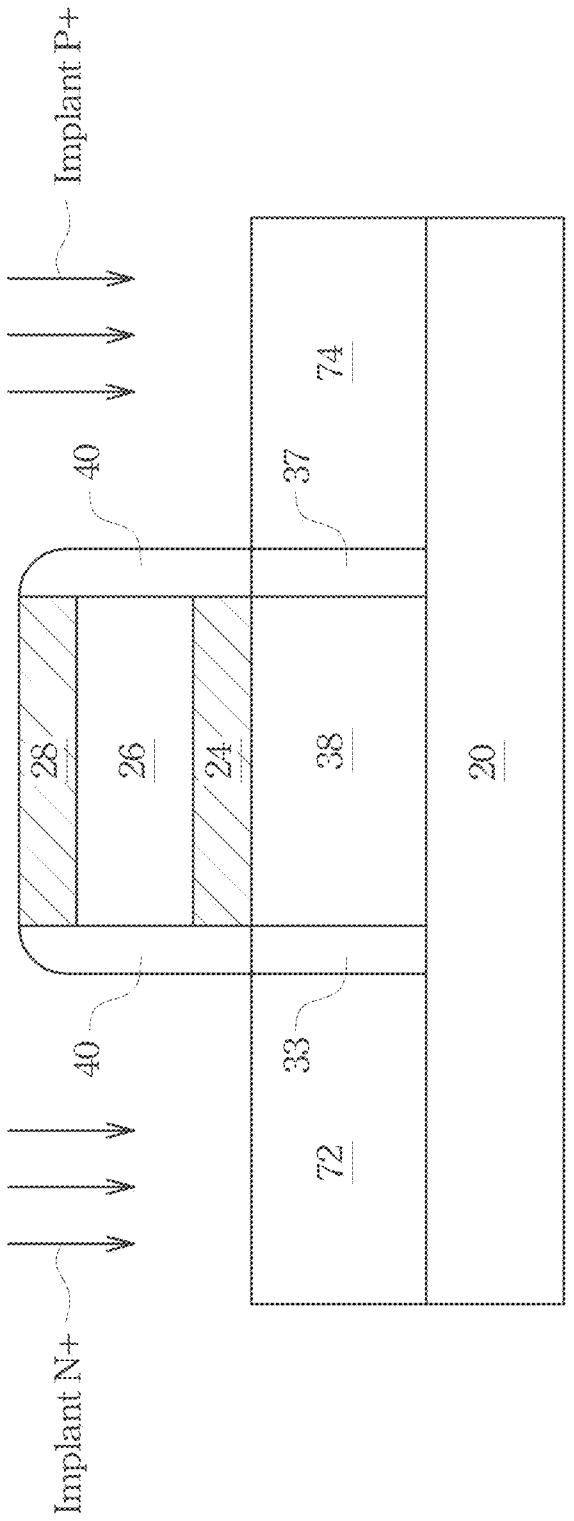
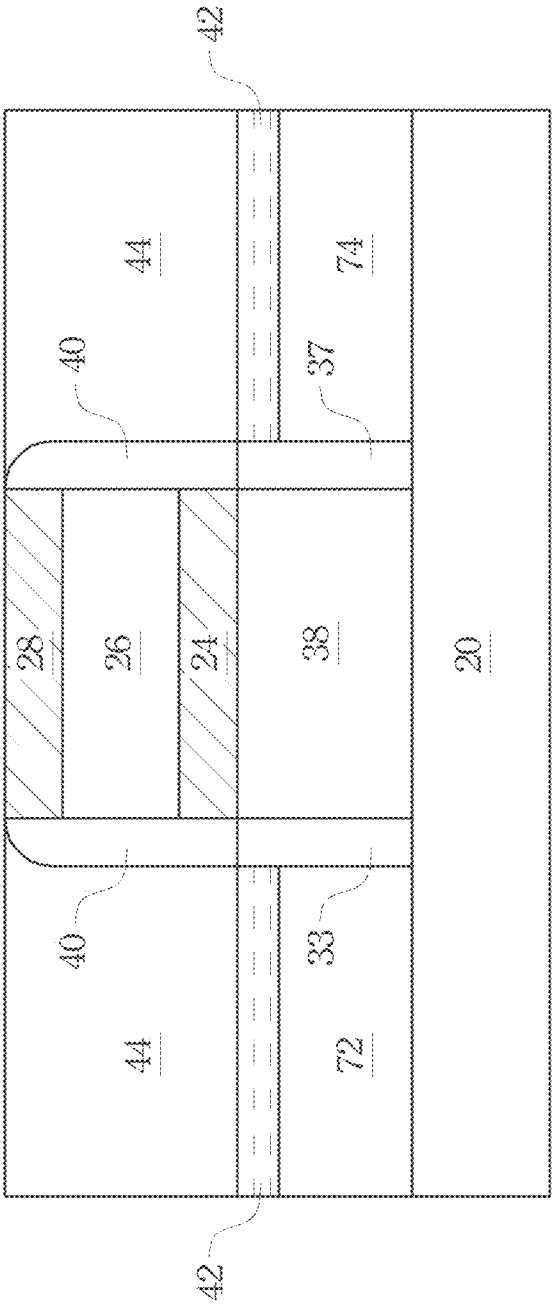


Fig. 17



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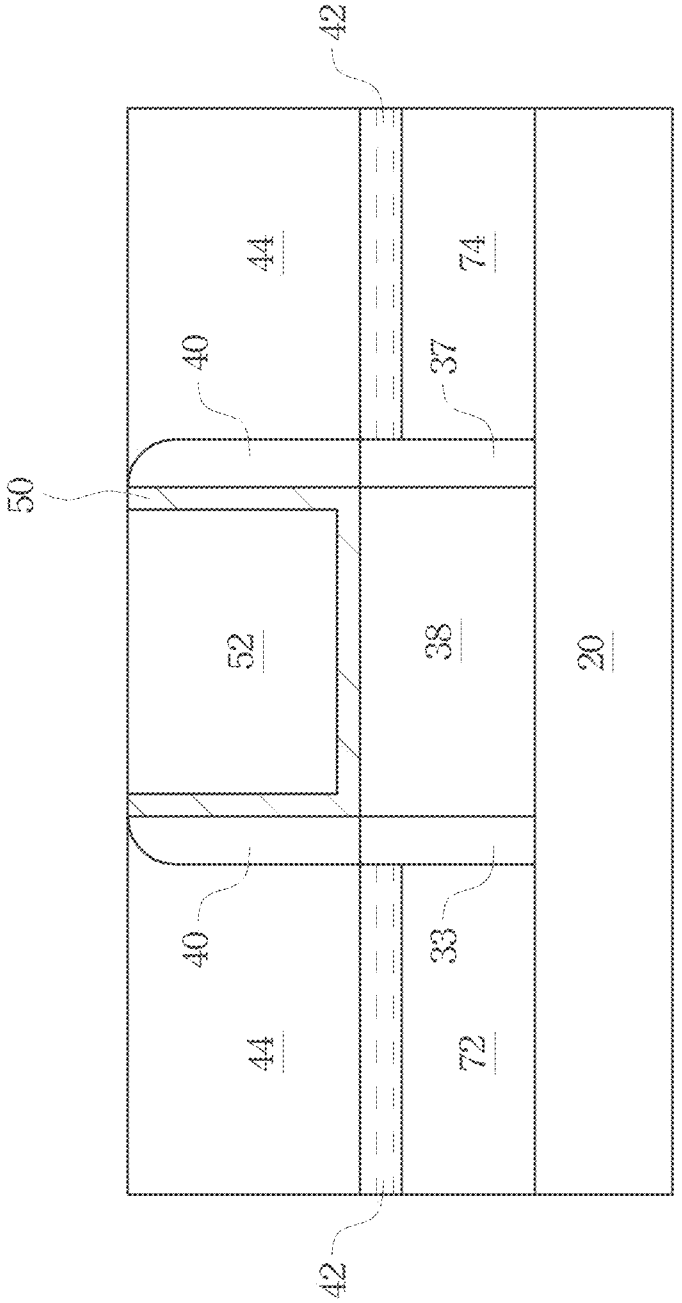


Fig. 19A

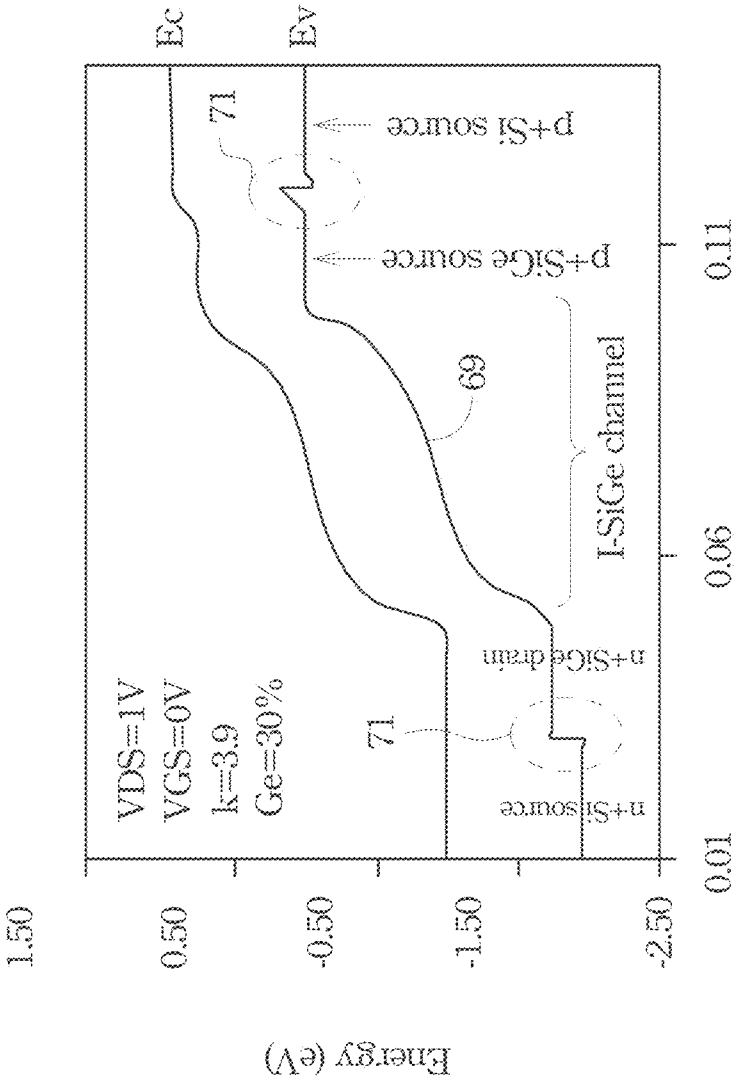

Ec
Ev
71
p+Si source
p+SiGe source
69
I-SiGe channel
n+SiGe drain
71
n+Si source
VDS=1V
VGS=0V
k=3.9
Ge=30%
1.50
0.50
-0.50
-1.50
-2.50
0.01
0.06
0.11
Energy (eV)
Distance along the channel

Fig. 19B

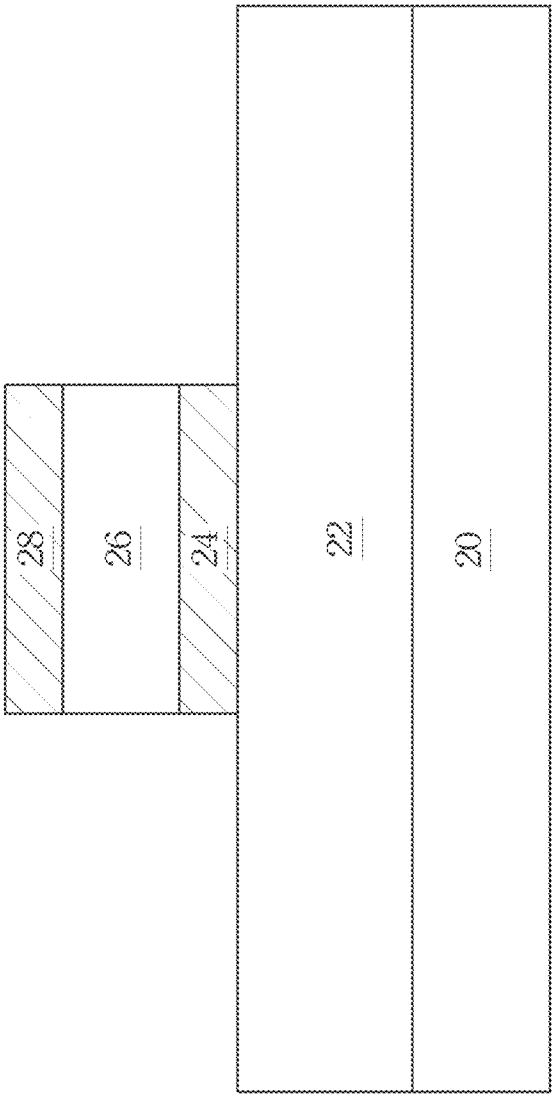
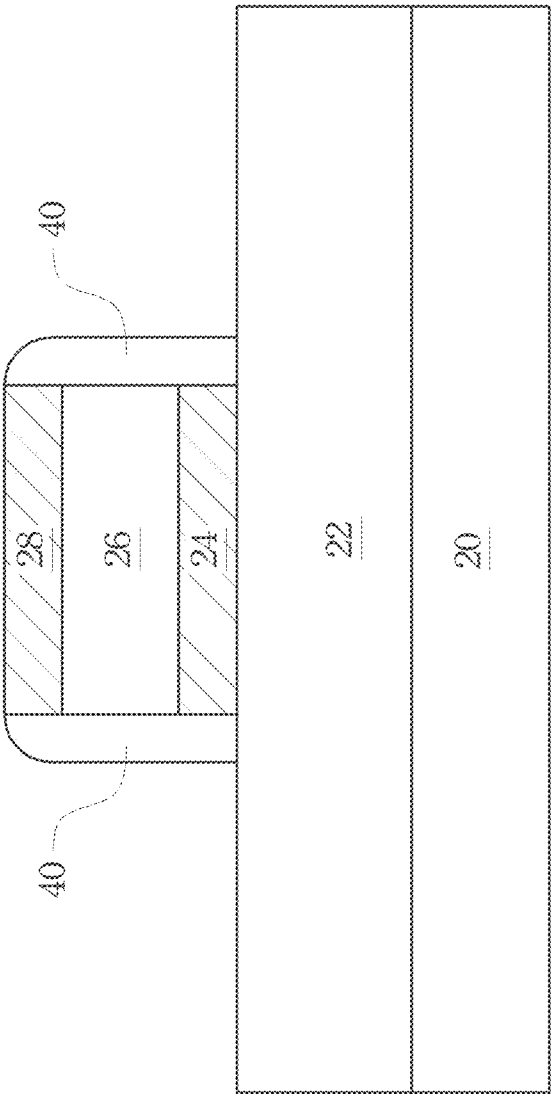


Fig. 20



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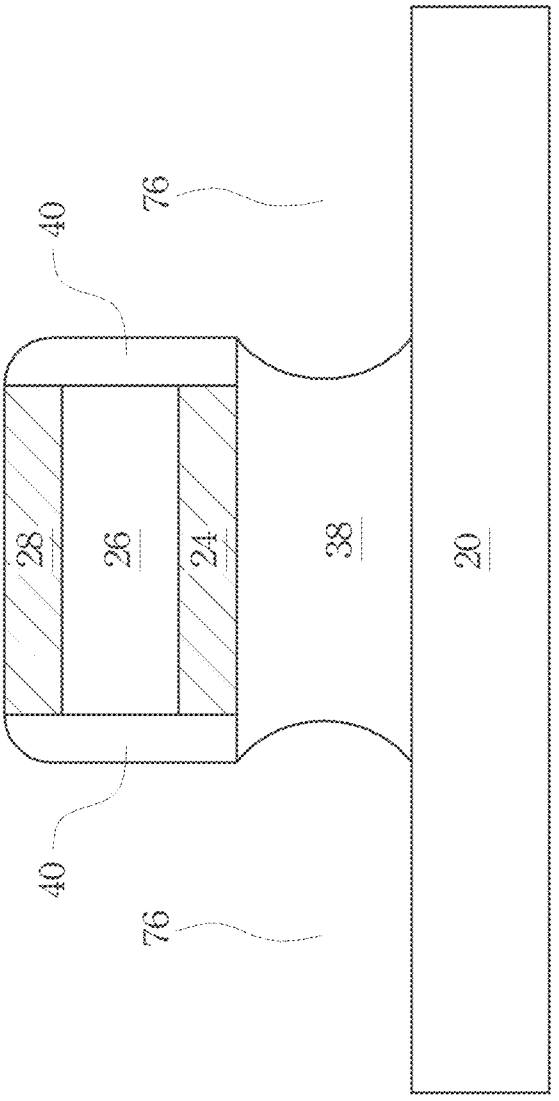
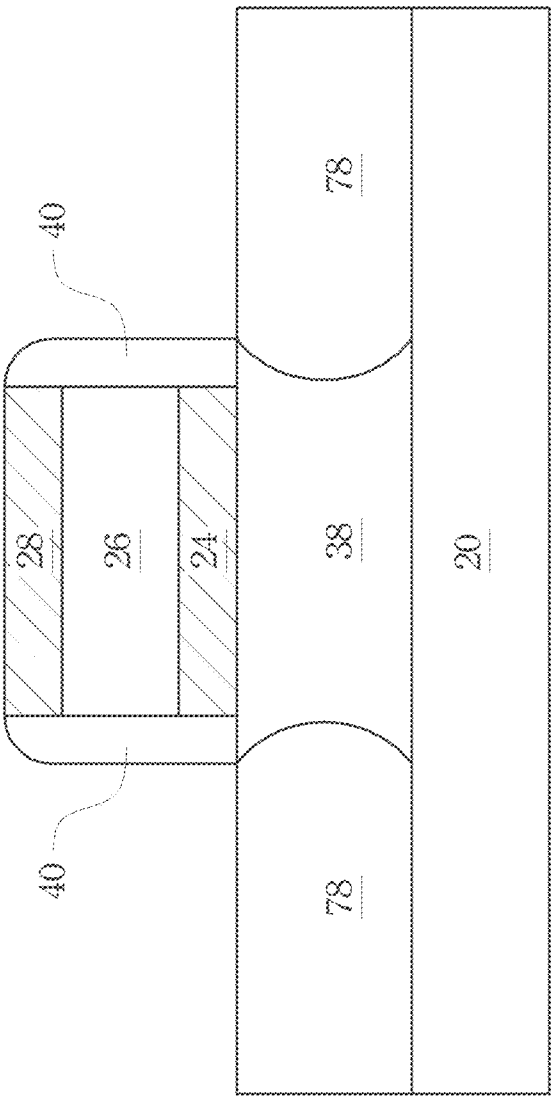


Fig. 22



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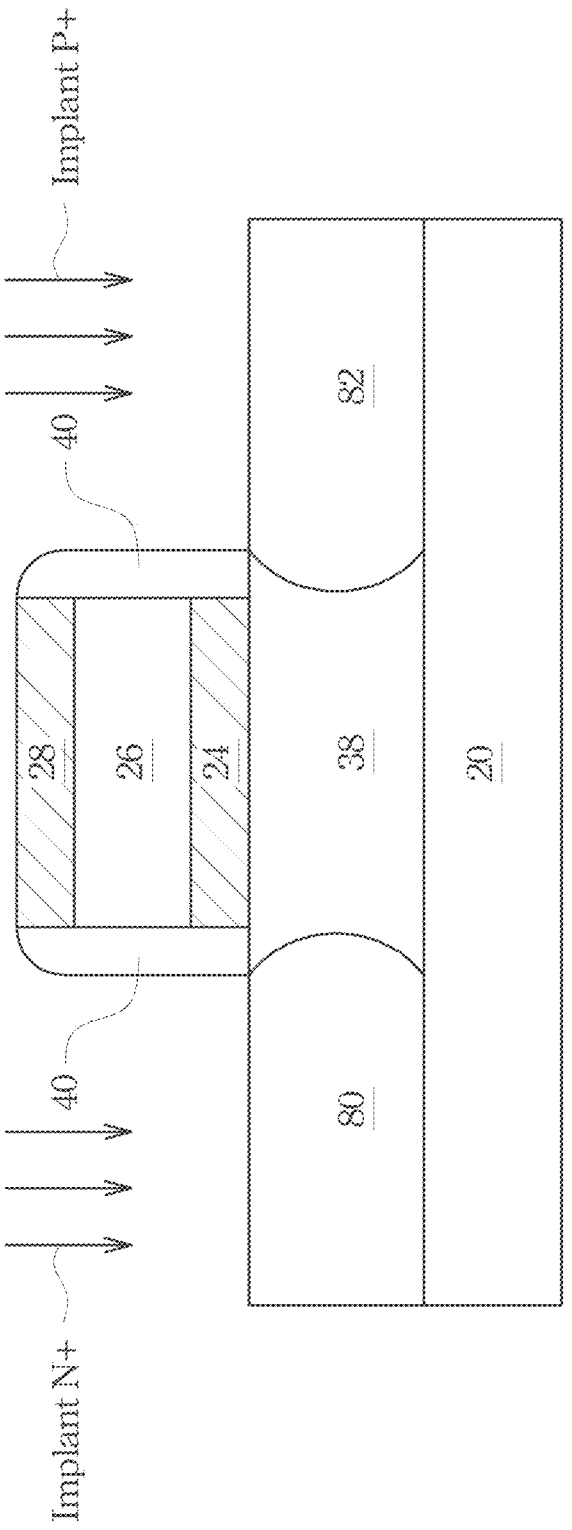


Fig. 24

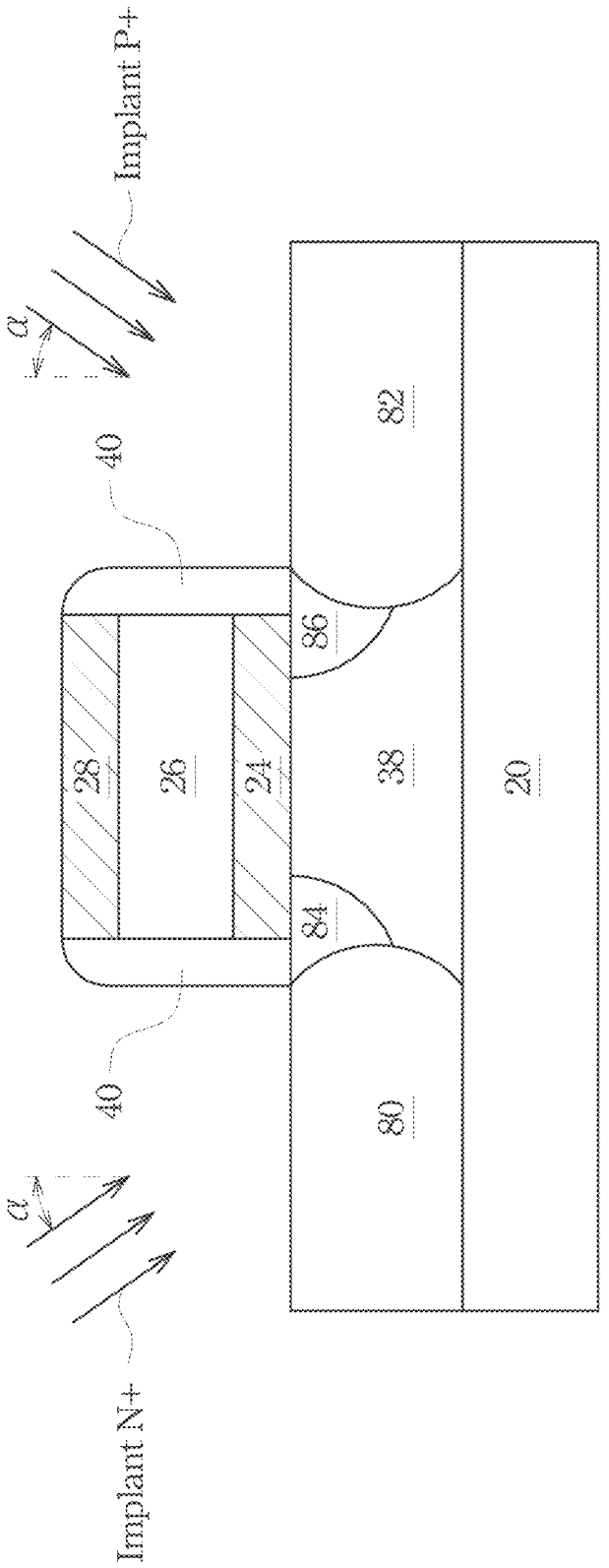
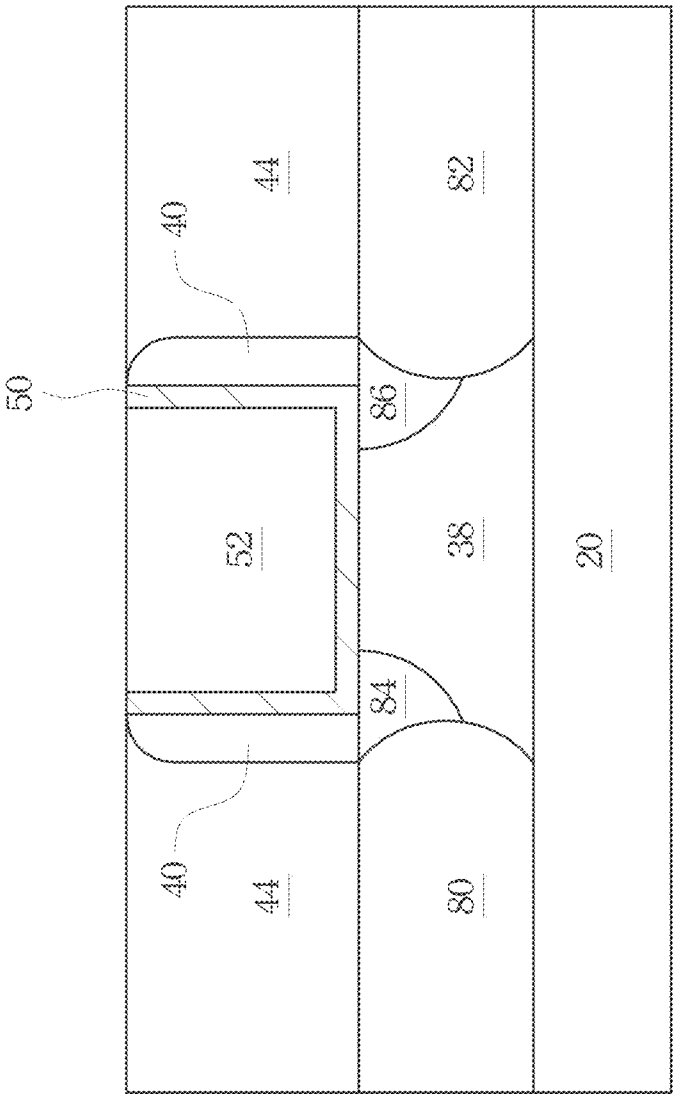


Fig. 25



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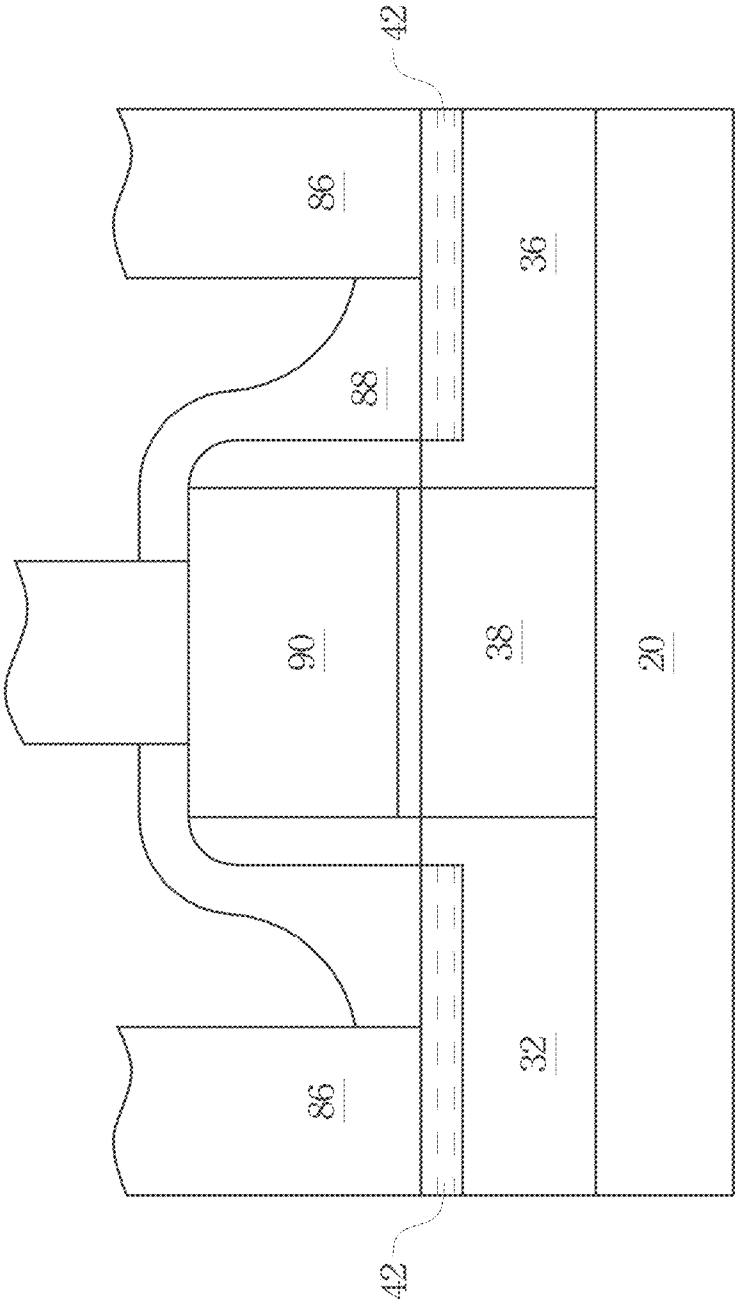

Fig. 27

TUNNEL FIELD-EFFECT TRANSISTOR WITH NARROW BAND-GAP CHANNEL AND STRONG GATE COUPLING

This application is a divisional of U.S. patent application Ser. No. 12/880,236, entitled "Tunnel Field-Effect Transistor with Narrow Band-Gap Channel and Strong Gate Coupling," filed on Sep. 13, 2010, which application is a divisional of U.S. patent application Ser. No. 11/828,211, entitled "Tunnel Field-Effect Transistor with Narrow Band-Gap Channel and Strong Gate Coupling," filed on Jul. 25, 2007, which applications are incorporated herein by reference.

TECHNICAL FIELD

This invention relates generally to semiconductor devices, and more specifically to tunnel field-effect transistors formed of gated p-i-n diodes.

BACKGROUND

The metal-oxide-semiconductor (MOS) is a dominating technology for integrated circuits at 90 nm technology and beyond. A MOS device can work in three regions, depending on gate voltage V_g and source-drain voltage V_{ds}, linear, saturation, and sub-threshold regions. The sub-threshold region is a region where V_g is smaller than the threshold voltage V_t. The sub-threshold swing represents the easiness of switching the transistor current off and thus is an important factor in determining the speed of a MOS device. The sub-threshold swing can be expressed as a function of m*kT/q, where m is a parameter related to capacitance. The sub-threshold swing of a typical MOS device has a limit of about 60 mV/decade (kT/q) at room temperature, which in turn sets a limit for further scaling of operation voltage VDD and threshold voltage V_t. This limitation is due to the drift-diffusion transport mechanism of carriers. For this reason, existing MOS devices typically cannot switch faster than 60 mV/decade at room temperatures. The 60 mV/decade sub-threshold swing limit also applies to FinFET or ultra thin-body MOSFET on silicon-on-insulator (SOI) devices. However, even with better gate control over the channel, an ultra thin body MOSFET on SOI or FinFET can only achieve close to, but not below, the limit of 60 mV/decade. With such a limit, faster switching at low operation voltages for future nanometer devices cannot be achieved.

To solve the above-discussed problem, tunnel field-effect transistors (FET) have been explored. FIG. **1** illustrates a FET device formed of a p-i-n diode called the I-MOS (impact-ionization MOS). The I-MOS has a heavily doped p-type (source) region **10** and a heavily doped n-type (drain) region **12** separated by an intrinsic channel region **14**. Gate **16** is formed over the intrinsic channel region **14** to control the intrinsic channel region **14**. The I-MOS has an offset region **18** between source region **10** and edge **11** of gate **16**. When the intrinsic channel region **14** is inverted by the gate bias applied to gate **16**, the drain-source voltage drops mainly across the offset region **18** and triggers an avalanche breakdown. The "avalanche multiplication" during breakdown serves as an internal positive feedback, so that the sub-threshold swing can be at a value less than 10 mV/decade at a very low drain voltage (for example, 0.2V). Such an I-MOS offers a promising approach for future MOS technology at 45 nm node and below due to the low power usage, high switching speed, and high on-current to off-current ratio.

The I-MOS shown in FIG. **1** suffers from some drawbacks, however. The output characteristics have large drain-to-source voltage dependence. Further, although it is capable of ultra-fast switching by avalanche mechanism, the critical width of the offset region **18** is sensitive to alignment errors between the gate and the source/drain. This leads to large variations of electrical fields in the offset region **18** during switching, which in turn leads to large variations of the sub-threshold swing. Furthermore, the avalanche mechanism of the I-MOS device is temperature sensitive, and temperature variations also lead to variations in sub-threshold swing.

FIG. **2** illustrates an asymmetric tunnel FET device formed of gated p-i-n diode, which includes a heavily doped drain region **102** and a heavily doped source region **104** separated by channel region **103**. Drain region **102** comprises silicon, while source region **104** comprises silicon germanium. The channel region **103** is formed of intrinsic silicon. Gate **108** controls channel region **103**. The tunnel FET device shown in FIG. **2** has a kT/q independent sub-threshold swing and a low off-state current. However, such a structure can only improve the on-currents of n-channel tunnel FET devices, while the on-currents of p-channel tunnel FET devices are not improved.

What is needed in the art, therefore, is a tunnel FET structure providing a high on current, a low off-current, and a reliable performance for both p-channel and n-channel tunnel FET devices.

SUMMARY OF THE INVENTION

In accordance with one aspect of the present invention, a semiconductor device includes a low energy band-gap layer comprising a semiconductor material; a gate dielectric on the low energy band-gap layer; a gate electrode over the gate dielectric; a first source/drain region adjacent the gate dielectric, wherein the first source/drain region is of a first conductivity type; and a second source/drain region adjacent the gate dielectric. The second source/drain region is of a second conductivity type opposite the first conductivity type. The low energy band-gap layer is located between the first and the second source/drain regions.

In accordance with another aspect of the present invention, a semiconductor device includes a semiconductor substrate; a low energy band-gap region over the semiconductor substrate; a gate dielectric on the low energy band-gap region; a gate electrode over the gate dielectric; a pair of spacers on opposite sidewalls of the gate electrode; and a first and a second source/drain region on opposing sides of the low energy band-gap region. The first and the second source/drain regions have a higher energy band-gap than the low energy band-gap region, and are of opposite conductivity types. The semiconductor device further includes a first self-aligned offset region between and adjoining the low energy band-gap region and the first source/drain region, wherein the first self-aligned offset region is of a same conductivity type as the first source/drain region; and a second self-aligned offset region between and adjoining the low energy band-gap region and the second source/drain region. The second self-aligned offset region is of a same conductivity type as the second source/drain region. The first and the second self-aligned offset regions include a same material as the low energy band-gap region.

In accordance with yet another aspect of the present invention, a semiconductor device includes a semiconductor substrate; a low energy band-gap region over the semiconductor substrate; a gate dielectric on the low energy band-gap region; a gate electrode over the gate dielectric; a pair of spacers on opposing sidewalls of the gate electrode; and a first and a second source/drain region on opposing sides of the low

energy band-gap region. The first and the second source/drain regions have a higher band-gap than the low energy band-gap region, and are of opposite conductivity types. The semiconductor device further includes a first source/drain extension region between and adjoining the low energy band-gap region and the first source/drain region, wherein the first source/drain extension region is of a same conductivity type as the first source/drain region; and a second source/drain extension region between and adjoining the low energy band-gap region and the second source/drain region. The second source/drain extension region is of a same conductivity type as the second source/drain region. The first and the second source/drain extension regions are at least moderately doped.

In accordance with yet another aspect of the present invention, a method for forming a semiconductor device includes providing a low energy band-gap layer; forming a gate dielectric on the low energy band-gap layer; forming a gate electrode over the gate dielectric; forming a first source/drain region adjacent the gate dielectric, wherein the first source/drain region is of a first conductive type; and forming a second source/drain region adjacent the gate dielectric and on an opposing side of the gate electrode than the first source/drain region, wherein the second source/drain region is of a second conductivity type opposite the first conductivity type.

In accordance with yet another aspect of the present invention, a method for forming a semiconductor device includes providing a semiconductor substrate; forming a low energy band-gap layer over the semiconductor substrate; forming a dummy gate stack over the low energy band-gap layer; implanting portions of the low energy band-gap layer unmasked by the dummy gate stack, wherein portions of the low energy band-gap layer on opposite sides of the dummy gate stack are at least moderately implanted with impurities having opposite conductivity types; forming gate spacers on sidewalls of the dummy gate stack after the step of implanting; using the dummy gate stack and the gate spacer as a mask, recessing the low energy band-gap layer to form recesses; filling the recesses with a semiconductor material having a higher band-gap than the low energy band-gap layer to form a first and a second semiconductor region; implanting the first and the second semiconductor regions with impurities having opposite conductivity types; removing the dummy gate stack; forming a gate dielectric layer and a gate electrode layer in a space left by the dummy gate stack; and performing a chemical mechanical polish, wherein remaining portions of the gate dielectric layer and the gate electrode layer form a gate dielectric and a gate electrode, respectively.

In accordance with yet another aspect of the present invention, a method for forming a semiconductor device includes providing a semiconductor substrate; forming a low energy band-gap layer over the semiconductor substrate; forming a dummy gate stack over the low energy band-gap layer; forming gate spacers on sidewalls of the dummy gate stack; using the dummy gate stack and the gate spacers as a mask, recessing the low energy band-gap layer to form recesses; filling the recesses with a semiconductor material having a higher band-gap than the low energy band-gap layer to form a first and a second semiconductor region; performing a first and a second implantation substantially vertical to implant the first and the second semiconductor regions with impurities having the first and the second conductivity types, respectively; tilt performing a third and a fourth implantation to form a first and a second source/drain extension region adjoining the first and the second semiconductor regions, respectively, wherein the first and the second source/drain extension regions are at least moderately doped and have same conductivity types as the first and the second semiconductor regions, respectively; removing the dummy gate stack; forming a gate dielectric layer and a gate electrode layer in a space left by the dummy gate stack; and performing a chemical mechanical polish, wherein remaining portions of the gate dielectric layer and the gate electrode layer form a gate dielectric and a gate electrode, respectively.

The advantageous features of the present invention include balanced performance of p-channel and n-channel FET devices, reduced leakage current, and improved sub-threshold swing and on-current.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. **1** illustrates an I-MOS device formed of gated p-i-n diode including an offset channel region;

FIG. **2** illustrates a tunnel field-effect transistor (FET), wherein the source region is formed of silicon germanium, the drain region is formed of silicon, and the channel region includes intrinsic silicon;

FIGS. **3** through **10** are cross-sectional views of intermediate stages in the manufacturing of a first embodiment of the present invention, wherein source and drain regions are formed by implantations;

FIG. **11**A illustrates maximum electrical fields at tunneling junctions as a function of dielectric constants of gate dielectrics;

FIG. **11**B illustrates an I-V curve of the first embodiment;

FIG. **11**C illustrates a simulated energy band diagram of the first embodiment;

FIG. **11**D compares the drive currents of the first embodiment of the present invention with various MOS devices having different structures and channel materials;

FIG. **12** illustrates expected I-V curves of asymmetric n-channel and p-channel tunnel

FET devices;

FIG. **13** illustrates an inverter formed of asymmetric tunnel FETs;

FIGS. **14** through **19**A are cross-sectional views of intermediate stages in the manufacturing of a second embodiment of the present invention, wherein offset regions are formed between a channel region and respective source/drain regions;

FIG. **19**B illustrates a simulated energy band diagram of the second embodiment;

FIGS. **20** through **26** are cross-sectional views of intermediate stages in the manufacturing of a third embodiment of the present invention, wherein at least moderately doped source/drain extension regions are formed between the channel region and source/drain regions; and

FIG. **27** illustrates an embodiment of the present invention having a gate-first structure, wherein a stressed contact etch stop layer is formed.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

Novel tunnel field-effect transistors (FET) formed of gated p-i-n diodes and the methods of forming the same are provided. The intermediate stages of manufacturing preferred embodiments of the present invention are illustrated. The variations of the preferred embodiments are then discussed. Throughout the various views and illustrative embodiments of the present invention, like reference numbers are used to designate like elements.

A first embodiment of the present invention is provided in FIGS. **3** through **10**. Referring to FIG. **3**, substrate **20** is provided. In an embodiment, substrate **20** is a bulk substrate comprising a single crystalline semiconductor material, such as silicon, or a compound semiconductor material. In other embodiments, substrate **20** may include more than one semiconductor layer. For example, substrate **20** may have a silicon-on-insulator or silicon-on-carbide structure, including silicon layer $\mathbf{20}_3$ on insulator layer $\mathbf{20}_2$. Insulator layer $\mathbf{20}_2$ may further be located on semiconductor layer $\mathbf{20}_1$. In yet other embodiments, substrate **20** includes an insulator.

Low (energy) band-gap layer **22** is formed over substrate **20**. Throughout the description, the term "low band-gap" refers to band-gaps lower than the band-gap of silicon (1.12 eV). In the preferred embodiment, low band-gap layer **22** is formed of silicon germanium (SiGe). In other embodiments, other semiconductor materials having low band-gaps, such as Ge, GaAs, InGaAs, InAs, InSb, and combinations thereof, can be used. Due to the possible mismatch in the lattice constants of low band-gap layer **22** and the underlying substrate **20**, low band-gap layer **22** may be strained. Alternatively, low band-gap layer **22** forms a bulk substrate, with no underlying substrate **20**.

In the embodiment wherein the top layer of substrate **20** includes a crystalline semiconductor material, an epitaxial growth may be performed to grow low band-gap layer **22** on substrate **20**. Further, in the case low band-gap layer comprises SiGe, the germanium atomic percentage is preferably less than about 80 percent. It is realized, however, that the optimum germanium percentage is related to the desirable tunnel FET characteristics. For example, if high switching speed is preferred, the germanium percentage is preferably high. However, this may cause the leakage current of the resulting tunnel FET to increase. Conversely, if low power consumption is more preferred over high switching speed, low band-gap layer **22** preferably has a lower germanium percentage.

Low band-gap layer **22** is preferably intrinsic. In an embodiment, low band-gap layer **22** is un-doped. Alternatively, low band-gap layer **22** is lightly doped to a concentration of less than about $1E15/cm^3$.

FIG. **4** illustrates the formation of a dummy gate stack, which includes dummy gate dielectric **24**, dummy gate electrode **26**, and dummy gate mask **28**. The dummy gate stack may be formed simultaneously with the formation of gate stacks of other metal-oxide-semiconductor (MOS) devices on the same chip. As is known in the art, the formation of the dummy gate stack includes forming a gate dielectric layer, forming a gate electrode layer on the gate dielectric layer, forming a gate mask layer on the gate electrode, and patterning the stacked layers.

Photo resist **30** is then applied and patterned, followed by an implantation to dope an n-type impurity, which may include phosphorous, arsenic, and combinations thereof. The implantation may be vertically performed, or tilted toward the dummy gate stack. As a result, drain region **32** is formed. Drain region **32** may be substantially aligned to the edge of the dummy gate stack, or extend under the dummy gate stack if the implantation is tilted. Photo resist **30** is then removed.

Referring to FIG. **5**, photo resist **34** is applied and patterned, covering drain region **32** and a portion of the dummy gate stack. An implantation is then performed to dope a p-type impurity, such as boron, indium, and combinations thereof. Again, the implantation may be vertically performed, or tilted toward the dummy gate stack. As a result, source region **36** is formed. Similarly, source region **36** may be substantially aligned to the edge of the dummy gate stack, or extend under the dummy gate stack if the implantation is tilted. Intrinsic channel region **38** will be formed in an un-implanted region between drain region **32** and source region **36**.

In an embodiment, both drain region **32** and source region **36** are heavily doped, and thus drain region **32** is referred to as an n+ region, while source region **36** is referred to as a p+ region. In the described embodiments, "heavily doped" means an impurity concentration of above about $10^{20}/cm^3$. One skilled in the art will recognize, however, that heavily doped is a term of art that depends upon the specific device type, technology generation, minimum feature size, and the like. It is intended, therefore, that the term be interpreted in light of the technology being evaluated and not be limited to the described embodiments. The resulting tunnel FET device will be an ambipolar FET device, which means that the tunnel FET device can be either an n-channel device or a p-channel device, depending on whether the gate voltage is positive or negative, respectively.

In alternative embodiments, one of the drain region **32** and source region **36** is heavily doped, while the other is moderately doped (referred to as an n region or a p region, depending on the impurity type). The term "moderately doped" may indicate an impurity concentration of lower than "heavily doped," for example, between about $10^{18}/cm^3$ and about $10^{20}/cm^3$. If drain region **32** is an n region, and source region **36** is a p+ region, the resulting tunnel FET will be an n-channel FET, and will be turned on by a positive gate voltage. Conversely, if drain region **32** is an n+ region, and source region **36** is a p region, the resulting tunnel FET will be a p-channel FET, and will be turned on by a negative gate voltage.

FIG. **6** illustrates the formation of gate spacers **40** and source/drain silicide regions **42**. As is known in the art, the formation of gate spacers **40** may include forming a gate dielectric layer, and etching the gate dielectric layer to remove horizontal portions. Source/drain silicide regions **42** may be formed by blanket forming a metal layer, and performing an annealing to cause a reaction between the metal layer and the underlying silicon. The un-reacted metal is then removed.

Referring to FIG. **7**, a first inter-layer dielectric (ILD) **44** is formed, followed by a chemical mechanical polish (CMP) to level the top surface of ILD **44** to the top surface of dummy gate mask **28**. ILD **44** may include commonly used ILD materials, such as boronphosphosilicate glass (BPSG). Other elements such as carbon, nitrogen, oxygen, and combinations thereof, may also be included.

In FIG. **8**, photo resist **46** is applied and patterned, forming opening **48**, through which dummy gate mask **28** is exposed. Next, as is shown in FIG. **9**, the dummy gate stack is removed, preferably by etching, exposing the intrinsic channel region **38**.

Referring to FIG. **10**, gate dielectric **50** and gate electrode **52** are formed. The formation process may include forming a gate dielectric layer, forming a gate electrode layer, and performing a CMP to remove excess materials. In the preferred embodiment, gate dielectric **50** includes a high-k dielectric with a preferred k value between about 7 and about 60. The preferred materials of gate dielectric **50** may include high-k metal oxides such as HfO_2, silicon nitride, silicon oxide,

silicon oxynitride, and combinations thereof. Gate dielectric **50** may also have a composite structure including more than one layer. Gate electrode **52** may include doped polysilicon, metals, metal silicides, multi-layers thereof, and combinations thereof.

The process steps discussed in the preceding paragraphs illustrate the formation of tunnel FET device **54**. An advantageous feature of using the high-k gate dielectric materials is the increase in the drive current of tunnel FET device **54**. FIG. **11**A illustrates a simulation result, which reveals the relationship between the maximum electrical field E_{max} in the tunneling junction and the k value of gate dielectric **50**. Lines **56**, **58**, and **60** are the results of gate-to-source voltage being 1V, 1.5V, and 2V, respectively. It is noted that when the k value increases, the maximum electrical field E_{max} increases accordingly. However, when the k value reaches around **60**, the maximum electrical field E_{max} starts to saturate, and may even decrease if the k value further increases. It is expected that with a constant physical thickness of the high-k gate dielectric **50**, the current gain is substantially exponential. However, the capacitance only increases linearly. Therefore, the gain in the drive current of the tunnel FET device more than offsets the degradation in the capacitance (and hence RC delay). Accordingly, the high-k dielectric materials are preferred.

Simulation results also revealed that the drive currents of tunnel FETs are related to the germanium percentage in the intrinsic channel region **38**. When the germanium percentage increases, the drive current increases accordingly.

FIG. **11**B illustrates a simulated I-V characteristic of the embodiment shown in FIG. **10**. It is found that the saturation drive currents ID are independent from the drain voltages VD, and is only affected by the gate voltages Vg.

FIG. **11**C illustrates a simulated energy band diagram of a symmetrical channel FET device as shown in FIG. **10**, wherein the intrinsic channel is formed of SiGe. Lines $\mathbf{51}_1$ and $\mathbf{51}_2$ are a conduction band and a valence band, respectively, with no gate voltage applied, while lines $\mathbf{51}_3$ and $\mathbf{51}_4$ are a conduction band and a valence band, respectively with 1 volt gate-to-source voltage applied. It is noted that strong inversion occurs after the gate voltage is applied. The strong inversion causes the narrowing between bands $\mathbf{51}_3$ and $\mathbf{51}_4$, and hence electrons can easily tunnel through the energy barrier between valence band $\mathbf{51}_4$ and conduction band $\mathbf{51}_3$ (refer to arrow $\mathbf{51}_5$), which barrier is narrowed due to the strong inversion.

FIG. **11**D illustrates the drive currents of various devices as a function of gate voltages. Dash line $\mathbf{53}_1$ is the simulation result of a SiGe intrinsic tunnel FET device (with 40 percent germanium) having a metal gate and a high-k gate dielectric (k=20). The remaining lines $\mathbf{53}_2$ through $\mathbf{53}_6$ are results taken from various publications and simulation results. Lines $\mathbf{53}_2$, $\mathbf{53}_3$, and $\mathbf{53}_4$ and are results of tunnel FET devices with silicon channels, while lines $\mathbf{53}_5$ and $\mathbf{53}_6$ are results of conventional MOS devices. FIG. **11**D has shown that at a gate voltage of 1 volt, the embodiment of the present invention (line $\mathbf{53}_1$), has a higher drive current than others.

FIG. **12** illustrates expected I-V curves of asymmetric p-channel and n-channel tunnel FET devices. Preferably, for n-channel tunnel FET devices, there are no drive currents when negative gate voltages are applied, and drive currents are generated when positive gate voltages are applied. The drive currents increase with the increase in the gate voltages. On the other hand, for p-channel tunnel FET devices, there are no drive currents when positive gate voltages are applied. With negative gate voltages, drive currents are generated, wherein the drive currents increase with the increase in the magnitude of the negative gate voltage. The reverse breakdown voltages of both p-channel and n-channel devices preferably have magnitudes substantially equal to, or even greater than, VDD. By adjusting the work function and the doping concentrations in source and drain regions, the starting points **55** from which the drive currents begin to flow may be adjusted.

Table 1 shows the simulated electrical performance of various tunnel FETs having different channel materials and different gate dielectrics.

TABLE 1

When Vdd = 1 V		Tunnel FET		MOS
Substrate (i-Channel)	Si	Si	SiGe	Si
Gox	SiO_2	K = 10	K = 20	SiO_2
EOT (Å)	20	7.8	3.9	20
Ion (A/μm)	~1e−6	~1e−4	~3e−3	~1e−3
Ioff (A/μm)	<1e−14	~1e−10	~1e−10	~1e−9
S (mV/dec 300K)	<60	<60	<60	>60
DIBL (mV/V)	<20	<20	<20	>150

Table 1 has proven that the performances of tunnel FET devices having intrinsic SiGe channels are overall at least comparable, and likely to be better than conventional MOS devices. Tunnel FET devices with intrinsic SiGe channels have greater drive currents than tunnel FET devices with intrinsic Si channels, although leakage currents of tunnel FET devices with intrinsic SiGe channels are likely to be greater than that of the tunnel FET devices with intrinsic Si channels.

It is appreciated that the work function of gate electrode **52** also affects the device performance, such as the I-V curve of tunnel FET device **54**. To achieve the optimum I-V curve, the doping concentrations of drain region **32**, source region **36**, intrinsic channel region **38**, and the work function of gate electrode **52**, need to be tuned.

As discussed in the preceding paragraphs, an n-channel tunnel FET device and a p-channel tunnel FET device can be formed by heavily doping either one of the drain region **32** or source region **36**, respectively, and moderately doping the other source/drain region. FIG. **13** illustrates an inverter formed using the asymmetrically doped tunnel FETs. The inverter includes p-channel tunnel FET device **62** and n-channel tunnel FET device **64**. The bracket signs indicate the heavily doped sides of the respective tunnel FET devices. The inverter shown in FIG. **13** works essentially the same as the inverters formed of conventional MOS devices. When a high input voltage Vin is applied, the p-channel tunnel FET device **62** is turned off, while the n-channel tunnel FET device **64** is turned on. Conversely, when a low input voltage Vin is applied, the p-channel tunnel FET device **62** is turned on, while the n-channel tunnel FET device **64** is turned off. The relationships between input voltage Vin and the states of n-channel tunnel and p-channel tunnel FET devices are illustrated in Table 2.

TABLE 2

Vin	Vout	N-Channel FET	P-Channel FET
High	Low	on	off
Low	High	off	on

FIGS. **14** through **19** illustrate cross-sectional views in the manufacturing of a second embodiment. The initial steps of this embodiment may be essentially the same as shown in

FIGS. **3** through **5**, and hence forming drain region **32**, source region **36**, and channel region **38**. Next, as shown in FIG. **14**, gate spacers **40** are formed using essentially the same method as discussed in the first embodiment. In FIG. **15**, the exposed SiGe regions **32** and **36** are recessed, forming recesses **68**, while the portions of SiGe regions **32** and **36** protected by gate spacers **40** are left, forming self-aligned offset regions **33** and **37**, respectively. The recessing step may be performed by anisotropically or isotropically etching the exposed SiGe regions **32** and **36** using plasma. Alternatively, the recessing step may include implanting amorphizing species, such as silicon, germanium, argon, and the like, into the exposed portions of the low energy band-gap layer to form amorphized regions, and selectively etching the amorphized regions. SiGe regions **32** and **36** may be recessed until the underlying substrate **20** is exposed. Alternatively, only a top portion of the SiGe regions **32** and **36** are recessed.

In FIG. **16**, silicon is epitaxially grown in recesses **68**, forming silicon regions **70**. Preferably, selective epitaxial growth (SEG) is performed using a chemical vapor deposition tool, wherein the precursors include silicon-containing gases such as SiH_4 (silane).

FIG. **17** illustrates the implantation of silicon regions **70**. The silicon region **70** adjoining offset region **33** is heavily doped with an n-type impurity, forming n+ region **72**, while the silicon region **70** adjoining offset region **37** is heavily doped with a p-type impurity, forming p+ region **74**. As one skilled in the art will perceive, the formation of the n+ region **72** and the p+ region **74** involves the formation of photo resists as masks.

FIG. **18** illustrates the formation of source/drain silicide regions **42** and ILD **44**, which may be formed using essentially the same methods and materials as in the first embodiment. Next, dummy gate mask **28**, dummy gate electrode **26**, and dummy gate dielectric **24** are removed, and gate dielectric **50** and gate electrode **52** are formed. The resulting structure is shown in FIG. **19**A. Again, the materials and the formation methods of gate dielectric **50** and gate electrode **52** may be essentially the same as in the first embodiment.

FIG. **19**B illustrates a simulated energy band diagram of tunnel FET devices similar to what is shown in FIG. **19**A, except the simulated tunnel FET devices have gate-first structures. It is noted that the valence band **69** has heterogeneous structures **71**. It is believed that such heterogeneous structures act as barriers for the leakage currents. As a result, the leakage currents of the structure shown in FIG. **19**A are significantly reduced.

Similarly, instead of doping both the source side and drain side (each including an offset region **33** or **37** and an adjoining doped region **72** or **74**) heavily, either one of the source/drain sides may be heavily doped, while the other side may be moderately doped, forming asymmetric tunnel FETs.

An advantageous feature of this embodiment is that by replacing portions of the source/drain regions with silicon, the self-aligned offset SiGe regions adjoin silicon regions, hence forming a hetero-structure, and the off-state leakage current is reduced. Simulation results have revealed that by using this structure, the leakage current can be reduced by up to two orders. A possible reason may be that the butted silicon regions result in a higher band barrier to retard the leakage currents.

FIGS. **20** through **26** illustrate a third embodiment of the present invention. Referring to FIG. **20**, low band-gap layer **22** is formed on substrate **20**. A dummy gate stack, including dummy gate dielectric **24**, dummy gate electrode **26**, and dummy mask **28**, is then formed. Next, gate spacers **40** are formed, as is shown in FIG. **21**. FIG. **22** illustrates the recessing of low band-gap layer **22**, wherein the recessing is preferably isotropic, so that the resulting recesses **76** may extend under gate spacers **40**. Alternatively, the recessing is anisotropic. Recesses **76** are then filled with epitaxially grown silicon, forming silicon regions **78**, as is shown in FIG. **23**.

Referring to FIG. **24**, n+ drain region **80** and p+ region source **82** are formed. To form n+ drain region **80**, a first photo resist (not shown) is formed and patterned, covering a half of the illustrated structure, and an implantation is performed to introduce an n-type impurity, forming n+ drain region **80**. The first photo resist is then removed, and a second photo resist is formed to cover the other half of the illustrated structure. An implantation is then performed to introduce a p-type impurity, forming p+ source region **82**. The second photo resist is then removed. Preferably, the implantations are substantially vertical.

FIG. **25** illustrates the formation of n+ drain extension region **84** and p+ source extension region **86**. To form n+ drain extension region **84**, a photo resist is formed and patterned. A tilt implantation, which tilts toward the dummy gate stack, is then performed. The implantation energy is preferably less than the energy used for implanting n+ drain region **80**. Accordingly, as shown in FIG. **25**, the bottoms of n+ drain extension region **84** and p+ source extension region **86** are higher than the bottoms of the respective n+ drain region **80** and p+ region source **82**. The photo resist is then removed. Similarly, p+ source extension region **86** is also formed using essentially the same tilt implantation process as n+ drain region **80**.

Referring to FIG. **26**, ILD **44**, gate dielectric **50**, and gate electrode **52**, which are preferably essentially the same as in the first embodiment, are formed.

In the embodiments discussed in the preceding paragraphs, the left sides of the structures are referred to as the drain sides and the right sides are referred to as source sides. One skilled in the art will realize that the source and drain sides are interchangeable, providing appropriate voltages are applied. In addition, although the first, the second, and the third embodiments use gate-last approaches, wherein the respective gate dielectrics and gate electrodes are formed after the formation of source/drain regions by replacing dummy gate stacks, one skilled in the art will realize that gate-first approach may also be used. FIG. **27** illustrates an exemplary tunnel FET device with a gate-first structure. Contacts **86** are electrically connected to drain region **32** and source region **36**. Contact etch stop layer **88** is formed over drain region **32**, source region **36**, and gate **90**. Preferably, for p-channel tunnel FET devices, the respective CESLs provide compressive stresses, while for n-channel tunnel FET devices, the respective CESLs provide tensile stresses.

Simulations have been performed to compare the results of the embodiments of the present invention to conventional MOSFET devices and asymmetric tunnel FET devices, wherein the conventional tunnel FET devices have an asymmetric structure as shown in FIG. **2**. The results are shown in Table 3:

TABLE 3

	Conventional MOSFET		Conventional Tunnel FET		Embodiment 1		Embodiments 2 and 3	
	NFET	PFET	NFET	PFET	NFET	PFET	NFET	PFET
Ion	1	0.5	1	0.01	1	1	1	1
Ioff	1	1	10^{-6}	10^{-6}	10^{-4}	10^{-4}	10^{-6}	10^{-6}

Wherein the second row indicates the type of the FET devices, the third row shows drive currents of the FET devices, and the fourth row shows the leakage currents. The current values are relative currents (or current ratios) relative to the respective currents of the conventional n-type MOSFETs. The results have shown that the drive currents of the embodiments of the present invention are comparable to conventional MOS devices. However, the leakage currents of the embodiments of the present invention are significantly lower. Compared to the conventional tunnel FET devices, the first embodiment of the present invention has higher p-channel drive currents, although the leakage currents are higher. The n-channel characteristics of the second and the third embodiments of the present invention are comparable to the conventional tunnel FET devices. However, the p-channel characteristics of the second and the third embodiments are significantly better than the conventional p-channel tunnel FET devices.

The embodiments of the present invention have several advantageous features. First, the tunnel FET devices break the conventional MOSFET sub-threshold swing limit, and thus can achieve very high on/off current ratios. Second, the embodiments of the present invention may be applied to both p-channel and n-channel tunnel FET devices without sacrificing either on-currents or off-currents. Third, the current-voltage characteristics have weak temperature dependence and can be used for high-temperature applications. Lastly, the embodiments of the present invention have excellent resistance to short-channel effects and can be used for analog and digital applications with one channel length.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed is:

1. A method comprising:

forming a gate dielectric over a first semiconductor layer, wherein the first semiconductor layer is overlying and contacting a second semiconductor layer, and wherein the first semiconductor layer has a first band-gap smaller than a band-gap of the second semiconductor layer;

forming a gate electrode over the gate dielectric;

forming a first source/drain region adjacent the gate dielectric, wherein the first source/drain region is of a first conductive type; and

forming a second source/drain region adjacent the gate dielectric and on an opposing side of the gate electrode than the first source/drain region, wherein the second source/drain region is of a second conductivity type opposite the first conductivity type.

2. The method of claim **1**, wherein the steps of forming the first and the second source/drain regions comprise implanting an n-type impurity and a p-type impurity, respectively, into portions of the first semiconductor layer not masked by the gate electrode.

3. The method of claim **1**, wherein the steps of forming the gate dielectric and the gate electrode comprise:

forming a dummy gate stack;

forming gate spacers on sidewalls of the dummy gate stack;

removing the dummy gate stack after the steps of forming the gate spacers and the first and the second source/drain regions;

forming a gate dielectric layer and a gate electrode layer in a space left by the dummy gate stack; and

performing a chemical mechanical polish to remove excess portions of the gate dielectric layer and the gate electrode layer, wherein remaining portions of the gate dielectric layer and the gate electrode layer form the gate dielectric and the gate electrode, respectively.

4. The method of claim **1**, wherein the first source/drain region is doped heavily to have an impurity concentration higher than about $10^{20}/cm^3$, and the second source/drain region is doped moderately to have an impurity concentration between about $10^{18}/cm^3$ and about $10^{20}/cm^3$.

5. The method of claim **1**, wherein the steps of forming the first and the second source/drain regions comprise:

implanting portions of the first semiconductor layer to form a first and a second source/drain extension region, respectively, wherein portions of the first semiconductor layer on opposite sides of the gate electrode are at least moderately doped with impurities having opposite conductivity types;

recessing the first semiconductor layer to form recesses;

filling the recesses with a semiconductor material having a higher band-gap than the first semiconductor layer to form a first and a second semiconductor region; and

implanting the first and the second semiconductor regions with impurities having opposite conductivity types to foam a first and a second source/drain region, respectively.

6. The method of claim **1**, wherein the steps of forming the first and the second source/drain regions comprise:

recessing the first semiconductor layer to form recesses;

filling the recesses with a semiconductor material having a higher band-gap than first semiconductor layer to form a first and a second semiconductor region;

performing a first and a second implantations substantially vertical to implant the first and the second semiconductor regions with impurities of the first and the second conductivity types, respectively; and

tilt performing a third and a fourth implantation to form a first and a second source/drain extension region adjoining the first and the second semiconductor regions, respectively, wherein the third and the fourth implantations are not vertical to an interface between the gate dielectric and the first semiconductor layer, and wherein the first and the second source/drain extension regions are at least moderately doped and have same conductivity types as the first and the second semiconductor regions, respectively.

7. The method of claim **6**, wherein the first and the second implantations are performed with higher energies than the third and the fourth implantations, respectively.

8. The method of claim **6**, further comprising epitaxially growing a silicon germanium layer, wherein the first semiconductor layer comprises the silicon germanium layer.

9. A method comprising:

forming a semiconductor layer over and contacting a semiconductor substrate, wherein the semiconductor layer

has a first band-gap smaller than a second band-gap of the semiconductor substrate;

forming a dummy gate stack over the semiconductor layer;

implanting portions of the semiconductor layer unmasked by the dummy gate stack, wherein the portions of the semiconductor layer on opposite sides of the dummy gate stack are at least moderately implanted with impurities having opposite conductivity types;

forming gate spacers on sidewalls of the dummy gate stack after the step of implanting;

using the dummy gate stack and the gate spacer as a mask to recess the semiconductor layer to form recesses;

filling the recesses with a semiconductor material having a higher band-gap than the semiconductor layer to form a first and a second semiconductor region;

implanting the first and the second semiconductor regions with impurities having opposite conductivity types;

removing the dummy gate stack;

forming a gate dielectric layer and a gate electrode layer in a space left by the dummy gate stack; and

performing a chemical mechanical polish, wherein remaining portions of the gate dielectric layer and the gate electrode layer form a gate dielectric and a gate electrode, respectively.

10. The method of claim **9**, wherein the step of recessing comprises plasma etching.

11. The method of claim **9**, wherein the step of recessing comprises:

implanting amorphizing species into exposed portions of the semiconductor layer to form amorphized regions; and

selectively etching the amorphized regions.

12. The method of claim **9**, wherein the step of removing the dummy gate stack comprises:

forming an inter-layer dielectric (ILD);

planarizing a top surface of the ILD to level with a top surface of the dummy gate stack; and

etching the dummy gate stack.

13. The method of claim **9**, wherein the step of forming the semiconductor layer comprises epitaxially growing the semiconductor layer having a band-gap lower than a band-gap of silicon.

14. A method comprising:

forming a semiconductor layer over and contacting a semiconductor substrate, wherein the semiconductor layer has a first band-gap smaller than a second band-gap of the semiconductor substrate;

forming a dummy gate stack over the semiconductor layer;

forming gate spacers on sidewalls of the dummy gate stack;

using the dummy gate stack and the gate spacers as a mask to recess the semiconductor layer to form recesses;

filling the recesses with a semiconductor material having a higher band-gap than the semiconductor layer to form a first and a second semiconductor region;

performing a first and a second implantation substantially vertically to implant the first and the second semiconductor regions with impurities having opposite conductivity types, wherein a first source/drain region and a second source/drain region are formed;

tilt performing a third and a fourth implantation to form a first and a second source/drain extension region adjoining the first and the second semiconductor regions, respectively, wherein the third and the fourth implantations are not vertical to an interface between the semiconductor layer and the semiconductor substrate, and wherein the first and the second source/drain extension regions are at least moderately doped and have same conductivity types as the first and the second semiconductor regions, respectively;

removing the dummy gate stack;

forming a gate dielectric layer and a gate electrode layer in a space left by the dummy gate stack; and

performing a chemical mechanical polish, wherein remaining portions of the gate dielectric layer and the gate electrode layer form a gate dielectric and a gate electrode, respectively.

15. The method of claim **14**, wherein the first and the second implantations are performed with higher energies than the third and the fourth implantations, respectively.

16. The method of claim **15**, wherein the first and the second source/drain extension regions have depths smaller than depths of the respective first and the second source/drain regions.

17. The method of claim **14**, wherein the step of recessing comprises plasma etching.

18. The method of claim **14**, wherein the step of recessing comprises an isotropic etching.

19. The method of claim **14**, wherein the step of recessing comprises:

implanting amorphizing species into exposed portions of the semiconductor layer to form amorphized regions; and

selectively etching the amorphized regions.

20. The method of claim **14**, wherein the step of removing the dummy gate stack comprises:

forming an inter-layer dielectric (ILD);

planarizing a top surface of the ILD to level with a top surface of the dummy gate stack; and

etching the dummy gate stack.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.	: 8,697,510 B2
APPLICATION NO.	: 13/741086
DATED	: April 15, 2014
INVENTOR(S)	: Krishna Kumar Bhuwalka

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims

In Col. 12, line 37, claim 5, delete "foam" and insert --form--

Signed and Sealed this
Twenty-ninth Day of July, 2014

Michelle K. Lee

Michelle K. Lee
Deputy Director of the United States Patent and Trademark Office