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MAGNETIC CORE SWITCHING AND SELECTING CIRCUITS

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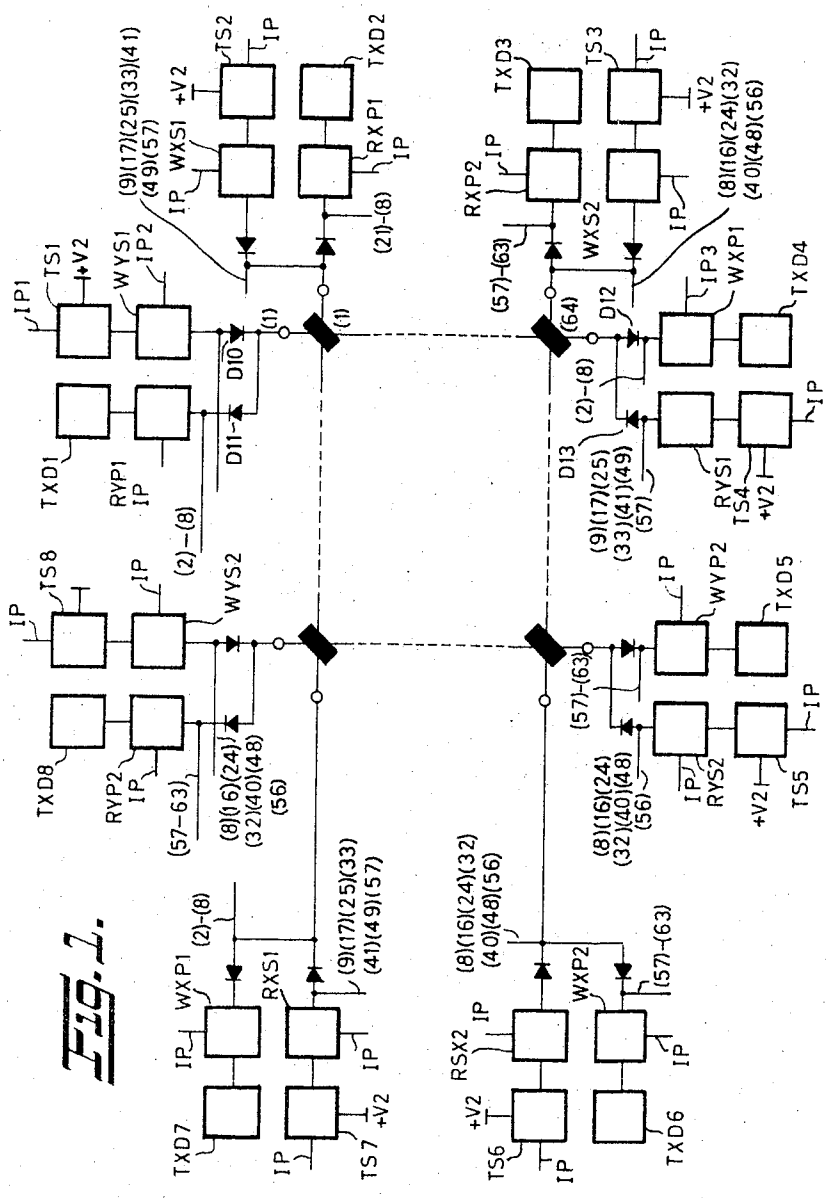


Fig. 1.

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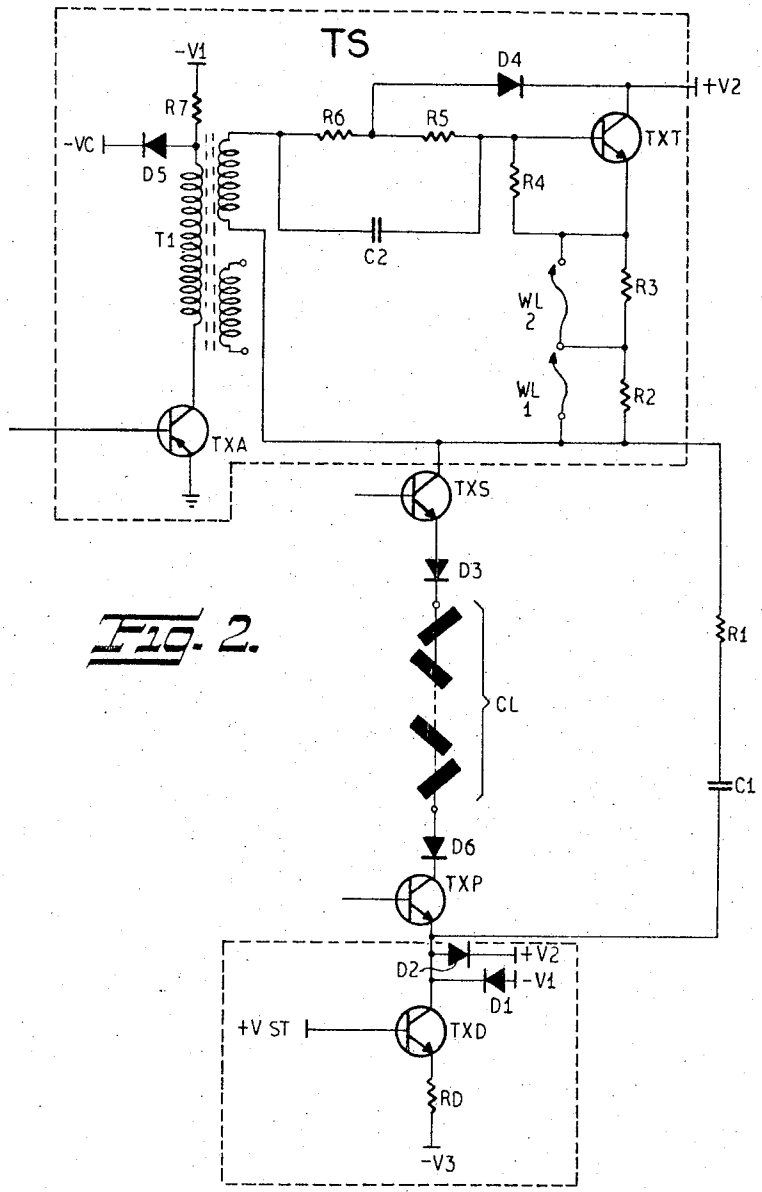


Fig. 2.

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MAGNETIC CORE SWITCHING AND SELECTING CIRCUITS

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The invention relates to transistor switching and selecting circuits for connecting a constant current pulse signal to an inductive load and finds particular application in coincident current types of magnetic memory systems.

Memories of the coincident current type comprise a matrix of crossing control lines having a magnetic core at each intersection or at a plurality of intersections. Each magnetic core is controlled by a pulse applied to each of two control lines or to at least two of a plurality of control lines at the point of intersection at which the required core is situated, the arrangement being such that the core is energised when coincident pulses are applied to the required point of intersection. The cores are driven between two states of saturation, one saturation state being arbitrarily taken as the "1" state and the other saturation state as the "0" condition.

In coincident current memory matrices the uniformity of the coincident currents applied to obtain both conditions of saturation is essential. For example in a single plane matrix, should one of the coincident current pulses applied to accomplish saturation be less than the necessary half-switching value, the selected core will not be switched. On the other hand, when one of the coincident current pulses is too great, other than selected cores connected to receive that pulse may be switched.

In addition, it has been determined that a magnetic core is never driven to what might be termed "absolute saturation," for the driving current pulse required to obtain such a condition would be of an infinite amplitude value. For this reason, different current pulses applied to a magnetic core switch the core along slightly different hysteresis paths. If then, a first current pulse is applied to drive a core to a first saturation condition and a second current of a different value is applied to drive the core to the opposite condition, when either current pulse is reapplied after the initial application thereof, the core is driven on a hysteresis path different from that on which it was driven when the current was initially applied.

Since the output current which may be measured is directly related to the hysteresis path of the switching operation, output signals will vary unless substantially-identical current pulses are applied for switching the magnetic cores to both saturation conditions.

It is clearly desirable that suitable switching circuits shall be available for providing the requisite "read-out" and "write" currents for a magnetic core matrix store and these switching circuits, often called selectors, should moreover have a very short operating time in order that the speed of operation of the store shall not be impaired. It is usual to use transistor circuits for such selectors and in known systems it is usual to operate a current definer circuit and primary and secondary selector circuits for each row and column selection. The use of primary and secondary selectors allows, for example, a total of thirty-two (i.e. 16 primary and 16 secondary) selectors in a 64 x 64 bit matrix to be used together with sixteen current definer circuits instead of sixty-four selectors and sixty-four current definers for the same size matrix.

Certain difficulties are encountered when transistor circuits are employed for the selectors when a large capacity fast access store is required. The first difficulty encountered is due to the back E.M.F. generated across the core line when a half current pulse is connected to the drive wire. This back E.M.F. may be of the order of 20–25 volts in a large store and, as the emitter electrode of the secondary selector transistor is connected to the core line, non-selected selectors may be erroneously switched. The second difficulty is experienced with reference to power handling capacities for the transistors employed. In constant current switching systems, the primary selector transistor must remain unsaturated to allow the core line to be driven from a high source impedance. However, transistors having such power handling capabilities are relatively slow acting devices. The third and final difficulty, again with reference to power handling capacity transistors, is the fact that substantially large drive requirements must be satisfied for the power transistors making unsuitable the normal logic levels employed in the store control circuitry.

It is the object of the invention to overcome the above-mentioned difficulties and to provide a relatively cheap and efficient transistorised switching and selecting circuit for use in the control of core lines in a large capacity fast access magnetic core matrix store.

According to the invention in a magnetic core matrix arranged to operate on the coincident current principle and employing transistor selecting circuits for selecting one of a plurality of column drive wires and one of a plurality of row drive wires, the selecting circuits each including a current defining circuit, a primary selector stage connected between the output of the current defining circuit and one end of the drive wire and a secondary selector stage connected to the other end of the drive wire, the transistor in each of said current defining circuits is permanently conductive to a defined state and is operatively associated with a first source of operating potential connected to said transistor when the drive wire is not being selected and is operatively associated with an alternative source of operating potential on the operation of a third selector stage, the alternative source of potential being connected to the current defining circuit over the primary selector stage, the drive wire, the secondary selector stage and the third selector stage and the operation of the selecting circuit is such that when the primary and secondary selector stages are conditioned for operation, the third selector stage upon activation controls the passage of a defined current pulse through the drive wire the current pulse beginning after the beginning of and ending before the ending of the period during which the primary and secondary selector stages are conditioned for operation.

The invention will be better understood from the following description taken in conjunction with the accompanying drawings comprising FIGS. 1 and 2. Of the drawings,

FIG. 1 shows diagrammatically a 64 x 64 magnetic core matrix store and

FIG. 2 shows in more detail the selector stages and current defining circiut for one core line CL.

Referring first to FIG. 1, the drawing shows only two column core lines **1** and **64** and two row core lines also **1** and **64**. Each core line is used for reading and writing by reversal of the direction of current flow over the line. For writing purposes, there is provided for each core line a timing selector stage such as TS1 for column core line **1**, a secondary selector such as WYS1, a primary selector such as WYP1 and a current defining circiut such as TXD4. Similarly for reading purposes, there is provided for each core line a timing selector stage such as TS4 for column core line **1**, a secondary selector such as RYS1, a primary selector such as RYP1 and a current defining circuit such as TXD1. The writing and reading circuits are separated electrically by the diodes **D10**, **D11**, **D12** and

D13, and it will be seen that similar drive arrangements are provided for the row core lines. The blocks in FIG. 1 representing the timing selectors TS1 to TS8 consist of the circuit shown within the dotted lines in FIG. 2 and referenced TS and the blocks representing the primary and secondary selectors consist of the same circuit with some slight differences which will be explained when describing FIG. 2 in detail. In addition the blocks in FIG. 1 representing the current defining circuits TXD1 to TXD8 all consist of the circiut contained within the dotted rectangle, of the transistor TXD of FIG. 2. In FIG. 1, the input leads corresponding to lead IP in FIG. 2 are referenced IP1, IP2 and IP3 for timing selector TS1, secondary selector WYS1 and primary selector WYP1 respectively, the other input leads in FIG. 1 being given the general reference IP.

The core lines are divided into groups of eight and the method of selecting a core line is such that the primary selectors are each connected to all the core lines of a particular group while the secondary selectors are each connected to corresponding core lines in all the groups. Thus the write primary selector WYP1 as indicated in FIG. 1, is connected to core lines 1 to 8 i.e. to all the core lines of the first group whereas the write secondary selector WYS1 is connected to core lines 1, 9, 17, 25, 33, 41, 49 and 57 i.e. the first core line in each of the eight groups. Similarly the read primary selector RYP1 is connected to core lines 1 to 8 whereas the read secondary selector RYS1 is connected to core lines 1, 9, 17, 25, 33, 41, 49 and 57. The write and read primary and secondary selectors WYP2, WYS2, RYP2 and RYS2 are similarly connected and so are the write and read primary and secondary selectors WXP1, WXP2, WXS1, WXS2, RXP1, RXP2, RXS1 and RXS2 for the row core lines. The references in brackets attached to various leads in FIG. 1 indicate the core lines to which such leads are connected.

Referring now to FIG. 2 only the timing selector stage TS, using transitsor TXT, is shown in detail, the primary and secondary selector stages, using transistors TXP and TXS respectively, being the same as the timing selector stage except that resistors R2 and R3 and their associated wander leads L1 and WL2 are omitted. The circuit arrangement employing transistor TXA is a typical output stage for a pulse amplifier which is used to drive the timing selector stage while transistor TXD is employed in the current pulse definer circuit.

In the quiescent state of the circuits, i.e. when no magnetic core lines are being selected, all the current defining transistors TXD (TXD1 to TXD8, FIG. 1) conduct. These transistors are arranged to pass a standard current defined by the value of emitter resistor RD (FIG. 2) and the stabilised base voltage +VST which is positive with respect to earth. Diode D1 is included to provide a source of current for transistor TXD while the other selector stage transistors are cut off, voltages —V3 being more negative than voltage —V1 and both these voltages being negative with respect to earth.

Assume it is now required to select the core line CL for writing purposes, then the primary and secondary selector stages WYP1 and WYS1 (FIG. 1) are actuated by the leading edge of an input drive pulse on input leads IP2 and IP3. However, the transistors TXP and TXS (FIG. 2) in these selector stages do not conduct sufficiently to provide enough collector current at this time to have any appreciable effect on the magnetic cores threaded by core line CL. The duration of the input drive pulse to the primary and secondary selector stages is defined by the characteristics of the input transformers corresponding to T1 and is arranged to be of greater duration than that which will be generated by transformer T1 of the timing selector.

The timing selector stage TS, using transistor TXT, is operated by a negative-going edge, which may typically be from 0 volt to —6 volts, applied to the base of transistor TXA, the selector stage drive amplifier output transistor. The input drive edge causes transistor TXA to conduct providing a sharp change in current in the primary winding of transformer T1. The voltage ratio of this transformer is arranged to give maximum voltage drive to the selector stage without starving the clamping diode D5 of current when transistor TXA is conducting and the drive pulse generated by the transformer is "on." Resistor R7 in the collector of transistor TXA is provided to limit the collector current to a value within the power rating of the transistor used in the event of transistor TXA being left conducting due to fault conditions.

The current pulse produced in the secondary winding of transformer T1 is passed by resistors R5 and R6 to cause transistor TXT to conduct. Capacitor C2 is provided to decrease the rise time of the leading edge of the current pulse. Two secondary windings are shown the second being connected to another timing selector (not shown) which may be used to drive half the stack of a large capacity magnetic core matrix. The second secondary winding would, of course, not be provided in any of the selector stages.

When transistor TXT conducts transistors TXS and TXP both pass collector current and in fact, these, transistors pass the total collector current of the current definer transistor TXD. As mentioned previously this current is the closely defined half-current pulse required for coincident current core selection. It will be appreciated at this point that it is desirable that the maximum voltage available is used to drive the core line CL. For this reason it is important that the selector stage transistors have as small voltage drop across them as is practical and ideally these transistors should saturate. However, saturation causes a delay in switching off and, therefore, an anti-saturation diode, such as D4 in the timing selector stage, is included to prevent saturation but limit the voltage drop across the transistors.

When the current pulse from the secondary winding of transformer T1 is complete, transistor TXT is cut off thus terminating the current pulse in core line CL. Diode D1 will again provide collector current for transistor TXD. The back E.M.F. built up across the core line CL will cause the collector of transistor TXS to become positive with respect to earth. The back E.M.F. is prevented from reaching a value which would damage transistor TXD by means of diode D2. This diode prevents the collector of transistor TXD from becoming more positive than +V2 which is arranged to be within the maximum inverse collector/omitter voltage rating for this transistor. Furthermore, when the timing selector stage transistor TXT is switched on and off, the momentarily large and rapid voltage changes at the collector of the current definer transistor TXD coupled via both secondary windings of the primary input transformer to the undriven primary winding, on a primary selector stage served by the same current definer but not required for the particular selection, and then transformed back to the secondary windings of this unselected primary selector stage may cause this primary selector to operate. This unwanted primary selector stage is also associated with the secondary selector stage required, so that two core lines will be selected which obviously cannot be tolerated.

To prevent the difficulties mentioned above a resistor such as R4 shown in the timing selector stage, is provided in both primary and secondary selector stages. This resistor successfully damps out these voltage surges. Resistor R4 may, in the primary selector stage, be replaced by a diode, cathode to the base of transistor TXP, if more efficient damping is required.

After the completion of the timing selector stage drive pulse the primary and secondary selector stage drive pulse terminate and these selector stage transistors are cut off.

From the above description it will be seen that the current definer transistor TXD is permanently conductive and therefore a "slow" relatively inexpensive transistor

may be employed. As the selector stages are transformer fed no elaborate voltage changing circuits are required to provide sufficient drive to these stages and therefore they may be incorporated in the logic switching control arrangements provided for a large capacity fact access store employing normal logic voltage levels. Resistors R2 and R3 are provided with their associated shorting wander leads WL1 and WL2 to even-up the differences in rise times experienced with high and low gain transistors. This may alternatively be achieved by the use of a tapped drive transformer. Resistor R1 and capacitor C1, which have been omitted from FIG. 1 in order not to over-complicate the drawings, are provided as a compensation network to reduce overshoot in the current pulse. The actual values will be affected by the amount of stray capacitance experienced in a built-up store.

It will be appreciated that the invention is not limited to the precise method of core line selection described with reference to FIG. 1 but is applicable to any method which employs a primary selector connected to one end of the core line and a secondary selector connected to other end of the core line.

The description has concentrated on n-p-n transistors for the current definer and selector stage transistors and this is intended to be in no way limiting to the invention. It will be obvious to those skilled in the art that p-n-p transistors may be employed with suitable adjustments in voltage levels.

I claim:

1. A magnetic core storage matrix arranged to operate on the coincident current principle and comprising a plurality of column drive wires, a plurality of row drive wires, a plurality of magnetic cores, one at each of the intersections of the column drive wires with the row drive wires selecting circuits for selecting one of said column drive wires and one of said row drive wires, each selecting circuit including a transistor current defining circuit, a primary transistor selector stage connected between the output of said current defining circuit and one end of the drive wire associated therewith, a secondary transistor selector stage connected to the other end of said drive wire, a first source of operating potential for maintaining the transistor in said current defining circuit conductive to a defined state when said drive wire is not being selected, means for conditioning said primary transistor and secondary transistor selector stages for operation, a third selector stage, an alternative source of operating potential for the transistor in said current defining circuit, means for operating said third selector stage to connect said alternative source of operating potential to the transistor in said current defining circuit whereby the defined conductive state of the transistor in said current defining circuit is maintained and a current pulse is passed through said drive wire, the current pulse beginning after the beginning and ending before the ending of the period during which said primary and secondary selector stages are conditioned for operation.

2. A magnetic core storage matrix as claimed in claim 1, wherein said first operating source of potential is connected to said current defining circuit over a diode which is so arranged that it is reverse biased when said third selector stage is activated and forwardly biased when said third selector stage is not activated.

3. A magnetic core storage matrix as claimed in claim 2, wherein a further diode is connected to the current defining circuit at one end and to a further source of potential at the other said diode being arranged to conduct and to prevent damage to said current defining circuit by the back e.m.f. generated across said core line when said third selector stage is switched from the active to the non-active state.

4. A magnetic core storage matrix as claimed in claim 1, wherein the selector stages are pulse operated over individual input transformers, the characteristics of which are such that the duration of the input drive pulse to the primary and secondary selector stages is greater than the duration of the input drive pulse to the third selector stage.

5. A magnetic core storage matrix as claimed in claim 4, wherein the input transformer of a selector stage is connected to the base of the transistor of that stage over a resistor and a point on said resistor is connected to the anode of a diode, the cathode of which is connected to the collector of the transistor.

6. A magnetic core storage matrix as claimed in claim 4, wherein a resistor is connected between the base and emitter of the transistors in the selector stages, the resistor having such a value as to damp any voltage surges due to the switching on and off of the transistor in the third selector stage.

7. A magnetic core storage matrix as claimed in claim 1, wherein a series-connected resistor and capacitor are connected between the collector of the transistor in the secondary selector stage and the emitter of the transistor in the primary selector stage.

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