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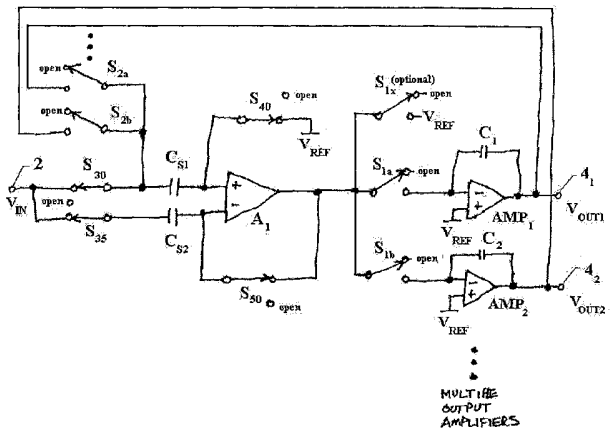
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(54) Title: ANALOG DEMULTIPLEXER



(57) Abstract: The analog demultiplexer (Fig. 6) includes an input amplifier (A_1), and output amplifiers (AMP_1-AMP_N). The output and inverting (-) input of amplifiers (AMP_1-AMP_N) are connected by a respective capacitor (C_1-C_N). Switches (S_{1a}, S_{1b}, etc.) connect the output of amplifier (A_1) to the inverting input of one of (AMP_1-AMP_N). Switches (S_{2a}, S_{2b}, etc.) connect the output of one of (AMP_1-AMP_N) to the non-inverting input of the amplifier A_1. Switches (S_{2a}, S_{2b}, etc.) and (S_{1a}, S_{1b}, etc.) open and close together in pairs. With feedback from the output of (AMP_1-AMP_N) through (A_1), the gain and any offset of (AMP_1-AMP_N) is divided down by the gain of (A_1). Amplifier (A_1) has capacitors (C_{S1} and C_{S2}) connected to its inputs. Switch (S_{50}) connects the inverting input of amplifier (A_1) to its output, and switch (S_{40}) connects the non-inverting input of (A_1) to a voltage reference (V_{REF}) matching (V_{REF}) applied to (AMP_2). Switches (S_{30}) and (S_{35}) connect (C_{S1}) and (C_{S2}) to the demultiplexer input (2). In operation, switches (S_{40}, S_{50}, S_{30} and S_{35}) are initially closed, while switches (S_{2a}, S_{2b}, etc.) are open to charge both capacitors (C_{S1}) and (C_{S2}) and the inputs and output of (A_1) to (V_{REF}). Switch (S_{50}) provides feedback to divide down gain errors and offset of (A_1). Switches (S_{30}, S_{35}, S_{40} and S_{50}) are then open, while one of switches (S_{2a}, S_{2b}, etc.) is closed with one switch (S_{1a}, S_{1b}, etc) to drive one of the output voltages (V_{OUT1}-V_{OUTN}). With inputs and outputs of (A_1) and the connected (AMP_1-AMP_N) initially be at (V_{REF}), very little settling time is needed.

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ANALOG DEMULTIPLEXER

CLAIM OF PRIORITY TO PROVISIONAL APPLICATION

This application claims priority to provisional application SC/Serial No. 60/317,482, entitled "Analog Demultiplexer" filed September 5, 2001.

CROSS REFERENCE TO RELATED APPLICATION

U.S. Patent Application Serial No. _____ entitled "A Method And Apparatus To Generate Reference Voltages For Flat Panel Displays" filed simultaneously with this application on September 5, 2002 is incorporated herein by reference..

BACKGROUND

Technical Field

The present invention relates to analog demultiplexer for distributing signals from a single input line to one of multiple output lines. In particular, the present invention relates to an analog demultiplexer for distributing a video input signal to one of several video display column drivers, with the analog demultiplexer having minimal offset due to its amplifiers, and having a minimal amplifier settling time.

Related Art

Fig. 1 shows one conventional configuration for an analog demultiplexer. The analog demultiplexer allows a multiplexed analog input voltage V_{IN} received at input 2 to be demultiplexed using a switch S_1 to provide an output voltage V_{OUT1}-V_{OUTN} at a respective one of outputs 4_1-4_N. The logic control driving switch S_1 toggles switch S_1 to direct an input voltage V_{IN} to one specific output buffer AMP_1-AMP_N. In this way, an input voltage provided at

input V_{IN} can be demultiplexed to one of numerous output buffers AMP_1-AMP_N.

Assuming the input voltage V_{IN} at input 2 is to be sampled as output voltage V_{OUT1} at output 4_1, switch S_1 closes to connect amplifier A_1 to the capacitor C_1 and the input of amplifier AMP_1. The voltage at V_{IN} is sampled onto capacitor C_1 and the buffered voltage appears on V_{OUT1}. Then the switch S_1 is opened. The hold capacitor C_1 retains the sampled voltage, and thus, the voltage at V_{OUT1} remains constant for a period of time. In a similar manner, the input voltage V_{IN} at input 2 can be connected using switch S_1 to sample and hold the input voltage V_{IN} using another one of the capacitors C_2-C_N and its corresponding amplifier AMP_2-AMP_N.

The undesirable effects of the analog demultiplexer of the configuration of Fig. 1 are as follows:

(1) The amplifiers A_1 and AMP_1-AMP_N all create a voltage offset from the signal at V_{IN};

(2) The amplifiers A_1 and AMP_1-AMP_N are all shown with a gain of +1, but gain errors occur;

(3) A pedestal voltage offset error occurs when the switch S_1 opens; and

(4) The output amplifiers AMP_1-AMP_N are NOT identical - - Or the same input voltage at V_{IN} generates a different output at each output $VOUT_1$-$VOUT_N$.

To improve the performance of analog demultiplexers, several approaches have been used. These approaches are described to follow.

A. 1st Improvement

A first improvement over the analog demultiplexer of Fig. 1 is shown in Fig. 2. In operation, assuming the voltage V_{IN} at input 2 is to be sampled as an output voltage V_{OUT1} at output 4_1, then switch S_1 closes and connects the output

of amplifier A_1 to capacitor C_1 and the non-inverting input of amplifier AMP_1. At the same instant a second switch S_2 closes, connecting the output of amplifier AMP_1 to the inverting input of amplifier A_1. Note components carried over from Fig. 1 to Fig. 2 are similarly labeled, even though they are connected in a different manner, as will be components carried over into subsequent figures. The equivalent circuit for this switch state for Fig. 2 is shown in Fig. 3.

With feedback from output amplifier AMP_1 to A_1, the equivalent circuit is assumed to have a unity gain configuration. Assuming that the circuit is stable and the gain of both amplifier A_1 and amplifier AMP_1 are very large, any offset of AMP_1 is divided down by the gain of A_1. The voltage V_{IN} plus the offset of amplifier A_1 is sampled onto the hold capacitor C_1. So,

$$V_{OUT1} = V_{IN} + Vos(\text{offset of } A_1)$$

Advantages of the configuration of Fig. 2 are as follows:

(1) The voltage offset of AMP_1 is divided down by the gain of A_1; and
(2) The gain error or AMP_1 is divided down by the gain of A_1.

Undesirable effects of the configuration of Fig. 2 are as follows:

(1) The voltage offset of amplifier A_1;
(2) A voltage offset caused by charge injection of switch S_2 when it opens;
(3) The gain error of amplifier A_1; and
(4) A long settling time after switch S_2 closes.

Before switch S_2 of Fig. 2 closes, amplifier A_1 would be in an open loop configuration. Thus, its output will be in an undetermined voltage state. Amplifier A_1 is "saturated". Amplifier A_1 returns into its "active" region by

glitching and ringing its output before it settles. (Settling time depends on the Bandwidth and Phase Margin of the cascaded amplifiers). When the output of amplifier A_1 rings, so does V_{OUT1}, an undesirable effect.

B. 2nd Improvement

A second improvement over the analog demultiplexer of Fig. 1 is shown in Fig. 4. In the circuit of Fig. 4, a hold capacitor C_1, C_2, etc. is placed between the inverting input and output of each of the output amplifiers AMP_1, AMP_2, etc. Switches S_1 and S_2 operate as a pair to connect one of the output amplifiers AMP_1, AMP_2, ... between the output of amplifier A_1 and its non-inverting input. A switch S_3 connects the output of A_1 to a reference voltage V_{REF} when the switches S_1 and S_2 are not connected. The non-inverting input of the output amplifiers AMP_1, AMP_2,... are likewise connected to the reference V_{REF}.

In operation it is first assumed that V_{IN} is to be sampled to V_{OUT1}. Switch S_1 then closes and connects the output of amplifier A_1 to capacitor C_1 and the inverting input of amplifier AMP_1. At the same instant, switch S_2 closes, connecting the output of amplifier AMP_1 to the non-inverting input of amplifier A_1. Switches S_1 and S_3 are non-overlapping, or are not connected at the same time. The equivalent circuit of such a connection is shown in Fig. 5.

With feedback, the circuit is in a unity gain configuration. If the gain of amplifier A_1 and AMP_1 are large, then

$$V_{OUT1} \sim V_{IN} + Vos1 \text{ (offset of amplifier } A_1).$$

With amplifier AMP_1 in a feedback path, its inverting input (which is also the output of amplifier A_1) is approximately equal to V_{REF}. For this unity-gain configuration to settle fast, both sides of switch S_1 have to be approximately V_{REF} before switch S_1 closes.

So, the output of the amplifier A_1 should be approximately at V_{REF} before switch S_1 closes. This is done by clamping the output of A_1 to V_{REF} by turning on switch S_3 (note: switch S_1 and S_3 are non-overlapping). This ensures that amplifier A_1 stays in the "active" region resulting in a faster settling time.

Advantages of the configuration of Fig. 4 are as follows:

(1) The voltage offset of AMP_1 is divided down by the gain of A_1, and is negligible.

(2) The settling time is reduced (Voltage at both sides of switch S_1 are approximately the same and amplifier A_1 is in its active region when switch S_1 closes).

(3) The gain error of AMP_1 is divided down by the gain of A_1.

Undesirable effects of the configuration of Fig. 4 are as follows:

(1) The voltage offset of amplifier A_1 remains;

(2) The gain error of amplifier A_1 remains; and

(3) Charge injection of switch S_1 to the output capacitor causing an offset error on the output.

SUMMARY

In accordance with the present invention, an analog demultiplexer is provided with the voltage offset and gain error of amplifiers AMP_1-AMP_N and A_1 divided down to a minimal value. Further, the analog demultiplexer has a minimal settling time, and charge injection from switch S_1 to the output generates a minimal offset error.

The analog demultiplexer in accordance with the present invention (referring to Fig. 6) includes an input amplifier A_1, and a plurality of output amplifiers AMP_1-AMP_N, similar to Fig. 2. The output and inverting (-) input of amplifiers AMP_1-AMP_N are connected by a respective capacitor C_1-C_N, as in

Fig. 2. Also, similar to Fig. 2, a switch S_1 (in the case of Fig. 6 multiple switches S_{1a}, S_{1b}, etc.) serve to connect the output of amplifier A_1 to the inverting input of a respective one of amplifiers AMP_1-AMP_N. Similar to Fig. 2, a switch S_2 (in the case of Fig. 6 multiple switches S_{2a}, S_{2b}, etc.) serve to connect the output of one of amplifiers AMP_1-AMP_N to the non-inverting input of the amplifier A_1. As in Fig. 2, switches S_{2a}, S_{2b}, etc. can function to switch together with respective ones of switches S_{1a}, S_{1b}, etc. As in Fig. 2, with feedback from the output of amplifiers AMP_1-AMP_N through A_1, the gain as well as the offset of any of AMP_1-AMP_N is divided down by the gain of A_1.

Unlike the circuit of Fig. 2, the amplifier A_1 has a capacitor C_{S1} connected to its non-inverting input and another capacitor C_{S2} connected to its inverting input. A switch S_{50} connects the inverting input of amplifier A_1 to its output, and a switch S_{40} connects the non-inverting input of amplifier A_1 to a voltage reference V_{REF} matching a voltage reference V_{REF} applied to the non-inverting input of amplifier AMP_2. A switch S_{30} connects the capacitor C_{S1} to receive the demultiplexer input 2, while a switch S_{35} connects the capacitor C_{S2} to the demultiplexer input 2. In operation, switches S_{40}, S_{50}, S_{30} and S_{35} are initially closed, while switches S_{2a}, S_{2b}, etc. are open to charge up both capacitors C_{S1} and C_{S2} to V_{REF} to assure both inputs of amplifier A_1 and its output are at V_{REF}. Switch S_{50} provides feedback to assure gain errors and offset of A_1 are divided down. Switches S_{30}, S_{35}, S_{40} and S_{50} are then open, while one of switches S_{2a}, S_{2b}, etc. is closed in correspondence with a switch S_{1a}, S_{1b}, etc. Since the inputs and output of both A_1 and the corresponding amplifier AMP_1-AMP_N will initially be at V_{REF}, very little settling time will be required to stabilize the respective output voltage V_{OUT1}-V_{OUTN}.

To improve switching speed in one embodiment, the switches S_{1a}, S_{1b}, etc. are formed from as a CMOS switch made from a combined PMOS and NMOS transmission gate. The NMOS transistor enables the circuit to switch fast, while the PMOS transistor being on after the circuit settles removes

voltage offset typically existing with only an NMOS transistor. Using a CMOS switch, in one embodiment a dummy switch can be added in series with the CMOS switch which is half the size to cancel any charge offset produced by the active switch. In another embodiment, the gate size of transistors for switches S_{1a}, S_{1b} etc. are reduced to limit any offset due to these switches.

BRIEF DESCRIPTION OF THE DRAWINGS

Further details of the present invention are explained with the help of the attached drawings in which:

Fig. 1 shows one conventional configuration for an analog demultiplexer;

Fig. 2 shows a first improvement over the analog demultiplexer of Fig. 1;

Fig. 3 shows an equivalent circuit for the switch state of Fig. 2;

Fig. 4 shows a second improvement over the analog demultiplexer of Fig. 1;

Fig. 5 shows an equivalent circuit for the switch state of Fig. 4;

Fig. 6 shows an analog demultiplexer in accordance with the present invention;

Fig. 7 shows the analog demultiplexer of Fig. 7 with connections only between the input amplifier A_1 and output amplifier AMP_1.

Fig. 8 shows an equivalent circuit for the switch state of Fig. 7.

Fig. 9 shows the equivalent circuit for Fig. 7 with switches S_{40} and S_{50} changing to an open state;

Fig. 10 shows the equivalent circuit for Fig. 7 with the S_{40} and S_{50} of Fig. 9 remaining open and additionally switches S_{30} and S_{35} opening;

Fig. 11 shows an equivalent circuit for Fig. 7 with the switches S_{30}, S_{40}, S_{50} remaining open, but switches S_{2a} and S_{1a} closing;

Fig. 12 shows an equivalent circuit with switches S_{30}, S_{40}, S_{50} remaining open, and switch S_{2a} remaining closed, but S_{1a} reopening;

Fig. 13 shows transistors used to create a switch S1a, and voltages applied to reduce any offset due to charge injection; and

Fig. 14 shows components for an embodiment of the input amplifier A1.

DETAILED DESCRIPTION

An approach for an analog demultiplexer in accordance with the present invention is shown in Fig. 6. Using this circuit and switching S_{1a}, S_{1b} ... etc. and S_{2a}, S_{2b} ... etc., control logic can guide V_{IN} to be sampled and held on a specific one of the output buffers AMP_1-AMP_N. Note that Fig. 6 shows use of multiple switches S_{1a}, S_{1b} ... etc. and S_{2a}, S_{2b} ... etc., as an alternative, a single switch could be used for all of switches S_{1a}, S_{1b} ... etc. or S_{2a}, S_{2b} ... etc.. However, use of multiple switches permits the input amplifier A_1 to be connected to more than one of the output amplifiers AMP_1-AMP_N at one time. Further note that although switches such as S_{1a} and S_{2a} typically open and close together simultaneously in prior art designs, in the present invention the switches may or may not close simultaneously.

For a description of operation, to simplify the system of Fig. 6, Fig. 7 is included showing only two amplifiers, assuming V_{IN} is to be sampled to an output amplifier AMP_1. Further, it is initially assumed that the gain of amplifier A_1 =A1 and the gain of amplifier AMP_1 = A2. The connection of switches in Fig. 7 enable the value V_{REF} to be maintained at the inputs and output of amplifiers A_1 and AMP_1-AMP_N prior to connection of the amplifier A1 to one of amplifiers AMP_1-AMP_N is described to follow with equivalent circuits shown for each stage.

A. 1st Stage

First, switches S_{40}, S_{50}, S_{30} and S_{35} are closed, making the circuit portion shown in Fig. 7 appear as shown in the equivalent circuit of Fig. 8. Amplifier A_1 is in a unity-gain configuration. Amplifier AMP_1 is in the "hold" state, keeping the previously set V_{OUT1} constant. Thus, the following applies.

$$Vx = A1(V_+ + V_{OS1} - V_-)$$
$$= A1(V_{REF} + V_{OS1} - Vx)$$
$$Vx(1+A1) = A1(V_{REF} + V_{OS1})$$
$$Vx = [A1/(1+A1)](Vref + V_{OS1})$$

Voltage across capacitor $C_{S1} = V_{CS1} = V_{IN} - V_{REF}$

Voltage across capacitor $C_{S2} = V_{CS2} = V_{IN} - V_X$
$$= V_{IN} - [A1(1+A1)](V_{REF} + V_{OS1}).$$

B. 2nd Stage

Next, switches S_{40} and S_{50} are opened creating a circuit as shown in Fig. 9. When switches S_{40} and S_{50} are opened, there is charge injected into capacitors C_{S1} and C_{S2}. The offset would be common mode if $S_{40}/C_{S1} \sim S_{50}/C_{S2}$. Assuming the size of switches $S_{40}=S_{50}$ and $C_{S1}=C_{S2}$, the offset to both capacitors caused by charge injection would be the same.

C. 3rd Stage

Next, in addition to the switches open in Fig. 9, switches S_{30} and S_{35} are opened creating a circuit as shown in Fig. 10. As a further option in this state, switch S_{1x} can be closed, connecting V_X to V_{REF} , so V_X is clamped to V_{REF}. Switch S_{1x} is then opened before stage 4.

D. 4th Stage

Next, switches S_{1a}, S_{2a} and S_{35} are closed creating a circuit as shown in Fig. 11. As configured in Fig. 11, the equations of Appendix I of this application apply.

E. 5th Stage

Next, switch S_{1a} is reopened as shown in Fig. 12, as the amplifier AMP_1 has sampled and will hold the value V_{IN} at the output V_{OUT1}.

F. 6th Stage

Next, or in conjunction with switch S_{1a}, switch S_{2a} is reopened, to prepare for a subsequent sampling since V_{IN} has been sampled and held by output amplifier AMP_1. The control logic can now start to sample V_{IN} to a different amplifier (for example AMP_2). With sampling to AMP_2, all the stages explained herein are then performed again, but with AMP_2 replacing AMP_1. After V_{IN} is sampled to AMP_2, the control logic samples V_{IN} to another amplifier and so on. To overcome voltage droop, the output amplifiers AMP_1-AMP_N are refreshed repetitively by a subsequent sampling of V_{IN}.

The advantages of the configuration in accordance with the present invention are as follows:

(1) The offset for both amplifier A_1 and AMP_1 are reduced by the gain of A_1;
(2) The circuit settles fast because both sides of switch S_{1a} are almost at the same potential before switch S_{1a} closes; and
(3) CMRR and gain error for both amplifiers are corrected.

To improve the charge injection in switch S_{1a}, the following additional steps can be performed:

(1) Use a small switch; and
(2) Use charge injection cancellation techniques like:

- in CMOS, use PMOS and NMOS transmission gates; and
- use a dummy switch.

Use of small switch, simply implies use of one or more transistors making up the switch with a small gate size. The smaller gate size reduces charge buildup, and thus charge injection when the switch opens or closes. Typically, a high voltage transmission gate is large in dimension to withstand the higher voltage applied on it. Due to the large gate size, a large charge will be lying underneath the gate when it is in its "on" state. When the switch opens, the charge will inject into the hold capacitor creating an offset seen on the output amplifier. The voltage driving the transmission gate switches will be between a high voltage and ground. The large voltage swing on the transmission gate feeds through to the hold capacitor through the overlap capacitance of the large switch, providing another source offset.

Use of CMOS designs enables reduction in charge injection since it uses PMOS transistors causing less charge buildup. The CMOS design still includes an NMOS transistor to which turns on initially much faster than the PMOS transistor. In CMOS high voltage designs, charge injection will still produce an offset in the hold capacitors of the output amplifiers. The offset is caused by the charge under the gate injecting into the hold capacitor when the switch opens. The amount of offset is determined by: (1) the control voltage swing of the switch; and (2) the size of the switch.

A low voltage CMOS switch 10 used for switch S_{1a} includes PMOS and NMOS transistors 11 and 12 as shown in Fig. 13. The source-drain path of the NMOS transistor 11 and PMOS transistor 12 are connected in parallel between the output of amplifier A_1 and an input of amplifier AMP_1. The gates of transistors 11 and 12 receive complementary control signals ϕ and ϕbar.

To avoid offset, particular control voltages as well as use of a dummy switch may be employed as further illustrated in Fig. 13. In the approach of

Fig. 13, two supply voltages are used for amplifier A_1. (Vdd=High voltage; V1d=low voltage). The output of amplifier A_1 is prevented from going above V1d (output of amplifier A1 can swing between Vss1 and V1d; Note: Vss1 and Vss could be tied together). The dummy switch 15 has transmission gates half the size of the transmission gates of transistors 11 and 12 forming the low voltage switch 10. The transmission gates of the dummy switch 10 are driven by a signal ϕ and ϕbar, similar to switch 10. Signals ϕ and ϕbar swing between voltages of V1d and Vss1. The output of amplifier A_1 is prevented from going above V1d so that a low voltage switch 10 and dummy switch 15 can be used for switch S_{1a}.

By using a low voltage switch (small gate area - small charge under the gate), the offsets caused by charge injection and clock feedthrough can be further minimized. The dummy switch 15 that is half the size of switch 10 is used to cancel the charge produced by switch 10.

Another improvement is having the value of V_{REF} between V1d and Vss. When the circuit settles in the unity gain configuration, the output of amplifier A_1 would be at V_{REF}. The chosen V_{REF} voltage is dependent on the size of the PMOS and NMOS transistors in switch S_{1a}. If the PMOS and NMOS transistors in switch S_{1a} are the same size, the charge in both the transistors (holes recombining with the electrons) would cancel each other out if:

$$V_{REF}=(V1d + Vss)/2.$$

An example of a circuit implementation of amplifier A_1 is shown in Fig. 14. Amplifier A_1 includes two PMOS transistors 21 and 22 connected in a differential fashion. Transistor 21 has a gate forming the inverting (-) input of amplifier A_1, while the gate of transistor 22 forms the non-inverting (+) input of amplifier A_1. The sources of transistors 21 and 22 are fed from a current sink 20 connected to Vdd. Drains of transistors 21 and 22 are connected through

respective NMOS transistors 24 and 25 to Vss. Note Vss and Vss1 are the same voltage. Transistors 24 and 25 are then connected in a current mirror configuration with respective NMOS transistors 27 and 28. Transistor 27 has a source-drain path connected in series with transistor 30 between V1d and Vss1, while transistor 28 has a source-drain path connected in series with transistor 31 between V1d and Vss1. The connection between the source-drain paths of transistors 28 and 31 form the output of the amplifier A_1.

Although the present invention has been described above with particularity, this was merely to teach one of ordinary skill in the art how to make and use the invention. Many additional modifications will fall within the scope of the invention, as that scope is defined by the claims which follow.

What Is Claimed Is:

1. an analog demultiplexer comprising:

an input amplifier (A_1) having an inverting (-) input, a non-inverting (+) input and an output;

output amplifiers (AMP_1-AMP_N), each having an inverting (-) input, a non-inverting (+) input and an output;

feedback capacitors (C_1-C_N), each feedback capacitor connecting the inverting (-) input of one of the output amplifiers to its output;

a first input capacitor having a first terminal, and having a second terminal connected to the non-inverting (+) input of the input amplifier (A_1);

a second input capacitor having a first terminal, and having a second terminal connected to the inverting (+) input of the input amplifier (A_1);

output feedback switches (S_{2a}, S_{2b}, etc.), each of the output feedback switches selectively connecting an output of one of the output amplifiers (AMP_1-AMP_N) and the first terminal of the first input capacitor (C_{S1});

amplifier connection switches (S_{1a}, S_{1b}, etc.), each of the amplifier connection switches selectively connecting the output of the input amplifier (A_1) and the inverting (-) input of one of the output amplifiers (AMP_1-AMP_N);

an input amplifier feedback switch (S_{50}) selectively connecting the inverting (-) input and output of the input amplifier (A_1);

a reference connection switch (S_{40}) selectively connecting the non-inverting (+) input of the input amplifier (A_1) to a voltage reference supply (V_{REF});

a first input connection switch (S_{30}) for selectively connecting an input of the analog demultiplexer to the first terminal of the first input capacitor (C_{S1}); and

a second input connection switch (S_{35}) for selectively connecting the input of the analog demultiplexer to the first terminal of the second input capacitor (C_{S2}).

2. The analog demultiplexer of claim 1, wherein each of the amplifier connection switches (S_{1a}, S_{1b}, etc.) comprises:

a PMOS transistor having a source-drain path connecting the output of the input amplifier (A_1) to the inverting (-) input of one of the output amplifiers (AMP_1-AMP_N), and having a gate connected to receive a switch control input signal; and

an NMOS transistor having a source-drain path connected in parallel with the PMOS transistor, and having a gate connected to receive an inverse of the switch control input signal.

3. The analog demultiplexer of claim 1, wherein each of the amplifier connection switches (S_{1a}, S_{1b}, etc.) comprises:

a first PMOS transistor having a source-drain path connected on a first end to the output of the input amplifier (A_1), and having a gate connected to receive a switch control input signal;

a second PMOS transistor having a source-drain path connected on a first end to a second end of the source-drain path of the first PMOS transistor, and connected on a second end to the inverting (-) input of one of the output amplifiers (AMP_1-AMP_N), and having a gate connected to receive the switch control input signal;

an first NMOS transistor having a source-drain path connected in parallel with the first PMOS transistor, and having a gate receiving an inverse of the switch control input; and

a second NMOS transistor having a source-drain path connected in parallel with the second PMOS transistor, and having a gate receiving an inverse of the switch control input.

4. The analog demultiplexer of claim 3,

wherein the gate size of the first PMOS transistor is less than about half of the gate size of the second PMOS transistor, and

wherein the gate size of the first NMOS transistor is less than about half of the gate size of the second NMOS transistor.

5. The analog demultiplexer of claim 1, wherein the voltage reference supply (V_{REF}) is connected to the non-inverting (+) input of the output amplifiers (AMP_1-AMP_N).

6. The analog demultiplexer of claim 1, wherein the input amplifier has an output voltage ranging between a high value (Vdd1) and a low value (Vss1), and wherein voltage on the voltage reference supply (V_{REF}) is between the high value (Vdd1) and the low value (Vss1) .

7. The analog demultiplexer of claim 4, wherein the input amplifier has an output voltage ranging between a high value (Vdd1) and a low value (Vss1), and wherein voltages provided as the switch control input ranges between the high value (Vdd1) and the low value (Vss1).

8. The analog demultiplexer of claim 1, wherein corresponding ones of the output feedback switches (S_{2a}, S_{2b}, etc.) close substantially simultaneously with one of the amplifier connection switches (S_{1a}, S_{1b}, etc.), but do not open simultaneously.

9. The analog demultiplexer of claim 1, further comprising a reference switch (S_{1x}) which closes to connect the output of the input amplifier (A_1) to the voltage reference when none of the amplifier connection switches (S_{1a}, S_{1b}, etc.) are closed.

10. The analog demultiplexer of claim 1, wherein the output feedback switches (S_{2a}, S_{2b}, etc.) and the amplifier connection switches (S_{1a}, S_{1b}, etc.) remain open when the input amplifier feedback switch (S_{50}), the reference connection switch (S_{40}), the first input connection switch (S_{30}), and second input connection switch (S_{35}) are closed.

11. The analog demultiplexer of claim 1, the input amplifier feedback switch (S_{50}) and the reference connection switch (S_{40}) open before opening of, the first input connection switch (S_{30}), and second input connection switch (S_{35}).

12. An analog demultiplexer comprising:

an input amplifier (A_1) having a first input, a second input and an output;

output amplifiers (AMP_1-AMP_N), each having a first input, a second input and an output;

feedback capacitors (C_1-C_N), each feedback capacitor connecting the first input of one of the output amplifiers to its output;

a first input capacitor having a first terminal, and having a second terminal connected to the first input of the input amplifier (A_1);

a second input capacitor having a first terminal, and having a second terminal connected to the second input of the input amplifier (A_1);

at least one output feedback switch (S_2) for connecting an output of one of the output amplifiers (AMP_1-AMP_N) and the first terminal of the first input capacitor (C_{S1});

at least one amplifier connection switch (S_1) for selectively connecting the output of the input amplifier (A_1) and the first input of one of the output amplifiers (AMP_1-AMP_N);

a reference connection switch (S_{40}) selectively connecting the first input of the input amplifier (A_1) to a voltage reference (V_{REF}) connection;

a first input connection switch (S_{30}) for selectively connecting an input of the analog demultiplexer to the first terminal of the first input capacitor (C_{S1}); and

a second input connection switch (S_{35}) for selectively connecting the input of the analog demultiplexer to the first terminal of the second input capacitor (C_{S2}).

13. The analog demultiplexer of claim 11 further comprising an input amplifier feedback switch (S_{50}) selectively connecting the second input and output of the input amplifier (A_1);

14. The analog demultiplexer of claim 11, wherein the voltage reference connection (V_{REF}) is connected to the second input of the output amplifiers (AMP_1-AMP_N).

15. A method of demultiplexing an input signal (V_{IN}) using an input amplifier (A_1) and a plurality of output amplifiers (AMP_1-AMP_N), the method comprising the steps of:

connecting switches so that a reference voltage V_{REF} is connected to the inputs and outputs of the input amplifier (A_1);

storing the reference voltage V_{REF} value so that it remains for a period of time on the inputs of the input amplifier (A_1) after the switches applying a voltage reference V_{REF} to the inputs and outputs of the input amplifier (A_1) are open;

opening the switches connecting V_{REF} to the inputs and output of the input amplifier (A_1);

connecting the output of the input amplifier (A_1) to an input of a given one of the output amplifiers (A_1-A_N), a first input of the input amplifier (A_1) receiving the input signal (V_{IN}); and

connecting the output of the given output amplifier to a second input of the input amplifier (A_1).

5

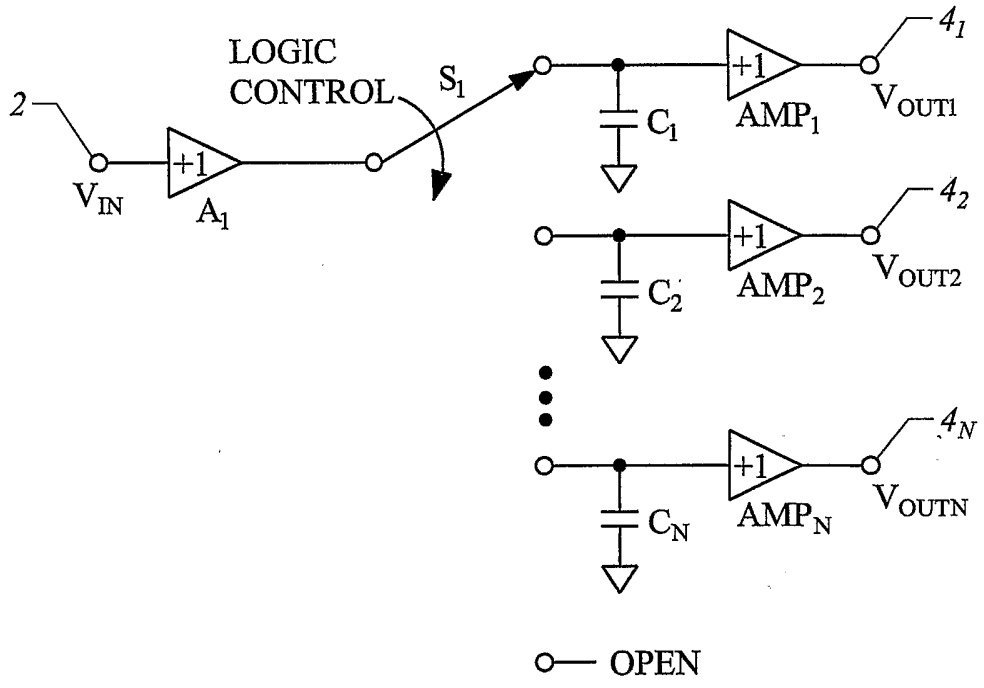

LOGIC
CONTROL
S1
2
+1
VIN
A1
C1
+1
AMP1
41
VOUT1
C2
+1
AMP2
42
VOUT2
CN
+1
AMPN
4N
VOUTN
OPEN

FIG. 1

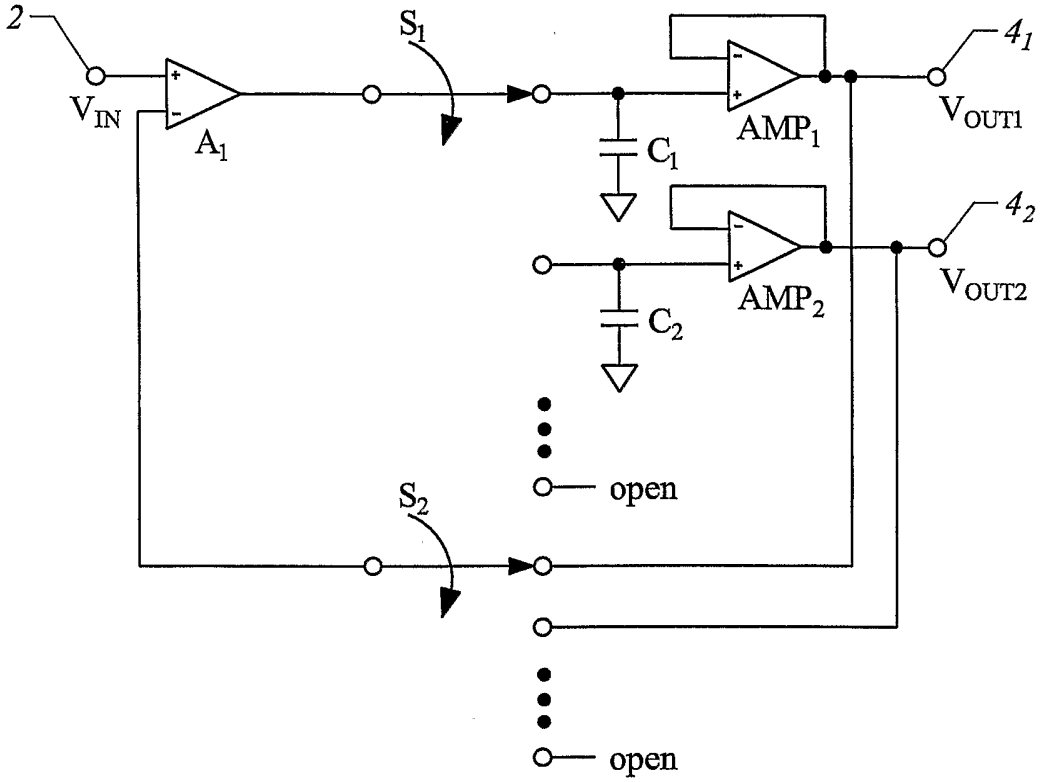

2
V_{IN}
A_1
S_1
C_1
AMP_1
4_1
V_{OUT1}
C_2
AMP_2
4_2
V_{OUT2}
open
S_2
open

FIG. 2

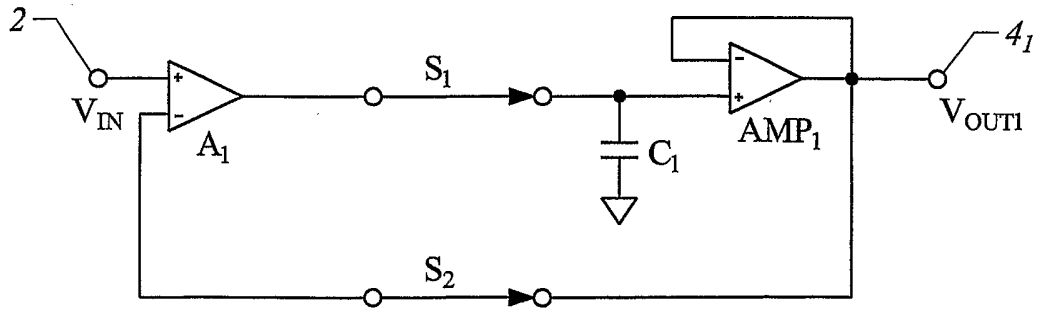

2
V_{IN}
A_1
S_1
C_1
AMP_1
4_1
V_{OUT1}
S_2

FIG. 3

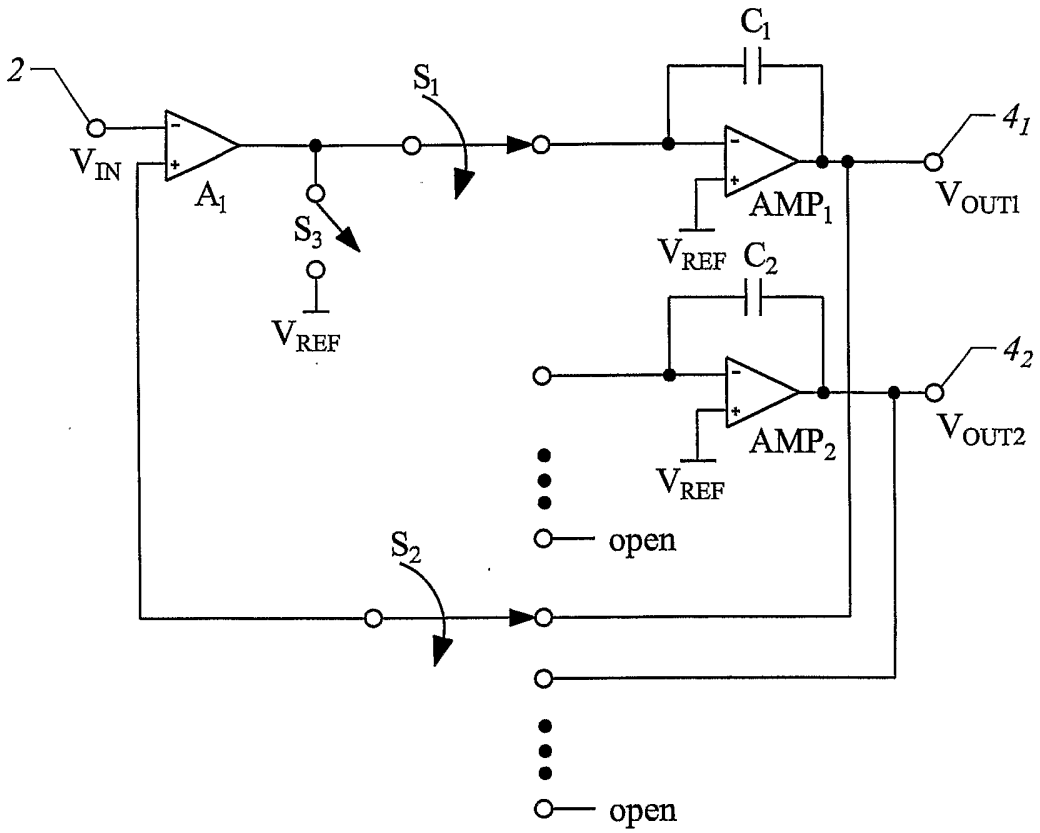

2
V_{IN}
A_1
S_1
S_3
V_{REF}
C_1
AMP_1
V_{REF}
4_1
V_{OUT1}
C_2
AMP_2
V_{REF}
4_2
V_{OUT2}
open
S_2
open

FIG. 4

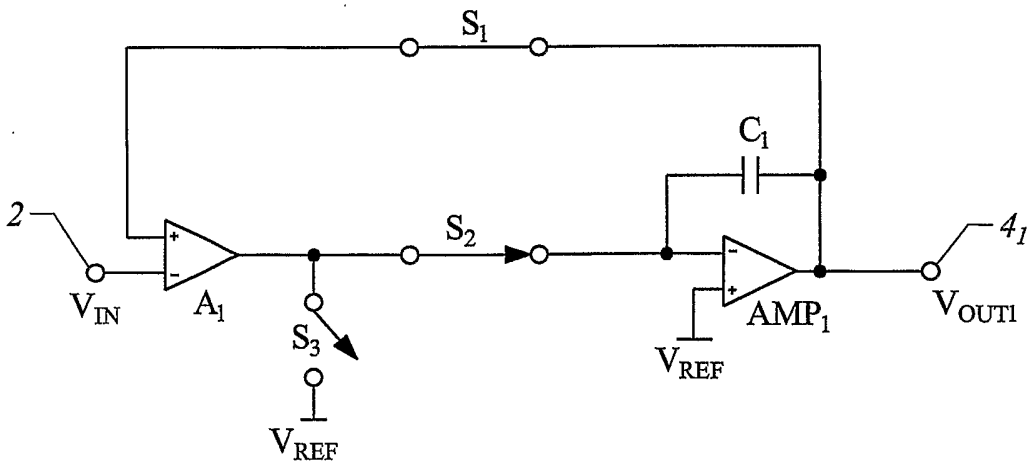

S_1
C_1
2
S_2
4_1
V_{IN}
A_1
S_3
AMP_1
V_{OUT1}
V_{REF}
V_{REF}

FIG. 5

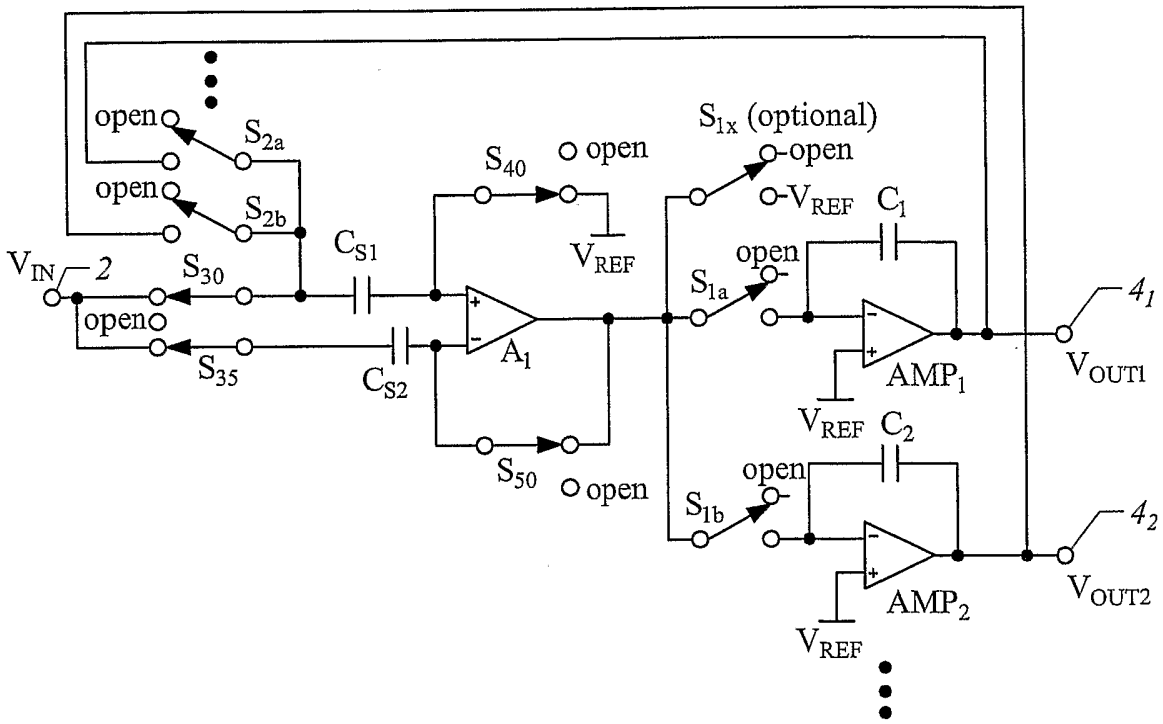

open
S2a
open
S2b
VIN
2
S30
open
S35
CS1
CS2
S40
open
VREF
S50
open
A1
S1x (optional)
open
VREF
C1
open
S1a
AMP1
VREF
VOUT1
41
VREF
C2
open
S1b
AMP2
VREF
VOUT2
42

FIG. 6

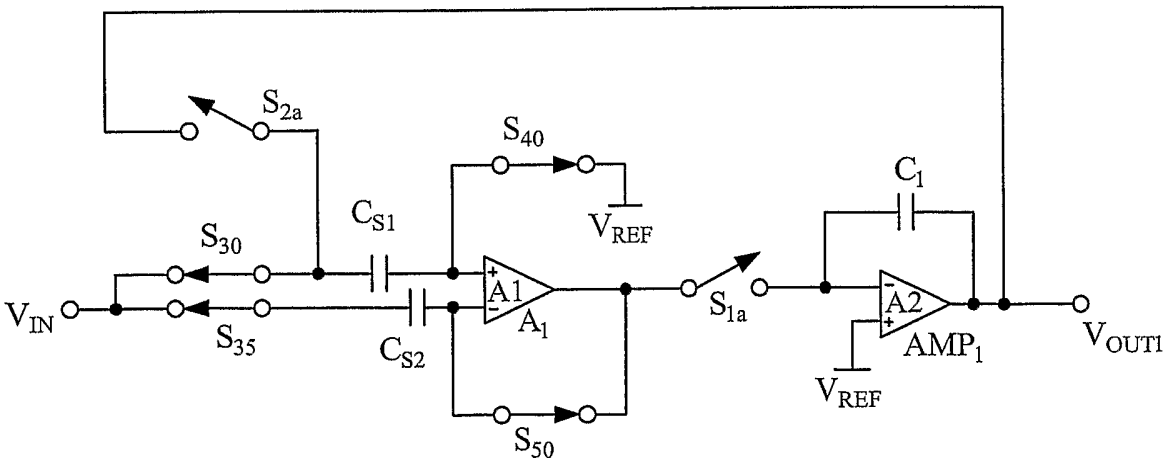

S2a
S40
C1
CS1
VREF
S30
VIN
A1
A1
S1a
A2
AMP1
VOUT1
S35
CS2
VREF
S50

FIG. 7

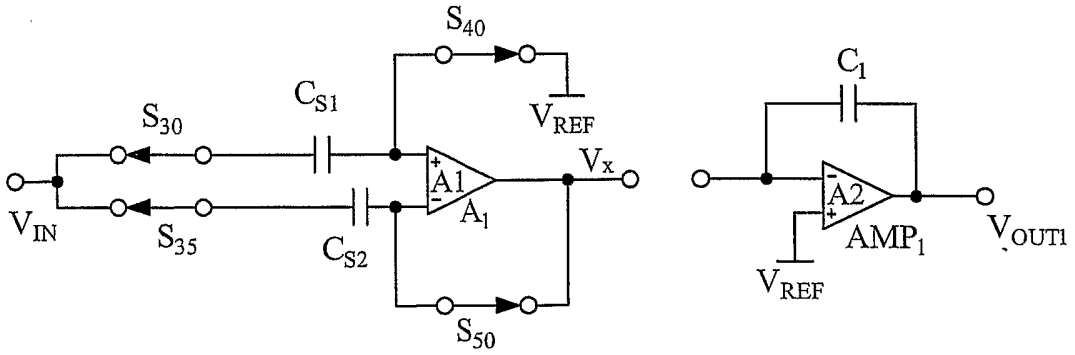


FIG. 8

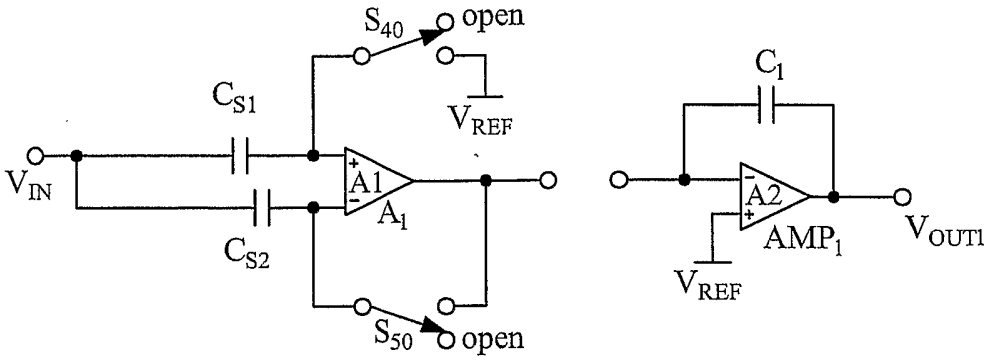


FIG. 9

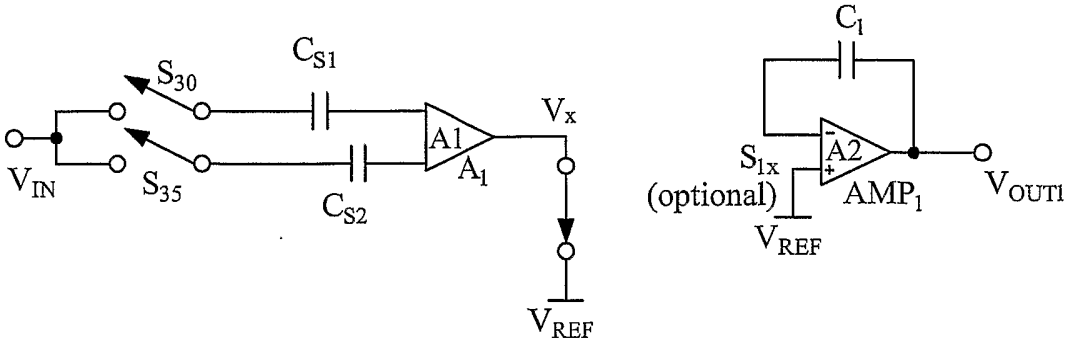


FIG. 10

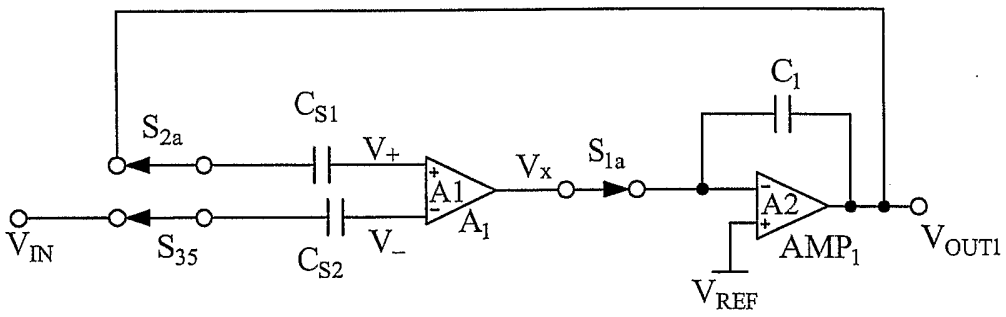

C_1
C_{S1}
S_{2a}
V_+
A1
V_x
S_{1a}
A2
V_{IN}
S_{35}
C_{S2}
V_-
A_1
AMP_1
V_{OUT1}
V_{REF}

FIG. 11

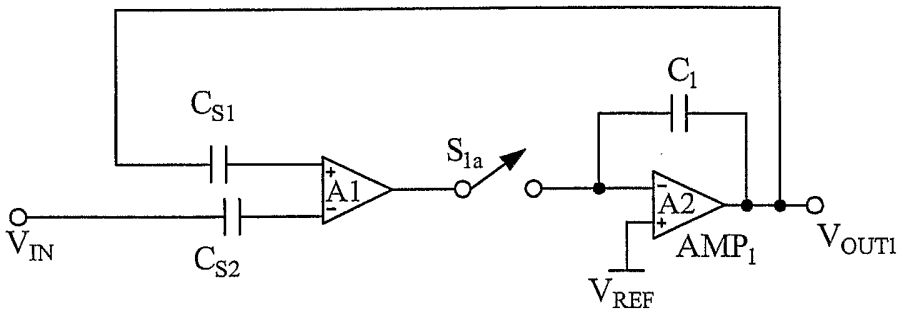

C_1
C_{S1}
S_{1a}
A1
A2
V_{IN}
C_{S2}
AMP_1
V_{OUT1}
V_{REF}

FIG. 12

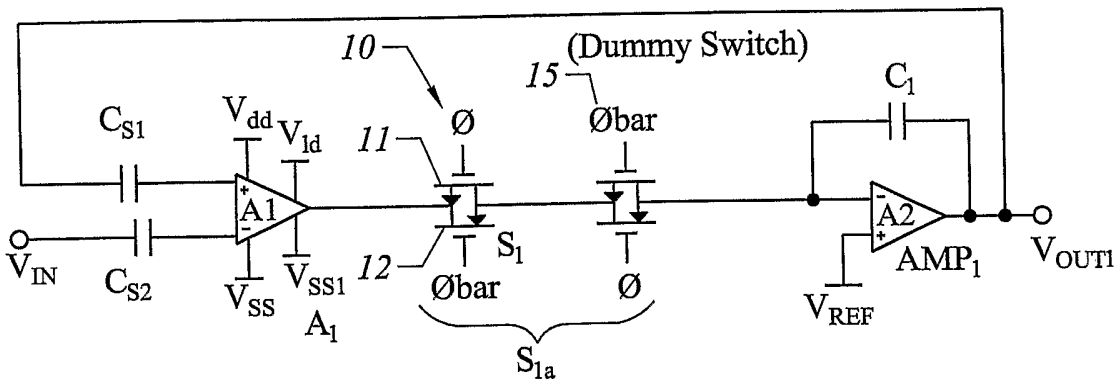

10
(Dummy Switch)
15
C1
Vdd
Vld
11
Ø
Øbar
CS1
A1
A2
VIN
CS2
VSS
VSS1
12
S1
Øbar
Ø
AMP1
VOUT1
VREF
A1
S1a

FIG. 13

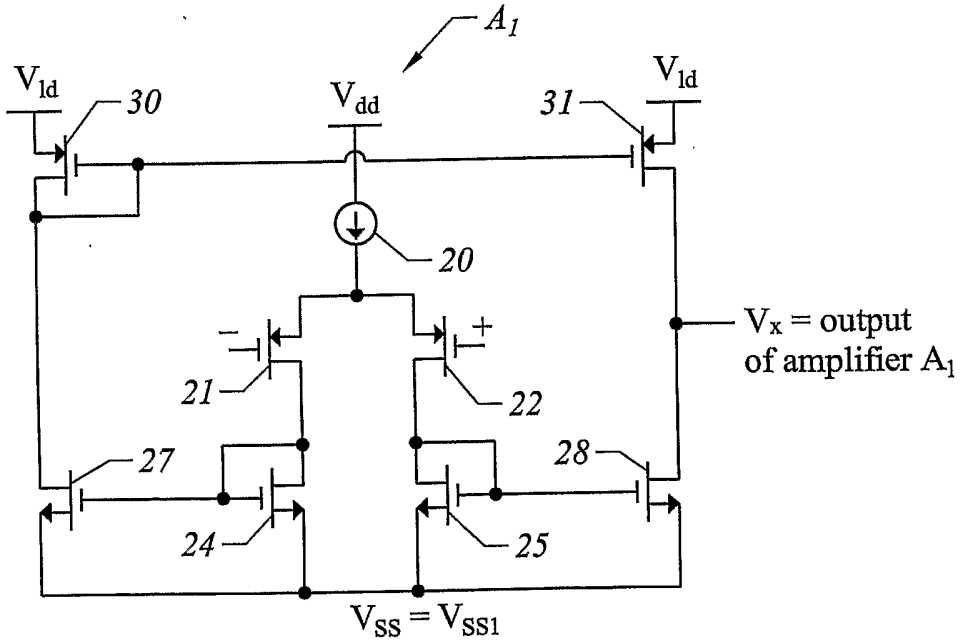

A1
Vld
30
Vdd
31
Vld
20
Vx = output
of amplifier A1
21
22
27
28
24
25
VSS = VSS1

FIG. 14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/28198

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H03K 17/62, 17/693, 17/735, 17/76
US CL : 327/415

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 327/415, 416

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4,860,354 A (VAN ROERMUND) 22 August 1989 (22.08.1989), see entire document.	1-15
A	US 4,455,754 A (BENJAMIN) 26 June 1984 (26.06.1984), see entire document.	1-15
A	US 3,619,511 A (ISHIKAWA) 09 November 1971 (09.11.1971), see entire document.	1-15

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 October 2002 (31.10.2002)	07 FEB 2003
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer Kenneth Wells Telephone No. 703-308-0956

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

PCT/US02/28198

Continuation of B. FIELDS SEARCHED Item 3:
EAST
search terms: demultiplexer, switch, capacitor, amplifier