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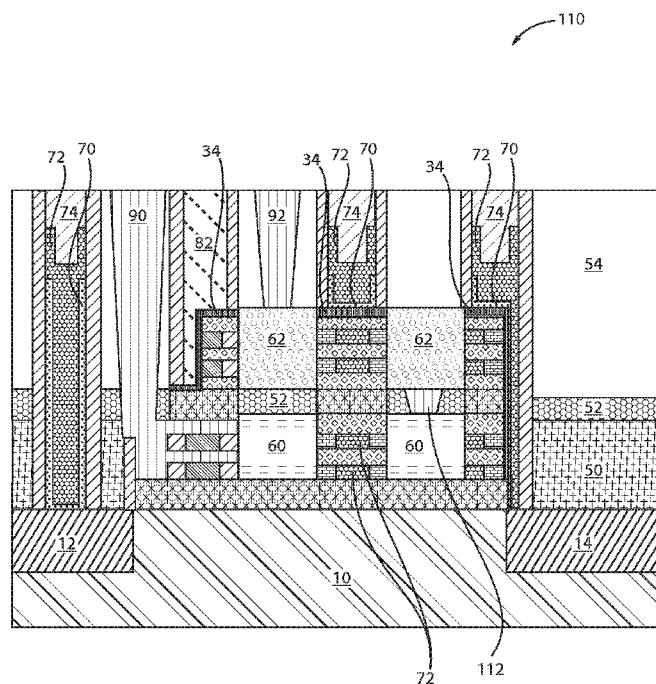


FIG. 9

(57) Abstract: A method is presented for constructing a semiconductor device. The method includes forming a plurality of fins over a nanosheet stack and a substrate, forming spacers (34) between the nanosheet stack and one or more of the plurality of fins, each spacer defining a different shape, forming gate spacers adjacent the plurality of fins, the gate spacers directly contacting the one or more of the plurality of fins having a spacer, forming a barrier spacer between a set of fins of the plurality of fins, the barrier spacer directly contacting a top surface of a shallow trench isolation (STI) region (12), forming n-type epitaxial regions (60) between the plurality of fins, forming p-type epitaxy regions (62) over the n-type epitaxial regions (60), and forming a first contact (90) extending vertically through the semiconductor device adjacent the barrier spacer and extending laterally away from the barrier spacer to directly contact a sidewall of an n-type epitaxial region.

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BOTTOM CONTACT FOR STACKED GAA FET

BACKGROUND

[0001] The present invention relates generally to semiconductor devices, and more specifically, to methods and systems for forming a bottom contact for a stacked gate-all-around (GAA) field effect transistor (FET).

[0002] As the fin width in a finFET approaches 5nm, channel width variations could cause undesirable variability and mobility loss. One promising transistor candidate, gate-all-around FET, could circumvent the problem. Gate-all-around is a device in which a gate is placed on all four sides of the channel. GAA is basically a silicon nanowire with a gate going around it. In some cases, the gate-all-around FET could have indium gallium arsenide (InGaAs) or other III-V materials in the channels.

SUMMARY

[0003] In accordance with an embodiment, a method is provided for constructing a semiconductor device. The method includes forming a plurality of fins over a nanosheet stack and a substrate, forming spacers between the nanosheet stack and one or more of the plurality of fins, each spacer defining a different shape, forming gate spacers adjacent the plurality of fins, the gate spacers directly contacting the one or more of the plurality of fins having a spacer, forming a barrier spacer between a set of fins of the plurality of fins, the barrier spacer directly contacting a top surface of a shallow trench isolation (STI) region, forming n-type epitaxial regions between the plurality of fins, forming p-type epitaxy regions over the n-type epitaxial regions, and forming a first contact extending vertically through the semiconductor device adjacent the barrier spacer and extending laterally away from the barrier spacer to directly contact a sidewall of an n-type epitaxial region of the n-type epitaxial regions.

[0004] In accordance with another embodiment, a method is provided for constructing a stacked gate-all-around field effect transistor (GAA FET). The method includes forming a plurality of fins over a nanosheet stack and a substrate, forming barrier spacers over shallow trench isolation (STI) regions, forming n-type epitaxial regions between the plurality of fins, forming p-type epitaxy regions over the n-type epitaxial regions, and forming a first contact extending vertically through the GAA FET and extending laterally away from the barrier spacers to directly contact a sidewall of an n-type epitaxial region of the n-type epitaxial regions.

[0005] In accordance with yet another embodiment, a stacked gate-all-around field effect transistor (GAA FET) is provided. The GAA FET includes barrier spacers disposed over shallow trench isolation (STI) regions, n-type epitaxial regions formed between the plurality of fins, p-type epitaxy regions formed over the n-type epitaxial regions, and a first contact extending vertically through the GAA FET and extending laterally away from the barrier spacers to directly contact a sidewall of an n-type epitaxial region of the n-type epitaxial regions.

[0006] It should be noted that the exemplary embodiments are described with reference to different subject-matters. In particular, some embodiments are described with reference to method type claims whereas other embodiments have been described with reference to apparatus type claims. However, a person skilled in the art will gather from the above and the following description that, unless otherwise notified, in addition to any combination of features belonging to one type of subject-matter, also any combination between features relating to different subject-matters, in particular, between features of the method type claims, and features of the apparatus type claims, is considered as to be described within this document.

[0007] These and other features and advantages will become apparent from the following detailed description of illustrative embodiments thereof, which is to be read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The invention will provide details in the following description of preferred embodiments with reference to the following figures wherein:

[0009] FIG. 1 is a cross-sectional view of a semiconductor structure including a stacked gate-all-around (GAA) field effect transistor (FET) formed over a substrate, in accordance with an embodiment of the present invention;

[0010] FIG. 2 is a cross-sectional view of the semiconductor structure of FIG. 1 where gate spacers are formed adjacent the fins and inner spacers are formed in the nanosheets, in accordance with an embodiment of the present invention;

[0011] FIG. 3 is a cross-sectional view of the semiconductor structure of FIG. 2 where n-type and p-type epitaxial regions are formed and an epi spacer is formed therebetween, in accordance with an embodiment of the present invention;

[0012] FIG. 4 is a cross-sectional view of the semiconductor structure of FIG. 3 where replacement metal gate (RMG) work function metal (WFM) formation takes place, in accordance with an embodiment of the present invention;

[0013] FIG. 5 is a cross-sectional view of the semiconductor structure of FIG. 4 where a first cut is performed, in accordance with an embodiment of the present invention;

[0014] FIG. 6 is a cross-sectional view of the semiconductor structure of FIG. 5 where a second cut is performed, in accordance with an embodiment of the present invention;

[0015] FIG. 7 is a cross-sectional view of the semiconductor structure of FIG. 6 where a first contact is formed, in accordance with an embodiment of the present invention;

[0016] FIG. 8 is a cross-sectional view of the semiconductor structure of FIG. 7 where a pair of second contacts are formed, in accordance with an embodiment of the present invention; and

[0017] FIG. 9 is a cross-sectional view of the semiconductor structure of FIG. 8 where a buried strap is formed between the n-type and p-type epitaxial regions, in accordance with another embodiment of the present invention.

[0018] Throughout the drawings, same or similar reference numerals represent the same or similar elements.

DETAILED DESCRIPTION

[0019] Embodiments in accordance with the present invention provide methods and devices for forming a bottom contact for a stacked gate-all-around (GAA) field effect transistor (FET).

[0020] Conventional integrated circuits incorporate 2-D planar field effect transistors (FETs) in which current flows through a semiconducting channel between a source and a drain, in response to a voltage applied to a control gate. To provide better control of the current flow, 3D transistors have also been developed. A 3D transistor is an electronic switching device in which the planar semiconducting channel of a traditional FET is replaced by a semiconducting fin that extends outward, normal to the substrate surface. In such a device, the gate, which controls current flow in the fin, wraps around three sides of the fin so as to influence the current flow from three surfaces instead of one. The improved control achieved with a 3D design results in faster switching performance and reduced current leakage, which allows 3D transistors to consume less power so that they can operate at a lower supply voltage.

[0021] More recently, another type of 3D transistor has been developed for technology nodes below 10 nm, referred to as a gate-all-around (GAA) FET, in which the gate surrounds all four sides of the current channel so as to influence the current flow from every direction, and reduce short channel effects (SCE). Instead of providing a fin, in a GAA FET the current channel takes the form of one or more silicon nanowires coupling the source and drain regions.

[0022] The exemplary embodiments of the present invention employ the GAA FET by forming a self-aligned bottom contact utilizing space at the cell boundary of the GAA FET.

[0023] Examples of semiconductor materials that can be used in forming such nanosheet structures include silicon (Si), germanium (Ge), silicon germanium alloys (SiGe), silicon carbide (SiC), silicon germanium carbide (SiGeC), III-V compound semiconductors and/or II-VI compound semiconductors. III-V compound semiconductors are materials that include at least one element from Group III of the Periodic Table of Elements and at least one element from Group V of the Periodic Table of Elements. II-VI compound semiconductors are materials that include at least one element from Group II of the Periodic Table of Elements and at least one element from Group VI of the Periodic Table of Elements.

[0024] It is to be understood that the present invention will be described in terms of a given illustrative architecture; however, other architectures, structures, substrate materials and process features and steps/blocks can be varied within the scope of the present invention. It should be noted that certain features cannot be shown in all figures for the sake of clarity. This is not intended to be interpreted as a limitation of any particular embodiment, or illustration, or scope of the claims.

[0025] FIG. 1 is a cross-sectional view of a semiconductor structure including a stacked gate-all-around (GAA) field effect transistor (FET) formed over a substrate, in accordance with an embodiment of the present invention.

[0026] In various example embodiments, a semiconductor structure 5 includes shallow trench isolation (STI) regions 12, 14 formed within a substrate 10. A nanosheet stack 20 can be formed over the substrate 10 and can include alternating layers of several semiconductor layers.

[0027] In one example, a first semiconductor layer 22 is formed over the substrate 10. The first semiconductor layer 22 can be, e.g., silicon germanium (SiGe) with a high concentration of Ge. In one example, the Ge content can be about 60%. One skilled in the art can contemplate higher concentrations of Ge. This first semiconductor layer 22 can be referred to as a bottom first semiconductor layer 22.

[0028] A first stack of alternating layers of a second semiconductor layer 24 and a third semiconductor layer 26 can then be formed over the first semiconductor layer 22. The second semiconductor layer 24 can be, e.g., silicon germanium (SiGe) and the third semiconductor layer 26 can be, e.g., silicon (Si). The second semiconductor layer 24 can include SiGe with a low concentration of Ge. In one example, the Ge content can be about 30%. One skilled in the art can contemplate lower concentrations of Ge.

[0029] After the first stack of alternating second and third semiconductor layers 24, 26 are formed over the first semiconductor layer 22, another semiconductor layer 22 (top semiconductor layer 22) can be formed over the first stack of alternating second and third semiconductor layers 24, 26. Thus, the alternating second and third semiconductor layers 24, 26 can be formed between two first semiconductor layers 22 (each having a high concentration of Ge, e.g., 60%).

[0030] Subsequently, a second stack of alternating second and third semiconductor layers 24, 26 can be formed over the top first semiconductor layer 22.

[0031] Spacers 34 can then be constructed over the second stack of alternating second and third semiconductor layers 24, 26. In one example, three spacers 34 are shown. The left-hand spacer 34 has a substantially stepped configuration. The central spacer 34 has a substantially flat configuration. The right-hand side spacer 34 has a substantially inverted L-shaped configuration. The first spacer 34 (left-hand side) contacts the second stack of alternating second and third semiconductor layers 24, 26. The second spacer 34 (center) directly contacts a top surface of the second stack of alternating second and third semiconductor layers 24, 26. The third spacer 34 (right-hand side) contacts both the first and second stacks of alternating second and third semiconductor layers 24, 26. The spacer 34 (right-hand side) directly contacts both the top and bottom first semiconductor layers 22.

[0032] A plurality of fins 30 including hardmasks 32 thereon are formed over the nanosheet stack 20 and the STI regions 12.

[0033] Structure 5' is a cross-sectional view along line Y1. Structure 5' illustrates the spacer 34 formed over the first nanosheet stack, as well as the fin 30 with hardmask 32.

[0034] Structure 5'' is a cross-sectional view along line Y2. Structure 5'' illustrates the nanosheet stack 20 including the first stack of alternating second and third semiconductor layers 24, 26 separated from the second stack of alternating second and third semiconductor layers 24, 26 by the top first semiconductor layer 22.

[0035] Top view 7 illustrates the cuts along lines X, Y1 and Y2.

[0036] In one or more embodiments, the substrate 10 can be a semiconductor or an insulator with an active surface semiconductor layer. The substrate 10 can be crystalline, semi-crystalline, microcrystalline, or amorphous. The substrate 10 can be essentially (e.g., except for contaminants) a single element (e.g., silicon), primarily (e.g., with doping) of a single element, for example, silicon (Si) or germanium (Ge), or the substrate 10 can include a compound, for example, Al_2O_3 , SiO_2 , GaAs, SiC, or SiGe. The substrate 10 can also have multiple material layers, for example, a semiconductor-on-insulator substrate (SeOI), a silicon-on-insulator substrate (SOI), germanium-on-insulator substrate (GeOI), or silicon-germanium-on-insulator substrate (SGOI). The substrate 10 can also have other layers forming the substrate 10, including high- k oxides and/or nitrides. In one or more embodiments, the substrate 10 can be a silicon wafer. In an embodiment, the substrate 10 is a single crystal silicon wafer.

[0037] The shallow trench isolation (STI) regions 12 can be formed by etching a trench in doped bottom source/drain (S/D) regions (not shown) utilizing a conventional dry etching process such as reactive ion etching (RIE) or plasma etching. The trenches can optionally be lined with a conventional liner material, e.g., silicon nitride or silicon oxynitride, and then chemical vapor deposition (CVD) or another like deposition process is used to fill the trench with silicon oxide or another like STI dielectric material. The STI dielectric can optionally be densified after deposition. A conventional planarization process such as chemical-mechanical polishing (CMP) can optionally be used to provide a planar structure.

[0038] Referring to, e.g., the nanosheet stack 20, although it is specifically contemplated that the second semiconductor layers 24 can be formed from silicon germanium and that the third semiconductor layers 26 can be formed from silicon, it should be understood that any appropriate materials can be used instead, as long as the two semiconductor materials have etch selectivity with respect to one another. As used herein, the term “selective” in reference to a material removal process denotes that the rate of material removal for a first material is greater than the rate of removal for at least another material of the structure to which the material removal process is being applied. The alternating semiconductor layers 24/26 can be deposited by any appropriate mechanism. It is specifically contemplated that the semiconductor layers 24/26 can be epitaxially grown from one another, but alternate deposition processes, such as chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), or gas cluster ion beam (GCIB) deposition, are also contemplated.

[0039] The fins 30 can be formed from a semiconductor material including, but not limited to Si, strained Si, Si:C, SiGe, SiGe:C, Si alloys, Ge, Ge alloys, GaAs, InAs, InP, as well as other III/V and II/VI compound semiconductors. The fins 30 can be etched by employing, e.g., a reactive ion etch (RIE) or the like.

[0040] The hardmask materials can include any of one or more of SiN, SiCN, SiBN and/or SiBCN, among other materials. The hardmask 32 can be an oxide, for example, a silicon oxide hardmask. The hardmask 32 can be patterned by any suitable patterning techniques, including but not limited to, lithography followed by etching, sidewall image transfer (SIT), self-aligned double patterning (SADP), self-aligned multiple patterning (SAMP), self-aligned quadruple patterning (SAQP), or any suitable combination of those techniques.

[0041] The spacers 34 can include any of one or more of SiN, SiBN, SiCN and/or SiBCN films.

[0042] FIG. 2 is a cross-sectional view of the semiconductor structure of FIG. 1 where gate spacers are formed adjacent the fins and inner spacers are formed in the nanosheets, in accordance with an embodiment of the present invention.

[0043] In various exemplary embodiments, the first and second stacks of nanosheet stack 20 are etched and gate spaces 40 are formed adjacent the plurality of fins 30. Additionally, a single gate spacer 42 (or barrier spacer 42) is formed on the STI region 12. The barrier spacer 42 extends a height of the first stack S1. The barrier spacer 42 extends to a bottom surface of the oxide 46'.

[0044] Moreover, inner spacers 44 are formed in the nanosheet stack 20 after etching.

[0045] The etching can include a dry etching process such as, for example, reactive ion etching, plasma etching, ion etching or laser ablation. The etching can further include a wet chemical etching process in which one or more chemical etchants are used to remove portions of the blanket layers that are not protected by the patterned photoresist.

[0046] The top and bottom first semiconductor layers 22 are replaced with an oxide 46'. The oxide 46' separates the first stack S1 from the second stack S2.

[0047] As a result, a stacked FET 45 is formed having different fin structures 41, 47, 48, 49.

[0048] The Y1 cut illustrates the spacer 34 formed over the oxide 46'.

[0049] The Y2 cut illustrates the barrier spacers 42 on opposed ends of the oxide 46'.

[0050] FIG. 3 is a cross-sectional view of the semiconductor structure of FIG. 2 where n-type and p-type epitaxial regions are formed and an epi spacer is formed therebetween, in accordance with an embodiment of the present invention.

[0051] In various exemplary embodiments, n-type epitaxial regions 60 are formed over the oxide 46'. An epitaxial spacer 52 is then formed over the n-type epitaxial regions 60. P-type epitaxial regions 62 are then formed over the epitaxial spacer 52. The n-type epitaxial regions 60 and the p-type epitaxial regions 62 are formed between the fin structures 47, 48, 49.

[0052] Additionally, a first dielectric 50 is formed over the STI regions 12 and 14. A second dielectric 54 is formed over the epitaxial spacer 52. Thus, the second dielectric 54 is separated from the first dielectric 50 by the epitaxial spacer 52.

[0053] It is noted that the barrier spacer 42 is disposed between a portion of the first dielectric 50 and one of the n-type epitaxial regions 60. The barrier spacer 42 prevents the one n-type epitaxial region 60 from extending onto STI region 12.

[0054] The n-type epitaxial regions 60 directly contact the sidewalls of the first stack S1, whereas the p-type epitaxial regions 62 directly contact the sidewalls of the second stack S2. The epitaxial spacer 52 directly contacts sidewalls of the oxide 46'.

[0055] The Y2 cut clearly illustrates the epitaxial spacer 52 separating the n-type epitaxial regions 60 from the p-type epitaxial regions 62. Moreover, the epitaxial spacer 52 separates the first dielectric 50 from the second dielectric 54. The n-type epitaxial regions 60 extends onto a top surface of the barrier spacer 42.

[0056] FIG. 4 is a cross-sectional view of the semiconductor structure of FIG. 3 where replacement metal gate (RMG) work function metal (WFM) formation takes place, in accordance with an embodiment of the present invention.

[0057] In various exemplary embodiments, the fins 30 and the hardmask 32 are removed and replaced with a WFM. Each fin structure 41', 47', 48', 49' includes a different configuration.

[0058] The gate spacers 40 are thus filled with an inter-layer dielectric (ILD) 70, a high-k material 72, and a WFM 74.

[0059] Fin structure 41' extends to a top surface of the STI region 12. The ILD 70 directly contacts the top surface of the STI region 12. The ILD 70 defines a substantially elongated U-shaped configuration. The high-k material 72 is formed within the ILD 70. At a top portion of the fin structure 41', the high-k material 72 directly contacts inner sidewalls of the gate spacer 40. The WFM 74 directly contacts inner sidewalls of the gate spacer 40 and extends into a U-shaped area defined at the top of the high-k material 72.

[0060] Fin structure 47' extends over the nanosheet stack. Fin structure 47' includes a spacer 34 (inverted Z-shaped configuration). The spacer 34 separates the ILD 70 from the stack S2. The fin structure thus defines a stepped configuration.

[0061] Fin structure 48' extends over the nanosheet stack. Fin structure 48' includes a spacer 34 that is substantially flat. As a result, the ILD 70 has a substantially U-shaped configuration for accommodating the high-k material 72. At a top portion of the fin structure 48', the high-k material 72 directly contacts inner sidewalls of the gate spacer 40. The WFM 74 directly contacts inner sidewalls of the gate spacer 40 and extends into a U-shaped area defined at the top of the high-k material 72.

[0062] Fin structure 49' extends over the nanosheet stack. Fin structure 49' includes a spacer 34 that defines an inverted L-shape. The spacer 34 extends an entire length of the nanosheet stack. As a result, the ILD 70 and the high-k material encompassed within the ILD 70 both extend a length of the nanosheet stack. The ILD 70 directly contacts a top surface of the STI region 14.

[0063] In some examples, the selective wet etch or the selective dry etch can selectively remove the portions of second semiconductor layer 24 (e.g., the SiGe layer) and leave the entirety or portions of the third semiconductor layer 26. The removal creates gaps or openings or indentations between the third semiconductor layers 26 of the FET device. These openings are filled with the high-k material 72.

[0064] The dry and wet etching processes can have etching parameters that can be tuned, such as etchants used, etching temperature, etching solution concentration, etching pressure, source power, RF bias voltage, RF bias power, etchant flow rate, and other suitable parameters. Dry etching processes can include a biased plasma etching process that uses a chlorine-based chemistry. Other dry etchant gasses can include Tetrafluoromethane (CF₄), nitrogen trifluoride (NF₃), sulfur hexafluoride (SF₆), and helium (He), and Chlorine trifluoride (ClF₃). Dry etching can also be performed anisotropically using such mechanisms as DRIE (deep reactive-ion etching). Chemical vapor etching can be used as a selective etching method, and the etching gas can include hydrogen chloride (HCl), Tetrafluoromethane (CF₄), and gas mixture with hydrogen (H₂). Chemical vapor etching can be performed by CVD with suitable pressure and temperature.

[0065] The ILD 70 can be any suitable material, such as, for example, porous silicates, carbon doped oxides, silicon dioxides, silicon nitrides, silicon oxynitrides, or other dielectric materials. Any known manner of forming the ILD 70 can be utilized. The ILD 70 can be

formed using, for example, CVD, PECVD, ALD, flowable CVD, spin-on dielectrics, or PVD.

[0066] In various embodiments, the high-k material 72 can include but is not limited to work function metals such as titanium nitride, titanium carbide, titanium aluminum carbide, tantalum nitride and tantalum carbide; conducting metals such as tungsten, aluminum and copper; and oxides such as silicon dioxide (SiO_2), hafnium oxide (e.g., HfO_2), hafnium silicon oxide (e.g., HfSiO_4), hafnium silicon oxynitride ($\text{Hf}_w\text{Si}_x\text{O}_y\text{N}_z$), lanthanum oxide (e.g., La_2O_3), lanthanum aluminum oxide (e.g., LaAlO_3), zirconium oxide (e.g., ZrO_2), zirconium silicon oxide (e.g., ZrSiO_4), zirconium silicon oxynitride ($\text{Zr}_w\text{Si}_x\text{O}_y\text{N}_z$), tantalum oxide (e.g., TaO_2 , Ta_2O_5), titanium oxide (e.g., TiO_2), barium strontium titanium oxide (e.g., BaTiO_3 — SrTiO_3), barium titanium oxide (e.g., BaTiO_3), strontium titanium oxide (e.g., SrTiO_3), yttrium oxide (e.g., Y_2O_3), aluminum oxide (e.g., Al_2O_3), lead scandium tantalum oxide ($\text{Pb}(\text{Sc}_x\text{Ta}_{1-x})\text{O}_3$), and lead zinc niobate (e.g., $\text{PbZn}_{1/3}\text{Nb}_{2/3}\text{O}_3$).

[0067] The WFM 74 or conductive material 74, can be, e.g., tungsten (W).

[0068] FIG. 5 is a cross-sectional view of the semiconductor structure of FIG. 4 where a first cut is performed, in accordance with an embodiment of the present invention.

[0069] In various exemplary embodiments, a first cut 80 is performed. This is clearly illustrated along line Y1.

[0070] FIG. 6 is a cross-sectional view of the semiconductor structure of FIG. 5 where a second cut is performed, in accordance with an embodiment of the present invention.

[0071] In various exemplary embodiments, a second cut 82 is performed. This is illustrated in the X direction and in the Y1 direction. In the Y1 direction, the second cut 82 encompasses the entire spacer 34. In the X direction, the second cut 82 removes the ILD 70, the high-material 72, and the WFM 74 from where the fin structure 47' was positioned.

[0072] FIG. 7 is a cross-sectional view of the semiconductor structure of FIG. 6 where a first contact is formed, in accordance with an embodiment of the present invention.

[0073] In various exemplary embodiments, a first contact 90 is formed. The first contact 90 is positioned between the fin structure 41' and the second cut 82. The first contact 90 extends laterally underneath the cut 82. The first contact 90 can be referred to as the bottom contact.

[0074] FIG. 8 is a cross-sectional view of the semiconductor structure of FIG. 7 where a pair of second contacts are formed, in accordance with an embodiment of the present invention.

[0075] In various exemplary embodiments, a pair of second contacts 92 are formed. One of the second contacts 92 extends to a top surface of a p-type epitaxial region 62 and a different

second contact 92 extends into a different p-type epitaxial region 62, such that it contacts the n-type epitaxial region 60. This occurs between fin structures 48', 49'.

[0076] Structure 100 illustrates the X direction cut, structure 100' illustrates the Y1 direction cut, and structure 100'' illustrates the Y2 direction cut.

[0077] FIG. 9 is a cross-sectional view of the semiconductor structure of FIG. 8 where a buried strap is formed between the n-type and p-type epitaxial regions, in accordance with another embodiment of the present invention.

[0078] In an alternative exemplary embodiment, a buried strap 112 can be formed directly between the n-type epitaxial region 60 and the p-type epitaxial region 62.

[0079] In conclusion, a self-aligned to gate, bottom contact is formed by utilizing space at the cell boundary on a stacked GAA FET. The semiconductor device includes a stacked gate all around FET standard cell with contact to bottom FET formed past dummy gate at the edge of the cell, a step sheet structure across the gate plane, partial extension of the bottom sheet past the end gate (no tuck thereunder), contact to the bottom gate through sacrificial epi/sheet under the dummy gate, and self-aligned dummy gate isolation of the top sheet from the bottom contact. The method includes a stepped RX structure in through PC plane with tuck under the top sheet, bottom sheet extending past PC, formation of N/P epi as POR with partial unmerged p-epi in bottom RX region extending past the PC, cut of cell end non-active gate with special CT (post sheet release and RMG) and fill with SiN, bottom contact etch landing on unmerged epi, removal of unmerged epi, and isotropic etch of unmerged epi and Si sheets under cell edge gate.

[0080] Regarding FIGS. 1-9, deposition is any process that grows, coats, or otherwise transfers a material onto the wafer. Available technologies include, but are not limited to, thermal oxidation, physical vapor deposition (PVD), chemical vapor deposition (CVD), electrochemical deposition (ECD), molecular beam epitaxy (MBE) and more recently, atomic layer deposition (ALD) among others. As used herein, "depositing" can include any now known or later developed techniques appropriate for the material to be deposited including but not limited to, for example: chemical vapor deposition (CVD), low-pressure CVD (LPCVD), plasma-enhanced CVD (PECVD), semi-atmosphere CVD (SACVD) and high density plasma CVD (HDPCVD), rapid thermal CVD (RTCVD), ultra-high vacuum CVD (UHVCVD), limited reaction processing CVD (LRPCVD), metal-organic CVD (MOCVD), sputtering deposition, ion beam deposition, electron beam deposition, laser assisted deposition, thermal oxidation, thermal nitridation, spin-on methods, physical vapor

deposition (PVD), atomic layer deposition (ALD), chemical oxidation, molecular beam epitaxy (MBE), plating, evaporation.

[0081] Reference throughout the specification to conventional etching techniques known in the art of semiconductor fabrication for selective removal of polysilicon, silicon nitride, silicon dioxide, metals, photoresist, polyimide, or similar materials includes such processes as wet chemical etching, reactive ion (plasma) etching (RIE), washing, wet cleaning, pre-cleaning, spray cleaning, chemical-mechanical planarization (CMP) and the like. Specific embodiments are described herein with reference to examples of such processes. However, the present disclosure and the reference to certain deposition techniques should not be limited to those described. In some instances, two such techniques may be interchangeable. For example, stripping photoresist may entail immersing a sample in a wet chemical bath or, alternatively, spraying wet chemicals directly onto the sample.

[0082] The term “processing” as used herein includes deposition of material or photoresist, patterning, exposure, development, etching, cleaning, stripping, implanting, doping, stressing, layering, and/or removal of the material or photoresist as needed in forming a described structure.

[0083] It is to be understood that the present invention will be described in terms of a given illustrative architecture; however, other architectures, structures, substrate materials and process features and steps/blocks can be varied within the scope of the present invention.

[0084] It will also be understood that when an element such as a layer, region or substrate is referred to as being “on” or “over” another element, it can be directly on the other element or intervening elements can also be present. In contrast, when an element is referred to as being “directly on” or “directly over” another element, there are no intervening elements present. It will also be understood that when an element is referred to as being “connected” or “coupled” to another element, it can be directly connected or coupled to the other element or intervening elements can be present. In contrast, when an element is referred to as being “directly connected” or “directly coupled” to another element, there are no intervening elements present.

[0085] The present embodiments can include a design for an integrated circuit chip, which can be created in a graphical computer programming language, and stored in a computer storage medium (such as a disk, tape, physical hard drive, or virtual hard drive such as in a storage access network). If the designer does not fabricate chips or the photolithographic masks used to fabricate chips, the designer can transmit the resulting design by physical mechanisms (e.g., by providing a copy of the storage medium storing the design) or

electronically (e.g., through the Internet) to such entities, directly or indirectly. The stored design is then converted into the appropriate format (e.g., GDSII) for the fabrication of photolithographic masks, which usually include multiple copies of the chip design in question that are to be formed on a wafer. The photolithographic masks are utilized to define areas of the wafer (and/or the layers thereon) to be etched or otherwise processed.

[0086] Methods as described herein can be used in the fabrication of integrated circuit chips. The resulting integrated circuit chips can be distributed by the fabricator in raw wafer form (that is, as a single wafer that has multiple unpackaged chips), as a bare die, or in a packaged form. In the latter case, the chip is mounted in a single chip package (such as a plastic carrier, with leads that are affixed to a motherboard or other higher level carrier) or in a multichip package (such as a ceramic carrier that has either or both surface interconnections or buried interconnections). In any case, the chip is then integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes integrated circuit chips, ranging from toys and other low-end applications to advanced computer products having a display, a keyboard or other input device, and a central processor.

[0087] It should also be understood that material compounds will be described in terms of listed elements, e.g., SiGe. These compounds include different proportions of the elements within the compound, e.g., SiGe includes $\text{Si}_x\text{Ge}_{1-x}$ where x is less than or equal to 1, etc. In addition, other elements can be included in the compound and still function in accordance with the present embodiments. The compounds with additional elements will be referred to herein as alloys.

[0088] Reference in the specification to “one embodiment” or “an embodiment” of the present invention, as well as other variations thereof, means that a particular feature, structure, characteristic, and so forth described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearances of the phrase “in one embodiment” or “in an embodiment”, as well any other variations, appearing in various places throughout the specification are not necessarily all referring to the same embodiment.

[0089] It is to be appreciated that the use of any of the following “/”, “and/or”, and “at least one of”, for example, in the cases of “A/B”, “A and/or B” and “at least one of A and B”, is intended to encompass the selection of the first listed option (A) only, or the selection of the second listed option (B) only, or the selection of both options (A and B). As a further

example, in the cases of “A, B, and/or C” and “at least one of A, B, and C”, such phrasing is intended to encompass the selection of the first listed option (A) only, or the selection of the second listed option (B) only, or the selection of the third listed option (C) only, or the selection of the first and the second listed options (A and B) only, or the selection of the first and third listed options (A and C) only, or the selection of the second and third listed options (B and C) only, or the selection of all three options (A and B and C). This can be extended, as readily apparent by one of ordinary skill in this and related arts, for as many items listed.

[0090] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of example embodiments. As used herein, the singular forms “a,” “an” and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms “comprises,” “comprising,” “includes” and/or “including,” when used herein, specify the presence of stated features, integers, steps, operations, elements and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components and/or groups thereof.

[0091] Spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper,” and the like, can be used herein for ease of description to describe one element's or feature's relationship to another element(s) or feature(s) as illustrated in the FIGS. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the FIGS. For example, if the device in the FIGS. is turned over, elements described as “below” or “beneath” other elements or features would then be oriented “above” the other elements or features. Thus, the term “below” can encompass both an orientation of above and below. The device can be otherwise oriented (rotated 90 degrees or at other orientations), and the spatially relative descriptors used herein can be interpreted accordingly. In addition, it will also be understood that when a layer is referred to as being “between” two layers, it can be the only layer between the two layers, or one or more intervening layers can also be present.

[0092] It will be understood that, although the terms first, second, etc. can be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another element. Thus, a first element discussed below could be termed a second element without departing from the scope of the present concept.

[0093] Having described preferred embodiments of a method for forming a bottom contact for a stacked gate-all-around (GAA) field effect transistor (FET) (which are intended to be

illustrative and not limiting), it is noted that modifications and variations can be made by persons skilled in the art in light of the above teachings. It is therefore to be understood that changes may be made in the particular embodiments described which are within the scope of the invention as outlined by the appended claims. Having thus described aspects of the invention, with the details and particularity required by the patent laws, what is claimed and desired protected by Letters Patent is set forth in the appended claims.

CLAIMS

1. A method for constructing a semiconductor device, the method comprising:
forming a plurality of fins over a nanosheet stack and a substrate;
forming spacers between the nanosheet stack and one or more of the plurality of fins, each spacer defining a different shape;
forming gate spacers adjacent the plurality of fins, the gate spacers directly contacting the one or more of the plurality of fins having a spacer;
forming a barrier spacer between a set of fins of the plurality of fins, the barrier spacer directly contacting a top surface of a shallow trench isolation (STI) region;
forming n-type epitaxial regions between the plurality of fins;
forming p-type epitaxy regions over the n-type epitaxial regions; and
forming a first contact extending vertically through the semiconductor device adjacent the barrier spacer and extending laterally away from the barrier spacer to directly contact a sidewall of an n-type epitaxial region of the n-type epitaxial regions.
2. The method of claim 1, wherein each of the plurality of fins formed over the nanosheet stack has a different shape.
3. The method of claim 1, wherein an epitaxial spacer separates the n-type epitaxial regions from the p-type epitaxy regions.
4. The method of claim 1, further comprising replacing the plurality of fins with work function metal (WFM) after formation of the p-type epitaxy regions.
5. The method of claim 1, wherein a first spacer of the spacers formed between the nanosheet stack and one or more of the plurality of fins defines a substantially stepped configuration.
6. The method of claim 1, wherein a second spacer of the spacers formed between the nanosheet stack and one or more of the plurality of fins is substantially flat.
7. The method of claim 1, wherein a third spacer of the spacers formed between the nanosheet stack and one or more of the plurality of fins defines a substantially inverted L-shaped configuration.

8. The method of claim 1, wherein a second contact is formed to a top surface of a p-type epitaxial region of the p-type epitaxial regions.

9. The method of claim 1, wherein a third contact is formed through a p-type epitaxial region of the p-type epitaxial regions to a top surface of a respective n-type epitaxial region of the n-type epitaxial regions.

10. A method for constructing a stacked gate-all-around field effect transistor (GAA FET), the method comprising:

forming a plurality of fins over a nanosheet stack and a substrate;
forming barrier spacers over shallow trench isolation (STI) regions;
forming n-type epitaxial regions between the plurality of fins;
forming p-type epitaxy regions over the n-type epitaxial regions; and
forming a first contact extending vertically through the GAA FET and extending laterally away from the barrier spacers to directly contact a sidewall of an n-type epitaxial region of the n-type epitaxial regions.

11. The method of claim 10, further comprising forming spacers between the nanosheet stack and one or more of the plurality of fins

12. The method of claim 11, wherein each spacer defines a different shape.

13. The method of claim 11, wherein a first spacer of the spacers formed between the nanosheet stack and one or more of the plurality of fins defines a substantially stepped configuration.

14. The method of claim 11, wherein a second spacer of the spacers formed between the nanosheet stack and one or more of the plurality of fins is substantially flat.

15. The method of claim 11, wherein a third spacer of the spacers formed between the nanosheet stack and one or more of the plurality of fins defines a substantially inverted L-shaped configuration.

16. The method of claim 10, wherein an epitaxial spacer separates the n-type epitaxial regions from the p-type epitaxy regions.

17. The method of claim 10, further comprising replacing the plurality of fins with work function metal (WFM) after formation of the p-type epitaxy regions.

18. The method of claim 10,
wherein a second contact is formed to a top surface of a first p-type epitaxial region of the p-type epitaxial regions; and
wherein a third contact is formed through a second p-type epitaxial region of the p-type epitaxial regions to a top surface of a respective n-type epitaxial region of the n-type epitaxial regions.

19. A stacked gate-all-around field effect transistor (GAA FET) comprising:
barrier spacers disposed over shallow trench isolation (STI) regions;
n-type epitaxial regions formed between the plurality of fins;
p-type epitaxy regions formed over the n-type epitaxial regions; and
a first contact extending vertically through the GAA FET and extending laterally away from the barrier spacers to directly contact a sidewall of an n-type epitaxial region of the n-type epitaxial regions.

20. The stacked GAA FET of claim 19, wherein spacers are disposed between the nanosheet stack and one or more of the plurality of fins, each spacer defining a different shape.

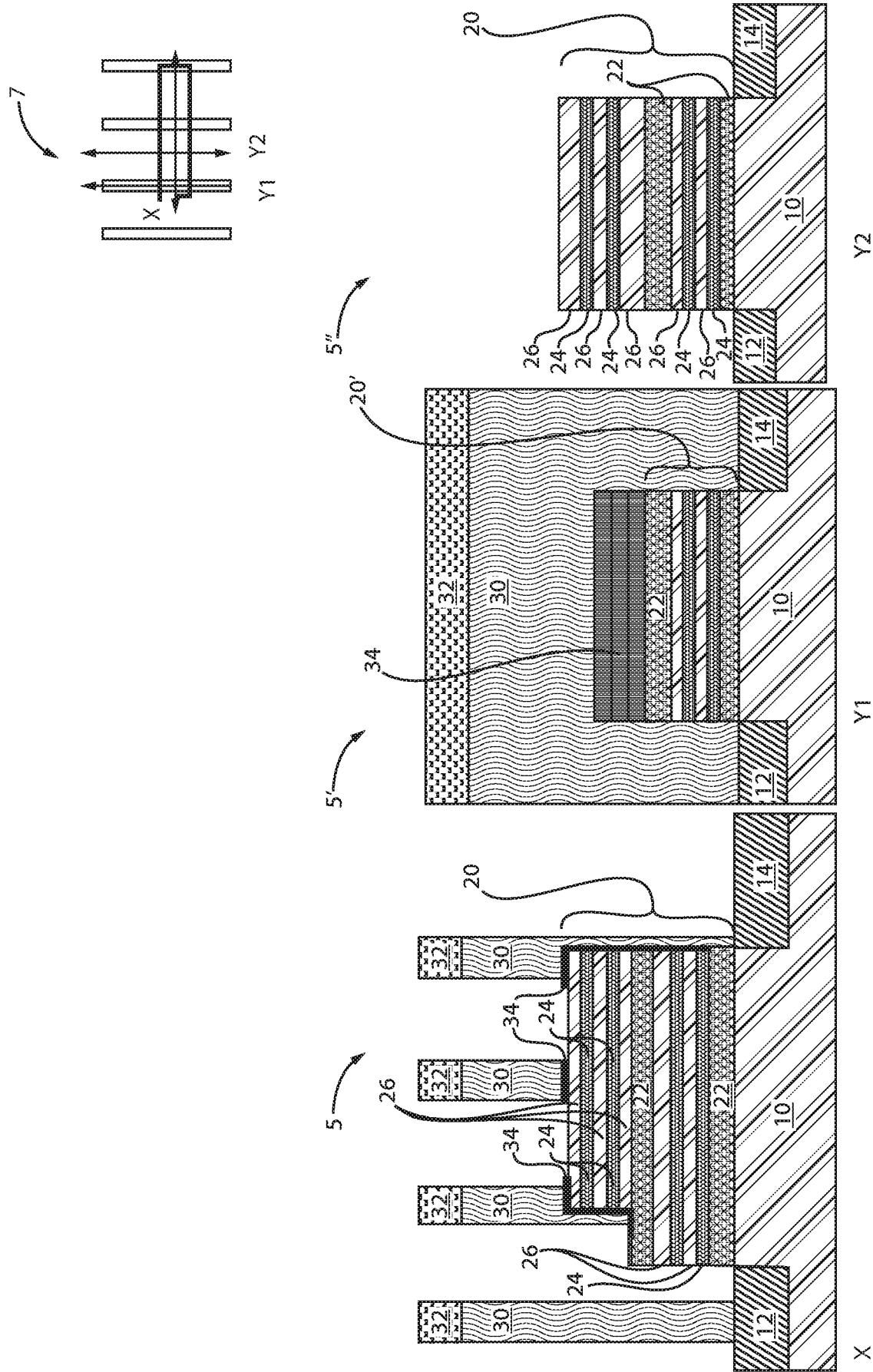
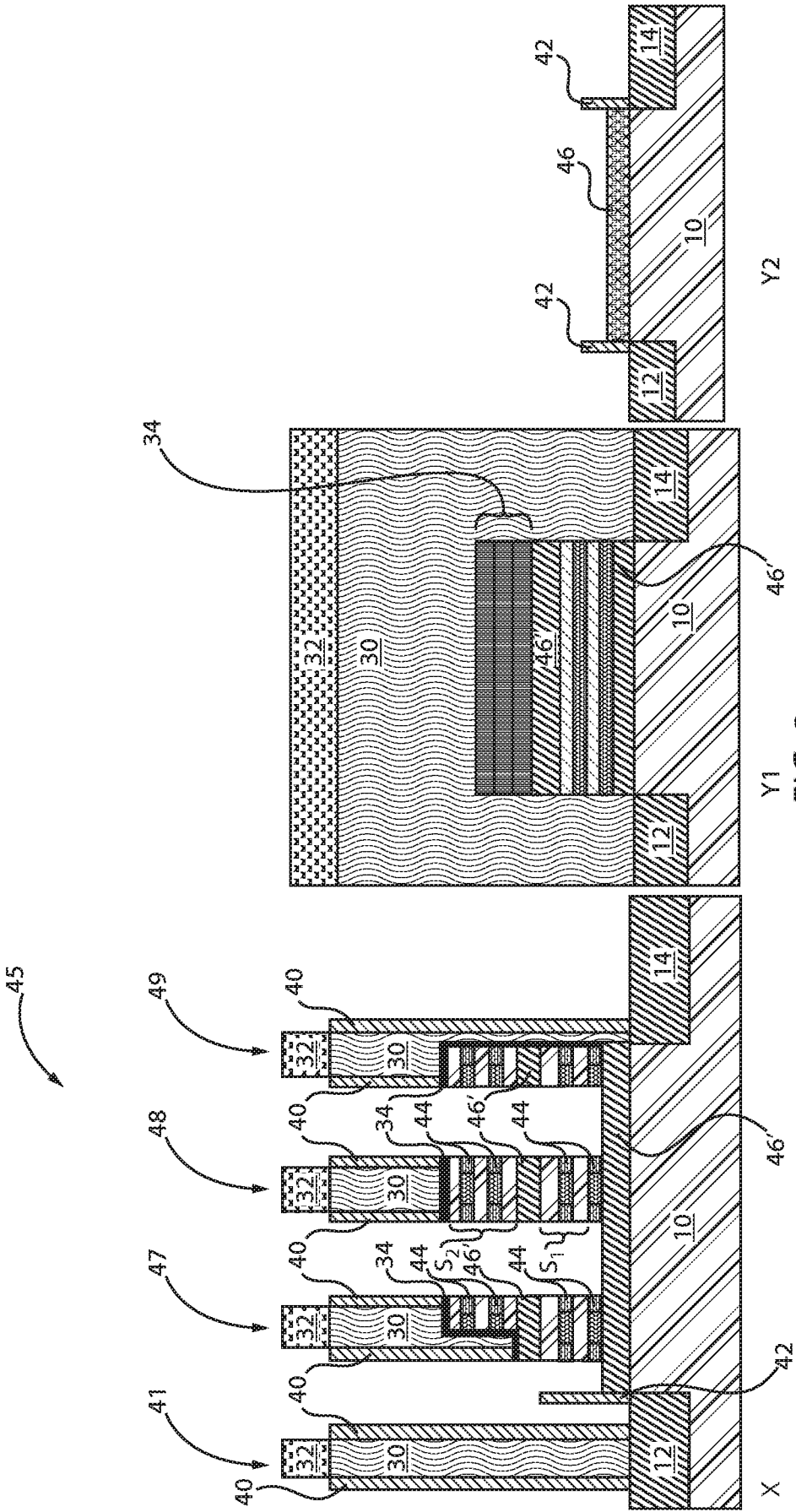


FIG. 1



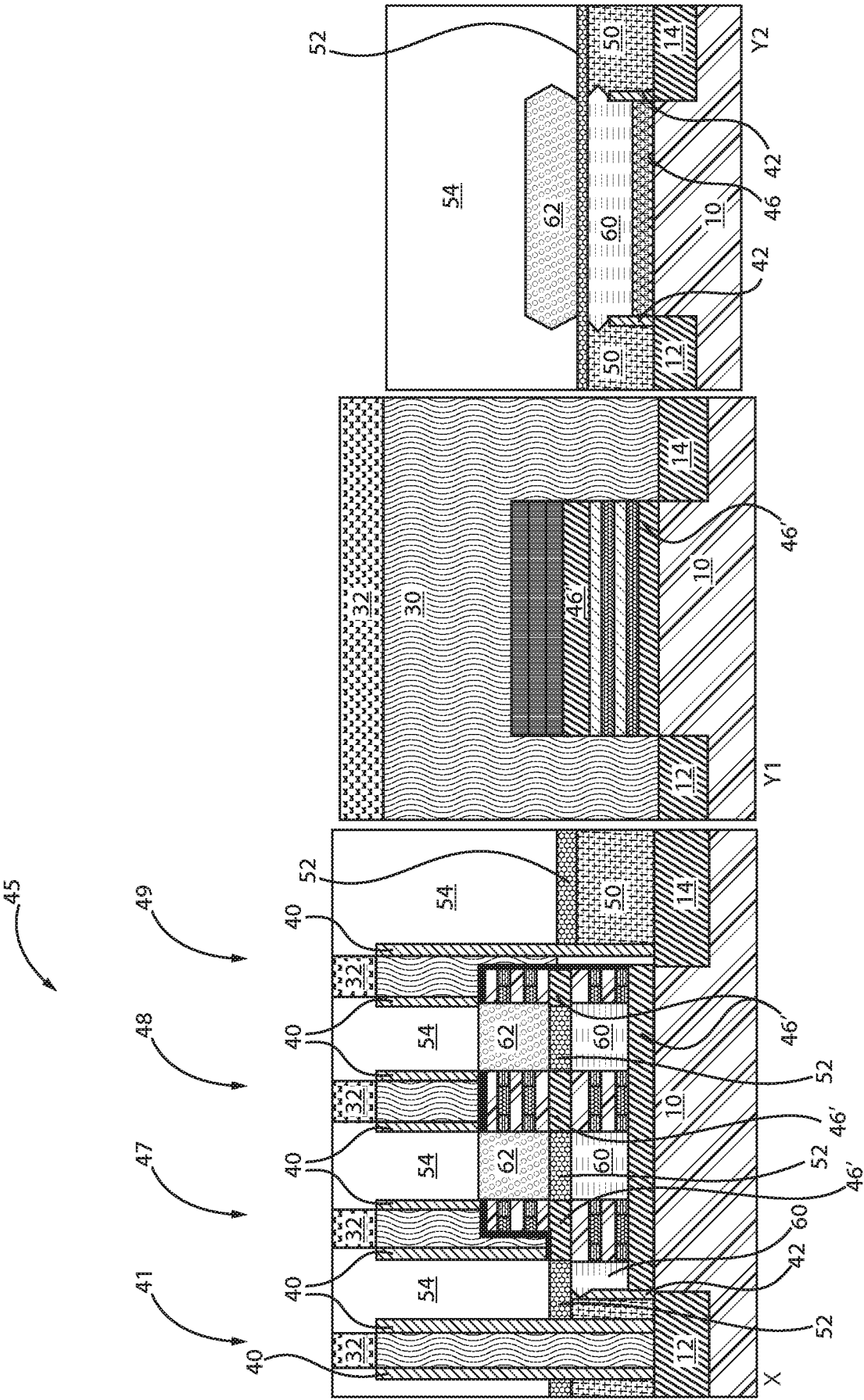


FIG. 3

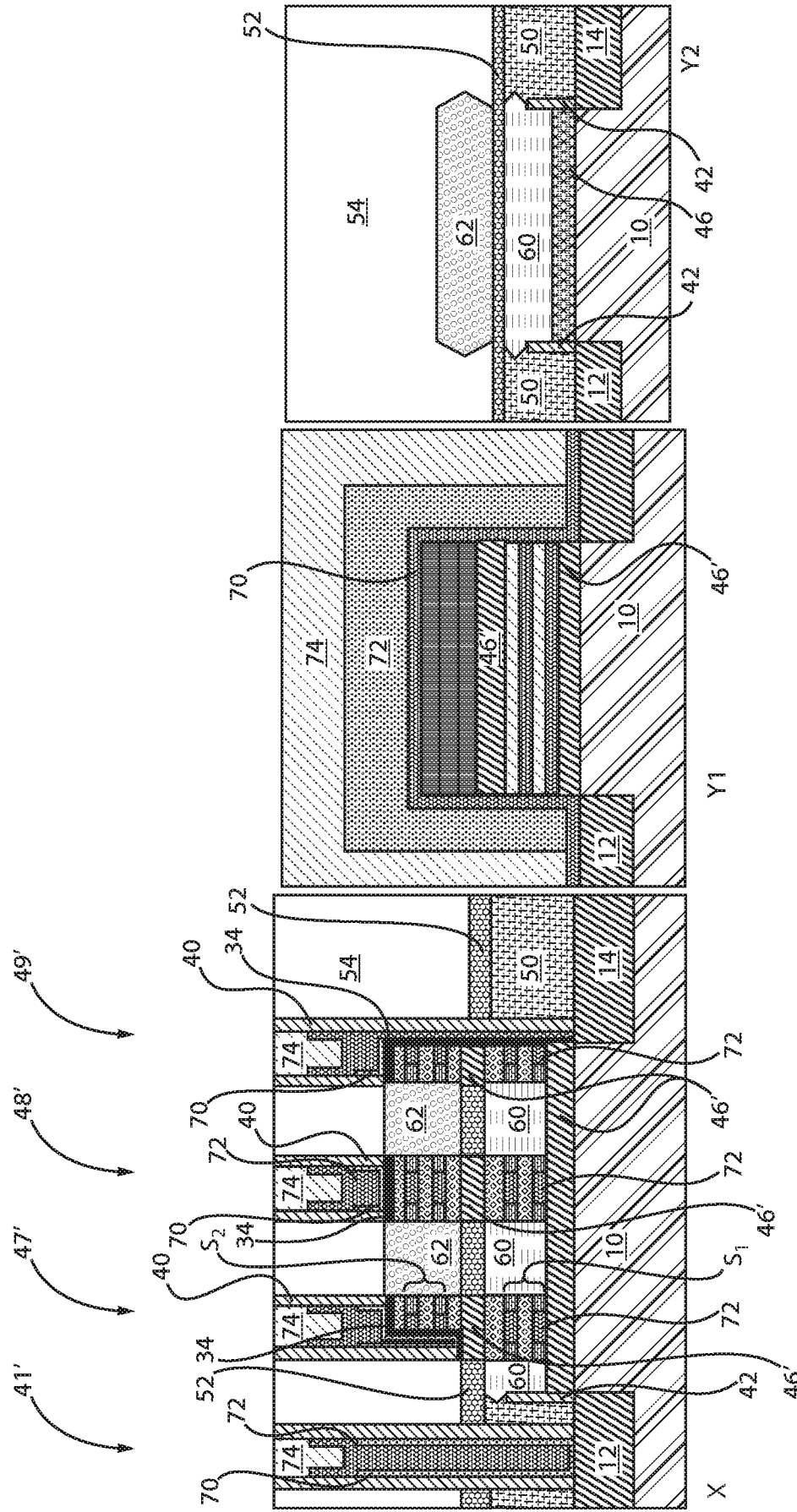
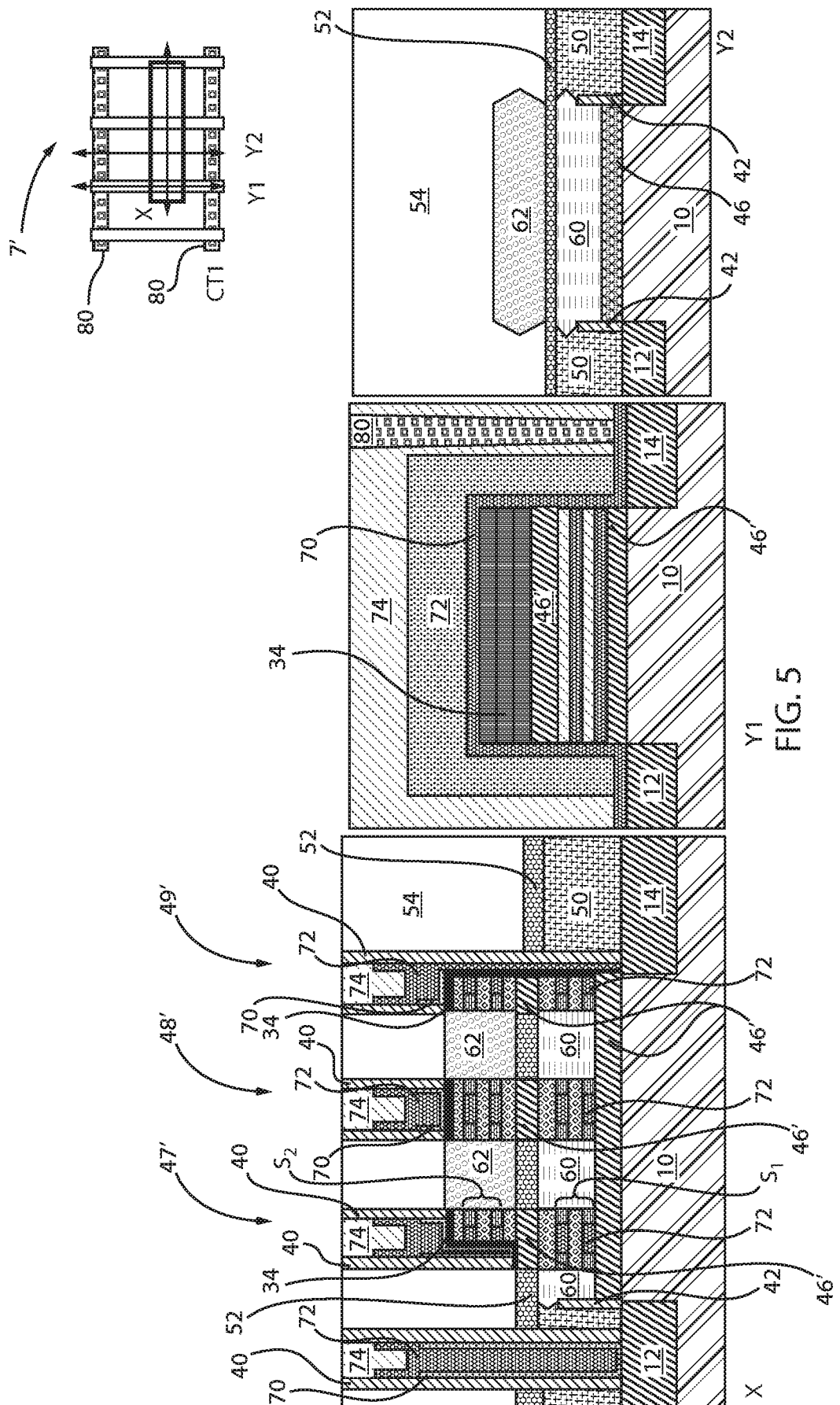
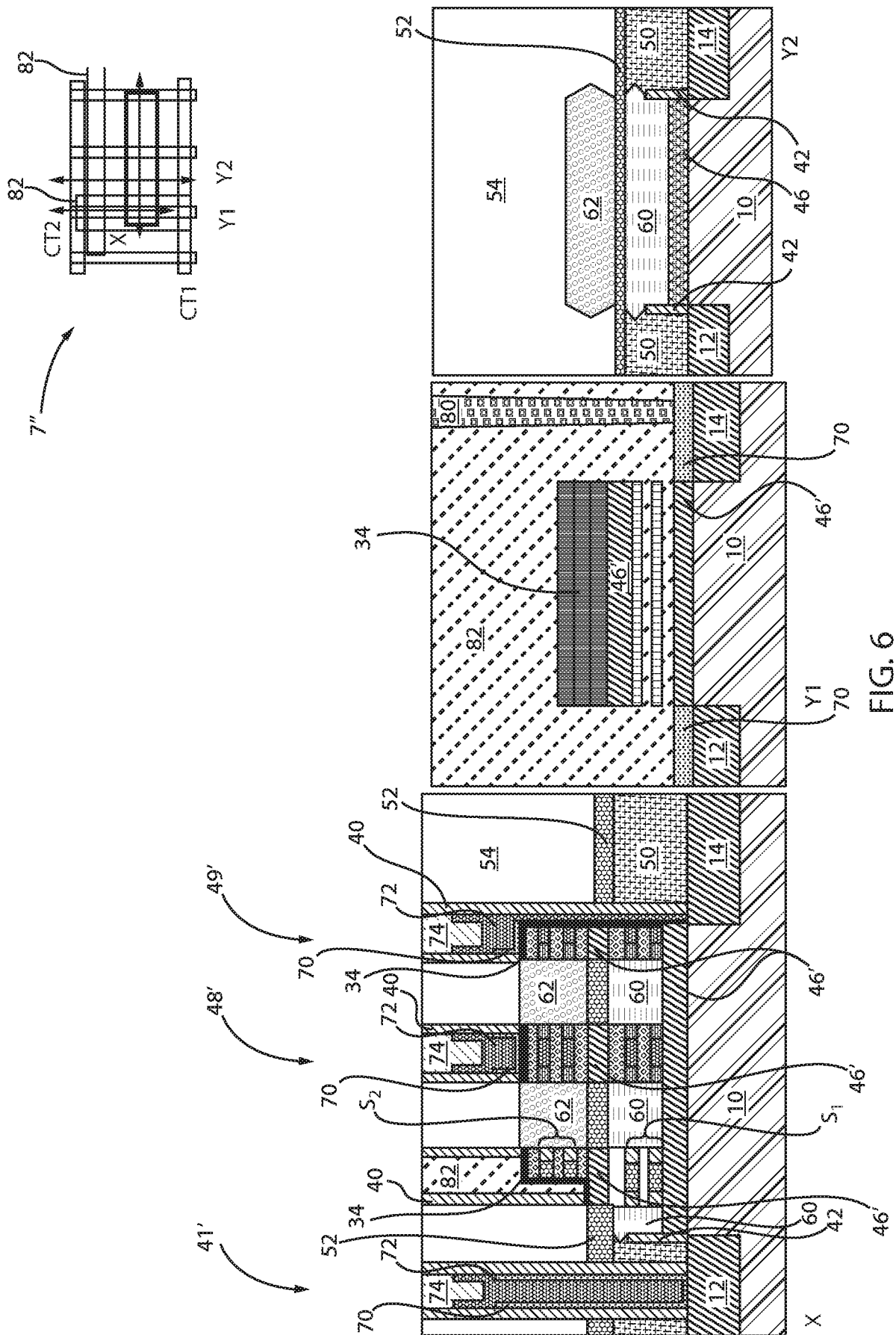


FIG. 4





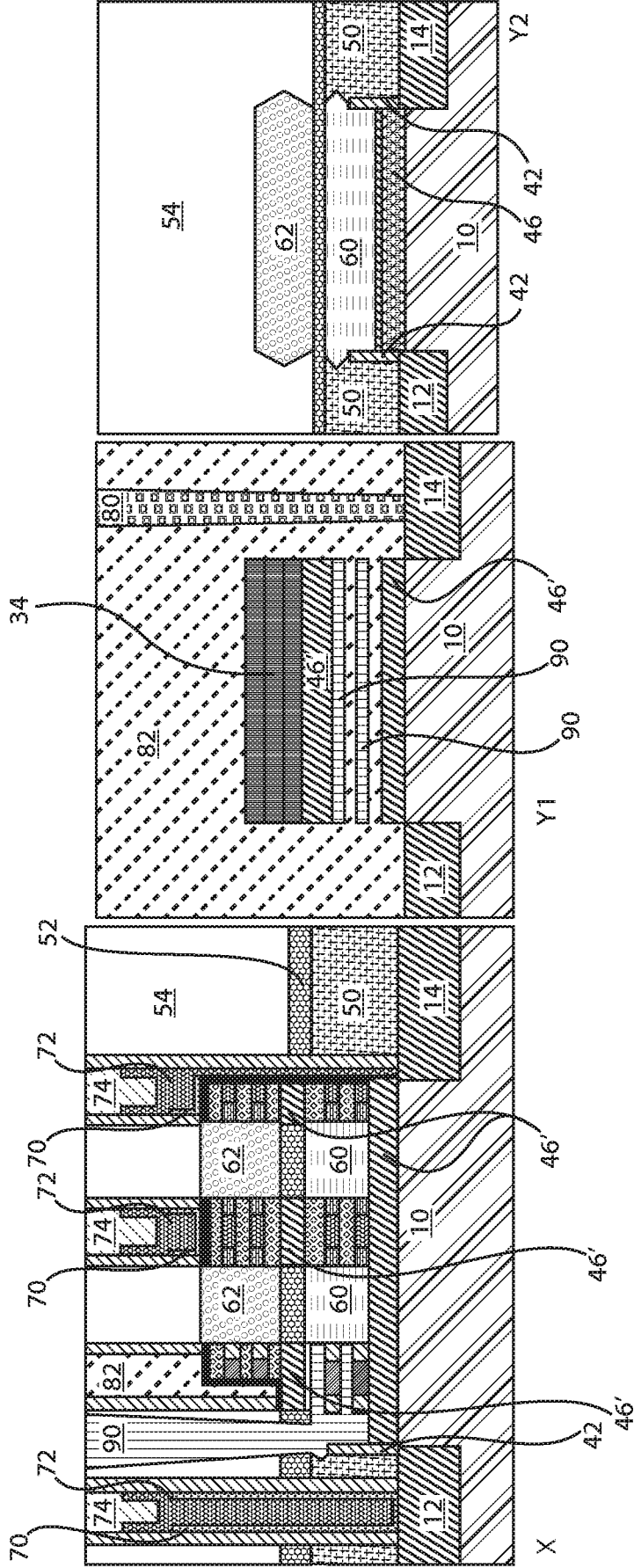


FIG. 7

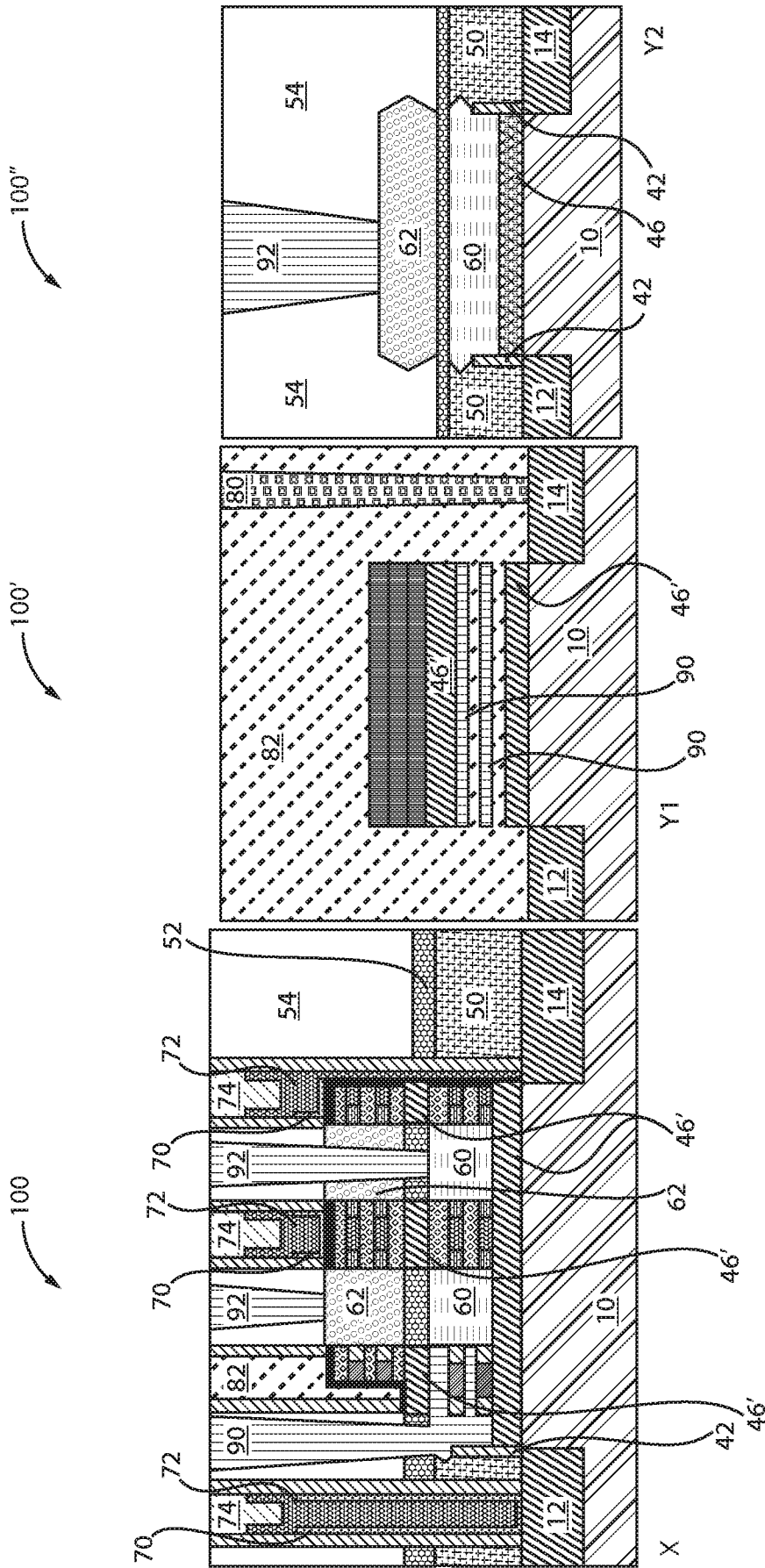


FIG. 8

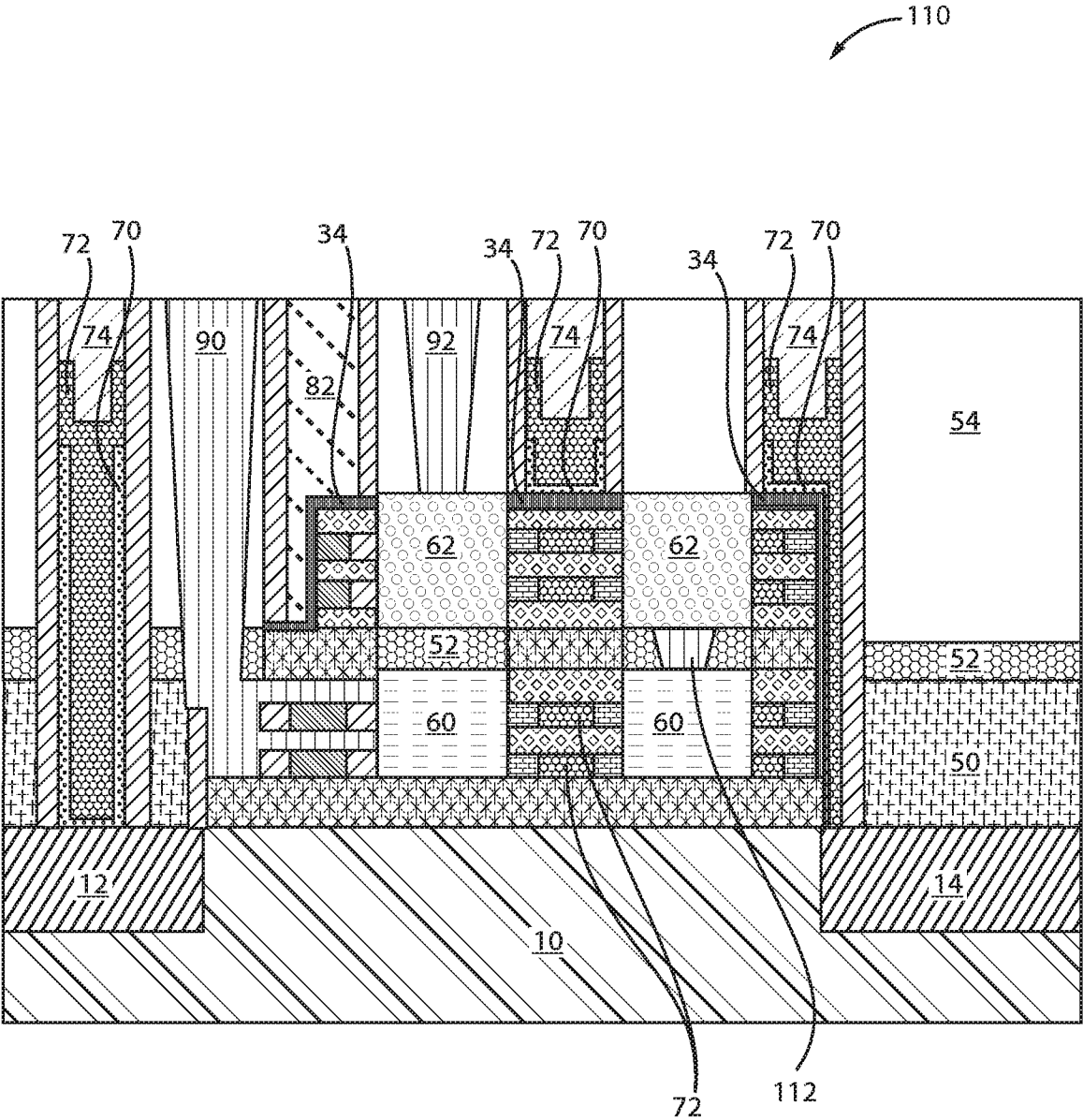


FIG. 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2022/060633

A. CLASSIFICATION OF SUBJECT MATTER INV. H01L21/822 H01L21/8238 H01L27/06 H01L27/092 ADD. H01L29/775		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H01L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2018/374791 A1 (SMITH JEFFREY [US] ET AL) 27 December 2018 (2018-12-27) paragraphs [0057] - [0063]; figures 1, 2, 12, 13, 19, 20 -----	10, 16-20
Y	US 2021/175128 A1 (GARDNER MARK I [US] ET AL) 10 June 2021 (2021-06-10) paragraphs [0034], [0036], [0040], [0044], [0047] - [0056], [0058]; figures 1-3, 5, 9, 12-21 -----	1-20
Y	US 2021/202500 A1 (CHANEMOUGAME DANIEL [US] ET AL) 1 July 2021 (2021-07-01) paragraphs [0078] - [0081]; figures 12, 14D -----	1-20
A	US 2017/358584 A1 (WANG CHIN-SHAN [TW] ET AL) 14 December 2017 (2017-12-14) paragraphs [0020] - [0023]; figure 2A -----	5, 7, 13, 15
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search		Date of mailing of the international search report
17 January 2023		27/01/2023
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer Seck, Martin

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/IB2022/060633

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2018374791 A1	27-12-2018	CN 110800113 A JP 6865864 B2 JP 2020524907 A KR 20200011035 A TW 201917893 A US 2018374791 A1 WO 2018237106 A1	14-02-2020 28-04-2021 20-08-2020 31-01-2020 01-05-2019 27-12-2018 27-12-2018
US 2021175128 A1	10-06-2021	NONE	
US 2021202500 A1	01-07-2021	KR 20220121861 A TW 202135242 A US 2021202500 A1 WO 2021138551 A1	01-09-2022 16-09-2021 01-07-2021 08-07-2021
US 2017358584 A1	14-12-2017	CN 107492542 A TW 201743458 A US 2017358584 A1 US 2018151570 A1 US 2020035684 A1 US 2021343723 A1	19-12-2017 16-12-2017 14-12-2017 31-05-2018 30-01-2020 04-11-2021