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- (54) **Title:** AIR GAP FORMATION BY PHYSICAL VAPOR DEPOSITION

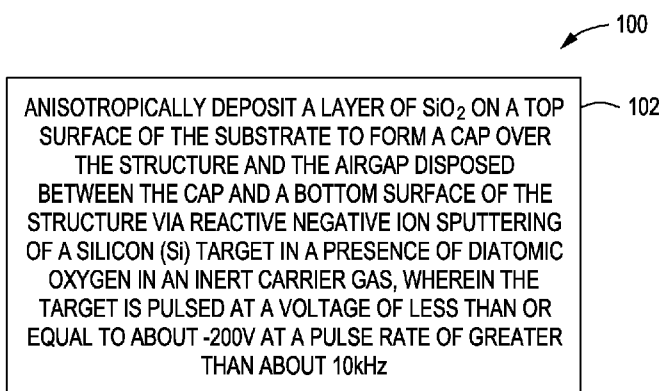


FIG. 1

- (57) **Abstract:** Methods for forming an airgap within a structure of a substrate, comprising anisotropically depositing a layer of SiO₂ on a top surface of the substrate to form a cap over the structure and the airgap disposed between the cap and a bottom surface of the structure via reactive negative ion sputtering of a silicon (Si) target in a presence of diatomic oxygen in an inert carrier gas, wherein the target is pulsed at a voltage of less than or equal to about -200 V at a pulse rate of greater than about 10 kHz. A substrate having an airgap is also disclosed.



Air Gap Formation by Physical Vapor Deposition

FIELD

[0001] Embodiments of the present disclosure generally relate to processing of a semiconductor substrate or device, and in particular, to forming an airgap within a structure disposed in a substrate.

BACKGROUND

[0002] The inventors have observed that the scaling down of DRAM structures especially beyond 20 nm nodes results in bitline sensing margin becoming problematic due to the increasing ratio of parasitic bitline capacitance (C_b) to cell capacitance (C_s). The inventors have noticed that air gap structures may be utilized to decrease C_b in low C_s applications. However, the inventors have also observed that processes for forming an air gap do not provide adequate results.

[0003] Thus, the inventors have provided improved techniques for forming air gaps in structures.

SUMMARY

[0004] In embodiments, a method to form an airgap within a structure of a substrate comprises anisotropically deposit a layer of SiO_2 on a top surface of the substrate to form a cap over the structure and the airgap disposed between the cap and a bottom surface of the structure via reactive negative ion sputtering of a silicon (Si) target in a presence of diatomic oxygen in an inert carrier gas, wherein the target is pulsed at a voltage of less than or equal to about -200 V at a pulse rate of greater than about 10 kHz.

[0005] In embodiments, a substrate comprises a structure disposed within the substrate having a structure width of less than or equal to about 20 nm, and a structure depth of greater than or equal to about 60 nm; and a layer of SiO_2 disposed over a top surface of the substrate forming a cap over the structure with an airgap disposed between the cap and a bottom surface of the structure; wherein a distance from a top of the airgap to a point coplanar with a top surface of the substrate is greater than or equal to about 25 nm; wherein a maximum width of the airgap formed is greater than or equal to about 40% of the structure width; and

wherein a length of the airgap is greater than or equal to about 25 nm less than the structure depth.

[0006] In embodiments, a non-transitory computer readable medium is provided, having instructions stored thereon which, when executed, causes a processing chamber to perform any of the methods described herein.

[0007] Other and further embodiments of the present disclosure are described below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Embodiments of the present disclosure, briefly summarized above and discussed in greater detail below, can be understood by reference to the illustrative embodiments of the disclosure depicted in the appended drawings. However, the appended drawings illustrate only typical embodiments of the disclosure and are therefore not to be considered limiting of scope, for the disclosure may admit to other equally effective embodiments.

[0009] FIG. 1 is a flowchart depicting a method to form an airgap within a structure of a substrate according to an embodiment.

[0010] FIG. 2 is a flowchart depicting a method to form an airgap within a structure of a substrate according to an embodiment.

[0011] FIG. 3 depicts a reaction chamber suitable for use according to embodiments disclosed herein.

[0012] FIG. 4A depicts a structure disposed in a substrate having a portion of a layer of SiO₂ disposed over a portion of the top surface, but which does not form a cap over the structure according to embodiments disclosed herein.

[0013] FIG. 4B depicts a structure disposed in a substrate having a layer of SiO₂ disposed over the top surface forming a cap over the structure with an airgap disposed within the structure according to embodiments disclosed herein.

[0014] FIG. 4C depicts a structure disposed in a substrate having a layer of SiO₂ disposed over the top surface forming a cap over the structure with an airgap disposed within the structure according to embodiments disclosed herein.

[0015] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. The figures are not drawn to scale and may be simplified for clarity. Elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0016] Embodiments of a method to form an airgap within a structure of a substrate are provided herein. In embodiments, the method comprises anisotropically depositing a layer of SiO₂ or other dielectric material having a dielectric constant less than or equal to about that of SiO₂ on a top surface of the substrate to form a cap over the structure and the airgap disposed between the cap and a bottom surface of the structure via reactive negative ion sputtering of a silicon (Si) target in a presence of diatomic oxygen in an inert carrier gas, wherein the target is pulsed at a voltage of less than or equal to about -200 V at a pulse rate of greater than about 10 kHz. In embodiments, the target is pulsed at a voltage of about -300 V to about -500 V at a pulse rate from about 10 kHz to about 1000 kHz. In embodiments, the method further comprises applying an RF bias to the substrate of less than or equal to about 500 W. In some embodiments, the RF bias is applied at a frequency from about 2 MHz to about 20 MHz.

[0017] In embodiments, a weight-to-weight ratio (weight:weight) of diatomic oxygen to the inert carrier gas is greater than or equal to about 1:1. In embodiments, the inert carrier gas comprises argon, and the weight-to-weight ratio of diatomic oxygen to argon is greater than or equal to about 10:1.

[0018] In embodiments, the substrate is maintained at a temperature from about 200°C to about 500°C.

[0019] In embodiments, the structure disposed in the substrate has a structure width of less than or equal to about 20 nm, and a structure depth of greater than or equal to about 60 nm, determined from a point coplanar with the top surface of the substrate to a bottom surface of the substrate.

[0020] In embodiments, a maximum width of the airgap formed within the structure is greater than or equal to about 40% of a structure width. Stated another way, the maximum width of the airgap formed within the structure is from the structure width to about 40% of the structure width. In embodiments, the maximum width of the airgap formed within the structure is greater than 90% of the structure width.

[0021] In embodiments, a distance from a top of the airgap to a point coplanar with the top surface of the substrate is greater than or equal to about 25 nm. In embodiments, the distance from the top of the airgap to the point coplanar with the top surface of the structure is from about 30 nm to about 40 nm. In embodiments, a length of the airgap is from about 25 nm less than a structure depth to about 45 nm less than the structure depth.

[0022] In embodiments, the anisotropically depositing the layer of SiO₂ on a top surface of the substrate to form the cap over the structure and the airgap disposed between the cap and the bottom surface of the structure comprises depositing a first layer of SiO₂ on the top surface of the substrate at a first deposition rate, followed by depositing a second layer of SiO₂ on the first layer and on portions of the top surface of the substrate not covered by the first layer at a second deposition rate to form the cap over the structure, wherein the second deposition rate is greater than the first deposition rate.

[0023] In embodiments, the first layer of SiO₂ is deposited while the target is pulsed at a first voltage, and the second layer is deposited while the target is pulsed at a second voltage which is less than the first voltage. In embodiments, a first weight-to-weight ratio of diatomic oxygen to the inert carrier gas of the first deposition rate is less than a second weight-to-weight ratio of diatomic oxygen to the inert carrier gas of the second deposition rate. In embodiments, an RF bias is applied to the substrate during the first deposition rate at a first power, and the RF bias applied to the substrate during the second deposition rate is at a second power which is less than the first power.

[0024] FIG. 1 is a flowchart of an example method 100 to form an airgap within a structure of a substrate.

[0025] As shown in FIG. 1, the method 100 may include anisotropically depositing a layer of SiO₂ on a top surface of the substrate to form a cap over the structure and the airgap disposed between the cap and a bottom surface of the structure via reactive negative ion sputtering of a silicon (Si) target in a presence of diatomic oxygen in an inert carrier gas, where the target is pulsed at a voltage of less than or equal to about -200 V at a pulse rate of greater than about 10 kHz (block 102).

[0026] The method 100 may include additional embodiments, such as any single embodiment or any combination of embodiments described below and/or in connection with one or more other processes described elsewhere herein. In embodiments, the target is pulsed at a voltage of about -300 V to about -500 V at a pulse rate from about 10 kHz to about 1000 kHz. In some embodiments, the voltage is less than or equal to about -200 V, or less than or equal to about -250 V, or less than or equal to about -300 V, or less than or equal to about -350 V, or less than or equal to about -400 V, or less than or equal to about -450 V, or less than or equal to about -500 V.

[0027] In embodiments, the method 100 may include applying an RF bias to the substrate, which in embodiments may be at a power of less than or equal to about 500 W and the RF bias may be applied at a frequency from about 2 MHz to about 20 MHz. In embodiments, an RF bias applied to the substrate is less than or equal to about 500 W, or less than or equal to about 450 W, or less than or equal to about 400 W, or less than or equal to about 350 W, or less than or equal to about 300 W, or less than or equal to about 250 W, or less than or equal to about 200 W, or less than or equal to about 150 W, or less than or equal to about 100 W, or less than or equal to about 50 W, or less than or equal to about 10 W. In embodiments, the lower limit of the RF bias applied to the substrate is greater than or equal to about 1 W.

[0028] In some embodiments of the method 100, alone or in combination with one or more other embodiments, a weight-to-weight ratio of diatomic oxygen to the inert carrier gas is greater than or equal to about 1:1. In embodiments, the inert carrier gas comprises argon. In some embodiments, the inert carrier gas consists essentially of or consists of argon. In embodiments of the method 100, the weight-

to-weight ratio of diatomic oxygen to the inert carrier gas is greater than or equal to about 10:1, or greater than or equal to about 100:1, greater than or equal to about 1000:1. In some embodiments, the weight-to-weight ratio of diatomic oxygen to argon is greater than or equal to about 10:1, or greater than or equal to about 100:1, greater than or equal to about 1000:1.

[0029] In some embodiments of the method 100, the substrate is maintained at a temperature of greater than or equal to about 200°C, or greater than or equal to about 300°C, or greater than or equal to about 400°C, and less than or equal to about 500°C.

[0030] FIG. 2 is a flowchart of an example method 200, a method to form an airgap within a structure of a substrate. In some embodiments, one or more process blocks of Fig. 2 may be performed by a device.

[0031] As shown in FIG. 2, method 200 may include anisotropically depositing a first layer of SiO₂ on a top surface of the substrate at a first deposition rate (block 202), which in embodiments may only partially cover the top surface of the substrate, e.g., a seed layer, which is followed by depositing a second layer of SiO₂ on the top surface of the substrate at a second deposition rate which is greater than the first deposition rate to form a cap over the structure and the airgap disposed between the cap and a bottom surface of the structure via reactive negative ion sputtering of a silicon (Si) target in a presence of diatomic oxygen in an inert carrier gas, where the target is pulsed at a voltage of less than or equal to about -200 V at a pulse rate of greater than about 10 kHz (block 204).

[0032] Method 200 may include additional embodiments, such as any single embodiment or any combination of embodiments described in connection with method 100, and/or in connection with one or more other processes described elsewhere herein. In an embodiment, the first voltage of the first deposition rate is higher than a second voltage of the second deposition rate. In embodiments, the first voltage of the first deposition rate is from about -200 V to greater than or equal to about -250 V, or greater than or equal to about -300 V, and the second voltage of the second deposition rate is less than or equal to about -300 V, or less than or

equal to about -350 V, or less than or equal to about -400 V, or less than or equal to about -450 V, or less than or equal to about -500 V.

[0033] In embodiments, a first weight-to-weight ratio of diatomic oxygen to the inert carrier gas of the first deposition rate is less than a second weight-to-weight ratio of diatomic oxygen to the inert carrier gas of the second deposition rate. In embodiments, a first weight-to-weight ratio of diatomic oxygen to the inert carrier gas of the first deposition rate is greater than or equal to about 1:1, or greater than or equal to about 10:1, or greater than or equal to about 100:1, and a second-weight-to-weight ratio of diatomic oxygen to the inert carrier gas of the second deposition rate is greater than or equal to about 10:1, or greater than or equal to about 100:1, or greater than or equal to about 500:1, or greater than or equal to about 1000:1.

[0034] In embodiments, an RF bias is applied to the substrate during the first deposition rate at a first power of less than or equal to about 500 W, or less than or equal to about 450 W, or less than or equal to about 400 W, or less than or equal to about 350 W, and the RF bias is applied to the substrate during the second deposition rate at a second power of less than or equal to about 300 W, or less than or equal to about 250 W, or less than or equal to about 200 W, or less than or equal to about 150 W, or less than or equal to about 100 W, or less than or equal to about 50 W, or less than or equal to about 10 W. In embodiments, the lower limit of the RF bias applied to the substrate is greater than or equal to about 1 W.

[0035] FIG. 3 schematically depicts a reaction chamber 300 according to embodiments disclosed herein, wherein a silicon (Si) target 302 is utilized to anisotropically deposit a layer of silicon dioxide (SiO₂) on a top surface 304 of a substrate 306 via reactive negative ion sputtering of the Si target 302 in a presence of diatomic oxygen in an inert carrier gas (depicted in a processing volume 308 of the reaction chamber 300), e.g., Ar/O₂. The Si target 302 is coupled to a DC power source 310 and pulsed at a voltage of less than or equal to about -200 V at a pulse rate of greater than about 10 kHz. In embodiments, an RF source 312 applies RF bias to the substrate of less than or equal to about 500 W at a frequency from about 2 MHz to about 20 MHz.

[0036] FIG. 4A depicts a structure 400 disposed in the substrate 306 having structure width 402, a structure depth 404 equal to a perpendicular linear distance from a point coplanar with the top surface 304 of the substrate 306 (represented by point (x) on dotted line 406) to a bottom surface 410 of the structure 400. FIG. 4A further depicts a portion of a layer of SiO₂ 408 disposed over a portion of the top surface 304 of the substrate 306, but which does not form a cap 412 over the structure 400 as shown in FIG. 4B. In other words, in FIG. 4A, the layer of SiO₂ 408 disposed over the top surface 304 of the substrate 306 does not completely cover and plug the top of the structure 400.

[0037] In some embodiments, the structure 400 disposed in the substrate 306 has a structure width 402 of less than or equal to about 20 nm, or less than or equal to about 15 nm, or less than or equal to about 10 nm, and a structure depth 404 of greater than or equal to about 60 nm, or greater than or equal to about 80 nm, or greater than or equal to about 100 nm. As depicted in FIGs. 4A and 4B, the structure may be disposed within a layer of tungsten.

[0038] FIG. 4B depicts the same structure 400 from FIG. 4A, disposed within the substrate 306, wherein a layer of SiO₂ disposed over a top surface 304 of the substrate 306 forms a cap 412 over the structure 400 with an airgap 414 disposed between the cap 412 and the bottom surface 410 of the structure 400. As depicted in FIG. 4B, in embodiments, a maximum width 416 of the airgap 414 formed within the structure 400 is greater than or equal to about 40% of a structure width 402. In some embodiments, the maximum width 416 of the airgap 414 formed within the structure 400 is greater than 90% of the structure width.

[0039] FIG. 4B further depicts a distance 420 from a top 418 of the airgap 414 to a point (x) coplanar 406 with the top surface 304 of the substrate 306 is greater than or equal to about 25 nm, which in embodiments may be greater than or equal to about 30 nm, or greater than or equal to about 35 nm, or greater than or equal to about 40 nm.

[0040] As is also depicted in FIG. 4B, in embodiments, a length 422 of the airgap 414 is from about 25 nm less than a structure depth 404 to about 45 nm less than the structure depth 404 (see FIG. 4A).

[0041] FIG. 4C depicts an embodiment in which the maximum width 416 of the airgap 414 formed within the structure 400 is equal to the structure width 402, a distance from a top 418 of the airgap 414 to a point (x) coplanar 406 with the top surface 304 of the substrate 306 is greater than or equal to about 25 nm, and a length 422 of the airgap 414 is from about 25 nm less than a structure depth to about 45 nm less than the structure depth 404 of the structure 400.

[0042] In embodiments, the resulting substrate according to embodiments herein having a structure 400 disposed within the substrate 306 in which a layer of SiO₂ 408 is disposed over a top surface 304 of the substrate 306 forming a cap 412 over the structure 400 with an airgap 414 disposed between the cap 412 and a bottom surface 410 of the structure 400, has a dielectric constant of less than about 2, or less than about 1.8.

[0043] In embodiments, the distance from a top 418 of the airgap 414 to a point (x) coplanar 406 with the top surface 304 of the substrate 306 is sufficient such that upon further processing, e.g., CMP, in which all or a portion of the layer of SiO₂ 408 disposed over the top surface 304 of the substrate 306 is removed, the airgap 414 remains beneath the cap 412 covering the opening of the structure 400.

[0044] In embodiments, the distance from a top 418 of the airgap 414 to a point (x) coplanar 406 with the top surface 304 of the substrate 306 may be controlled by controlling the voltage and/or the pulse rate at which the target is pulsed, by controlling the RF bias, and/or by controlling the pressure of diatomic oxygen, which is related to the mass:mass ratio of diatomic oxygen to the inert carrier gas. The distance from a top 418 of the airgap 414 to a point (x) coplanar 406 with the top surface 304 of the substrate 306 may be increased by decreasing the voltage and/or increasing the power including the pulse rate at which the target is pulsed, and/or decreasing the RF bias applied to the substrate, and/or by increasing the partial pressure of diatomic oxygen, which is related to increasing the mass:mass ratio of diatomic oxygen to the inert carrier gas.

[0045] The instant disclosure includes, but is not limited to the following embodiments.

E1. A method to form an airgap within a structure of a substrate, comprising:

anisotropically depositing a layer of SiO₂ on a top surface of the substrate to form a cap over the structure and the airgap disposed between the cap and a bottom surface of the structure via reactive negative ion sputtering of a silicon (Si) target in a presence of diatomic oxygen in an inert carrier gas, wherein the target is pulsed at a voltage of less than or equal to about -200 V at a pulse rate of greater than about 10 kHz.

E2. The method according to embodiment E1, wherein the target is pulsed at a voltage of about 300 V to about -500 V at a pulse rate from about 10 kHz to about 1000 kHz.

E3. The method according to embodiments E1-E2, further comprising applying an RF bias to the substrate of less than or equal to about 500 W.

E4. The method according to embodiment E3, wherein the RF bias is applied at a frequency from about 2 MHz to about 20 MHz.

E5. The method according to embodiments E1-E4, wherein a weight-to-weight ratio of diatomic oxygen to the inert carrier gas is greater than or equal to about 1:1.

E6. The method according to embodiment E5, wherein the inert carrier gas comprises argon, and wherein a weight-to-weight ratio of diatomic oxygen to argon is greater than or equal to about 10:1.

E7. The method according to embodiments E1-E6, wherein the substrate is maintained at a temperature from about 200°C to about 500°C.

E8. The method according to embodiments E1-E7, wherein the structure has a structure width of less than or equal to about 20 nm, and a structure depth of greater than or equal to about 60 nm.

E9. The method according to embodiments E1-E8, wherein a maximum width of the airgap formed within the structure is greater than or equal to about 40% of a structure width.

E10. The method according to embodiment E9, wherein the maximum width of the airgap formed within the structure is greater than 90% of the structure width.

E11. The method according to embodiments E1-E10, wherein a distance from a top of the airgap to a point coplanar with the top surface of the substrate is greater than or equal to about 25 nm.

E12. The method according to embodiment E11, wherein the distance from the top of the airgap to the point coplanar with the top surface of the structure is from about 30 nm to about 40 nm.

E13. The method according to embodiments E1-E12, wherein a length of the airgap is from about 25 nm less than a structure depth to about 45 nm less than the structure depth.

E14. The method according to embodiments E1-E13, wherein a first layer of SiO₂ is deposited on the top surface of the substrate at a first deposition rate, followed by depositing a second layer of SiO₂ on the first layer and on the top surface of the substrate at a second deposition rate to form the cap over the structure, wherein the second deposition rate is greater than the first deposition rate.

E15. The method according to embodiment E14, wherein the first layer of SiO₂ is deposited while the target is pulsed at a first voltage, and the second layer is deposited while the target is pulsed at a second voltage which is less than the first voltage.

E16. The method according to embodiments E14-E15, wherein a first weight-to-weight ratio of diatomic oxygen to the inert carrier gas of the first deposition rate is less than a second weight-to-weight ratio of diatomic oxygen to the inert carrier gas of the second deposition rate.

E17. The method according to embodiments E14-E16, wherein an RF bias is applied to the substrate during the first deposition rate is at a first power, and the RF bias applied to the substrate during the second deposition rate is at a second power which is less than the first power.

E18. A substrate, comprising a structure disposed according to the method of embodiments E1-E17.

E19. A substrate, comprising:

a structure disposed within the substrate having a structure width of less than or equal to about 20 nm, and a structure depth of greater than or equal to about 60 nm; and

a layer of SiO₂ disposed over a top surface of the substrate forming a cap over the structure with an airgap disposed between the cap and a bottom surface of the structure;

wherein a distance from a top of the airgap to a point coplanar with a top surface of the substrate is greater than or equal to about 25 nm;

wherein a maximum width of the airgap formed is greater than or equal to about 40% of the structure width; and

wherein a length of the airgap is greater than or equal to about 25 nm less than the structure depth.

E20. The substrate according to embodiments E18-E19, wherein:

the distance from the top of the airgap to the point coplanar with the top surface of the substrate is greater than or equal to about 25 nm;

the maximum width of the airgap is greater than or equal to about 90% of the structure width;

a length of the airgap is equal to the distance from a top of the airgap to the bottom surface of the structure; and

the structure has a dielectric constant K of less than about 2.

E21. A non-transitory computer readable medium, having instructions stored thereon which, when executed, cause a processing chamber to perform the method according to embodiments E1-E17.

E22. A non-transitory computer readable medium, having instructions stored thereon which, when executed, cause a processing chamber to perform a method to form an airgap within a structure of a substrate, the method comprising:

anisotropically depositing a layer of SiO₂ on a top surface of the substrate to form a cap over the structure and the airgap disposed between the cap and a bottom surface of the structure via reactive negative ion sputtering of a silicon (Si) target in

a presence of diatomic oxygen in an inert carrier gas, wherein the target is pulsed at a voltage of less than or equal to about -200 V at a pulse rate of greater than about 10 kHz.

[0046] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof.

Claims:

1. A method to form an airgap within a structure of a substrate, comprising:
anisotropically depositing a layer of SiO₂ on a top surface of the substrate to form a cap over the structure and the airgap disposed between the cap and a bottom surface of the structure via reactive negative ion sputtering of a silicon (Si) target in a presence of diatomic oxygen in an inert carrier gas, wherein the target is pulsed at a voltage of less than or equal to about -200 V at a pulse rate of greater than about 10 kHz.
2. The method of claim 1, wherein the target is pulsed at a voltage of about 300 V to about -500 V at a pulse rate from about 10 kHz to about 1000 kHz.
3. The method of claim 1, further comprising applying an RF bias to the substrate of less than or equal to about 500 W.
4. The method of claim 3, wherein the RF bias is applied at a frequency from about 2 MHz to about 20 MHz.
5. The method of claim 1, wherein a weight-to-weight ratio of diatomic oxygen to the inert carrier gas is greater than or equal to about 1:1.
6. The method of claim 5, wherein the inert carrier gas comprises argon, and wherein a weight-to-weight ratio of diatomic oxygen to argon is greater than or equal to about 10:1.
7. The method of claim 1, wherein the substrate is maintained at a temperature from about 200°C to about 500°C.
8. The method of claim 1, wherein the structure has a structure width of less than or equal to about 20 nm, and a structure depth of greater than or equal to about 60 nm.

9. The method of claim 1, wherein a maximum width of the airgap formed within the structure is greater than or equal to about 40% of a structure width.
10. The method of claim 9, wherein the maximum width of the airgap formed within the structure is greater than 90% of the structure width.
11. The method of claim 1, wherein a distance from a top of the airgap to a point coplanar with the top surface of the substrate is greater than or equal to about 25 nm.
12. The method of claim 11, wherein the distance from the top of the airgap to the point coplanar with the top surface of the structure is from about 30 nm to about 40 nm.
13. The method of claim 1, wherein a length of the airgap is from about 25 nm less than a structure depth to about 45 nm less than the structure depth.
14. The method of claims 1-13, wherein a first layer of SiO₂ is deposited on the top surface of the substrate at a first deposition rate, followed by depositing a second layer of SiO₂ on the first layer and on the top surface of the substrate at a second deposition rate to form the cap over the structure, wherein the second deposition rate is greater than the first deposition rate.
15. The method of claim 14, wherein the first layer of SiO₂ is deposited while the target is pulsed at a first voltage, and the second layer is deposited while the target is pulsed at a second voltage which is less than the first voltage.
16. The method of claim 14, wherein a first weight-to-weight ratio of diatomic oxygen to the inert carrier gas of the first deposition rate is less than a second weight-to-weight ratio of diatomic oxygen to the inert carrier gas of the second deposition rate.

17. The method of claim 14, wherein an RF bias is applied to the substrate during the first deposition rate is at a first power, and the RF bias applied to the substrate during the second deposition rate is at a second power which is less than the first power.

18. A substrate, comprising:

- a structure disposed within the substrate having a structure width of less than or equal to about 20 nm, and a structure depth of greater than or equal to about 60 nm; and

- a layer of SiO₂ disposed over a top surface of the substrate forming a cap over the structure with an airgap disposed between the cap and a bottom surface of the structure;

- wherein a distance from a top of the airgap to a point coplanar with a top surface of the substrate is greater than or equal to about 25 nm;

- wherein a maximum width of the airgap formed is greater than or equal to about 40% of the structure width; and

- wherein a length of the airgap is greater than or equal to about 25 nm less than the structure depth.

19. The substrate of claim 18, wherein:

- the distance from the top of the airgap to the point coplanar with the top surface of the substrate is greater than or equal to about 25 nm;

- the maximum width of the airgap is greater than or equal to about 90% of the structure width;

- a length of the airgap is equal to the distance from a top of the airgap to the bottom surface of the structure; and

- the structure has a dielectric constant K of less than about 2.

20. A non-transitory computer readable medium, having instructions stored thereon which, when executed, cause a processing chamber to perform a method to form an airgap within a structure of a substrate, the method comprising:

anisotropically depositing a layer of SiO₂ on a top surface of the substrate to form a cap over the structure and the airgap disposed between the cap and a bottom surface of the structure via reactive negative ion sputtering of a silicon (Si) target in a presence of diatomic oxygen in an inert carrier gas, wherein the target is pulsed at a voltage of less than or equal to about -200 V at a pulse rate of greater than about 10 kHz.

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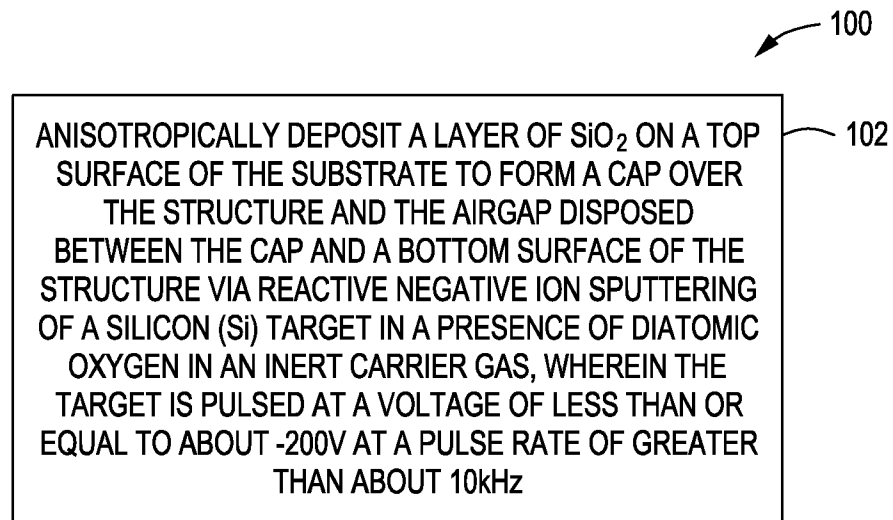


FIG. 1

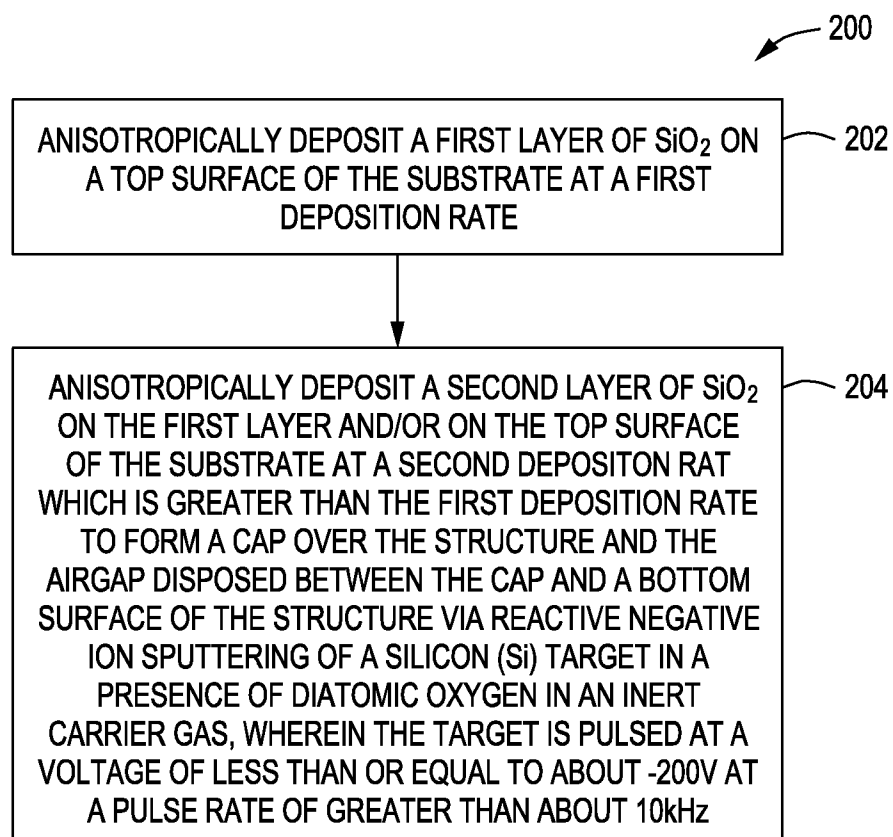
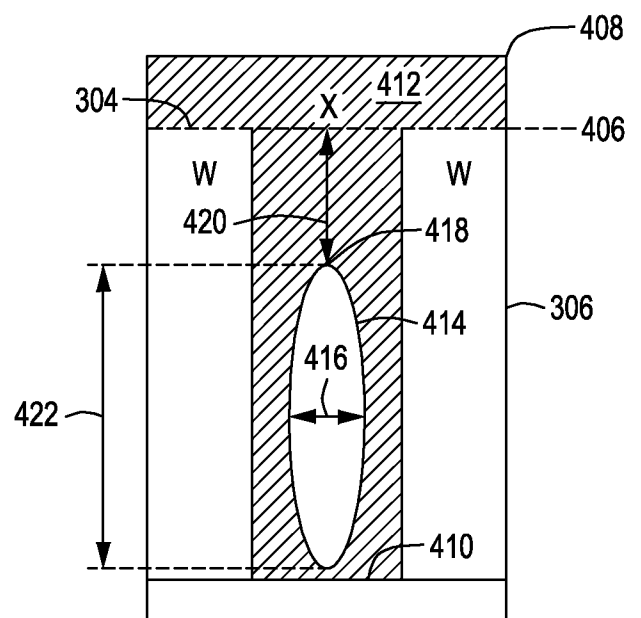
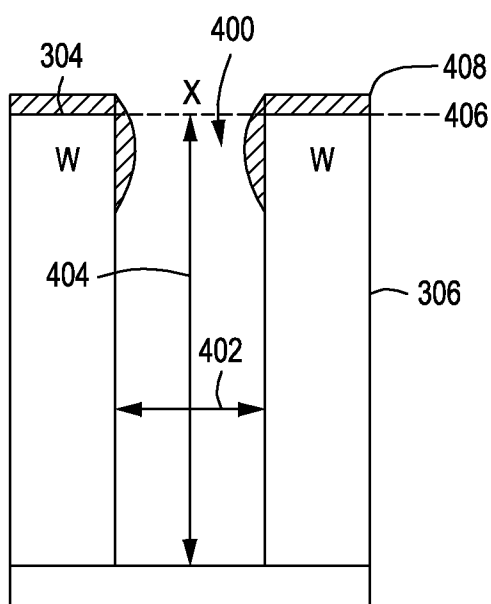
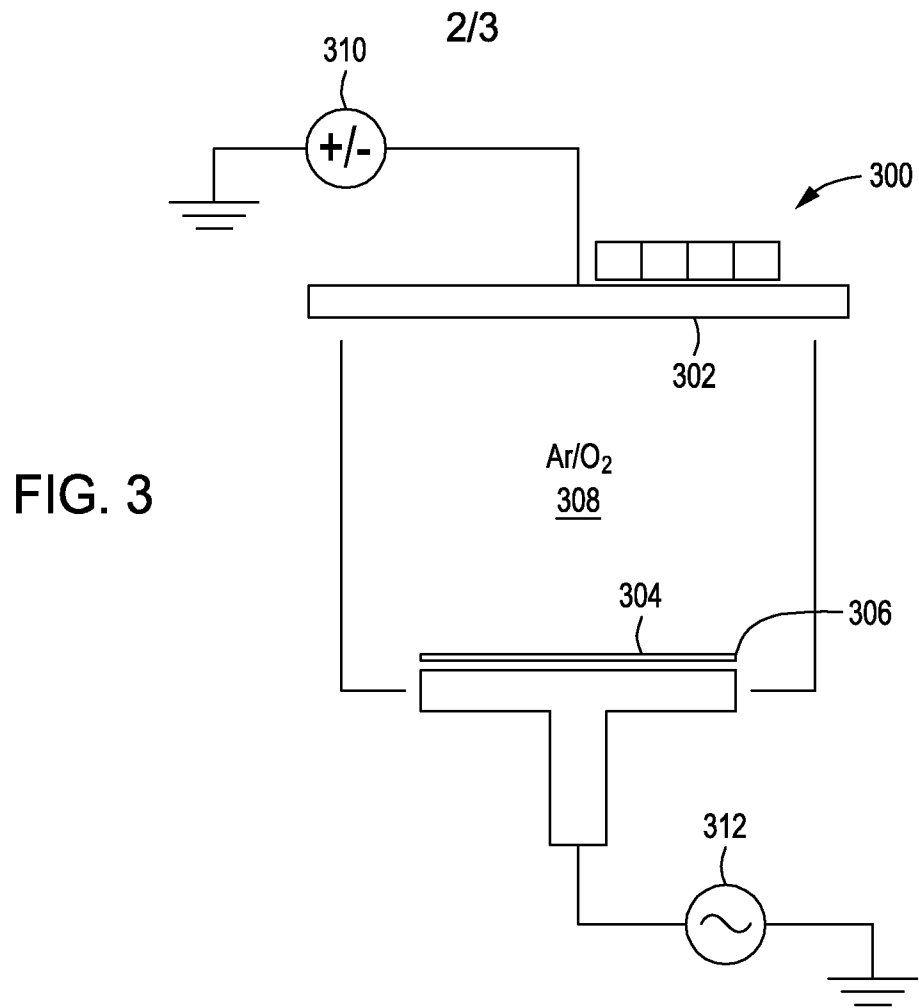


FIG. 2



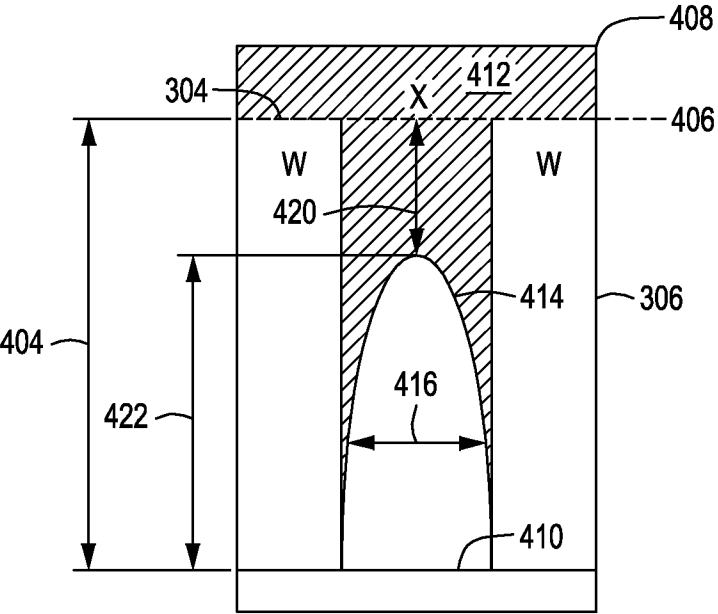


FIG. 4C

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2024/012989

A. CLASSIFICATION OF SUBJECT MATTER H01L 21/02(2006.01)i; H01L 21/768(2006.01)i According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H01L 21/02(2006.01); B32B 9/04(2006.01); C23C 14/34(2006.01); H01L 21/768(2006.01); H01L 23/528(2006.01) Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Korean utility models and applications for utility models Japanese utility models and applications for utility models Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) eKOMPASS(KIPO internal) & Keywords: DRAM, cell capacitance, PVD(physical vapor deposition), air gap		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2020-0203271 A1 (XIA TAI XIN SEMICONDUCTOR (QING DAO) LTD.) 25 June 2020 (2020-06-25) paragraphs [0029]-[0048], claim 8 and figures 2a-3c	18-19 1-17,20
Y	US 2010-0183900 A1 (ERIK WALLIN et al.) 22 July 2010 (2010-07-22) paragraph [0018], claims 2, 4 and figure 1	1-17,20
A	US 2011-0104891 A1 (AMIR AL-BAYATI et al.) 05 May 2011 (2011-05-05) paragraphs [0062]-[0092] and figures 5A-9B	1-20
A	US 2013-0267088 A1 (JONG-MIN BAEK et al.) 10 October 2013 (2013-10-10) paragraph [0050] and figures 2-9	1-20
A	US 2017-0229337 A1 (LAM RESEARCH CORPORATION) 10 August 2017 (2017-08-10) paragraphs [0031]-[0035] and figures 1-6	1-20
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents: “A” document defining the general state of the art which is not considered to be of particular relevance “D” document cited by the applicant in the international application “E” earlier application or patent but published on or after the international filing date “L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) “O” document referring to an oral disclosure, use, exhibition or other means “P” document published prior to the international filing date but later than the priority date claimed “T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention “X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone “Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art “&” document member of the same patent family		
Date of the actual completion of the international search 31 May 2024		Date of mailing of the international search report 31 May 2024
Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon 35208, Republic of Korea Facsimile No. +82-42-481-8578		Authorized officer LEE, Kang Ha Telephone No. +82-42-481-5003

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/US2024/012989

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