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(54) Title: MONOLITHIC INTEGRATION OF BACK-END P-CHANNEL TRANSISTOR WITH III-N N-CHANNEL TRANSISTOR

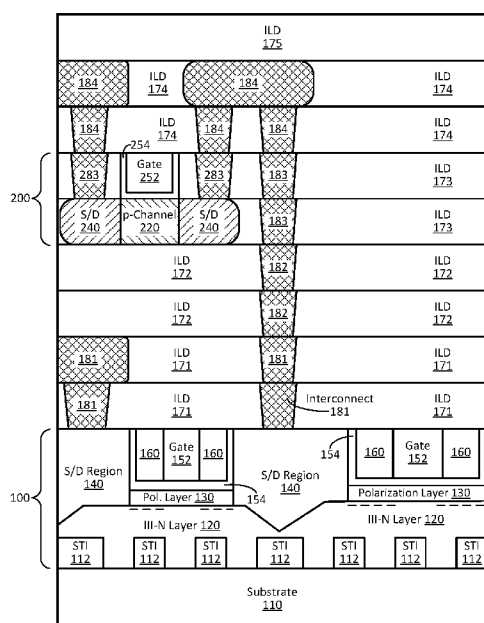


FIG. 1A

(57) Abstract: Techniques are disclosed for monolithic co-integration of a group III-N n-channel transistor with a back-end p-channel transistor. Such a co-integration scheme may be used, for example, for system-on-chip (SoC) applications including voltage regulator circuits and/or RF front end circuits. In such example applications, the back-end p-channel transistor may be used for the control logic portion of the circuit. The channel material for the back-end p-channel transistor can be selected, in some instances, to have suitable performance capabilities (e.g., carrier mobility at least approximately on par with silicon PMOS) and also have a suitable processing temperature budget that is in line with interconnect or back-end processing (e.g., a budget of approximately 400°C). Example suitable channel material for the back-end transistor includes polycrystalline or amorphous germanium (Ge), although other suitable materials will be apparent in light of this disclosure. Other embodiments may be described and/or disclosed.

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MONOLITHIC INTEGRATION OF BACK-END P-CHANNEL TRANSISTOR WITH III-N N-CHANNEL TRANSISTOR

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BACKGROUND

In the fields of wireless communication and power management, various components can be implemented using solid-state devices. For example, in radio frequency (RF) communication, the RF front-end is a generic term for the circuitry between an antenna and a digital baseband system. The RF front-end may include multiple components, such as power amplifiers, low-noise amplifiers, and voltage regulators. Such RF front-end components may include one or more transistors, such as one or more field-effect transistors (FETs). A FET is a semiconductor device that includes three terminals: a gate, a source, and a drain. A FET uses an electric field applied by the gate to control the electrical conductivity of a channel through which charge carriers (e.g., electrons or holes) flow from the source to the drain. In instances where the charge carriers are electrons, the FET is referred to as an n-channel device, and in instances where the charge carriers are holes, the FET is referred to as a p-channel device. Some FETs have a fourth terminal called, the body or substrate, which can be used to bias the transistor. A metal-oxide-semiconductor FET (MOSFET) is configured with an insulator between the gate and the body of the transistor, and MOSFETs are commonly used for amplifying or switching electronic signals. In some cases, MOSFETs include sidewall spacers (or so-called gate spacers) on either side of the gate that can help determine the channel length and can help with replacement gate processes, for example. Complementary MOS (CMOS) structures use a combination of p-channel MOSFET (PMOS) and n-channel MOSFET (NMOS) to implement logic gates and other digital circuits.

Integrated circuit (IC) fabrication primarily includes two portions: the front-end or front-end-of-line (FEOL) and the back-end or back-end-of-line (BEOL). The front-end or FEOL is the first portion of IC fabrication where individual semiconductor devices are formed, including all processes up to the deposition of metal interconnect layers. The back-end or BEOL, not to be confused with back-end chip fabrication, is the second portion of IC fabrication where the individual semiconductor devices get interconnected with metal wiring. BEOL may include any number of metallization layers, depending on the target application or end use.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A-B illustrate example integrated circuit (IC) structures including a group III-N n-channel transistor monolithically integrated with a back-end p-channel transistor, in accordance with some embodiments of the present disclosure. Note that the structures shown in Figures 1A-B are cross-sectional views taken along an orthogonal-to-gate direction. Also note that, generally, the example structure of Figure 1A utilizes a patterned shallow trench isolation (STI) layer for lateral epitaxial overgrowth (LEO) of the III-N layer for the III-N n-channel transistor, whereas the example structure of Figure 1B utilizes a buffer layer for growth of the III-N layer for the III-N n-channel transistor.

Figure 2 illustrates the example IC structure of Figure 1A, including an interlayer dielectric (ILD) hardening scheme, in accordance with an embodiment of the present disclosure.

Figure 3 illustrates the example IC structure of Figure 1A, including a back-end complementary metal-oxide-semiconductor (CMOS) device, in accordance with an embodiment of the present disclosure.

Figure 4 illustrates an example method of forming an IC structure including a group III-N n-channel transistor monolithically integrated with a back-end p-channel transistor, in accordance with some embodiments of the present disclosure.

Figure 5 illustrates an example computing system implemented with the integrated circuit structures and/or techniques disclosed herein, in accordance with some embodiments of the present disclosure.

These and other features of the present embodiments will be understood better by reading the following detailed description, taken together with the figures herein described. In the drawings, each identical or nearly identical component that is illustrated in various figures may be represented by a like numeral. For purposes of clarity, not every component may be labeled in every drawing. Furthermore, as will be appreciated, the figures are not necessarily drawn to scale or intended to limit the described embodiments to the specific configurations shown. For instance, while some figures generally indicate straight lines, right angles, and smooth surfaces, an actual implementation of the disclosed techniques may have less than perfect straight lines and right angles, and some features may have surface topography or otherwise be non-smooth, given real-world limitations of fabrication processes. Further still, some of the features in the drawings may include a patterned and/or shaded fill, which is primarily provided to assist in visually differentiating the different features. In short, the figures are provided merely to show example structures.

DETAILED DESCRIPTION

Techniques are disclosed for monolithic co-integration of a group III-N n-channel transistor with a back-end p-channel transistor. Such a co-integration scheme may be used, for example, for system-on-chip (SoC) applications including voltage regulator circuits and/or RF front end circuits. In such example applications, the back-end p-channel transistor may be used for the control logic portion of the circuit. The back-end p-channel transistor (e.g., a back-end PMOS transistor) may be monolithically formed in the interconnect stack to be co-integrated with a III-N n-channel transistor (e.g., an NMOS) located at the conventional device layer or front-end location of an integrated circuit (IC). The channel material for the back-end p-channel transistor can be selected, in some instances, to have suitable performance capabilities (e.g., approximately similar to that of silicon PMOS) and also have a suitable processing temperature budget that is in line with interconnect or back-end processing (e.g., a budget of approximately 400 °C). As such, a thin film (e.g., less than 50 nm thick) of a suitable semiconductor material can be inserted during back-end processing in the interconnect stack to enable fabrication of the back-end p-channel devices. Moreover, as the thin film will be formed during back-end processing, it can have a polycrystalline or amorphous structure, which is less desired than the typical monocrystalline/single crystal structure that can be achieved when forming transistors at the conventional device layer during front-end processing. An example of such a material that would be suitable for such a purpose is polycrystalline or amorphous germanium (Ge), although other suitable materials will be apparent in light of this disclosure. In some instances, the back-end control logic may instead be performed by a CMOS device, and as such, both a p-channel transistor and an n-channel transistor will be formed in the back-end of the IC to form the CMOS device. In some instances, the interconnect stack above and local to the III-N n-channel transistor may have to withstand high voltage supplies, and thus a site-specific ILD hardening scheme may be used to ensure high voltage compatibility of the interconnect stack at those locations. Numerous variations and configurations will be apparent in light of this disclosure.

General Overview

For integrated circuits including semiconductor devices, some such devices may use both n-channel and p-channel transistors, such as controller and driver circuits. For high voltage applications of such devices, group III-N semiconductor channel material transistors are being explored. For example, III-N material integration on 300 mm silicon (Si) substrates may be achieved via thick buffer growth or lateral epitaxial overgrowth (LEO) from patterned trenches.

Such III-N material integration shows significant benefit for n-channel devices as compared to Si or gallium arsenide for voltage regulation and RF power amplifier applications, for example. However, such applications require p-channel control logic. Due to bandstructure, III-N p-channel transistors have relatively poor performance (e.g., as compared to Si p-channel transistors), and as such, p-channel transistors are difficult to implement using III-N materials. While Si p-channel transistors (e.g., Si PMOS) have been explored as an option, such transistors are difficult to process due to the substrate surface orientation used for processing III-N transistors (e.g., a Si substrate having a <111> surface orientation) and due to the significant step height between thick III-N transistor devices (as a result of the thick III-N epitaxial deposition used for the devices) and substantially thinner Si devices. Moreover, the significant step height difference in the thicknesses of the devices (the vertical dimension when looking at a cross-section of the devices that is orthogonal to the gate) may be at least 200 nm (and may even be greater than 1 micron), thereby making processing both of the devices at the transistor level very difficult.

Thus and in accordance with one or more embodiments of this disclosure, techniques are provided for monolithic integration of a group III-N n-channel transistor with a back-end p-channel transistor. As used herein, group III-N material or III-N material includes a compound of one or more group III elements (e.g., aluminum, gallium, indium, boron, thallium), with nitrogen. Accordingly, III-N material as used herein includes, but is not limited to, gallium nitride (GaN), indium nitride (InN), aluminum nitride (AlN), aluminum indium nitride (AlInN), aluminum gallium nitride (AlGaN), indium gallium nitride (InGaN), and aluminum indium gallium nitride (AlInGaN). As will be understood based on this disclosure, monolithic integration of the III-N n-channel transistor and the p-channel transistor includes that the two transistors are formed on the same substrate. In other words, monolithic integration does not require one of the two transistors to be formed on a separate transfer substrate and then bonded to a receiving substrate including the other of the two transistors, which may be referred to as layer stacking. Such a bonding integration scheme or layer stacking may be detected through an oxide bond used to bond the transferred device to the receiving substrate, where the oxide bond layer is a different material than the interlayer dielectric (ILD) material used elsewhere on the receiving substrate. In contrast, the monolithic integration schemes described herein can be achieved by forming both the III-N n-channel transistor and p-channel transistor on the same substrate (or die or chip), without the use of bonding/layer stacking techniques.

In some embodiments, the p-channel transistors that are formed using a monolithic integration scheme are formed during the back-end or back-end-of-line (BEOL) of the IC

fabrication. As previously described, the back-end or BEOL, used in conjunction with IC fabrication, refers to the portion of IC fabrication where individual devices get interconnected with wiring. In other words, BEOL processing generally begins after front-end or front-end-of-line (FEOL) processing has been completed to form, for example, transistors at the conventional device level. In some embodiments, a thin film of the p-channel material is formed during BEOL processing, in the interconnect stack, to enable fabrication of a p-channel transistor for co-integration with the III-N n-channel transistor (e.g., where the p-channel transistor is used for control logic applications). In some embodiments, both a p-channel transistor and an n-channel transistor may be formed during BEOL processing to be co-integrated with the III-N n-channel transistor, where the BEOL p-channel and n-channel transistors form a complementary device, such as a complementary metal-oxide-semiconductor (CMOS) device (e.g., and the CMOS device may be used for control logic applications). In some embodiments, such BEOL transistor devices may be selected based on having performance attributes that are at least similar to Si p-channel transistor devices and a temperature budget that aligns with back-end/interconnect processing (e.g., temperature processing of less than 500, 450, 400, 350, or 300° C). For instance, in some such embodiments, the BEOL p-channel transistor devices may be formed using any suitable channel material that meets those two criteria, such as germanium (Ge), silicon germanium (SiGe), or III-Sb material. As used herein, group III-Sb material or III-Sb material includes a compound of one or more group III elements (e.g., aluminum, gallium, indium, boron, thallium), with antimony. Accordingly, III-Sb material as used herein includes, but is not limited to, gallium antimonide (GaSb), indium antimonide (InSb), aluminum antimonide (AlSb), aluminum indium antimonide (AlInSb), aluminum gallium antimonide (AlGaSb), indium gallium antimonide (InGaSb), and aluminum indium gallium antimonide (AlInGaSb). In embodiments where the back-end p-channel transistor includes SiGe channel material, the concentration of Ge may be expressed as x in the representation $\text{Si}_{1-x}\text{Ge}_x$, and in some such embodiments, x may be selected to be at least 0.5, 0.6, 0.7, 0.8, or 0.9 (i.e., at least 50, 60, 70, 80, or 90 percent Ge concentration), or some other suitable threshold Ge concentration, as will be apparent in light of this disclosure. Note that as a result of forming the thin film of semiconductor material (used for the back-end transistor channel region) during back-end processing, the material can have a polycrystalline or amorphous structure, as will be described in more detail herein.

In some embodiments, the co-integration of III-N n-channel transistors with p-channel transistors formed during BEOL processing may also include an interlayer dielectric (ILD) hardening scheme that is specific and local to the III-N n-channel transistor areas. In other

words, the ILD hardening scheme may be performed in ILD portions above areas where the III-N n-channel devices are formed. In some such embodiments, the ILD hardening scheme may be used to allow for larger dielectric breakdown at a given pitch, thereby enabling voltages of greater than 5 V and even up to hundreds of volts to be supplied to the III-N n-channel transistors as needed for particular applications, such as voltage regulator and RF power amplifier applications, to name a few example applications. In some embodiments, the hardening scheme may include radiation and/or implantation after the deposition of the ILD material, as will be apparent in light of this disclosure.

Use of the techniques and structures provided herein may be detectable using tools such as: electron microscopy including scanning/transmission electron microscopy (SEM/TEM), scanning transmission electron microscopy (STEM), and reflection electron microscopy (REM); composition mapping; x-ray crystallography or diffraction (XRD); energy-dispersive x-ray spectroscopy (EDS); secondary ion mass spectrometry (SIMS); time-of-flight SIMS (ToF-SIMS); atom probe imaging or tomography; local electrode atom probe (LEAP) techniques; 3D tomography; or high resolution physical or chemical analysis, to name a few suitable example analytical tools. In particular, in some embodiments, such tools may indicate an integrated circuit including a III-N n-channel transistor on a substrate and located at a conventional transistor layer and a p-channel transistor above the III-N n-channel transistor, and more specifically, above the first interconnect layer (as the p-channel transistor is formed during BEOL processing). In other words, the back-end p-channel transistor may be located at a metallization layer, such as at metallization layer 1, 2, 3, 4, 5, 6, 7, 8, 9, or 10 (e.g., at one of M1-M10), or at some other suitable metallization layer, as will be apparent in light of this disclosure. In some embodiments, the III-N n-channel transistor and p-channel transistor may be electrically connected to each other. In some embodiments, the p-channel transistor may be offset from the III-N n-channel transistor, such that a single cross-sectional view of the IC would not show both transistors. However, in some such embodiments, the p-channel transistor would still be formed during BEOL processing and still be above the III-N n-channel transistor (and above the first interconnect layer), such that two cross-sectional views of the IC may be used to reveal the multi-transistor structure as described herein. In some embodiments, the p-channel transistor may include materials that are compatible with back-end processing (e.g., temperatures below 400 °C). In some embodiments, the p-channel transistor formed during BEOL processing may also be electrically connected to an n-channel transistor formed during BEOL processing to, for example, form CMOS configuration (e.g., including a PMOS transistor and an NMOS transistor) that is electrically connected to the III-N n-channel transistor.

In some embodiments, as a result of the monolithic integration schemes described herein and as a result of the semiconductor channel material layer of the p-channel transistor being formed during back-end processing (e.g., formed on interlayer dielectric (ILD) material), the structure of the material of the channel layer of the back-end transistor can be polycrystalline or amorphous. Such structures would typically be avoided for the semiconductor channel material of a transistor as compared to monocrystalline structures which are highly ordered and have a substantially unbroken lattice structure. Monocrystalline structures are preferred due to, for example, relatively better transistor performance. As can be understood, transistors added to the back-end portion of an IC via bonding (and thus not using the monolithic integration schemes described herein) are formed on a transfer wafer as described above, and thereby have a monocrystalline structure in the channel material of the transistor. Such bonded transistors including channel material having a monocrystalline structure would, with all else being equal, typically achieve better performance. However, such bonding or layer stacking schemes are complicated relative to the monolithic integration techniques described herein, requiring additional processing and/or cost. Therefore, although the monolithic integration schemes described herein result in back-end transistors having polycrystalline or amorphous semiconductor channel material, use of such back-end transistors can greatly reduce processing complexity and cost, while still providing an effective solution for co-integration of III-N n-channel transistors with p-channel transistors (e.g., such as p-channel transistors for control logic applications for III-N high voltage NMOS devices). Moreover, in some embodiments, the polycrystalline or amorphous back-end p-channel transistors formed using the techniques described herein may actually perform better than, for example, a typical monocrystalline Si p-channel transistor. Such performance benefits may be observed based on improved p-channel Hall mobility, for example. Accordingly, the techniques and structures disclosed herein may be detected via detection of such back-end transistors including channel material having polycrystalline or amorphous structures. Further, footprint/IC area benefits can be derived from the vertical integration scheme of the monolithic integration techniques described herein, such as the formation of back-end p-channel transistors above III-N n-channel transistors, for example. Numerous configurations and variations will be apparent in light of this disclosure.

Architecture and Methodology

Figures 1A-B illustrate example integrated circuit (IC) structures including a group III-N n-channel transistor 100 monolithically integrated with a back-end p-channel transistor 200, in accordance with some embodiments of the present disclosure. Note that the structures shown in Figures 1A-B are cross-sectional views taken along an orthogonal-to-gate direction. Generally,

in these example embodiments, the IC structures include a front-end III-N n-channel transistor 100 and a back-end p-channel transistor 200, formed from the same substrate 110, as shown. As described herein, IC fabrication primarily includes two portions: the front-end or front-end-of-line (FEOL) and the back-end or back-end-of-line (BEOL). As shown in Figures 1A-B, the front-end or FEOL processing may include forming the structures at the level indicated by bracket 100 on substrate 110, in accordance with some embodiments. Further, in some such embodiments, the back-end or BEOL processing may include forming the structures above the level indicated by bracket 100, including the p-channel transistor indicated by bracket 200. The example structures of Figures 1A-B are similar, with a primary difference being the techniques used to form III-N layer 120, as will be described in more detail herein. Generally, the example structure of Figure 1A utilizes a patterned shallow trench isolation (STI) layer 112 for lateral epitaxial overgrowth (LEO) of the III-N layer 120, whereas the example structure of Figure 1B utilizes buffer layer 114 for growth of the III-N layer 120. Note that the transistors in the present disclosure are primarily described and depicted in the context of metal-oxide-semiconductor field-effect transistors (MOSFETs); however, the present disclosure is not intended to be so limited. For example, in some embodiments, one or more of the transistors may be tunnel field-effect transistors (TFETs) or any other suitable transistor configuration, as will be apparent in light of the present disclosure. Further the transistors in the present disclosure are primarily described and depicted in the context of planar transistor configurations. However, in some embodiments, the techniques can be used to form transistors including a non-planar configuration, such as finned or finFET configurations (e.g., including a dual-gate or tri-gate configuration) or gate-all-around configurations (e.g., including one or more nanowires or nanoribbons). Note that the monolithic integration techniques are primarily depicted and described herein in the context of one III-N transistor 100 co-integrated with one back-end transistor 200, for ease of description; however, the present disclosure is not intended to be limited to any quantity of transistors, unless otherwise stated. For example, one or more back-end transistors or transistor-based devices may be co-integrated with one or more front-end transistors or transistor-based devices using the techniques described herein. In some embodiments, the techniques may be used to benefit devices of varying scales, such as transistor devices having critical dimensions in the micrometer range or in the nanometer range (e.g., transistors formed at the 32, 22, 14, 10, 7, or 5 nm process nodes, or beyond).

Substrate 110, in some embodiments, may include: a bulk substrate including a group IV material, such as silicon (Si), germanium (Ge), SiGe, or silicon carbide (SiC), and/or at least one group III-V material and/or sapphire and/or any other suitable material(s) as will be apparent in

light of this disclosure; an X on insulator (XOI) structure where X is one of the aforementioned materials (e.g., group IV and/or group III-V and/or sapphire) and the insulator material is an oxide material or dielectric material or some other electrically insulating material; or some other suitable multilayer structure where the top layer includes one of the aforementioned materials (e.g., group IV and/or group III-V and/or sapphire). Note that group IV material as used herein includes at least one group IV element (e.g., carbon, silicon, germanium, tin, lead), such as Si, Ge, SiGe, or SiC to name some examples. Note that group III-V material as used herein includes at least one group III element (e.g., aluminum, gallium, indium, boron, thallium) and at least one group V element (e.g., nitrogen, phosphorus, arsenic, antimony, bismuth), such as gallium nitride (GaN), gallium arsenide (GaAs), indium gallium nitride (InGaN), and indium gallium arsenide (InGaAs), to name some examples. In some embodiments, substrate 110 may include a surface crystalline orientation described by a Miller Index of $\langle 100 \rangle$, $\langle 110 \rangle$, or $\langle 111 \rangle$, or its equivalents, as will be apparent in light of this disclosure. Although substrate 110, in this example embodiment, is shown as having a thickness (the dimension in the Y direction) similar to the other layers for ease of illustration, in some instances, substrate 110 may be much thicker than the other layers, such as having a thickness in the range of 50 to 950 microns, for example. In some embodiments, substrate 110 may be used for one or more other IC devices, such as various diodes (e.g., light-emitting diodes (LEDs) or laser diodes), various transistors (e.g., MOSFETs or TFETs), various capacitors (e.g., MOSCAPs), various microelectromechanical systems (MEMS), various nanoelectromechanical systems (NEMS), various sensors, or any other suitable semiconductor or IC devices, depending on the end use or target application. Accordingly, in some embodiments, the structures described herein may be included in a system-on-chip (SoC) application, as will be apparent in light of this disclosure.

III-N layer 120, in some embodiments, may include any suitable III-N material, such as GaN or InGaN, or any other suitable group III-N semiconductor material, as will be apparent in light of this disclosure. In some embodiments, formation of one or more of the layers in the structures shown in Figures 1A-B, such as III-N layer 120, may be performed using metal-organic chemical vapor deposition (MOCVD), molecular-beam epitaxy (MBE) chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), and/or any other suitable process as will be apparent in light of this disclosure. As previously described, III-N material, as used herein, includes a compound of one or more group III elements (e.g., aluminum, gallium, and/or indium), with nitrogen. Accordingly, III-N materials as variously used herein include, but are not limited to, GaN, InN, AlN, AlInN, AlGaIn, InGaIn, and AlInGaIn. In some embodiments, GaN may be particularly well-suited for III-N layer 120

because of its wide bandgap, high critical breakdown electric field, and high electron saturation, for example. For instance, embodiments employing GaN for the III-N layer 120 may be particularly well-suited for high-voltage and high-frequency applications, such as in the context of RF power amplifiers and low-noise amplifiers, to name some example devices. In some
5 embodiments, III-N layer 120 may have a multilayer structure including multiple III-N materials. In some embodiments, III-N layer 120 may or may not include grading (e.g., increasing and/or decreasing) the content of one or more materials in at least a portion of the layer. In some embodiments, III-N layer 120 may be doped with another material, such as with one or more suitable p-type or n-type dopants, for example. In some embodiments, III-N layer 120 may be
10 formed to have a thickness (the dimension in the Y direction) between 20 nm and 2 microns, or any other suitable thickness, as will be apparent in light of this disclosure. Note that the thickness of the III-N layer 120 may be measured as the thickness above substrate 110, above STI features 112, or above buffer layer 114, for example.

In the example structure of Figure 1A, III-N layer 120 is formed using LEO processing.
15 Such LEO processing may include, for example, forming and patterning shallow trench isolation (STI) layer on substrate 110 to form individual STI features 112 as shown and then growing the III-N layer 120 material on substrate 110 and from the openings in the STI features 112, such that defects that may be present bend or otherwise form over the STI features 112, leaving the remainder of the III-N layer 120 material suitable for transistor channel use. Such defects may
20 be present due to the growth of the III-N layer 120 material (e.g., GaN) on the substrate 110 material (e.g., Si). In such embodiments, STI 112 may include any suitable material, such as any suitable dioxide (e.g., silicon dioxide) and/or any suitable nitride (e.g., silicon nitride), to name a few examples. In the example structure of Figure 1B, III-N layer 120 is formed using buffer layer 114. In this example embodiment, buffer layer 114 may be used to assist with the
25 formation of III-N layer 120 such that layer 120 can achieve device quality. As such, buffer layer 114 may include any suitable III-N material. For instance, in the case where III-N layer 120 is GaN and substrate 110 is Si, an AlGaN or InGaN buffer layer may be used below the GaN layer to assist with ensuring the GaN layer (to be used for the n-channel material) is of a sufficient device quality, for example. In some embodiments, buffer layer 114 may have any
30 suitable thickness (the dimension in the Y direction) such as between 50 nm and 5 microns, or any other suitable thickness, as will be apparent in light of this disclosure. In some embodiments, an optional nucleation layer (not shown) may be present in the structure of Figure 1A and/or the structure of Figure 1B, where such nucleation layer would be below III-N layer 120, such as in embodiments where III-N layer 120 is formed on a non-III-V material substrate

(e.g., formed on a Si substrate). In such embodiments, the nucleation layer may be present to, for example, improve growth conditions and/or prevent the III-N layer 120 from reacting with the substrate material in an undesired manner. In some such embodiments, the nucleation layer, where present, may include a III-V or III-N material, such as AlN or a low temperature GaN layer (e.g., epitaxially grown at a temperature in the range of 700 to 950 degrees Celsius), for example. In some embodiments, the nucleation layer, where present, may have any suitable thickness (dimension in the Y direction), such as a thickness of 10 nm to 2 microns (e.g., 200nm to 1 micron), or any other suitable thickness as will be apparent in light of this disclosure.

Polarization charge inducing layer 130, in some embodiments, may be formed using any suitable techniques, as will be apparent in light of the present disclosure. In some embodiments, polarization charge inducing layer 130 may include any suitable materials, such as one or more III-V materials, and more specifically in some embodiments, one or more III-N materials, for example. In some embodiments, polarization charge inducing layer 130 may include aluminum, such that the layer includes at least one of AlN, AlGa_N, InAlN, and InAlGa_N, for instance. In some embodiments, polarization charge inducing layer 130 may increase carrier mobility in the transistor channel region (e.g., in III-N layer 120) and/or be used to form a two-dimensional electron gas (2DEG) configuration with underlying III-N layer 120, for example. Note that the 2DEG configuration is represented by dashed lines near the top of III-N layer 120, in the example structures of Figures 1A-B. In some such embodiments, polarization layer 130 may include material having a higher bandgap than the material of III-N layer 120, to form the 2DEG configuration, for example, and such a scheme may be referred to as polarization doping. For instance, in some embodiments, III-N layer 120 may include GaN and polarization charge inducing layer 130 may include AlN and/or AlGa_N, for example. In other embodiments, III-N layer 120 may include AlGa_N and polarization charge inducing layer 130 may include GaN, AlN, and/or AlGa_N, for example. In some embodiments, polarization charge inducing layer 130 may have a multilayer structure including multiple III-V materials. In some such embodiments, where the polarization layer 130 is a multilayer structure, one of the layers in the multilayer structure may be present to further increase carrier mobility in the transistor channel region and/or to improve compatibility (e.g., density of interface traps) between polarization charge inducing layer 130 and overlying layers (such as gate dielectric layer 154, in the structures of Figures 1A-B), for example. In some embodiments, polarization charge inducing layer 130 may or may not include grading (e.g., increasing and/or decreasing) the content of one or more materials in at least a portion of the layer. In some embodiments, polarization charge inducing

layer 130 may have a thickness (the dimension in the Y direction) of 0.1 to 100 nm (e.g., 0.5 to 5 nm), or any other suitable thickness, as will be apparent in light of this disclosure.

Source/drain (S/D) regions 140, in some embodiments, may be formed using any suitable techniques, as will be apparent in light of the present disclosure. For example, in some
5 embodiments, S/D regions 140 may be formed by any combination of optional patterning/masking/lithography/etching with depositing/growing/regrowing the S/D region 140 material(s), which may then be followed by a planarization and/or polish process, for instance. Note that although S/D regions 140 are shown as one continuous portion in Figures 1A-B, in some embodiments, the S/D regions 140 may include multiple portions, such as S/D material
10 adjacent to the channel region (which is the top portion of III-N layer 120) and S/D contacts above the S/D material. However, in some embodiments, the first layer of interconnect 181 may be considered S/D contacts for S/D regions 140. Regardless of the configuration, in some embodiments, the S/D material (which will be in at least a portion of the S/D region 140) may be any suitable material, such as III-V material, III-N material, and/or any other suitable material(s),
15 as will be apparent in light of this disclosure. In addition, in some embodiments, the S/D region 140 material may be doped in an n-type or p-type manner, for example, using any suitable doping techniques. In an example embodiment, S/D regions 140 may include indium and nitrogen (e.g., InN or InGaN) and be doped in an n-type manner using, e.g., Si, Se, and/or Te, with doping amounts of around 2×10^{20} per cubic cm, for instance. In some embodiments, one or
20 both of the S/D regions 140 of III-N transistor 100 may have a multilayer structure including multiple materials. In some embodiments, one or both of the S/D regions 140 may or may not include grading (e.g., increasing and/or decreasing) the content of one or more materials in at least a portion of one or both of the regions.

As previously stated, in some embodiments, S/D regions 140 may include S/D contacts. In
25 some such embodiments, S/D contacts may include any suitable material, such as a conductive metal or alloy (e.g., aluminum, tungsten, silver, nickel-platinum, or nickel-aluminum). In some embodiments, S/D contacts may include a resistance reducing metal and a contact plug metal, or just a contact plug, depending on the end use or target application. Example contact resistance reducing metals include silver, nickel, aluminum, titanium, gold, gold-germanium, nickel-
30 platinum, or nickel aluminum, and/or other such resistance reducing metals or alloys. The contact plug metal may include, for instance, aluminum, silver, nickel, platinum, titanium, or tungsten, or alloys thereof, although any suitably conductive contact metal or alloy can be used, depending on the end use or target application. In some embodiments, additional layers may be present in the S/D contact regions 140, such as adhesion layers (e.g., titanium nitride) and/or

liner or barrier layers (e.g., tantalum nitride), if so desired. Note that, in some embodiment, gate stack processing (including forming gate dielectric layer 154 and gate 152) may be performed prior to the formation of S/D regions 140, while in other embodiments, gate stack processing may be performed after the formation of S/D regions 140, for example. As can be seen in
5 Figures 1A-B, the S/D region 140 in the center of the example structures shown is electrically connected to the right-most S/D region 240 of back-end transistor 200. Depending on the end use or target application, the source or drain of transistor 100 may be connected to the source or drain of transistor 200.

In the example structure of Figure 1B, a selective wet etch process was used to form
10 notches from which the S/D regions 140 were grown. As can be seen, the notches were formed above and in the ends of the polarization layer 130 and any suitable techniques may be used to form such notches, such as using a wet etch process that selectively removes material from the interface between polarization charge inducing layer 130 and gate dielectric layer 154, for example. For instance, in an example embodiment, the selective wet etch used to form notches
15 may include an etchant of tetramethylammonium hydroxide (TMAH) and a lateral/horizontal etch direction (in the X direction) at the sides of the interface between polarization layer 130 and gate dielectric layer 154. In some such embodiments, the ledges of polarization charge inducing layer 130 exposed by the formation of the notches (e.g., exposed by performing the selective wet etch) may provide relatively high-quality surfaces from which to grow S/D region 140 material
20 and thus result in S/D material having a relatively high-quality crystalline structure. Numerous S/D configurations will be apparent in light of this disclosure and the present disclosure is not intended to be limited to any particular configuration unless otherwise stated.

Gate 152 and gate dielectric layer 154, in some embodiments, may be formed using any suitable techniques. As is also shown in Figures 1A-B, spacers 160 are adjacent to gate 152, in
25 this example embodiment, and such spacers 160 may be formed using any suitable techniques. The processing of gate dielectric layer 154, gate 152, and spacers 160 may be achieved using any suitable techniques as will be apparent in light of this disclosure, such as any suitable wet and/or dry etch processes, any suitable deposition processes such as those described herein (e.g., MBE, CVD, PVD), any suitable planarization and/or polishing processes, and so forth. In some cases,
30 gate 152 may be referred to as a gate electrode or metal gate (e.g., when gate 152 includes metal material), and generally, gate 152 and gate dielectric layer 154 may be referred to as a gate stack. Although gate dielectric layer 154 is shown located below and adjacent to spacers 160, in some embodiments, gate dielectric layer 154 material need not be present in those locations, and the material of gate dielectric layer 154 may only be located below gate 152 or be located below gate

152 and between gate 152 and spacers 160, for example. In some embodiments, gate dielectric layer 154 may be located over at least a portion of the S/D regions 140, such as is shown in Figure 1B (where gate dielectric layer 154 is over the notch portion of S/D regions), for example. In some such embodiments, such a structure may occur as a result of a blanket
5 deposition of the gate dielectric layer 154, for example.

In some embodiments, spacer material 160 may include any suitable material, such as dielectric material, oxide material (e.g., silicon oxide) and/or nitride material (e.g., silicon nitride), for example. In some embodiments, gate dielectric layer 154 may include silicon dioxide and/or high-k dielectric material, or any other suitable gate dielectric material. Example
10 high-k dielectric materials include, for instance, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate, to name some examples. In some embodiments, an annealing process may be
15 carried out on the gate dielectric layer 154 to improve its quality when a high-k material is used, for example. In some embodiments, the material of gate 152 and/or the gate contact (which may be located behind or in front of the example structure shown in Figures 1A-B) may include any suitable material, such as polysilicon, silicon nitride, silicon carbide, or various suitable metals or metal alloys, such as aluminum (Al), tungsten (W), titanium (Ti), tantalum (Ta), copper (Cu),
20 titanium nitride (TiN), or tantalum nitride (TaN), for example. In some embodiments, one or more material layers may be formed between the gate dielectric layer 154 and the gate 152 to, for example, increase the interface quality between the two features and/or to improve the electrical properties between the two features. Such intervening layers may include one or more work-function material layers, for example. In some embodiments, gate dielectric layer 154 and/or
25 gate 152 may include a multi-layer structure of two or more material layers. In some embodiments, gate dielectric layer 154 and/or gate 152 may include grading (e.g., increasing and/or decreasing) the content of one or more materials in at least a portion of the layer(s). Numerous gate stack configurations will be apparent in light of this disclosure and the present disclosure is not intended to be limited to any particular configuration unless otherwise stated.

Note that, in the example structures of Figures 1A-B, the channel region of III-N transistor 100 may be defined by the gate stack (including gate dielectric layer 154 and gate 152), such that the transistor channel is located below the gate stack. Also note that, in this example embodiment, polarization charge inducing layer 130 located above III-N layer 120 forms a two-dimensional electron gas (2DEG) configuration when the transistor is in an on state (indicated
30

with dashed lines near the top of III-N layer 120). As can be understood based on this disclosure, a 2DEG configuration includes a gas of carriers (e.g., electrons or holes) free to move in two dimensions but tightly confined in the third. Such a tight confinement can lead to quantized energy levels for motion in the third. Although 2DEG configurations include electron carriers and two-dimensional hole gas (2DHG) configurations include hole carriers, the term 2DEG will be used herein to generally refer to both carrier type configurations (both electron and hole carriers) for ease of description, unless otherwise stated. Therefore, in some instances, the 2DEG configuration locations may be considered a part of the channel region, as the 2DEG configurations (along with the channel located below the gate stack) allow charge carriers (e.g., electrons or holes) to flow from the source to the drain when the transistor is in an on state. In embodiments where III-N transistor 100 is an n-channel transistor, the carriers will be electrons and thus an actual 2DEG configuration will form. However, in some embodiments, III-N layer 120 material may be doped to achieve the proper transistor configuration, such as doping the III-N layer 120 material with a p-type dopant (e.g., using Be and/or C) to achieve an n-channel transistor, for example.

Continuing with the example structures of Figures 1A-B, back-end or BEOL processing may occur after III-N transistor 100 (which is an n-channel transistor, in these example embodiments) has been formed. Such back-end processing, in these example embodiments, includes the formation of metallization layers above the transistor 100 as well as the monolithic formation of back-end transistor 200 in the metallization layers. The metallization layers include interlayer dielectric (ILD) material (indicated by numbers in the 170s, specifically, 171-175) and interconnect material (indicated by numbers in the 180s, specifically, 181-184). Note that the different metallization layers are numbered with the last number of each feature representing the related metallization layer, such that metallization layer 1 (M1) is represented by ILD layers 171 and interconnect features 181, metallization layer 2 (M2) is represented by ILD layers 172 and interconnect features 182, and so forth. In some cases, the higher level of each same numbered layers may be considered the actual metallization layer, while the lower level of each same numbered layers may be considered the pre-metal dielectric or intra-metal dielectric through which vias are made to connect the actual metallization layers. As previously described, the first set of interconnects 181 (the set in physical contact with S/D regions 140) may be considered S/D contacts, in some instances, whereas in other instances, such S/D contacts may be included in S/D regions 140, for example. In some embodiments, ILD layers 171-175 may include any suitable material, such as dielectric material, oxide material (e.g., silicon oxide), nitride material (e.g., silicon nitride), and/or carbide material (e.g., silicon carbide), for example. In some

embodiments, interconnect features 181-184 may include any suitable electrically conductive material, such as copper (Cu), cobalt (Co), molybdenum (Mo), rhodium (Rh), beryllium (Be), chromium (Cr), manganese (Mn), aluminum (Al), silver (Ag), gold (Au), titanium (Ti), indium (In), ruthenium (Ru), palladium (Pd), tungsten (W), nickel (Ni), and/or graphene, to name a few examples. Formation of the ILD layers 171-175 and interconnect features 181-184 may be performed using any suitable techniques such as any suitable wet and/or dry etch processes, any suitable deposition processes such as those described herein (e.g., MBE, CVD, PVD), any suitable planarization and/or polishing processes, and so forth. Note that although the term interconnect is used to identify the metal features in the back-end portion (above device level 100) of the example IC structures shown in Figures 1A-B, the metal features need not connect two devices and may be included in the structure for other reasons (e.g., to generate a desired capacitance).

Back-end transistor 200, is co-integrated in the interconnect stack, in these example embodiments. Specifically, as shown in the example structures of Figures 1A-B, the back-end transistor 200 has been formed in metallization layer three (M3); however, as can be understood based on this disclosure, back-end transistor 200 could be formed in any metallization layer or in any location in the interconnect stack. In other words, the back-end transistor 200 is monolithic and thus does not require layer stacking to insert the transistor 200 in the IC structure. This is achieved, in these example embodiments, by the insertion of a thin polycrystalline or amorphous film in the interconnect stack, to enable fabrication of the back-end transistor 200 (e.g., for control logic purposes). The thin film layer may then be used for the back-end transistor 200 channel region (and may also be used, which is shown as channel 220 in Figures 1A-B, and may also be used for S/D regions 240 of the back-end transistor 200, as will be apparent in light of this disclosure. In these example embodiments, the channel region is a p-channel region (e.g., including n-type doped semiconductor material) and the thin film can be formed using any suitable techniques. For instance, in one example embodiment, the thin film may be deposited or grown onto the underlying metallization layer (e.g., using a sputtering process) and then the film may be patterned and etched to keep areas that are to be used for back-end transistors and then to form ILD material at the same level as the thin film layer (the bottom level of ILD 173, in this example case). Vias can then be formed in that ILD layer (which essentially acts as STI material for the one or more back-end transistors) to allow for the formation of interconnect features (the bottom 183 feature, in this example case). However, the present disclosure is not intended to be limited to such a blanket deposition of the thin film used for the channel region of back-end transistor 200. For example, in some embodiments, the thin film material for the channel regions

of back-end transistors may be selectively deposited in the areas where the back-end transistors are intended to be formed.

The p-channel region 220, in some embodiments, may be formed using any suitable techniques, such as those described above. In some embodiments, the material of the thin film used for the formation of the thin film utilized for p-channel region 220 may be selected based on having performance attributes that are at least similar to Si p-channel transistor devices (e.g., Hall mobility performance attributes) and a temperature budget that aligns with back-end/interconnect processing (e.g., temperature processing budget of less than 500, 450, 400, 350, or 300 °C). In some such embodiments, the thin film, and thus p-channel region 220, may include germanium (Ge), silicon germanium (SiGe), or III-Sb material. As previously described, group III-Sb material or III-Sb material, as used herein, includes a compound of one or more group III elements (e.g., aluminum, gallium, indium, boron, thallium), with antimony. Accordingly, III-Sb material as used herein includes, but is not limited to, GaSb, InSb, AlSb, AlInSb, AlGaSb, InGaSb, and AlInGaSb. In embodiments where the back-end p-channel transistor includes SiGe channel material, the concentration of Ge may be expressed as x in the representation $\text{Si}_{1-x}\text{Ge}_x$, and in some such embodiments, x may be selected to be at least 0.5, 0.6, 0.7, 0.8, or 0.9 (i.e., at least 50, 60, 70, 80, or 90 percent Ge concentration), or some other suitable threshold Ge concentration, as will be apparent in light of this disclosure. In some embodiments, p-channel region 220 may be doped with an n-type dopant, such that the channel includes hole carriers when operated. In one example embodiment, where the p-channel region 220 includes n-type doped polycrystalline Ge (poly-Ge), the hole Hall mobility for a given hole concentration exceeds even crystalline Si, and such poly-Ge based transistor devices are compatible with back-end processing thermal budgets (such as temperatures below 400 °C). In such an example embodiment, the Ge material may be n-type doped with any suitable material, such as group IV material (e.g., phosphorous and/or arsenic), or any other suitable material as will be apparent in light of the present disclosure.

In some embodiments, the thickness (dimension in the Y direction) of the thin film that is deposited to be used for p-channel region 220 (and thus the thickness of the p-channel region 220) may be in the range of 2 to 50 nm (e.g., 3 to 20 nm). As previously described, in the example structures of Figures 1A-B, back-end transistor 200 is shown having a planar configuration. However, in some embodiments, back-end transistor 200 may have a non-planar configuration, such as a finned configuration. Therefore, the thin film deposited to be used for p-channel region 220 may instead be deposited and/or formed as a fin

Source/drain (S/D) regions 240, in some embodiments, may be formed using any suitable techniques. For example, in some embodiments, S/D regions 240 may be formed via molecular doping that does not exceed the back-end thermal budget for the particular configuration (such as a thermal budget of 400 °C), which may involve adhering a self-assembled monolayer on the surface of the S/D regions 240 and driving the dopant material into the S/D regions 240 via a relatively low temperature anneal. In some embodiments, S/D regions 240 may be formed by removing portions of the thin film material layer used for the formation of p-channel region 220 and replacing them with the final S/D region 240 material. In some embodiments, S/D regions 240 may be p-type doped using any suitable dopant (which may be selected based on the primary S/D region 240 material), for example. In some embodiments, S/D regions 240 may be omitted and thus not present, resulting in the S/D region 240 being metal that makes contact directly with p-channel region 220, for example. The gate stack in back-end transistor 200, in some embodiments, may include gate dielectric layer 254 and gate 252, as shown in Figures 1A-B, and may be formed using any suitable techniques, as will be apparent in light of the present disclosure. For example, after the deposition of the thin film layer used to form p-channel 220 and optionally form S/D regions 240, an additional ILD layer (the upper level ILD 173, in this example case) may be deposited thereon and a trench may be made to allow formation of the gate stack (along with vias for formation of S/D contacts 283 and interconnect 183), for instance. The previous relevant discussion with respect to gate dielectric layer 154 is equally applicable to gate dielectric 254 and the previous relevant discussion with respect to gate 152 is equally applicable to gate 252. The previous relevant discussion of S/D contacts with respect to III-N transistor 100 is equally applicable to S/D contacts 283. Also note that the material between S/D contacts 283 and gate dielectric 254 may be a part of upper level ILD material layer 173 or it may be separate spacer material formed to help insulate gate 252 from S/D contacts 283, for example. Note that back-end transistor 200 is primarily described and depicted in the context of being a p-channel MOSFET (PMOSFET or PMOS); however, the present disclosure is not intended to be so limited. For instance, in one example embodiment, back-end transistor 200 may be a p-channel TFET (PTFET), where the p-channel region 220 is intrinsic (undoped or minimally doped), and the S/D regions 240 are oppositely type doped (e.g., one is p-type doped and the other is n-type doped). Numerous configurations of back-end transistor 200 will be apparent in light of the present disclosure.

As shown in Figures 1A-B, back-end transistor 200 (which is a p-channel transistor, in these example embodiments) is located above III-N transistor 100 (which is an n-channel transistor, in these example embodiments). In other words, back-end transistor 200 is located at

a metallization layer (and as previously described, at M3, in these example embodiments). In some embodiments, back-end transistor 200 may be at a BEOL metallization layer that is at least the second metallization layer (e.g., M2, M3, M4, M5, M6, and so forth). Further, back-end transistor 200 is above at least one interconnect layer, and that at least one interconnect layer may be in electrical contact with at least one of gate 152 and/or one of the S/D regions 140 of III-N transistor 100 (and thus, in electrical contact with at least one of the gate, the source region, and the drain region of the III-N transistor 100). As can also be seen in Figures 1A-B, one of the S/D regions 140 of III-N transistor 100 is electrically connected to one of the S/D regions 240 of back-end transistor 200, via the interconnect going vertically through the center of the structures shown (and including interconnect features 181, 182, 183, and 184, as well as S/D contact 283), in these example embodiments. Note that although back-end transistor 200 is shown as being directly above III-N transistor 100 in the example structures of Figures 1A-B, such that one cross-sectional view orthogonal to the gates 152, 252 of the transistors includes both III-N transistor 100 and back-end transistor 200, the monolithically co-integrated IC structure need not be so limited. In some embodiments, back-end transistor 200 may still be located above III-N transistor 100 (e.g., above at least one interconnect level and/or at a metallization layer of at least M1), but may not be directly above III-N transistor 100, such that two cross-sectional views may be needed to show the IC configuration. In such embodiments, the techniques may be detected by showing that the two transistors are electrically connected. Regardless of whether back-end transistor 200 is directly above or only above III-N transistor 100, back-end transistor 200 may be used for controller purposes (e.g., control logic purposes) in combination with III-N transistor 100, which may be used for voltage regulation and/or power amplifier applications (such as RF power amplification applications); however, the present disclosure is not intended to be so limited unless otherwise stated and numerous applications of the techniques and structures described herein will be apparent in light of this disclosure. Any suitable additional techniques may be performed to complete formation of one or more devices utilizing III-N transistor 100 co-integrated with back-end transistor 200, as will be apparent in light of this disclosure.

Figure 2 illustrates the example IC structure of Figure 1A, including an interlayer dielectric (ILD) hardening scheme, in accordance with an embodiment of the present disclosure. As shown in Figure 2, the structure is the same as that in Figure 1A, except that the ILD levels in the first two metallization layers of the structure of Figure 1A (ILD 171, 172) have been hardened to form hardened ILD 271, 272 and to allow for larger dielectric breakdown at a given pitch, thereby enabling greater than 5 V (and even up to hundreds of volts) to be supplied to the III-N transistor 100 that may be needed for various applications, such as for voltage regulator

applications and/or RF power amplifier applications, which may have voltage supplies of approximately 20 V or greater, for example. All other relevant discussion with reference to the example structures of Figures 1A-B is equally applicable to the example structure of Figure 2. In some embodiments, the ILD hardening scheme may be site specific to areas local to III-N transistor 100 (and any other such III-N transistors on the IC). Such hardening schemes may be implemented, in some embodiments, via radiation and/or implantation, and/or via any other suitable techniques. In some embodiments, the ILD hardening scheme may include a process where a full ILD and interconnect level is formed (e.g., one back-end layer, such as the lower layer of ILD 171 including interconnect features 181), perform patterning and resist/hardmask deposition to protect areas that are not intended to be hardened via radiation/implantation while leaving open areas to be hardened via radiation/implantation, performing the radiation/implantation, removing the resist/hardmask and continuing with the next back-end level (e.g., the upper layer of ILD 171 including interconnect features 181), and repeating as desired. In some such embodiments, the radiation/implantation may include ion implantation to cause structural damage to the ILD material being hardened using a chemically inert noble element, such as helium, neon, argon, krypton, and/or xenon, for example, or any other suitable material as will be apparent in light of this disclosure (e.g., boron, aluminum, and/or nitrogen). Further, in some such embodiments, the radiation implantation process used may be based on the ILD material being hardened. The hardened ILD may be detected via chemical analysis to detect implanted species, for example. In some embodiments, it would not be desired to harden the ILD above and local to back-end transistor 200, as such hardening may increase parasitic capacitance and thus degrade performance. Moreover, such a back-end transistor 200 may only need 1-2 V to operate effectively, which should be adequately supported by non-hardened ILD. Therefore, in some embodiments, the hardening scheme may be local to III-N transistor 100, for example. Numerous ILD hardening schemes will be apparent in light of the present disclosure.

Figure 3 illustrates the example IC structure of Figure 1A, including a back-end complementary metal-oxide-semiconductor (CMOS) device 300, in accordance with an embodiment of the present disclosure. As shown in Figure 3, the structure is the same as that in Figure 1A, except that instead of having a back-end p-channel transistor 200 (e.g., a PMOS) electrically connected to III-N transistor 100 (e.g., an NMOS), in the example structure of Figure 3, a CMOS device 300 is electrically connected to III-N transistor 100. All other relevant discussion with reference to the example structures of Figures 1A-B is equally applicable to the example structure of Figure 3. Back-end CMOS device 300, in this example embodiment, includes a p-channel transistor on the left side (which is the same as the p-channel transistor 200

in the example structures of Figures 1A-B) and an n-channel transistor on the right side. To be clear, the right n-channel transistor includes channel region 320, S/D regions 340, S/D contacts 383, gate dielectric 354, and gate 352, as shown. As can be seen, the n-channel transistor includes the same features of the p-channel transistor, with the indicating numbers of the features being in the 300s instead of the 200s, and thus, the previous discussion with respect to p-channel transistor 200 is equally applicable to the n-channel transistor in CMOS device 300 (e.g., previous relevant discussion with respect to using a thin film to form the channel region 220 is equally applicable to channel region 320, previous relevant discussion with respect to S/D regions 240 is equally applicable to S/D regions 340, and so forth). Note that although the p-channel transistor and the n-channel transistor are on the same level (e.g., both on the lower level of metallization layer M3) in the example structure of Figure 3, the present disclosure is not intended to be so limited, unless otherwise stated. For example, in some embodiments, the p-channel transistor of CMOS device 300 may be above or below the n-channel transistor.

As can be understood based on this disclosure, the n-channel transistor includes n-channel region 320 that is opposite in type relative to the p-channel region 220. For example, to form p-channel region 220, that region 220 may be n-type doped, whereas to form n-channel region 320, that region 320 may be p-type doped. In some embodiments, n-channel region 320 of the n-channel transistor may be doped with a p-type dopant, such that the channel includes electron carriers when operated. In one example embodiment, n-channel region 320 may include p-type doped polycrystalline Ge (poly-Ge). In such an example embodiment, the poly-Ge material may be p-type doped with any suitable material, such as boron, aluminum, and/or gallium, or any other suitable p-type dopant material. Likewise, the n-type poly-Ge material may be n-type doped with any suitable material, such as phosphorus, arsenic, and/or antimony, or any other suitable n-type dopant material. Further, in some embodiments, n-channel transistor may include n-type doped S/D regions 340 (which may be selected based on the primary S/D region 340 material), for example. Note that although complementary device 300 is primarily described and depicted in the context of a CMOS device, as it includes two MOSFET transistors (e.g., a PMOS and an NMOS), the present disclosure is not intended to be so limited. For instance, in an example embodiment, the complementary device may include a PTFET and an n-channel TFET (NTFET) and thus be a complementary TFET (CTFET) device. Still other embodiments may be PMOS only or NMOS only (as opposed to CMOS).

Figure 4 illustrates an example method 400 of forming an IC structure including a group III-N n-channel transistor monolithically integrated with a back-end p-channel transistor, in accordance with some embodiments of the present disclosure. Example method 400 includes

providing 410 a substrate, such as substrate 110 depicted in Figures 1A-B, 2, and 3 and described herein, for example. For instance, in some embodiments, the substrate may be a Si substrate having a <111> surface orientation, just to name an example. Example method 400 continues with forming 412 a III-N n-channel transistor at the front-end portion (or typical device location) of the substrate, such as III-N transistor 100 depicted in Figures 1A-B, 2, and 3 and described here, for example. For instance, in some embodiments, the III-N n-channel transistor may be formed by patterning shallow trench isolation (STI) material on the substrate and depositing the III-N material using lateral epitaxial overgrowth (LEO) processing (such as was done to form transistor 100 of Figure 1A) or by utilizing a buffer layer for growth of the III-N material (such as was done to form transistor 100 of Figure 1B), for example. Additional processing, such as deposition of the polarization charge inducing layer, S/D region material regrowth, gate stack processing, and any other suitable processing may occur to complete the formation of the III-N n-channel transistor at the front-end portion of the substrate. Example method 400 continues with forming 414 an interconnect layer that is in electrical contact with at least one of the gate, the source (or source region), and the drain (or drain region) of the III-N n-channel transistor. The interconnect layer may be formed by depositing interlayer dielectric (ILD) material over the III-N n-channel transistor and forming electrically conductive features (interconnects) in the ILD material, where at least one of the interconnect features is electrically in contact with the gate, the source (e.g., via a source contact), or the drain (e.g., via a drain contact). For instance, in the example IC structure of Figure 1A, the interconnect layer may be the first metallization layer (M1) including ILD 171 and interconnect features 181, where that interconnect layer is in electrical contact with both of the S/D regions 140 as shown.

Example method 400 continues with optionally hardening 416 ILD material over the III-N n-channel transistor, in accordance with some embodiments. Hardening 416 may be achieved via radiation and/or implantation as described herein. For example, as described herein with reference to Figure 2, optional hardening 416 may be performed locally on ILD material located over III-N n-channel transistor to allow for larger dielectric breakdown at a given pitch, thereby enabling increased voltages (e.g., greater than 5 V) to be supplied to the III-N transistor, which may be used for voltage regulator applications and/or RF power amplifier applications having increased voltage supplies (e.g., greater than 5 V). Note that hardening process 416 is optional because it need not be performed in some embodiments. Example method 400 continues with forming 418 p-channel transistor at the back-end portion of the substrate, thereby monolithically co-integrating the back-end p-channel transistor with the III-N n-channel transistor (as opposed to, e.g., bonding the p-channel transistor), such as back-end transistor 200 depicted in Figures

1A-B and 2 and described herein, for example. The back-end p-channel transistor may be formed by depositing a thin film layer (e.g., a Ge, SiGe, or III-Sb layer) in the interconnect stack, where the film is used for the p-channel transistor channel material, forming S/D regions, gate stack processing, and any other suitable processing to complete formation of the back-end p-channel transistor. In some embodiments, a back-end n-channel transistor may also be formed and electrically coupled with the back-end p-channel transistor to form a back-end complementary transistor configuration, such as CMOS device 300 formed in the back-end portion of the example IC structure of Figure 3. Example method 400 may then continue with completing 420 formation of a transistor-based device that utilizes III-N n-channel transistor and back-end p-channel transistor, such as completing back-end processing by forming the final metallization layer(s) or performing any other suitable processes, as can be understood based on this disclosure. For example, in some embodiments, the transistor-based device may be a voltage regulator circuit or an RF front end circuit, where the back-end p-channel transistor is used for the control logic portion of the circuit. Numerous variations and configurations will be apparent in light of this disclosure.

Example System

Figure 5 illustrates an example computing system 1000 implemented with the integrated circuit structures and/or techniques disclosed herein, in accordance with some embodiments of the present disclosure. As can be seen, the computing system 1000 houses a motherboard 1002. The motherboard 1002 may include a number of components, including, but not limited to, a processor 1004 and at least one communication chip 1006, each of which can be physically and electrically coupled to the motherboard 1002, or otherwise integrated therein. As will be appreciated, the motherboard 1002 may be, for example, any printed circuit board, whether a main board, a daughterboard mounted on a main board, or the only board of system 1000, etc.

Depending on its applications, computing system 1000 may include one or more other components that may or may not be physically and electrically coupled to the motherboard 1002. These other components may include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). Any of the components included in computing system 1000 may include one or more integrated circuit structures or devices formed using the disclosed techniques in accordance with an

example embodiment. In some embodiments, multiple functions can be integrated into one or more chips (e.g., for instance, note that the communication chip 1006 can be part of or otherwise integrated into the processor 1004).

The communication chip 1006 enables wireless communications for the transfer of data to and from the computing system 1000. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including, but not limited to, Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing system 1000 may include a plurality of communication chips 1006. For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others. In some embodiments, communication chip 1006 may include a monolithic co-integration IC structures as variously described herein.

The processor 1004 of the computing system 1000 includes an integrated circuit die packaged within the processor 1004. In some embodiments, the integrated circuit die of the processor includes onboard circuitry that is implemented with one or more integrated circuit structures or devices formed using the disclosed techniques, as variously described herein. The term “processor” may refer to any device or portion of a device that processes, for instance, electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 1006 also may include an integrated circuit die packaged within the communication chip 1006. In accordance with some such example embodiments, the integrated circuit die of the communication chip includes one or more integrated circuit structures or devices formed using the disclosed techniques as variously described herein. As will be appreciated in light of this disclosure, note that multi-standard wireless capability may be integrated directly into the processor 1004 (e.g., where functionality of any chips 1006 is integrated into processor 1004, rather than having separate communication chips). Further note that processor 1004 may be a chip set having such wireless capability. In short, any number of

processor 1004 and/or communication chips 1006 can be used. Likewise, any one chip or chip set can have multiple functions integrated therein.

In various implementations, the computing device 1000 may be a laptop, a netbook, a notebook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, a digital video recorder, or any other electronic device that processes data or employs one or more integrated circuit structures or devices formed using the disclosed techniques, as variously described herein.

Further Example Embodiments

The following examples pertain to further embodiments, from which numerous permutations and configurations will be apparent.

Example 1 is an integrated circuit (IC) including: an n-channel transistor including: a first channel layer including group III-nitride (III-N) material; a gate above the first channel layer; and source and drain regions adjacent to the first channel layer; an interconnect layer in electrical contact with at least one of the gate, the source region, and the drain region of the n-channel transistor; and a p-channel transistor including a second channel layer having a polycrystalline or amorphous structure, wherein the second channel layer is above the interconnect layer; wherein each of the n-channel transistor, interconnect layer, and p-channel transistor form a monolithic structure on a common substrate.

Example 2 includes the subject matter of Example 1, wherein the first channel layer includes gallium nitride (GaN).

Example 3 includes the subject matter of any of Examples 1-2, further including a polarization charge inducing layer above the first channel layer, wherein the polarization charge inducing layer includes material having a higher bandgap than material of the first channel layer.

Example 4 includes the subject matter of any of Examples 1-3, wherein the second channel layer is n-type doped.

Example 5 includes the subject matter of any of Examples 1-4, wherein the second channel layer includes germanium (Ge).

Example 6 includes the subject matter of any of Examples 1-4, wherein the second channel layer includes $\text{Si}_{1-x}\text{Ge}_x$ where x is greater than 0.5.

Example 7 includes the subject matter of any of Examples 1-4, wherein the second channel layer includes III-Sb material.

Example 8 includes the subject matter of any of Examples 1-7, wherein the n-channel transistor is electrically connected to the p-channel transistor.

Example 9 includes the subject matter of any of Examples 1-8, further including interlayer dielectric (ILD) material above the n-channel transistor, wherein the ILD material has been
5 hardened via at least one of radiation and implantation.

Example 10 includes the subject matter of any of Examples 1-9, wherein the second channel layer has a thickness in a vertical dimension of less than 50 nanometers.

Example 11 includes the subject matter of any of Examples 1-10, wherein the second channel layer is located at a back-end-of-line metallization layer of the IC.

10 Example 12 includes the subject matter of Example 11, wherein the metallization layer is at least the second metallization layer.

Example 13 includes the subject matter of any of Examples 1-12, further including a gate dielectric layer between the gate and the first channel layer.

Example 14 includes the subject matter of any of Examples 1-13, further including an
15 additional n-channel transistor including a third channel layer and electrically connected to the p-channel transistor to form a complementary metal-oxide-semiconductor (CMOS) device, wherein the third channel layer is above the interconnect layer.

Example 15 is a voltage regulator including the subject matter of any of Examples 1-14.

Example 16 is a radio frequency (RF) power amplifier including the subject matter of any
20 of Examples 1-14.

Example 17 is a computing system including the subject matter of any of Examples 1-14.

Example 18 is an integrated circuit (IC) including: a first transistor including: a first channel layer including group III-nitride (III-N) material; a polarization charge inducing layer above the first channel layer, wherein the polarization charge inducing layer includes material
25 having a higher bandgap than material of the first channel layer; a gate above the polarization charge inducing layer; a gate dielectric layer between the polarization charge inducing layer and the gate; and source and drain regions adjacent to the first channel layer; and a second transistor including a second channel layer having a polycrystalline or amorphous structure, wherein the second channel layer includes at least one of germanium (Ge), silicon germanium ($\text{Si}_{1-x}\text{Ge}_x$)
30 where x is greater than 0.5, and group III-antimonide (III-Sb) material, and wherein the second channel layer is located at a back-end-of-line metallization layer of the IC; wherein the first transistor and second transistor form a monolithic structure on a common substrate.

Example 19 includes the subject matter of Example 18, wherein the first channel layer includes gallium nitride (GaN).

Example 20 includes the subject matter of any of Examples 18-19, wherein the first transistor is an n-channel transistor and the second transistor is a p-channel transistor.

5 Example 21 includes the subject matter of any of Examples 18-20, wherein the second channel layer is n-type doped.

Example 22 includes the subject matter of any of Examples 18-21, wherein the second channel layer includes Ge.

10 Example 23 includes the subject matter of any of Examples 18-21, wherein the second channel layer includes $\text{Si}_{1-x}\text{Ge}_x$ where x is greater than 0.5.

Example 24 includes the subject matter of any of Examples 18-21, wherein the second channel layer includes III-Sb material.

Example 25 includes the subject matter of any of Examples 18-24, wherein the first transistor is electrically connected to the second transistor.

15 Example 26 includes the subject matter of any of Examples 18-25, further including interlayer dielectric (ILD) material above the first transistor, wherein the ILD material has been hardened via at least one of radiation and implantation.

Example 27 includes the subject matter of any of Examples 18-26, wherein the second channel layer has a thickness in a vertical dimension of less than 30 nanometers.

20 Example 28 includes the subject matter of any of Examples 18-27, wherein the second channel layer is located above an interconnect layer in electrical contact with at least one of the gate, the source region, and the drain region of the first transistor.

Example 29 includes the subject matter of any of Examples 18-28, wherein the metallization layer is at least the second metallization layer.

25 Example 30 includes the subject matter of any of Examples 18-29, wherein the common substrate is a silicon (Si) substrate having a surface orientation of $\langle 111 \rangle$.

Example 31 includes the subject matter of any of Examples 18-30, further including a third transistor including a third channel layer and electrically connected to the second transistor to form a complementary metal-oxide-semiconductor (CMOS) device, wherein the third channel
30 layer is located at a back-end-of-line metallization layer of the IC.

Example 32 is a voltage regulator including the subject matter of any of Examples 18-31.

Example 33 is a radio frequency (RF) power amplifier including the subject matter of any of Examples 18-31.

Example 34 is a computing system including the subject matter of any of Examples 18-31.

Example 35 is a method of forming an integrated circuit (IC), the method including:
5 forming an n-channel transistor including: a first channel layer including group III-nitride (III-N) material; a gate above the first channel layer; and source and drain regions adjacent to the first channel layer; forming an interconnect layer in electrical contact with at least one of the gate, the source region, and the drain region of the n-channel transistor; and forming a p-channel transistor including a second channel layer having a polycrystalline or amorphous structure, wherein the
10 second channel layer is above the interconnect layer; wherein each of the n-channel transistor, interconnect layer, and p-channel transistor form a monolithic structure on a common substrate.

Example 36 includes the subject matter of Example 35, wherein the second channel layer is formed by depositing a film on an underlying metallization layer during back-end-of-line (BEOL) processing of the IC.

15 Example 37 includes the subject matter of any of Examples 35-36, further including depositing interlayer dielectric (ILD) material above the n-channel transistor and performing at least one of radiation and implantation to harden the ILD material.

Example 38 includes the subject matter of any of Examples 35-37, further including forming an additional n-channel transistor including a third channel layer and electrically
20 connected to the p-channel transistor to form a complementary metal-oxide-semiconductor (CMOS) device, wherein the third channel layer is above the interconnect layer.

Example 39 includes the subject matter of any of Examples 35-38, wherein the first channel layer includes gallium nitride (GaN).

Example 40 includes the subject matter of any of Examples 35-39, further including
25 forming a polarization charge inducing layer above the first channel layer, wherein the polarization charge inducing layer includes material having a higher bandgap than material of the first channel layer.

Example 41 includes the subject matter of any of Examples 35-40, wherein the second channel layer is n-type doped.

30 Example 42 includes the subject matter of any of Examples 35-41, wherein the second channel layer includes germanium (Ge).

Example 43 includes the subject matter of any of Examples 35-41, wherein the second channel layer includes silicon germanium ($\text{Si}_{1-x}\text{Ge}_x$) where x is greater than 0.5.

Example 44 includes the subject matter of any of Examples 35-41, wherein the second channel layer includes group III-antimonide (III-Sb) material.

5 Example 45 includes the subject matter of any of Examples 35-44, wherein the n-channel transistor is electrically connected to the p-channel transistor.

Example 46 includes the subject matter of any of Examples 35-45, wherein the second channel layer has a thickness in a vertical dimension of less than 50 nanometers.

10 Example 47 includes the subject matter of any of Examples 35-46, wherein the second channel layer is formed at a back-end-of-line metallization layer of the IC.

Example 48 includes the subject matter of any of Examples 35-47, further including forming a gate dielectric layer between the gate and the first channel layer.

15 The foregoing description of example embodiments has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit this disclosure to the precise forms disclosed. Many modifications and variations are possible in light of this disclosure. It is intended that the scope of this disclosure be limited not by this detailed description, but rather by the claims appended hereto. Future filed applications claiming priority to this application may claim the disclosed subject matter in a different manner, and may generally include any set of one or more limitations as variously disclosed or otherwise
20 demonstrated herein.

CLAIMS

What is claimed is:

1. An integrated circuit (IC) comprising:
an n-channel transistor including:
 - 5 a first channel layer including group III-nitride (III-N) material;
 - a gate above the first channel layer; and
 - source and drain regions adjacent to the first channel layer;
an interconnect layer in electrical contact with at least one of the gate, the source region,
and the drain region of the n-channel transistor; and
 - 10 a p-channel transistor including a second channel layer having a polycrystalline or
amorphous structure, wherein the second channel layer is above the interconnect
layer;
wherein each of the n-channel transistor, interconnect layer, and p-channel transistor
form a monolithic structure on a common substrate.
- 15 2. The IC of claim 1, wherein the first channel layer includes gallium nitride (GaN).
3. The IC of claim 1, further comprising a polarization charge inducing layer above
the first channel layer, wherein the polarization charge inducing layer includes material having a
higher bandgap than material of the first channel layer.
4. The IC of claim 1, wherein the second channel layer is n-type doped.
- 20 5. The IC of claim 1, wherein the second channel layer includes germanium (Ge).
6. The IC of claim 1, wherein the second channel layer includes silicon germanium
(Si_{1-x}Ge_x) where x is greater than 0.5.
7. The IC of claim 1, wherein the second channel layer includes group III-
antimonide (III-Sb) material.
- 25 8. The IC of claim 1, wherein the n-channel transistor is electrically connected to the
p-channel transistor.

9. The IC of claim 1, further comprising interlayer dielectric (ILD) material above the n-channel transistor, wherein the ILD material has been hardened via at least one of radiation and implantation.

10. The IC of claim 1, wherein the second channel layer has a thickness in a vertical dimension of less than 50 nanometers.

11. The IC of claim 1, wherein the second channel layer is located at a back-end-of-line metallization layer of the IC.

12. The IC of claim 11, wherein the metallization layer is at least the second metallization layer.

13. The IC of claim 1, further comprising a gate dielectric layer between the gate and the first channel layer.

14. The IC of claim 1, further comprising an additional n-channel transistor including a third channel layer and electrically connected to the p-channel transistor to form a complementary metal-oxide-semiconductor (CMOS) device, wherein the third channel layer is above the interconnect layer.

15. A voltage regulator including the IC of any of claims 1-14.

16. A radio frequency (RF) power amplifier including the IC of any of claims 1-14.

17. A computing system including the IC of any of claims 1-14.

18. An integrated circuit (IC) comprising:
a first transistor including:
a first channel layer including group III-nitride (III-N) material;
a polarization charge inducing layer above the first channel layer, wherein the polarization charge inducing layer includes material having a higher bandgap than material of the first channel layer;
a gate above the polarization charge inducing layer;
a gate dielectric layer between the polarization charge inducing layer and the gate;
and
source and drain regions adjacent to the first channel layer; and

a second transistor including a second channel layer having a polycrystalline or amorphous structure, wherein the second channel layer includes at least one of germanium (Ge), silicon germanium ($\text{Si}_{1-x}\text{Ge}_x$) where x is greater than 0.5, and group III-antimonide (III-Sb) material, and wherein the second channel layer is located at a back-end-of-line metallization layer of the IC;

wherein the first transistor and second transistor form a monolithic structure on a common substrate.

19. The IC of claim 18, wherein the first transistor is electrically connected to the second transistor.

20. The IC of claim 18, wherein the second channel layer has a thickness in a vertical dimension of less than 30 nanometers.

21. The IC of claim 18, wherein the metallization layer is at least the second metallization layer.

22. The IC of any of claims 18-21, wherein the common substrate is a silicon (Si) substrate having a surface orientation of $\langle 111 \rangle$.

23. A method of forming an integrated circuit (IC), the method comprising:
forming an n-channel transistor including:

a first channel layer including group III-nitride (III-N) material;

a gate above the first channel layer; and

source and drain regions adjacent to the first channel layer;

forming an interconnect layer in electrical contact with at least one of the gate, the source region, and the drain region of the n-channel transistor; and

forming a p-channel transistor including a second channel layer having a polycrystalline or amorphous structure, wherein the second channel layer is above the interconnect layer;

wherein each of the n-channel transistor, interconnect layer, and p-channel transistor form a monolithic structure on a common substrate.

24. The method of claim 23, wherein the second channel layer is formed by depositing a film on an underlying metallization layer during back-end-of-line (BEOL) processing of the IC.

25. The method of any of claims 23-24, further comprising depositing interlayer
5 dielectric (ILD) material above the n-channel transistor and performing at least one of radiation and implantation to harden the ILD material.

1/6

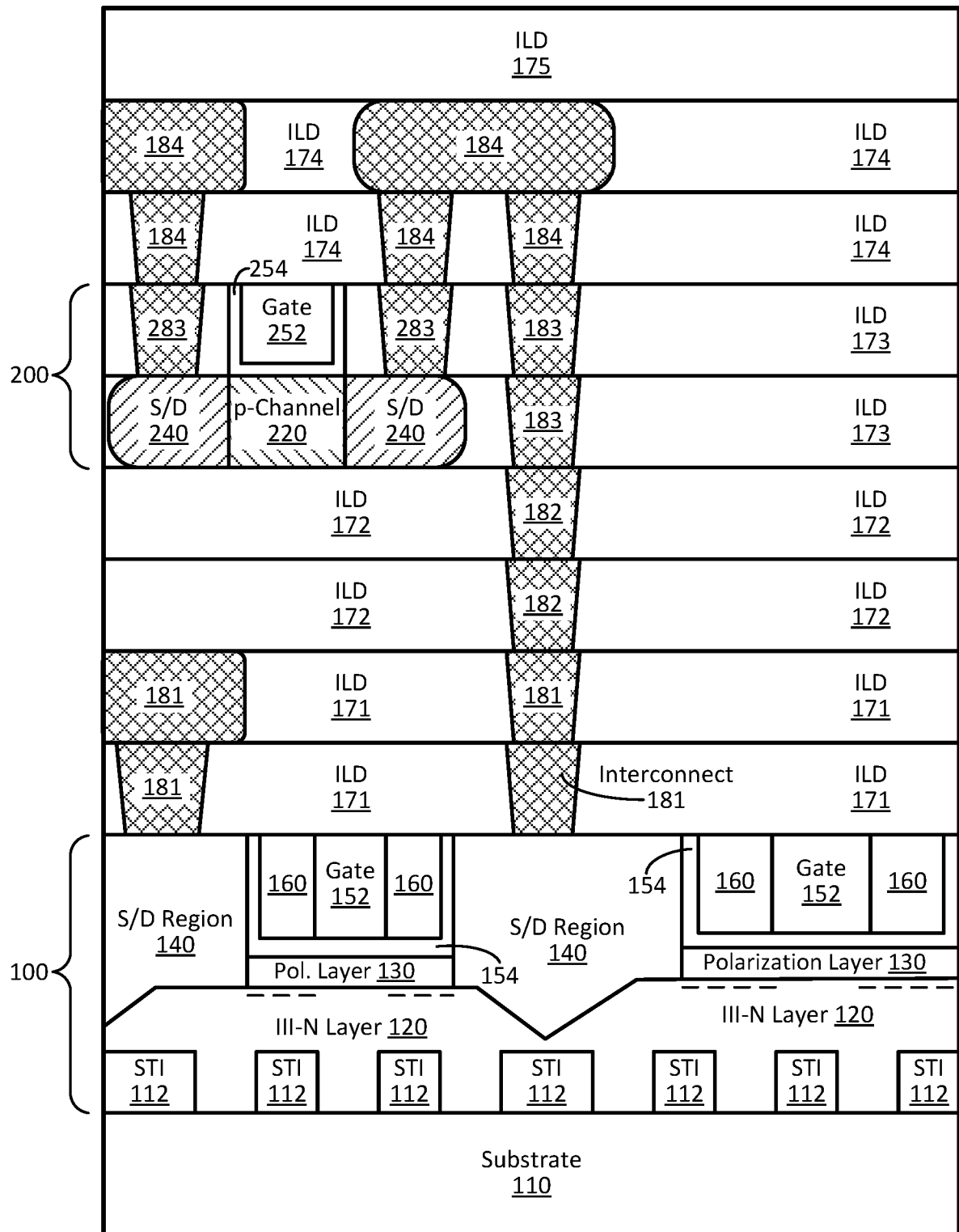
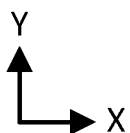


FIG. 1A



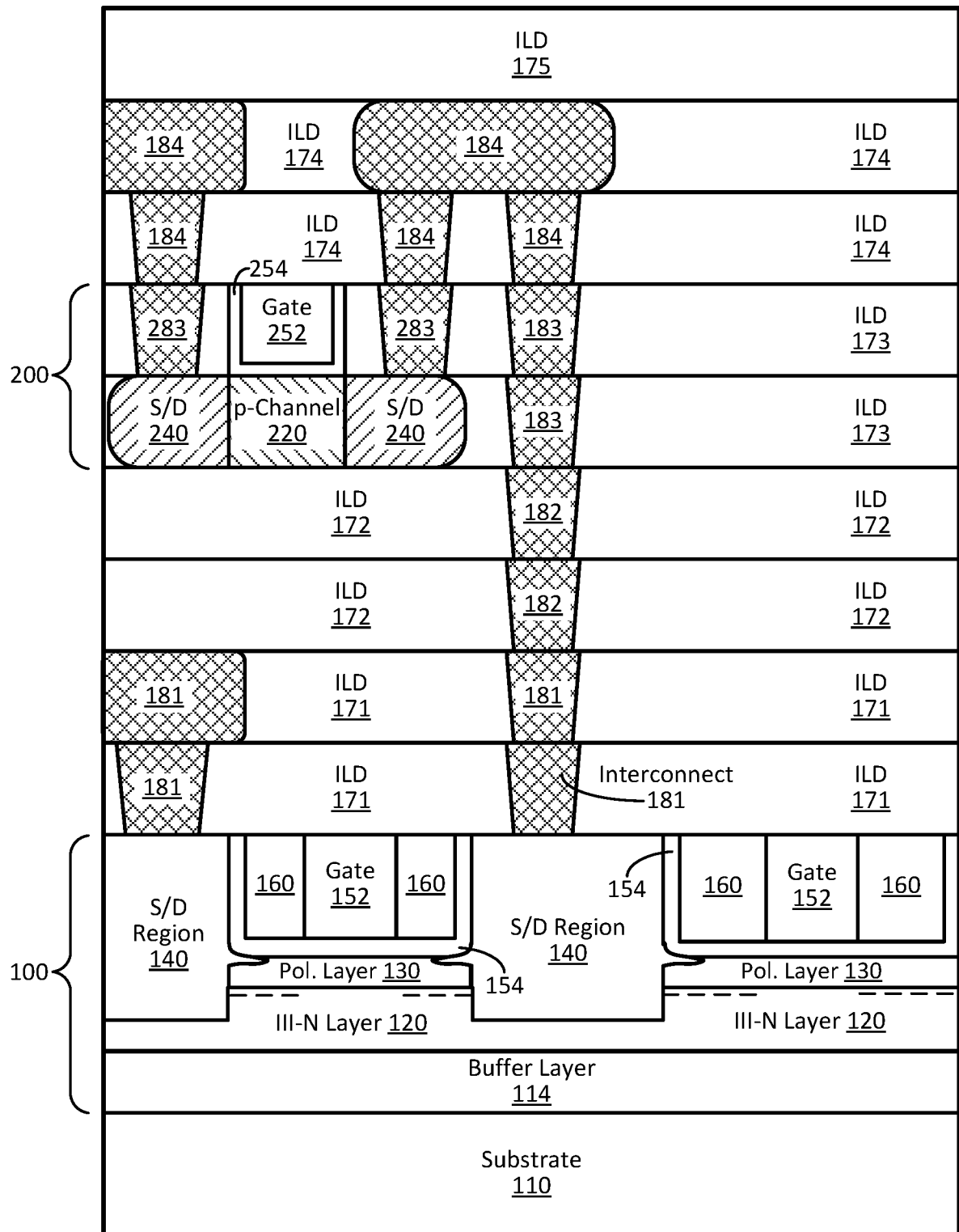
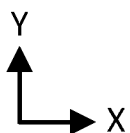


FIG. 1B



3/6

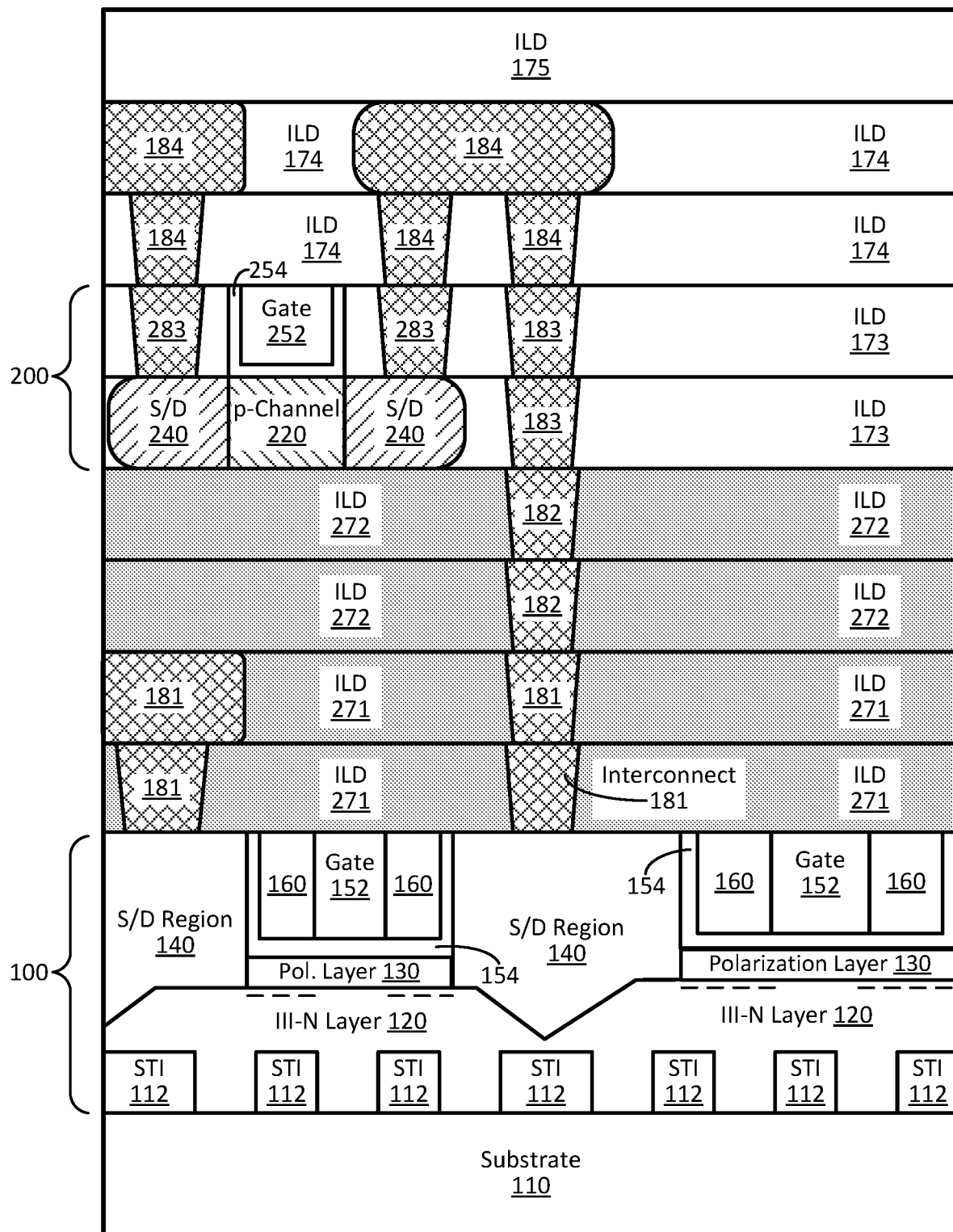


FIG. 2

4/6

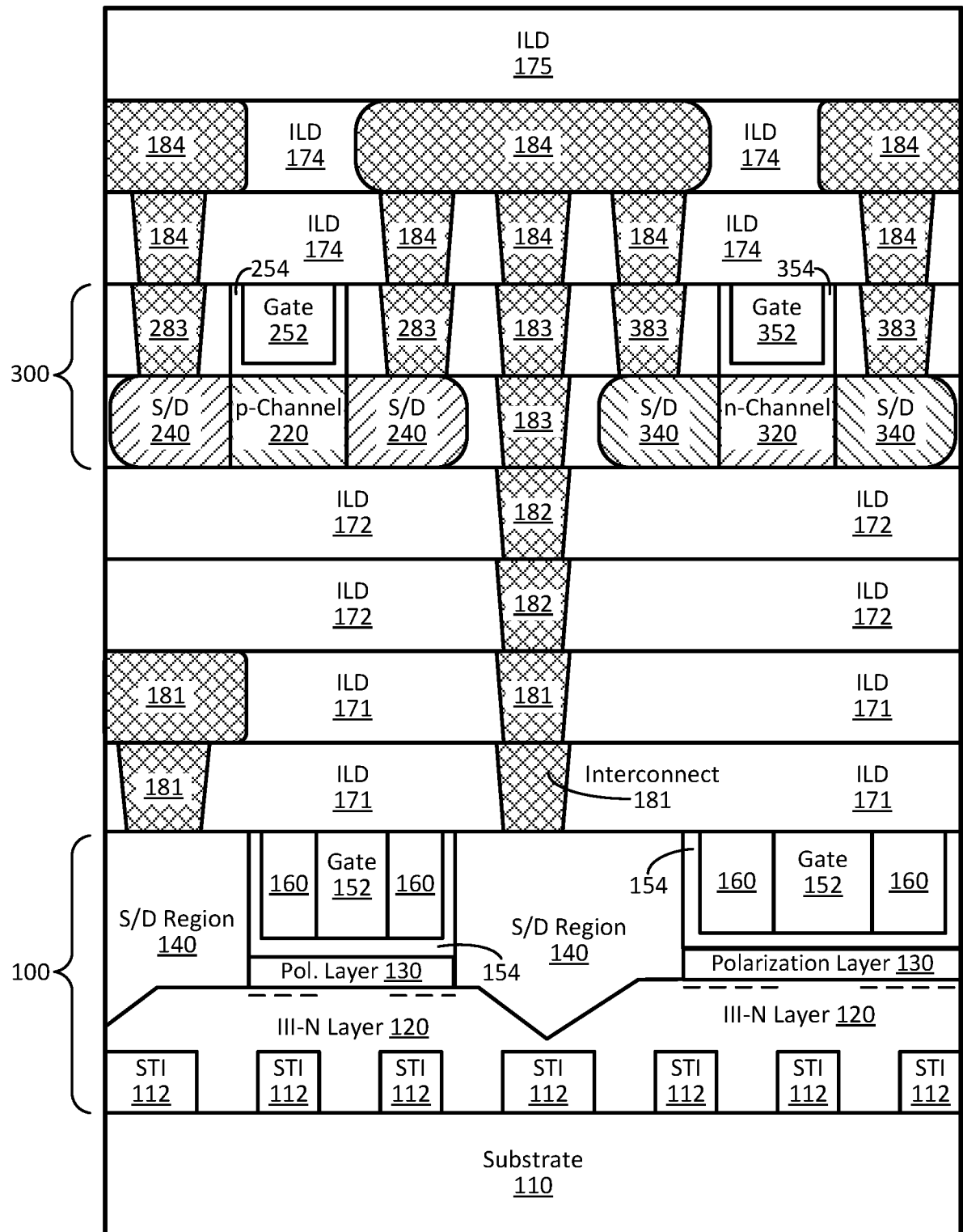
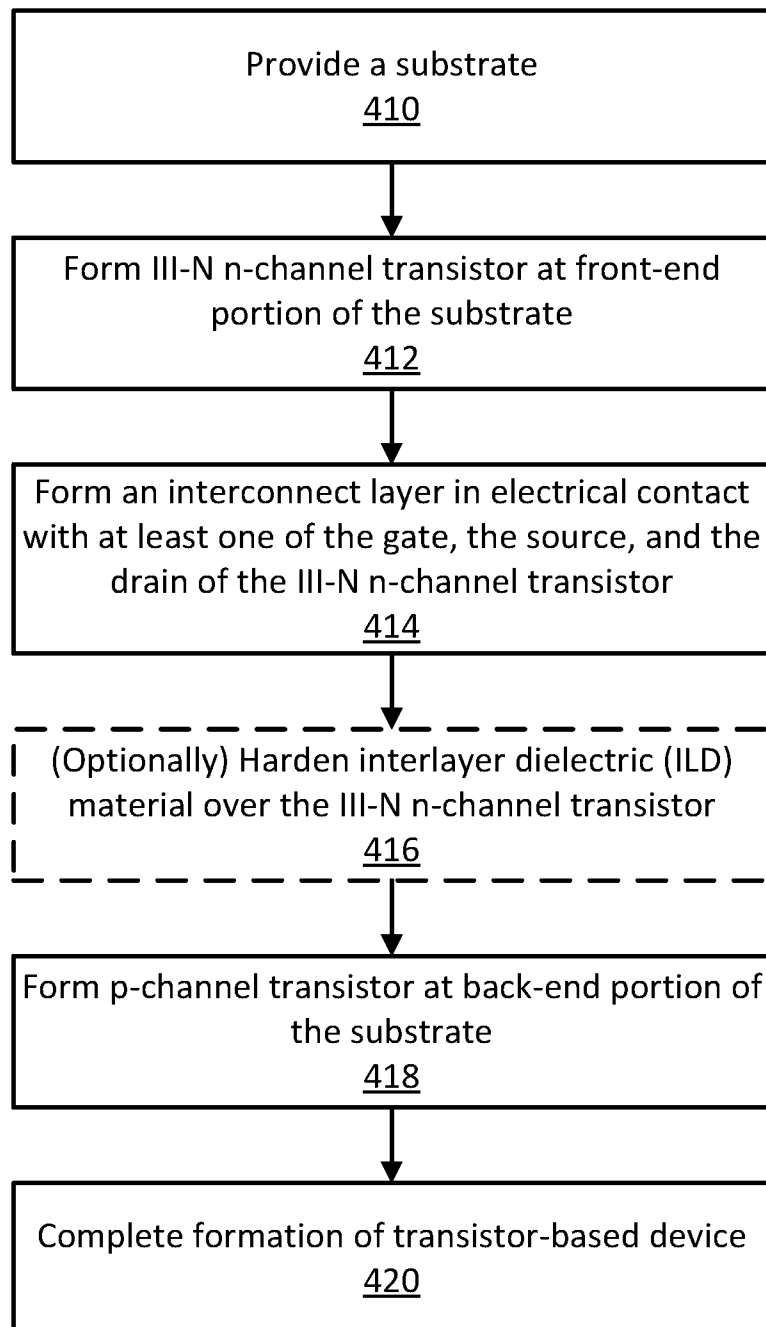


FIG. 3

5/6

Method
400 →**FIG. 4**

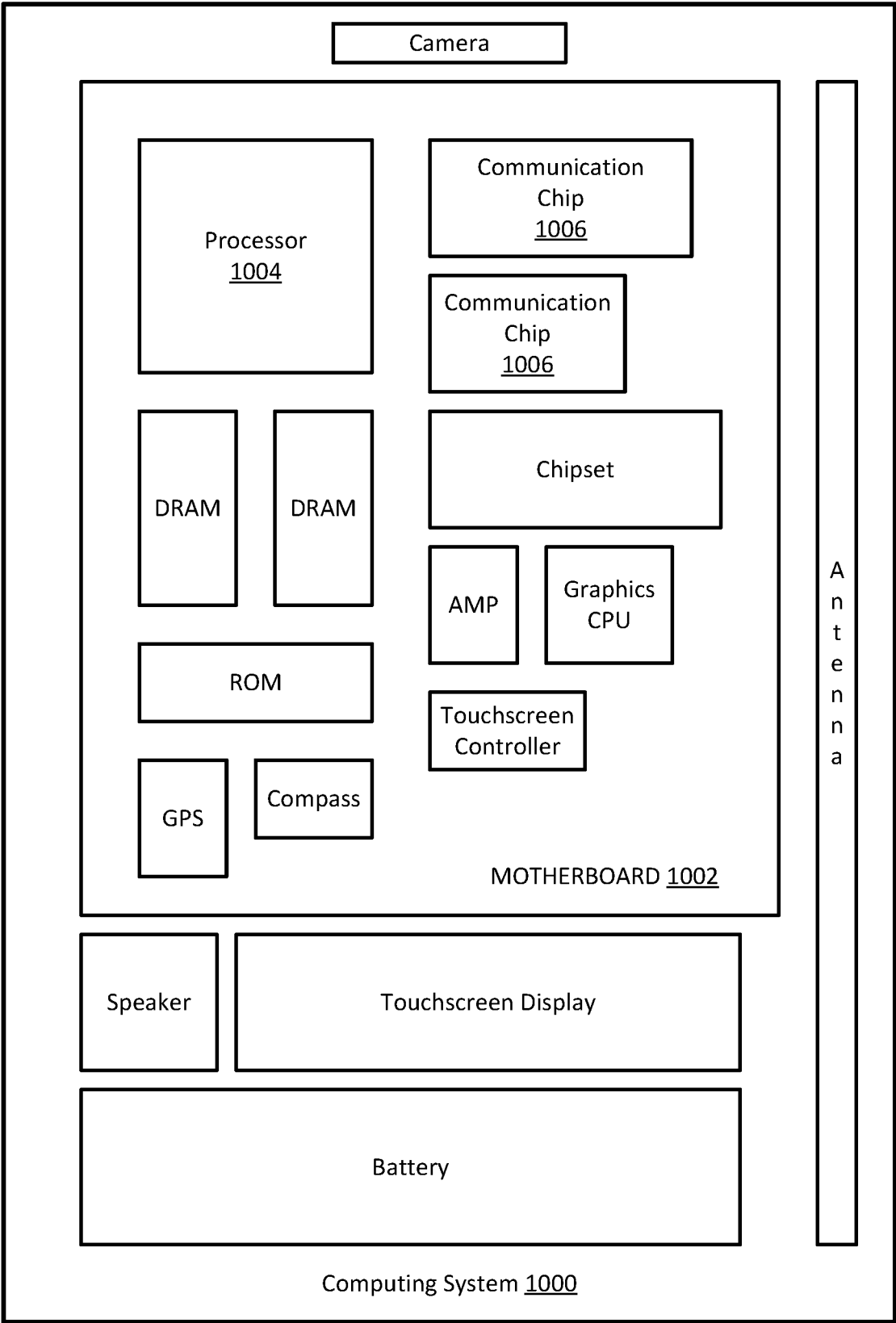


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/036396**A. CLASSIFICATION OF SUBJECT MATTER****H01L 27/092(2006.01)i, H01L 21/8249(2006.01)i, H01L 29/66(2006.01)i, H01L 29/78(2006.01)i, H01L 21/8238(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/092; H01L 21/336; H01L 21/4763; H01L 29/04; H01L 23/544; H01L 29/205; H01L 29/66; H01L 29/775; H01L 21/8249; H01L 29/78; H01L 21/8238

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: transistor, polycrystalline, amorphous, BEOL

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014-0145272 A1 (MONOLITHIC 3D INC.) 29 May 2014 See abstract, paragraphs [0072]-[0077], [0246] and figures 1-5, 42D.	1-2, 4-17, 23, 25
Y		3, 18-22, 24
Y	US 2014-0094223 A1 (SANSAPTAK DASGUPTA et al.) 03 April 2014 See paragraphs [0017]-[0039] and figures 1A-2B.	3, 18-22
Y	KR 10-0305402 B1 (SK HYNIX INC.) 02 November 2001 See page 3 and figures 3-6.	24
A	US 2009-0114903 A1 (AMOL M. KALBURGE) 07 May 2009 See paragraphs [0013]-[0020] and figures 1-10.	1-25
A	US 2005-0110159 A1 (CHANG-WOO OH et al.) 26 May 2005 See paragraphs [0025]-[0032] and figures 1-5.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

06 March 2017 (06.03.2017)

Date of mailing of the international search report

06 March 2017 (06.03.2017)

Name and mailing address of the ISA/KR

International Application Division

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/036396

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014-0145272 A1	29/05/2014	US 8742476 B1	03/06/2014
US 2014-0094223 A1	03/04/2014	CN 104603912 A	06/05/2015
		EP 2901471 A1	05/08/2015
		EP 2901471 A4	18/05/2016
		KR 10-2015-0038225 A	08/04/2015
		TW 201431067 A	01/08/2014
		TW 201611279 A	16/03/2016
		TW I506780 B	01/11/2015
		WO 2014-051779 A1	03/04/2014
KR 10-0305402 B1	02/11/2001	KR 10-2000-0045456 A	15/07/2000
US 2009-0114903 A1	07/05/2009	KR 10-2010-0051595 A	17/05/2010
		TW 200913276 A	16/03/2009
		WO 2009-023349 A2	19/02/2009
		WO 2009-023349 A3	24/09/2009
US 2005-0110159 A1	26/05/2005	KR 10-0574957 B1	28/04/2006
		KR 10-2005-0049101 A	25/05/2005