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(54) **SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF**

(71) Applicant: **TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.**, Hsinchu (TW)

(72) Inventors: **JIA-YOU TSAI**, TAIPEI CITY (TW); **KUNG-WEI LEE**, NEW TAIPEI CITY (TW)

(73) Assignee: **TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.**, Hsinchu (TW)

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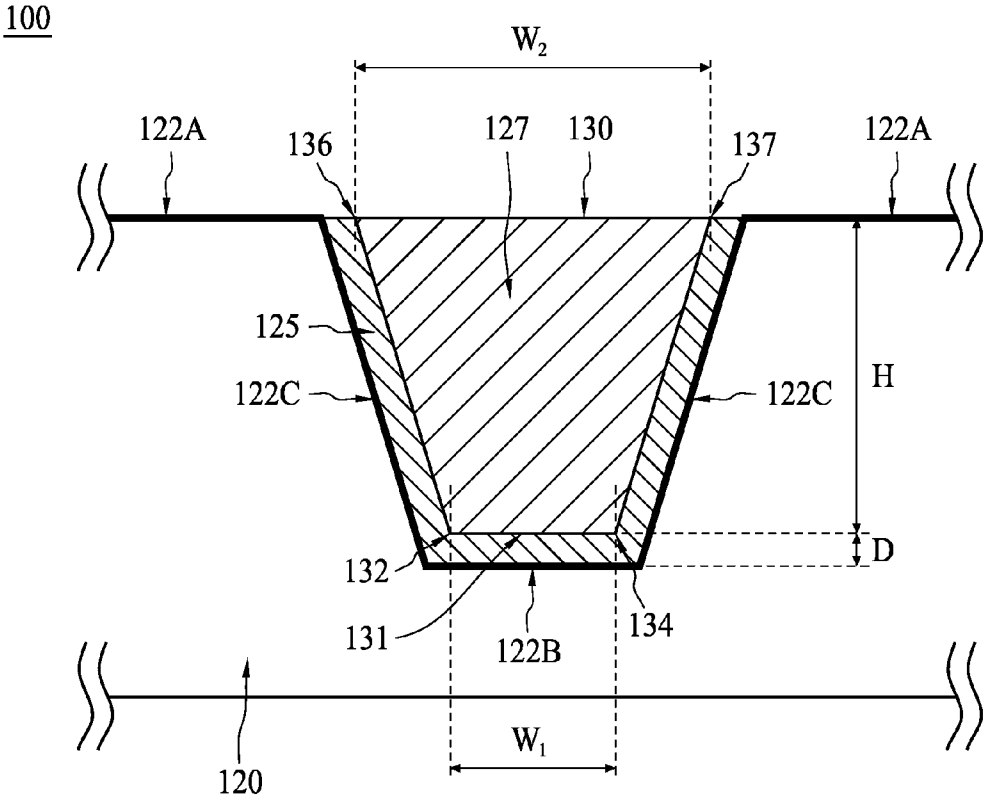
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USPC ..... **257/510**; 438/437

(57) **ABSTRACT**

A semiconductor structure includes a surface having a plurality of portions and a dielectric material over the surface. The dielectric material includes an aspect ratio substantially equal to or greater than a predetermined value.



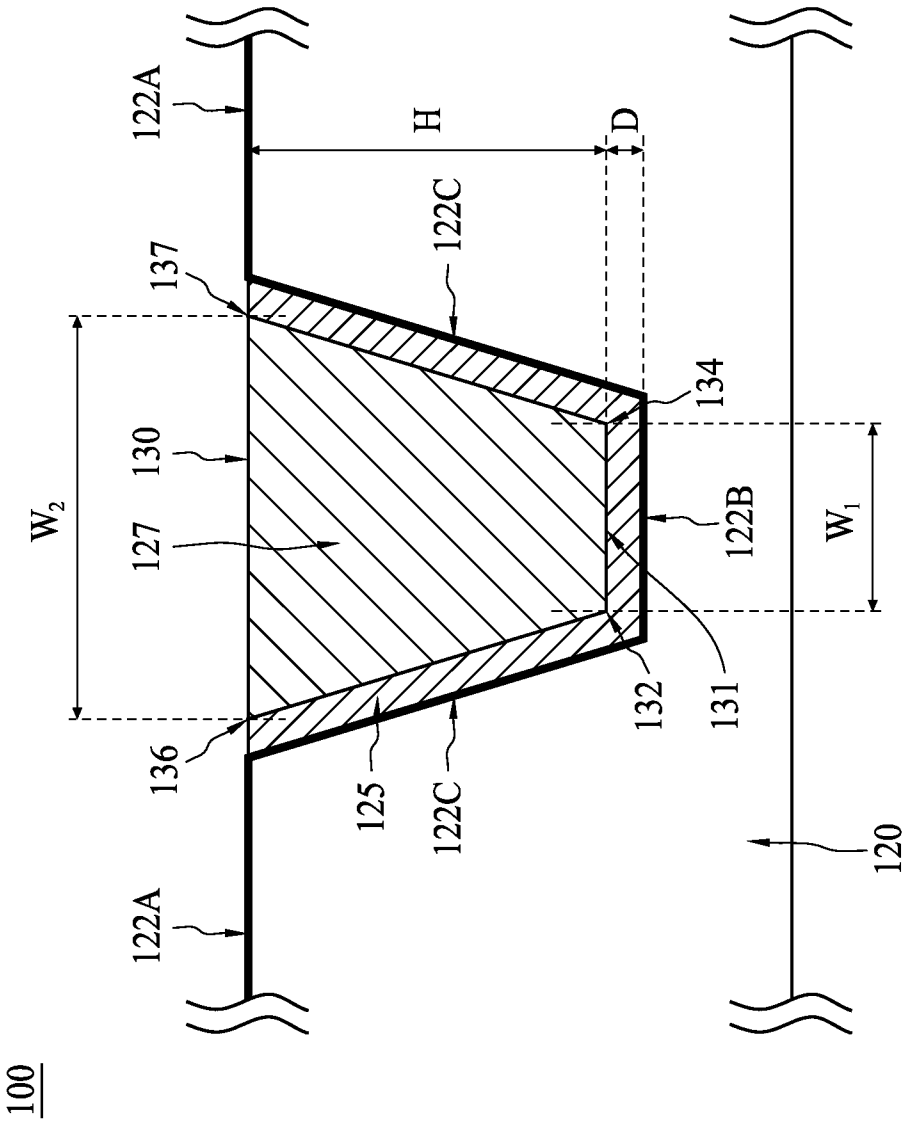

100
122A
H
D
122C
137
134
130
$W_2$
127
122B
$W_1$
132
131
136
125
122C
120
122A

FIG. 1

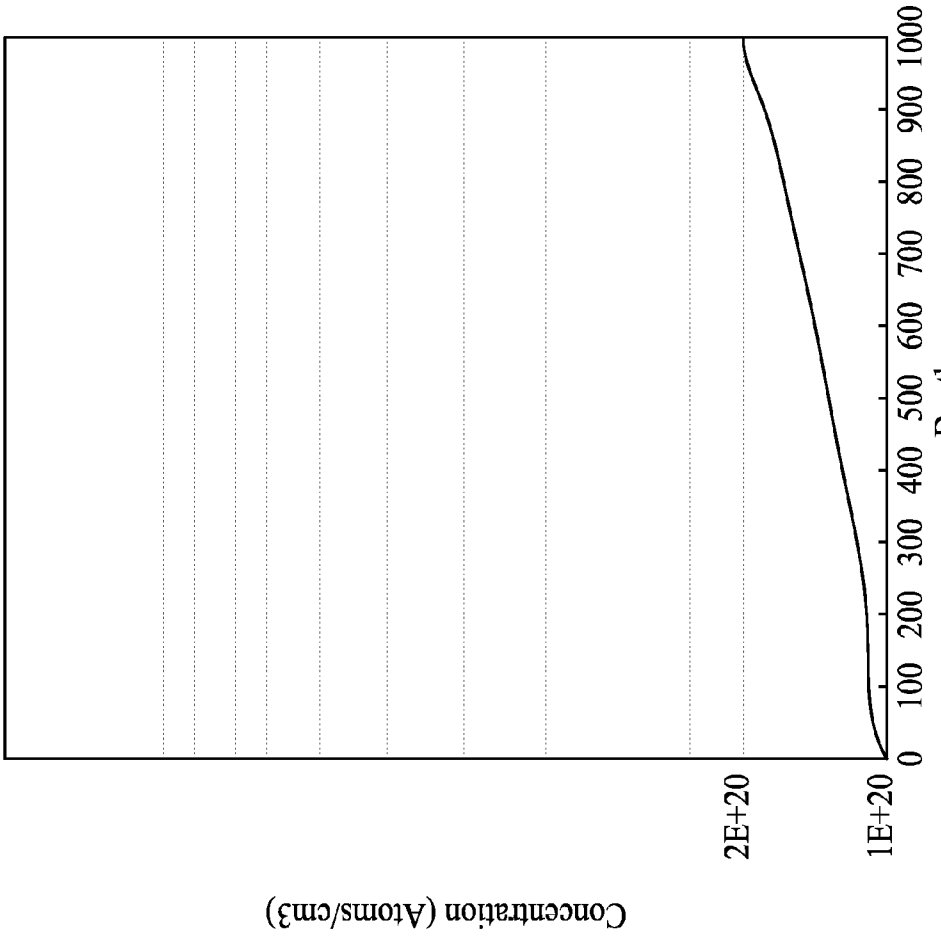

Concentration (Atoms/cm3)
2E+20
1E+20
0
100
200
300
400
500
600
700
800
900
1000
Depth

FIG. 2

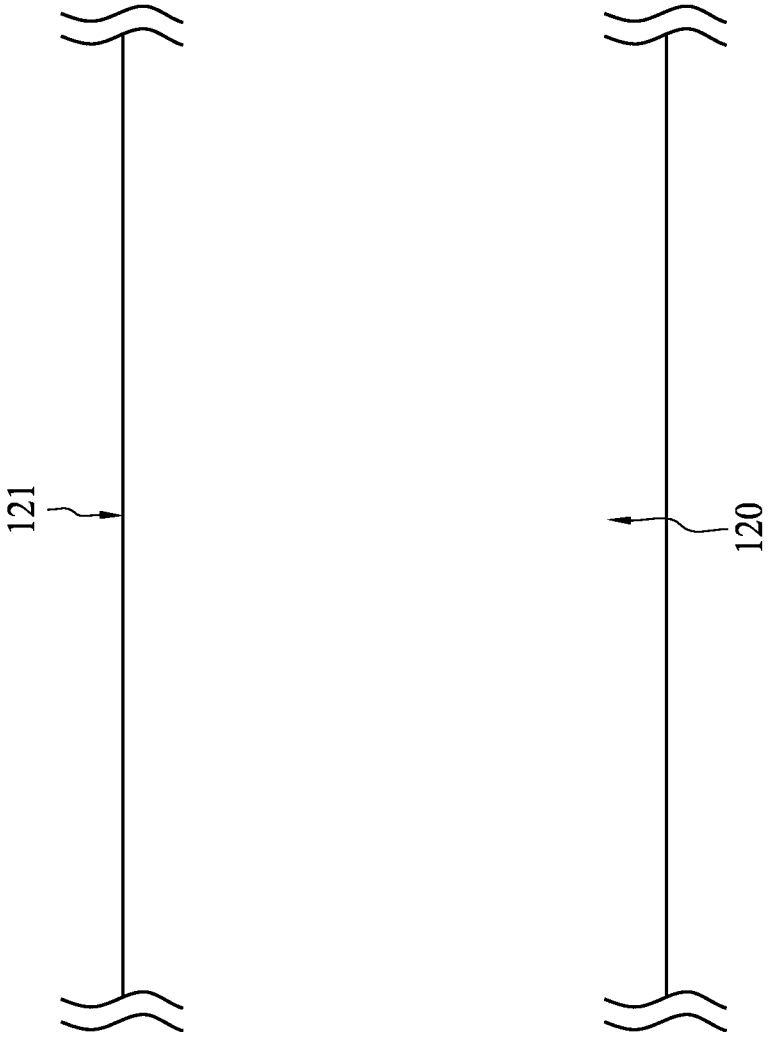



FIG. 3A

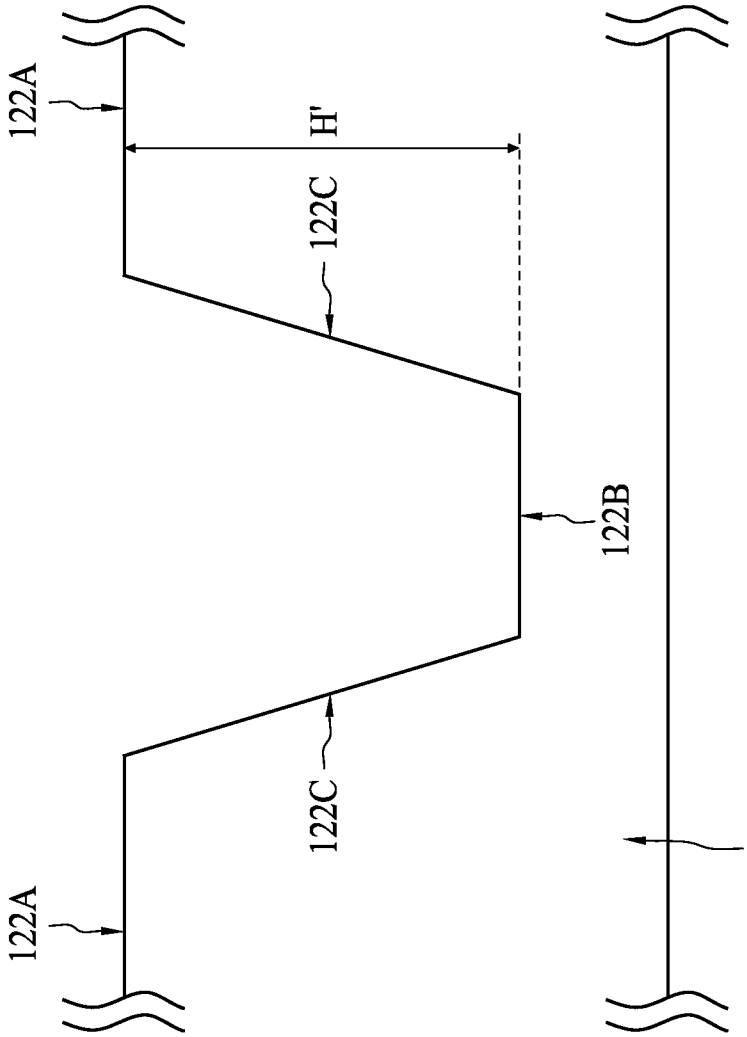



FIG. 3B

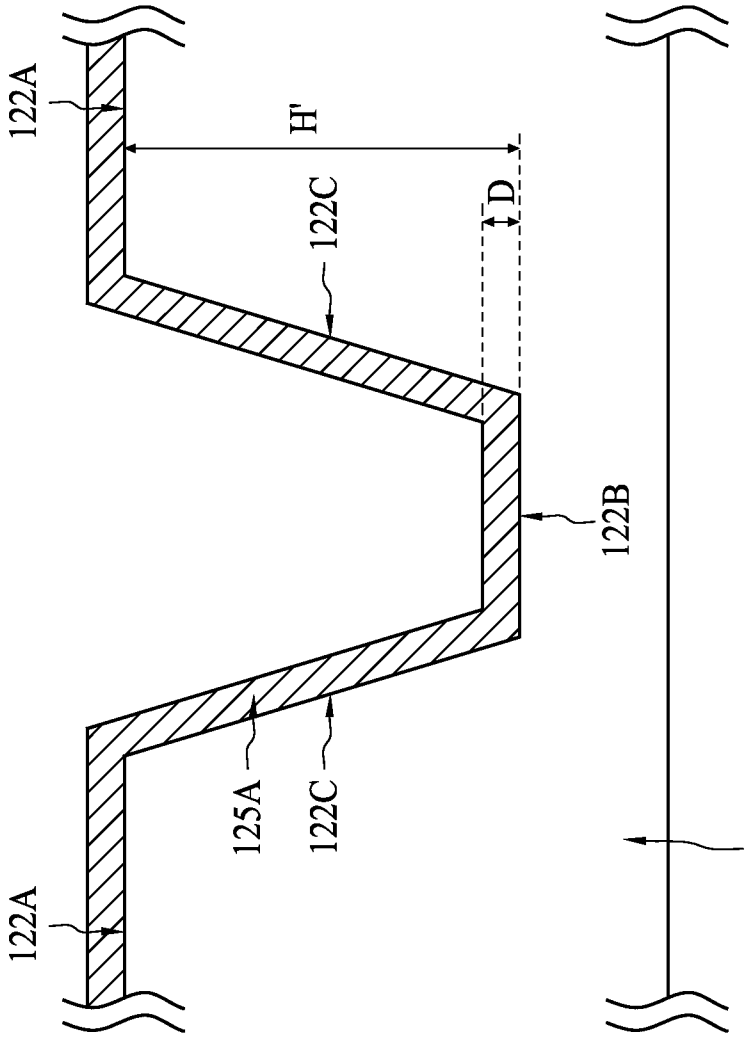



FIG. 3C

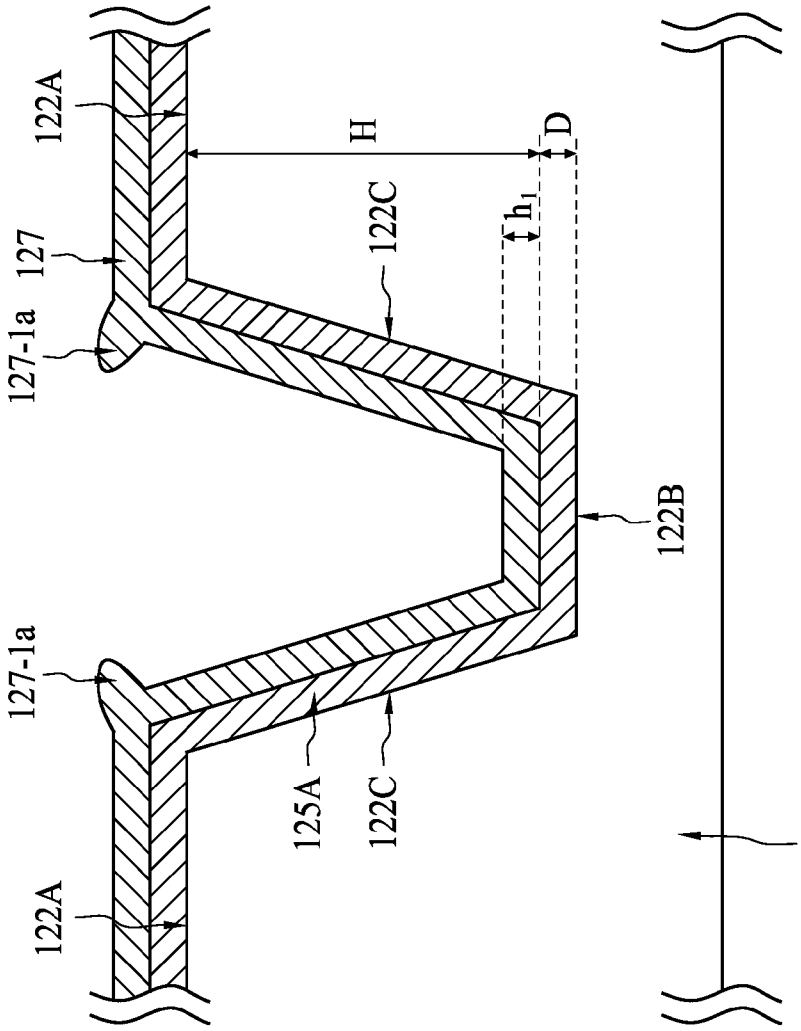



FIG. 3D

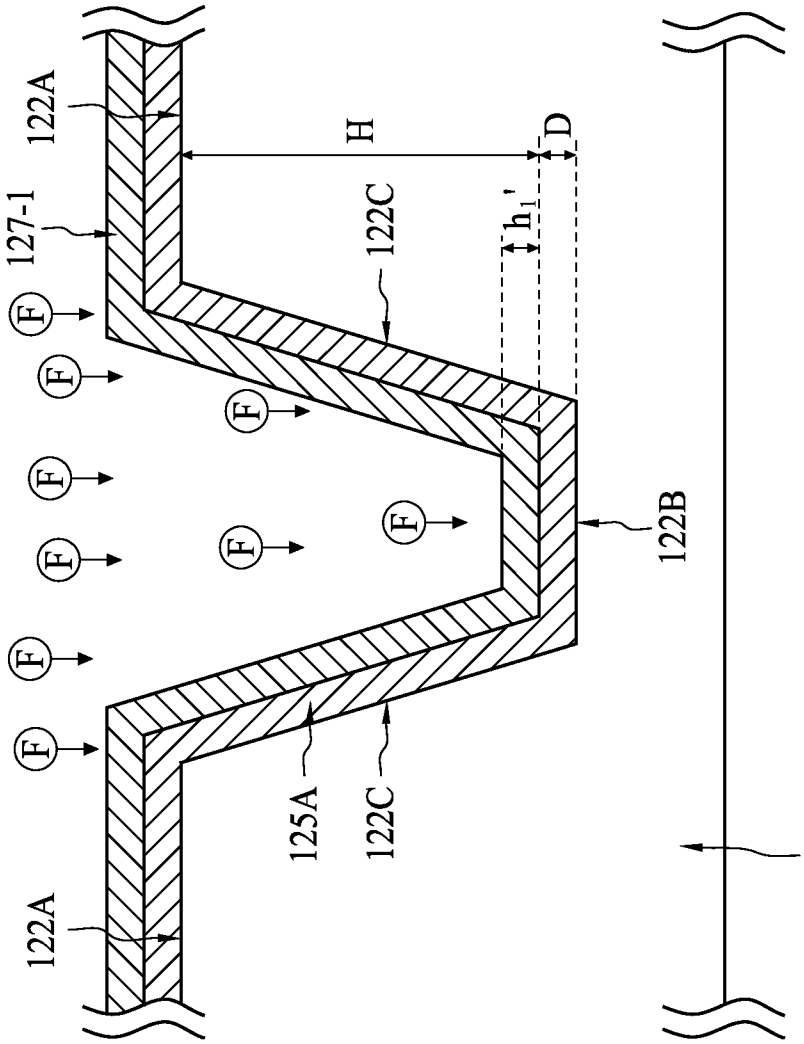



FIG. 3E

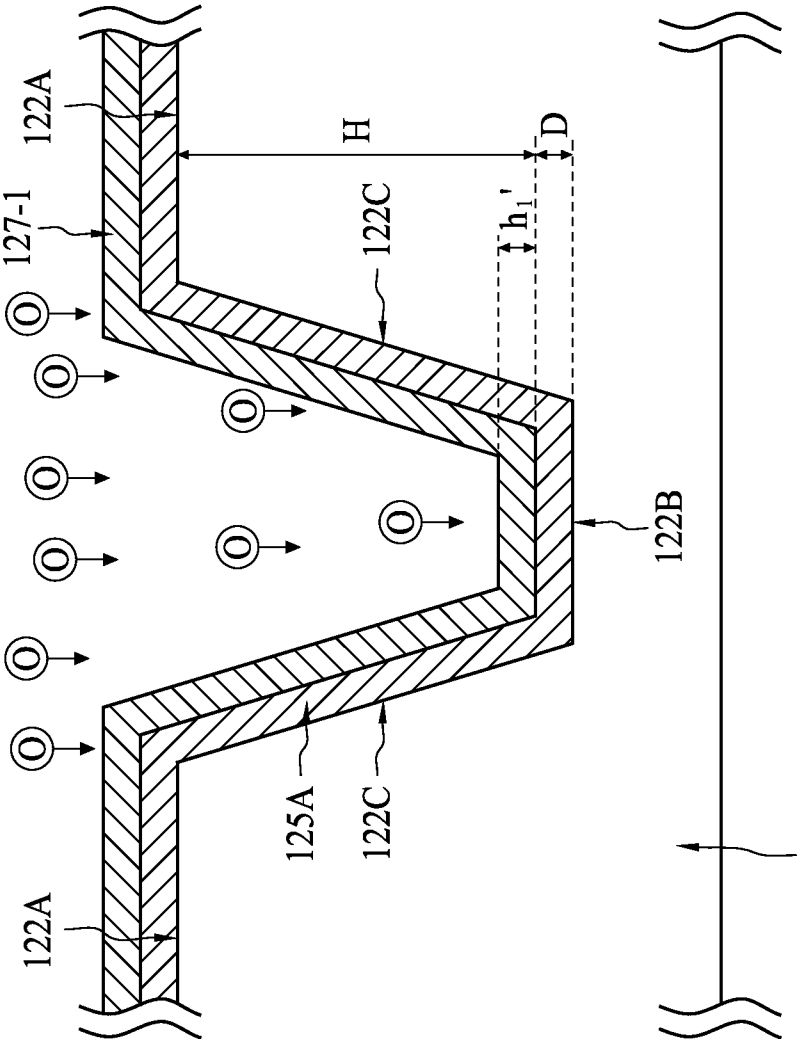



FIG. 3F

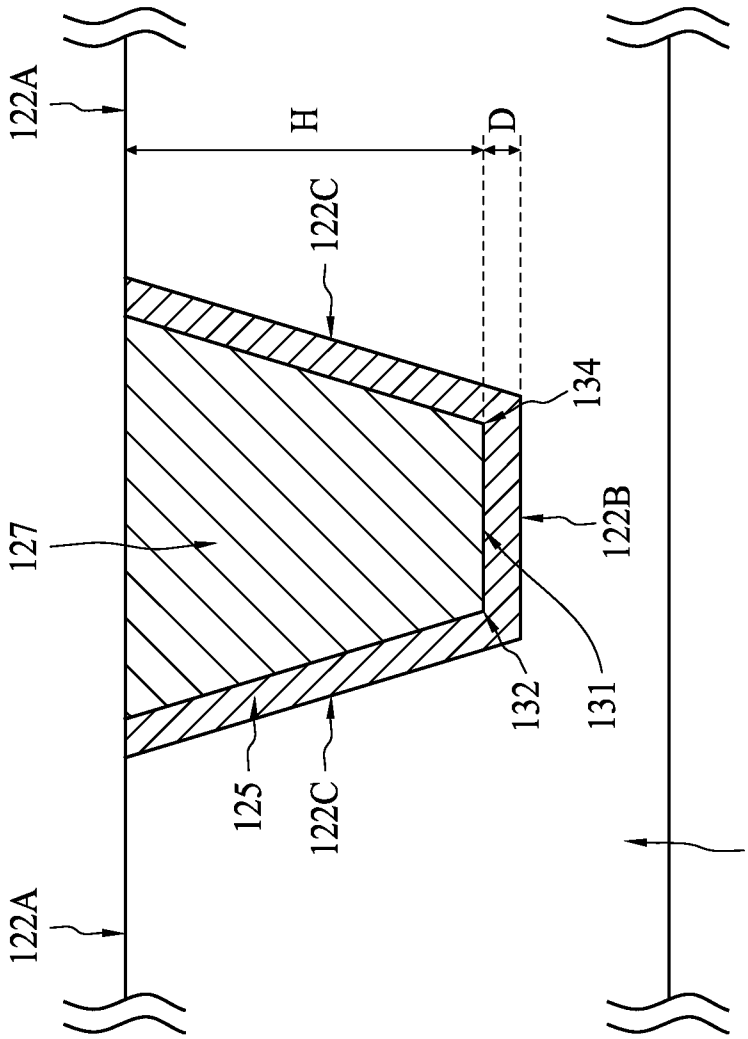



FIG. 3G

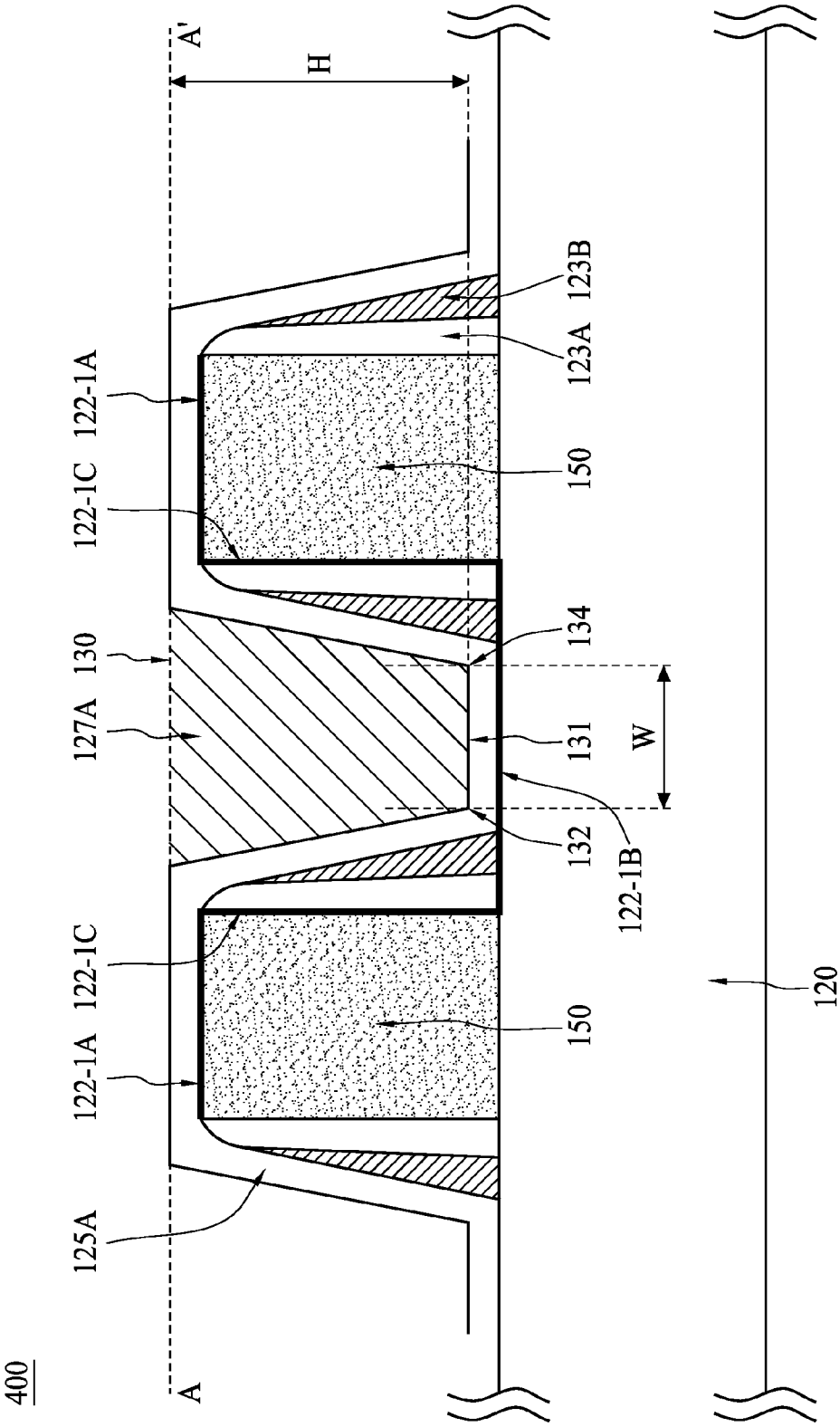

400
A
A'
H
125A
122-1A
122-1C
150
122-1C
122-1A
150
127A
130
131
132
W
122-1B
134
123A
123B
120

FIG. 4

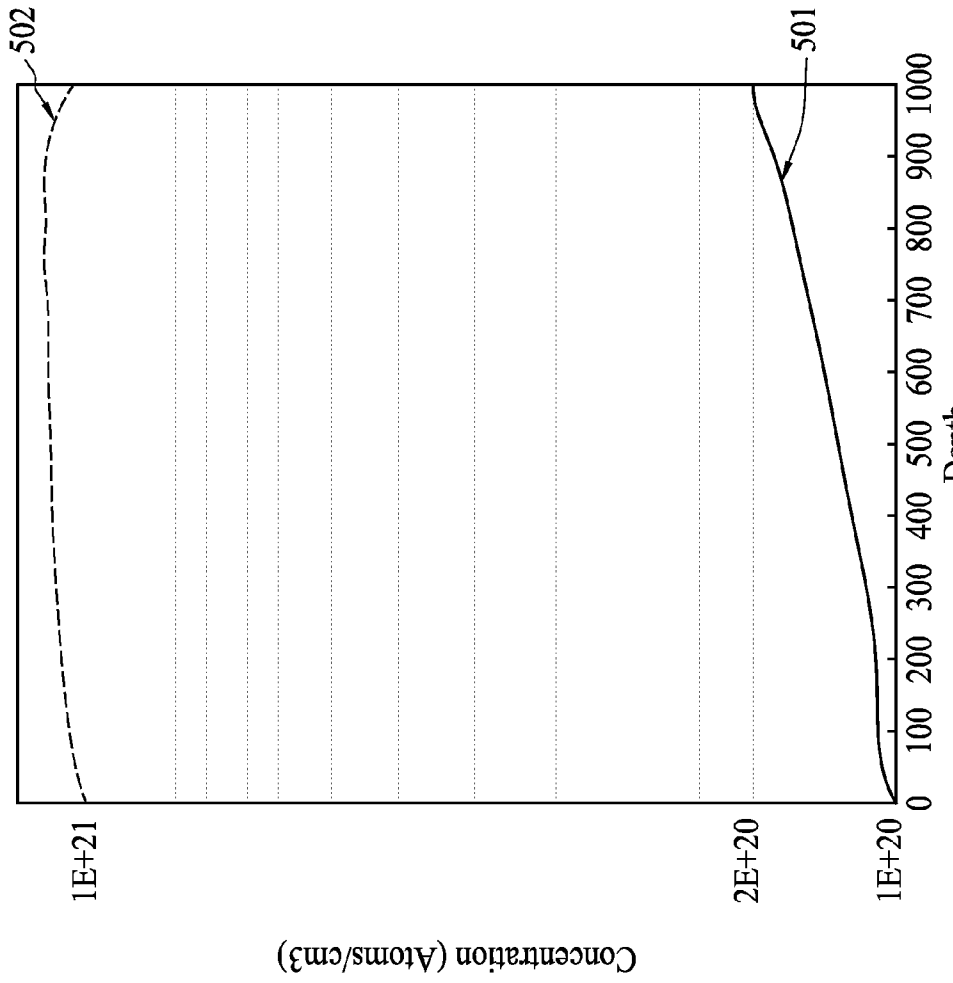

502
501
1E+21
2E+20
1E+20
Concentration (Atoms/cm3)
0
100
200
300
400
500
600
700
800
900
1000
Depth

FIG. 5

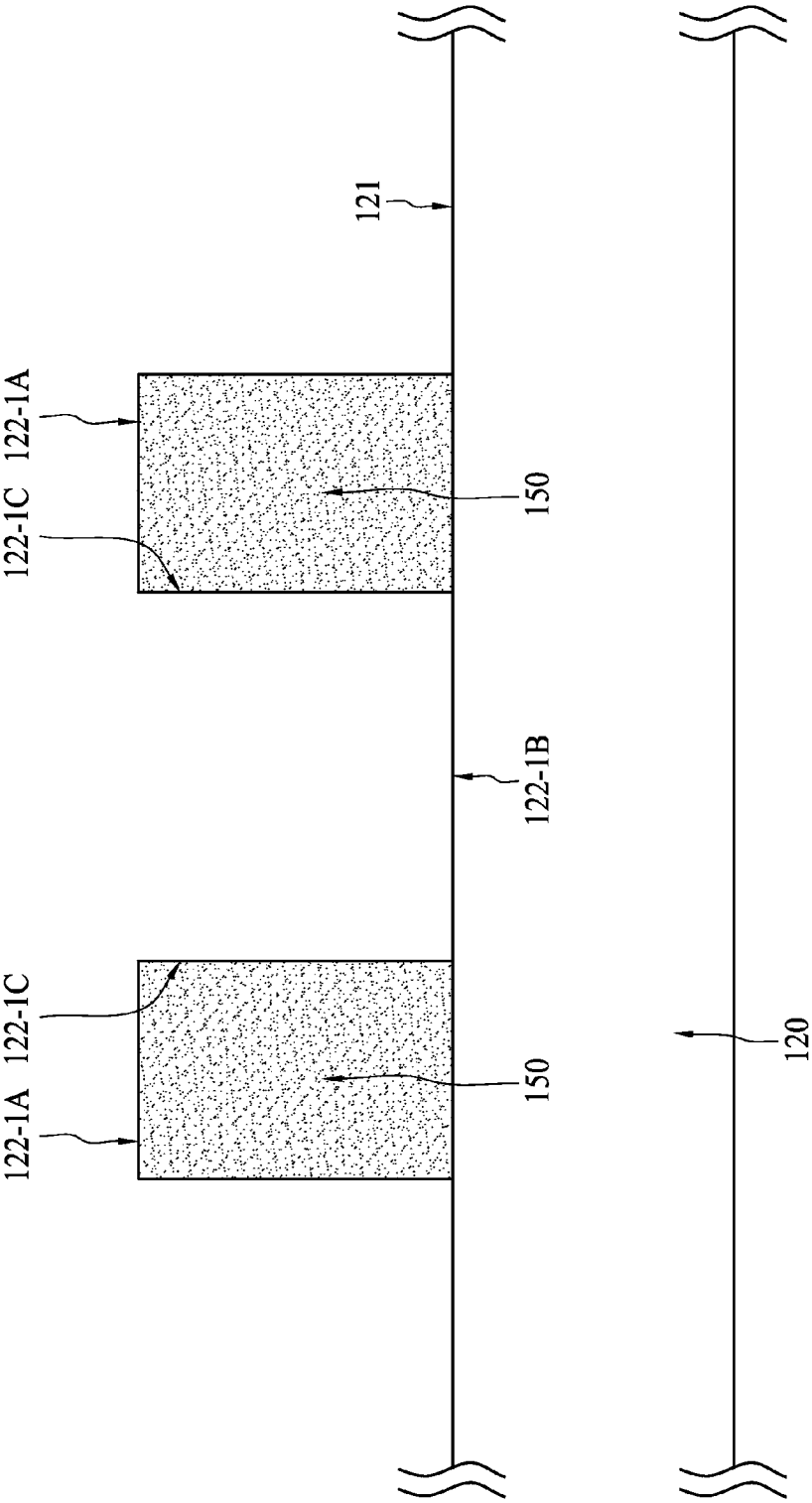



FIG. 6A

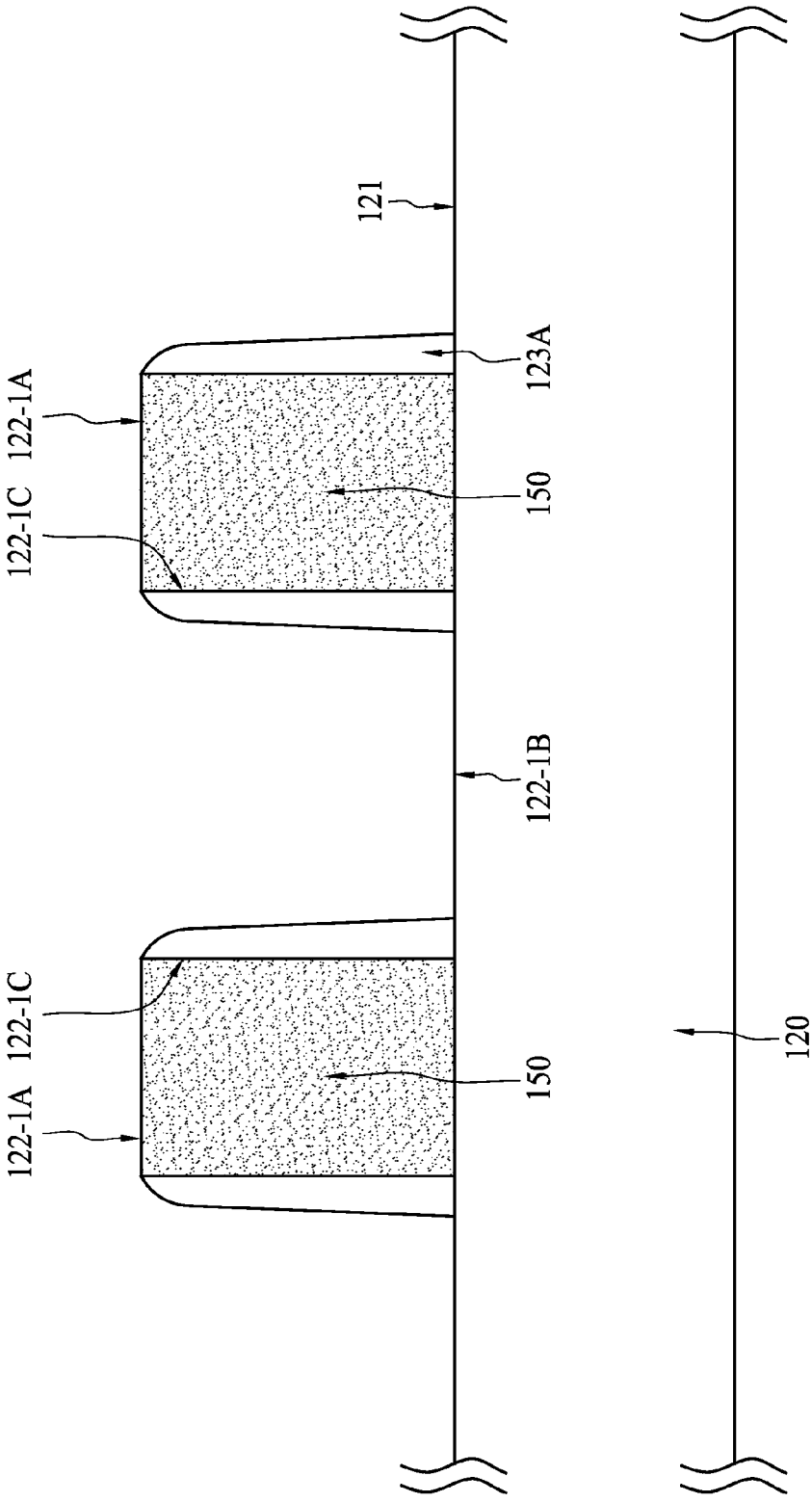



FIG. 6B

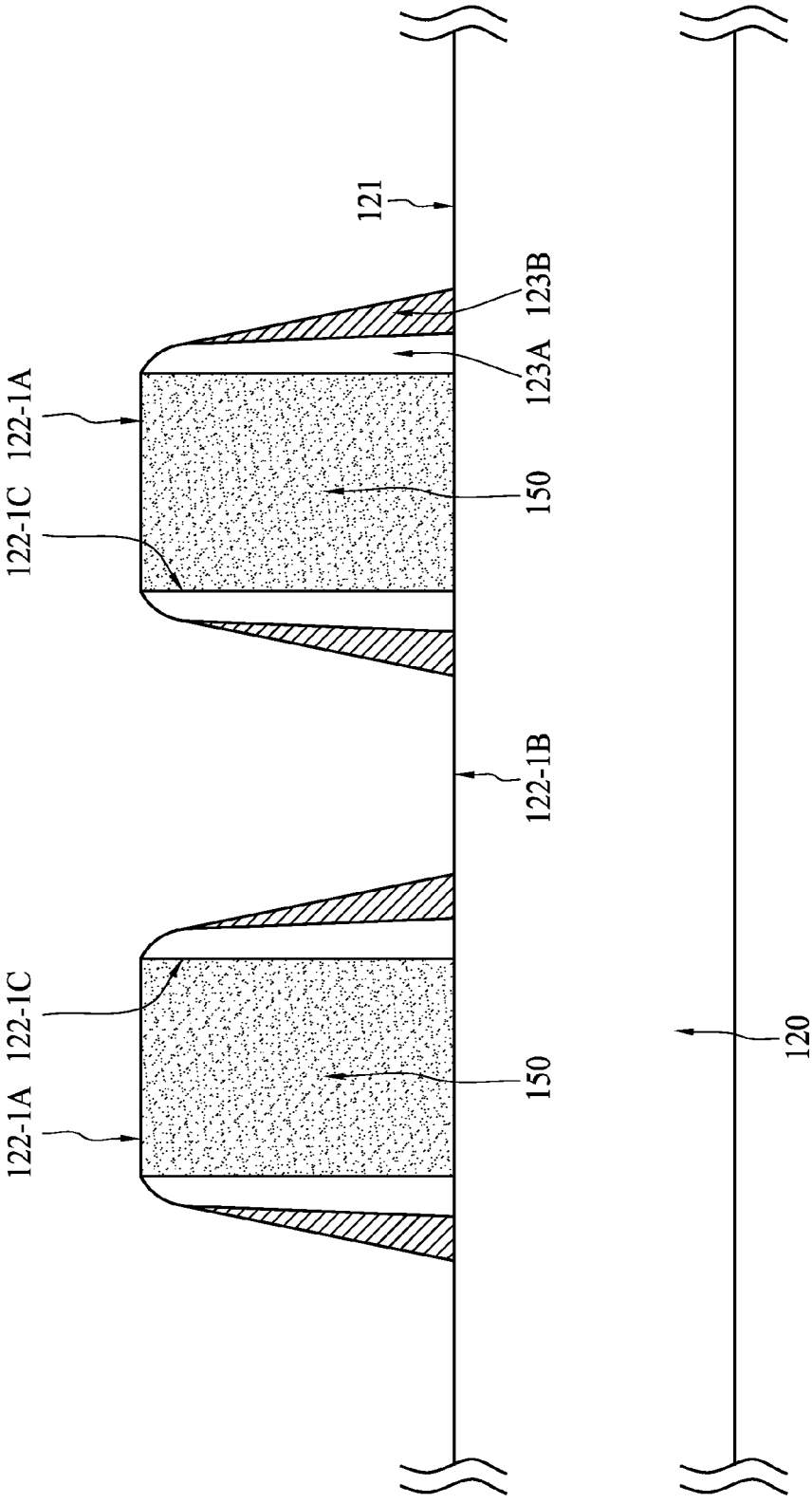



FIG. 6C

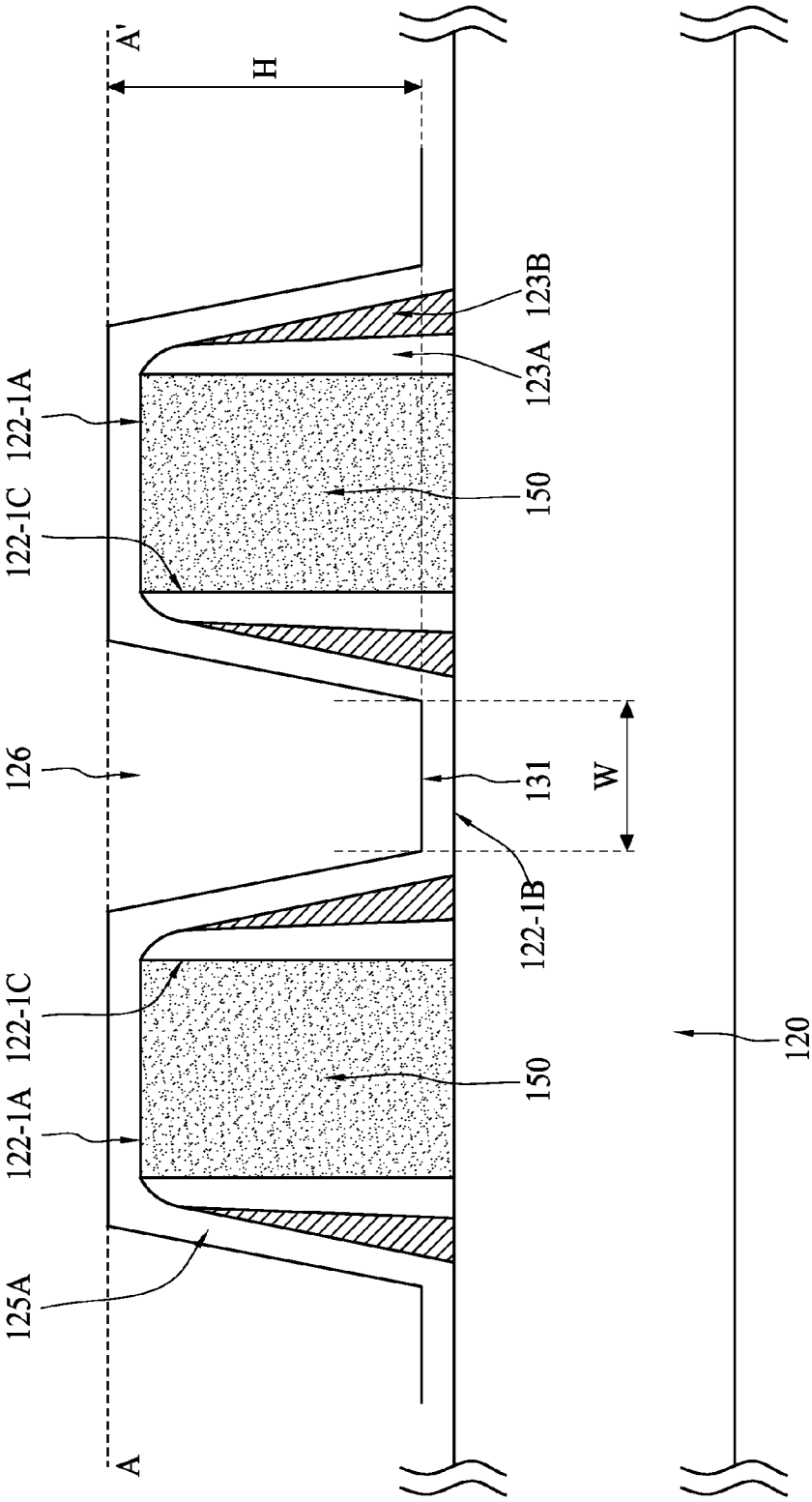

A'
H
123B
123A
122-1A
150
122-1C
126
131
W
122-1B
122-1C
150
122-1A
125A
A
120

FIG. 6D

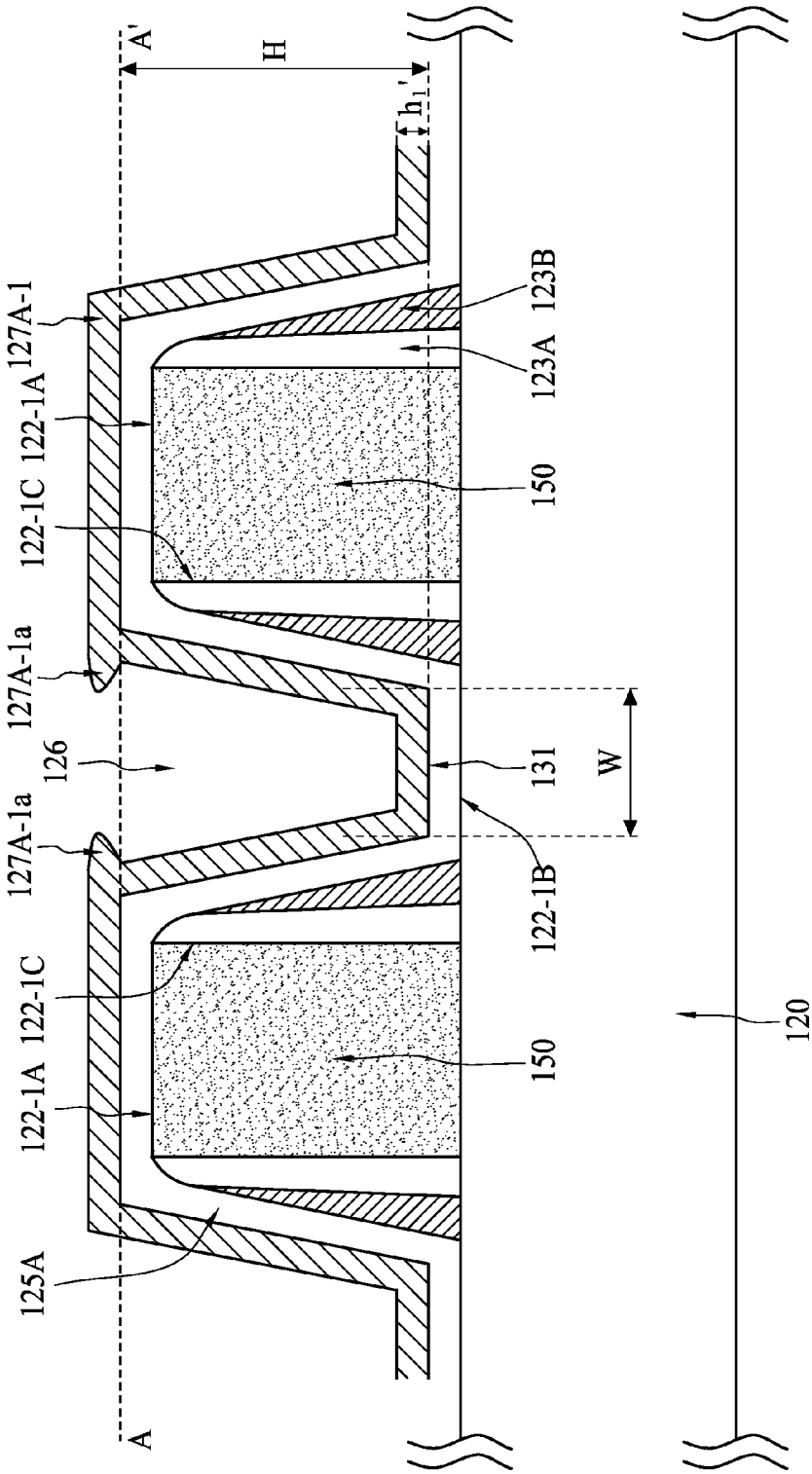

A'
H
$h_1'$
127A-1
123B
123A
122-1A
122-1C
150
127A-1a
126
131
W
127A-1a
122-1B
122-1C
150
122-1A
125A
A
120

FIG. 6E

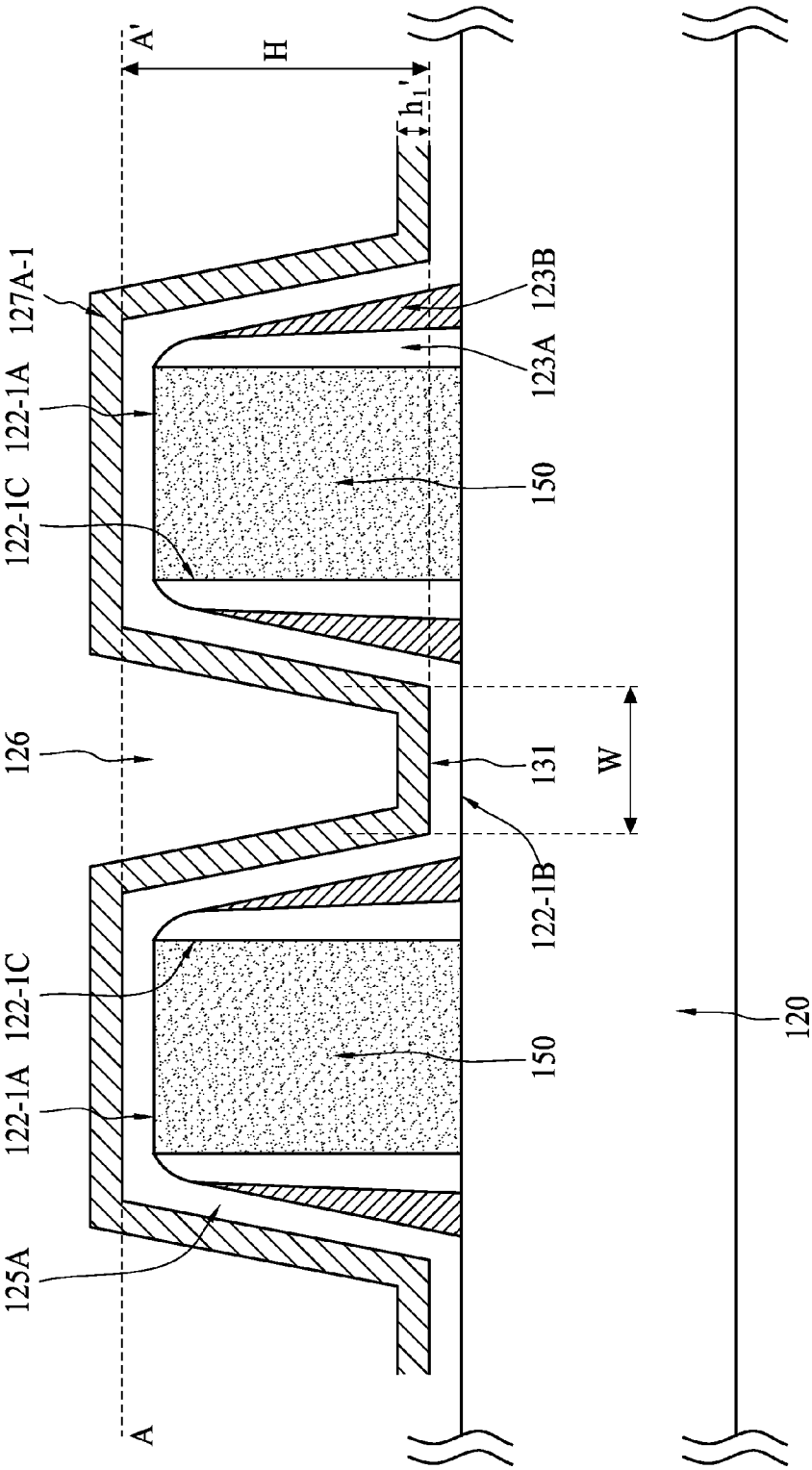

A'
H
$h_1'$
127A-1
123B
123A
122-1A
150
122-1C
126
131
W
122-1B
122-1C
150
122-1A
125A
120
A

FIG. 6F

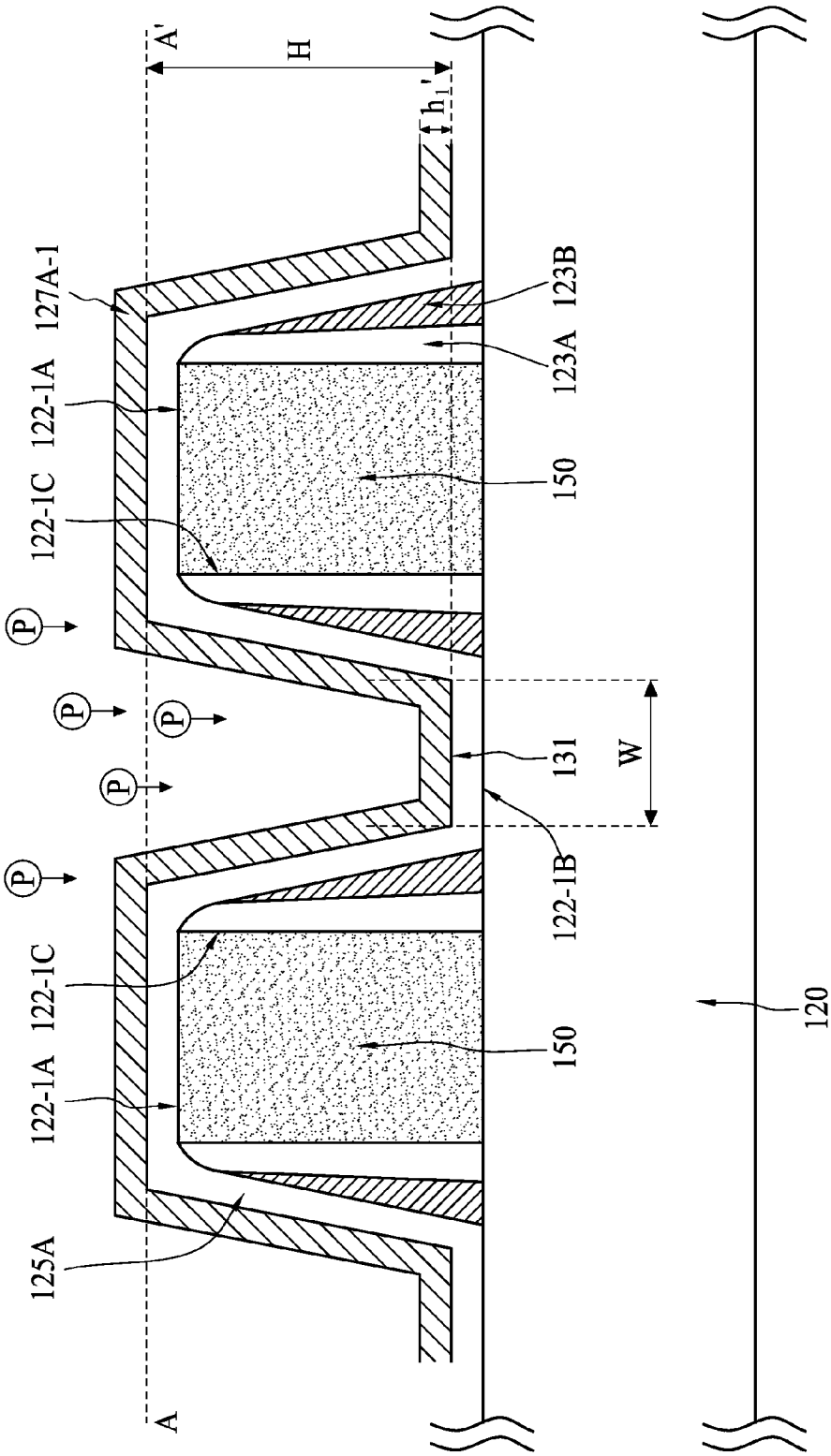



FIG. 6G

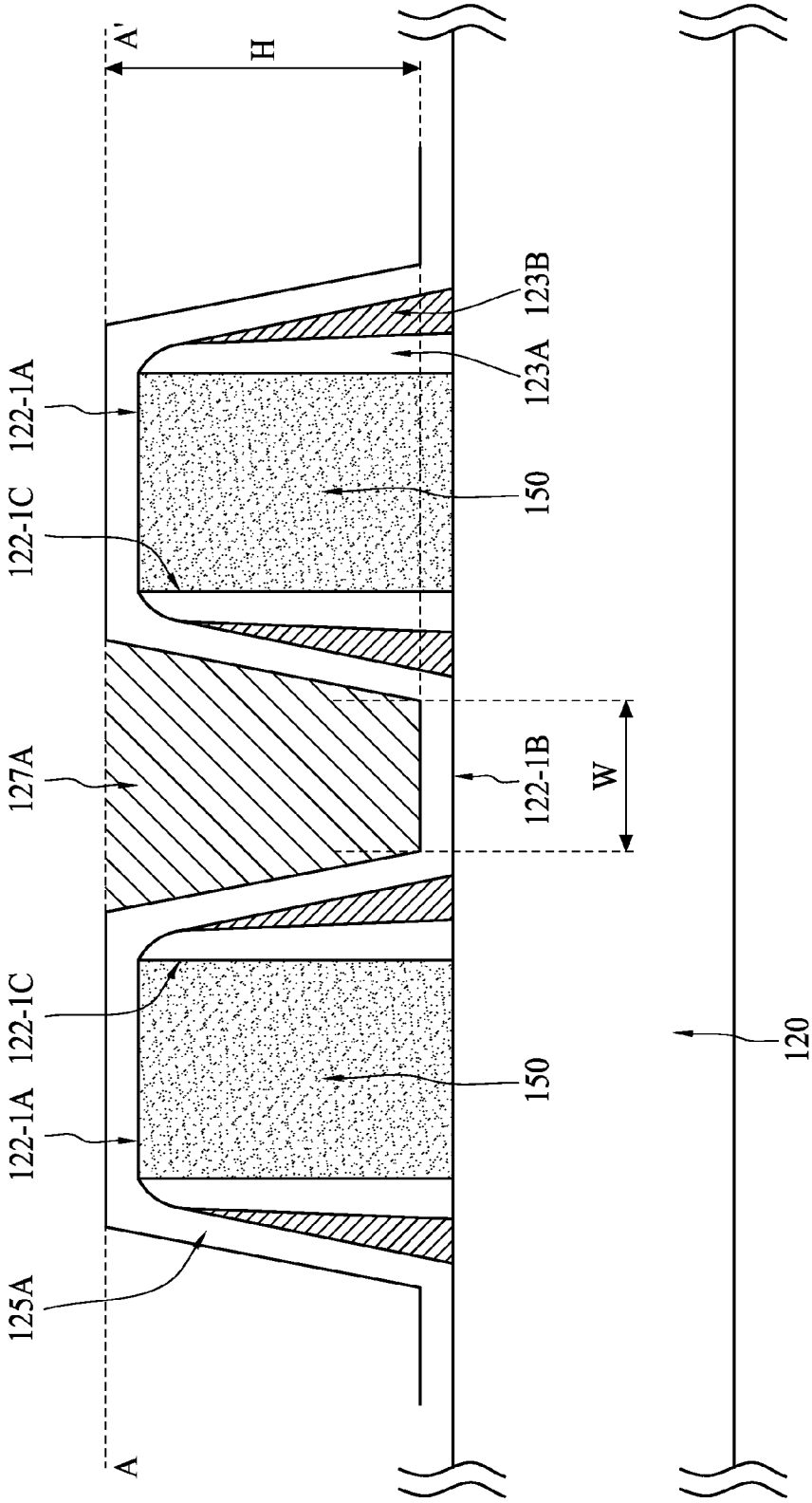

A'
H
123B
123A
122-1A
150
122-1C
127A
122-1B
W
122-1C
150
122-1A
125A
A
120

FIG. 6H

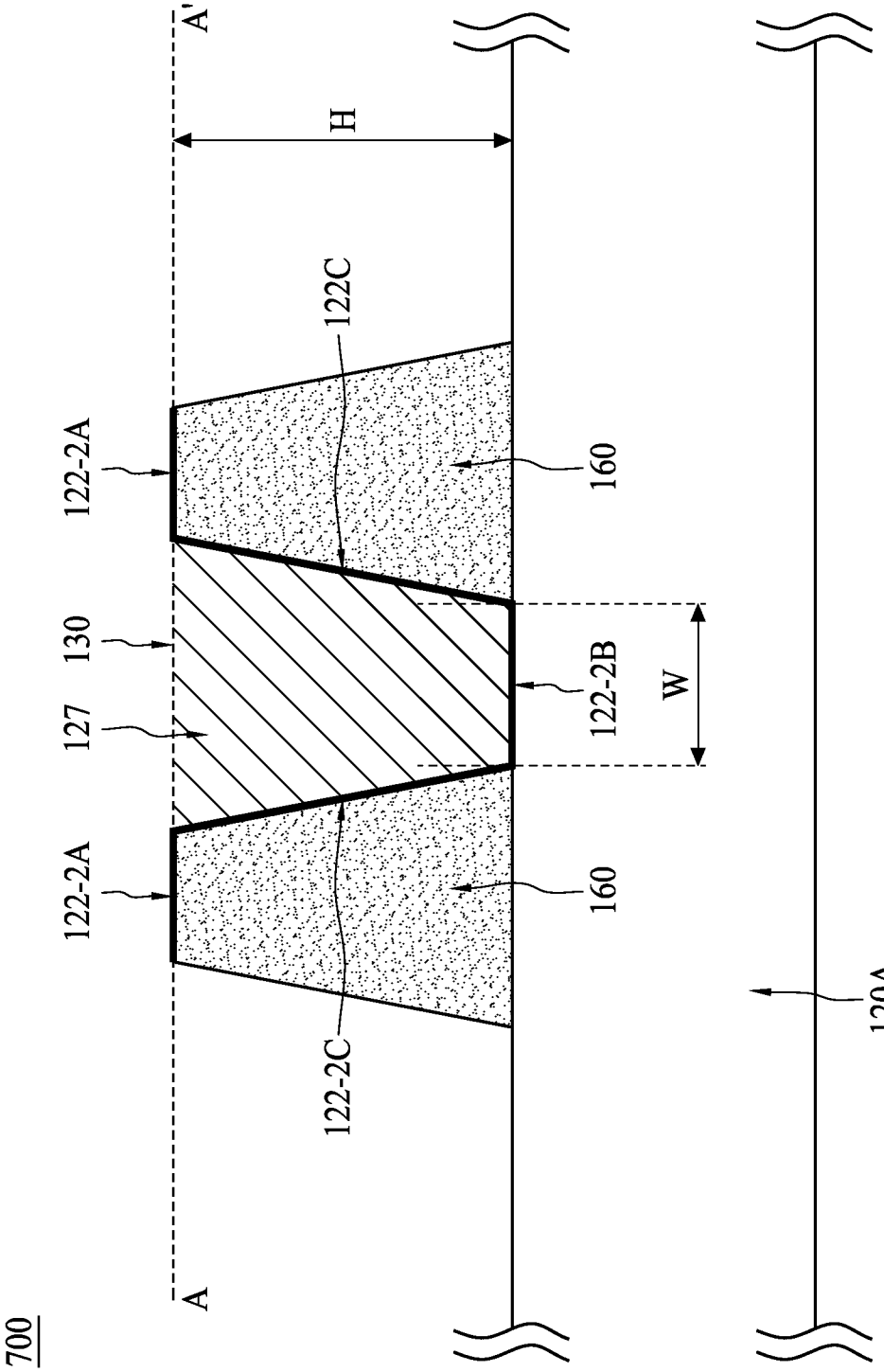



FIG. 7

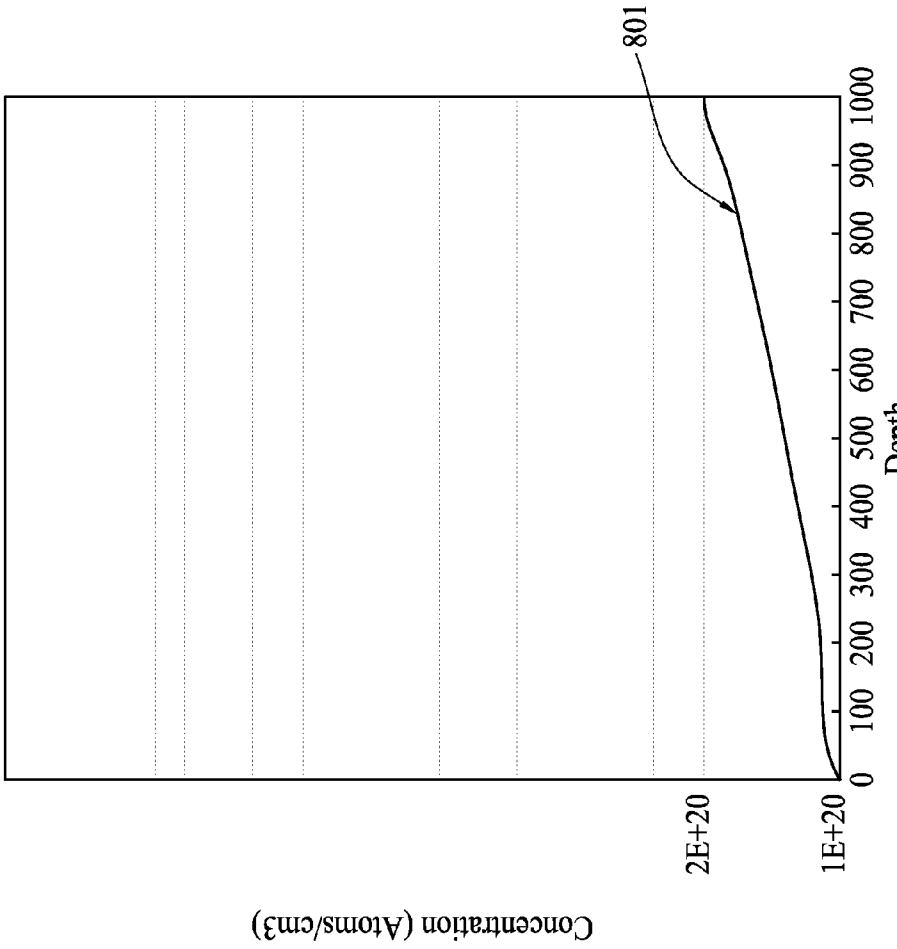

801
Concentration (Atoms/cm3)
2E+20
1E+20
0
100
200
300
400
500
600
700
800
900
1000
Depth

FIG. 8

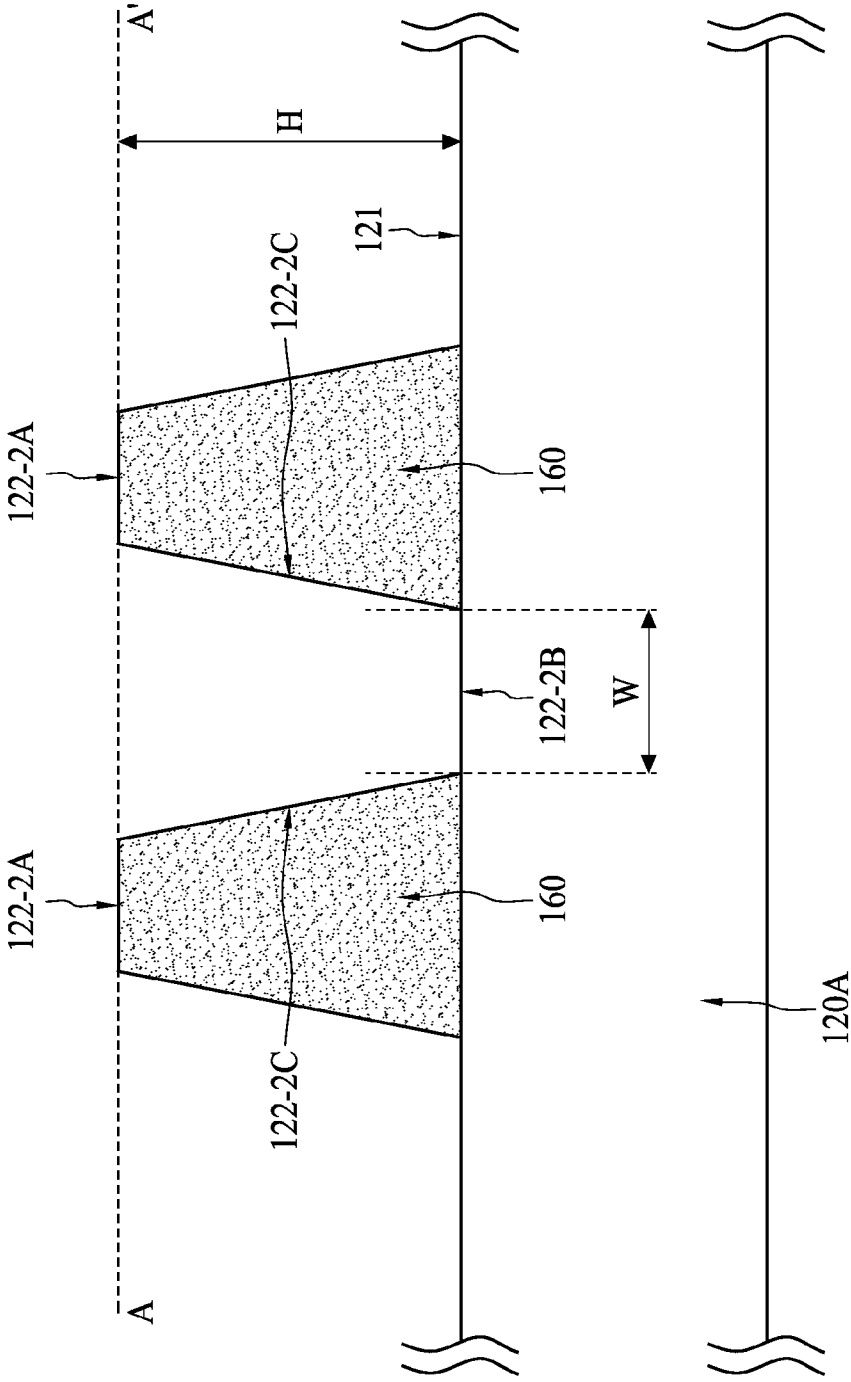



FIG. 9A

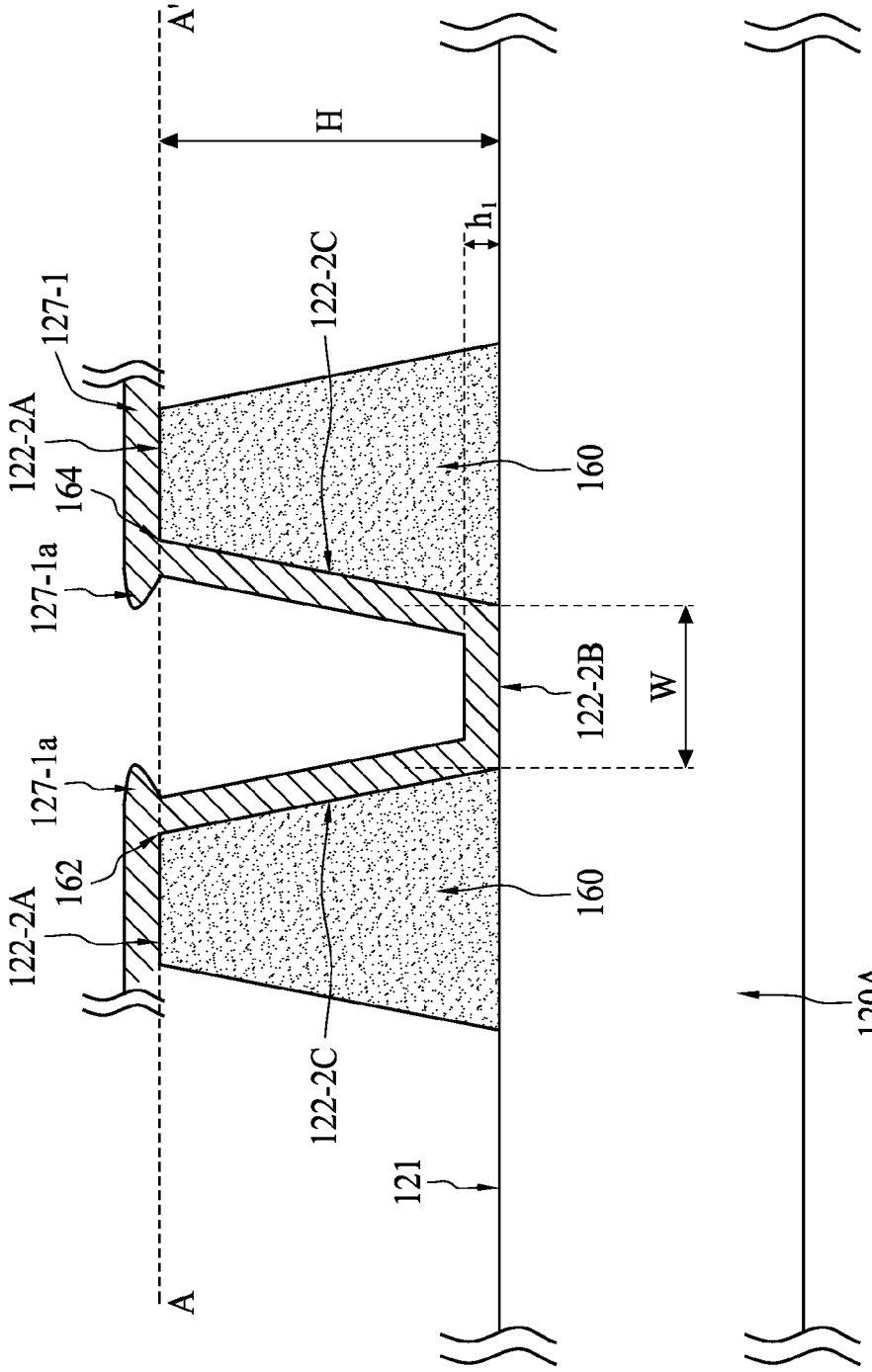

A'
H
$h_1$
122-2C
127-1
122-2A
164
160
127-1a
122-2B
W
127-1a
162
122-2A
160
122-2C
121
A
120A

FIG. 9B

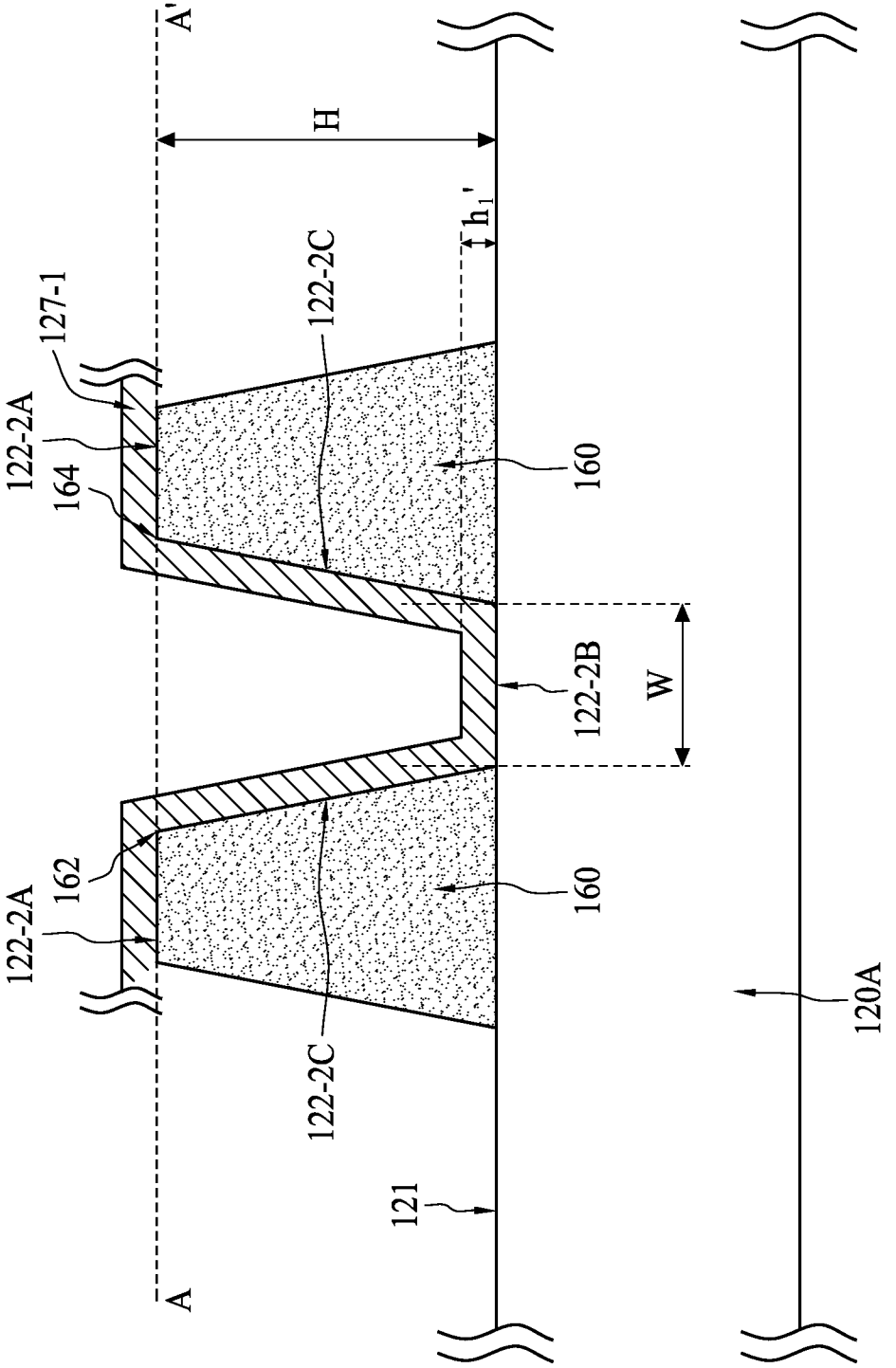

A'
H
$h_1'$
122-2C
127-1
122-2A
164
160
122-2B
W
162
122-2A
160
122-2C
121
A
120A

FIG. 9C

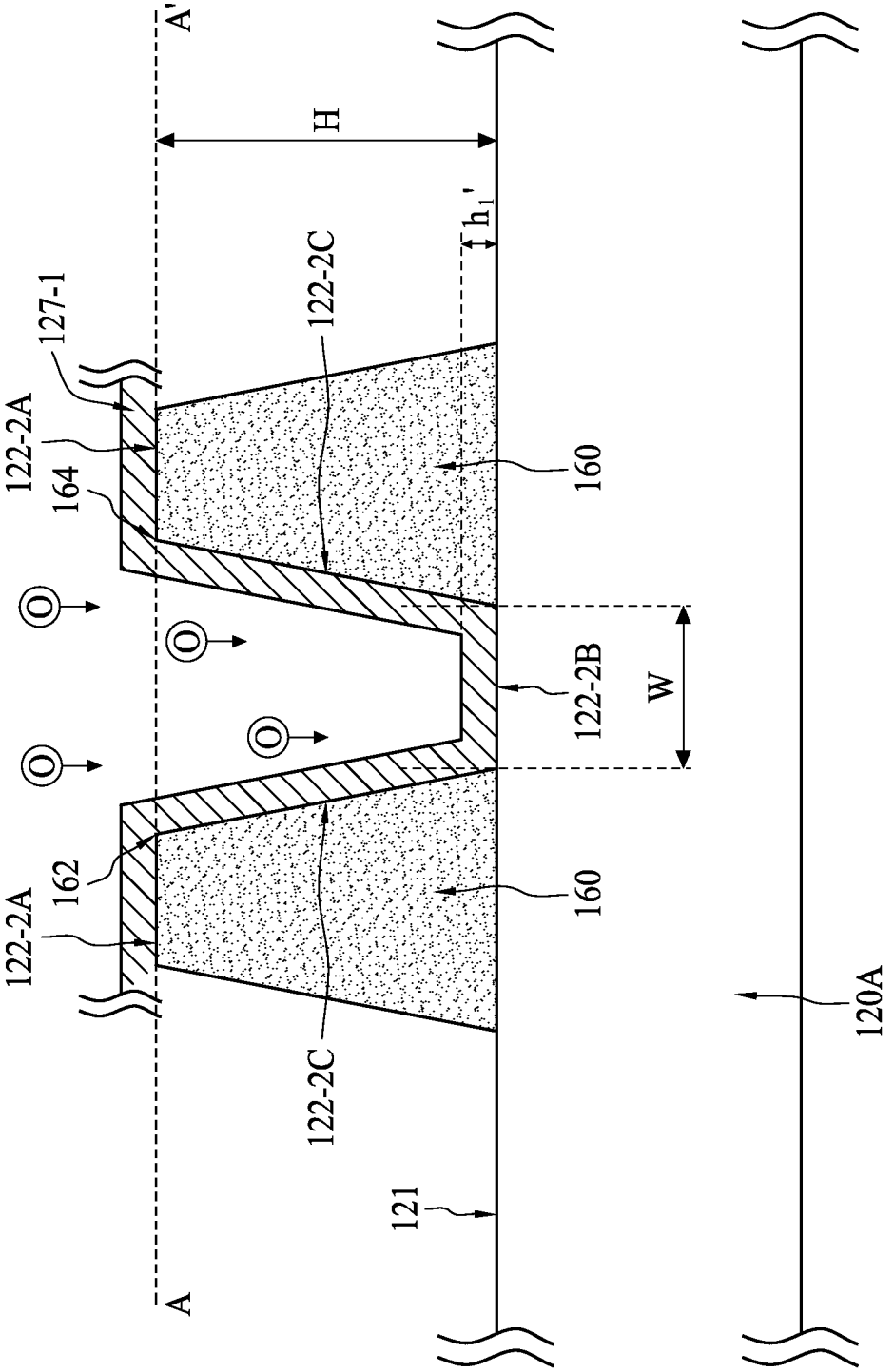

A'
H
$h_1'$
122-2C
127-1
122-2A
164
160
122-2B
W
162
122-2A
160
122-2C
121
A
120A

FIG. 9D

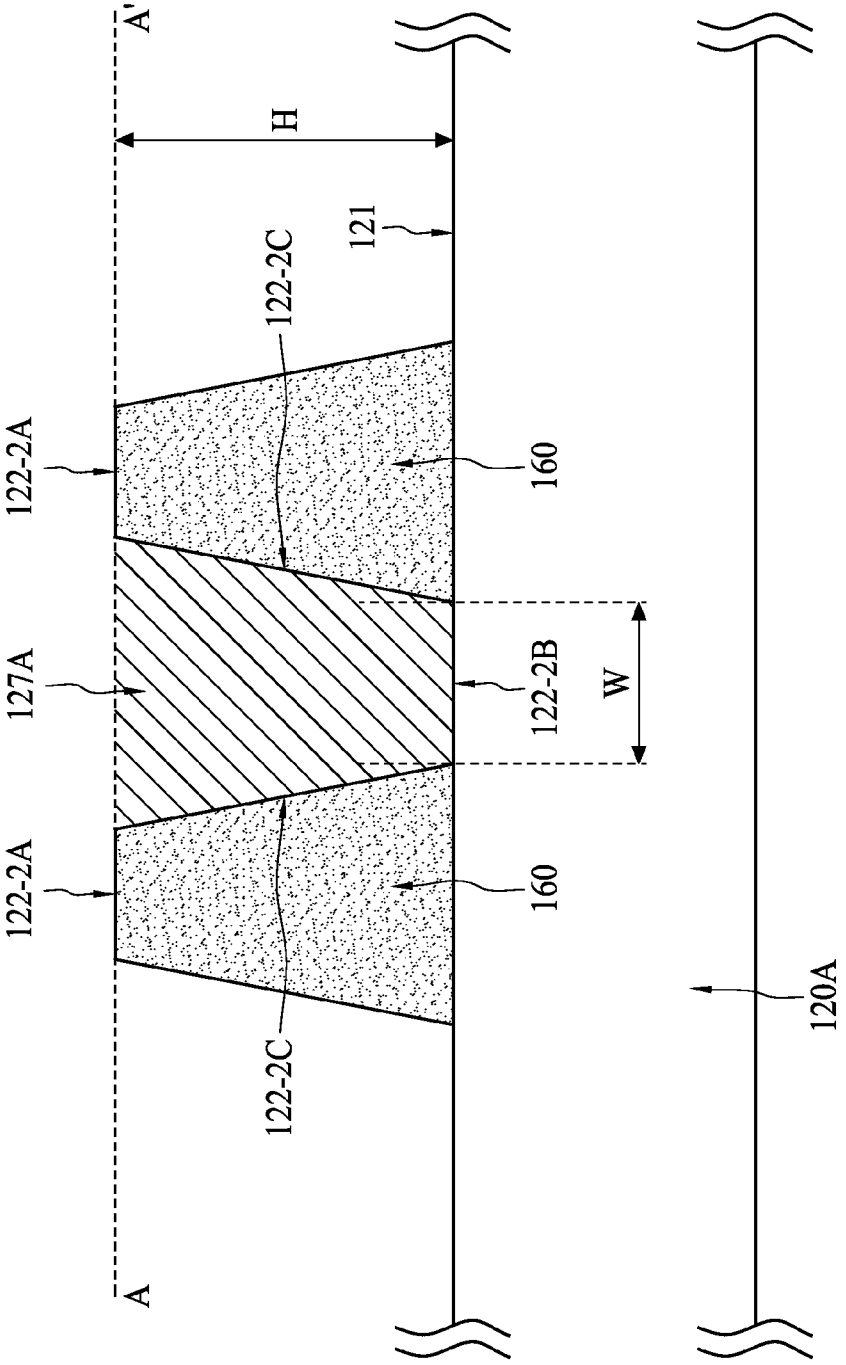



FIG. 9E

# SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF

## FIELD

**[0001]** The disclosure relates to a semiconductor structure, and more particularly to a semiconductor structure with a dielectric material.

## BACKGROUND

**[0002]** Semiconductor devices are widely used in different fields as costs and physical dimensions reduce with advancing technologies. Structures of semiconductor devices become more and more complicated because transistor density per unit area increases. Multilevel of conductive pattern features are also adopted to improve performance of semiconductor devices.

**[0003]** Dielectric material is adopted as a structure in semiconductor devices to isolate transistors in different regions. Dielectric material is also utilized to separate conductive patterns located in different levels. As the geometry shrinks, a multi-step method is used to grow the dielectric material in a multi-layer manner. However, the interface between each layer is a weak point of the dielectric material.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0004]** Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, some features are not drawn to scale. In fact, the dimensions of the some features may be arbitrarily increased or reduced for clarity of discussion.

**[0005]** FIG. **1** is a schematic of a semiconductor structure, in accordance with some embodiments of the present disclosure

**[0006]** FIG. **2** is a fluorine concentration distribution in a dielectric material of the structure in FIG. **1**, according to some embodiments of the present disclosure.

**[0007]** FIGS. **3**A-**3**G are schematic diagrams illustrating a method of manufacturing the semiconductor structure in FIG. **1** at an STI stage, according to some embodiments of the present disclosure.

**[0008]** FIG. **4** is an exemplary semiconductor structure at an ILD stage, according to some embodiments of the present disclosure.

**[0009]** FIG. **5** is a fluorine and phosphorous concentration distribution of a dielectric material in the structure of FIG. **4**, according to some embodiments of the present disclosure.

**[0010]** FIGS. **6**A-**6**H are schematic diagrams illustrating a method of manufacturing the semiconductor structure in FIG. **5** at an ILD stage, according to some embodiments of the present disclosure.

**[0011]** FIG. **7** is an exemplary semiconductor structure at an IMD stage, according to some embodiments of the present disclosure.

**[0012]** FIG. **8** is a fluorine concentration distribution of a dielectric material of the structure in FIG. **7**, according to some embodiments of the present disclosure.

**[0013]** FIGS. **9**A-**9**E are schematic diagrams illustrating a method of manufacturing the semiconductor structure in FIG. **8** at IMD stage, according to some embodiments of the present disclosure.

## DETAILED DESCRIPTION OF THE INVENTION

**[0014]** According to the present disclosure, a dielectric material is introduced in a semiconductor structure. The dielectric material is arranged as a gap filling film between pattern features in some stages. In some embodiments, the dielectric material acts as an isolation filled in a trench of a substrate. In some embodiments, the dielectric material acts as an isolation between conductive lines. The conductive lines are electrically conductive or semi-conductive.

**[0015]** In some embodiments of the present disclosure, concentration of phosphorus is substantially constant across the dielectric material. In some embodiments, fluorine concentration changes in a substantially linear manner across the dielectric material. In some embodiments, the dielectric layer is a portion of the dielectric material.

**[0016]** In the present disclosure, some exemplary stages are used to illustrate some embodiments. A shallow trench isolation (STI) stage refers to a stage in which STI structures are defined. The STI structures are designed to isolate transistor gates, sources, drains, etc. An inter layer dielectric (ILD) stage is in between formation of a transistor gate and formation of a first metal layer. An IMD stage is after the ILD stage.

### Semiconductor Structure at STI Stage

**[0017]** FIG. **1** is an exemplary semiconductor structure **100** at an STI stage, in accordance with some embodiments. A semiconductor substrate **120** of the semiconductor structure **100** provides a foundation to form semiconductor circuitry. In some embodiments, the substrate **120** is a silicon substrate with a first conductivity type, which is a p-type, for example. In some embodiments, the substrate **120** has several doped regions. Some of the doped regions have a second conductivity type opposite to the first conductivity type. Some of the doped regions have the first conductivity type with a higher concentration than that of the substrate **120**. The semiconductor substrate **120** has a surface **122** (not labeled in the drawing) that includes two portions **122**A, two portions **122**C, and a portion **122**B. The surface **122** is a jagged surface and is illustrated by a coarse line in FIG. **1**. Each portion **122**C is in between a corresponding portion **122**A and the portion **122**B. The portion **122**B is connected with two portions **122**C.

**[0018]** A liner **125** is disposed on the surface **122**. As illustratively shown in FIG. **1**, the liner **125** is disposed on the portion **122**B and two portions **122**C of the surface **122**. In some embodiments not shown in FIG. **1**, the liner **125** is also disposed on two portions **122**A. The liner **125** has a thickness D between about 50 Å and 700 Å. In some embodiments, the liner **125** is electrically isolative.

**[0019]** A dielectric material **127** is disposed on the liner **125**. In some other embodiments that there is not the liner **125**, the dielectric material **127** is directly disposed on the portion **122**B and two portions **122**C. The dielectric material **127** has a predetermined shape, which is determined by the portion **122**B and two portions **122**C. As illustratively shown in FIG. **1**, the dielectric material **127** has a shape of a trapezoid. In some other embodiments, the dielectric material **127** has a shape of a quadrilateral. Other shapes of the dielectric material **127** are within the contemplated scope of the present disclosure.

**[0020]** The dielectric material **127** has predetermined dimensions, such as a first width $W_1$, a second width $W_2$ and a height H. As shown in FIG. **1**, the width $W_1$ is defined by a corner **132** and a corner **134** of the dielectric material **127**. The

width $W_2$ is defined by a corner **136** and a corner **137** of the dielectric material **127**. The height H is defined by a top surface **130** of the dielectric material **127** and a bottom surface **131** of the dielectric material **127**. In FIG. **1**, the bottom surface **131** is an interface between the dielectric material **127** and the liner **125**. The dielectric material **127** has an aspect ratio, which is defined by a ratio of the height H over the width $W_1$ of the dielectric material **127**. In some embodiments, the height H is greater than 72 nm and the width W is smaller than 30 nm. As a result, the aspect ratio of the dielectric material **127** is 2.4. In some embodiments, the aspect ratio of the dielectric material **127** is greater than 2.4, and is, for example, 2.8, 3.5, etc. In some embodiments, such as a 40 nm CMOS (complimentary metal oxide semiconductor) device, the aspect ratio of the dielectric material **127** in the STI stage is greater than 2.4 in order to meet the design rule. Other values of the aspect ratio are within the contemplated scope of the present disclosure.

**[0021]** The dielectric material **127** has a silicon glass matrix and electrically isolates active regions in the substrate **120**. In some embodiments with references to FIG. **1**, the dielectric material **127** has a fluorine ion in the silicon glass matrix. FIG. **2** is a graph representing fluorine concentration distribution in the dielectric material **127** according to some embodiments. The fluorine concentration is measured by a secondary ion mass spectrometer (SIMS), an Auger electron nanoscope (Auger) or other suitable analysis tools. In FIG. **2**, the Y-axis represents the fluorine concentration in atomic ratio per cubic centimeters (Atoms/$cm^3$). The X-axis represents a depth of the dielectric material **127** that is referenced from the top surface **130** of the dielectric material **127**, and the unit is Å.

**[0022]** In the illustration of FIG. **2**, the dielectric material **127** has a depth of about 1000 Å. The depth is also the height H of the dielectric material **127** shown in FIG. **1**. The fluorine concentration is thus illustrated from 0 Å to about 1000 Å. From 0 Å to about 1000 Å, the fluorine concentration changes from about 1×E20 Atoms/$cm^3$ to about 2×E20 Atoms/$cm^3$. Effectively, the fluorine concentration is lowest at the surface **130** and is highest at the interface **131**.

**[0023]** FIGS. **3**A-**3**G are cross sectional views of the semiconductor structure **100** at the STI stage illustrated in FIG. **1**, according to some embodiments of the present disclosure.

**[0024]** In FIG. **3**A, a substrate **120** having a surface **121** is provided. In FIG. **3**B, a portion of the substrate **120** is removed to form a trench in the substrate **120**. Two portions labeled **122**A are remaining portions of the surface **121** in FIG. **3**B. Two sidewalls of the trench correspond to two portions **122**C in FIG. **1**. A bottom surface of the trench corresponds to the portion **122**B in FIG. **1**. Two portions **122**A, two portions **122**C and portion **122**C form the surface **122** in FIG. **1**. The trench has a height H' defined as a distance from the surface portion **122**A and the surface portion **122**B.

**[0025]** In FIG. **3**C, a layer **125**A is formed on the surface **122**. The layer **125**A has a thickness D referenced from the bottom of the trench. In FIG. **3**D, a dielectric layer **127-1** is formed on the layer **125**A. Effectively, the dielectric layer **127-1** is also formed over the surface **122**. In some embodiments without the liner **125**, the dielectric layer **127-1** is formed on the surface **122**. The dielectric layer **127-1** has a thickness $h_1$.

**[0026]** A chemical vapor deposition (CVD) process is used to form the dielectric layer **127**A. In some embodiments, the CVD process is a high density plasma (HDP) or high aspect ratio process (HARP). The CVD process includes a deposition step and an insitu sputter step. The deposition step is to form some dielectric material in the trench and the insitu sputter step uses ions such as argon ions to remove a portion of the dielectric material. The dielectric layer **127-1** in FIG. **3**D is a final profile formed by the CVD process. The dielectric layer **127-1** has two overhangs **127-1***a*.

**[0027]** In FIG. **3**E, an insitu etch step is used to remove a portion of the dielectric layer **127-1**. During this operation, the overhangs **127-1***a* in FIG. **3**D are removed. In some embodiments as illustrated with reference to FIG. **3**E, an $NF_3$ gas is ionized to remove the portion of the dielectric layer **127-1**. A circle with an "F" represents a fluorine ion of the ionized NF3 gas. The thickness of the dielectric layer **127-1** is reduced to $h_1$'. In some embodiments, the thickness $h_1$' is about ⅙ of the height H. The height H is defined by a surface portion **122**A and the interface between the dielectric layer **127-1** and the liner **125**.

**[0028]** In FIG. **3**F, an operation to treat a top surface of the dielectric layer **127-1** with plasma is illustrated. In this operation, a gas is introduced and ionized by a first radio frequency (RF) power to form the plasma. In some embodiments, the gas is oxygen and the first RF power is between about 1000 W and 9000 W. A circle with an "O" illustrates an oxygen ion. A second RF power is also introduced to accelerate the plasma to treat the top surface of the dielectric layer **127-1**. In some embodiments, the second RF power is between about 1000 W and 9000 W. During this operation, fluorine concentration at the top surface of the dielectric layer **127-1** is adjusted. The fluorine concentration in the dielectric layer **127-1** changes in a linear manner.

**[0029]** In some embodiments, several cycles are used to form the dielectric material **127** to a predetermined thickness. For example, operations with reference to FIGS. **3**D to **3**F are repeated to form a cycle of forming the dielectric layer **127-1**. In some embodiments as illustrated in FIG. **3**G, an operation that repeats the cycle 6-7 times is used to form the dielectric material **127** in the trench having the thickness H. A portion of the layer **125**A in FIG. **3**F is also removed to result in the liner **125**.

## Semiconductor Structure at ILD Stage

**[0030]** FIG. **4** is an exemplary semiconductor structure **400** at an ILD stage, in accordance with some embodiments. The semiconductor structure **400** has a surface **122-1** (not labeled in the drawing) and two conductors **150** on the substrate **120**. The surface **122-1** includes at least two portions **122-1**A, two portions **122-1**C, and a portion **122-1**B. The portion **122-1**A, **122-1**B, and **122-1**C correspond to the portion **122**A, **122**B, and **122**C in FIG. **1**, respectively. The conductors **150** are electrically conductive and, in some embodiments, are gates of the semiconductor structure **400**. The two conductors **150** are identical, and the conductor **150** on the right side is used in the exemplary illustration that is also applicable to the other conductor **150**. A portion **122-1**C is a sidewall of the conductor **150** and a portion **122-1**A is a top surface of the conductor **150**. A first spacer **123**A is adjacent to a sidewall of the conductor **150**. A second spacer **123**B is adjacent to the first spacer **123**A. Spacers **123**A and **123**B are symmetrical with reference to the conductor **150**. In some embodiments, the semiconductor structure **400** has at least one spacer at each side of the conductor **150**.

**[0031]** A liner **125**A is disposed over the substrate **120** and other locations. For example, a portion of the liner **125**A is over the conductors **150**, another portion is on the top surface

**122-1**A of the conductor **150**, and another portion is on the spacers **123**A and **123**B. In some embodiments, the liner **125**A is an etch stop layer.

**[0032]** A dielectric material **127**A corresponds to the dielectric material **127** in FIG. **1**, and includes phosphorous ions in addition to fluorine ions as in the dielectric material **127**. The dielectric material **127**A also has a silicon glass matrix and electrically isolates the conductors **150**.

**[0033]** FIG. **5** is a fluorine concentration distribution of the dielectric material **127**A in FIG. **4** according to some embodiments. The fluorine concentration is measured by a secondary ion mass spectrometer (SIMS), an Auger electron nanoscope (Auger) or other suitable analysis tools. In FIG. **5**, the Y-axis represents the fluorine concentration and the unit is atomic ratio per cubic centimeters (atoms/$cm^3$). The X-axis represents a depth of the dielectric material **127**A with reference to a line AA' in FIG. **4**, and the unit is Å. Line **501** represents the fluorine concentration versus the depth of the dielectric material **127**A. In the illustration of FIG. **5**, the dielectric material **127**A has a depth of about 1000 Å. The depth is also the height H of the dielectric material **127**A. The fluorine concentration is thus illustrated from 0 Å to about 1000 Å. From 0 Å to about 1000 Å, the fluorine concentration changes from about 1×E20 Atoms/$cm^3$ to about 2×E20 Atoms/$cm^3$. Effectively, the fluorine concentration is lowest at the surface **130** shown in FIG. **4** and is highest at the interface **131**.

**[0034]** Line **502** represents the phosphorous concentration distribution versus the depth of the dielectric material **127**A. In FIG. **5**, the phosphorous concentration is substantially constant in the dielectric material **127**A.

**[0035]** FIGS. **6**A-**6**H are cross sectional views of the semiconductor structure **400** at the ILD stage illustrated in FIG. **4**, according to some embodiments of the present disclosure.

**[0036]** In FIG. **6**A, two conductors **150** are formed on the surface **121** of the substrate **120**. Each conductor **150** includes a sidewall **122-1**C. The top surface of each conductor **150** corresponds to the portion **122-1**A in FIG. **4**. A portion of the surface **121** between the two conductors **150** corresponds to the portion **122-1**B in FIG. **4**.

**[0037]** In FIG. **6**B, a first spacer **123**A is formed on a corresponding sidewall **122-1**C of the conductors **150**. In FIG. **6**C, a second spacer **123**B is formed adjacently to the first spacer **123**A. For simplicity, only elements associated with one conductor **150** are labeled.

**[0038]** In FIG. **6**D, a liner **125**A is formed and covers the top surface **122-1**A of the conductor **150** and on the spacers **123**A and **123**B. A portion of the liner **125**A is on the bottom surface **122-1**B. An opening **126** between the conductors **150** has a height H and a width W.

**[0039]** In FIG. **6**E, a doped chemical vapor deposition (CVD) process is used to form a dielectric layer **127**A-**1** on the liner **125**A. In some embodiments, the doped CVD process is a high density plasma (HDP) or HARP process. The dopant is phosphorous ions. The doped chemical vapor deposition includes a deposition step and an insitu sputter step. The deposition step forms doped dielectric material on the liner **125**A. The insitu sputter step uses ion such as argon ions and removes a portion of the doped dielectric material.

**[0040]** A same fluorine ion etch process as illustrated in FIG. **3**E is adopted to remove the overhangs **127**A-**1***a* after the operation in FIG. **6**E. FIG. **6**F illustrates the height of dielectric layer **127**A-**1** is reduced to $h_1$'.

**[0041]** In FIG. **6**G, an operation to treat a top surface of the dielectric layer **127**A-**1** with plasma is illustrated. For some embodiments, a $PH_3$ gas is introduced and ionized by a first radio frequency (RF) power to form the plasma. Phosphorous ions are generated from the ionized $PH_3$ gas. A circle with an "P" illustrates an phosphorous ion. A second RF power is also introduced to accelerate the plasma to treat the top surface of the dielectric layer **127**A-**1**. The magnitude of the first and the second RF powers are as illustrated with reference to FIGS. **3**A-**3**G. During the first and second RF operations, phosphorous concentration at the top surface of the dielectric layer **127**A-**1** is adjusted. The phosphorous concentration in the dielectric layer **127**A-**1** is substantially constant throughout the dielectric layer **127**A-**1**. Fluorine concentration at the top surface of the dielectric layer **127**A-**1** is adjusted to change in a linear manner throughout the dielectric layer **127**A-**1**.

**[0042]** In some embodiments, several cycles are used to form the dielectric material **127**A to a predetermined height. For example, operations with reference to FIGS. **6**E to **6**G are repeated as a cycle to form the dielectric layer **127**A-**1**. An operation that repeats the cycle 6-7 times is used and results in the dielectric material **127**A having the height H.

Semiconductor Structure at IMD Stage

**[0043]** FIG. **7** is an exemplary semiconductor structure **700** at an IMD stage, in accordance with some embodiments. The semiconductor structure **700** has a surface **122-2** not labeled in the drawing) and two conductors **160** on a substrate **120**A. The surface **122-2** includes at least two portions **122-2**A two portions **122-2**C and a portion **122-2**B. The portion **122-2**A, **122-2**B, and **122-2**C correspond to the portion **122**A, **122**B, and **122**C in FIG. **1**, respectively. In some embodiments, the conductors **160** include metal. The substrate **120**A corresponds to the substrate **120** in FIG. **1**, and, in addition to silicon, also includes metal and dielectric.

**[0044]** A dielectric material **127** is on the portions **122-2**C and the portion **122-2**B. In some embodiments, a liner **125**A (not shown in the drawing) is between the dielectric material **127** and the surface **122-2**. The dielectric material **127** has a fluorine ion in the silicon glass matrix. The dielectric material **127** has a height H. In some embodiments, the height of the dielectric material **127** is dependant on a height of the conductor **160**.

**[0045]** FIG. **8** is a fluorine concentration distribution in the dielectric material **127** according to some embodiments. The X-axis represents a depth of the dielectric material **127** with reference to a line AA' in FIG. **7**, and the unit is Å. Line **801** represents the fluorine concentration versus the depth of the dielectric material **127**.

**[0046]** In the illustration of FIG. **8**, the dielectric material **127** has a depth of about 1000 Å. The depth is also the height H of the dielectric material **127**. For the embodiments as illustrated in FIG. **8**, the fluorine concentration is thus illustrated from 0 Å to about 1000 Å, which is substantially equal to the height H of the dielectric material **127**. Other values of the height are within the contemplated scope of the present disclosure. From 0 Å to about 1000 Å, the fluorine concentration changes from about 1×E20 Atoms/$cm^3$ to about 2×E20 Atoms/$cm^3$. Effectively, the fluorine concentration is lowest at the surface **130** and is highest at the portion **122-2**B.

**[0047]** FIGS. **9**A-**9**E are cross sectional views of the semiconductor structure **700** at the IMD stage illustrated in FIG. **7**, according to some embodiments of the present disclosure.

**[0048]** In FIG. **9**A, two conductors **160** are formed on a surface **121** of a substrate **120**A. In some embodiments with referenced to FIG. **9**A, the conductor **150** has a shape of a

trapezoid. In FIG. **9**B, a CVD process is used to form a dielectric layer **127-1** on the portions **122-2**A, **122-2**B and **122-2**C. In some embodiments, the CVD process is a HDP or HARP process. Two overhangs **127-1***a* are formed on top corners **164** of the conductors **160**.

**[0049]** A same fluorine ion etch process illustrated in FIG. **3**E is adopted to remove the overhangs **127-1***a*. The thickness of the dielectric layer **127-1** is reduced to $h_1'$ as illustrated in FIG. **9**C.

**[0050]** FIG. **9**D is used to illustrate an operation to treat a top surface of the dielectric layer **127-1** with plasma. In some embodiments with reference to FIG. **9**D, the plasma includes oxygen ions.

**[0051]** In some embodiments, several cycles are used to form the dielectric material **127** to a predetermined height. For example, operations with reference to FIGS. **9**B to **9**D are repeated to form a cycle to form the dielectric layer **127-1**. In some embodiments as illustrated in FIG. **9**E, an operation that repeats the cycle 6-7 times is used to form the dielectric material **127** having the thickness H.

**[0052]** In some embodiments, a semiconductor structure includes a surface having a plurality of portions and a dielectric material over the surface. The dielectric material includes an aspect ratio that is substantially equal to or greater than a predetermined value.

**[0053]** In some embodiments, a semiconductor structure includes conductors and a spacer disposed on a sidewall of each conductor of the conductors. The semiconductor structure has a liner on the spacer and a top surface of each conductor of the conductors. The semiconductor structure also has a phosphorous doped dielectric material between two conductors and the phosphorous concentration throughout the phosphorous doped dielectric material is substantially constant.

**[0054]** In some embodiments, a method of manufacturing a semiconductor structure includes forming a surface, forming a dielectric layer over the surface, etching the dielectric layer, and treating a top surface of the dielectric layer with plasma.

**[0055]** The above description includes exemplary operations, but these operations are not necessarily required to be performed in the order shown. Operations may be added, replaced, changed order, skipped, and/or eliminated as appropriate, in accordance with the spirit and scope of the disclosure. Accordingly, the scope of the disclosure should be determined with reference to the following claims, along with the full scope of equivalences to which such claims are entitled.

What is claimed is:

**1**. A semiconductor structure, comprising:

a surface including a plurality of portions;

a dielectric material over the surface, wherein the dielectric material includes an aspect ratio that is substantially equal to or greater than a predetermined value.

**2**. The semiconductor structure of claim **1**, further comprising a liner between a portion of the plurality of portions and the dielectric material.

**3**. The semiconductor structure of claim **1**, wherein the dielectric material includes an impurity having a concentration distributed in a linear manner throughout the dielectric material.

**4**. The semiconductor of claim **3**, wherein the impurity includes fluorine.

**5**. The semiconductor structure of claim **1**, wherein the dielectric material has an impurity with a concentration substantially constant throughout the dielectric material.

**6**. The semiconductor of claim **5**, wherein the impurity includes phosphorous.

**7**. The semiconductor of claim **1**, further comprising a plurality of conductors wherein each of the conductors includes a sidewall that is a portion of the surface.

**8**. A semiconductor structure, comprising:

a plurality of conductors;

a spacer disposed on a sidewall of each of the plurality of conductors;

a liner on the spacer and a surface of each of the plurality of conductors; and

a phosphorous doped dielectric material between two conductors of the plurality of conductors, wherein a phosphorous concentration throughout the phosphorous doped dielectric material is substantially constant.

**9**. The semiconductor structure of claim **8**, wherein the phosphorous doped dielectric material includes a thickness substantially equal to a height of the plurality of conductors.

**10**. The semiconductor structure of claim **8**, wherein the phosphorous doped dielectric material includes an aspect ratio equal to or greater than about 2.4.

**11**. The semiconductor structure of claim **8**, wherein the dielectric material has a width smaller than 30 nm.

**12**. The semiconductor structure of claim **8**, wherein the phosphorous doped dielectric material further comprises fluorine.

**13**. The semiconductor structure of claim **12**, wherein a fluorine concentration is distributed in a linear manner throughout the phosphorous doped dielectric material.

**14**. The semiconductor structure of claim **12**, wherein a fluorine concentration is highest at an interface between the phosphorous doped dielectric material and the liner.

**15**. A method of manufacturing a semiconductor structure, comprising:

forming a surface on substrate;

forming a dielectric layer over the surface;

etching the dielectric layer; and

treating a top surface of the dielectric layer with plasma.

**16**. The method of claim **15**, wherein treating the top surface of the dielectric layer is with phosphorous plasma.

**17**. The method of claim **15**, wherein treating the top surface of the dielectric layer is with oxygen plasma.

**18**. The method of claim **15**, wherein etching the dielectric layer is an $NF_3$ etch.

**19**. The method of claim **15**, further comprising repeating forming the dielectric layer.

**20**. The method of claim **15** further comprising forming a liner between the surface and the dielectric layer.

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