(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
10 February 2022 (10.02.2022)

WIPO | PCT

(10) International Publication Number
WO 2022/027428 A1

(51) International Patent Classification:
G09G 3/32 (2016.01)

(21) International Application Number:
PCT/CN2020/107384

(22) International Filing Date:
06 August 2020 (06.08.2020)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **HUAWEI TECHNOLOGIES CO., LTD.** [CN/CN]; Huawei Administration Building, Bantian, Longgang District, Shenzhen, Guangdong 518129 (CN).

(72) Inventors: **LIEN, Cheng-Chieh**; 19F, Concurred-Yokohama, 3-1, Kinko-cho, Kanagawa-ku, Yokohama, Kanagawa 221-0056 (JP). **SAKAIGAWA, Akira**; 19F, Concurred-Yokohama, 3-1, Kinko-cho, Kanagawa-ku, Yokohama, Kanagawa 221-0056 (JP).

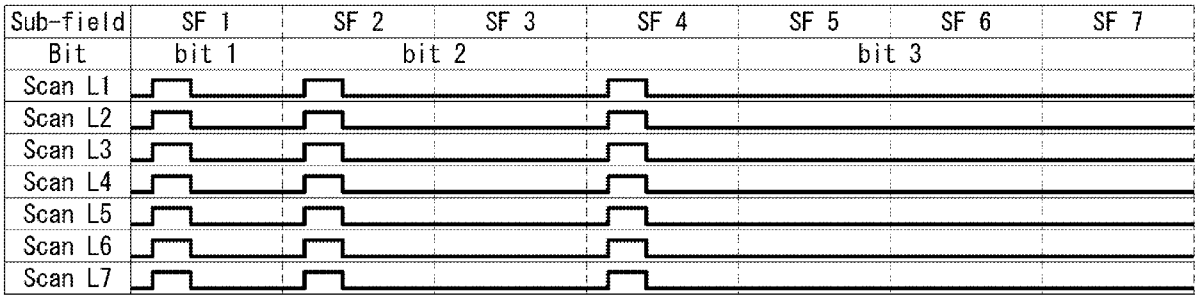
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) **Title:** BLANK SUB-FIELD DRIVING METHOD FOR A DISPLAY DEVICE

FIG. 3



(57) **Abstract:** An operating method of a display device including driving each pixel for each frame, wherein a plurality of pixels of the display device are disposed in an array of rows and columns, a period of one frame comprises one or more data sections and one or more off-sections so that ratios of time length of the data sections are substantially the same as a sequence of powers of 2, each data section corresponds to an ON or OFF period related to the specified brightness, grey scale color, or luminance, and each off-section corresponds to an OFF period unrelated to a specified brightness, grey scale color, or luminance. The method increases available data driving time. One of suitable applications of the present invention is a micro-LED display.

WO 2022/027428 A1

BLANK SUB-FIELD DRIVING METHOD FOR A DISPLAY DEVICE

TECHNICAL FIELD

[0001] The present invention generally relates to a method for driving a display device with pulse-width modulation (PWM).

BACKGROUND

[0002] The technology for light emitting diode (LED) displays has been increasingly developed in recent years. It has a large potential in the flat panel display market. The LED displays can be used in not only large panels such as TV and PC screens, but also tablets, smartphones, and wearable devices. Based on its high PPI (pixels per inch), it also has high potential to be used in AR/VR (augmented reality/virtual reality) application. In the future, micro-LED display can replace LCDs and even also OLED displays.

[0003] In order to display a grey scale color, the micro-LED display is driven in the time domain by using PWM, due to the characteristic different from a liquid crystal display (LCD) and an organic light emitting diode (OLED) display. However, if the number of bits for specifying grey scale colors and the number of lines of a display device increase, the time for driving each pixel becomes short and is insufficient to complete the process.

SUMMARY

[0004] An operating method of a display device is provided to increase available data driving time.

[0005] According to a first aspect, an operating method of a display device is provided, where the method includes driving each pixel for each frame, wherein a plurality of pixels of the display device are disposed in an array of rows and columns, a period of one frame includes one or more data sections and one or more off-sections so that ratios of time length of the data sections are substantially the same as a sequence of powers of 2, each data section corresponds to an ON or OFF period related to the specified brightness, grey scale color, or luminance, and each off-section corresponds to an OFF period unrelated to a specified brightness, grey scale color, or luminance, and.

[0006] In a possible implementation, GSU and Off_section are selected so that the following equation is satisfied:

$$CY \times SF\_number = GSU \times (DSW\_sum - 1) + Off\_section$$

where CY x SF_number corresponds to the period of one frame, SF_number is a number of sub-fields in one frame and is set to a number of the rows, CY is a number of units of time in one sub-field and is set to n + 1, n is a number of bits of data for specifying the brightness, grey scale color, or luminance, GSU is a number of units of time corresponding to a minimum ON period, DSW_sum is a sum of weights of the data sections and is set to 2^n – 1, and Off_section is a number of units of time corresponding to the Off-section.

[0007] In a possible implementation, the driving each pixel for each frame includes driving each pixel for each frame with pulse-width modulation (PWM).

[0008] In a possible implementation, the array corresponds to a part of the display device.

[0009] In a possible implementation, the pixel includes a thin film transistor (TFT).

[0010] In a possible implementation, the pixel includes a silicon substrate.

[0011] In a possible implementation, Vcc is applied to the pixel in an ON period, and Vss is applied to the pixel in the OFF period.

[0012] In a possible implementation, the display device is a micro-LED display.

[0013] According to a second aspect, a display device is provided, where the display device includes a plurality of pixels disposed in an array of rows and columns, a period of one frame includes one or more data sections and one or more off-sections so that ratios of time length of the data sections are substantially the same as a sequence of powers of 2, each data section corresponds to an ON or OFF period related to the specified brightness, grey scale color, or luminance, and each off-section corresponds to an OFF period unrelated to a specified brightness, grey scale color, or luminance, and a driver configured to drive each pixel for each frame.

[0014] In a possible implementation, GSU and Off_section are selected so that the following equation is satisfied:

$$CY \times SF\_number = GSU \times (DSW\_sum - 1) + Off\_section$$

where CY x SF_number corresponds to the period of one frame, SF_number is a number of sub-field in one frame and is set to a number of the rows, CY is a number of units of time in one sub-field and is set to n + 1, n is a number of bits of data for specifying the brightness, grey scale color, or luminance, GSU is a number of units of time corresponding to a minimum ON period, DSW_sum is a sum of weights of the data sections and is set to 2^n – 1, and Off_section is a number of units of time corresponding to the Off-section.

[0015] In a possible implementation, the driver is further configured to drive each pixel for each frame with pulse-width modulation (PWM).

[0016] In a possible implementation, the array corresponds to a part of the display device.

[0017] In a possible implementation, the pixel includes a thin film transistor (TFT).

[0018] In a possible implementation, the pixel includes a silicon substrate.

[0019] In a possible implementation, Vcc is applied to the pixel in the ON period, and Vss is applied to the pixel in the OFF period.

[0020] In a possible implementation, the display device is a micro-LED display.

BRIEF DESCRIPTION OF DRAWINGS

[0021] To describe the technical solutions in the embodiments of the present invention or in the prior art more clearly, the following briefly introduces the accompanying drawings required for describing the embodiments or the prior art.The accompanying drawings in the following description show merely some embodiments of the present invention, and a person of ordinary skill in the art may still derive other drawings from these accompanying drawings without creative efforts.

[0022] FIG. 1 shows a simplified diagram of a PWM light control;

[0023] FIG. 2 shows an example of basic PWM waveforms for driving pixels;

[0024] FIG. 3 shows an example of waveforms for driving pixels;

[0025] FIG. 4 shows another example of waveforms for driving pixels;

[0026] FIG. 5 shows another example of waveforms for driving pixels for 16 grey scales;

[0027] FIG. 6 shows an example of waveforms for driving pixels with ideal binary sections;

[0028] FIG. 7 shows an example of waveforms for bit depth n = 4 and the number of lines p = 13;

[0029] FIG. 8 shows a basic idea of aBlank Sub-field driving sequence;

[0030] FIG. 9 shows a non-recursive driving sequence and a recursive driving sequence;

[0031] FIG. 10 shows an example of waveforms for driving pixels in which bit depth n is 4 and the number of lines p is 13;

[0032] FIG. 11 shows another example of waveforms by the Blank Sub-field scheme;

[0033] FIG. 12 shows comparison of T_{DP} with bit depth = 10 between the Blank Sub-field scheme and the conventional scheme; and

[0034] FIG. 13 shows comparison of T_{DP} with bit depth = 12 between the Blank Sub-field scheme and the conventional scheme.

DESCRIPTION OF EMBODIMENTS

[0035] The following clearly and completely describes the technical solutions in the embodiments of the present invention with reference to the accompanying drawings in the embodiments of the present invention. The described embodiments are only some but not all of the embodiments of the present invention. All other embodiments obtained by a person of ordinary skill in the art based on the embodiments of the present invention without creative efforts shall fall within the protected scope of the present invention.

[0036] FIG. 1 shows a simplified diagram of a PWM light control. The PWM is widely used for driving a light emitting diode (LED). The LED is controlled according to the pulse width so that the LED has different accumulate energy and then has different luminance to achieve different grey scale color. The PWM is to modulate turn-on ratio, or called duty cycle in a period. The higher turn-on ratio be in the period, the higher accumulate energy the LED gets, and the higher accumulate energy the LED gets, the higher luminance the LED provides, and vice versa. For display applications, the PWM period is often set as same as a frame period.

[0037] A pixel may be a circuit for emitting light with a specified color and a specified brightness, grey scale, or luminance. A set of LEDs with red, blue, and green colors may be used for each pixel. However, the embodiments of the present invention focus on controlling brightness, grey scale, or luminance of each LED.

[0038] FIG. 2 shows an example of basic PWM waveforms by a Binary Address Group (BAG) scheme. The BAG scheme is based on digital driving or PWM scheme. It only has a two-state signal (1 or 0) for driving pixels on a display device. Original grey scale data is converted into n-bit binary data, and then a PWM period is divided into n time sections. The length of each time section is not the same but the time length relationship from small to large is 1T, 2T, 4T, 8T, ... The length of the last time section is 2^(n-1)*T. The order of time sections can be changed in any order. The only restriction is the total length of time sections should be (2^n-1)*T. In an example shown in FIG. 2, n = 4 and time sections are arranged from small to large. The total energy or luminance of an LED is in proportion to the sum of the areas under the waveform (grey areas marked "1"). It can be seen that the LED can be driven only by changing states n times (n is 4 in FIG. 2) in one PWM period (for example, changing states at the beginning of 1T, 2T, 3T, and 4T), then we can get 2^n steps (16 steps in FIG. 2) of different energy or luminance can be obtained. The 2^n steps can be used for displaying grey scales and the bit depth of pixel data is n.

[0039] Since each time section above corresponds to one bit data, this time section is also referred to as "a data section" below, and in particular, since in most examples below, the data is binary data, this time section is also referred to as "a binary section", and the length of this time

section is referred to as “a binary length”.

[0040] In general, pixels are disposed in an array of p rows (p scan lines) and q columns (q data lines) on a display device. The pixel may include a thin film transistor (TFT) or a silicon substrate. The array may correspond to all or a part of the display device. All pixels need to be driven in one frame time. The value of q has no relation to the driving time sequences, and the driving time sequences are repeated for q columns, and thus q can be any number, and it can be just assumed to be one for easy to understand.

[0041] FIG. 3 shows an example of waveforms for driving 7 scan lines (7 pixels), and each pixel is driven with 3 bits (hereinafter, each waveform for driving a pixel is also referred to as “a driving sequence”). At the initial part of SF1 (sub-field 1), SF2, and SF4, a high signal means being turned ON, and a low signal means being turned OFF, namely, state changes are performed. First, each line is driven with bit1 (least significant bit (LSB)). After a time period 1T, the same line is driven with bit 2. After a time period 2T, the same line is driven with bit 3 (most significant bit (MSB)). After a time period 4T, this time frame ends.

[0042] In this example, the number of bits for specifying a brightness, grey scale color, or illuminance is n=3, and the sum of the weights of bit1, bit2, and bit3 is 2^n-1 is 7, so one frame time is divided into 7 sub-fields (SFs). However, no processing is performed in SF3, SF5, SF6 and SF7 for driving pixels, namely, a duration of time is not used efficiently. In this method, if the number of lines is p, p*(2^n-1) SFs are needed for driving data.

[0043] FIG. 4 shows another example of driving pixels in an efficient way. The pixel on the Scan L1 line is driven in SF1 for bit 1, SF2 for bit 2, and SF4 for bit 3. For the Scan L2 line, one SF is shifted compared to the Scan L1 line, and the pixel is driven in SF2 for bit 1, SF3 for bit 2, and SF5 for bit 3. For the Scan L3 line, one SF is shifted compared to the Scan L2 line, and the pixel is driven in SF3 for bit 1, SF4 for bit 2, and SF6 for bit 3. The same operations are repeated for the Scan L4 line to the Scan L7 line.

[0044] This kind of driving scheme is called “Binary Address Group (BAG)” driving. The characteristic of the BAG is that the number of small periods for driving pixel data is p*n, which is much smaller than p*(2^n-1) when n becomes larger such as 10, 12, or 14. Only 7*3 = 21 data driving periods are needed in the example of Fig. 4, while 7*7 = 49 data driving periods are needed in the example of Fig. 3, because the SFs with a turn-on signal cannot be simultaneously processed.

[0045] More efficient driving waveforms in one frame can be constructed based on the BAG scheme. It is assumed that the number of rows p is 15, and bit depth n is 4. FIG. 5 shows another example of waveforms for driving pixels for 16 grey scales or 16 linear steps from 0 to 15 for all pixels in 15 lines.

[0046] In FIG. 5, one frame time T_{FRAME} is divided into 15 sub-field times T_{SF} because n=4 and 2^n-1 is 15. Therefore, T_{FRAME} equals 15*T_{SF} in this example. Next, each SF is divided into 4 periods for each bit for a state change. This period is called "available data driving time" represented by T_{DP}, and T_{DP} is a unit of time for constructing a driving sequence. Therefore, T_{SF} equals 4*T_{DP} in this example. In the BAG scheme, the binary length corresponding to each bit is mainly produced by combining SFs. If we set the starting time of the Scan L1 line to be located at SF1, and the order of the binary length is 1, 2, 4, and 8, bits 1, 2, 3 and 4 for state changes are located in SF1, SF2, SF4 and SF8, respectively.

[0047] As mentioned above, there are 15 T_{SF} in one T_{FRAME} and 4 T_{DP} in one T_{SF}. Therefore, there are 60 T_{DP} in one frame (or in one T_{FRAME}). 60 T_{DP} are numbered from 1 to 60 and each position is called an absolute position (AbsPos) in one frame. In FIG. 5, for Scan L1 line, bit 1 is at AbsPos 1, bit 2 is at AbsPos 6, bit 3 is at AbsPos 15, and bit 4 is at AbsPos 32. For Scan L2 line, the starting point is located at first T_{DP} of SF2 which is at AbsPos 5 in this frame. Bits 1, 2, 3 and 4 of Scan L2 line are located at AubPos 5, 10, 19 and 36. For Scan L3 line to Scan L15 line, bits 1, 2, 3, and 4 are located similarly. The periods for holding states for bits 1, 2, 3, and 4 are expected to be 1x, 2x, 4x, and 8x (multiples of 1, 2, 4, and 8, in other words, a sequence of powers of 2), respectively. However, the actual periods are 5*T_{DP}, 9*T_{DP}, 17*T_{DP}, and 29*T_{DP}, as shown in TABLE 1 below. It should be noted that for example, for Scan L1 line, 29* T_{DP} comes from the time length between bit 4 of SF8 of the current frame and bit 1 of SF1 of the next frame. The series 5, 9, 17 and 29 do not comply with binary relationships 1x, 2x, 4x and 8x (in TABLE 1, the column "Multi" shows ratios of "Binary sec 1" to "Binary sec 4" and "Sum" to "Binary sec 1" as multiples of "Binary sec 1"). There exists errors in this solution. Therefore, serial binary sections are non-ideal.

Time Length	T_{SF} + T_{DP}	Value	Multi
Binary sec 1 =	T_{SF}* 1 + T_{DP}* 1	= 5	1
Binary sec 2 =	T_{SF}* 2 + T_{DP}* 1	= 9	1.8
Binary sec 3 =	T_{SF}* 4 + T_{DP}* 1	= 17	3.4
Binary sec 4 =	T_{SF}* 8 + T_{DP}* -3	= 29	5.8
Sum =	T_{SF}* 15 + T_{DP}* 0	= 60	12

TABLE 1. Binary Section Length by Basic BAG Scheme (Bit Depth=4, Line=15)

[0048] FIG. 6 shows an example of waveforms for driving pixels with ideal binary sections. In order to solve the above problem of non-ideal binary sections, the driving waveform is modified. In this example, bit depth n is 4, and the number of lines is 12. First, SFs are divided into 5 periods but not 4 periods. It means T_{SF} equals 5*T_{DP}. The number of periods in one SF is defined as the number of cycles (CY). So, the CY is set to be n+1, which is bit depth + 1. Second, a grey scale unit (GSU)

is determined. GSU corresponds to the number of T_{DP} corresponding to the minimum binary section. In this case, in order to construct a sequence of ideal binary sections, the total length of binary sections will be a multiple of 15, because 1+2+4+8=15. The number of lines is 12, and GSU is selected to be 4. Since the time length of GSU is $4*T_{DP}$, the total length of binary sections is 4*15 which equals 60. Therefore, $T_{FRAME} = 60*T_{DP}$. Since CY = 5, each T_{SF} equals $5*T_{DP}$, there are 12 SFs in one frame, and thereby each SF can be a starting point of one line. Therefore, this is a solution with ideal binary sections for the case where n=4, and the number of lines= 12.

[0049] Besides, there is one difference between the basic BAG scheme (FIG. 5) and the BAG scheme with ideal binary sections (FIG. 6). We can observe that all T_{DP} in one SF are used for driving a pixel in FIG. 5. But there is one T_{DP} which is not used for driving a pixel in FIG. 6. It is the second T_{DP} position in every SF. The T_{DP} without driving a pixel is an "idle" period in each SF. It is an unavoidable sacrifice in timing when trying to use the BAG scheme with ideal binary sections.

[0050] The T_{DP} position in one SF is defined with a relative position (RelPos) so as to be easily described below. For each AbsPos, the relationship between AbsPos and RelPos is

$$AbsPos = (k-1) \times CY + RelPos \quad \cdots\cdots \quad (1)$$

where AbsPos belongs to the k^{th} SF.

[0051] TABLE 2 shows line numbers to be turned ON for each sub-field and each RelPos in the waveforms in FIG. 6. It is easy to check when the waveform sequence becomes long and lines increase significantly. TABLE 3 shows binary section lengths by the BAG Scheme with ideal binary sections (bit depth=4, the number of lines=12).

RelPos	1	2	3	4	5
Bit	Bit 1	Idle	Bit 3	Bit 4	Bit 2
SF 1	1	-	11	8	1
SF 2	2	-	12	9	2
SF 3	3	-	1	10	3
SF 4	4	-	2	11	4
SF 5	5	-	3	12	5
SF 6	6	-	4	1	6
SF 7	7	-	5	2	7
SF 8	8	-	6	3	8
SF 9	9	-	7	4	9
SF 10	10	-	8	5	10
SF 11	11	-	9	6	11
SF 12	12	-	10	7	12

TABLE 2. Line numbers to be turned ON by BAG Scheme with Ideal Binary Sections (Bit Depth=4, Line=12)

Time Length	T_{SF} + T_{DP}	Value	Multi
Binary sec 1 =	T_{SF}* 1 + T_{DP}* -1	= 4	1
Binary sec 2 =	T_{SF}* 2 + T_{DP}* -2	= 8	2
Binary sec 3 =	T_{SF}* 4 + T_{DP}* -4	= 16	4
Binary sec 4 =	T_{SF}* 8 + T_{DP}* -8	= 32	8
Sum =	T_{SF}* 15 + T_{DP}* -15	= 60	15

TABLE 3. Binary Section Length by BAG Scheme with Ideal Binary Sections (Bit Depth=4, Line=12)

[0052] The waveforms for driving pixels in FIG. 6 show ideal binary sections, in which brightness relationship is correct for a display device with p rows. However, the main problem is that the available data driving time T_{DP} is short and it is hard to complete the whole driving action. Also, in some cases, the ideal binary sections cannot use a duration of time in a most optimized way.

[0053] For further discussion, this BAG scheme is summarized with mathematical equations:

$$SF \times CY = GSU \times DSW\_sum \cdots\cdots (2)$$

[0054] DSW_sum means "data section weight sum" that is the sum of the weight of all data sections (binary sections). For example, if n = 4, the sum of the weight of all binary sections is 1 + 2 + 4 + 8 = 15. All BAG solutions need to satisfy equation (2) and the following equation (3):

$$T_{FRAME} = T_{DP} \times SF \times CY \cdots\cdots (3)$$

[0055] T_{DP} is the time period for driving pixels of each line, because T_{FRAME} is fixed once the frame rate is determined. CY depends on bit depth n. If T_{DP} needs to be increased for driving, the number of SFs needs to be decreased. However, as can be seen from the example in FIG. 6, the number of SFs cannot be lower than the number of lines, because each line should be driven once in one frame. Therefore, the principle to find a BAG solution is to find the minimum GSU that satisfies equation (2) and following equation (4):

$$SF \geqslant \text{the number of lines} \cdots\cdots (4)$$

[0056] Using a large number of bits, it is assumed that bit depth n =12, and the number of lines = 630. Then, CY should be n + 1 which is 13 and DSW_sum is 1 + 2 + 4 + ⋯ + 1024 + 2048 = 4095. According to equation (4), the minimum GSU should be 2 and the number of SFs becomes 2 x 4095 / 13 = 630, which satisfies SF $\geqslant$ the number of lines.

[0057] T_{DP} can be derived from equations (2) and (3) as follows:

$$T_{DP} = \frac{T_{SF}}{CY} = \frac{T_{FRAME}}{CY \times SF\_number} = \frac{T_{FRAME}}{GSU \times DSW\_sum} \quad \cdots\cdots \quad (5)$$

[0058] According to equation (5) with CY = 13 and SF_number = 630, T_{DP} is calculated as (T_{FRAME} / 630 / 13) = (T_{FRAME} / 8190). Assuming that frame rate = 60Hz, T_{FRAME} = 1/60 s. Then, T_{DP} is 2.035 us. In some worse cases, it might be insufficient to drive pixels. Thus, it needs to find ways to provide a longer T_{DP} and correct grey scales for each pixel.

[0059] FIG. 7 shows an example of waveforms for bit depth n = 4 and the number of lines p = 13. In FIG. 6, the number of lines is 12, GSU is 4, and there are only 12 SFs which can be starting points for 12 lines in FIG. 6. Since the number of lines is 13 in this case, the same GSU is not used. In this kind of BAG scheme, it is necessary that the number of SFs is larger than the number of lines. Otherwise, it cannot drive pixels in all lines successfully.

[0060] GSU = 6 is selected in this case. The time length of GSU is 6*T_{DP}. Then, the total length of binary sections is 6*15 that equals 90. Therefore, T_{FRAME} = 90*T_{DP} in this case. Because CY = 5, each TSF equals 5*T_{DP}, there are 18 SFs in one frame, and each SF can be a starting point of one line. Therefore, it is a solution for driving pixels with ideal binary sections for the case of n = 4 and the number of lines = 13. For this kind of solution, it always needs to find the minimum SF and the number of SFs should be larger than or equal to the number of lines. The waveforms of this solution is shown in FIG. 7.

[0061] The T_{DP} in FIG. 6 is (T_{FRAME} / 60) and T_{DP} in FIG. 7 is (T_{FRAME} / 90). As bit depth and the number of lines become larger, the T_{DP} becomes shorter and it is not enough to drive pixels correctly.

[0062] TABLE 4 shows line numbers to be turned ON for each sub-field and each RelPos in the waveforms in FIG. 7. TABLE 5 shows binary section length by BAG Scheme with ideal binary sections (bit depth=4, the number of lines=13).

RelPos	1	2	3	4	5
Bit	Bit 1	Bit 2	Bit 4	Bit 3	Idle
SF 1	1	–	11	–	–
SF 2	2	1	12	–	–
SF 3	3	2	13	–	–
SF 4	4	3	–	1	–
SF 5	5	4	–	2	–
SF 6	6	5	–	3	–
SF 7	7	6	–	4	–
SF 8	8	7	–	5	–
SF 9	9	8	1	6	–
SF 10	10	9	2	7	–
SF 11	11	10	3	8	–
SF 12	12	11	4	9	–
SF 13	13	12	5	10	–
SF 14	–	13	6	11	–
SF 15	–	–	7	12	–
SF 16	–	–	8	13	–
SF 17	–	–	9	–	–
SF 18	–	–	10	–	–

TABLE 4. Line numbers to be turned ON by BAG Scheme with Ideal Binary Sections (Bit Depth=4, Line=13)

Time Length	T_{SF} + T_{DP}	Value	Multi
Binary sec 1 =	T_{SF}* 1 + T_{DP}* 1	= 6	1
Binary sec 2 =	T_{SF}* 2 + T_{DP}* 2	= 12	2
Binary sec 3 =	T_{SF}* 4 + T_{DP}* 4	= 24	4
Binary sec 4 =	T_{SF}* 8 + T_{DP}* 8	= 48	8
Sum =	T_{SF}* 15 + T_{DP}* 15	= 90	15

TABLE 5. Binary Section Length by BAG Scheme with Ideal Binary Sections (Bit Depth=4, Line=13)

[0063] In the case of FIG. 6 and FIG. 7, the available data driving time (T_{DP}) is possibly not enough to drive pixels successfully, and when the number of lines increases from 12 to 13, the number of SFs increases from 12 to 18. Because there exists no solution with the numbers of SFs 13, 14, …, 17, the numbers of SFs with ideal binary sections are not consecutive. It is waste of a duration of time in one frame, and thus have room for improvement on timing of the driving

sequence.

[0064] The following describes "Blank Sub-field" driving sequences. Mainly, the idea is to add an off-section after binary sections in a driving sequence. The off-section can be extended. As the off-section extends, the number of SFs in one frame increases. An appropriate time length of an off-section is selected so that the number of SFs equals the number of lines, thereby the number of SFs is enough to drive all lines, and a duration of time is efficiently used than the BAG scheme. The T_{DP} of this Blank Sub-field scheme can be longer than the BAG scheme, and binary sections still comply with binary relationship.

[0065] FIG. 8 shows a basic idea of the Blank Sub-field driving sequence. It shows driving sequences of two rows (or two lines). In this example, bit depth n = 4. In a conventional BAG scheme idea, there are only 4 binary sections in a driving sequence because n is 4. All 4 binary sections are for driving a pixel with data defined by a user. If the data words of row 1 is 0101 in binary code, the 4 binary sections drive the pixel in row 1 with a voltage signal related to 0101. Assuming that voltage V_{CC} represents '1' and voltage V_{SS} represents '0', the 4 binary sections drive row 1 with V_{CC}, V_{SS}, V_{CC}, V_{SS} in order. It should be noted that the first V_{CC} is LSB, and last V_{SS} is MSB. For row 2, the data words of row 2 is 1110, and the 4 binary sections drive row 1 with V_{SS}, V_{CC}, V_{CC}, V_{CC} in order.

[0066] In the Blank Sub-field driving sequence, an extra section is added. In FIG. 8, the extra section is an off-section and put after binary sections. The off-section always drives the pixel with '0' which has no relationship with data words of that pixel. Because this off-section drives the pixel with '0' of an OFF signal, it does not change the grey scale by previous 4 binary sections in display devices such as micro-LED, OLED, or any materials that can be driven by PWM control.

[0067] Row 1 is driven with V_{CC}, V_{SS}, V_{CC}, V_{SS}, and V_{SS}. Row 2 is driven with V_{SS}, V_{CC}, V_{CC}, V_{CC}, and V_{SS}. In row 2, the value of V_{CC} can be a larger or smaller V_{SS}. Also V_{CC} and V_{SS} are not restricted to a positive or negative voltage. In the case where a P-channel TFT is driven, the value of OFF voltage V_{SS} might be larger than V_{CC}.

[0068] When constructing waveform arrangements for a display device with the Blank Sub-field scheme, there are two cases in which a driving sequence of binary sections is recursive and non-recursive. In the recursive case, one more action needs to be taken before adding an off-section to the driving sequence.

[0069] FIG. 9 shows how to arrange binary sections and an off-section in one frame. The recursive case is defined as the case where the total length of binary sections of a driving sequence is a multiple of CY. If the total length of binary sections of a driving sequence is not a multiple of CY, it is a non-recursive case. In the lower part of FIG. 9, in the driving sequence of the recursive

case, the RelPos of a starting point of the binary sections and the RelPos of the position right next to the end of binary sections are the same. This is because the length of binary sections in the driving sequence is divisible by CY, which CY is the number of units of time (T_{DP}) in one SF. The starting point of the next driving sequence is at the same RelPos, as shown by dotted arrows in (1) of Recursive Case. Hence, it is called a recursive case. On the other hand, in the upper part of FIG. 9, if the length of binary sections in the driving sequence is not divisible by CY, as shown by dotted arrows, it is a non-recursive case.

[0070] In the non-recursive case, it is only required to add an off-section after binary sections, and extend the off-section to enough length. Usually, the off-section is extended so that the number of SFs becomes the same as the number of lines. Then, the timing efficiency will be at its highest.

[0071] In the recursive case, an extra action is needed. The binary section corresponding to the MSB is reduced by the length of one unit of length. This unit of length is usually a GSU. The detail steps are shown in the lower part of FIG. 9. It is a simple case of n = 4. (1) judges that the driving sequence is recursive, (2) cuts one GSU from the binary section corresponding to the MSB, and makes the driving sequence non-recursive, and (3) adds an off-section after binary sections, and extends the off-section to enough length.

[0072] An example of a driving sequence for a display device is shown below.

[0073] FIG. 20 shows an example of waveforms for driving pixels in which bit depth n is 4 and the number of lines p is 13. This condition is the same as the example of FIG. 7. These two examples can be compared to find out differences.

[0074] First, the GSU is set to 4. The length of binary sections are 4, 8, 16, 32. The sum of binary sections is 60. We can calculate that the sequence starts from when AbsPos is 1, and its RelPos is 1. The AbsPos of the position right next to the end of binary sections is 61, and its RelPos is 1, too. The value 61 is calculated from 1 + 60. Because the two RelPos are the same, this is a recursive case.

[0075] Second, the binary sections are made to be non-recursive. The binary section corresponding to the MSB is calculated by multiplying GSU and the weight corresponding to the MSB that is 8. Instead of subtracting GSU from the length of the binary section corresponding to the MSB, the length of the non-recursive binary sections can be calculated as follows: subtracting 1 from 8 becomes 7 and multiplying 7 by GSU becomes 28. After that, the RelPos of the position right next to the end of the binary sections is 2.

[0076] Third, an off-section is added after the binary sections. Because the number of lines is 13, the off-section is extended to the length of $9*T_{DP}$. The number of SFs becomes 13 and is perfectly suitable for driving 13 lines.

[0077] Comparing waveforms of FIG. 7 and FIG. 20, it can be seen that only 13 SFs are needed in the Blank Sub-field scheme, but 18 SFs are needed in the "BAG Scheme". The T_{DP} for driving a pixel is enlarged by 18/13 because T_{DP} is (T_{FRAME} / 90) in FIG. 7 and T_{DP} is (T_{FRAME} / 65) in FIG. 20.

[0078] TABLE 6 shows line numbers to be turned ON by the Blank Sub-field scheme (bit depth=4, the number of lines=13). TABLE 7 shows binary section length by the Blank Sub-field scheme (bit depth=4, the number of lines=13).

RelPos	1	2	3	4	5
Bit	Bit 1	Off	Bit 3	Bit 4	Bit 2
SF 1	1	3	12	9	1
SF 2	2	4	13	10	2
SF 3	3	5	1	11	3
SF 4	4	6	2	12	4
SF 5	5	7	3	13	5
SF 6	6	8	4	1	6
SF 7	7	9	5	2	7
SF 8	8	10	6	3	8
SF 9	9	11	7	4	9
SF 10	10	12	8	5	10
SF 11	11	13	9	6	11
SF 12	12	1	10	7	12
SF 13	13	2	11	8	13

TABLE 6. Line numbers to be turned ON by Blank Sub-field scheme (Bit Depth=4, Line=13)

Time Length	T_{SF}	+	T_{DP}		Value	Multi
Binary sec 1 =	T_{SF}*	1 +	T_{DP}*	-1	= 4	1
Binary sec 2 =	T_{SF}*	2 +	T_{DP}*	-2	= 8	2
Binary sec 3 =	T_{SF}*	4 +	T_{DP}*	-4	= 16	4
Binary sec 4 =	T_{SF}*	8 +	T_{DP}*	-12	= 28	7
Off sec =	T_{SF}*	1 +	T_{DP}*	4	= 9	-
Sum =	T_{SF}*	16 +	T_{DP}*	-15	= 65	14

TABLE 7. Binary Section Length by Blank Sub-field scheme (Bit Depth=4, Line=13)

[0079] FIG. 21 shows another example of waveforms by the Blank Sub-field scheme. In this example, bit depth is 4 and the number of lines is 14 (CY = 5, SF_number = 14, DSW_sum = 15, and Off_section = 14). The number of lines is larger than the example in FIG. 20 by one. By the

Blank Sub-field scheme, the number of SFs can be adjusted to fit with the number of lines, and then it is possible to get larger available data driving time (T_{DP}) than the conventional BAG scheme.

[0080] TABLE 8 shows line numbers to be turned ON by the Blank Sub-field scheme (bit depth=4, the number of lines=14). TABLE 9 shows binary section lengths by the Blank Sub-field scheme (bit depth=4, the number of lines=14).

RelPos	1	2	3	4	5
Bit	Bit 1	Off	Bit 3	Bit 4	Bit 2
SF 1	1	4	13	10	1
SF 2	2	5	14	11	2
SF 3	3	6	1	12	3
SF 4	4	7	2	13	4
SF 5	5	8	3	14	5
SF 6	6	9	4	1	6
SF 7	7	10	5	2	7
SF 8	8	11	6	3	8
SF 9	9	12	7	4	9
SF 10	10	13	8	5	10
SF 11	11	14	9	6	11
SF 12	12	1	10	7	12
SF 13	13	2	11	8	13
SF 14	14	3	12	9	14

TABLE 8. Line numbers to be turned ON by Blank Sub-field scheme (Bit Depth=4, Line=14)

Time Length	T_{SF} + T_{DP}	Value	Multi
Binary sec 1 =	T_{SF}* 1 + T_{DP}* -1	= 4	1
Binary sec 2 =	T_{SF}* 2 + T_{DP}* -2	= 8	2
Binary sec 3 =	T_{SF}* 4 + T_{DP}* -4	= 16	4
Binary sec 4 =	T_{SF}* 8 + T_{DP}* -12	= 28	7
Off sec =	T_{SF}* 2 + T_{DP}* 4	= 14	-
Sum =	T_{SF}* 17 + T_{DP}* -15	= 70	14

TABLE 9. Binary Section Length by Blank Sub-field scheme (Bit Depth=4, Line=14)

[0081] TABLE 10 shows another example of the Blank Sub-field driving. In this example, bit depth is 10 and the number of lines is 960. This condition is closer to an actual display device. As the bit depth and the number of lines increase, it is too difficult to show complete waveforms for driving pixels. So, the waveforms are not shown in a figure, and only line numbers to be turned ON

are shown in TABLE 10. This table shows which line is turned ON at each T_{DP}. Each value in table shows which line is turned ON at the T_{DP} position. The T_{DP} position is at a certain RelPos in a certain SF. The relationship between the waveforms and the table is the same as FIG. 20 and TABLE 6, and FIG. 21 and TABLE 8.

[0082] In TABLE 10, 10 is selected as GSU. Because n = 10, the sum of the weight of binary sections (DSW_sum) = 1+2+4+…+256+512 = 1023, so the length of the binary sections is 10*1023 = 10,230. This is a recursive case and the length of the binary section needs to be modified to 1023 – 1 = 1022. Thus, the corrected length of the binary section is 10*1022 = 10,220. For n = 10, CY is set to be 11. For the Blank Sub-field scheme, the number of SFs is set to be the same as the number of SFs to get best time use efficiency. So, the number of SF is 960. Total number of T_{DP} in one frame is 960 * 11 = 10,560. If the frame rate of this display device is 60Hz, we can obtain the available data driving time T_{DP} of 1/60/10560 = 1.578 us. The equation for calculating T_{DP} for Blank Sub-field scheme is:

$$T_{DP} = \frac{T_{SF}}{CY} = \frac{T_{FRAME}}{CY \times SF\_number} = \frac{T_{FRAME}}{GSU \times (DSW\_sum - 1) + (Off\_section)} \quad \cdots\cdots (6)$$

$$Off\_section = GSU + BSF\_number \times CY \quad \cdots\cdots (7)$$

[0083] The length of the off-section is GSU plus a multiple of CY and the number of T_{DP} included in Blank Sub-field (BSF) ("BSF_number" in equation (7)). Finally, the length of binary sections is 10,220; the length of the off-section is 10,560-10,220 = 340. In this way, GSU and Off_section (the length of the off-section) are selected so that the following equation is satisfied: CY x SF_number = GSU x (DSW_sum – 1) + Off_section, where SF_number is the number of SFs in one frame. In complete waveforms in TABLE 10, the starting point of Scan L1 line in one frame is set to AbsPos = 1. The order of binary sections is set as following series: 1x, 2x, 4x, 8x, … , 256x, 511x, off-section.

RelPos	1	2	3	4	5	6	7	8	9	10	11
Bit	Bit1	Off	Bit6	Bit7	Bit4	Bit8	Bit10	Bit5	Bit3	Bit9	Bit2
SF 1	1	32	933	904	955	846	497	948	959	730	1
SF 2	2	33	934	905	956	847	498	949	960	731	2
SF 3	3	34	935	906	957	848	499	950	1	732	3
SF 4	4	35	936	907	958	849	500	951	2	733	4
SF 5	5	36	937	908	959	850	501	952	3	734	5
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
SF 478	478	509	450	421	472	363	14	465	476	247	478
SF 479	479	510	451	422	473	364	15	466	477	248	479
SF 480	480	511	452	423	474	365	16	467	478	249	480
SF 481	481	512	453	424	475	366	17	468	479	250	481
SF 482	482	513	454	425	476	367	18	469	480	251	482
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
SF 956	956	27	928	899	950	841	492	943	954	725	956
SF 957	957	28	929	900	951	842	493	944	955	726	957
SF 958	958	29	930	901	952	843	494	945	956	727	958
SF 959	959	30	931	902	953	844	495	946	957	728	959
SF 960	960	31	932	903	954	845	496	947	958	729	960

TABLE 10. Line numbers to be turned ON by Blank Sub-field scheme (Bit Depth=10, Line=960)

[0084] TABLE 11 shows an example in which bit depth is 12 and the number of lines is 960. The bit depth increases by 2 bits and the same number of lines is kept compared to the example in TABLE 10. In this case, 3 is selected as GSU. Because n = 12, 1+2+4+...+1024+2048 = 4095, so the length of binary sections is 3*4095 = 12,285. This is a recursive case and the length of the binary section needs to be modified to 4095 – 1 = 4094. Thus, the corrected length of the binary section is 3*4094 = 12,282. For n = 12, CY is set to be 13. For the Blank Sub-field driving, the number of SFs is set to be the same as the number of lines to get best time use efficiency. So, the number of SFs is 960. Total number of T_{DP} in one frame is 960 * 13 = 12,480. If the frame rate of this display device is 60Hz, the available data driving time T_{DP} is 1/60/12560 = 1.335 us.

[0085] The length of the off-section is GSU plus a multiple of CY and the number of BSF (Blank Sub-field). Finally, the length of the binary sections is 12,282, and the length of the off-section is 12,480-12,282 = 198. In complete waveforms in TABLE 11, the starting point of Scan L1 line in one frame is set at AbsPos = 1. The order of binary sections is set as following series: 1x, 2x, 4x, 8x, … , 1024x, 2047x, off-section.

RefPos	1	2	3	4	5	6	7	8	9	10	11	12	13
Bit	Bit1	Bit11	Bit6	Bit2	Bit8	Bit12	Bit5	Bit7	Bit4	Bit3	Off	Bit9	Bit10
SF 1	1	725	954	1	932	489	958	947	960	1	17	903	844
SF 2	2	726	955	2	933	490	959	948	1	2	18	904	845
SF 3	3	727	956	3	934	491	960	949	2	3	19	905	846
SF 4	4	728	957	4	935	492	1	950	3	4	20	906	847
SF 5	5	729	958	5	936	493	2	951	4	5	21	907	848
...	...	...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...
SF 478	478	242	471	478	449	6	475	464	477	478	494	420	361
SF 479	479	243	472	479	450	7	476	465	478	479	495	421	362
SF 480	480	244	473	480	451	8	477	466	479	480	496	422	363
SF 481	481	245	474	481	452	9	478	467	480	481	497	423	364
SF 482	482	246	475	482	453	10	479	468	481	482	498	424	365
...	...	...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...
SF 956	956	720	949	956	927	484	953	942	955	956	12	898	839
SF 957	957	721	950	957	928	485	954	943	956	957	13	899	840
SF 958	958	722	951	958	929	486	955	944	957	958	14	900	841
SF 959	959	723	952	959	930	487	956	945	958	959	15	901	842
SF 960	960	724	953	960	931	488	957	946	959	960	16	902	843

TABLE 11. Line numbers to be turned ON by Blank Sub-field scheme (Bit Depth=12, Line=960)

[0086] As application scenarios, the embodiments of the present invention can be mainly used for driving micro-LED display devices. Not only micro-LED displays but also any other display devices can be driven by PWM control such as a display device with a bi-stable emission device. From a product point of view, the embodiments of the present invention can be used in any kind of displays in consumer electronics, automotive, and industrial products.

[0087] For micro-LED display devices, the number of rows * the number of columns is p * q, the Blank Sub-field scheme of the embodiment of the present invention can provide a driving sequence for driving pixels including binary sections and at least one off-section. The binary sections usually have binary relationship but is not restricted to only binary. Other than binary (2-carry) relationship between binary sections, 3-carry, 4-carry, or m-carry relationship also can be used in the Blank Sub-field scheme. The m-carry system means data sections have the multiple relationship: 1, m, m^2, m^3, ...

[0088] According to the embodiments of the present invention, all of p * q pixels in an array of

a display device can display correct grey scale colors and the available data driving time is arranged in an optimized way.

[0089] The effects and advantages by the embodiments of the present invention are as follows:

[0090] The most significant improvement of the embodiments of the present invention is that the available data driving time T_{DP} is increased. The larger T_{DP} makes it easier to drive each pixel with correct data or voltage. So, color performance of the micro-LED is improved.

[0091] In the case of the BAG scheme, the equation for calculating T_{DP} is:

$$T_{DP} = \frac{T_{SF}}{CY} = \frac{T_{FRAME}}{CY \times SF\_number} = \frac{T_{FRAME}}{GSU \times DSW\_sum} \quad \cdots\cdots \quad (5)$$

[0092] As previously explained with reference to TABLE 10 for the Blank Sub-field scheme, the equation for calculating T_{DP} is:

$$T_{DP} = \frac{T_{SF}}{CY} = \frac{T_{FRAME}}{CY \times SF\_number} = \frac{T_{FRAME}}{GSU \times (DSW\_sum - 1) + (Off\_section)} \quad \cdots\cdots \quad (6)$$

[0093] In the case where bit depth is 10 and the number of lines is 960, for the BAG scheme, DSW_sum is 1023, CY is 11, and GSU is selected to 12 so that 1023*12/11 = 1116 according to equation (2). 1116 is the minimum number of SFs that is greater than or equal to 960 in the BAG scheme. Thus, T_{DP} is 1/60/11/1116 = 1.358 us according to equation (5) with T_{FRAME} is 1/60, CY = 11, and SF_number = 1116. On the contrary, T_{DP} of the Blank Sub-field scheme is calculated as 1.578 us according to equation (6) with Off_section = 12, and it is longer than T_{DP} in the BAG scheme by 16%.

[0094] In the case where bit depth is 12 and the number of lines is 960, for the BAG scheme, DSW_sum is 4095, CY is 13, and GSU is selected to 4 so that 4095*4/13 = 1260 according to equation (2). 1260 is the minimum number of SFs that is greater than or equal to 960 in the BAG scheme. Thus, T_{DP} is 1/60/13/1260 = 1.018 us according to equation (5) with T_{FRAME} is 1/60, CY = 13, and SF_number = 1260. On the contrary, T_{DP} of the Blank Sub-field scheme is calculated as 1.335 us according to equation (6) with Off_section = 4, and it is longer than T_{DP} in the BAG scheme by 31%.

[0095] TABLE 12 to TABLE 14 show T_{DP} improvement from the BAG scheme (without BSF) to the Blank Sub-field scheme in the following cases: bit depth is 4 and the number of lines is 13 in TABLE 12, bit depth is 10 and the number lines is 960 in TABLE 13, and bit depth is 12 and the number of lines is 960 in TABLE 14.

Driving Scheme	Bit Depth	Number of Lines	CY	GSU	Number of SFs	T_{SF} (ms)	T_{DP} (us)	ΔT_{DP} %
Without BSF	4	13	5	6	18	0.926	185.2	-
With BSF	4	13	5	4	13	1.282	256.4	38.4%

TABLE 12. T_{DP} Improvement by Blank Sub-field scheme (Bit Depth = 4)

Driving Scheme	Bit Depth	Number of Lines	CY	GSU	Number of SFs	T_{SF} (us)	T_{DP} (us)	ΔT_{DP} %
Without BSF	10	960	11	12	1,116	14.93	1.358	-
With BSF	10	960	11	10	960	17.36	1.578	16.3%

TABLE 13. T_{DP} Improvement by Blank Sub-field scheme (Bit Depth = 10)

Driving Scheme	Bit Depth	Number of Lines	CY	GSU	Number of SFs	T_{SF} (us)	T_{DP} (us)	ΔT_{DP} %
Without BSF	12	960	13	4	1,260	13.23	1.018	-
With BSF	12	960	13	3	960	17.36	1.335	31.3%

TABLE 14. T_{DP} Improvement by Blank Sub-field scheme (Bit Depth = 12)

[0096] TABLE 12 to TABLE 14 show that by using the Blank Sub-field scheme, the number of SFs can always be set to the same as the number of lines. And then get a larger available data driving time in driving sequence. For different display resolutions, there are different number of lines.

[0097] FIG. 22 and FIG. 23 show comparison of T_{DP} between the Blank Sub-field scheme and the conventional scheme for different display devices with the number of lines from 800 to 1,300. The x-axis denotes the number of lines of display devices and y-axis denotes available data driving time T_{DP}. We can observe that the shape of the graph for the Blank Sub-field scheme is consecutive and that for the conventional scheme is non-consecutive. For a certain number of lines, the difference in the vertical direction indicates T_{DP} improvement by the Blank Sub-field scheme from the conventional scheme. The timing improvement of the embodiments of the present invention is about 0% to 35%, and depends on the number of lines of display devices.

[0098] The embodiments of the present invention can be applied to not only micro-LED displays, but also display devices with other materials using PWM control, digital driving, or analog

and digital combined driving.

[0099] What is disclosed above is merely exemplary embodiments of the present invention, and certainly is not intended to limit the protection scope of the present invention. A person of ordinary skill in the art may understand that all or some of processes that implement the foregoing embodiments and equivalent modifications made in accordance with the claims of the present invention shall fall within the scope of the present invention.

CLAIMS

What is claimed is:

1.An operating method of a display device comprising:

driving each pixel for each frame, wherein a plurality of pixels of the display device are disposed in an array of rows and columns, a period of one frame comprises one or more data sections and one or more off-sections so that ratios of time length of the data sections are substantially the same as a sequence of powers of 2, each data section corresponds to an ON or OFF period related to the specified brightness, grey scale color, or luminance, and each off-section corresponds to an OFF period unrelated to a specified brightness, grey scale color, or luminance.

2. The operating method according to claim 1, wherein GSU and Off_section are selected so that the following equation is satisfied:

$$CY \times SF\_number = GSU \times (DSW\_sum - 1) + Off\_section$$

wherein CY x SF_number corresponds to the period of one frame, SF_number is a number of sub-fields in one frame and is set to a number of the rows, CY is a number of units of time in one sub-field and is set to n + 1, n is a number of bits of data for specifying the brightness, grey scale color, or luminance, GSU is a number of units of time corresponding to a minimum ON period, DSW_sum is a sum of weights of the data sections and is set to 2^n – 1, and Off_section is a number of units of time corresponding to the Off-section.

3. The operating method according to claim 1 or 2, wherein the driving each pixel for each frame comprises driving each pixel for each frame with pulse-width modulation (PWM).

4. The operating method according to any one of claims 1 to 3, wherein the array corresponds to a part of the display device.

5. The operating method according to any one of claims 1 to 4, wherein the pixel comprises a thin film transistor (TFT).

6. The operating method according to any one of claims 1 to 4, wherein the pixel comprises a silicon substrate.

7. The operating method according to any one of claims 1 to 6, wherein Vcc is applied to the pixel in an ON period, and Vss is applied to the pixel in the OFF period.

8. The operating method according to any one of claims 1 to 7, wherein the display device is a micro-LED display.

9. A display device comprising:

a plurality of pixels disposed in an array of rows and columns, wherein a period of one frame

comprises one or more data sections and one or more off-sections so that ratios of time length of the data sections are substantially the same as a sequence of powers of 2, each data section corresponds to an ON or OFF period related to the specified brightness, grey scale color, or luminance, and each off-section corresponds to an OFF period unrelated to a specified brightness, grey scale color, or luminance, and

a driver configured to drive each pixel for each frame.

10. The display device according to claim 9, wherein GSU and Off_section are selected so that the following equation is satisfied:

$$CY \times SF\_number = GSU \times (DSW\_sum - 1) + Off\_section$$

wherein CY x SF_number corresponds to the period of one frame, SF_number is a number of sub-field in one frame and is set to a number of the rows, CY is a number of units of time in one sub-field and is set to n + 1, n is a number of bits of data for specifying the brightness, grey scale color, or luminance, GSU is a number of units of time corresponding to a minimum ON period, DSW_sum is a sum of weights of the data sections and is set to 2^n – 1, and Off_section is a number of units of time corresponding to the Off-section.

11. The display device according to claim 9 or 10, wherein the driver is further configured to drive each pixel for each frame with pulse-width modulation (PWM).

12. The display device according to any one of claims 9 to 11, wherein the array corresponds to a part of the display device.

13. The display device according to any one of claims 9 to 12, wherein the pixel comprises a thin film transistor (TFT).

14. The display device according to any one of claims 9 to 12, wherein the pixel comprises a silicon substrate.

15. The display device according to any one of claims 9 to 14, wherein Vcc is applied to the pixel in the ON period, and Vss is applied to the pixel in the OFF period.

16. The display device according to any one of claims 9 to 15, wherein the display device is a micro-LED display.

FIG. 1

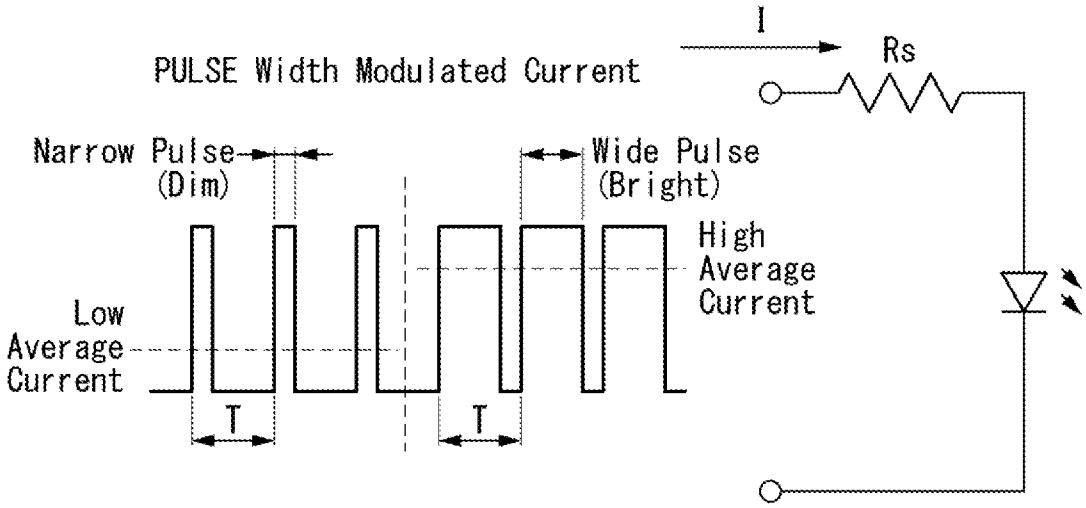

I
Rs
PULSE Width Modulated Current
Narrow Pulse
(Dim)
Wide Pulse
(Bright)
High
Average
Current
Low
Average
Current
T
T

FIG. 2

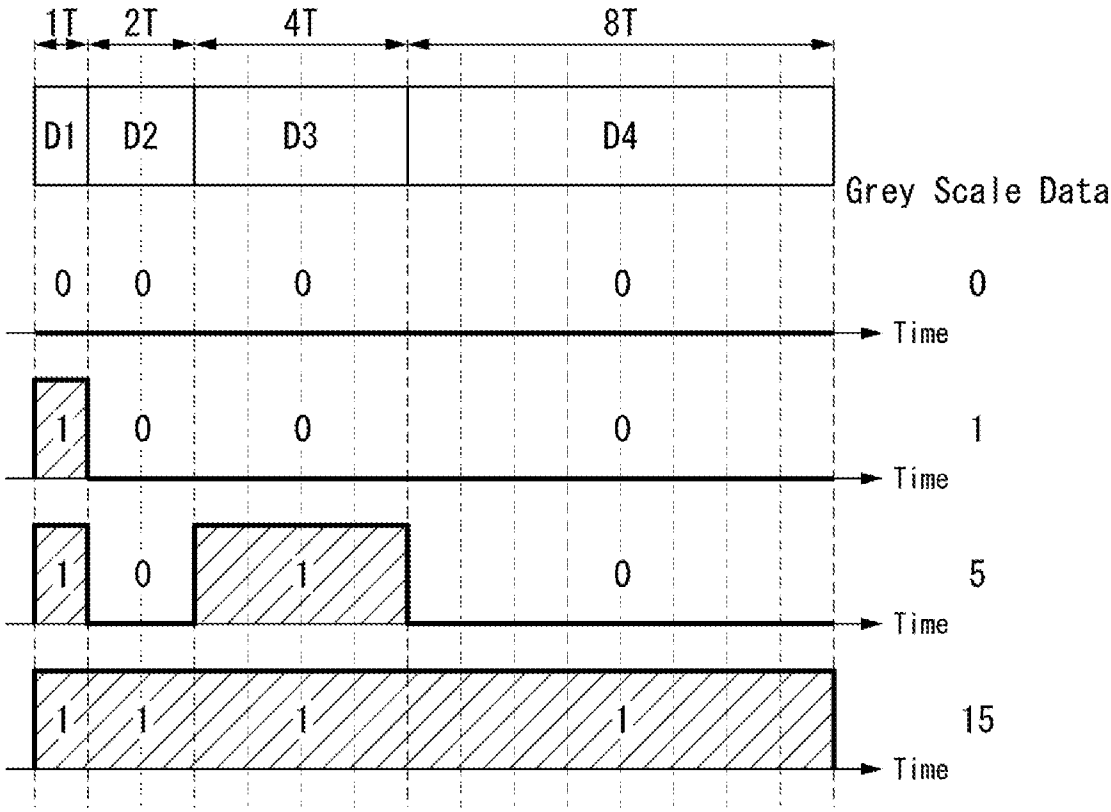

1T
2T
4T
8T
D1
D2
D3
D4
Grey Scale Data
0 0 0 0 0
Time
1 0 0 0 1
Time
1 0 1 0 5
Time
1 1 1 1 15
Time

FIG. 3

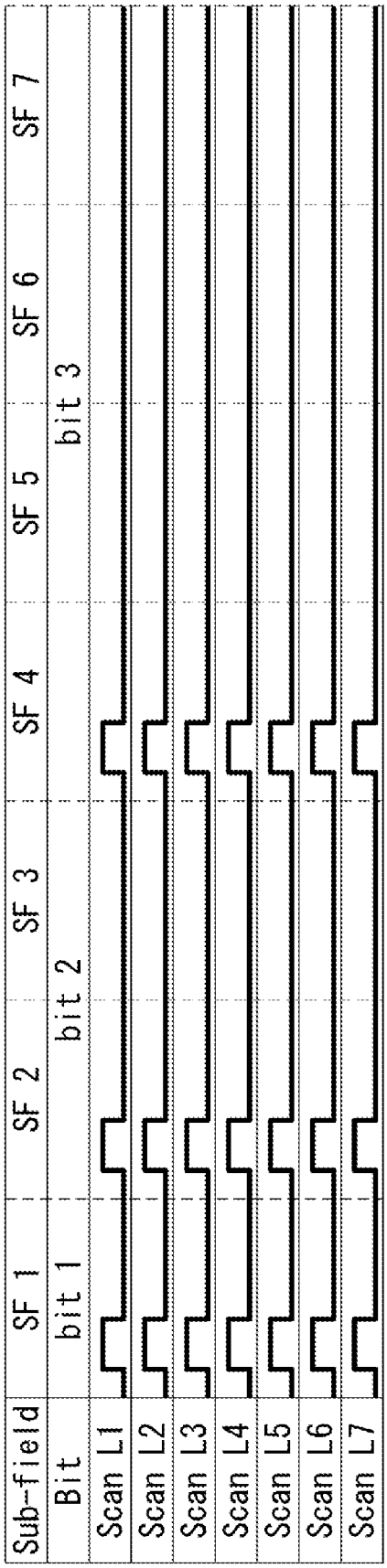
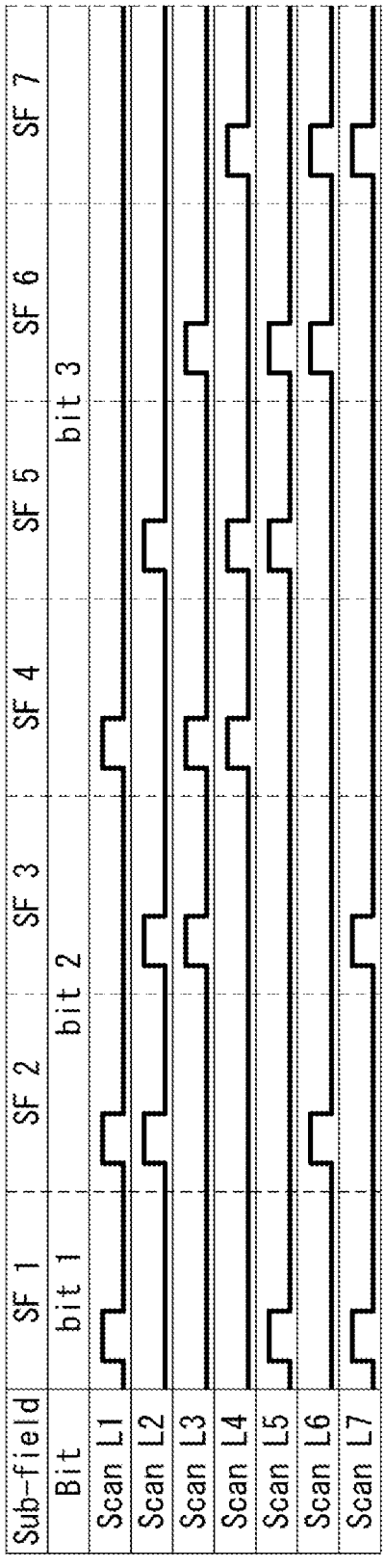

Sub-field
SF 1
SF 2
SF 3
SF 4
SF 5
SF 6
SF 7
Bit
bit 1
bit 2
bit 3
Scan L1
Scan L2
Scan L3
Scan L4
Scan L5
Scan L6
Scan L7

FIG. 4


Sub-field
SF 1
SF 2
SF 3
SF 4
SF 5
SF 6
SF 7
Bit
bit 1
bit 2
bit 3
Scan L1
Scan L2
Scan L3
Scan L4
Scan L5
Scan L6
Scan L7

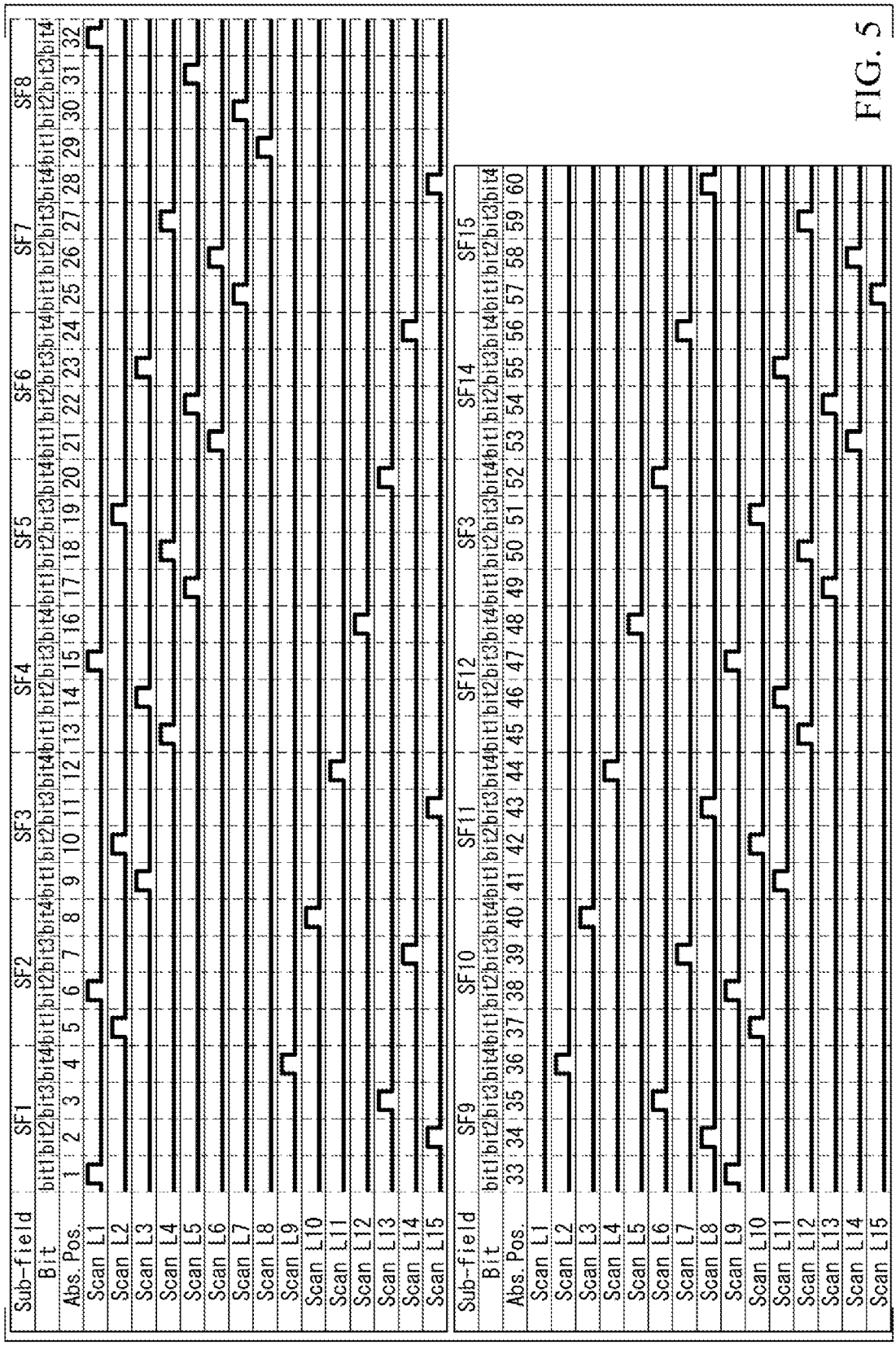

Sub-field SF1 SF2 SF3 SF4 SF5 SF6 SF7 SF8
Bit bit1 bit2 bit3 bit4 bit1 bit2 bit3 bit4 bit1 bit2 bit3 bit4 bit1 bit2 bit3 bit4 bit1 bit2 bit3 bit4 bit1 bit2 bit3 bit4
Abs. Pos. 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
Scan L1
Scan L2
Scan L3
Scan L4
Scan L5
Scan L6
Scan L7
Scan L8
Scan L9
Scan L10
Scan L11
Scan L12
Scan L13
Scan L14
Scan L15
Sub-field SF9 SF10 SF11 SF12 SF3 SF14 SF15
Bit bit1 bit2 bit3 bit4 bit1 bit2 bit3 bit4 bit1 bit2 bit3 bit4 bit1 bit2 bit3 bit4 bit1 bit2 bit3 bit4 bit1 bit2 bit3 bit4
Abs. Pos. 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60
Scan L1
Scan L2
Scan L3
Scan L4
Scan L5
Scan L6
Scan L7
Scan L8
Scan L9
Scan L10
Scan L11
Scan L12
Scan L13
Scan L14
Scan L15

FIG. 5

FIG. 6

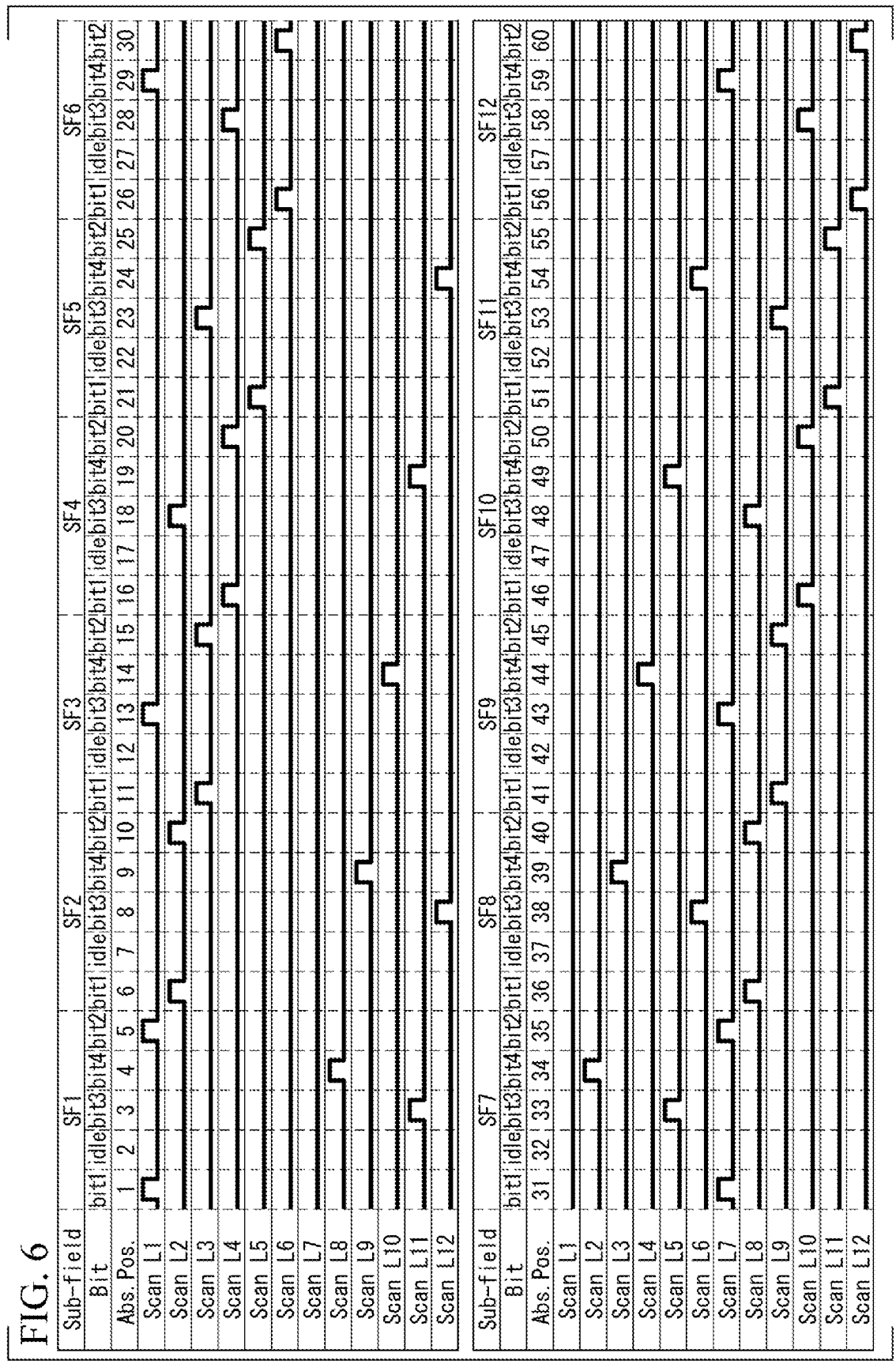

Sub-field SF1 SF2 SF3 SF4 SF5 SF6
Bit bit1 idle bit3 bit4 bit2 bit1 idle bit3 bit4 bit2 bit1 idle bit3 bit4 bit2 bit1 idle bit3 bit4 bit2
Abs. Pos. 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30
Scan L1
Scan L2
Scan L3
Scan L4
Scan L5
Scan L6
Scan L7
Scan L8
Scan L9
Scan L10
Scan L11
Scan L12
Sub-field SF7 SF8 SF9 SF10 SF11 SF12
Bit bit1 idle bit3 bit4 bit2 bit1 idle bit3 bit4 bit2 bit1 idle bit3 bit4 bit2 bit1 idle bit3 bit4 bit2 bit1 idle bit3 bit4 bit2
Abs. Pos. 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60
Scan L1
Scan L2
Scan L3
Scan L4
Scan L5
Scan L6
Scan L7
Scan L8
Scan L9
Scan L10
Scan L11
Scan L12

FIG. 7

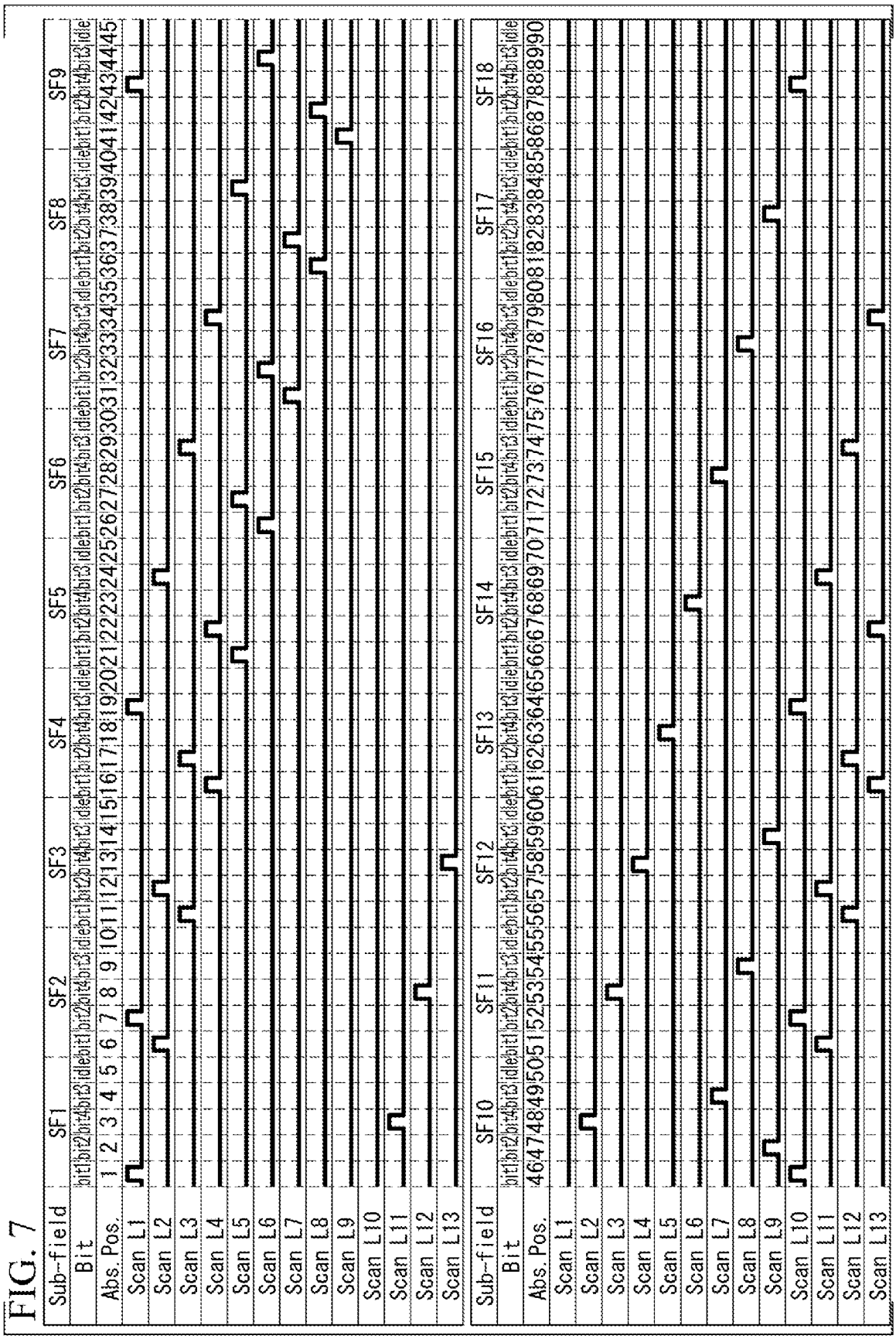

Sub-field
SF1
SF2
SF3
SF4
SF5
SF6
SF7
SF8
SF9
Bit
Abs. Pos.
Scan L1
Scan L2
Scan L3
Scan L4
Scan L5
Scan L6
Scan L7
Scan L8
Scan L9
Scan L10
Scan L11
Scan L12
Scan L13
SF10
SF11
SF12
SF13
SF14
SF15
SF16
SF17
SF18

FIG. 8

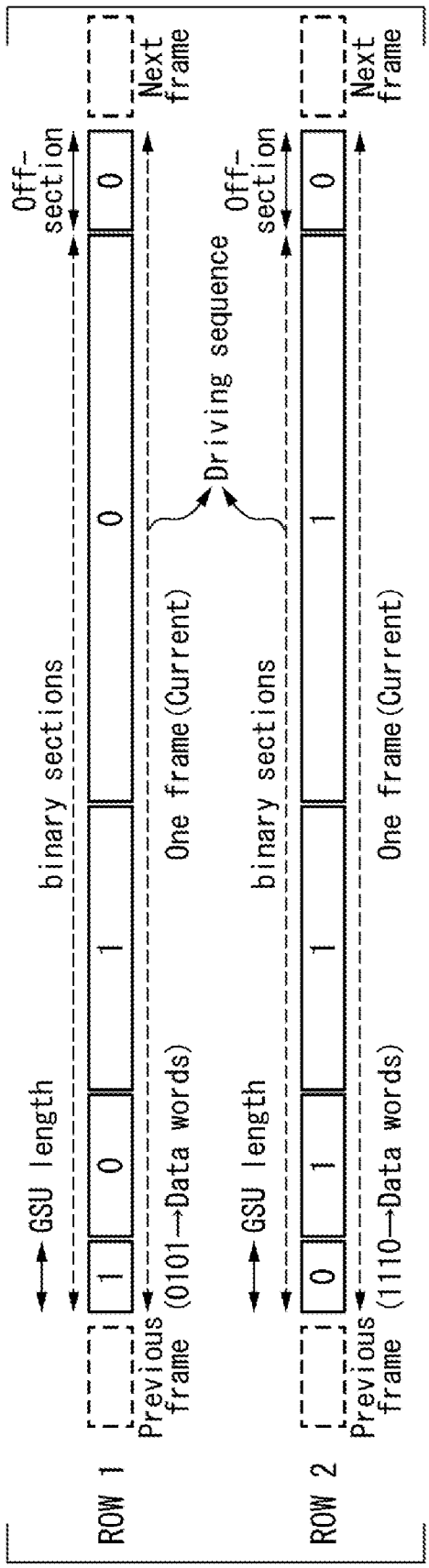

ROW 1
ROW 2
Previous frame
(0101→Data words)
(1110→Data words)
GSU length
binary sections
One frame(Current)
Driving sequence
Off-section
Next frame
1
0

FIG. 9

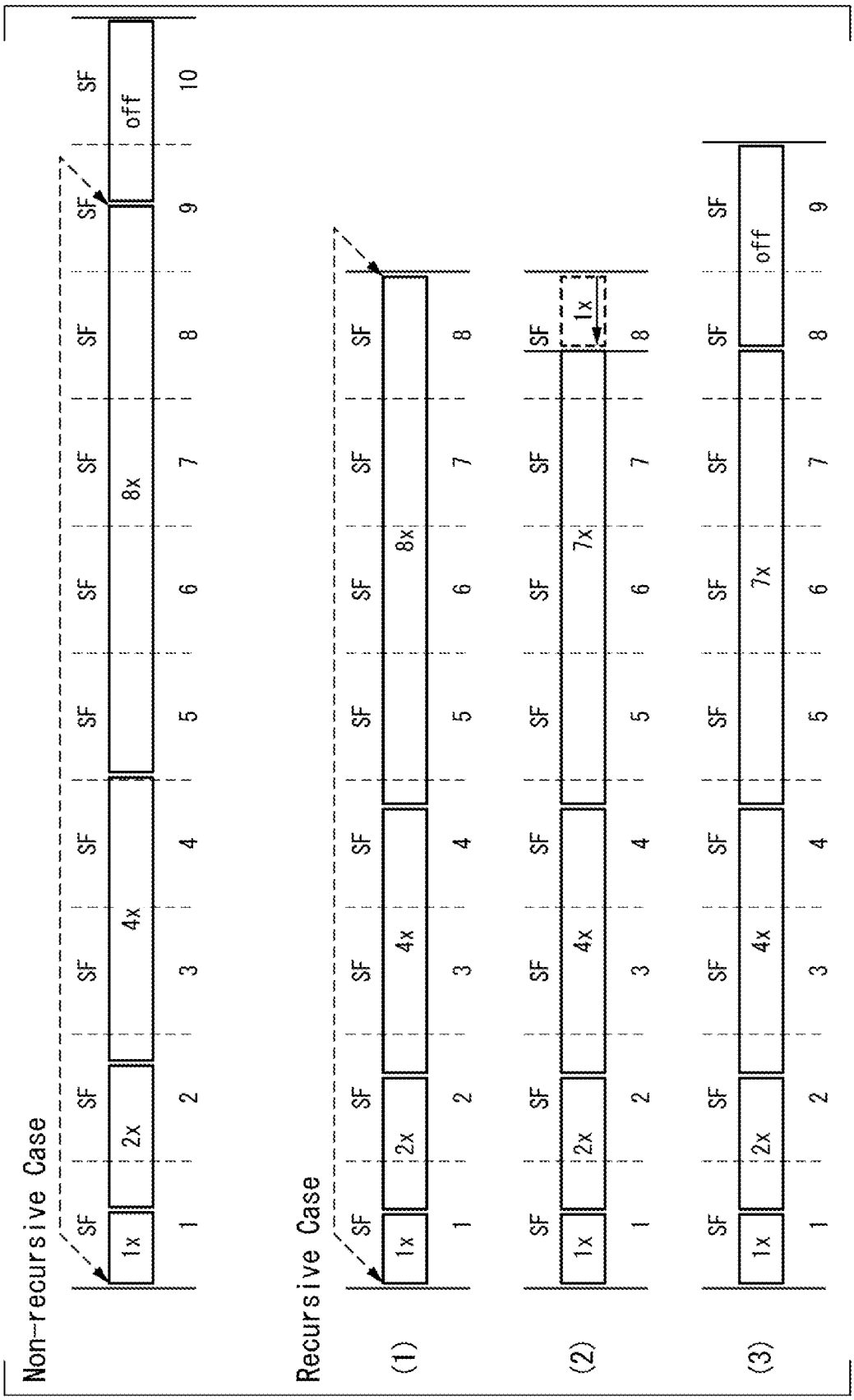

Non-recursive Case
SF
1x
2x
4x
8x
off
1 2 3 4 5 6 7 8 9 10
Recursive Case
(1)
(2)
(3)
1x
2x
4x
8x
7x
off
1 2 3 4 5 6 7 8
1 2 3 4 5 6 7 8
1 2 3 4 5 6 7 9

FIG. 10

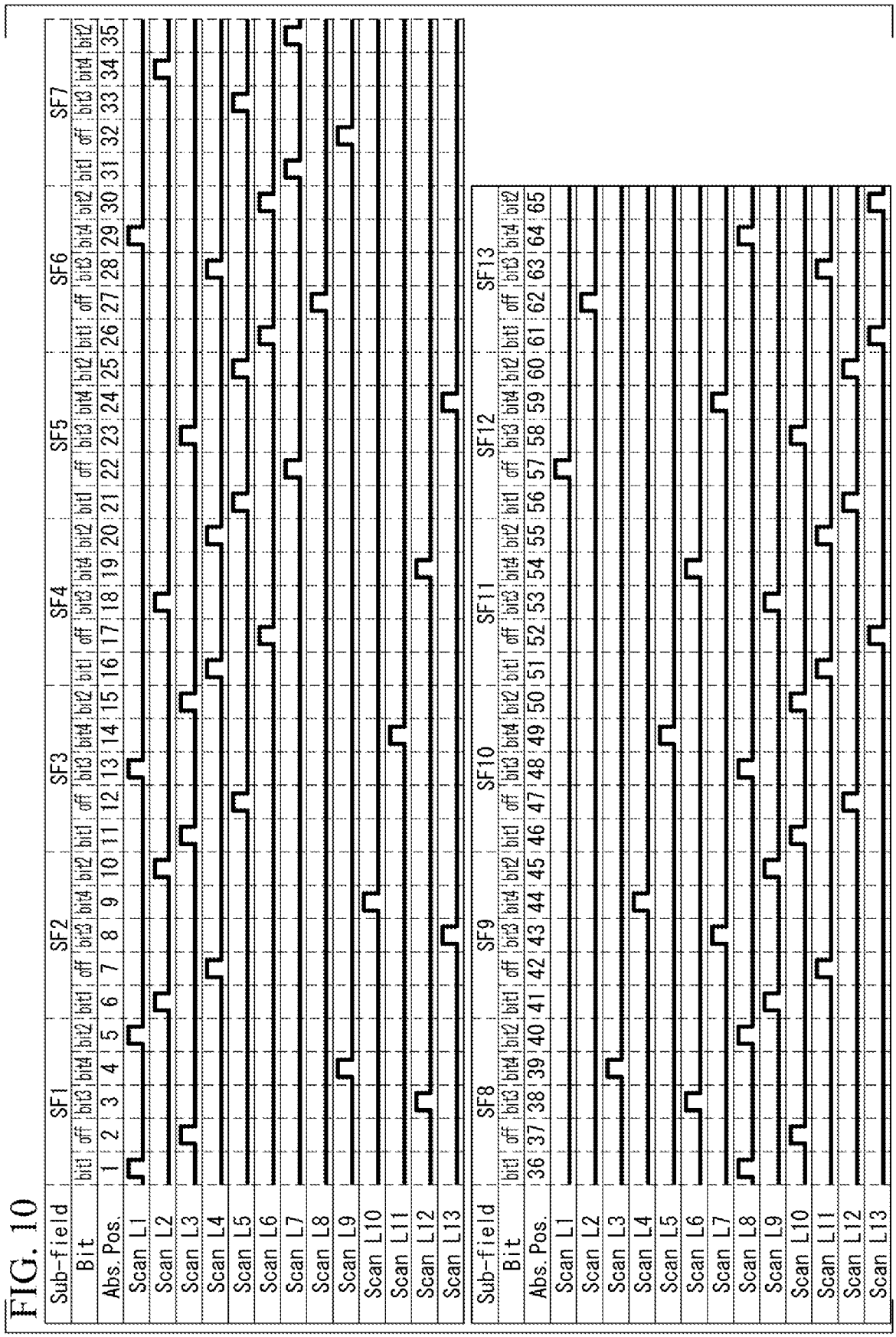

Sub-field
SF1
SF2
SF3
SF4
SF5
SF6
SF7
Bit
bit1 off bit3 bit4 bit2 bit1 off bit3 bit4 bit2 bit1 off bit3 bit4 bit2 bit1 off bit3 bit4 bit2 bit1 off bit3 bit4 bit2
Abs. Pos.
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
Scan L1
Scan L2
Scan L3
Scan L4
Scan L5
Scan L6
Scan L7
Scan L8
Scan L9
Scan L10
Scan L11
Scan L12
Scan L13
Sub-field
SF8
SF9
SF10
SF11
SF12
SF13
Bit
bit1 off bit3 bit4 bit2 bit1 off bit3 bit4 bit2 bit1 off bit3 bit4 bit2 bit1 off bit3 bit4 bit2 bit1 off bit3 bit4 bit2
Abs. Pos.
36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65
Scan L1
Scan L2
Scan L3
Scan L4
Scan L5
Scan L6
Scan L7
Scan L8
Scan L9
Scan L10
Scan L11
Scan L12
Scan L13

FIG. 11

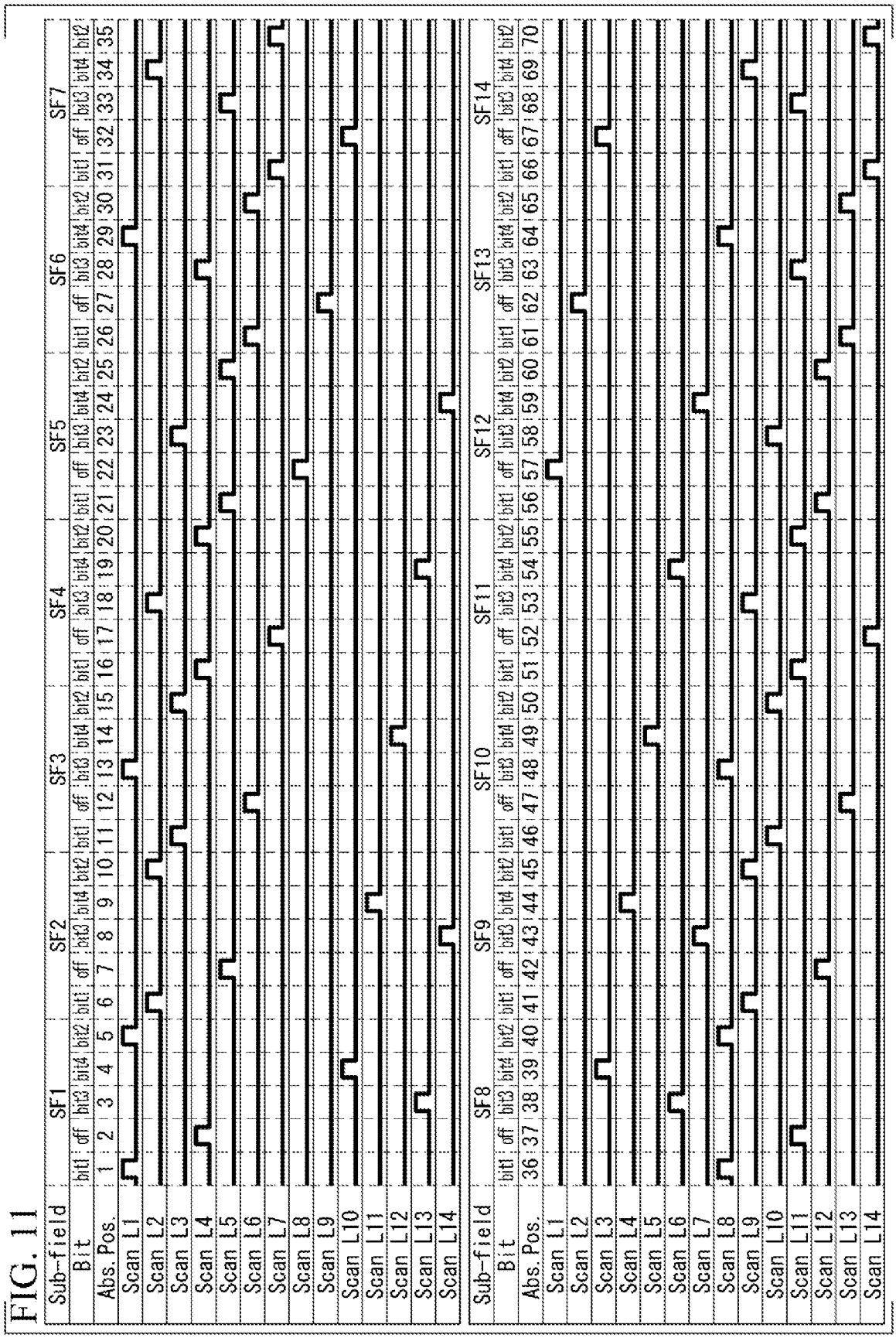

Sub-field
SF1
SF2
SF3
SF4
SF5
SF6
SF7
Bit
bit1 off bit3 bit4 bit2 bit1 off bit3 bit4 bit2 bit1 off bit3 bit4 bit2 bit1 off bit3 bit4 bit2 bit1 off bit3 bit4 bit2
Abs. Pos.
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
Scan L1
Scan L2
Scan L3
Scan L4
Scan L5
Scan L6
Scan L7
Scan L8
Scan L9
Scan L10
Scan L11
Scan L12
Scan L13
Scan L14
Sub-field
SF8
SF9
SF10
SF11
SF12
SF13
SF14
Bit
bit1 off bit3 bit4 bit2 bit1 off bit3 bit4 bit2 bit1 off bit3 bit4 bit2 bit1 off bit3 bit4 bit2 bit1 off bit3 bit4 bit2 bit1 off bit3 bit4 bit2
Abs. Pos.
36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70
Scan L1
Scan L2
Scan L3
Scan L4
Scan L5
Scan L6
Scan L7
Scan L8
Scan L9
Scan L10
Scan L11
Scan L12
Scan L13
Scan L14

FIG. 12

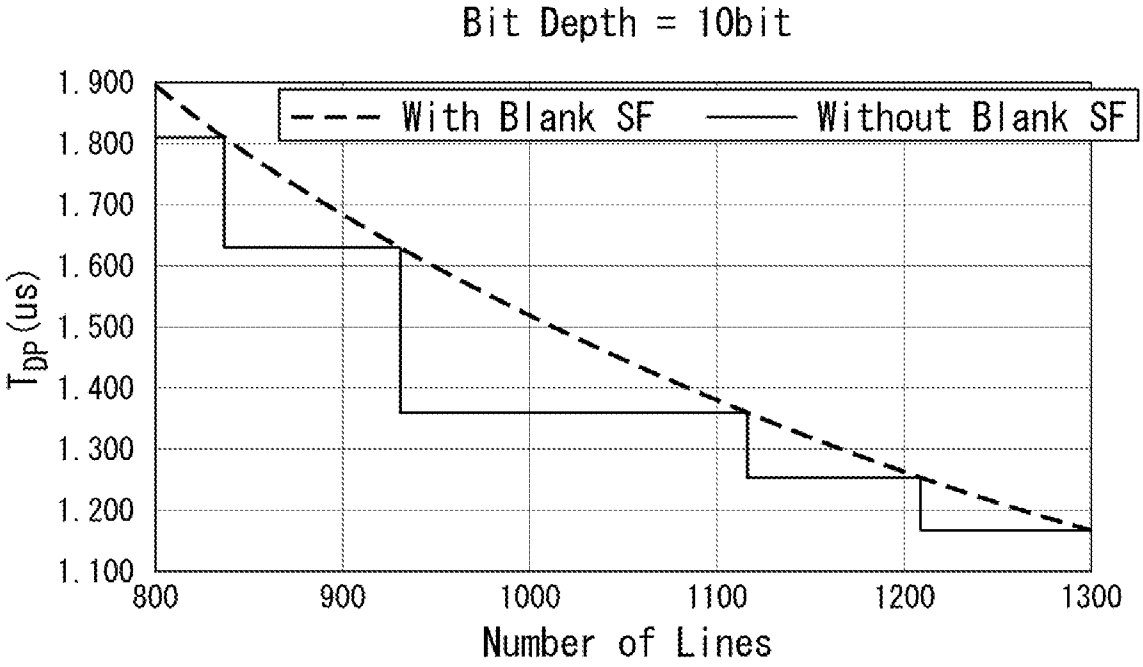
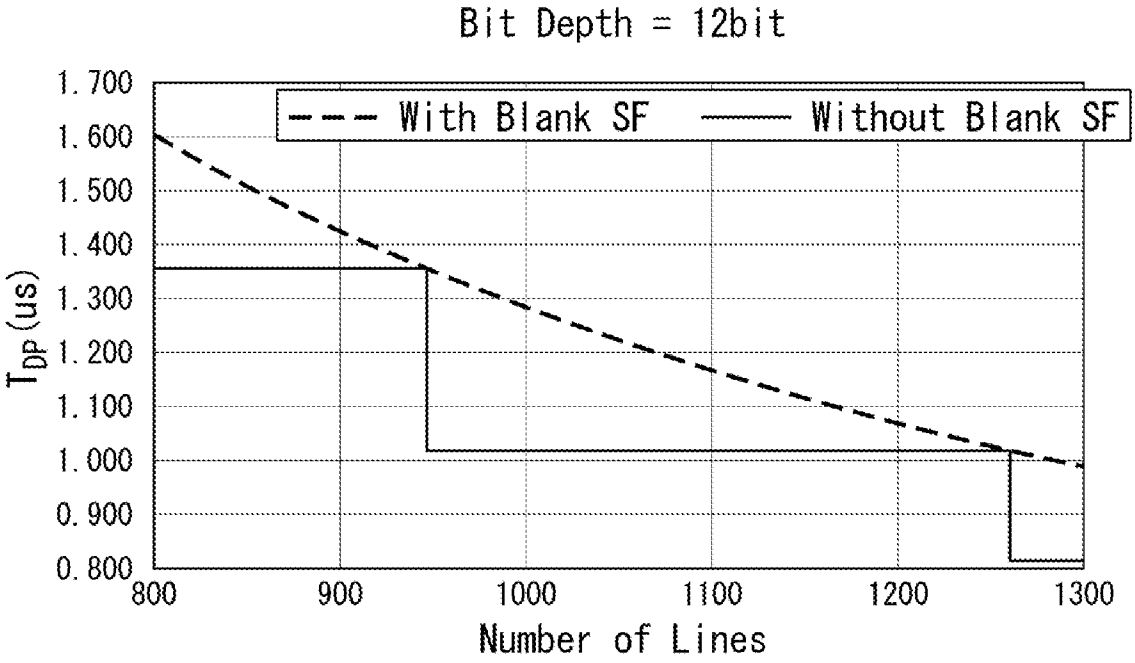

Bit Depth = 10bit
With Blank SF
Without Blank SF
1.900
1.800
1.700
1.600
1.500
1.400
1.300
1.200
1.100
T_{dp}(us)
800
900
1000
1100
1200
1300
Number of Lines

FIG. 13


Bit Depth = 12bit
With Blank SF
Without Blank SF
1.700
1.600
1.500
1.400
1.300
1.200
1.100
1.000
0.900
0.800
T_{DP}(us)
800
900
1000
1100
1200
1300
Number of Lines

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2020/107384

A. CLASSIFICATION OF SUBJECT MATTER

G09G 3/32(2016.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,CNKI,WPI,EPODOC: display, micro+, current?, PWM, sub+, frame?, field?, sub?frame?, sub?field?, "2", "n", "k", huawei

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 111179819 A (YUCHUANG SEMICONDUCTOR GUANGZHOU CO., LTD.) 19 May 2020 (2020-05-19) description, paragraphs [0042] to [0046], [0095] to [0140] and figures 3, 10 to 14	1, 3-9, 11-16
A	CN 111149148 A (HUAWEI TECH. CO., LTD.) 12 May 2020 (2020-05-12) the whole document	1-16
A	CN 107256691 A (SHENZHEN CHINA STAR OPTOELECTRONICS SEMICONDUCTOR DISPLAY TECH. CO., LTD.) 17 October 2017 (2017-10-17) the whole document	1-16
A	CN 102097070 A (LG DISPLAY CO., LTD.) 15 June 2011 (2011-06-15) the whole document	1-16
A	CN 102968966 A (SONY CORP.) 13 March 2013 (2013-03-13) the whole document	1-16
A	CN 110599948 A (SHENZHEN CHINA STAR OPTOELECTRONICS SEMICONDUCTOR DISPLAY TECH. CO., LTD.) 20 December 2019 (2019-12-20) the whole document	1-16
A	CN 101751866 A (NEC ELECTRONICS CORP.) 23 June 2010 (2010-06-23) the whole document	1-16

☑ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 April 2021	**06 May 2021**
Name and mailing address of the ISA/CN **National Intellectual Property Administration, PRC** **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088** **China** Facsimile No. **(86-10)62019451**	Authorized officer **LI,Peipei** Telephone No. **86-(10)-53962515**

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2020/107384

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2000089731 A (MATSUSHITA ELECTRIC IND. CO., LTD.) 31 March 2000 (2000-03-31) the whole document	1-16

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2020/107384

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	111179819	A	19 May 2020	None			
CN	111149148	A	12 May 2020	WO	2019075679	A1	25 April 2019
CN	107256691	A	17 October 2017	CN	107256691	B	27 September 2019
				US	10706781	B2	07 July 2020
				WO	2019029091	A1	14 February 2019
				US	2019051244	A1	14 February 2019
CN	102097070	A	15 June 2011	US	9514690	B2	06 December 2016
				TW	201120859	A	16 June 2011
				KR	101325314	B1	08 November 2013
				TW	I518661	B	21 January 2016
				US	2011141003	A1	16 June 2011
				CN	102097070	B	06 November 2013
				KR	20110066504	A	17 June 2011
				DE	102010042710	A1	16 June 2011
CN	102968966	A	13 March 2013	JP	5849538	B2	27 January 2016
				US	2013050304	A1	28 February 2013
				JP	2013050681	A	14 March 2013
				US	8963967	B2	24 February 2015
CN	110599948	A	20 December 2019	None			
CN	101751866	A	23 June 2010	JP	2010145488	A	01 July 2010
				JP	5307527	B2	02 October 2013
				US	8358264	B2	22 January 2013
				CN	101751866	B	25 June 2014
				US	2010164922	A1	01 July 2010
JP	2000089731	A	31 March 2000	None			