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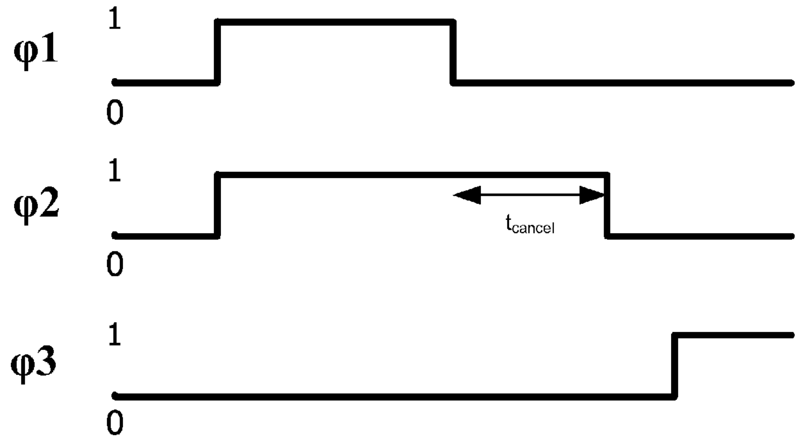

Figure 5

(57) Abstract: An architecture of an integrated circuit allows for the canceling of noise sampled on a capacitor in the integrated circuit, after an input signal has already been sampled. Thermal noise correlated with an arbitrary input signal may be canceled after selectively controlling a plurality of switching devices during a sequence of clock phases. An auxiliary capacitor may be used to store a voltage equal to the thermal noise and enable the cancellation of the thermal noise from the sampled signal in conjunction with a noise cancellation unit.

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NOISE CANCELLATION SYSTEM AND METHOD FOR AMPLIFIERS

FIELD OF THE INVENTION

[01] The present invention relates to a process for canceling noise sampled on a capacitor in an integrated circuit. The present invention further relates to a method for canceling thermal noise in high-accuracy and high-resolution integrated circuits. The present invention further relates to an architecture for an integrated circuit that cancels noise accompanying a sampled input signal, after the input signal has been sampled.

BACKGROUND INFORMATION

[02] The implementation of sampling processes on integrated circuits often requires the use of sampling networks or switched capacitor circuits. Switched capacitor circuits allow for discrete time signal processing by applying an input signal to a capacitor when a connected switch is closed. FIG. 1 illustrates a standard capacitive sampling circuit. When switch **20** is closed during the phase $\varphi 1$, the input signal is applied and a corresponding charge is stored on capacitor **10** that is proportional to the input signal, and this charge is held on capacitor **10** when switch **20** is opened.

[03] While basic switched capacitor circuits such as that illustrated in FIG. 1 are useful in implementing sampling processes, they have a number of drawbacks. Sampling an input signal in a switched capacitor circuit will not only sample the intended input signal, but any accompanying thermal noise. This noise is primarily produced by the switch, such as switch **20** in FIG. 1, in the switched capacitor circuits, and is particularly problematic when used in conjunction with small capacitors. When designing integrated circuits using switched capacitor circuits, consideration must be made for the presence of the sampled noise, especially in integrated circuits that require a high accuracy (such as high-accuracy sample and hold circuits) or high resolution (such as high-resolution data converters). Consideration, in particular, must be made to account for the power produced by the sampled noise. If switch **20** is represented by a simple resistive element having a resistance of R_{ON}, the thermal noise power of the sampled noise in a switched capacitor circuit can be expressed by Equation (i):

$$\text{noise\_power} = (4kTR_{ON}) * \left(\frac{1}{R_{ON}C} * \frac{1}{2\pi} * \frac{\pi}{2} \right) \quad \text{(i),}$$

where k = Boltzmann's constant, T = the absolute temperature in Kelvin, R_{ON} = the equivalent resistance of the switching device, and C = the capacitance of the sampling capacitor.

[04] Equation (i) may be further simplified into equation (ii):

$$\text{noise\_power} = \frac{kT}{C} \quad \text{(ii).}$$

[05] Previous techniques for designing integrated circuits have concentrated on reducing the magnitude of the noise sampled, such as in U.S. Patent No. 7,298,151 ("the 151 patent"). FIG. 2 illustrates a capacitive sampling circuit with a hold amplifier to reduce sampling noise, as described in the '151 patent. During phase φ1, switches **20** and **22** are closed, connecting capacitor **10** to the input at the bottom plate. When switch **20** is closed, the input signal is applied and stored on capacitor **10**. The closing of switch **22** allows for setting a DC potential voltage on the top plate of capacitor **10**, allowing for the setting of a charge at node S1, as illustrated in FIG. 2. The charge on capacitor **10** will therefore be proportional to the input voltage less the DC potential at S1. During φ2, switch **21** is closed, and the charge at S1 is frozen. Amplifier **30** is connected to capacitor **10** at node S1, and is used to buffer the sampled input voltage during the hold phase, φ2. During this hold phase, switch **23** is closed, creating a feedback loop for amplifier **30** through capacitor **12**. This arrangement, as described in the '151 patent, allows for the sampled noise to effectively have a power that is less than $\frac{kT}{C}$. While this process allows for the reduction of the noise in the integrated circuit, it does not provide for an actual cancellation of the noise in the circuit. Thus, sampled noise will continue to be present in the system and add to the power output of the integrated circuit.

[06] Other previous configurations have, instead of trying to reduce the noise sampled, attempted to reduce or cancel noise on a capacitor reset to a DC voltage in the designed integrated circuit or used correlated double sampling in imagers that relied on noise being present before a signal is sampled. None of these other previously implemented systems have allowed for an actual cancellation of the noise component from a sampled signal after a sample has already been taken.

[07] Thus there remains a need in the art for a system and a process that cancels the noise sampled on a sampling capacitor after an input signal has already been sampled.

BRIEF DESCRIPTION OF THE DRAWINGS

[08] Figure 1 is a diagram of a standard capacitive sampling circuit.

[09] Figure 2 is a diagram of a capacitive sampling circuit with a hold amplifier to reduce sampling noise.

[10] Figure 3 is a diagram of an integrated circuit with a noise cancellation unit to cancel out the thermal noise from the sampled input signal, according to the present invention.

[11] Figure 4 is a diagram of an integrated circuit with sample and hold amplifier functionality to cancel out the thermal noise from the sampled input signal, according to the present invention.

[12] Figure 5 is a timing diagram of the clock phases of the integrated circuit, according to the present invention.

[13] Figure 6 is a diagram of an integrated circuit with a controlled sample and hold amplifier gain to cancel out the thermal noise from the sampled input signal, according to the present invention.

DETAILED DESCRIPTION

[14] The subject invention will now be described in detail for specific preferred embodiments of the invention, it being understood that these embodiments are intended only as illustrative examples and the invention is not to be limited thereto.

[15] In switched capacitor circuits used to sample various input signals, cancellation of the accompanying noise component with an input signal may be done by sampling an arbitrary input signal containing the thermal noise and canceling the thermal noise after the sample is taken by selectively controlling a plurality of switching devices during a sequence of clock phases. Embodiments of the present invention may provide an input capacitor and a noise cancellation unit. A noise cancellation unit may include a buffer, an auxiliary capacitor, and additional switches. An auxiliary capacitor may be used to store a voltage equal to the thermal noise to enable cancellation of the thermal noise from the sampled signal. Embodiments of the present invention may also provide for a noise cancellation unit that includes a pair of amplifiers with a negative feedback loop that may control a gain of the circuit to cancel out the thermal noise in the sampled signal.

[16] FIG. 3 illustrates a diagram of an integrated circuit with a noise cancellation unit to cancel out the thermal noise from the sampled input signal of the present invention. Integrated circuit **100** may include an input capacitor, C_{in} **120**. The bottom plate of input capacitor **120** may be connected to an input for integrated circuit **100**, where an input voltage, VIN, may be applied. The top plate of input capacitor **120** may be connected to ground, or a constant voltage, through switching device **140** and to noise cancellation unit **130**. Switching device **140** may be connected to the top plate of capacitor **140** and the input to noise cancellation unit **130** at the input terminal of the switching device. The output terminal of switching device **140** may be connected to ground or a constant voltage. In alternative embodiments, switching device **140** may be connected to the top plate of capacitor **140** and noise cancellation unit **130** at the output terminal of the switching device, and to ground at the input terminal of the switching device. Switching device **140** may be closed during clock phase $\varphi 1$, which may correspond to a phase during the sampling mode.

[17] Noise cancellation unit **130** may be connected to input capacitor **120** at the input of noise cancellation unit **130**. The output of noise cancellation unit **130** may correspond to the output of the sampling segment of integrated circuit **100**. Noise cancellation unit **130** may also be connected to ground or a constant voltage through switching device **142**. Switching device **142** may be connected to noise cancellation unit **130** at the input terminal of the switching device, and to ground at the output terminal of the switching device, as illustrated in FIG. 3. In other embodiments, switching device **142** may be connected to noise cancellation unit **130** at the output terminal of the switching device, and to ground or a constant voltage at the input terminal of the switching device.

[18] During operation, an input signal, VIN, may be applied to the bottom plate of input capacitor **120**. Switching device **140** may be closed during clock phase $\varphi 1$, connecting the top plate of input capacitor **120** to ground. When switching device **140** is opened, a charge may be maintained on capacitor **120**, and VIN may be stored on capacitor **120**. The signal sampled on input capacitor **120** may also contain thermal noise that accompanied with VIN when the input voltage was sampled and stored on the capacitor. VIN and the sampled thermal noise may be output to noise cancellation unit **130**. During clock phase $\varphi 2$, switching device **142** may close, connecting noise cancellation unit **130** to ground. During this clock phase, noise cancellation unit **130** may cancel the sampled thermal noise. Noise cancellation unit **130** may output a signal that correlates to VIN, but does not contain any of the sampled thermal noise.

[19] FIG. 4 illustrates a diagram of an integrated circuit with sample and hold amplifier functionality to cancel out the thermal noise from the sampled input signal of the present invention. Integrated circuit **100** may include an input capacitor, C_{in} **120**. The bottom plate of input capacitor **120** may be selectively connected to an input for integrated circuit **100**, through switching device **144**. Switching device **144** may close during clock phase $\varphi 2$, and may be connected to the input of integrated circuit **100** at the input terminal of the switching device. Switching device **144** may be connected to the bottom plate of input capacitor **120** at the output terminal of the switching device.

[20] The bottom plate of input capacitor **120** may alternately be connected to ground or a constant voltage through switching device **146**. Switching device **146** may be selectively closed during clock phase $\varphi 3$. Switching device **146** may be connected to the bottom plate of input capacitor **120** at the input terminal of the switching device. Switching device **146** may also be connected at its input terminal to the output terminal of switching device **144**.

[21] The top plate of input capacitor **120** may be connected to ground or a constant voltage through switching device **140** and to buffer **150**. Switching device **140** may be connected to the top plate of input capacitor **120** and the input terminal of buffer **150** at the input terminal of the switching device. The output terminal of switching device **140** may be connected to ground or a constant voltage. In alternative embodiments, switching device **140** may be connected to the top plate of input capacitor **120** and buffer **150** at the output terminal of the switching device, and to ground at the input terminal of the switching device. Switching device **140** may be closed during clock phase $\varphi 1$, which may correspond to a phase during the sampling mode.

[22] Integrated circuit **100** may also include an auxiliary capacitor, C_{aux} **122**. Buffer **150**, auxiliary capacitor **122**, and switching device **142** may make up noise cancellation unit **130**. The output terminal of buffer **150** may be connected to the bottom plate of auxiliary capacitor **122**. The voltage at the top plate of auxiliary capacitor **122** may correspond to the output of the sampling segment of integrated circuit **100**. The top plate of auxiliary capacitor **122** may also be connected to ground through switching device **142**. Switching device **142** may be connected to the top plate of auxiliary capacitor **122** at the input terminal of the switching device, and to ground or a constant voltage at the output terminal of the switching device, as illustrated in FIG. 4. In other embodiments, switching device **142** may be connected to auxiliary capacitor **122** at the output terminal of the switching device, and to ground at the input terminal of the switching device.

[23] During operation, integrated circuit **100** may operate in accordance to designated clock phases $\varphi1$, $\varphi2$, and $\varphi3$. FIG. 5 illustrates the timing of the various clock phases. Switching device **140** may close first during clock phase $\varphi1$, connecting the top plate of input capacitor **120** to ground. During clock phase $\varphi2$, switching device **144** may be closed, connecting the input of integrated circuit **100** to input capacitor **120**. An input signal, VIN, may be applied to the bottom plate of input capacitor **120** and the input signal may be sampled for the rest of clock phase $\varphi1$. Switching device **142** may also be closed during clock phase $\varphi2$, connecting the top plate of auxiliary capacitor **122** to ground.

[24] When switching device **140** is opened after $\varphi1$, a charge may be maintained on capacitor **120**, and VIN may be stored on capacitor **120**. The top plate of input capacitor **120** may be at a voltage different from ground due to the presence of the thermal noise that was simultaneously sampled when VIN was stored on input capacitor **120**. The voltage at the top plate of input capacitor **120** corresponding to the thermal noise may be output to buffer **150**, which may buffer the voltage onto the bottom plate of auxiliary capacitor **122**. The top plate of auxiliary capacitor **122** may remain at ground for the duration of clock phase $\varphi2$ as switching device **142** remains closed. The voltage sampled on auxiliary capacitor **122** may be equal to the thermal noise sampled on input capacitor **120**, representing the voltage potential at the top plate of input capacitor **120**, and additional noise added from switching device **142**. The additional noise added from switching device **142** may be negated by choosing a larger capacitance for auxiliary capacitor **122**. A selection of a large capacitance for auxiliary capacitor **122** may effectively reduce thermal noise produced by switching device **142**. Selecting a large capacitance for auxiliary capacitor **122** may not add an additional load to the input to integrated circuit **100** because auxiliary circuit **122** is not driven by VIN.

[25] As illustrated by FIG. 5, clock phases φ1 and φ2 may overlap. Clock phase φ1 may end before clock phase φ2 ends. The period during which clock phase φ2 extends beyond clock phase φ1 may represent, t_{cancel}, the time period after which switching device **140** is opened and the sampled thermal noise from the top plate of input capacitor **120** is buffered onto auxiliary capacitor **122**.

[26] During clock phase φ3, switching device **146** may close. The closure of switching device **146** may short the bottom plate of input capacitor **120** to ground. Shorting input capacitor **120** to ground may change the potential voltage at the top plate of auxiliary capacitor **122** to -VIN. Integrated circuit **100** may then produce VIN at the output of the sampling stage of the circuit, without the presence of any sampled thermal noise.

[27] FIG. 6 illustrates a diagram of an integrated circuit with a controlled sample and hold amplifier gain to cancel out the thermal noise from the sampled input signal of the present invention. Integrated circuit **100** may include an input capacitor, C_{in} **120**. The bottom plate of input capacitor **120** may be selectively connected to an input for integrated circuit **100**, through switching device **144**. Switching device **144** may close during clock phase φ2, and may be connected to the input of integrated circuit **100** at the input terminal of the switching device. Switching device **144** may be connected to the bottom plate of input capacitor **120** at the output terminal of the switching device.

[28] The bottom plate of input capacitor **120** may alternately be connected to ground or a constant voltage through switching device **146**. Switching device **146** may be selectively closed during clock phase φ3. Switching device **146** may be connected to the bottom plate of input capacitor **120** at the input terminal of the switching device. Switching device **146** may also be connected at its input terminal to the output terminal of switching device **144**.

[29] The top plate of input capacitor **120** may be connected to ground or a constant voltage through switching device **140** and to the inverting input of amplifier **160**. Switching device **140** may be connected to the top plate of input capacitor **120** and the inverting input terminal of amplifier **160** at the input terminal of the switching device. The output terminal of switching device **140** may be connected to ground or a constant voltage. In alternative embodiments, switching device **140** may be connected to the top plate of input capacitor **120** and the inverting input of amplifier **160** at the output terminal of the switching device, and to ground at the input terminal of the switching device. Switching device **140** may be closed during clock phase $\varphi1$, which may correspond to a phase during sampling.

[30] Integrated circuit **100** may also include a pair of amplifiers, **160** and **162**. Amplifiers **160** and **162** may each have a open-loop gain that may amplify the input to the respective amplifier, although the overall closed-loop gain of integrated circuit **100** may be controlled by the connected feedback loop, as illustrated in FIG. 6. The inverting input of amplifier **160** may be connected to the top plate of input capacitor **120** and selectively to ground or a constant voltage through switching device **140**. The non-inverting input terminal of amplifier **160** may be connected to ground. Amplifier **160** may be connected to the bottom plate of auxiliary capacitor, C_{aux} **122**.

[31] The top plate of auxiliary capacitor **122** may be connected to ground through switching device **142** and to the inverting input terminal of amplifier **162**. Switching device **142** may be connected to the top plate of auxiliary capacitor **122** and to the inverting input of amplifier **162** at the input terminal of the switching device, and to ground or a constant voltage at the output terminal of the switching device, as illustrated in FIG. 6. In other embodiments, switching device **142** may be connected to auxiliary capacitor **122** and the inverting input of amplifier

162 at the output terminal of the switching device, and to ground at the input terminal of the switching device.

[32] The non-inverting input terminal of amplifier **162** may be connected to ground or a constant voltage. The output of amplifier **162** may also correspond to the output of the sampling segment of integrated circuit **100**. Amplifier **162** may increase the sample and hold amplifier gain and isolate auxiliary capacitor **124** from the output. A feedback loop may also be connected between the output of amplifier **162** and the inverting input of amplifier **160**. Switching device **148** may connect the output of amplifier **162** to feedback capacitor, C_{fb} **124**, in the feedback loop. Switching device **148** may be closed during clock phase φ3.

[33] The bottom plate of feedback capacitor **124** may be connected to the output of amplifier **162** when switching device **148** is closed. The top plate of the feedback capacitor **124** may be connected to the inverting input terminal of amplifier **160** and to the top plate of input capacitor **120**; therefore the potential voltage at the top plates for the feedback capacitor **124** and the input capacitor **120** may be the same. The top plate of feedback capacitor **124** may also be connected to ground through switching device **140**. Feedback may only be provided through the feedback loop during clock phase φ3, when switching device **148** is closed. The presence of the feedback loop may allow for controlling the sample and hold amplifier gain of integrated circuit **100**.

[34] During operation, integrated circuit **100** may operate in accordance to designated clock phases φ1, φ2, and φ3. Switching device **140** may close first during clock phase φ1, connecting the top plate of input capacitor **120** to ground. During clock phase φ2, switching device **144** may be closed, connecting the input of integrated circuit **100** to input capacitor **120**. An input signal, VIN, may be applied to the bottom plate of input capacitor **120** and the input signal may be sampled for the rest of clock phase φ1. Switching device **142** may also be closed during clock phase φ2, connecting the top plate of auxiliary capacitor **122** to ground.

[35] When switching device **140** is opened after φ1, a charge may be maintained on capacitor **120**, and VIN may be stored on capacitor **120**. The top plate of input capacitor **120** may be at a voltage different from ground due to the presence of the thermal noise that was simultaneously sampled when VIN was stored on input capacitor **120**. The voltage at the top plate of input capacitor **120** corresponding to the sampled thermal noise may be output to amplifier **160**, which may amplify this signal onto the bottom plate of auxiliary capacitor **122**. Amplifier **160** may also reduce the impact of additional noise added from switching device **142**, therefore providing that the input-referred voltage sampled on auxiliary capacitor **122** may correlate to the thermal noise sampled on input capacitor **120**, with minimal additional thermal noise from switching device **142**. The top plate of auxiliary capacitor **122** may remain at ground for the duration of clock phase φ2 as switching device **142** remains closed. During clock phase φ2, the applied inputs to both of the input terminals of amplifier **162** may be ground, and amplifier **162** may not output a voltage at its output.

[36] During clock phase φ3, switching device **146** may close. The closure of switching device **146** may short the bottom plate of input capacitor **120** to ground. Due to the high gain of amplifier **162**, along with the negative feedback configuration, shorting input capacitor **120** to ground may cause the charge on input capacitor **120** to transfer to feedback capacitor **124**, such that the output of amplifier **162** is equal –VIN * CIN / CFB. In addition, because auxiliary capacitor **122** has stored charge that corresponds to the noise voltage sampled on input capacitor **120**, none of the noise charge on input capacitor **120** will transfer to feedback capacitor **124**. In this way, integrated circuit **100** may then produce –(-VIN * CIN / CFB) at the output of the sampling stage of the circuit, without the presence of any sampled thermal noise.

[37] Several embodiments of the invention are specifically illustrated and/or described herein. However, it will be appreciated that modifications and variations of the invention are covered by the above teachings and within the purview of the appended claims without departing from the spirit and intended scope of the invention.

WHAT IS CLAIMED IS:

1. An integrated circuit for canceling noise sampled during a sampling phase, the integrated circuit comprising:

an input connected to an input voltage to be sampled;

a capacitor storing a sample of the input voltage during the sampling phase, wherein the noise is also sampled on the capacitor; and

an arrangement for noise cancelation, wherein the arrangement monitors the noise and cancels the noise during a hold phase.

2. An integrated circuit for canceling noise sampled during a sampling phase, the integrated circuit comprising:

an input connected to an input voltage to be sampled;

a first capacitor storing a first sample of the input voltage during the sampling phase, wherein the noise is also sampled on the first capacitor; and

a second capacitor storing a second sample, the second sample containing information about the noise of the first sample.

3. The integrated circuit according to claim 2, wherein the information in the second sample stored on the second capacitor is used to cancel the noise of the first sample.

4. The integrated circuit according to claim 2, further comprising:

a buffer to separate the first and the second capacitor.

5. The integrated circuit according to claim 2, further comprising:

an amplifier to separate the first and the second capacitor.

6. The integrated circuit according to claim 5, wherein the amplifier amplifies the sampled input voltage.

7. The integrated circuit according to claim 5, wherein the amplifier cancels the noise of the first sample.

8. The integrated circuit according to claim 5, further comprising:

an additional amplifier isolating the second capacitor from the output of the integrated circuit.

9. The integrated circuit according to claim 8, wherein the additional amplifier increases an overall gain of the integrated circuit.

10. The integrated circuit according to claim 8, further comprising:

a feedback loop connecting the output of the additional amplifier and the input of the amplifier.

11. The integrated circuit according to claim 10, wherein the feedback loop controls an overall gain of the integrated circuit.

12. The integrated circuit according to claim 10, wherein the feedback loop includes a third capacitor.

13. A method for canceling noise sampled during a sampling phase in an integrated circuit, the method comprising:

sampling an input voltage on a capacitor, the sampled input voltage including the noise;

monitoring the noise of the sampled input voltage by a first arrangement; and

canceling the noise during a hold phase by the first arrangement.

14. A method for canceling noise sampled during sampling in an integrated circuit, the method comprising:

during a first phase, sampling an input voltage on a first capacitor, the sampled input voltage including the noise;

during a second phase, outputting a voltage corresponding to the noise through a buffer to a second capacitor; and

during a third phase, transferring charge off of the first capacitor, wherein a charge corresponding to the sampled input voltage is transferred to a third capacitor, but a charge corresponding to a first phase sample is not transferred.

15. The method according to claim 14, further comprising:

connecting the second capacitor to a constant voltage during the first phase.

16. A method for canceling a noise component sampled during sampling in an integrated circuit, the method comprising:

during a first phase, sampling an input voltage on a first capacitor, the sampled input voltage including the noise;

during a second phase, amplifying a voltage corresponding to the noise through a first amplifier to a second capacitor;

during a third phase, performing the steps of:

(i) transferring a signal charge off of the first capacitor;

(ii) outputting a voltage potential at the top plate of the second capacitor through a second amplifier as an output of the integrated circuit; and

(iii) generating a feedback loop to control a gain of the integrated circuit, wherein a voltage potential at the output of the integrated circuit correlates to the sampled input voltage without the noise, multiplied by a gain factor.

17. The method according to claim 16, further comprising:

connecting the second capacitor to the constant voltage during the first phase.

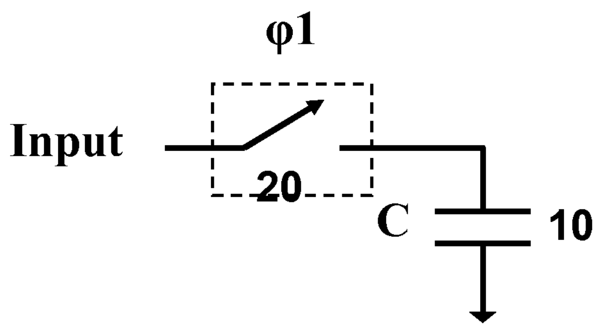

Figure 1

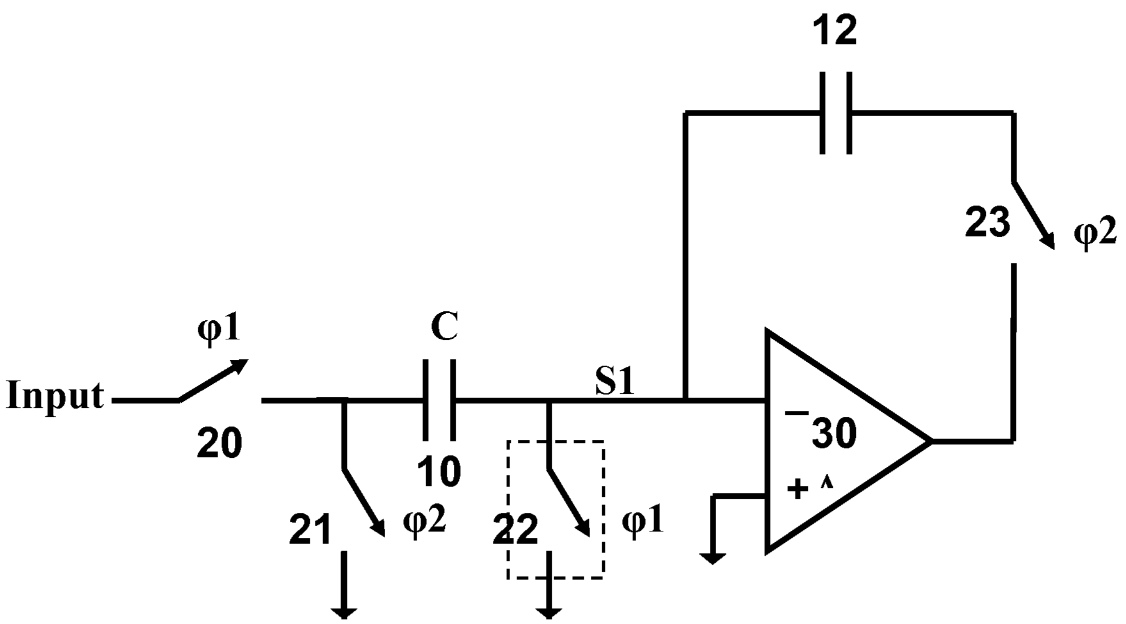

Figure 2

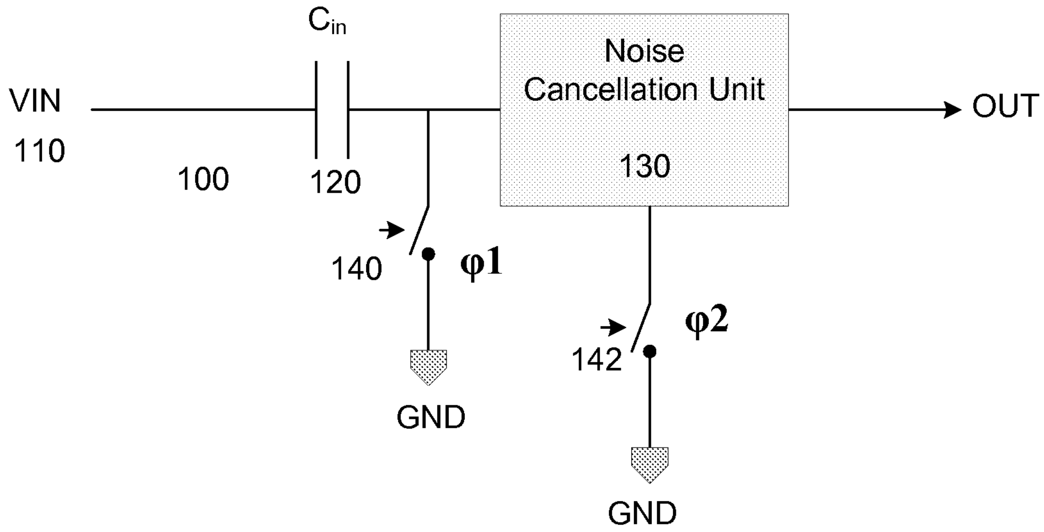

Figure 3

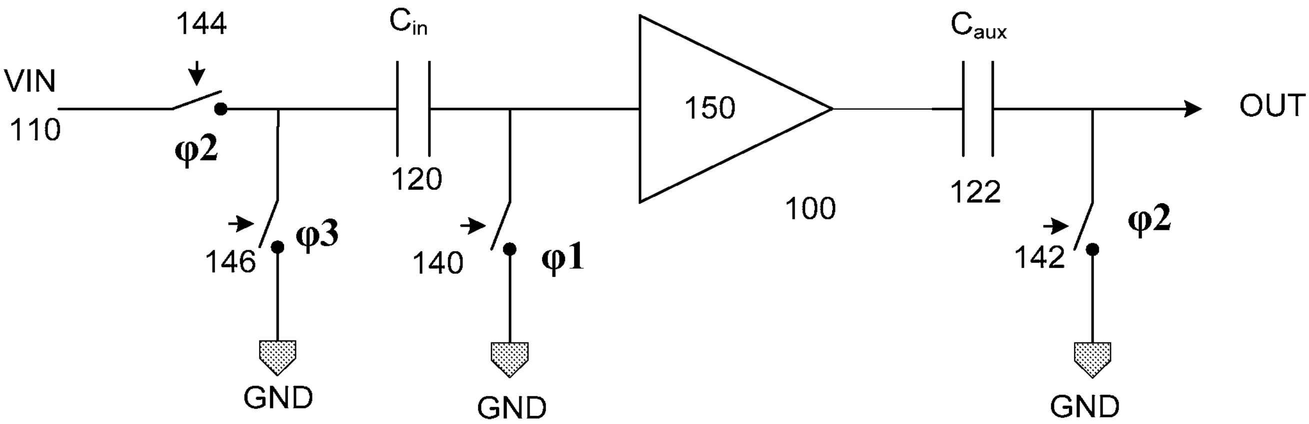

Figure 4

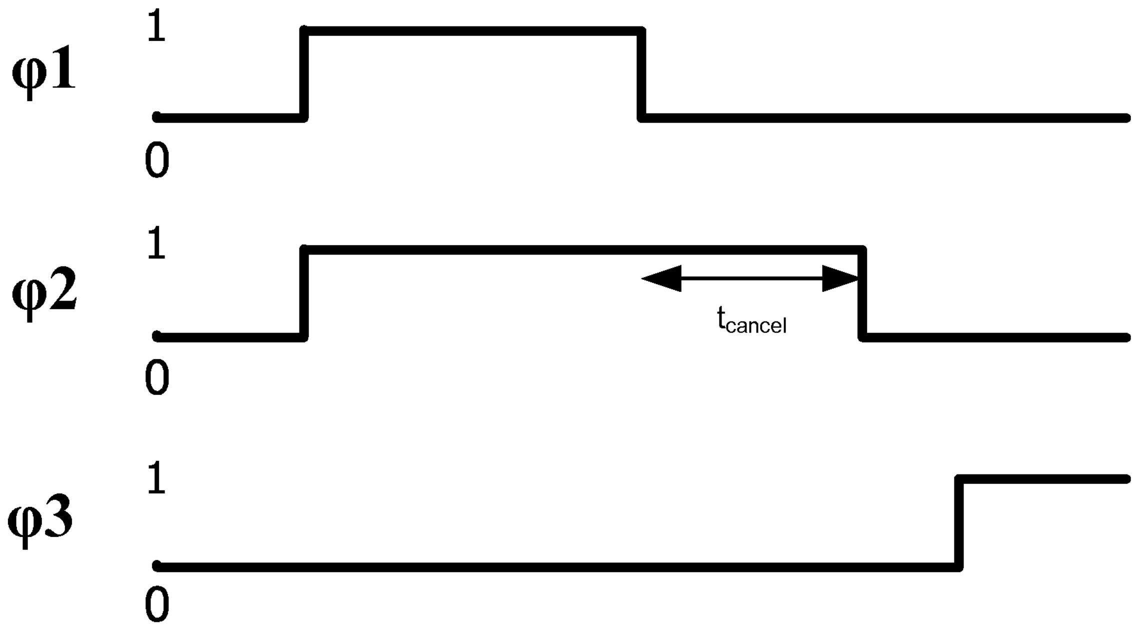

Figure 5

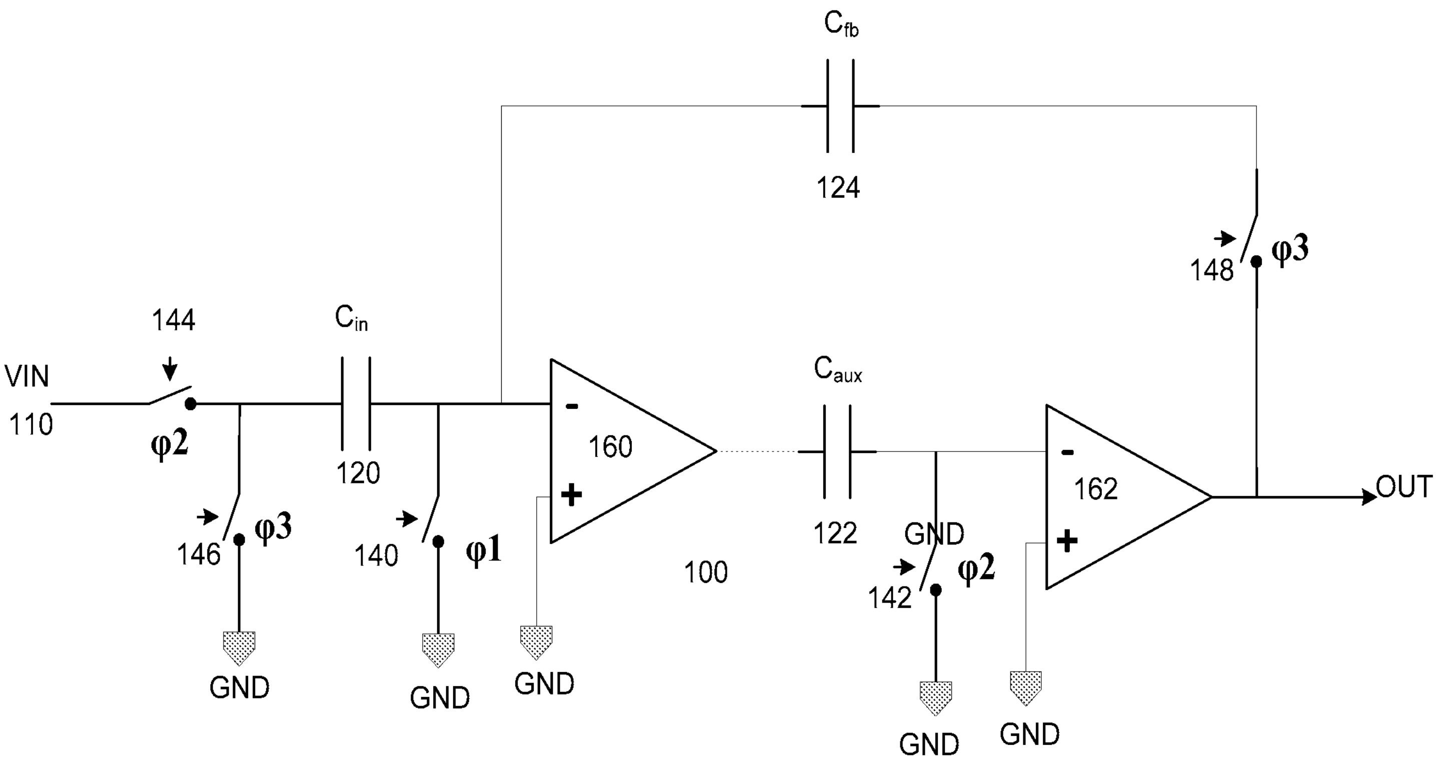

Figure 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US12/30074

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G11C 7/02 (2012.01)
USPC - 365/206, 63, 51

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8): G11C 7/02 (2012.01)
USPC: 365/206, 63, 51

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

MicroPatent (US-G, US-A, EP-A, EP-B, WO, JP-bib, DE-C,B, DE-A, DE-T, DE-U, GB-A, FR-A); DialogPro; IEEE; Google
noise, cancellation, suppression, sample, hold, switch, capacitor, thermal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 7,298,151 B2 (KAPUSTA, JR et al.) November 20, 2007, figure 3, figure 11, column 8, lines 35-37 & 39-41, column 9, lines 1-2	2, 4-6 and 8-11 --- 3, 7, 12 and 14-17
X --- Y	US 5,215,081 A (OSTROFF, et al.) June 1, 1993, figure 2, column 6, lines 20-27, 49-58, & 60-62	1 and 13 --- 7 and 14-17
Y	US 2006/0071709 A1 (MALOBERTI, et al.) April 6, 2006, figure 3, paragraph [0042]	3 and 12
Y	US 6,429,697 B1 (AMAZEEN, et al.) August 6, 2002, figure 1	16 and 17

☐ Further documents are listed in the continuation of Box C. ☐

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Date of the actual completion of the international search	Date of mailing of the international search report
25 May 2012 (25.05.2012)	29 JUN 2012

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