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(54) **Title**: RESISTIVE RANDOM ACCESS MEMORY CONTAINING A STEERING ELEMENT AND A TUNNELING DIELECTRIC ELEMENT

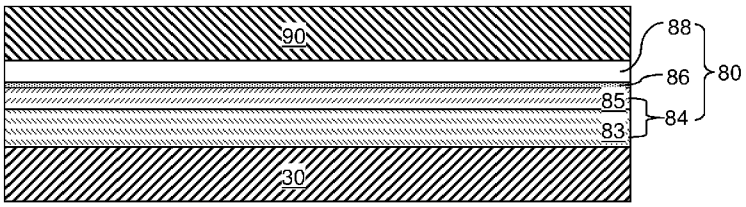


FIG. 6A

(57) **Abstract**: A memory device includes at least one memory cell. The at least one memory cell includes a steering element, a resistive memory element, and a tunneling dielectric element located between the steering element and the resistive memory element.

WO 2017/074548 A1

RESISTIVE RANDOM ACCESS MEMORY CONTAINING A STEERING ELEMENT AND A TUNNELING DIELECTRIC ELEMENT

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of priority to U.S. Patent Application No.: 14/924,144, filed October 27, 2015, the content of which is incorporated herein by reference in their entirety.

FIELD

[0002] The present disclosure relates generally to the field of semiconductor devices and specifically to three-dimensional non-volatile memory devices, such as a three-dimensional resistive random access memory (ReRAM) devices and other three-dimensional devices, and methods of making the same.

BACKGROUND

[0003] Resistance Random Access Memory, or "ReRAM," is a non-volatile memory device employing reversible change in resistance in a thin film with application of electrical voltage bias across the film. Application of the electrical voltage bias in one manner can cause decrease in the resistance of the thin film, for example, by formation of filaments that function as leakage current paths or by increasing a crystallinity of the thin film. Application of a different type of electrical voltage bias can cause reversal of the resistance of the thin film to an original high-resistance state, such as by removal of the filaments from the thin film or by decreasing the crystallinity of the thin film.

[0004] Thus, data can be stored in a ReRAM cell by changing the resistance of the thin film, which can be a solid-state material. The thin film is referred to as a memory film or a read/write film. Examples of ReRAM devices are described in World Intellectual Property Organization (WIPO) Publication No. WO2007004843 A1 to Hong et al. and U.S. Patent

Application Publication No. 2013/0043455 A1 to Bateman.

SUMMARY

[0005] One embodiment provides a memory device which includes at least one memory cell. The at least one memory cell includes a steering element, a resistive memory element, and a tunneling dielectric element located between the steering element and the resistive memory element.

[0006] Another embodiment provides a method of fabricating a memory device, comprising forming an alternating stack of insulating layers and sacrificial material layers that alternate along a first direction over a substrate, patterning the alternating stack to form sidewalls that extend along the first direction, forming an electrically conductive line extending along the first direction over the sidewalls of the alternating stack, forming recesses by removing the sacrificial material layers selective to the insulating layers, forming memory cells arranged along the first direction, and forming electrically conductive layers within each recess. Each of the memory comprises a resistive memory element, and at least one element of each memory cell is formed within a respective recess.

[0007] Another embodiment provides a method of fabricating a memory device, comprising forming an alternating stack of insulating layers and conductive material layers that alternate along a first direction over a substrate, patterning the alternating stack to provide sidewalls of the alternating stack, forming a layer stack including a continuous doped semiconductor layer, a tunneling dielectric layer, and a resistive memory material layer over the sidewalls of the alternating stack, and forming an electrically conductive line on the layer stack.

[0008] Another embodiment provides a method of making a memory device, comprising determining a desired current-voltage performance characteristic of the device, selecting at least one of a thickness and p-type doping concentration of a p-type semiconductor layer of a

diode steering element which provides the desired current-voltage performance characteristic, forming the diode steering element which comprises an n-type semiconductor layer and a p-type semiconductor layer having the selected at least one of thickness and doping concentration, forming a resistive memory element, and forming a tunneling dielectric element located between the diode steering element and the resistive memory element.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. 1A is a vertical cross-sectional view of an exemplary structure after formation of bit line access transistors and dielectric fill layers according to an embodiment of the present disclosure.

[0010] FIG. 1B is a see-through top-down view of the exemplary structure of FIG. 1A. The vertical plane A – A' is the plane of the cross-section for FIG. 1A.

[0011] FIG. 2A is a vertical cross-sectional view of the exemplary structure after formation of alternating stacks of insulating layers and conductive material layers according to an embodiment of the present disclosure.

[0012] FIG. 2B is a top-down view of the exemplary structure of FIG. 2A. The vertical plane A – A' is the plane of the cross-section for FIG. 2A.

[0013] FIG. 3 is a vertical cross-sectional view of the exemplary structure after deposition of a layer stack including memory elements according to an embodiment of the present disclosure.

[0014] FIG. 4A is a vertical cross-sectional view of the exemplary structure after removal of horizontal portions of the layer stack according to an embodiment of the present disclosure.

[0015] FIG. 4B is a top-down view of the exemplary structure of FIG. 4A. The vertical plane A – A' is the plane of the cross-section for FIG. 4A.

[0016] FIG. 5A is a vertical cross-sectional view of the exemplary structure after

formation of electrically conductive lines and dielectric pillars according to an embodiment of the present disclosure.

[0017] FIG. 5B is a top-down view of the exemplary structure of FIG. 5A. The vertical plane A – A' is the plane of the cross-section for FIG. 5A. The vertical plane C – C' is the plane of the cross-section for FIG. 5C.

[0018] FIG. 5C is another vertical cross-sectional view of the exemplary structure of FIGS. 5A and 5B.

[0019] FIG. 6A is a cross-sectional view of a portion of a first exemplary layer stack including memory elements of the present disclosure according to an embodiment of the present disclosure.

[0020] FIG. 6B is a cross-sectional view of a portion of a second exemplary layer stack including memory elements of the present disclosure according to an embodiment of the present disclosure.

[0021] FIG. 6C is a cross-sectional view of a portion of a third exemplary layer stack including memory elements of the present disclosure according to an embodiment of the present disclosure.

[0022] FIG. 6D is a cross-sectional view of a portion of a fourth exemplary layer stack including memory elements of the present disclosure according to an embodiment of the present disclosure.

[0023] FIG. 6E is a cross-sectional view of a portion of a fifth exemplary layer stack including memory elements of the present disclosure according to an embodiment of the present disclosure.

[0024] FIG. 7A is a graph illustrating current-voltage characteristics of a diode-tunneling dielectric-metal structure of the present disclosure and of a comparative diode-metal structure. FIG. 7B is a graph illustrating a variation in current-voltage characteristics of a

diode-tunneling dielectric-metal structure of the present disclosure as a function of the p-type semiconductor layer doping and thickness.

[0025] FIG. 8A is a schematic band diagram (i.e., plot of energy in eV versus position in the device in microns) of a layer stack of the present disclosure in a forward bias mode according to an embodiment of the present disclosure. FIG. 8B is a schematic band diagram of the layer stack of FIG. 8A in a reverse bias mode according to an embodiment of the present disclosure.

[0026] FIG. 8C is a comparative of schematic band diagrams in a reverse bias mode of the layer stack of FIG. 8A and of a comparative example which lacks the tunneling dielectric element.

[0027] FIGS. 9A-9D illustrate sequential vertical cross-sectional views of a method of making a first exemplary three-dimensional memory device employing an embodiment of the layer stack of the present disclosure.

[0028] FIGS. 10A-10D illustrate sequential vertical cross-sectional views of a method of making a second exemplary three-dimensional memory device employing an embodiment of the layer stack of the present disclosure.

[0029] FIGS. 11A-11D illustrate sequential vertical cross-sectional views of a method of making a third exemplary three-dimensional memory device employing an embodiment of the layer stack of the present disclosure.

[0030] FIGS. 12A-12C illustrate sequential vertical cross-sectional views of a method of making a fourth exemplary three-dimensional memory device employing an embodiment of the layer stack of the present disclosure.

[0031] FIGS. 13A-13C illustrates sequential vertical cross-sectional views of a method of making a fifth exemplary three-dimensional memory device employing an embodiment of the layer stack of the present disclosure.

DETAILED DESCRIPTION

[0032] As discussed above, the present disclosure is directed to a three-dimensional resistive random access memory (ReRAM) devices and other three-dimensional devices, and methods of making the same, the various aspects of which are described below. The embodiments of the disclosure can be employed to form various semiconductor devices such as three-dimensional monolithic memory array devices comprising ReRAM devices. The drawings are not drawn to scale. Multiple instances of an element may be duplicated where a single instance of the element is illustrated, unless absence of duplication of elements is expressly described or clearly indicated otherwise. Ordinals such as "first," "second," and "third" are employed merely to identify similar elements, and different ordinals may be employed across the specification and the claims of the instant disclosure.

[0033] As used herein, a "layer" refers to a material portion including a region having a substantially uniform thickness. A layer may extend over the entirety of an underlying or overlying structure, or may have an extent less than the extent of an underlying or overlying structure. Further, a layer may be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer may be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer may extend horizontally, vertically, and/or along a tapered surface. A substrate may be a layer, may include one or more layers therein, and/or may have one or more layer thereupon, thereabove, and/or therebelow.

[0034] As used herein, a "layer stack" refers to a stack of layers. As used herein, a "line" or a "line structure" refers to a layer that has a predominant direction of extension, i.e., having a direction along which the layer extends the most.

[0035] As used herein, a "field effect transistor" refers to any semiconductor device

having a semiconductor channel through which electrical current flows with a current density modulated by an external electrical field. As used herein, an "active region" refers to a source region of a field effect transistor or a drain region of a field effect transistor. A "top active region" refers to an active region of a field effect transistor that is located above another active region of the field effect transistor. A "bottom active region" refers to an active region of a field effect transistor that is located below another active region of the field effect transistor.

[0036] A monolithic three dimensional memory array is one in which multiple memory levels are formed above a single substrate, such as a semiconductor wafer, with no intervening substrates. The term "monolithic" means that layers of each level of the array are directly deposited on the layers of each underlying level of the array. In contrast, two-dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device. For example, non-monolithic stacked memories have been constructed by forming memory levels on separate substrates and vertically stacking the memory levels, as described in U.S. Patent No. 5,915,167 titled "Three Dimensional Structure Memory." The substrates may be thinned or removed from the memory levels before bonding, but as the memory levels are initially formed over separate substrates, such memories are not true monolithic three dimensional memory arrays.

[0037] The various three dimensional memory devices of the present disclosure can include a ReRAM device, and can be fabricated employing the various embodiments described herein. It is understood that a criss-cross array of memory elements that can be accessed by any access scheme can be employed for the resistive memory devices of the present disclosure, and the exemplary structures of the present disclosure are described herein merely provide non-limiting examples of implementation of the memory devices of the present disclosure.

[0038] Referring to FIGS. 1A and 1B, an exemplary structure is illustrated, which can be an in-process ReRAM device. As used herein, a "prototype" structure or an "in-process" structure refers to a transient structure that is subsequently modified in the shape or composition of at least one component therein.

[0039] The exemplary structure includes a substrate 6, which includes an insulating layer at an upper portion thereof. In one embodiment, the substrate 6 can be a stack of at least two material layers such as a stack of an underlying substrate material layer and an overlying substrate insulating layer. The substrate material layer can be a semiconductor material layer, a conductive material layer, or an insulating material layer that can provide structural support to the overlying structures, and may have a thickness greater than 50 microns, and typically in a range between 300 microns and 3 mm. In one embodiment, the substrate material layer can be a semiconductor wafer, such as a silicon wafer as known in the art. The substrate insulating layer can include an insulating material, and can have a thickness in a range from 100 nm to 3 microns, although lesser and greater thicknesses can also be employed.

[0040] In case the substrate material layer includes a semiconductor material, peripheral semiconductor devices for operation of a memory array device can be formed in, or on, the substrate material layer. For example, sense amplifiers, input-output (I/O) circuitry, control circuitry, and any other necessary peripheral circuitry can be formed on, or in, the substrate material layer. Additional devices that can be formed in, or on, the substrate material layer include, but are not limited to, global bit line select transistors for selecting global bit lines to be activated, local bit line select transistors for selecting local bit lines to be activated, and word line select transistor for selecting word lines to be activated.

[0041] As used herein, a "semiconductor material" refers to a material having electrical conductivity in the range from 1.0×10^{-6} S/cm to 1.0×10^{5} S/cm, and is capable of producing a doped material having electrical conductivity in a range from 1.0 S/cm to 1.0×10^{5} S/cm

upon suitable doping with an electrical dopant. As used herein, an "electrical dopant" refers to a p-type dopant that adds a hole to a valence band within a band structure, or an n-type dopant that adds an electron to a conduction band within a band structure. As used herein, a "conductive material" refers to a material having electrical conductivity greater than 1.0×10^5 S/cm. As used herein, an "insulating material" or a "dielectric material" refers to a material having electrical conductivity less than 1.0×10^{-6} S/cm. A "semiconducting material" refers to a material having electrical conductivity in a range from 1.0×10^{-6} S/cm to 1.0×10^5 S/cm. All measurements for electrical conductivities are made at the standard condition.

[0042] Global bit lines 10 are formed over the substrate 6. The global bit lines 10 are parallel electrically conductive lines that are laterally spaced apart in a first horizontal direction hd1, and extending in a second horizontal direction hd2. The global bit lines 10 can be formed, for example, by depositing at least one conductive material layer, and patterning the at least one conductive material layer employing a combination of lithographic methods and an anisotropic etch. The at least one conductive material layer can include, for example, at least one elemental metal (such as W, Co, Cu, and Al), a conductive doped semiconductor material, an intermetallic alloy including at least two elemental metals, a conductive metallic nitride, or a conductive metallic carbide. For example, the at least one conductive material layer can include a metallic barrier layer (such as a layer of TiN, TaN, or WN) and a metal layer (such as a layer of W, Ti, Ta, Cu, Al, or an alloy thereof). The space between the global bit lines 10 can be filled with a dielectric material (such as silicon oxide). The dielectric material can be subsequently planarized to remove excess portions from above a horizontal plane including the top surfaces of the global bit lines 10 to form separator dielectric material portions (not shown). A one-dimensional array of the global bit lines 10 and the separator dielectric material portions can extend along the second horizontal direction hd2. Alternatively, the one-dimensional array of the global bit lines 10 and the separator dielectric

material portions may be formed by depositing a dielectric material layer, forming trenches extending along the second horizontal direction hd2 and laterally spaced from one another along the first horizontal direction hd1, and filling the trenches with at least one conductive material to form the global bit lines 10 therein.

[0043] A two-dimensional array of select devices can be formed on the global bit lines 10 such that multiple select devices are formed on each global bit line 10. In one embodiment, the select devices can be transistor such as vertical thin film transistors employing a polycrystalline semiconductor channel. Examples of suitable transistors for the select devices are described, for example, in U.S. Patent Application No. 14/206,196, filed March 12, 2014, which is incorporated by reference herein in its entirety. In case the select devices are field effect transistors, the select transistors are herein referred to access transistors.

[0044] The access transistors are subsequently formed on global bit line 10. Each access transistor can be a vertical field effect transistor, and can include a bottom active region 14B (which can be a source region or a drain region), a semiconductor channel 14C, and a top active region 14T (which can be a drain region if the underlying bottom active region 14B is a source region, and a source region if the underlying bottom active region 14C is a drain region). As used herein, an "active region" refers to a source region or a drain region.

[0045] A semiconductor layer stack (14T, 14C, 14B) is formed over the top surfaces of the global bit lines 10 and the separator dielectric material portions. The semiconductor layer stack includes a first conductivity type semiconductor layer, a channel material layer including a semiconductor material, and a second conductivity type semiconductor layer having a same type of doping as the first conductivity type semiconductor layer. Subsequently, an optional sacrificial matrix layer 27 (e.g., a sacrificial cap) can be formed on the top surface of the semiconductor layer stack. The sacrificial matrix layer can include, for example, organosilicate glass, a semiconductor material, or other sacrificial material that can

be subsequently removed selective to the second conductivity type semiconductor layer.

[0046] The sacrificial matrix layer and the semiconductor layer stack are subsequently patterned into a one-dimensional array of rail structures extending along the first horizontal direction hd1. The rail structures include patterned remaining portions of the sacrificial matrix layer and the semiconductor layer stack, and are laterally spaced apart by trenches that extend along the first horizontal direction hd1. The first horizontal direction hd1 can be perpendicular to the second horizontal direction hd2 along which the global bit lines 10 extend.

[0047] A spacer dielectric portion 40 can be formed at the bottom of each trench. Each spacer dielectric portion 40 can be formed over of the global bit lines 10 and the separator dielectric material portions such that the top surface of the spacer dielectric portion 40 is located at a target height for placing a bottom edge of gate electrodes 18 to be subsequently formed. For example, the top surface of the spacer dielectric portion 40 can be at a level about the interface between the remaining portions of the first conductivity type semiconductor layer and the channel material layer. In one embodiment, each spacer dielectric portions 40 can include a vertical stack of a first spacer dielectric portion 40A and a second spacer dielectric portion 40B. The first spacer dielectric portion 40A can be deposited by a conformal deposition method, and the second spacer dielectric portion 40B can be deposited by a self-planarizing deposition method (such as spin coating). Portions of the first spacer dielectric portion 40A that protrudes above the top surface of the second spacer dielectric portion 40B can be removed, for example, by a selective etch that removes the material of the first spacer dielectric portion 40A selective to the material of the second spacer dielectric portion 40B. In one embodiment, the first spacer dielectric portion 40A can include silicon nitride, the second spacer dielectric portion 40B can include silicon oxide, and the selective etch can be a wet etch process that employs hot phosphoric acid.

[0048] The gate dielectrics 16 and the gate electrodes 18 of the access transistors can be subsequently formed, for example, by depositing a conformal gate dielectric layer (e.g., silicon oxide) and a conformal conductive material layer (e.g., heavily or degenerately doped polysilicon) in the trenches that separate the one-dimensional array of rail structures, and by anisotropically etching the conformal conductive material layer. The remaining vertical portions of the conformal conductive material layer constitute the gate electrodes 18, which extend along the first horizontal direction hd1. Each remaining portion of the conformal gate dielectric layer constitutes a gate dielectric 16. Each gate electrode 18 is laterally spaced from an adjacent rail structure by a vertical portion of a gate dielectric 16.

[0049] Remaining volumes of the trenches are filled with at least one dielectric material. Excess portions of the at least one dielectric material can be removed from above the horizontal plane including the top surfaces of the rail structures (which include remaining portions of the semiconductor layer stack and the sacrificial matrix layer) by a planarization process, which can employ, for example, chemical mechanical planarization. Each remaining portion of the deposited dielectric material in the trenches constitutes a dielectric rail structure 42.

[0050] Each dielectric rail structure 42 extends along the first horizontal direction hd1 parallel to the rail structures that include the remaining portions of the semiconductor layer stack and the sacrificial matrix layer. Each dielectric rail structure 42 can have a tapered bottom portion in which the width of the dielectric rail structure 42 monotonically or strictly increases as a function of a vertical distance from the substrate 6. In one embodiment, each dielectric rail structure 42 can include a dielectric liner 42A and a dielectric rail fill portion 42B. In one embodiment, the dielectric liners 42A can include silicon nitride, and the dielectric rail fill portions 42B can include silicon oxide.

[0051] As seen from above, dielectric rail structures 42 and the rail structures (including

remaining portions of the semiconductor layer stack (14T, 14C, 14B) and the sacrificial matrix layer 27) alternate along the second horizontal direction hd2 after formation of the dielectric rail structures 42.

[0052] Subsequently, a photoresist layer can be applied over the exemplary structure, and can be lithographically patterned to cover regions that overlie the global bit lines 10. In other words, openings are formed in areas between the areas of the global bit lines 10. In one embodiment, the photoresist layer can be patterned with the same pattern as the pattern of the one-dimensional array of the global bit lines 10 such that openings in the photoresist layer extend along the second horizontal direction hd2. Employing the combination of the photoresist layer and optionally the dielectric rail structures 42 as an etch mask, physically exposed portions of the rail structures (including remaining portions of the semiconductor layer stack and the sacrificial matrix layer) can be etched to form a two-dimensional array of pillar structures. Alternatively, the dielectric rail structures 42 are not used as a mask, and portions of the dielectric rail structures 42 that are not masked by the photoresist are etched together with the remaining portions of the semiconductor layer stack and the sacrificial matrix layer.

[0053] Each remaining portion of the sacrificial matrix layer constitutes a sacrificial material portion, and each remaining portion of the semiconductor layer stack constitutes a semiconductor pillar 14. Each pillar structure includes a vertical stack of a semiconductor pillar 14 and a sacrificial material portion 27. Each semiconductor pillar 14 includes a bottom active region 14B (which is a remaining portion of the first conductivity type semiconductor layer), a semiconductor channel 14C (which is a remaining portion of the channel material layer), and a top active region 14T (which is a remaining portion of the second conductivity type semiconductor layer).

[0054] Within each semiconductor pillar 14, one of the bottom active region 14B and the

top active region 14T is a source region, and the other of the bottom active region 14B and the top active region 14T is a drain region. The cross-sectional shape of each semiconductor pillar 14 can be substantially invariant throughout the entirety of the semiconductor pillar 14. Further, each overlying sacrificial material portion 27 can have substantially the same horizontal cross-sectional shape as the horizontal cross-sectional shape of the underlying semiconductor pillar 14.

[0055] The photoresist layer can be removed, for example, by ashing. The two-dimensional array of cavities that separate the pillar structures along the first horizontal direction hd1 can be filled with a dielectric fill material, which can include, for example, silicon oxide, organosilicate glass, and/or silicon nitride. The dielectric fill material can be removed from above the top surfaces of the dielectric rail structures 42, for example, by chemical mechanical planarization. Each remaining portions of the dielectric fill material constitutes a dielectric fill material portion 37 located between the semiconductor pillars 14 in the hd1 direction.

[0056] Referring to FIGS. 2A and 2B, an alternating stack of spacer material layers and insulating layers are formed over the one dimensional array of the dielectric rail structures 42 and the dielectric fill material portions as stacks of blanket (unpatterned) layers. A continuous insulating cap portion can be formed over the alternating stack of the spacer material layers and the insulating layers. In one embodiment of FIGS. 2A and 2B, the spacer material layers can be electrically conductive layers 30 that remain in a final device structure. In another embodiment, the spacer material layers can be sacrificial material layers that are subsequently replaced electrically conductive layers, as will be described in more detail below.

[0057] As used herein, an alternating stack of first elements and second elements refers to a structure in which instances of the first elements and instances of the second elements

alternate. Each instance of the first elements that is not an end element of the alternating plurality is adjoined by two instances of the second elements on both sides, and each instance of the second elements that is not an end element of the alternating plurality is adjoined by two instances of the first elements on both ends. The first elements may have the same thickness thereamongst, or may have different thicknesses. The second elements may have the same thickness thereamongst, or may have different thicknesses. The alternating plurality of the electrically conductive layers and the insulating layers may begin with an instance of the electrically conductive layers or with an instance of the insulating layers, and may terminate with an instance of the electrically conductive layers or with an instance of the insulating layers. In one embodiment, an instance of the first elements and an instance of the second elements may form a unit that is repeated with periodicity within the alternating plurality.

[0058] Subsequently, the continuous insulating cap portion and the alternating stack of the electrically conductive layers and the insulating layers are patterned to form line stack rail structures. Each line stack rail structure overlies a dielectric rail structure 42, extends along the first horizontal direction hd1, and is laterally spaced apart from one other line stack rail structures along the second horizontal direction hd2. Each patterned portion of the continuous insulating cap portion is herein referred to as an insulating cap portion 62. Each patterned portion of the electrically conductive layers is herein referred to as a conductive material layer 30 (e.g., word line). Each patterned portion of the insulating layer is herein referred to as an insulating layer. Thus, each line stack rail structure (30, 60, 62) includes an alternating stack of conductive material layers 30 and insulating layers 60 and an insulating cap portion 62. In one embodiment, each line stack rail structure (30, 60, 62) can have a lesser width along the second horizontal direction hd2 than the underlying dielectric rail structure 42, and can be entirety within the area of the underlying dielectric rail structure 42.

[0059] In one embodiment, the electrically conductive layers (i.e., the conductive material layers) 30 comprise a first electrically conductive material. In one embodiment, the first electrically conductive material can be a conductive metal nitride. In one embodiment, the first electrically conductive material can be selected from titanium nitride, tantalum nitride, titanium oxynitride in which a ratio of oxygen atoms to nitrogen atoms is less than 0.1, and tantalum oxynitride in which a ratio of oxygen atoms to nitrogen atoms is less than 0.1. Alternatively, conductive layers 30 may comprise a metal having a work function lower than 4.5 rather instead of or in addition to a metal nitride. In another embodiment, the first electrically conductive material can include a doped semiconductor material. The insulating layers 60 and the insulating cap portion 62 may comprise any suitable insulating material, such as silicon oxide.

[0060] The thickness of the conductive material layers 30 can be in a range from 5 nm to 60 nm, although lesser and greater thicknesses can also be employed. The thickness of the insulating lines 60 can be in a range from 5 nm to 60 nm, although lesser and greater thicknesses can also be employed. The thickness of the insulating cap portions 62 can be in a range from 5 nm to 300 nm, although lesser and greater thicknesses can also be employed.

[0061] A pair of a conductive material layer 30 and an insulating layer 60 can constitute a unit of repetition in the alternating stack (30, 60) of the conductive material layers 30 and the insulating layers 60. The total number of repetitions can be in a range from 8 to 1,024, although lesser and greater number of repetitions can also be employed. Thus, a plurality of alternating stacks (30, 60) of insulating layers 60 and conductive material layers 30 is formed over a substrate 6. Each of the insulating layers 60 and the conductive material layers 30 extends along the first horizontal direction (i.e., the word line direction) hd1. The alternating stacks (30, 60) are laterally spaced from one another along the second horizontal direction hd2 (i.e., the global bit line direction).

[0062] Subsequently, top regions of the sacrificial material portions 27 can be removed from above the top surfaces of the semiconductor pillars 14, for example, by an isotropic etch or an anisotropic etch. The isotropic or anisotropic etch can recess the sacrificial material portions 27 at least until the top surfaces of the semiconductor pillars 14 are physically exposed. In an illustrative example, if the sacrificial material portions 27 include organosilicate glass, a wet etch employing dilute hydrofluoric acid can be employed.

[0063] Referring to FIG. 3, an in-process layer stack 80L including multiple layers can be formed on the surfaces of the alternating stack (30, 60). The layer stack can include, from one side to another, a resistive memory material layer, a tunneling dielectric layer, and a steering element layer.

[0064] As used herein, a "resistive memory material" or a "reversibly resistance-switching material" is a material of which the resistivity can be altered by application of an electrical bias voltage across the material. As used herein, a "resistive memory material layer" refers to a layer including a resistive memory material. As used herein, a "resistive memory element" refers to a portion of a resistive memory material. As used herein, a "tunneling dielectric" refers to a dielectric material portion in which the predominant mode of electrical current conduction therethrough is charge carrier tunneling such as electron tunneling or hole tunneling. As used herein, a tunneling dielectric layer refers to a layer including at least one tunneling dielectric. As used herein, a "steering element" refers to an element, such as a diode, that provides a non-linear current-voltage characteristic for electrical current passing therethrough. In one embodiment, the steering element may have an asymmetric current-voltage characteristic (e.g., a diode which conducts current primarily in one direction (asymmetric conductance) and which has a lower resistance to the flow of current in one direction, and a higher resistance in the other direction). As used herein, a "steering element layer" refers to a layer including at least one steering element.

[0065] Examples of the resistive memory material include dielectric metal oxides through which reversible formation of conductive filaments can occur. Such dielectric metal oxides include, but are not limited to, oxides of Hf, Ti, Zr, Al, and Ta. The resistive memory materials provide reversible resistance switching by formation and erasure of conductive filaments. In a configuration in which a reversibly resistance-switching material is disposed between a first electrode (e.g., a word line or a vertical bit line) and a second electrode (e.g., a vertical bit line or a word line), conductive filaments can be formed within the reversibly resistance-switching material by application of an electrical bias, and can be removed from the reversibly resistance-switching material by application of a reverse electrical bias. In a non-limiting illustrative example, the first electrode can be made of titanium nitride (or any material that can be employed as the first electrically conductive material of the conductive material layers 30), and the second electrode can be made of platinum or n-doped polysilicon (or any material that can be employed as a second electrically conductive material of electrically conductive lines to be subsequently formed). The device of the present disclosure is not restricted to any one set of materials for forming the non-volatile memory elements.

[0066] Metal oxides are characterized by being insulating when initially deposited. A metal oxide can be formed with oxygen deficiencies (e.g., vacancies), or can be annealed to form oxygen deficiencies. The second electrode can include a high work function material having a work function greater than 4.5 eV, and can be employed to provide a high potential barrier for electrons at the interface with the reversibly resistance-switching material. As a result, at moderate voltages (below one volt), a very low current will flow through the reversibly resistance-switching material. The energy barrier at the interface between the second electrode and the reversibly resistance-switching material can be lowered by the presence of the oxygen vacancies (O^{+2}). In this case, the interface between the second

electrode and the reversibly resistance-switching material can provide the characteristics of a low resistance contact (Ohmic contact). The oxygen vacancies in the metal oxide of the reversibly resistance-switching material function as n-type dopants, thereby transforming the originally insulating metal oxide into an electrically insulating material having a lower resistivity (but still insulating). The resulting composite structure is in a non-conductive (high resistance) state in the absence of conductive filaments therein.

[0067] When a large forward bias voltage (such as a negative voltage of about -1.5 volt that is applied to the second electrode with respect to the first electrode) is applied across the reversibly resistance-switching material, the oxygen vacancies drift toward the interface between the high energy barrier material (such as platinum or n-dope polysilicon) and the reversibly resistance-switching material, and as a result, the potential barrier at the interface between the second electrode and the reversibly resistance-switching material is reduced and a relatively high current can flow through the structure. The device is then in its low resistance (conductive) state in which the reversibly resistance-switching material functions as a semiconducting material or a conductive material. Without wishing to be bound by a particular theory, it is believed that conduction occurs by formation of conductive filaments having a high density of oxygen vacancies, which may occur along grain boundaries.

[0068] The conductive path can be broken by applying a large reverse bias voltage (such as a positive voltage of about 1.5 volt that is applied to the second electrode with respect to the first electrode) across the reversibly resistance-switching material. Under a suitable reverse bias condition, the oxygen vacancies move away from the proximity of the interface between the high work function material and the reversibly resistance-switching material, and "break" the conductive filament. The resistivity of the reversibly resistance-switching material returns to its high resistance state. Both of the conductive and non-conductive states are non-volatile. Sensing the conduction of the memory storage element (for example, by

applying a voltage around 0.5 volts) can easily determine the state of the memory element.

[0069] While this specific conduction mechanism may not apply to all metal oxides, as a group, they have a similar behavior: transition from a low conductive state to a high conductive occurs state when appropriate voltages are applied, and the two states are non-volatile. Examples of other materials that can be used for the non-volatile memory elements include hafnium oxide, such as HfO_x where $1.9 < x < 2.1$. Suitable materials for the first electrode (e.g., word line) are any conducting material such as Ti(O)N, Ta(O)N, TiN, TiAlN, WN and TaN. Suitable materials for the second electrode (e.g., local bit line) include metals and doped semiconductor with a high work function (typically >4.5 eV) capable to getter oxygen in contact with the metal oxide to create oxygen vacancies at the contact. Some examples are TaCN, TiCN, Ru, RuO_2, Pt, Ti rich TiO_x, TiAlN, TaAlN, TiSiN, TaSiN, IrO_2 and doped polysilicon. The thicknesses of the electrodes are typically 1 nm or greater. Thicknesses of the metal oxide can be generally in the range of 2 nm to 20 nm.

[0070] In an alternative embodiment, the resistive memory material may comprise a semiconductor material, such as a chalcogenide semiconductor material, for example Ge-Sb-Te material, which changes its resistance due to a change in the crystallinity of the material. For example, the material may go from an amorphous crystal state to a polycrystalline crystal state upon application of a first voltage and go from the polycrystalline crystal state to an amorphous crystal state upon an application of a second voltage.

[0071] The tunneling dielectric layer includes a dielectric material through which electron tunneling or hole tunneling can occur. In one embodiment, the tunneling dielectric layer includes a dielectric material having a dielectric constant of at least 7.0. For example, the tunneling dielectric layer can include a dielectric material selected from silicon nitride and aluminum oxide. In one embodiment, the thickness of the tunneling dielectric layer can be in a range from 0.6 nm to 4 nm (such as from 1.0 nm to 3 nm), although lesser and greater

thicknesses can also be employed.

[0072] The steering element layer can include at least one semiconductor element that provides a non-linear current-voltage characteristic. For example, the steering element layer can include at least one diode therein. In one embodiment, each diode can include a heavily doped n-doped semiconductor region (i.e., n+ region) having n-type dopants at an atomic concentration greater than $5.0 \times 10^{19}/cm^3$, and a lightly or lighter doped p-doped semiconductor region (i.e., p- or p region) including p-type dopants at an atomic concentration less than $5.0 \times 10^{19}/cm^3$. In one embodiment, the n-doped semiconductor regions can be embodied as discrete n-doped semiconductor material portions. In another embodiment, the n-doped semiconductor regions can be embodied as portions of a continuous n-doped semiconductor material layer. In one embodiment, each n-doped semiconductor region can be incorporated as a portion of a second electrode.

[0073] Referring to FIGS. 4A and 4B, an anisotropic etch can be performed to remove horizontal portions of the in-process layer stack 80L. Each remaining vertical portions of the in-process layer stack 80L is a layer stack 80 including, from one side to another, a resistive memory material layer, a tunneling dielectric layer, and a steering element layer.

[0074] In one embodiment, each second electrode can be embodied as the electrically conductive layers 30, and each first electrode can be embodied as a vertically-extending electrically conductive line to be subsequently formed on a respective layer stack 80. In another embodiment, each first electrode can be embodied as the electrically conductive layers 30, and each second electrode can be embodied as a vertically-extending electrically conductive line to be subsequently formed on a respective layer stack 80.

[0075] Referring to FIGS. 5A – 5C, a laterally alternating stack of electrically conductive lines 90 and dielectric pillar structures 96 is formed within each trench located between a neighboring pair of line stack rail structures (30, 60, 62).

[0076] In one embodiment, a second electrically conductive material can be deposited within the trenches among the line stack rail structures (30, 60, 62), for example, by a conformal deposition process. The second electrically conductive material can include a conductive metallic nitride (e.g., TiN), a doped semiconductor material (e.g., polysilicon having p-type or n-type doping concentration greater than $5.0 \times 10^{19}/cm^3$), an elemental metal, and/or an intermetallic alloy (e.g., TiW) of at least two elemental metals. The second electrically conductive material can be the same as, or can be different from, the first electrically conductive material.

[0077] Excess portions of the second electrically conductive material deposited over the horizontal plane including the top surfaces of the line stack rail structures (30, 60, 62) can be removed, for example, by chemical mechanical planarization. Thus, each remaining portion of the deposited second electrically conductive material can fill a trench between a neighboring pair of line stack rail structures (30, 60, 62). Each portion of the deposited second electrically conductive material can be divided into a plurality of electrically conductive lines (e.g., local bit lines) that extend along the vertical direction, for example, by applying a photoresist layer over the top surfaces of the second electrically conductive material portions and the line stack rail structures (30, 60, 62), patterning the photoresist layer to form openings in areas that do not overlie the global bit lines 10, and removing the physically exposed portions of the second electrically conductive material employing a combination of the photoresist layer and the insulating cap portions 62 as an etch mask. Each remaining portion of the second electrically conductive material constitutes an electrically conductive line 90, which can have a shape of a pillar structure. A plurality of electrically conductive lines 90 is formed on the vertically spaced sets of layer stacks 80.

[0078] Each of the electrically conductive lines 90 can be formed over an area of a respective vertical field effect transistor (14, 16, 18), which is herein referred to as a first

select transistor. Each select transistor can electrically connect a global bit line 10 to an electrically conductive line 90, or can electrically disconnect (i.e., provide an electrical open between) the global bit line 10 and the second electrically conducive line 90. A switched node of each first select transistor (i.e., a top active region 14T) is connected to an end of a respective electrically conductive line 90. Each electrically conductive line 90 can be formed as a generally pillar-shaped structure.

[0079] The electrically conductive lines 90 form a two-dimensional array having the same periodicity as the array of vertical field effect transistors (14, 16, 18) (i.e., the first access transistors). The electrically conductive lines 90 are spaced apart from one another by cavities along the first horizontal direction hd1, and by the line stack rail structures (30, 60, 62) along the second horizontal direction hd2.

[0080] A dielectric material (such as silicon oxide) can be deposited into the cavities. Excess portions of the dielectric material can be removed from above a horizontal plane including the top surfaces of the line stack rail structures (30, 60, 62) and the electrically conductive lines 90, for example, by chemical mechanical planarization. Dielectric material pillars 96 are formed in each volume of the cavities, i.e., between the electrically conductive lines 90 and between the line stack rail structures (30, 60, 62) (and therefore, between the alternating stacks (30, 60)). In this configuration, the electrically conductive lines 90 are formed as a two-dimensional array in which the electrically conductive lines 90 are spaced from one another by the dielectric material pillars 96 along the first horizontal direction hd1, and by the alternating stacks (30, 60) along the second horizontal direction hd2.

[0081] As shown in FIG. 5C, second select transistors (T1 – T4) (e.g., word line select transistors) for selectively activating a respective conductive material layer 30 (i.e., word line) can be formed at any suitable stage of the processing sequence. For example, the second select transistors can be formed in, or on, the substrate 6 if the substrate 6 includes a

semiconductor substrate. Alternatively or additionally, the second select transistors can be formed prior to, concurrently with, or after formation of the first select transistors (14, 16, 18). Alternatively or additionally, the second select transistors can be formed prior to, or after, formation of the electrically conductive lines 90. Any method for forming transistors as known in the art can be employed to provide the second select transistors. A switched node (e.g., a source region or a drain region) of each second select transistor can be connected to an end of a respective conductive material layer 30, and another node (e.g., a drain region or a source region) can be connected to a voltage source (or current source) which provides a node activation voltage V_a.

[0082] In one embodiment, each global bit line 10 laterally extends along the second horizontal direction hd2, and two or more of the first selector transistors (14, 16, 18) can be electrically connected to the global bit line 10. The first select transistors (14, 16, 18) are configured to activate a selected electrically conductive line 90 by supplying an activation voltage thereto from a respective global bit line 10, and the second select transistors (T1 – T4) are configured to activate a selected conductive material layer 30 by supplying another activation voltage thereto. In one embodiment, the exemplary structure can include a monolithic three-dimensional memory device comprises a resistive random access memory (ReRAM) device.

[0083] Referring to FIG. 6A, a portion of a first exemplary layer stack 80 is illustrated, which includes a steering element 84, a resistive memory element 88 and a tunneling dielectric element 86 located between the steering element 84 and the resistive memory element 88. The layers in the stack 80 may be stacked vertically (i.e., in a direction perpendicular to the top surface of the substrate), horizontally (i.e., in a direction parallel to the top surface of the substrate) or in any one or more directions in between vertical and horizontal. In one embodiment, the stack 80 includes the steering element 84 having a non-

linear current-voltage characteristic for electrical current passing therethrough, the tunneling dielectric element 86 contacting the steering element 84, and the resistive memory element 88 contacting the tunneling dielectric element 86. The predominant mode of electrical current conduction through the tunneling dielectric element 86 is charge carrier tunneling such as electron tunneling or hole tunneling. The resistive memory element 88 includes a dielectric material having multiple states providing different electrical resistance depending on an electrical bias that is previously applied thereto.

[0084] In one embodiment, a first metallic material portion can be in contact with the steering element 84, and a second metallic material portion can be in contact with the resistive memory element 88. For example, an electrically conductive layer 30 (such as one of the electrically conductive layers 30 in the exemplary structure of FIGS. 5A – 5C) can be located in contact with the steering element 84, and an electrically conductive line 90 (such as one of the electrically conductive lines 90 in the exemplary structure of FIGS. 5A – 5C) can be located in contact with the resistive memory element 88.

[0085] In one embodiment, the steering element 84 includes a diode. For example, the diode can include a first conductivity type semiconductor layer 83 (e.g., an n-doped semiconductor layer) including dopants of a first conductivity type (e.g., n-type dopants) at an atomic concentration greater than $5.0 \times 10^{19}/cm^3$, such as $6.0 \times 10^{19}/cm^3$ to $1.0 \times 10^{21}/cm^3$, a second conductivity type semiconductor region 85 (e.g., a p-doped semiconductor layer) including dopants of a second conductivity type (which is the opposite of the first conductivity type, e.g., p-type dopants) at an atomic concentration less than $5.0 \times 10^{19}/cm^3$, such as $1.0 \times 10^{17}/cm^3$ to $4.0 \times 10^{19}/cm^3$. The thickness of the first conductivity type semiconductor layer 83 can be in a range from 20 nm to 1 micron, and the thickness of the second conductivity type semiconductor layer 85 can be in a range from 2 nm to 100 nm, although lesser and greater thicknesses can also be employed. In one embodiment, the

electrically conductive layer 30 and the first conductivity type semiconductor layer 83 can be embodied in a single conductive material layer including a doped semiconductor material having a doping of the first conductivity type.

[0086] In one embodiment, the tunneling dielectric element 86 comprises a dielectric material having a dielectric constant of at least 7.0, which can be silicon nitride or a dielectric metal oxide. In one embodiment, the tunneling dielectric element 86 can include a dielectric material selected from silicon nitride and aluminum oxide. In one embodiment, the dielectric constant of element 86 is less than the dielectric contact of element 88. Thus, if the element 88 comprises hafnium oxide having a dielectric constant of 25, then the dielectric constant of element 86 may be between 7 and 24. In one embodiment, the tunneling dielectric element 86 can have a thickness in a range from 0.6 nm to 4 nm (such as from 1 nm to 3 nm), although lesser and greater thicknesses can also be employed.

[0087] In one embodiment, the resistive memory element 88 comprises a dielectric oxide providing a reduction in resistivity upon formation of conductive filaments therein. In one embodiment, the resistive memory element 88 comprises a dielectric oxide of a metal selected from Hf, Ti, Zr and Ta, such as hafnium oxide. Any other resistive memory material (e.g., chalcogenide semiconductor) can be employed for the resistive memory element 88.

[0088] Referring to FIG. 6B, a portion of a second exemplary layer stack 80 is illustrated, which can include the same layer stack as the first exemplary layer stack 80 in FIG. 6A. An electrically conductive layer 30 (such as one of the electrically conductive layers 30 in the exemplary structure of FIGS. 5A – 5C) can be located in contact with the resistive memory element 88, and an electrically conductive line 90 (such as one of the electrically conductive lines 90 in the exemplary structure of FIGS. 5A – 5C) can be located in contact with the steering element 84. In one embodiment, the electrically conductive line 90 and the first conductivity type semiconductor layer 83 can be embodied in a single conductive material

layer including a doped semiconductor material (e.g., n+ polysilicon) having a doping of the first conductivity type.

[0089] Referring to FIG. 6C, a portion of a third exemplary layer stack 80 is illustrated, which can be derived from the first exemplary layer stack 80 by providing a metallic liner 89 between the resistive memory element 88 and the electrically conductive line 90. The metallic liner 89 can include a conductive diffusion barrier material such as a conductive metallic nitride (e.g., TiN, TaN, or WN) or a conductive metallic carbide (e.g., TiC, TaC, or WC). The metallic liner 89 can have a thickness in a range from 1 nm to 30 nm, although lesser and greater thicknesses can also be employed.

[0090] Referring to FIG. 6D, a portion of a fourth exemplary layer stack 80 is illustrated, which can be derived from the second exemplary layer stack 80 by providing a metallic liner 81 between the steering element 84 and the electrically conductive line 90. The metallic liner 81 can include a conductive diffusion barrier material such as a conductive metallic nitride (e.g., TiN, TaN, or WN) or a conductive metallic carbide (e.g., TiC, TaC, or WC). The metallic liner 81 can have a thickness in a range from 1 nm to 30 nm, although lesser and greater thicknesses can also be employed.

[0091] Referring to FIG. 6E, a portion of a fifth exemplary layer stack 80 is illustrated, which can be derived from the third or fourth exemplary layer stack 80 by providing an additional metallic liner. Specifically, a first metallic liner 81 can be provided between the electrically conductive layer 30 and the steering element 84, and a second metallic liner 89 can be provided between the electrically conductive line 90 and the resistive memory element 88.

[0092] The memory element which includes the tunneling dielectric element may provide a more symmetric current-voltage profile for forward and reverse bias modes than a similar memory element which lacks the tunneling dielectric element. The memory element

containing both a steering element and the tunneling dielectric element has both a high non-linearity factor (e.g., greater than 400:1 at 1 Volt, such as 425:1 to 750:1) and a high current density (e.g., greater than 10^5 A/cm^2, such as $5x10^5$ to $1x10^7$ A/cm^2).

[0093] FIG. 7A illustrates a current-voltage plot 710 of a diode-tunneling dielectric-metal structure of an embodiment the present disclosure, and a current-voltage plot 720 of a comparative diode-metal structure which lacks the tunneling dielectric. The diode-tunneling dielectric-metal structure can be derived from first or second exemplary layer stack 80 illustrated in FIGS. 6A or 6B by removing the resistive memory element 88. The comparative diode-metal structure can be derived from the diode-tunneling dielectric-metal structure by removing the tunneling dielectric element 86. Both structures include a second conductivity type (e.g., p-type) semiconductor layer 85 having a doping of about 2.0 x 10^{19}/cm^3 and having a thickness of 10 nm, while the embodiment structure also includes a silicon nitride tunneling dielectric element 86 having a thickness of 1.0 nm. As can be seen in FIG. 7A, the plot 710 of the embodiment device has a higher symmetry between forward and reverse bias modes (i.e., value of current for positive and negative voltage of the same absolute value) than the plot 720 of the comparative device. Thus, combination of the steering element 84 and the tunneling dielectric element 86 of the embodiment of the present disclosure can be employed as a non-linear switching device that is turned off when the external bias voltage is zero, and is turned on for a forward bias voltage and for a reverse bias voltage having an absolute magnitude as low as 1.0 V to 3.0 V.

[0094] FIG. 7B is a graph illustrating a variation in current-voltage characteristics of a diode-tunneling dielectric-metal structure of the present disclosure as a function of the p-type semiconductor layer 85 doping and thickness. The diode-tunneling dielectric-metal structure can be derived from first or second exemplary layer stack 80 illustrated in FIGS. 6A or 6B by removing the resistive memory element 88. In plot 730, the thickness of the p-type

semiconductor layer 85 is about 10 nm and its p-type doping concentration is $1x10^{19}$ cm^{-3}. In plot 740, the thickness of the p-type semiconductor layer 85 is also about 10 nm but its p-type doping concentration is increased to $2x10^{19}$ cm^{-3}. In plot 750, the thickness of the p-type semiconductor layer 85 is reduced to about 5 nm and its p-type doping concentration is increased to $5x10^{19}$ cm^{-3}. As can be seen from these plots, the curves become tighter around the zero volt axis as the thickness and the doping concentration of layer 85 decreases. In other words, a higher current is obtained for the same value of voltage as the thickness and doping concentration of layer 85 decreases. The dependence of the current-voltage performance characteristic(s) of the device on the p-type layer thickness and/or doping concentration permits a flexibility in the design of the memory device. For example, in a method of making the memory device at least one desired current-voltage performance characteristic (e.g., current for an applied voltage) of the device may be determined, such as by being calculated and/or being received from a user of the device. At least one of the thickness and p-type doping concentration of a p-type semiconductor layer of a diode steering element may then be selected which provides the desired current-voltage performance characteristic(s). The thickness and/or doping concentration may be selected from a look-up table based on experimental or calculated data, it may be selected from a graph such as Fig. 7B or it may be calculated. The diode steering element is then fabricated with the n-type semiconductor layer 83 and the p-type semiconductor layer 85 having the selected at least one of thickness and doping concentration. The resistive memory element and the tunneling dielectric element are then formed, such that the tunneling dielectric element is located between the diode steering element and the resistive memory element.

[0095] The operation of the combination of the steering element 84 and the tunneling dielectric element 86 of the present disclosure as a selector element in a forward bias condition is illustrated in FIG. 8A. During a forward bias condition (i.e., application of a 1V

and 2V positive voltage to the electrode 30 facing the p-type region of the diode), a high nonlinearity factor (NLF) is provided because of effective reduction of energy barrier (i.e., the lowering of the conduction and valence bands of the p-type silicon layer 85 at the interface with element 86) and enhanced electron tunneling through the tunneling dielectric element 86 from the electrode 30 to layer 85 of the diode. This phenomenon is analogous to formation of an inversion layer in the channel of a field effect transistor for increasing the current conduction in the channel.

[0096] The operation of the combination of the steering element 84 and the tunneling dielectric element 86 of the present disclosure as a selector element in a reverse bias condition (i.e., application of a -1V and -2V negative voltage to the electrode 30 facing the p-type region of the diode), is illustrated in FIG. 8B. During a reverse bias condition, electrons can tunnel through the tunneling dielectric element 86 from the side of the electrode 30 through element 86. The p-doped semiconductor layer 85 can be in an accumulation mode to provide a significant electrical current through the selector element. In other words, holes accumulate at the boundary between layer 85 and element 86 to lower the conduction and valence bands of layer 85 to facilitate tunneling of electrons from the electrode 30 through element 86 and layer 85 into the n-type semiconductor layer 83.

[0097] This effect is illustrated in more detail in FIG. 8C which shows the band gap diagrams of the embodiment device and the comparative device described above in reverse bias condition at -1V. For the same -1V reverse bias, the barrier to electron tunneling from the electrode 30 into the n-type semiconductor layer 83 through the p-type semiconductor layer 85 is higher for the comparative device than for the embodiment device. This is believed to be due to the accumulation of holes in the valence band of layer 85 at the interface with element 86. This results in a lowering of the conduction and valence band energies of layer 85 at the interface with layer 86 and in enhancement of tunneling of

electrons from electrode 30 through element 86 and layer 85 into layer 83 due to the lower tunneling barrier (i.e., lower conduction band energy) in layer 85. Thus, the embodiment device provides a more symmetric forward and reverse bias current-voltage characteristic and provides a lower current density for the same voltage or the same current density for a lower voltage than the comparative device.

[0098] In summary, the present inventors realized that symmetric prior art steering devices, such as metal-insulator-metal (MIM) and metal-semiconductor-metal (MSM) suffer from the nonlinearity factor ("NLF") -current tradeoff: thicker films have excellent NLF but drop too much voltage (and thus current decreases); thinning the films requires less voltage drop but their NLF is degraded. A prior art forward-biased diode provides high NLF and high current capacity, but at the cost of being highly asymmetric.

[0099] In contrast, the present inventors realized that using the diode with a thin lightly doped p-type region and a heavily doped n-type region in series with the tunneling dielectric element in the forward bias condition (i.e., mode) provides a high NLF and a high current, and in the reverse bias condition (i.e., mode) provides a comparable or better performance than the MSM structure. It provides a high current and good symmetry while trading off the high NLF similar to the MSM structure. The embodiment device can be used in forward bias mode for RESET operation, where the highest current and the lowest voltage are desirable.

[00100] Furthermore, the present inventors realized that addition of tunneling dielectric element adjacent to the p-type semiconductor regions of the diode reduces the asymmetry in the diode current-voltage behavior in forward and reverse bias modes. This is believed to be due to the facilitation of electron tunneling from the cathode electrode 30 to the p- layer 83 through the element 86. This is believed to occur because the p- layer 83 is in accumulation in the presence of layer 86 and the field direction is conducive for electron tunneling. This improves the current in the reverse bias direction and makes the I-V plot more symmetric in

forward and bias modes. Thus, it is believed that element 86 mitigates asymmetry of the standard p-n diode selector current-voltage behavior in forward and reverse bias modes. Furthermore, as described with respect to FIG. 7B, the combined current-voltage characteristics of the device (e.g., of the steering element including the diode, the tunneling dielectric and the conductor, such as a metal) may be tuned by adjusting the thickness and/or the doping concentration of p-type layer 85. This improves the flexibility in the design of the device by obtaining the desired current-voltage characteristics of the device by selecting a specific thickness and doping concentration of the p-type layer 85.

[00101] The layer stack 80 of the present disclosure can be embodied in many different configurations, and can be formed employing many different sets of processing steps. The following exemplary manufacturing methods and structures are non-limiting exemplary implementations of the layer stack 80 of the present disclosure.

[00102] In embodiments illustrated in FIGS. 9A-9D and 10A-10D, an alternating stack of insulating layers 60 and spacer material layers can be formed as an alternating stack of insulating layers 60 and sacrificial material layers 33 during formation of the exemplary structure of FIGS. 5A – 5C (e.g., at the processing step corresponding to FIGS. 2A and 2B). The sacrificial material layers 33 can then be replaced with electrically conductive layers (e.g., word lines) 30 during a subsequent step. In these embodiments, the tunneling dielectric element 86 and/or the steering element 84 are optional and may or may not be included in the memory cells. In other words, in these embodiments, the memory cell may include the resistive memory element 88 and portions of a word line 30 and bit line 90, and optionally one or both of the tunneling dielectric element 86 and/or the steering element 84.

[00103] The sacrificial material layers 33 can include a material that can be removed selective to the material of the insulating layers 60 in a subsequent processing step. For example, the insulating layers 60 can include silicon oxide (such as silicon dioxide,

fluorosilicate glass, borosilicate glass, borophosphosilicate glass, phosphosilicate glass, and organosilicate glass), and the sacrificial material layers 33 can include silicon nitride or amorphous or polycrystalline semiconductor material (such as polysilicon).

[00104] Referring to FIGS. 9A-9D, a first exemplary three-dimensional memory device employing an embodiment of the layer stack 80 of the present disclosure is illustrated at various stages of a manufacturing process. As shown in FIG. 9A, an alternating stack of insulating layers 60 and sacrificial material layers 33 that alternate along a first direction is formed over a substrate. The substrate can be, for example, the substrate 6 of the exemplary structure of FIGS. 1A and 1B, or can be any other substrate that can provide mechanical support to the alternating stack. The first direction may be a vertical direction that is perpendicular to the substrate as illustrated in FIGS. 2A and 2B, or may be a horizontal direction. The alternating stack can be patterned to form sidewalls that extend along the first direction. A combination of lithographic methods and an etch process can be employed to form the sidewalls of the alternating stack. For example, the processing steps of FIGS. 2A and 2B may be employed to form the sidewalls of the alternating stack. In one embodiment, the sidewalls of the alternating stack may be within a same plane (i.e., a two-dimensional Euclidean plane).

[00105] A doped semiconductor layer (e.g., polysilicon) can be formed on the sidewalls of the alternating stack (33, 60). The doped semiconductor layer is herein referred to as a second conductivity type semiconductor layer 85. The conductivity type of the second conductivity type semiconductor layer 85 is herein referred to as a second conductivity type. The second conductivity type may be p-type or n-type. In one embodiment, the second conductivity type can be p-type. In one embodiment, the atomic concentration of the dopants of the second conductivity type can be less than $5.0 \times 10^{19}/cm^3$, although greater atomic concentrations can also be employed.

[00106] Another doped semiconductor layer (herein referred to as a first conductivity type semiconductor layer 83) having a doping of the opposite conductivity type can be formed on the second conductivity type semiconductor layer 85 to provide a continuous p-n junction. The direction of the thickness of the first conductivity type semiconductor layer 83 is herein referred to as a second direction. The first conductivity type semiconductor layer 83 extends at least along the first direction, and may extend along a third direction that is perpendicular to the first direction and to the second direction. The extent of the first conductivity type semiconductor layer 83 as deposited may have a greater extent along the first direction than along the second and third directions, thereby rendering the first conductivity type semiconductor layer 83 to be an electrically conductive line 90. Alternatively or additionally, the first conductivity type semiconductor layer 83 can be subsequently patterned such that each remaining portion of the first conductivity type semiconductor layer 83 extends farther along the first direction than along the second and third directions, thereby rendering each remaining portion of the first conductivity type semiconductor layer 83 to be an electrically conductive line 90. Thus, the electrically conductive line 90 can be formed by depositing a first conductivity type semiconductor layer 83 having a doping of a first conductivity type over the sidewalls of the alternating stack (33, 60).

[00107] The layer stack 80 employed in the first exemplary three-dimensional memory device can be the same as a modification of the exemplary structure of FIG. 6B in which the first conductivity type semiconductor layer 83 functions as the electrically conductive line 90. Thus, a structure (83/90) that is both an electrically conductive line 90 and a first conductivity type semiconductor layer 83 extends along the first direction over the sidewalls of the alternating stack (33, 60). The second conductivity type semiconductor layer 85 is interposed between the electrically conductive line 90 and the sidewalls of the alternating stack (33, 60). The electrically conductive line 90 is formed on the second conductivity type semiconductor

layer 85.

[00108] Each portion of the p-n junction between the first and second conductivity type semiconductor layers (83, 85) that is located adjacent to a sidewall of the sacrificial material layers 33 constitutes a steering element. Each steering element comprises a portion of a continuous p-n junction between the first and second conductivity type semiconductor layers (83, 85). Each of the steering elements comprises a diode.

[00109] As shown in FIG. 9B, a backside trench 92 is formed in the stack. The sacrificial material layers 33 can be removed selective to the insulating layers 60 and to the second conductivity type semiconductor layer 85 through the trench 92 by an etch process, which can be an isotropic etch process or an anisotropic etch process. In an illustrative example, the insulating layers 60 can include silicon oxide, the sacrificial material layers 33 can include silicon nitride, and the etch process can be a wet etch process employing phosphoric acid. In another illustrative example, the insulating layers 60 can include silicon oxide, the sacrificial material layers 33 can include germanium or a silicon-germanium alloy, and the etch process can be a wet etch process employing hydrogen peroxide. Recesses 43 are formed in volumes from which the sacrificial material layers 33 are removed. The recesses 43 as initially formed are cavities bounded by surfaces of the insulating layers 33 and physically exposed surfaces of the second conductivity type semiconductor layer 85.

[00110] Tunneling dielectric elements are formed by depositing a tunneling dielectric layer 86L through the trench 92 within the recesses 43 and directly on surfaces of the insulating layers 33 and directly on surfaces of the steering elements (83, 85) by any suitable method, such as atomic layer deposition (ALD). Each tunneling dielectric element is a portion of the tunneling dielectric layer 86L that is located in proximity to a steering element, i.e., a portion of the p-n junction in proximity to the recesses 43. In one embodiment, the tunneling dielectric layer 86L can include a dielectric material having a dielectric constant of at least

7.0 (such as silicon nitride or a dielectric metal oxide), and can have a thickness in a range from 0.6 nm to 4 nm.

[00111] Resistive memory elements are formed as a resistive memory material layer 88L through the trench 92 within the recesses 43 and on the tunneling dielectric elements (as embodied as the tunneling dielectric layer 86L), such as a hafnium oxide layer formed by ALD. Each resistive memory element includes a portion of the resistive memory material layer 86L that is separated from the second conductivity type semiconductor layer 85 by the thickness of the tunneling dielectric layer 86L. In other words, each resistive memory element is a portion of the resistive memory material layer 86L that is in contact with a portion of the tunneling dielectric layer 86L which contacts the second conductivity type semiconductor layer 85. In one embodiment, each of the resistive memory elements comprises a dielectric oxide providing a reduction in resistivity upon formation of conductive filaments therein.

[00112] As shown in FIG. 9C, a continuous electrically conductive layer 30L can be formed by depositing at least one conductive material in the remaining portions of the recesses 43 as a continuous material layer. All remaining volumes of the recesses 43 may be filled by the continuous electrically conductive layer. In one embodiment, the continuous electrically conductive layer 30L can include at least one electrically conductive material selected from a metal nitride, an elemental metal, and an intermetallic alloy of at least two elemental metals. Alternatively or additionally, the continuous electrically conductive layer 30L can include a doped semiconductor material, such as doped polysilicon.

[00113] The proximal sidewalls 60A of the insulating layers 60 contact the steering elements (83, 85), and the distal sidewalls 60B of the insulating layers 60 do not contact the steering elements (83, 85). As shown in FIG. 9D, the continuous electrically conductive layer 30L, the resistive memory material layer 88L, and optionally, the tunneling dielectric

layer 86L can be divided into discrete portions by removing portions in the trench 92 that are spaced from the steering elements (83, 85) by the insulating layers 30. Specifically, portions of the continuous electrically conductive layer 30L, the resistive memory material layer 88L, and optionally, the tunneling dielectric layer 86L in the trench 92 that are farther away from the first and second conductivity type semiconductor layers (83, 85) than the distal surfaces of the insulating layers 60 can be removed, for example, by an anisotropic etch employing an etch mask layer, which may be a patterned photoresist layer (not shown) and/or a topmost insulating layer 60 (or 62 in FIG. 5A) in case the first direction is a vertical direction. Dielectric fill material portions 98 can be formed in trench 92 formed by removal of portions of the continuous electrically conductive layer 30L, the resistive memory material layer 88L, and optionally, the tunneling dielectric layer 86L.

[00114] Each remaining discrete portion of the continuous electrically conductive layer 30L constitutes an electrically conductive layer 30 (e.g., word line). Each remaining discrete portion of the resistive memory material layer 88L constitutes a resistive memory element 88. In case the tunneling dielectric layer 86L is divided into discrete portions, each remaining portion of the tunneling dielectric layer 86L constitutes a tunneling dielectric element 86. A combination of an electrically conductive layer 30, a resistive memory element 88, and a tunneling dielectric element 86 can be formed within each recess 43. Each combination of a resistive memory element 88, a tunneling dielectric element 86, and a steering element that is a portion of the first and second conductivity type semiconductor layers (83, 85) that is proximal to a respective tunneling dielectric element 86 collectively constitutes a memory cell. An array of memory cells arranged along the first direction is provided. Each of the memory cells comprises a steering element (83, 85), a tunneling dielectric element 86, and a resistive memory element 88. At least one element of each memory cell is formed within a respective recess 43. Thus, the n+ polysilicon pillars act as both the n+ layer 83 of the diode

and as the vertical bit lines 90.

[00115] Referring to FIGS. 10A-10D, a second exemplary three-dimensional memory device employing an embodiment of the layer stack 80 with discrete portions of element 86 of the present disclosure is illustrated at various stages of a manufacturing process. As shown in FIG. 10A, an alternating stack of insulating layers 60 and sacrificial material layers 33 that alternate along a first direction is formed over a substrate, and is patterned to form sidewalls as in the processing steps of FIG. 9A. A second conductivity type semiconductor layer 85 and a first conductivity type semiconductor layer 83 are sequentially formed as in the processing steps of FIG. 9A. As shown in FIG. 10B, recesses 43 are formed by partially or fully removing the sacrificial material layers 33 selective to the insulating layers 60 and to the second conductivity type semiconductor layer 85 employing an etch process as in the processing steps of FIG. 9B.

[00116] Tunneling dielectric elements 86 are formed as discrete dielectric material portions (e.g., discrete strips or segments) that are self-aligned to portions of the steering elements that are physically exposed to the recesses 43. For example, the silicon nitride sacrificial layers 33 are partially removed by etching to leave discrete silicon nitride segments or strips 86 at the end of the recesses 43. Alternatively, layers 33 are fully removed and then separate tunneling dielectric elements 86 can be formed by a self-aligned formation process such as nitridation of surface portions of the second conductivity type semiconductor layer 85 that are physically exposed to the recesses 43. In one embodiment, each tunneling dielectric element 86 can include a dielectric material having a dielectric constant of at least 7.0 (such as silicon nitride or a dielectric metal oxide), and can have a thickness in a range from 0.6 nm to 4 nm.

[00117] Resistive memory elements are formed as a resistive memory material layer 88L within the recesses 43 and on the tunneling dielectric 86. Processing steps of FIG. 9B may be

employed to form the resistive memory material layer 88L.

[00118] As shown in FIG. 10C, a continuous electrically conductive layer 30L can be formed by depositing at least one conductive material in the remaining portions of the recesses 43 as a continuous material layer. Processing steps of FIG. 9C may be employed to form the continuous electrically conductive layer 30L.

[00119] As shown in FIG. 10D, the continuous electrically conductive layer 30 and the resistive memory material layer 88L can be divided into discrete portions by removing portions that are spaced from the steering elements (83, 85) by the insulating layers 30 employing the same methods as in the processing steps of FIG. 9D. Each remaining discrete portion of the continuous electrically conductive layer 30L constitutes an electrically conductive layer 30. Each remaining discrete portion of the resistive memory material layer 88L constitutes a resistive memory element 88. Dielectric fill material portions 98 can be formed in trenches formed by removal of portions of the continuous electrically conductive layer 30L and the resistive memory material layer 88L.

[00120] Referring to FIGS. 11A-11D, a third exemplary three-dimensional memory device employing an embodiment of the layer stack 80 with local (i.e., discrete) diodes of the present disclosure is illustrated at various stages of a manufacturing process. As shown in FIG. 11A, an alternating stack of insulating layers 60 and doped semiconductor layers 85L of the second conductivity type that alternate along a first direction is formed over a substrate, and is patterned to form sidewalls as in the processing steps of FIG. 9A. The first direction may be a vertical direction that is perpendicular to the substrate as illustrated in FIGS. 2A and 2B, or may be a horizontal direction.

[00121] The doped semiconductor layers 85L include a doped semiconductor material including electrical dopants. The conductivity type of the doped semiconductor layer 85L is a second conductivity type, and as such, the doped semiconductor layers 85L are second

conductivity type semiconductor layers. The second conductivity type may be p-type or n-type. In one embodiment, the second conductivity type can be p-type. In one embodiment, the atomic concentration of the dopants of the second conductivity type can be less than 5.0 x $10^{19}/cm^3$, although greater atomic concentrations can also be employed.

[00122] The alternating stack can be patterned to form sidewalls that extend along the first direction. A combination of lithographic methods and an etch process can be employed to form the sidewalls of the alternating stack. For example, the processing steps of FIGS. 2A and 2B may be employed to form the sidewalls of the alternating stack. In one embodiment, the sidewalls of the alternating stack may be within a same plane (i.e., a two-dimensional Euclidean plane).

[00123] A first conductivity type semiconductor layer 83 can be formed on the sidewalls of the alternating stack (85L, 60) to provide a plurality of discrete p-n junctions that are located within a same plane as sidewalls of the insulating layers 60. The first conductivity type semiconductor layer 83 is a doped semiconductor layer having a doping of a first conductivity type (which is the opposite conductivity type of the second conductivity type). For example, if the first conductivity type is p-type, the second conductivity type is n-type, and vice versa. The direction of the thickness of the first conductivity type semiconductor layer 83 is herein referred to as a second direction. The first conductivity type semiconductor layer 83 extends at least along the first direction, and may extend along a third direction that is perpendicular to the first direction and to the second direction. The extent of the first conductivity type semiconductor layer 83 as deposited may have a greater extent along the first direction than along the second and third directions, thereby rendering the first conductivity type semiconductor layer 83 to be an electrically conductive line 90. Alternatively or additionally, the first conductivity type semiconductor layer 83 can be subsequently patterned such that each remaining portion of the first conductivity type

semiconductor layer 83 extends farther along the first direction than along the second and third directions, thereby rendering each remaining portion of the first conductivity type semiconductor layer 83 to be an electrically conductive line 90. Thus, the electrically conductive line 90 can be formed by depositing a first conductivity type semiconductor layer 83 having a doping of a first conductivity type over the sidewalls of the alternating stack (85L, 60).

[00124] The layer stack 80 employed in the third exemplary three-dimensional memory device can be the same as a modification of the exemplary structure of FIG. 6B in which the first conductivity type semiconductor layer 83 functions as the electrically conductive line 90. Thus, a structure (83/90) that is both an electrically conductive line 90 and a first conductivity type semiconductor layer 83 extends along the first direction over the sidewalls of the alternating stack (85L, 60).

[00125] As shown in FIG. 11B, the doped semiconductor layers 85L can be partially removed through the backside trench selective to the insulating layers 60 by an etch process, which can be an isotropic etch process or an anisotropic etch process. In an illustrative example, the insulating layers 60 can include silicon oxide, the doped semiconductor layers 85L includes a p-doped or n-doped polysilicon material, and the etch process can include a dry etch employing hydrogen chloride, or can be a wet etch process employing KOH. In one embodiment, each doped semiconductor layer 85L can be partially removed to leave an unetched portion, which is herein referred to as a second conductivity type semiconductor layer 85. The thickness of the second conductivity type semiconductor layers 85 along the second direction can be in a range from 5 nm to 30 nm, although lesser and greater thicknesses can also be employed. Each second conductivity type semiconductor layer 85 is self-aligned to a portion of a sidewall of the first conductivity type semiconductor layer 83 located between a neighboring pair of insulating layers 60. Recesses 43 are formed in

volumes from which portions of the doped semiconductor layers 85L are removed. The recesses 43 as initially formed are cavities bounded by surfaces of the insulating layers 60 and physically exposed surfaces of the second conductivity type semiconductor layer 85.

[00126] Alternatively, the doped semiconductor layers 85L may be completely removed, and the second conductivity type semiconductor layers 85 may be formed employing a self-aligned formation method such as gas phase doping or ion implantation on surface portions of the first conductivity type semiconductor layer 83, or by selective deposition of a doped semiconductor material on the physically exposed surfaces of the first conductivity type semiconductor layer 83 on the side of the recesses 43. In one embodiment, selective epitaxy or a selective semiconductor deposition process can be employed for selective deposition of the doped semiconductor material. Electrical dopants of the second conductivity type can be introduced into the second conductivity type semiconductor layers 85 by in-situ doping and/or by gas phase doping.

[00127] A p-n junction that is formed between the first conductivity type semiconductor layer 83 and each of the second conductivity type semiconductor layers 85 constitutes a steering element. In other words, each steering element comprises a discrete p-n junction between the first conductivity type semiconductor layer 83 and a second conductivity type semiconductor layer 85 adjacent to a recess 43 Each of the steering elements comprises a diode.

[00128] In one embodiment, tunneling dielectric elements can be formed by depositing a tunneling dielectric layer 86L within the recesses 43 and directly on surfaces of the insulating layers 60 and directly on surfaces of the steering elements (83, 85). Each tunneling dielectric element can be a portion of the tunneling dielectric layer 86L that is located in proximity to a steering element, i.e., a portion of the p-n junction in proximity to the recesses 43. In one embodiment, the tunneling dielectric layer 86L can include a dielectric material having a

dielectric constant of at least 7.0 (such as silicon nitride or a dielectric metal oxide), and can have a thickness in a range from 0.6 nm to 4 nm.

[00129] Alternatively, tunneling dielectric elements 86 can be formed as discrete dielectric material portions that are self-aligned to portions of the steering elements that are physically exposed to the recesses 43. For example, the tunneling dielectric elements 86 can be formed by a self-aligned formation process such as nitridation of surface portions of the second conductivity type semiconductor layer 85 that are physically exposed to the recesses 43. In one embodiment, each tunneling dielectric element 86 can include a dielectric material having a dielectric constant of at least 7.0 (such as silicon nitride or a dielectric metal oxide), and can have a thickness in a range from 0.6 nm to 4 nm.

[00130] Resistive memory elements are formed as a resistive memory material layer 88L within the recesses 43 and on the tunneling dielectric layer 86L (or on tunneling dielectric elements 86). Processing steps of FIG. 9B may be employed to form the resistive memory material layer 88L.

[00131] As shown in FIG. 11C, a continuous electrically conductive layer 30L can be formed by depositing at least one conductive material in the remaining portions of the recesses 43 as a continuous material layer. Processing steps of FIG. 9C may be employed to form the continuous electrically conductive layer 30L.

[00132] As shown in FIG. 11D, a continuous electrically conductive layer 30 and the resistive memory material layer 88L can be divided into discrete portions by removing portions that are spaced from the steering elements (83, 85) by the insulating layers 60 employing the same methods as in the processing steps of FIG. 9D. Each remaining discrete portion of the continuous electrically conductive layer 30L constitutes an electrically conductive layer 30 (e.g., word line). Each remaining discrete portion of the resistive memory material layer 88L constitutes a resistive memory element 88. Dielectric fill

material portions 98 can be formed in cavities formed by removal of portions of the continuous electrically conductive layer 30L, the resistive memory material layer 88L, and optionally, the tunneling dielectric layer 86L. Layer 83/90 forms a vertical pillar bit line.

[00133] In embodiments illustrated in FIGS. 12A-12C and 13A-13C, an alternating stack of insulating layers 60 and spacer material layers can be formed as an alternating stack of insulating layers 60 and conductive material layers 30 during formation of the exemplary structure of FIGS. 5A – 5C (e.g., at the processing step corresponding to FIGS. 2A and 2B). The conductive material layers 30 are permanent layers that are not removed in subsequent processing steps. For example, the insulating layers 60 can include silicon oxide (such as silicon dioxide, fluorosilicate glass, borosilicate glass, borophosphosilicate glass, phosphosilicate glass, and organosilicate glass). The conductive material layers 30 can include a doped semiconductor material having a doping of a first conductivity type and functioning as first conductivity type semiconductor layers 83 as in the embodiment illustrated in FIG. 12A, or can include a metallic material and/or a doped semiconductor material as in the embodiment illustrated in FIG. 13A.

[00134] Referring to FIG. 12A, a fourth exemplary three-dimensional memory device employing an embodiment of the layer stack 80 of the present disclosure is illustrated at various stages of a manufacturing process. An alternating stack of insulating layers 60 and conductive material layers 30 that alternate along a first direction is formed over a substrate. The substrate can be, for example, the substrate 6 of the exemplary structure of FIGS. 1A and 1B, or can be any other substrate that can provide mechanical support to the alternating stack. The first direction may be a vertical direction that is perpendicular to the substrate as illustrated in FIGS. 2A and 2B, or may be a horizontal direction.

[00135] The conductive material layers 30 include a doped semiconductor material having a doping of a first conductivity type and functioning as first conductivity type semiconductor

layers 83. In other words, a structure (30/83) that functions as a conductive material layer 30 and a first conductivity type semiconductor layer 83 is formed between each neighboring pair of insulating layers 60. The first conductivity type may be p-type or n-type. In one embodiment, the first conductivity type can be n-type (i.e., layer 30/83 is both a word line and the n+ portion of the diode). In one embodiment, the atomic concentration of the dopants of the first conductivity type can be greater than $5.0 \times 10^{19}/cm^3$, although greater atomic concentrations can also be employed.

[00136] The alternating stack can be patterned to form sidewalls that extend along the first direction. A combination of lithographic methods and an etch process can be employed to form the sidewalls of the alternating stack. For example, the processing steps of FIGS. 2A and 2B may be employed to form the sidewalls of the alternating stack. In one embodiment, the sidewalls of the alternating stack may be within a same plane (i.e., a two-dimensional Euclidean plane).

[00137] A layer stack including a continuous doped semiconductor layer 85, a tunneling dielectric layer 86L, and a resistive memory material layer 88L are formed over the sidewalls of the alternating stack (30, 60). The continuous doped semiconductor layer has a doping of a second conductivity type that is the opposite of the first conductivity type, and is herein referred to as a second conductivity type semiconductor layer 85. In one embodiment, the second conductivity type can be p-type. In one embodiment, the atomic concentration of the dopants of the second conductivity type can be less than $5.0 \times 10^{19}/cm^3$, although greater atomic concentrations can also be employed. A plurality of discrete p-n junctions are formed at interfaces between the second conductivity type semiconductor layer 85 and each of the first conductivity type semiconductor layers 83. Each steering element comprises a portion of a p-n junction between the first and second conductivity type semiconductor layers (83, 85). Each of the steering elements comprises a diode.

[00138] The layer stack 80 employed in the fourth exemplary three-dimensional memory device can be the same as a modification of the exemplary structure of FIG. 6A in which the first conductivity type semiconductor layer 83 functions as the electrically conductive layer 30 (e.g., word line). Thus, a structure (83/30) that is both an electrically conductive layer 30 and a first conductivity type semiconductor layer 83 (i.e., both word line and n+ region of the diode) is present between each neighboring pair of insulating layers 60. The second conductivity type semiconductor layer 85 is located over the sidewalls of the alternating stack (30, 60), and can be formed as a planar layer extending over an entirety of the sidewalls of the alternating stack (30, 60) and contacting the entirety of the sidewalls of the alternating stack (30, 60) and having a uniform thickness throughout. Thus, the device includes vertically stacked, horizontally extending n+ layers 30/83 between insulating layers 60 and vertically extending p- layer 85 on the sidewall of the stack to form the local diodes.

[00139] As shown in FIG. 12B, tunneling dielectric elements are formed by depositing a tunneling dielectric layer 86L over the sidewalls of the alternating stack (30, 60) and on the second conductivity type semiconductor layer 85. Each tunneling dielectric element is a portion of the tunneling dielectric layer 86L that is located in proximity to a steering element, i.e., a p-n junction between the second conductivity type semiconductor layer 85 and one of the first conductivity type semiconductor layers 83. In one embodiment, the tunneling dielectric layer 86L can include a dielectric material having a dielectric constant of at least 7.0 (such as silicon nitride or a dielectric metal oxide), and can have a thickness in a range from 0.6 nm to 4 nm. The tunneling dielectric layer 86L can be formed as a planar layer extending over an entirety of the sidewalls of the alternating stack (30, 60) and having a uniform thickness throughout.

[00140] Resistive memory elements are formed as a resistive memory material layer 88L over the sidewalls of the alternating stack (30, 60) and on the tunneling dielectric elements

(as embodied as the tunneling dielectric layer 86L). Each resistive memory element includes a portion of the resistive memory material layer 88L that is proximal to a steering element as embodied as a p-n junction between the second conductivity type semiconductor layer 85 and a first conductivity type semiconductor layer 83. In one embodiment, each of the resistive memory elements comprises a dielectric oxide providing a reduction in resistivity upon formation of conductive filaments therein. The resistive memory material layer 88L can be formed as a planar layer extending over an entirety of the sidewalls of the alternating stack (30, 60) and having a uniform thickness throughout.

[00141] As shown in Fig. 12C, at least one electrically conductive line 90 can be formed on the resistive memory material layer 88L. The electrically conductive line 90 includes at least one metallic material and/or a doped semiconductor material. The at least one metallic material can include an elemental metal, a conductive metallic nitride, a conductive metallic carbide, an intermetallic alloy, and/or a metal-semiconductor alloy.

[00142] The direction perpendicular to the plane of the p-n junctions is herein referred to as a second direction. Each electrically conductive line 90 extends at least along the first direction, and may extend along a third direction that is perpendicular to the first direction and to the second direction. The extent of each electrically conductive line 90 as deposited may have a greater extent along the first direction than along the second and third directions. Alternatively or additionally, the electrically conductive line 90 can be deposited as a conductive material layer, and can be subsequently patterned such that each remaining portion of the electrically conductive line 90 extends farther along the first direction than along the second and third directions (e.g., line 90 forms a vertical bit line pillar).

[00143] Referring to FIGS. 13A-13C, a fifth exemplary three-dimensional memory device employing an embodiment of the layer stack 80 of the present disclosure is illustrated at various stages of a manufacturing process. As shown in FIG. 13A, an alternating stack of

insulating layers 60 and conductive material layers 30 that alternate along a first direction is formed over a substrate. The substrate can be, for example, the substrate 6 of the exemplary structure of FIGS. 1A and 1B, or can be any other substrate that can provide mechanical support to the alternating stack. The first direction may be a vertical direction that is perpendicular to the substrate as illustrated in FIGS. 2A and 2B, or may be a horizontal direction. In one embodiment, the conductive material layers 30 may include at least one metallic material selected from a metal nitride, an elemental metal, and an intermetallic alloy of at least two elemental metals. Alternatively or additionally, the conductive material layers 30 may include a semiconductor material and/or a metal-semiconductor alloy. In other words, the word line 30 is separate from the n+ layer 83 of the diode in this embodiment.

[00144] The alternating stack can be patterned to form sidewalls that extend along the first direction. A combination of lithographic methods and an etch process can be employed to form the sidewalls of the alternating stack. For example, the processing steps of FIGS. 2A and 2B may be employed to form the sidewalls of the alternating stack. In one embodiment, the sidewalls of the alternating stack may be within a same plane (i.e., a two-dimensional Euclidean plane).

[00145] As shown in FIG. 13B, a layer stack including a resistive memory material layer 88L, a tunneling dielectric layer 86L, and a continuous doped semiconductor layer (i.e., a second conductivity type semiconductor layer 85) can be formed over the sidewalls of the alternating stack (30, 60). Each of the resistive memory material layer 88L, the tunneling dielectric layer 86L, and the second conductivity type semiconductor layer 85 can be the same as in the fourth exemplary three-dimensional memory device of FIG. 12B.

[00146] The resistive memory material layer 88L can be located over the sidewalls of the alternating stack (30, 60), and can be formed as a planar layer extending over an entirety of the sidewalls of the alternating stack (30, 60) and contacting the entirety of the sidewalls of

the alternating stack (30, 60) and having a uniform thickness throughout. Each of the tunneling dielectric layer 86L and the second conductivity type semiconductor layer 85 can be formed as a planar layer extending over an entirety of the sidewalls of the alternating stack (30, 60) and having a uniform thickness throughout.

[00147] The second conductivity type semiconductor layer 85 has a doping of the second conductivity type, which may be p-type or n-type. In one embodiment, the second conductivity type can be p-type. In one embodiment, the atomic concentration of the dopants of the second conductivity type can be less than $5.0 \times 10^{19}/cm^3$, although greater atomic concentrations can also be employed.

[00148] As shown in FIG. 13C, a first conductivity type semiconductor layer 83 having a doping of the opposite conductivity type can be formed on the second conductivity type semiconductor layer 85 to provide a continuous p-n junction. The direction of the thickness of the first conductivity type semiconductor layer 83 is herein referred to as a second direction. The first conductivity type semiconductor layer 83 extends at least along the first direction, and may extend along a third direction that is perpendicular to the first direction and to the second direction. The extent of the first conductivity type semiconductor layer 83 as deposited may have a greater extent along the first direction than along the second and third directions, thereby rendering the first conductivity type semiconductor layer 83 to be an electrically conductive line 90 (e.g., line 90 is both a bit line and the n+ layer of the diode). Alternatively or additionally, the first conductivity type semiconductor layer 83 can be subsequently patterned such that each remaining portion of the first conductivity type semiconductor layer 83 extends farther along the first direction than along the second and third directions, thereby rendering each remaining portion of the first conductivity type semiconductor layer 83 to be an electrically conductive line 90. Thus, the electrically conductive line 90 can be formed by depositing a first conductivity type semiconductor layer

83 having a doping of a first conductivity type over the sidewalls of the alternating stack (30, 60).

[00149] The layer stack 80 employed in the fifth exemplary three-dimensional memory device can be the same as a modification of the exemplary structure of FIG. 6B in which the first conductivity type semiconductor layer 83 functions as the electrically conductive line 90. Thus, a structure (83/90) that is both an electrically conductive line 90 and a first conductivity type semiconductor layer 83 extends along the first direction over the sidewalls of the alternating stack (33, 60). The second conductivity type semiconductor layer 85 is interposed between the electrically conductive line 90 and the sidewalls of the alternating stack (30, 60). The electrically conductive line 90 is formed on the second conductivity type semiconductor layer 85.

[00150] Each of the exemplary three-dimensional memory devices described above include an alternating stack of insulating layers 60 and conductive material layers 30 that alternate along a first direction; an electrically conductive line 90 that extend along the first direction and separated from the alternating stack (30, 60) along a second direction; and a plurality of memory elements (85, 86, 88 and optionally 83 if element 83 is separate from the layers 30 or 90) located at each level of the conductive material layers 30. Each memory element (83, 85, 86, 88) includes a steering element (83, 85); a tunneling dielectric element 86 contacting the steering element, wherein a predominant mode of electrical current conduction through the tunneling dielectric element 86 is charge carrier tunneling; and a resistive memory element 88 contacting the tunneling dielectric element 86 and including a dielectric material having multiple states providing different electrical resistance depending on an electrical bias that is previously applied thereto. The steering element (83, 85) can comprise a diode. The tunneling dielectric element 86 can comprise a dielectric material having a dielectric constant of at least 7.0, and can have a thickness in a range from 0.6 nm to

4 nm. Each of the resistive memory elements 88 can comprise a dielectric oxide providing a reduction in resistivity upon formation of conductive filaments therein.

[00151] In some embodiments, the resistive memory elements 88 can include discrete portions of a dielectric metal oxide disposed between neighboring pairs of an insulating layer 60 and an electrically conductive layer 30, and each resistive memory element 88 can include a pair of parallel portions (e.g., horizontal portions that extend perpendicular to the plane of the p-n junction(s)) adjoined by a connecting portion (e.g., a vertical portion that extends parallel to the plane of the p-n junction(s)), and can surround a respective conductive material layer 30 on three sides as illustrated in FIGS. 9D, 10D and 11D. In one embodiment, the tunneling dielectric elements 86 can include discrete portions of a dielectric material having a dielectric constant of at least 7.0, and each tunneling dielectric element 86 can include a pair of parallel (e.g., horizontal) portions adjoined by a connecting (e.g., vertical) portion, and surrounds a respective resistive memory element 88 on three sides as illustrated in FIGS. 9D and 11D. In one embodiment, the tunneling dielectric elements 86 can include discrete portions (e.g., vertical strips or segments) of a dielectric material having a dielectric constant of at least 7.0, and each resistive memory element 86 can be in physical contact with at least one of the insulating layers 60 as illustrated in FIG. 10D.

[00152] In some embodiments, the steering elements (83, 85) in the plurality of memory elements can include portions of a single p-n junction within a layer stack 80 including a p-doped semiconductor layer (e.g., one of the first and second conductivity type semiconductor layers (83, 85)) and an n-doped semiconductor layer (e.g., another of the first and second conductivity type semiconductor layers (83, 85)) such that the portions of the layer stack 80 are spaced from one another along the first direction as illustrated in FIGS. 9D, 10D, and 13C.

[00153] In some embodiments, the steering elements (83, 85) in the plurality of memory

elements can include a plurality of disjoined p-n junctions located at each level of the conductive material layers 30 and spaced from one another along the first direction as illustrated in FIG. 11D (vertical segments or strips 85) and FIG. 12C (horizontal segments 83).

[00154] In some embodiments, the electrically conductive line 90 comprises a doped semiconductor layer having a doping of a first conductivity type, and each steering element in the plurality of memory elements comprise a diode including a portion of the doped semiconductor layer and a plurality of doped semiconductor portions (e.g., portions of the second conductivity type semiconductor layer 85) located at each level of the conductive material layers 30 and having a doping of a second conductivity type that is the opposite of the first conductivity type as illustrated in FIGS. 9D, 10D, 11D and 13C.

[00155] In some embodiments, the resistive memory elements 88 in the plurality of memory elements comprise portions of a continuous vertical dielectric material layer extending along the first direction such that the portions of the dielectric material layer are spaced from one another along the first direction as illustrated in FIGS. 12C and 13C. In some embodiments, the tunneling dielectric elements 86 in the plurality of memory elements comprise portions of a continuous vertical tunneling dielectric layer extending along the first direction such that the portions of the tunneling dielectric layer are spaced along the first direction as illustrated in FIGS. 12C and 13C.

[00156] In some embodiments, the conductive material layers 30 (e.g., word lines) may comprise horizontally extending doped semiconductor layers 83 having a doping of a first conductivity type, and a doped semiconductor line (as embodied as a second conductivity type semiconductor layer 85) extending along the first (vertical) direction and having a doping of a second conductivity type (which is the opposite of the first conductivity type) contacts each of the insulating layers 60 and conductive material layers 30 as illustrated in

FIG. 12C.

[00157] Although the foregoing refers to particular preferred embodiments, it will be understood that the disclosure is not so limited. It will occur to those of ordinary skill in the art that various modifications may be made to the disclosed embodiments and that such modifications are intended to be within the scope of the disclosure. Where an embodiment employing a particular structure and/or configuration is illustrated in the present disclosure, it is understood that the present disclosure may be practiced with any other compatible structures and/or configurations that are functionally equivalent provided that such substitutions are not explicitly forbidden or otherwise known to be impossible to one of ordinary skill in the art. All of the publications, patent applications and patents cited herein are incorporated herein by reference in their entirety.

WHAT IS CLAIMED IS:

1. A memory device comprising at least one memory cell, the at least one memory cell comprising:

a steering element;

a resistive memory element; and

a tunneling dielectric element located between the steering element and the resistive memory element.

2. The memory device of Claim 1, wherein:

the steering element comprises a diode;

a predominant mode of electrical current conduction through the tunneling dielectric element is charge carrier tunneling; and

the resistive memory element has multiple states providing different electrical resistance depending on an electrical bias that is previously applied thereto.

3. The memory device of Claim 2, wherein the diode comprises:

an n-doped semiconductor region including n-type dopants at an atomic concentration greater than $5.0 \times 10^{19}/cm^3$; and

a p-doped semiconductor region including p-type dopants at an atomic concentration less than $5.0 \times 10^{19}/cm^3$.

4. The memory device of Claim 3, wherein the tunneling dielectric element contacts the p-doped semiconductor region of the diode.

5. The memory device of Claim 4, wherein during an application of a reverse bias to the memory cell, holes accumulate in the p-type semiconductor region of the diode adjacent to the tunneling dielectric element to facilitate electron tunneling from the resistive memory element to the n-type semiconductor region of the diode through the tunneling dielectric element and the p-type semiconductor region of the diode.

6. The memory device of Claim 1, wherein the tunneling dielectric element comprises a dielectric material having a dielectric constant of at least 7.0 and the resistive memory element comprises a dielectric oxide providing a reduction in resistivity upon formation of conductive filaments therein.

7. The memory device of Claim 6, wherein the tunneling dielectric element comprises a dielectric material selected from silicon nitride and aluminum oxide which does not form conductive filaments therein upon application of a bias thereto.

8. The memory device of Claim 1, wherein the tunneling dielectric element has a thickness in a range from 0.6 nm to 4 nm.

9. The memory device of Claim 1, wherein the resistive memory element comprises a dielectric oxide of a metal selected from Hf, Ti, Zr, and Ta.

10. The memory device of Claim 1, further comprising:

one of a word line or a bit line in contact with the steering element; and

another one of the word line or the bit line in contact with the resistive memory element.

11. The memory device of Claim 10, further comprising a substrate and an alternating stack of insulating layers and conductive material layers comprising the word lines that alternate along a first direction which is perpendicular to a top surface of the substrate.

12. The memory device of Claim 11, wherein:

the bit line extends along the first direction and is separated from the alternating stack along a second direction; and

a plurality of the memory elements are located at each level of the word lines.

13. The memory device of Claim 12, wherein:

the resistive memory elements in the respective memory elements comprise discrete portions of a dielectric metal oxide disposed between neighboring pairs of the insulating layer and the word line; and

each resistive memory element comprises a pair of parallel portions adjoined by a connecting portion which surround the word line on three sides.

14. The memory device of Claim 13, wherein:

the tunneling dielectric elements comprise discrete portions of a dielectric material having a dielectric constant of at least 7.0; and

each tunneling dielectric element comprises a pair of parallel portions adjoined by a connecting portion, which surround the resistive memory element and the word line on three sides.

15. The memory device of Claim 12, wherein the steering elements in the plurality of memory elements comprise portions of a single p-n junction within a layer stack including a p-doped semiconductor layer and an n-doped semiconductor layer, the portions of the layer stack being spaced from one another along the first direction.

16. The memory device of Claim 12, wherein the steering elements in the plurality of memory elements comprise a plurality of discrete p-n junctions located at each level of the word lines and spaced from one another along the first direction.

17. The memory device of Claim 12, wherein:

the bit line comprises a doped semiconductor layer having a doping of a first conductivity type; and

each steering element in the plurality of memory elements comprise a diode including a portion of the doped semiconductor layer and a plurality of doped semiconductor portions located at each level of the word lines and having a doping of a second conductivity type that is the opposite of the first conductivity type.

18. The memory device of Claim 12, wherein:

the resistive memory elements in the plurality of memory elements comprise portions of a dielectric material layer extending along the first direction, the portions of the dielectric material layer being spaced from one another along the first direction; and

the tunneling dielectric elements in the plurality of memory elements comprise portions of a tunneling dielectric layer extending along the first direction, the portions of the tunneling dielectric layer being spaced along the first direction.

19. The memory device of Claim 18, wherein:

the word lines comprise doped semiconductor layers having a doping of a first conductivity type; and

a doped semiconductor material layer extending along the first direction and having a doping of a second conductivity type that is the opposite of the first conductivity type contacts each of the insulating layers and word lines.

20. The memory device of Claim 12, wherein:

the steering element comprises a diode;

the tunneling dielectric element comprises a dielectric material having a dielectric constant of at least 7.0;

the tunneling dielectric element has a thickness in a range from 0.6 nm to 4 nm; and

each of the resistive memory elements comprises a dielectric oxide providing a reduction in resistivity upon formation of conductive filaments therein.

21. A method of fabricating a memory device, comprising:

forming an alternating stack of insulating layers and sacrificial material layers that alternate along a first direction over a substrate;

patterning the alternating stack to form sidewalls that extend along the first direction;

forming an electrically conductive line extending along the first direction over the sidewalls of the alternating stack;

forming recesses by removing the sacrificial material layers selective to the insulating layers;

forming memory cells arranged along the first direction, wherein each of the memory comprises a resistive memory element, and wherein at least one element of each memory cell is formed within a respective recess; and

forming electrically conductive layers within each recess.

22. The method of Claim 21, further comprising:

a steering element located in each of the memory cells; and

a tunneling dielectric element located between the steering element and the resistive memory element in each of the memory cells.

23. The method of Claim 22, wherein the electrically conductive line is formed by depositing a first conductivity type semiconductor layer having a doping of a first conductivity type over the sidewalls of the alternating stack.

24. The method of Claim 23, further comprising forming a second conductivity type semiconductor layer over the sidewalls of the alternating stack, wherein:

the electrically conductive line is formed on the second conductivity type semiconductor layer; and

the steering elements comprise portions of a continuous p-n junction between the first and second conductivity type semiconductor layers.

25. The method of Claim 23, further comprising forming a plurality of second conductivity type semiconductor portions on each surface of the first conductivity type semiconductor layer that are physically exposed to the recesses, wherein:

the first conductivity type semiconductor layer is formed directly on sidewalls of the insulating layers; and

the steering elements comprise discrete p-n junctions that are spaced from one another.

26. The method of Claim 22, wherein the tunneling dielectric elements are formed by depositing a tunneling dielectric layer within the recesses and directly on surfaces of the insulating layers and directly on surfaces of the steering elements, wherein each tunneling dielectric element is a portion of the tunneling dielectric layer.

27. The method of Claim 22, wherein the tunneling dielectric elements are formed as discrete dielectric material portions that are self-aligned to portions of the steering elements that are physically exposed to the recesses.

28. The method of Claim 22, further comprising:

forming a resistive memory material layer within the recesses and on the tunneling dielectric elements; and

dividing the resistive memory material layer into discrete resistive memory elements by removing portions of the resistive memory material layer that extend along the first direction and spaced from the steering elements by the insulating layers.

29. The method of Claim 22, wherein:

the electrically conductive layers comprise horizontal word lines extending parallel to a top surface of the substrate;

electrically conductive line comprises a vertical bit line which extends perpendicular to the top surface of the substrate;

each of the resistive memory elements comprises a dielectric oxide providing a reduction in resistivity upon formation of conductive filaments therein;

each of the steering elements comprises a diode;

the tunneling dielectric elements comprise a dielectric material having a dielectric constant of at least 7.0; and

each of the tunneling dielectric elements has a thickness in a range from 0.6 nm to 4 nm.

30. A method of fabricating a memory device, comprising:

forming an alternating stack of insulating layers and conductive material layers that alternate along a first direction over a substrate;

patterning the alternating stack to provide sidewalls of the alternating stack;

forming a layer stack including a continuous doped semiconductor layer, a tunneling dielectric layer, and a resistive memory material layer over the sidewalls of the alternating stack; and

forming an electrically conductive line on the layer stack.

31. The method of Claim 30, wherein:

memory elements arranged along the first direction are formed, wherein each of the memory elements comprises a respective p-n junction, a portion of the tunneling dielectric layer, and a portion of the resistive memory material layer; and

each of the p-n junctions includes an interface region between the continuous doped semiconductor layer and an element selected from the electrically conductive line and the conductive material layers.

32. The method of Claim 31, wherein each of the continuous doped semiconductor layer, the tunneling dielectric layer, and the resistive memory material layer is formed as a planar layer extending over an entirety of the sidewalls of the alternating stack and having a uniform thickness.

33. The method of Claim 31, wherein:

the conductive material layers comprise a doped semiconductor material having a doping of an opposite conductivity type than a conductivity type of the continuous doped semiconductor layer; and

the p-n junctions extend along the first direction.

34. The method of Claim 33, wherein the doped semiconductor layer is formed directly on the sidewalls of the alternating stack.

35. The method of Claim 33, wherein the electrically conductive line comprises a doped semiconductor material having a doping of an opposite conductivity type than a conductivity type of the continuous doped semiconductor layer, and the p-n junctions extend along the first direction.

36. The method of Claim 35, wherein:

the conductive material layers comprise at least one metallic material selected from a metal nitride, an elemental metal, and an intermetallic alloy of at least two elemental metals; and

the resistive memory material layer is formed directly on the sidewalls of the alternating stack.

37. The method of Claim 33, wherein:

each of the resistive memory elements comprises a dielectric oxide providing a reduction in resistivity upon formation of conductive filaments therein;

each of the steering elements comprises a diode;

the tunneling dielectric elements comprise a dielectric material having a dielectric constant of at least 7.0; and

each of the tunneling dielectric elements has a thickness in a range from 0.6 nm to 4 nm.

38. A method of operating the memory device of Claim 4, comprising applying a reverse bias to the memory cell, such that holes accumulate in the p-type semiconductor region of the diode adjacent to the tunneling dielectric element to facilitate electron tunneling from the resistive memory element to the n-type semiconductor region of the diode through the tunneling dielectric element and the p-type semiconductor region of the diode.

39. A method of making a memory device, comprising:

determining a desired current-voltage performance characteristic of the device;

selecting at least one of a thickness and p-type doping concentration of a p-type semiconductor layer of a diode steering element which provides the desired current-voltage performance characteristic;

forming the diode steering element which comprises an n-type semiconductor layer and a p-type semiconductor layer having the selected at least one of thickness and doping concentration;

forming a resistive memory element; and

forming a tunneling dielectric element located between the diode steering element and the resistive memory element.

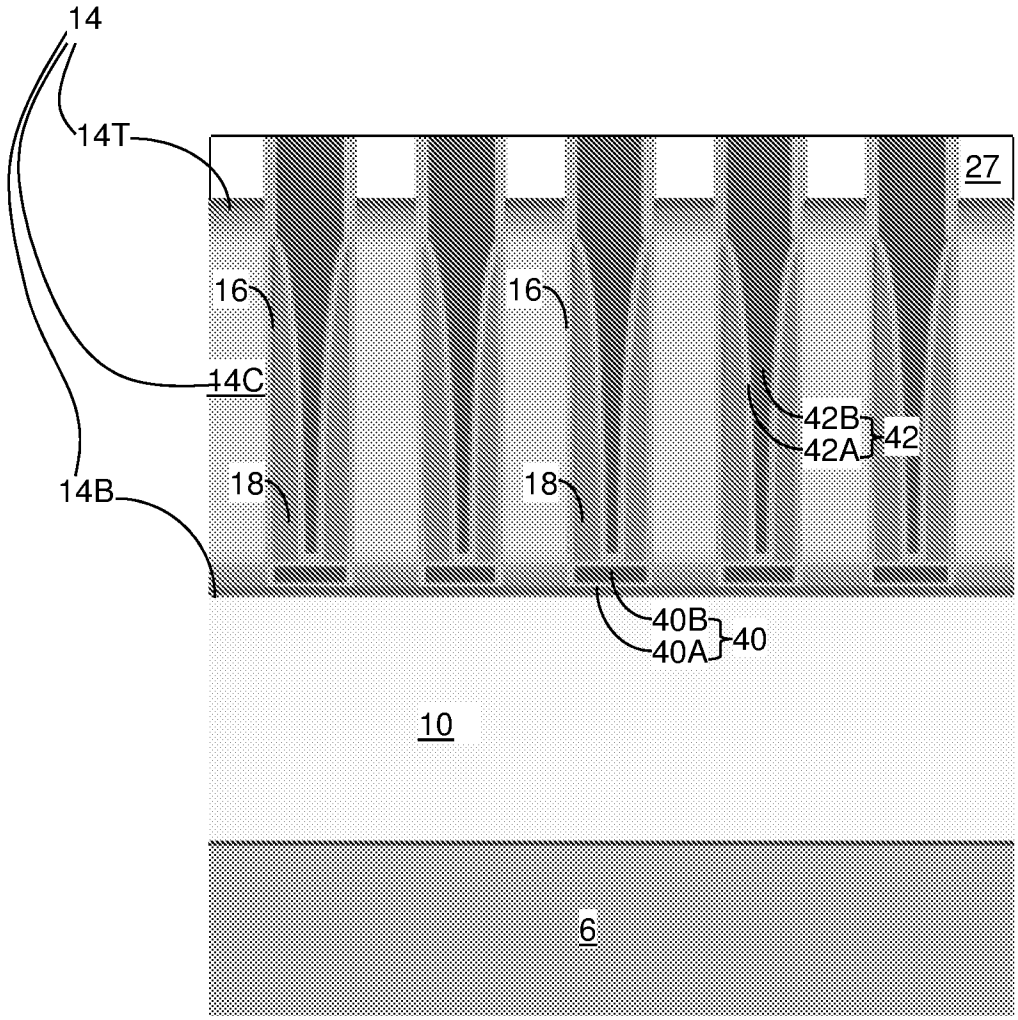


FIG. 1A

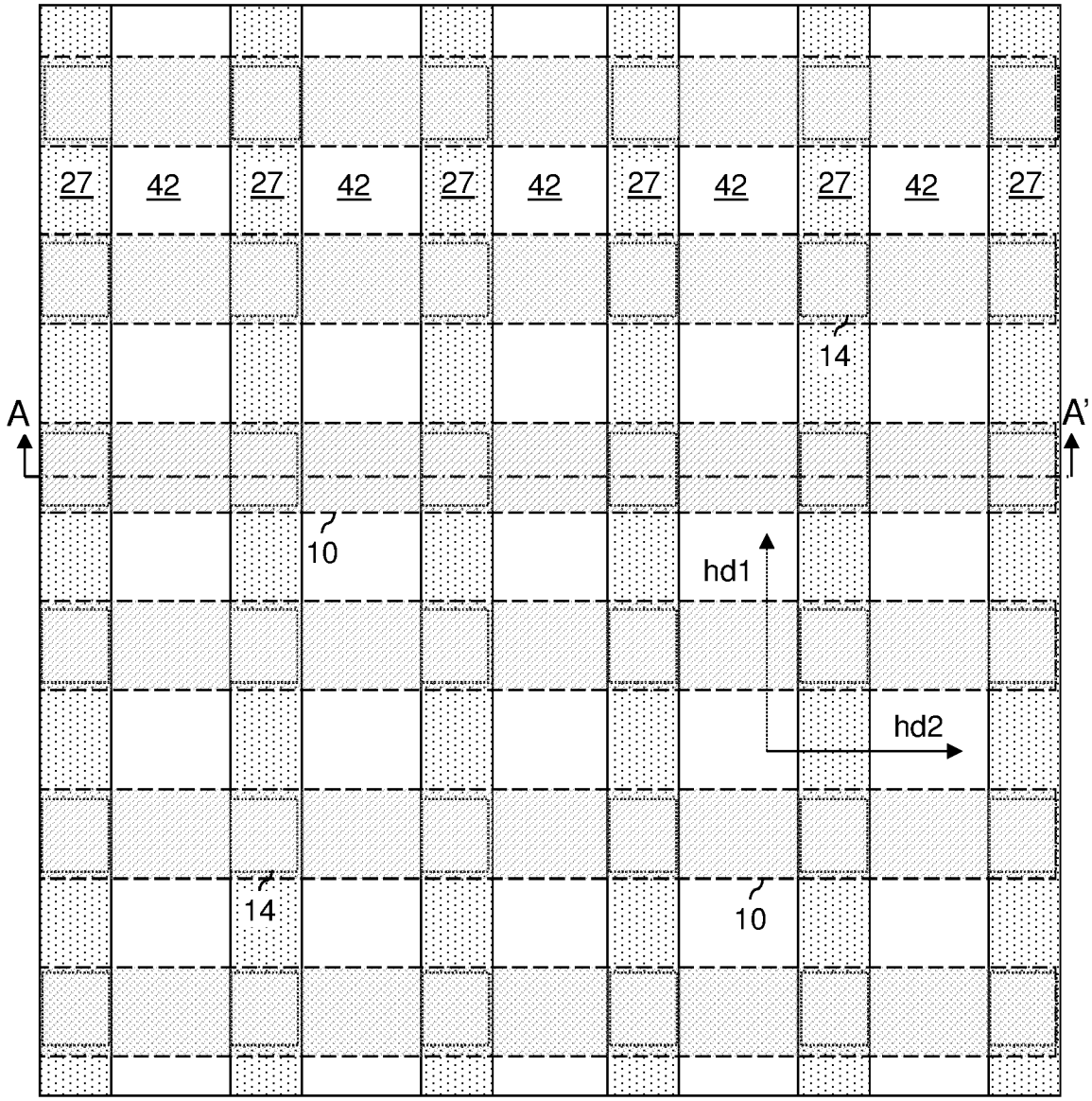


FIG. 1B

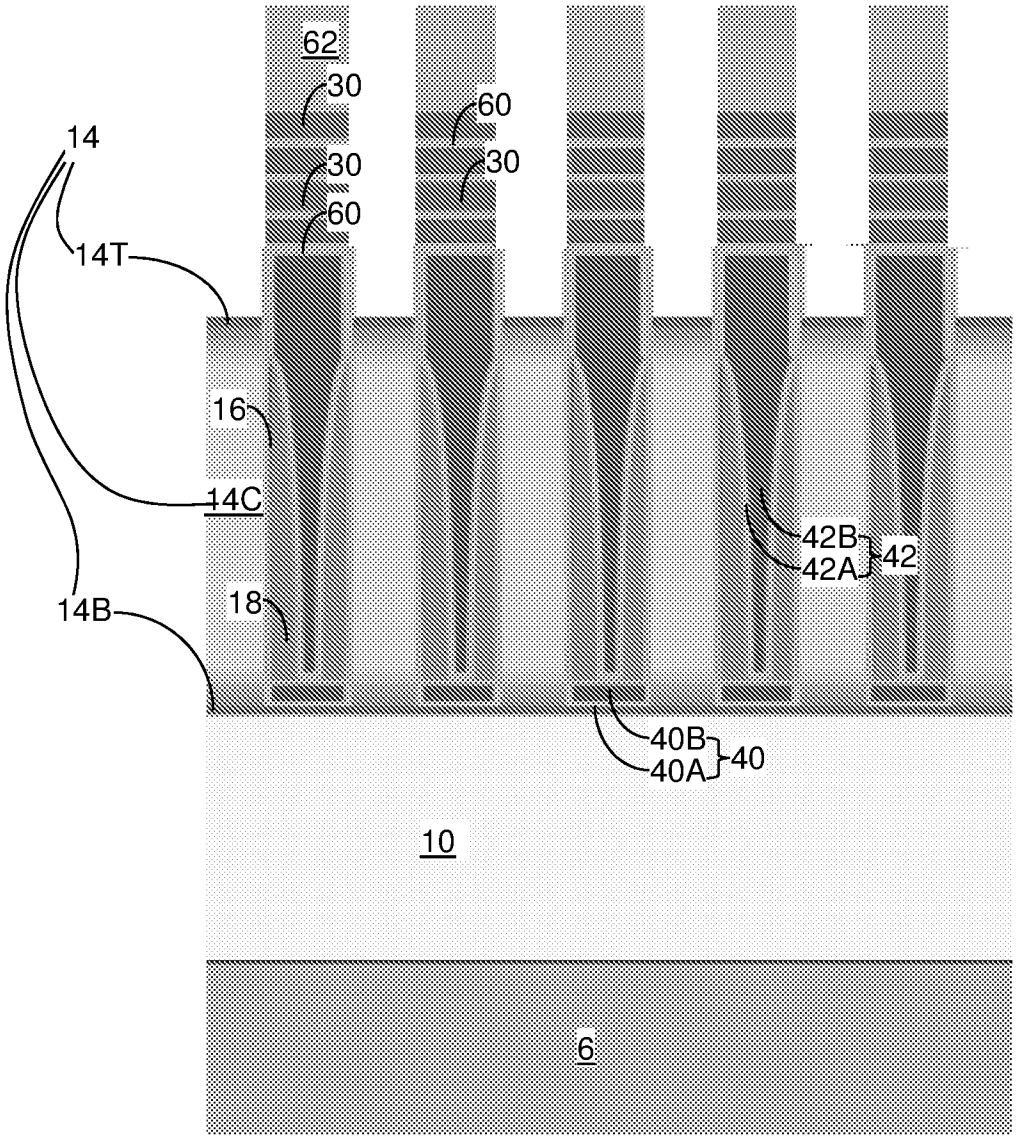


FIG. 2A

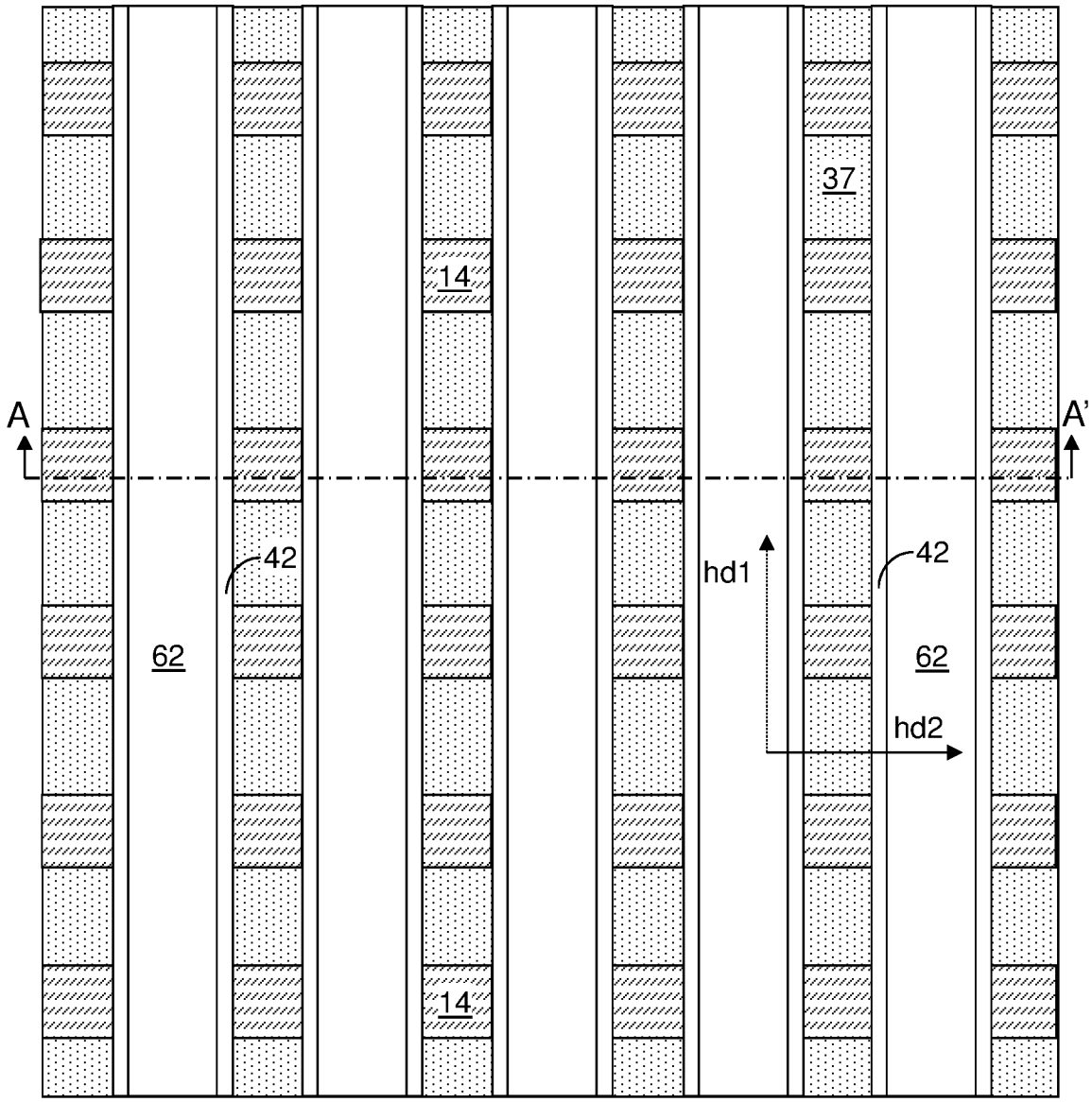


FIG. 2B

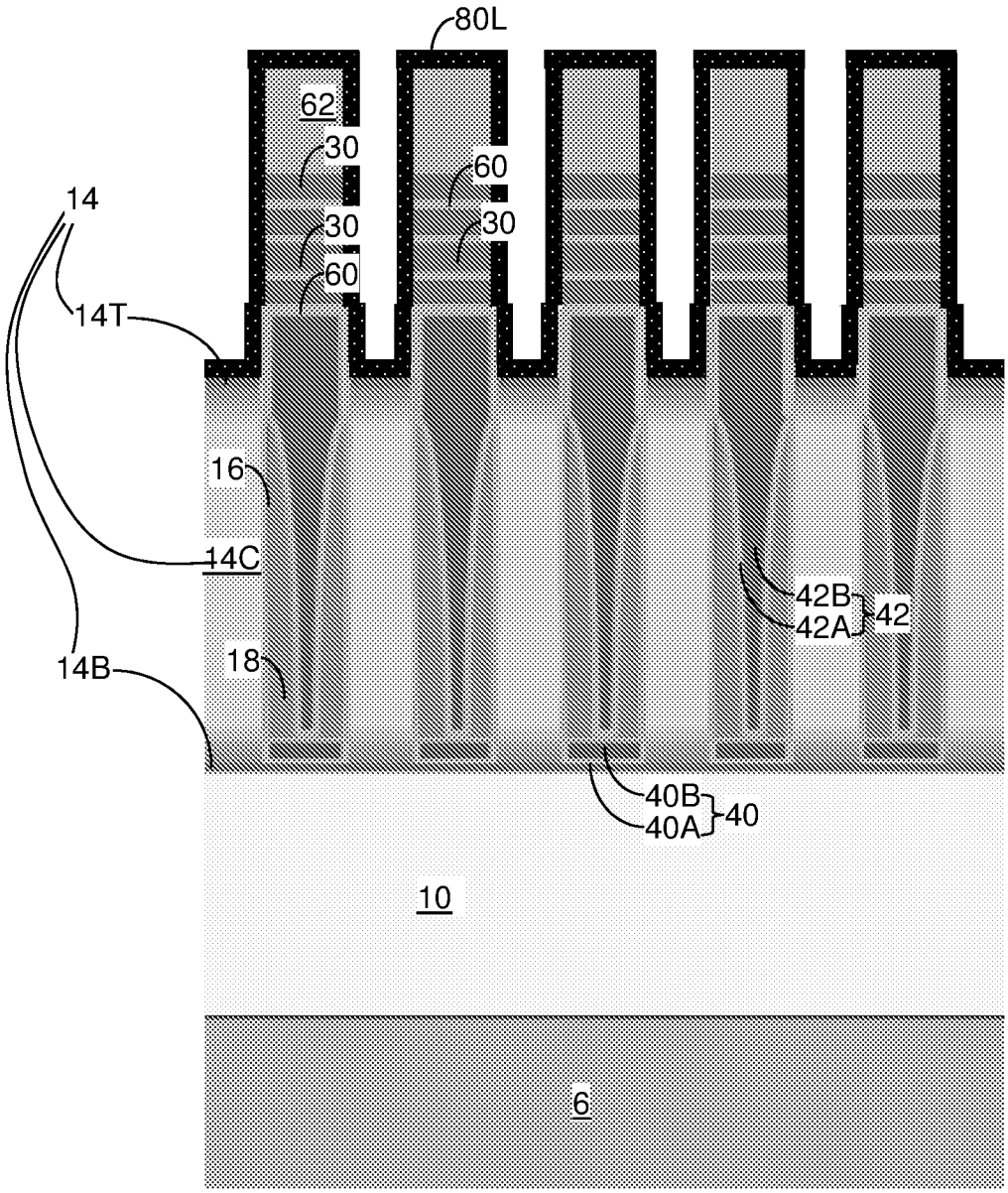


FIG. 3

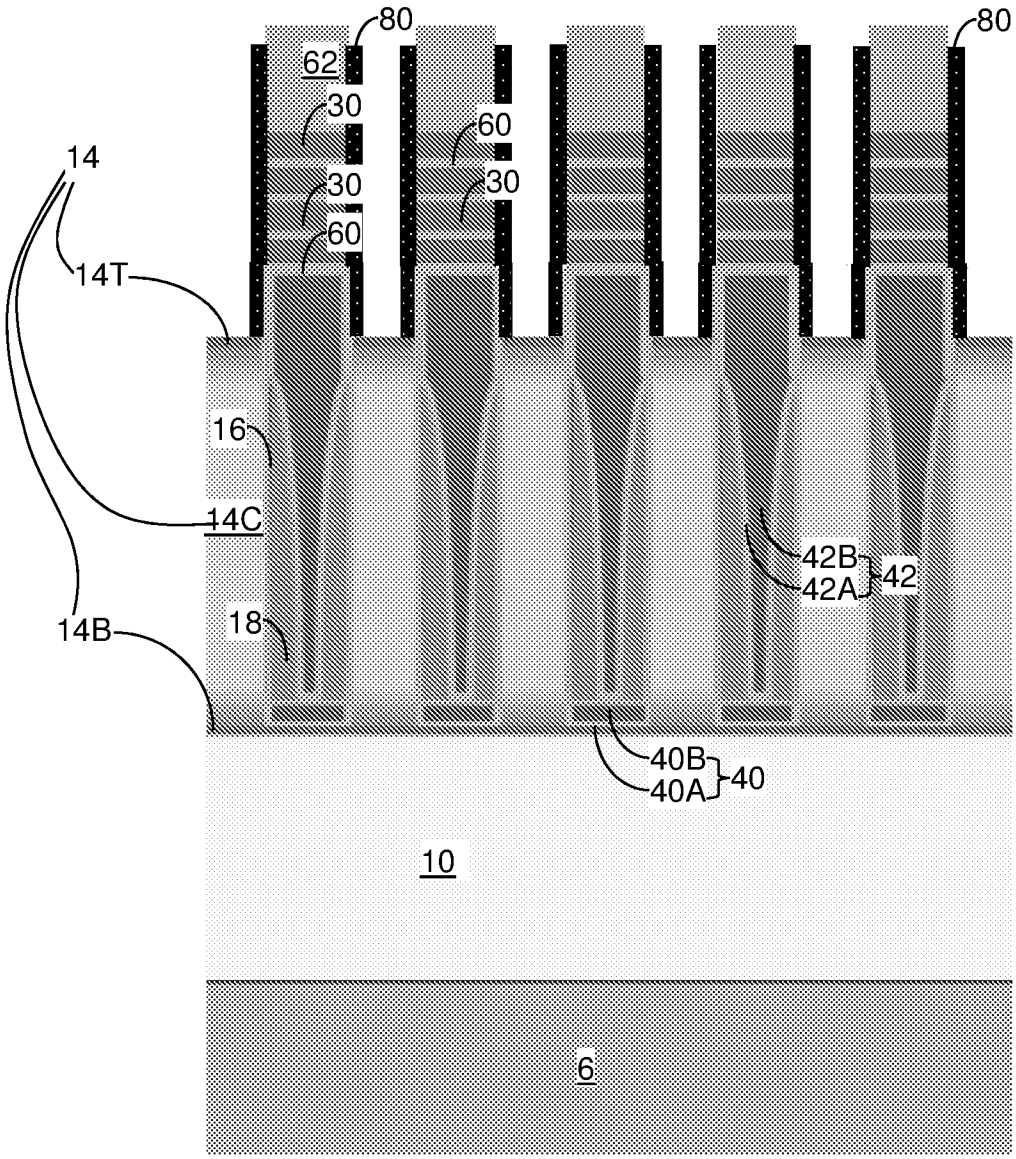

80
80
62
30
60
14
30
30
60
14T
16
14C
42B
42A
42
18
14B
40B
40A
40
10
6

FIG. 4A

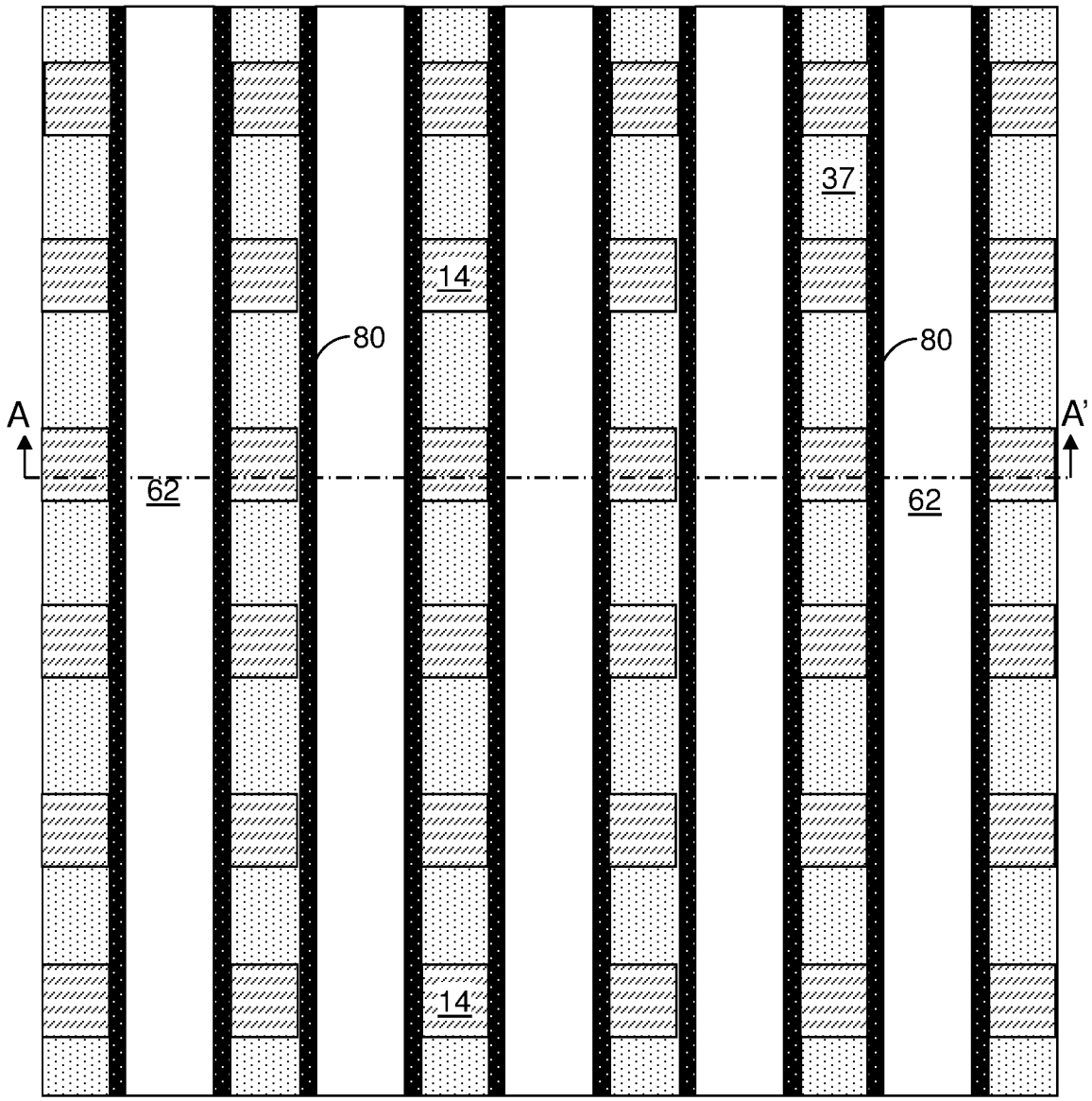


FIG. 4B

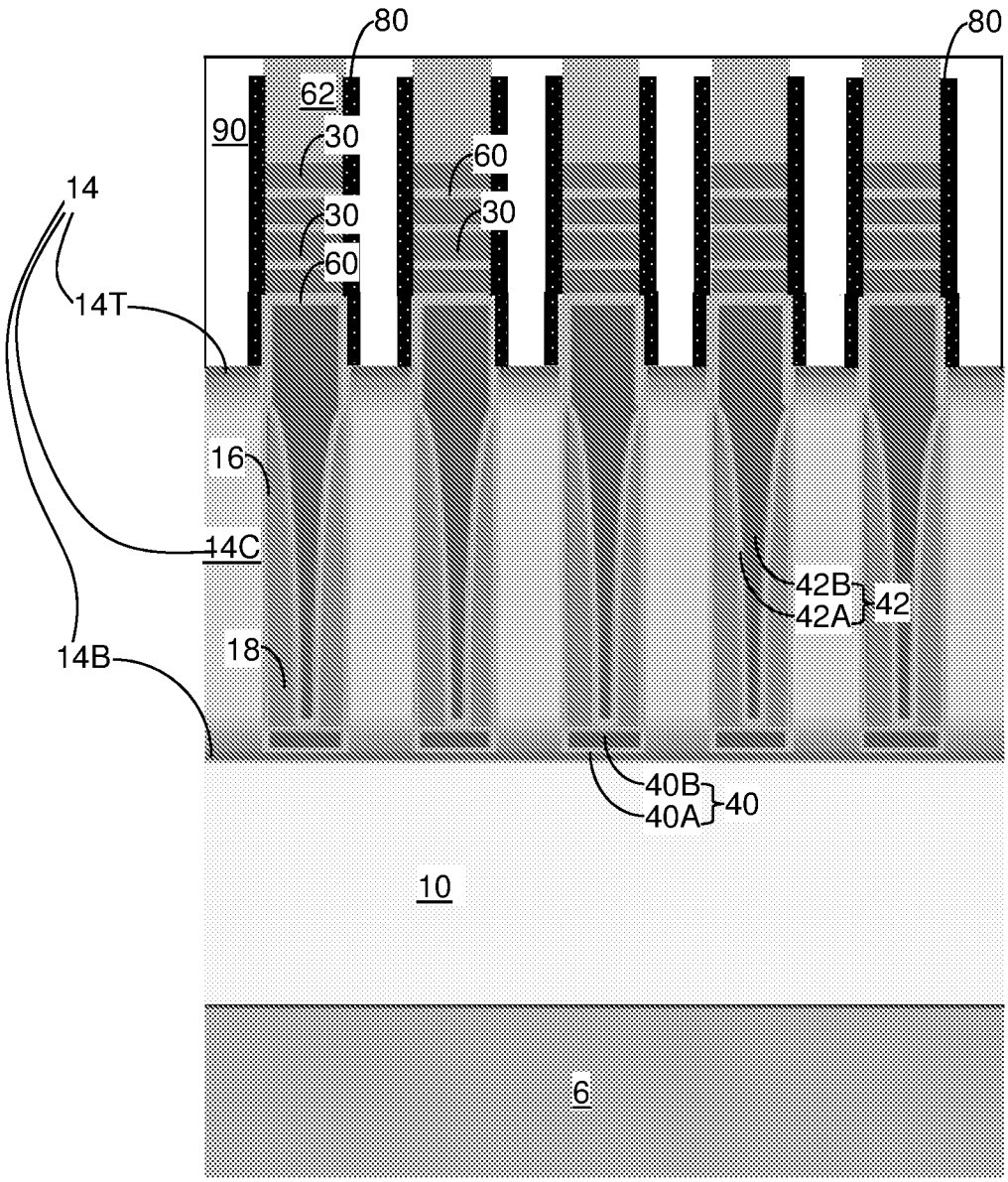

80
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62
90
30
60
14
30
30
60
14T
16
14C
42B
42A
42
18
14B
40B
40A
40
10
6

FIG. 5A

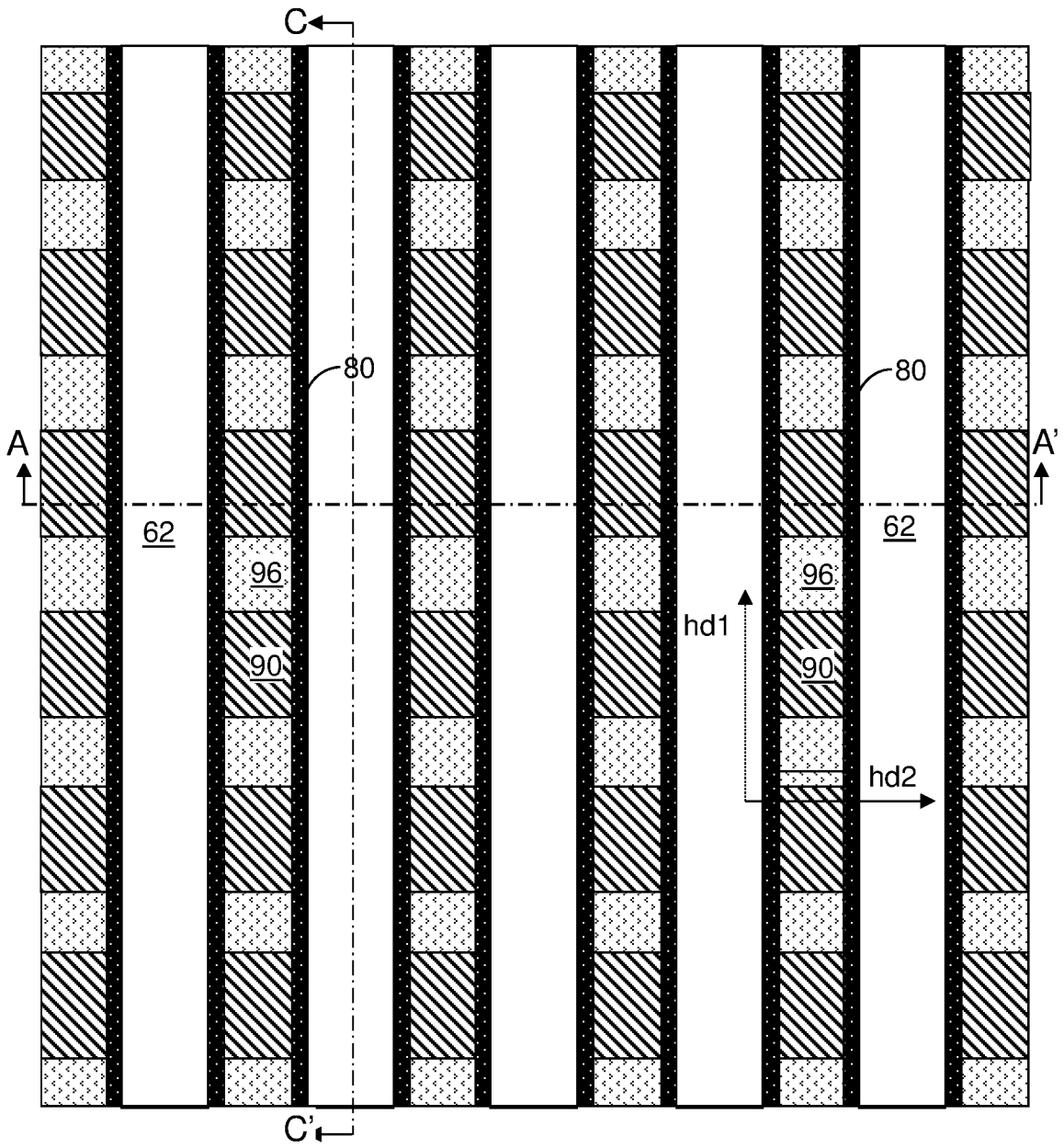


FIG. 5B

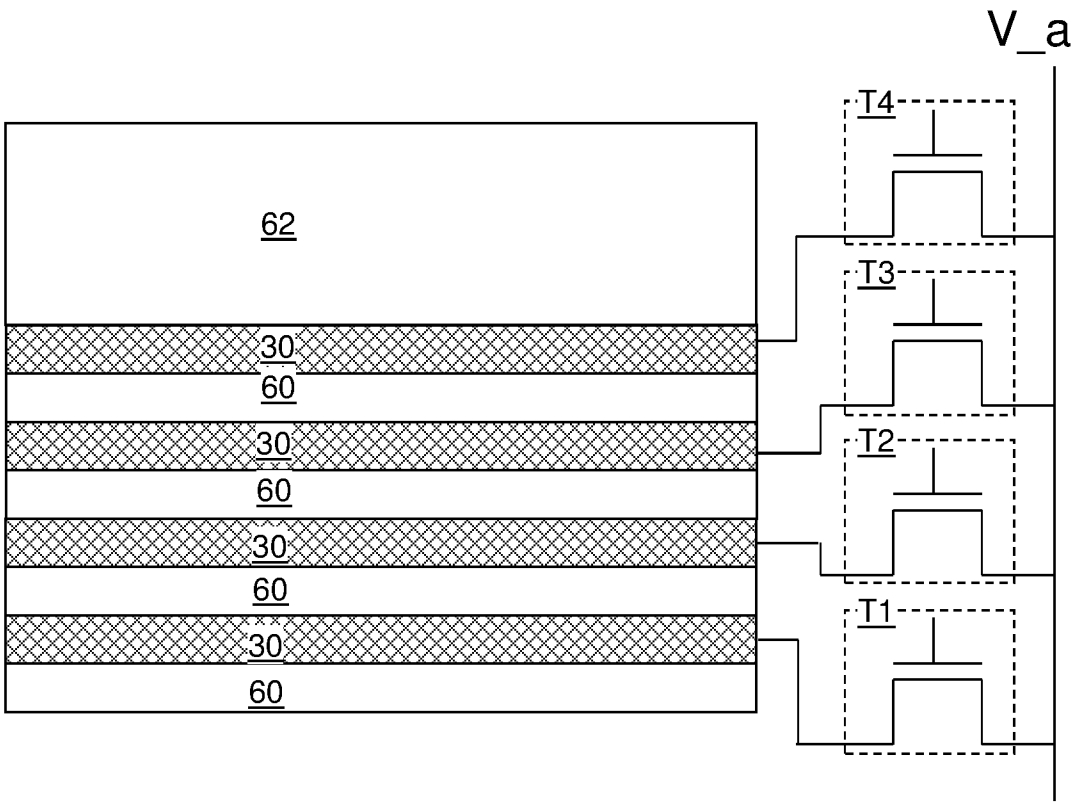


FIG. 5C

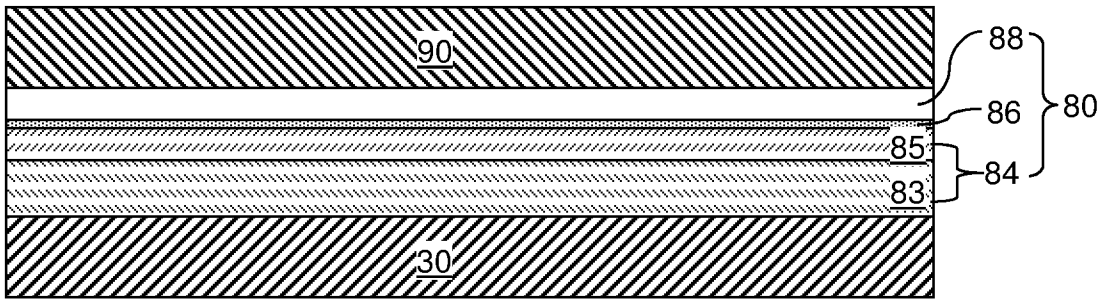


FIG. 6A

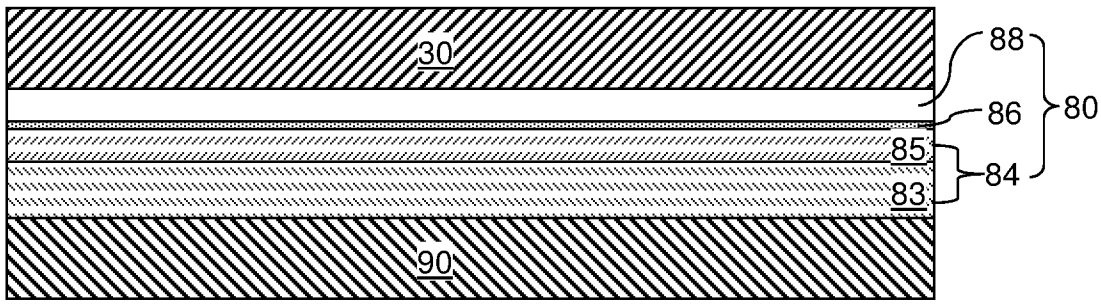


FIG. 6B

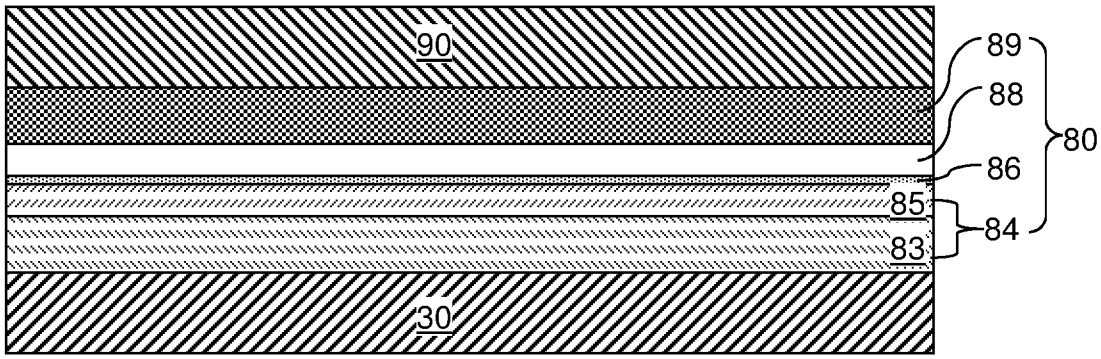


FIG. 6C

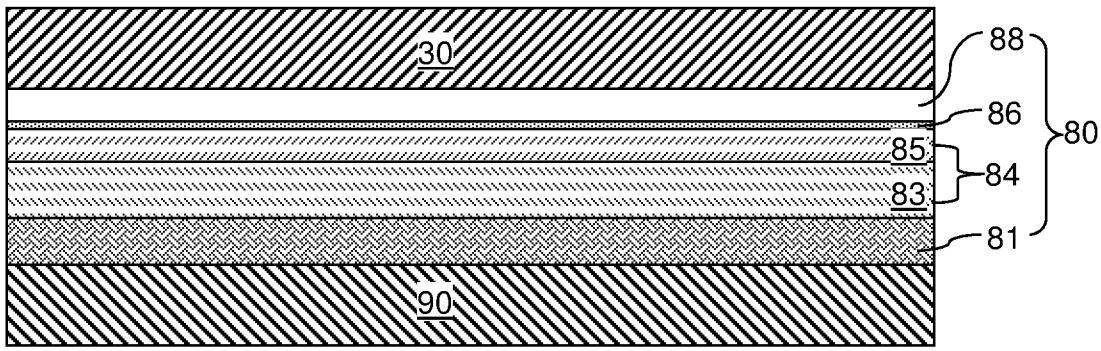


FIG. 6D

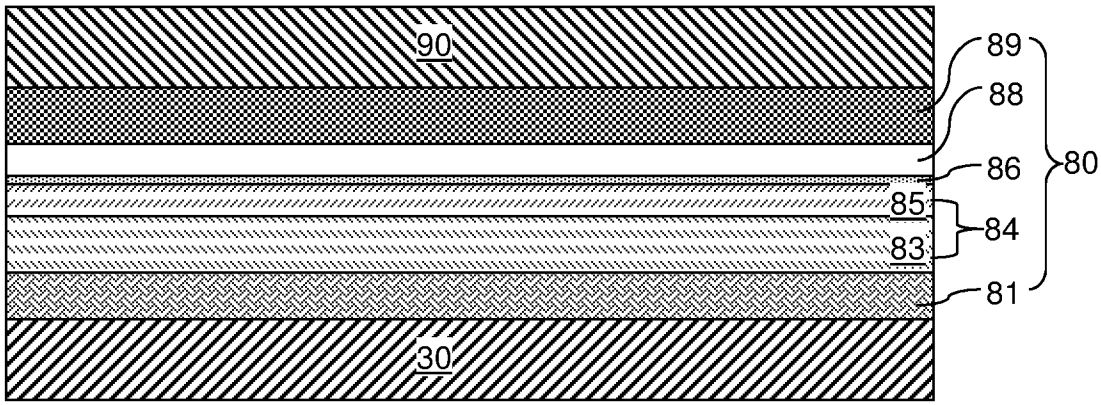


FIG. 6E

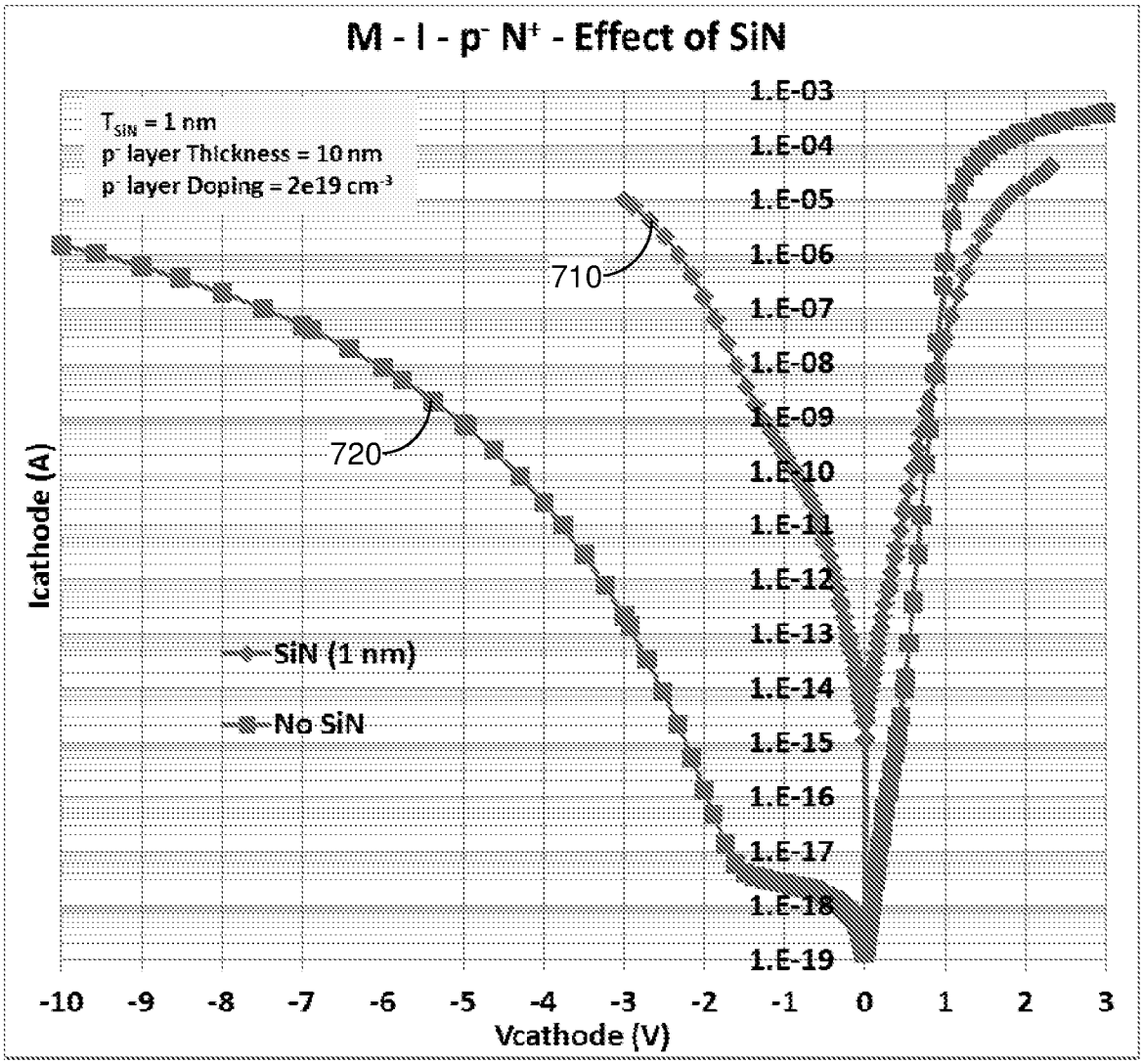

M - I - p⁻ N⁺ - Effect of SiN
T_SiN = 1 nm
p⁻ layer Thickness = 10 nm
p⁻ layer Doping = 2e19 cm⁻³
710
720
SiN (1 nm)
No SiN
Icathode (A)
1.E-03
1.E-04
1.E-05
1.E-06
1.E-07
1.E-08
1.E-09
1.E-10
1.E-11
1.E-12
1.E-13
1.E-14
1.E-15
1.E-16
1.E-17
1.E-18
1.E-19
-10 -9 -8 -7 -6 -5 -4 -3 -2 -1 0 1 2 3
Vcathode (V)

FIG. 7A

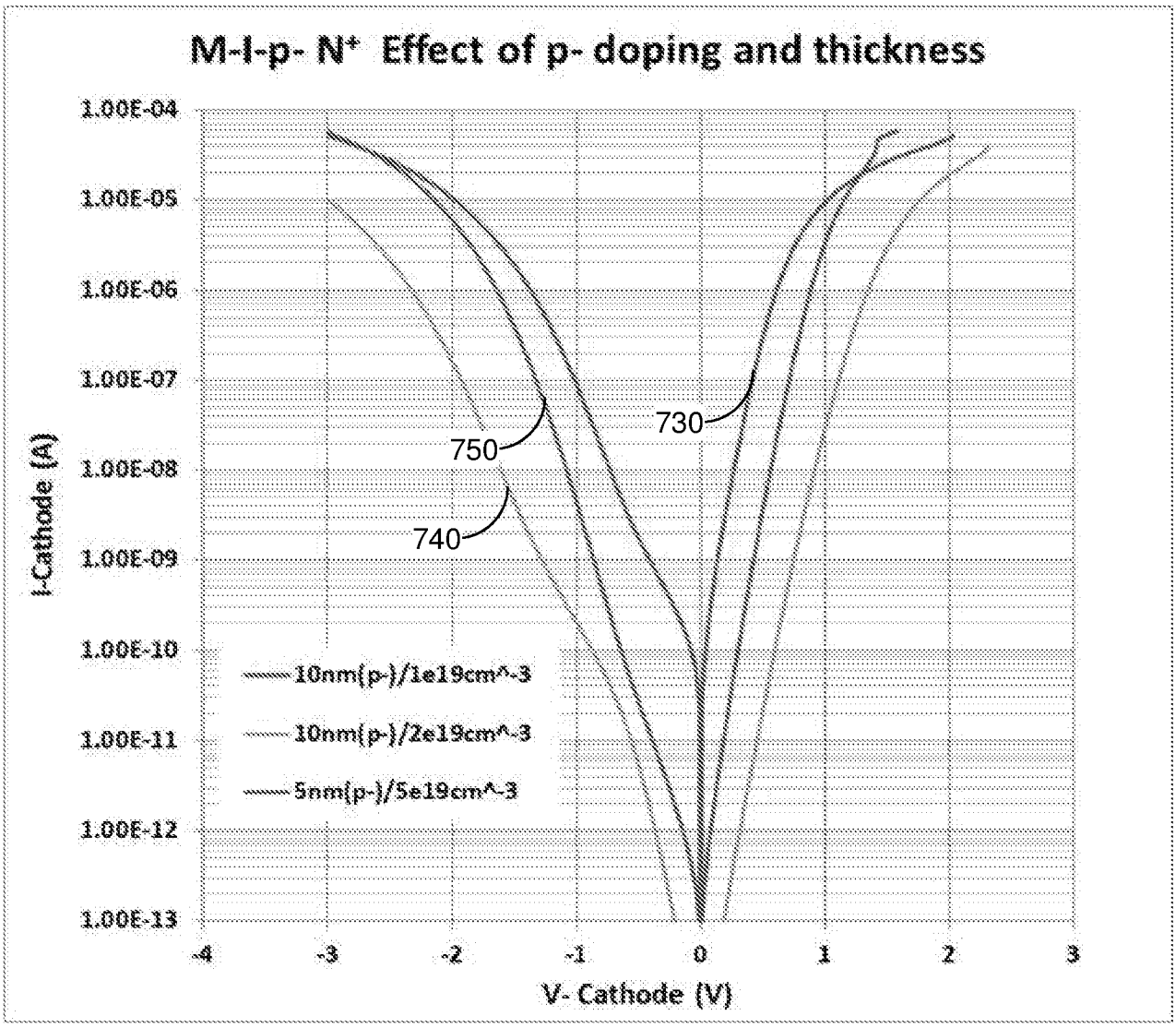

M-I-p- N+ Effect of p- doping and thickness
I-Cathode (A)
1.00E-04
1.00E-05
1.00E-06
1.00E-07
1.00E-08
1.00E-09
1.00E-10
1.00E-11
1.00E-12
1.00E-13
-4
-3
-2
-1
0
1
2
3
V- Cathode (V)
730
750
740
10nm(p-)/1e19cm^-3
10nm(p-)/2e19cm^-3
5nm(p-)/5e19cm^-3

FIG. 7B

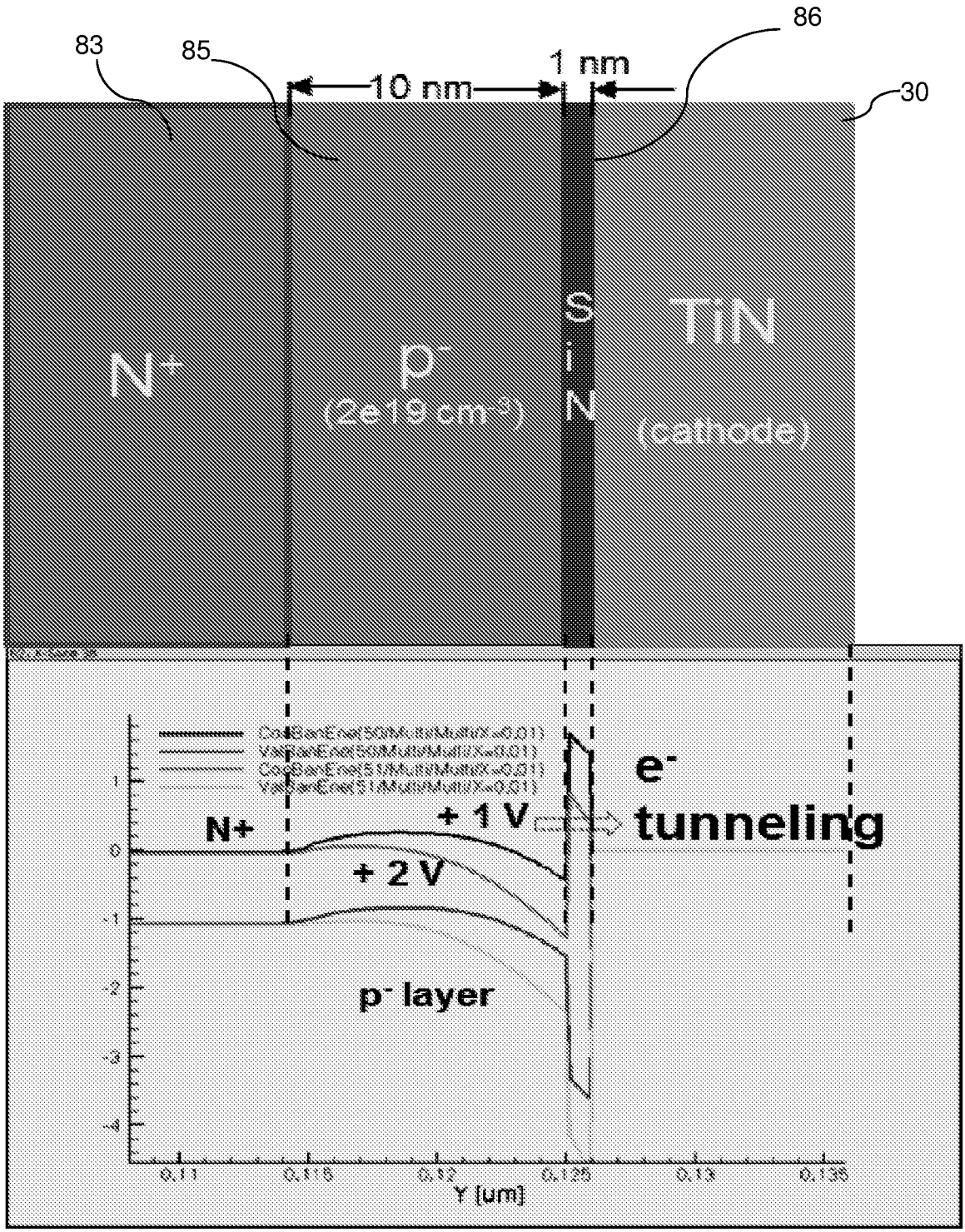

83
85
86
10 nm
1 nm
30
N+
P-
(2e19 cm-3)
Si
N
TiN
(cathode)
N+
+ 1 V
+ 2 V
p- layer
e-
tunneling
Y [um]

FIG. 8A

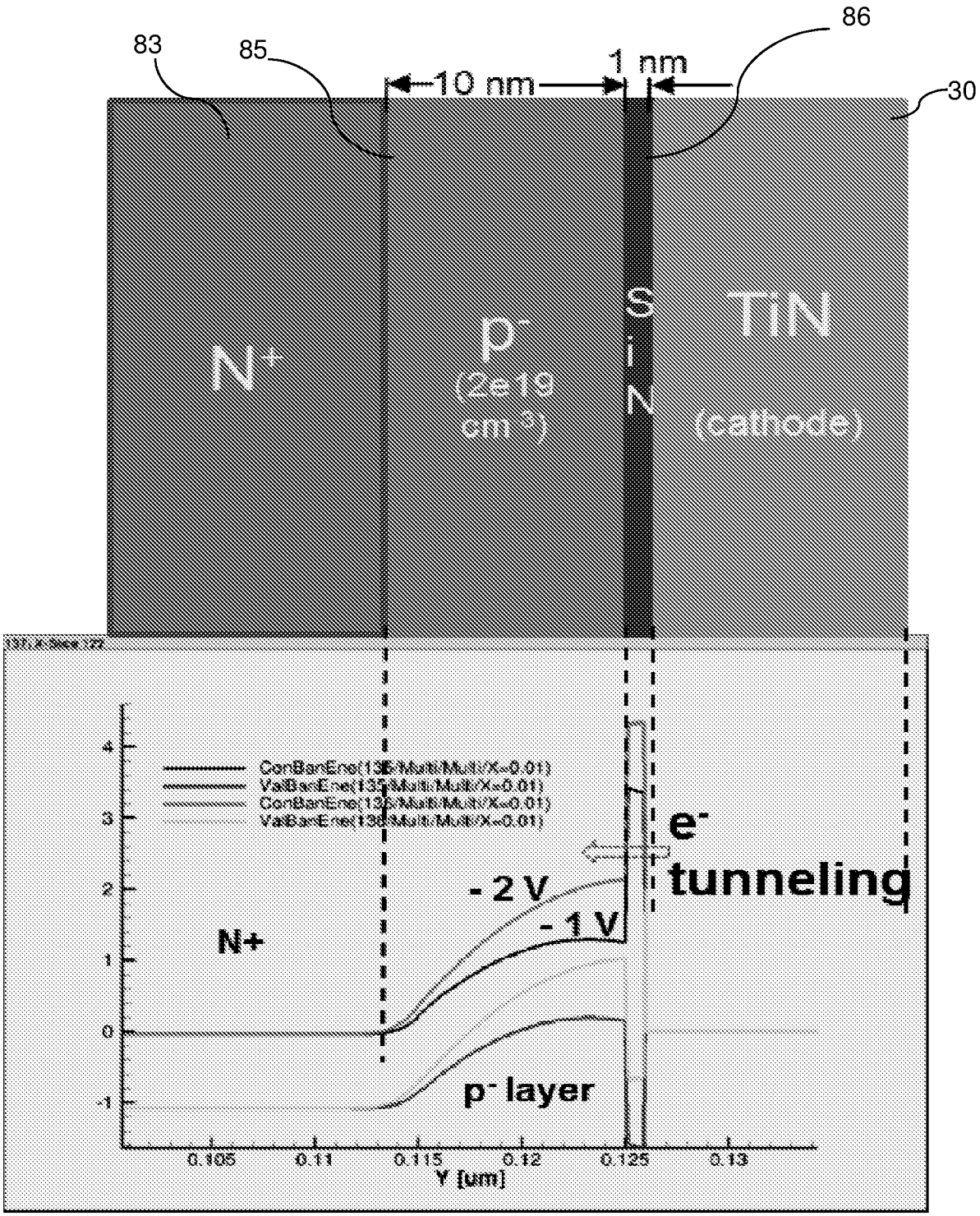

83
85
86
10 nm
1 nm
30
N+
p-
(2e19
cm-3)
Si
N
TiN
(cathode)
e-
tunneling
- 2 V
- 1 V
N+
p- layer
Y [um]

FIG. 8B

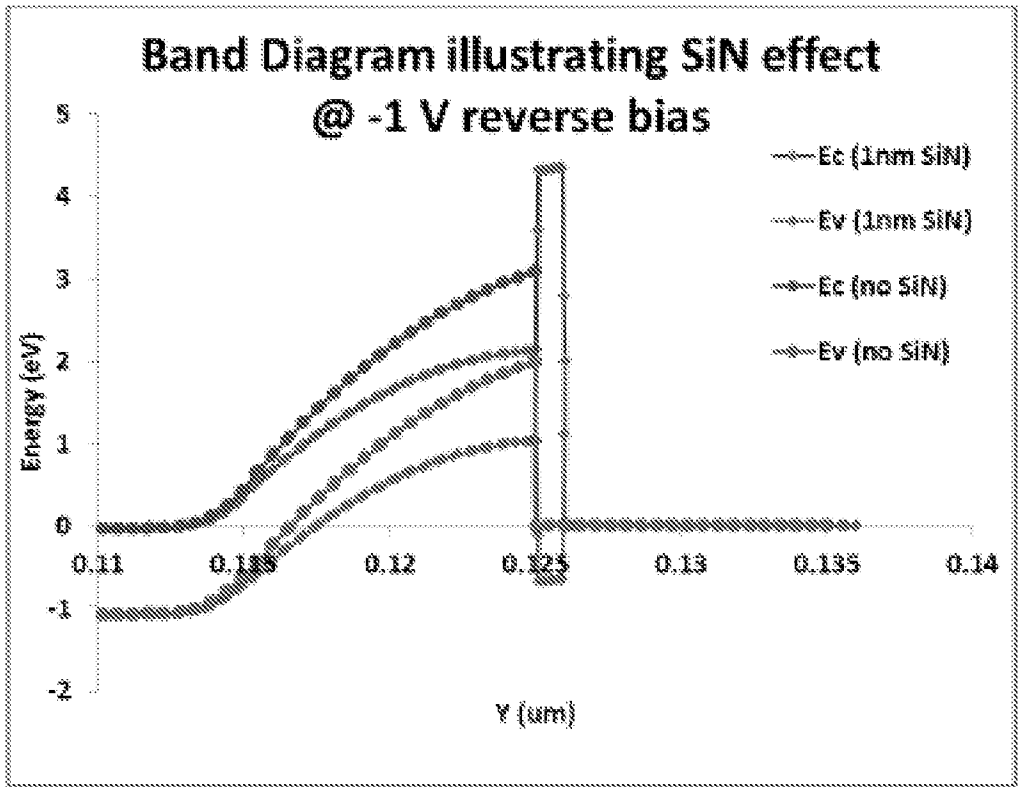

Band Diagram illustrating SiN effect
@ -1 V reverse bias
Ec (1nm SiN)
Ev (1nm SiN)
Ec (no SiN)
Ev (no SiN)
Energy (eV)
5
4
3
2
1
0
-1
-2
0.11
0.115
0.12
0.125
0.13
0.135
0.14
Y (um)

FIG. 8C

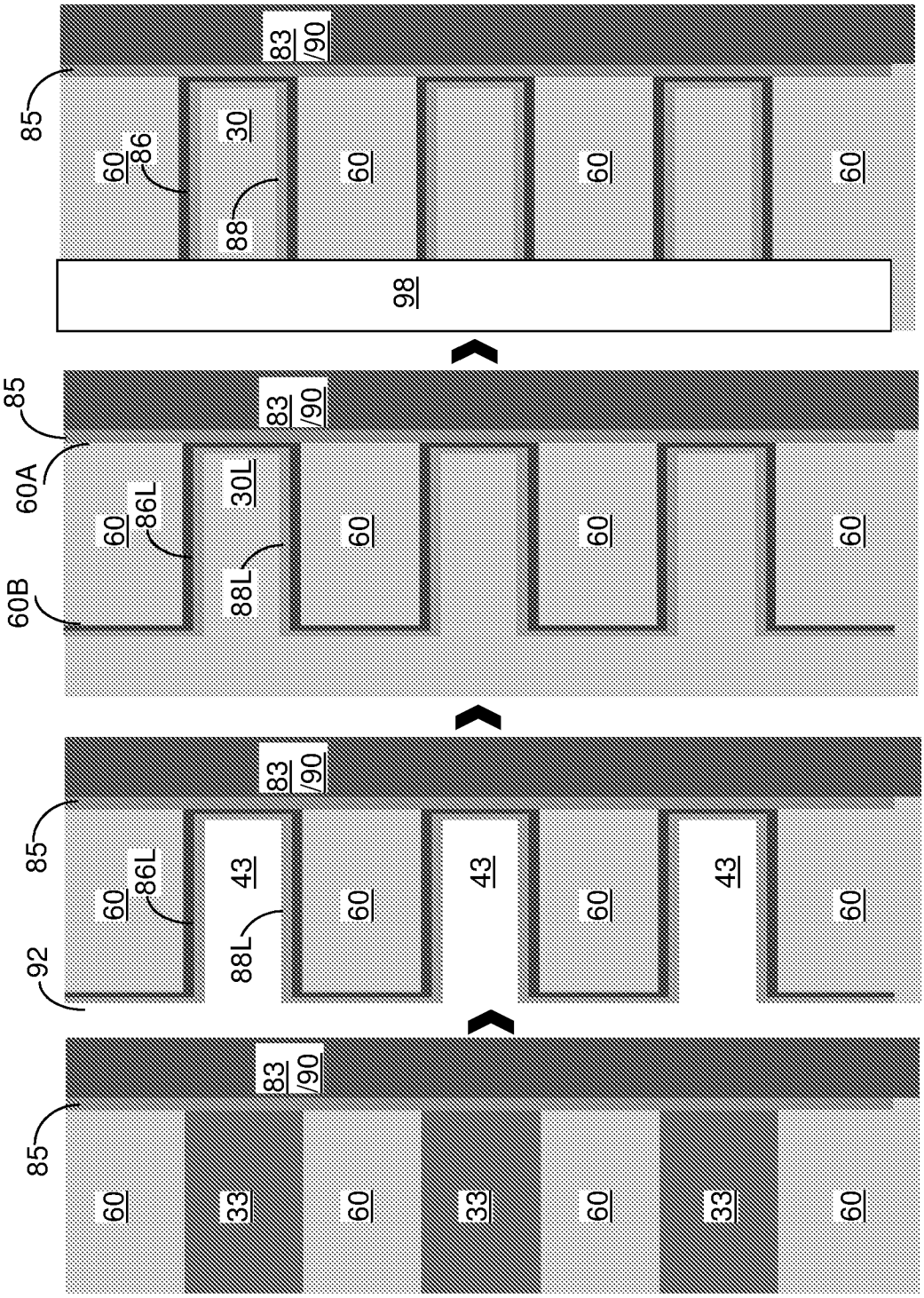


FIG. 9D

FIG. 9C

FIG. 9B

FIG. 9A

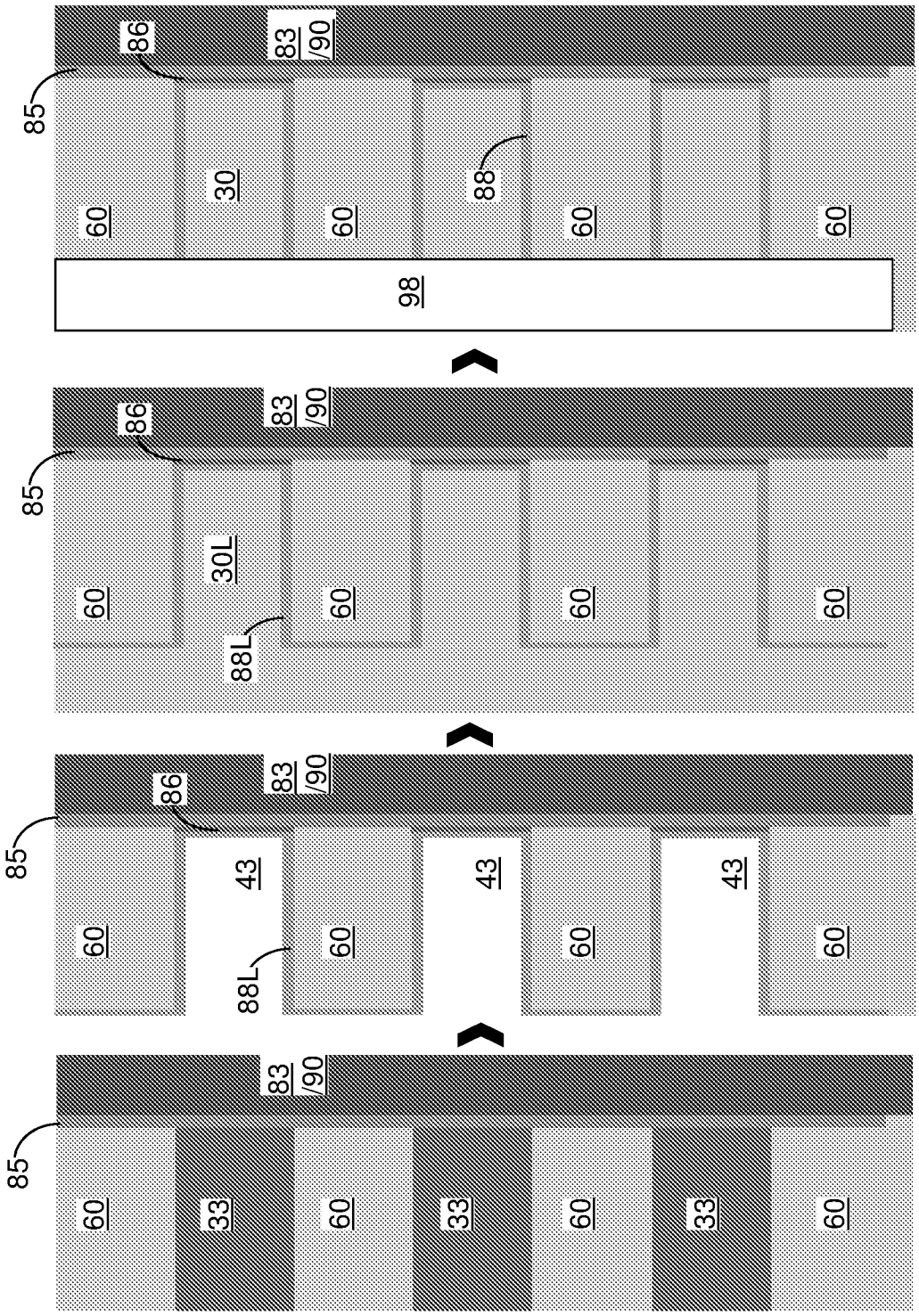


FIG. 10A FIG.10B FIG. 10C FIG. 10D

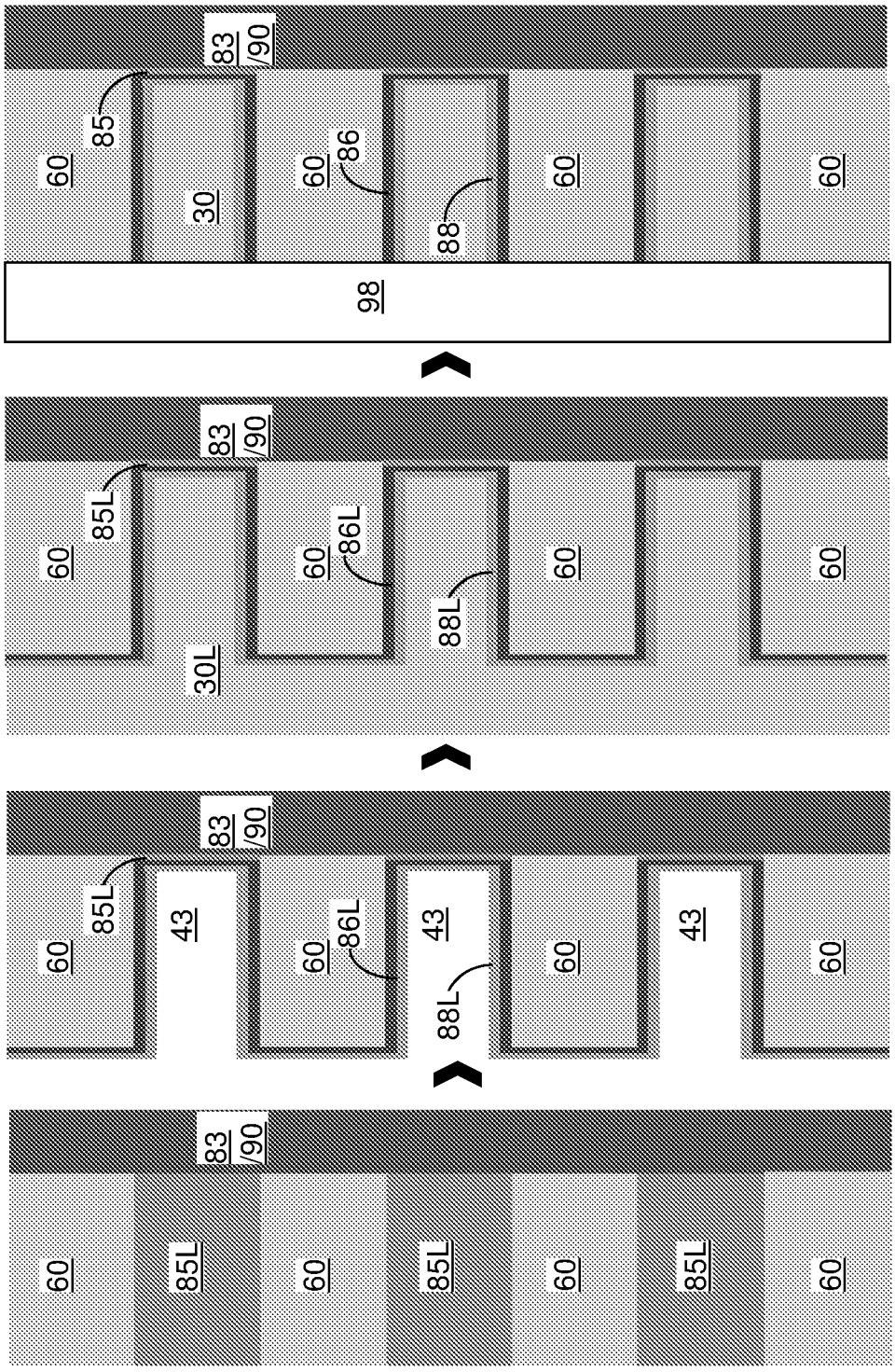


FIG. 11A

FIG. 11B

FIG. 11C

FIG. 11D

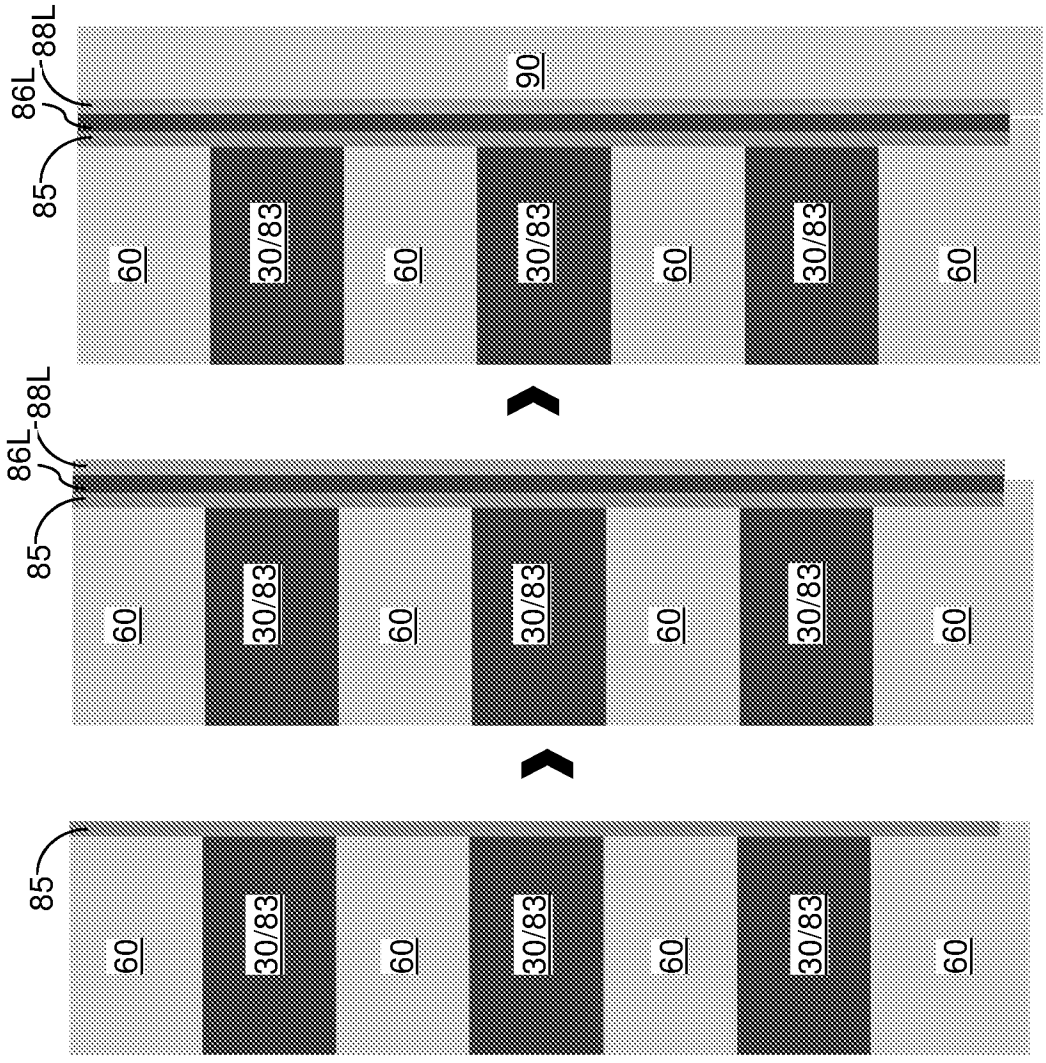


FIG. 12A

FIG. 12B

FIG. 12C

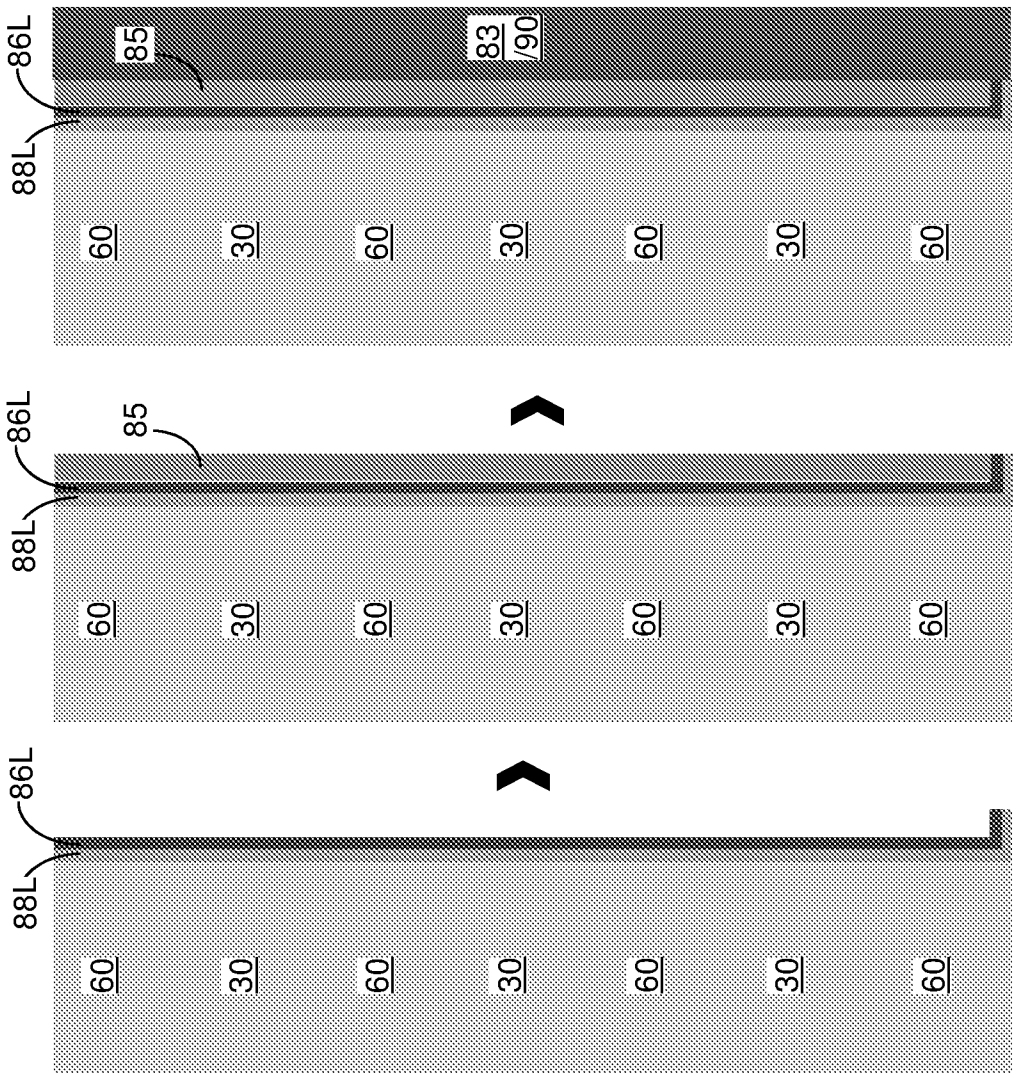


FIG. 13A FIG. 13B FIG. 13C

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/049259

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L45/00 H01L27/24 H01L23/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014/014889 A1 (SHIM SUNIL [KR] ET AL) 16 January 2014 (2014-01-16)	1-12, 16-23, 26,29, 38,39
A	paragraph [0055] - paragraph [0115]; figures 5-9,30,31	13-15, 24,25, 27,28, 30-37
X	US 2012/147649 A1 (SAMACHISA GEORGE [US] ET AL) 14 June 2012 (2012-06-14) paragraph [0244] - paragraph [0253]; figures 23,25	21,23
X	US 2012/001249 A1 (ALSMEIER JOHANN [US] ET AL) 5 January 2012 (2012-01-05) paragraph [0103] - paragraph [0108]; figures 28-30	30

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 November 2016	01/12/2016

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Koskinen, Timo

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2016/049259

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		JP 2014022729 A	03-02-2014
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		US 2014014889 A1	16-01-2014
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US 2012147649 A1	14-06-2012	CN 103370745 A	23-10-2013
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		EP 2731110 A2	14-05-2014
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		US 2014179068 A1	26-06-2014
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		US 2015171099 A1	18-06-2015
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