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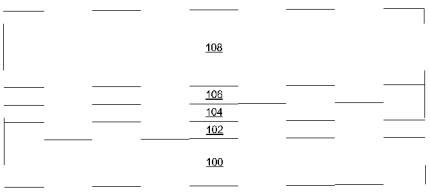

FIG._1A

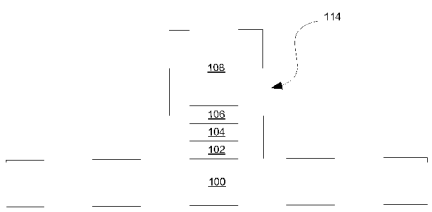

FIG._1B

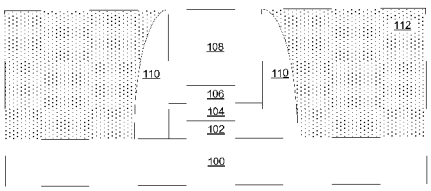

FIG._1C

(57) Abstract: A method for improving the reliability of a high-k gate dielectric layer comprises incorporating a noble metal into a transistor gate stack that contains the high-k gate dielectric layer and annealing the transistor gate stack in a molecular hydrogen or deuterium containing atmosphere. The annealing process drives at least a portion of the molecular hydrogen or deuterium toward the high-k gate dielectric layer. When the molecular hydrogen or deuterium contacts the noble metal, it is converted into atomic hydrogen or deuterium that is able to treat the high-k gate dielectric layer and improve its reliability.

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IMPROVING THE RELIABILITY OF HIGH-K GATE DIELECTRIC LAYERS

Background

In the manufacture of next generation integrated circuits, the fabrication of gate electrodes for complementary metal-oxide-semiconductor (CMOS) transistors has advanced to replace silicon dioxide and polysilicon with high-*k* dielectric materials and metal. A replacement metal gate process is often used to form the gate electrode. A typical replacement metal gate process begins by forming a high-*k* dielectric material and a sacrificial gate between a pair of spacers on a semiconductor substrate. After further processing steps, such as an annealing process, the sacrificial gate is removed and the resulting trench is filled with one or more metal layers. The metal layers can include workfunction metals as well as polysilicon electrode layers. This type of MOS transistor is often referred to as a high-k/metal gate transistor.

It has been shown that the reliability of the high-k gate dielectric layer tends to degrade over time. This is at least partially due to a high concentration of "dangling bonds" on the dielectric material, which serve as reactive sites and eventually lead to breakdown of the gate dielectric and failure of the MOS transistor. The dangling bonds therefore serve to decrease the performance, reliability, and lifetime of the transistor. Accordingly, improved methods of forming high-k/metal gate transistors are needed that can address the issue of dangling bonds in order to improve reliability in the high-k gate dielectric layer, thereby improving transistor performance and extending the life of the transistor.

Brief Description of the Drawings

Figures 1A to 1C illustrate the fabrication of a gate stack for a high-k/metal gate transistor that includes a polysilicon gate electrode.

Figure 2 illustrates a method to convert molecular hydrogen into atomic hydrogen.

Figures 3A to 3C illustrate a method of treating a high-k gate dielectric layer with atomic hydrogen in accordance with an implementation of the invention.

Figures 4A to 4C illustrate a method of treating a high-k gate dielectric layer with atomic hydrogen in accordance with another implementation of the invention.

Figures 5A to 5C illustrate a method of treating a high-k gate dielectric layer with atomic hydrogen in accordance with another implementation of the invention.

Figures 6A to 6C illustrate a method of treating a high-k gate dielectric layer with atomic hydrogen in accordance with yet another implementation of the invention.

Detailed Description

Described herein are systems and methods of improving the reliability of a high-k gate dielectric layer. In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the present invention may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present invention may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present invention, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

As used herein, the term high-k/metal gate transistor refers to a MOS transistor that has a gate oxide formed using a high-k dielectric material and a gate electrode that includes at least one metal that is not polysilicon. A conventional process for forming such a high-k/metal gate transistor is illustrated in Figures 1A to 1C. Starting with Figure 1A, a substrate 100 is shown upon which a high-k gate dielectric layer 102, a metal layer 104, an optional barrier metal layer 106, and a gate electrode layer 108 are deposited.

The substrate 100 may be formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the substrate 100 may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. Although a few examples of materials from which the substrate 100 may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present invention.

Some of the materials that may be used to form the high-k gate dielectric layer 102 include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. Particularly preferred are hafnium oxide (e.g., HfO_2), zirconium oxide, and aluminum oxide. Although a few examples of materials that may be used to form the high-k gate dielectric layer 102 are described here, that layer may be made from other materials. Deposition processes such as chemical vapor deposition (CVD) or atomic layer deposition (ALD) may be used to deposit the high-k gate dielectric layer 102. In various implementations of the invention, the high-k gate dielectric layer 102 may have a thickness that ranges from 5 Angstroms (Å) to 50 Å.

The metal layer 104 may be formed using any conductive material from which a metal gate electrode may be derived, and may be formed on high-k gate dielectric layer 102 using well known physical vapor deposition (PVD), CVD, or ALD processes. When the metal layer 104 will serve as an N-type workfunction metal, layer 104 preferably has a workfunction that is between about 3.9 eV and about 4.2 eV. N-type materials that may be used to form the metal layer 104 include hafnium, zirconium, titanium, tantalum, aluminum, and metal carbides that include these elements, i.e., titanium carbide, zirconium carbide, tantalum carbide, hafnium carbide and aluminum carbide. When the metal layer 104 will serve as a P-type workfunction metal, layer 104 preferable has a workfunction that is between about 4.9 eV and about 5.2 eV. P-type materials that may be used to form the metal layer 104 include ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. The metal layer 104 should be thick enough to ensure

that any material formed on it will not significantly impact its workfunction. Preferably, the metal layer 104 is between about 10 Å and about 300 Å thick, and more preferably is between about 10 Å and about 200 Å thick. Although a few examples of materials that may be used to form the metal layer 104 are described here, that layer may be made from many other materials.

The barrier metal layer 106, if used, may be formed using materials that include, but are not limited to, titanium nitride and tantalum nitride. The barrier layer 106 serves to protect the workfunction metal layer and the gate dielectric layer. The gate electrode layer 108 serves as a conductive fill material for the high-k/metal gate stack. The gate electrode layer 108 may be formed from materials such as polysilicon or a metal such as aluminum. In some implementations, polysilicon is used as a sacrificial gate electrode that is later replaced with a metal gate electrode. In some implementations, a sacrificial material may be used as are well known in the art.

As shown in Figure 1B, the layers deposited on the substrate 100 are then patterned to form a gate stack 114. Patterning processes are well known in the art. For instance, one patterning process begins by depositing a photoresist material over the polysilicon layer 108 and patterning the photoresist using ultraviolet radiation and an optical mask to define features such as the gate stack 114 in the resist layer. The photoresist layer is developed to form a photoresist mask that protects the defined features, such as the portion of the underlying layers that will form the gate stack 114. An etchant is then applied to remove unprotected portions of the underlying layers, yielding a patterned gate stack 114.

Turning to Figure 1C, a pair of spacers 110 and an ILD layer 112 are formed on the substrate 100. The spacers 110 are formed adjacent to the gate stack 114 by depositing a material, such as silicon nitride, on the substrate 100 and then etching the material to form the pair of spacers 110. After the spacers 110 are formed, a low-k dielectric material is deposited and polished to form the ILD layer 112. Low-k dielectric materials that may be used for the ILD layer 112 include, but are not limited to, silicon dioxide (SiO_2), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layer 112 may include pores or other voids to further reduce its dielectric constant. A source region and a drain region

(not shown) may have been formed in the substrate prior to deposition of the ILD layer 112.

As mentioned above, the high-k gate dielectric layer 102 may, over time, degrade and become less reliable due to, at least in part, the reactive dangling bonds that remain on the dielectric material after it is deposited. Therefore, to improve the reliability of the high-k gate dielectric layer 102 in the high-k/metal gate transistor described above, implementations of the invention use a novel process to treat the high-k gate dielectric layer with atomic hydrogen or an isotope of hydrogen such as deuterium. The atomic hydrogen or deuterium serves to react with and eliminate the dangling bonds on the high-k dielectric layer that often lead to device failure.

Figure 2 illustrates a method for converting molecular hydrogen (H_2) or deuterium (D_2) into atomic hydrogen (2 H) or deuterium (2 D). The molecular hydrogen or deuterium may be annealed in the presence of a thin noble metal catalyst layer 200. In implementations of the invention, the thin noble metal catalyst layer 100 may be a metal such as palladium (Pd), platinum (Pt), ruthenium (Ru), rhodium (Rh), osmium (Os), and iridium (Ir). These noble metals serve as effective solid phase catalysts for the activation of molecular hydrogen or deuterium into atomic hydrogen or deuterium. Therefore, during the anneal, the molecular hydrogen or deuterium is driven across the thin noble metal catalyst layer 100 where it is converted into atomic hydrogen or deuterium. This atomic hydrogen or deuterium may then be used to treat the high-k gate dielectric layer.

Figures 3A to 3C illustrate one implementation of the invention where a thin noble metal catalyst layer is used to treat a high-k gate dielectric layer. Figure 3A illustrates the transistor described in Figures 1A to 1C, which includes a substrate 100 upon which a transistor gate stack 114 is formed. The transistor gate stack 114 includes the high-k gate dielectric layer 102, the workfunction metal layer 104, a barrier layer 106, and the gate electrode 108. The gate electrode 108 may be formed from polysilicon or it may be formed from a metal such as aluminum. The transistor also includes the spacers 110 and source and drain regions 116. An ILD layer 112 is deposited and planarized over the high-k/metal gate transistor.

Turning to Figure 3B, a thin noble metal catalyst layer 300 is deposited over the transistor structure, for instance, on the ILD layer 112 and on the gate electrode 108. This

places the noble metal in close proximity to the high-k gate dielectric layer 102. The thin noble metal catalyst layer 300 may consist of Pd, Pt, Ru, Rh, Os, or Ir and may have a thickness that ranges from around 5 Å to around 50 Å. Various deposition methods may be used to deposit the noble metal catalyst layer 300, including but not limited to chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), electroplating, electroless plating, or a metal immobilization process (MIP), such as a palladium immobilization process (PIP), as are well known in the art.

Next, turning the Figure 3C, an annealing process is carried out in an atmosphere that includes molecular hydrogen or deuterium. The annealing process may take place at a temperature that falls between 400°C and 950°C for a time duration that ranges from 5 seconds to 120 seconds. The hydrogen or deuterium may be introduced into the reactor at a flow rate that ranges from 5000 standard cubic centimeters per minute (SCCM) to 15000 SCCM.

During the annealing process, at least a portion of the molecular hydrogen or deuterium diffuses into the transistor gate through the noble metal catalyst layer 300. As the molecular hydrogen or deuterium contacts the noble metal catalyst, at least a portion of the molecular hydrogen or deuterium is converted into atomic hydrogen or deuterium. The annealing process then delivers this atomic hydrogen or deuterium down through the transistor gate stack where at least a portion of the atomic hydrogen or deuterium reaches the high-k gate dielectric layer 102. Here, the atomic hydrogen or deuterium treats the high-k dielectric material by combining with the reactive dangling bonds, rendering them passivated and substantially reducing their concentration. This quenching of the dangling bonds reduces the likelihood of device failure.

After the high-k gate dielectric layer 102 has been treated with the atomic hydrogen or deuterium and the annealing process is completed, the noble metal catalyst layer 300 may be removed. Conventional processes may be used for the removal of the noble metal layer, such as a chemical mechanical planarization (CMP) process or an etching process.

In further implementations of the invention, in lieu of a separate thin noble metal layer, a noble metal may be alloyed into a layer of the transistor gate stack to function as a

catalyst for the conversion of molecular hydrogen or deuterium into atomic hydrogen or deuterium. Figures 4A through 4C illustrate one such implementation.

Starting with Figure 4A, a substrate 100 is shown upon which a high-k gate dielectric layer 102, a modified workfunction metal layer 302, a barrier layer 106, and a gate electrode layer 108 are formed. The modified workfunction metal layer 302 is a workfunction metal that has been alloyed with a noble metal, thereby placing the noble metal in close proximity to the high-k gate dielectric layer 102. In some implementations of the invention, the modified workfunction metal layer 302 may be formed using a CVD or an ALD process. In some implementations, the modified workfunction metal layer 302 may be formed by alloying any of the workfunction metals listed above with a noble metal such as palladium or platinum. In one implementation, the modified workfunction metal layer 302 may be formed by sputtering from an alloy target, where the alloy target includes the desired workfunction metal and the desired noble metal. In an alternate implementation, an ALD process may be used where pulses of a workfunction metal precursor are alternated with pulses of a noble metal precursor.

Turning to Figure 4B, the high-k gate dielectric layer 102, the modified workfunction metal layer 302, the barrier layer 106, and the gate electrode layer 108 are etched to form a transistor gate stack. Spacers 110 are formed adjacent to the gate stack, source and drain regions 116 are formed in the substrate 100, and an ILD layer 112 is deposited and planarized over the structure.

Finally, turning the Figure 4C, an annealing process is carried out in the presence of molecular hydrogen or deuterium. The annealing process may take place at a temperature that falls between 400°C and 950°C for a time duration that ranges from 5 seconds to 120 seconds. The hydrogen or deuterium may be introduced into the reactor at a flow rate that ranges from 5000 SCCM to 15000 SCCM.

During the annealing process, at least a portion of the molecular hydrogen or deuterium diffuses into the transistor gate and passes through the modified workfunction metal layer 302. As the molecular hydrogen or deuterium contacts the noble metal catalyst, at least a portion of the molecular hydrogen or deuterium is converted into atomic hydrogen or deuterium. This atomic hydrogen or deuterium continues down to the high-k gate dielectric layer 102 where it combines with the reactive dangling bonds, rendering

them passivated and substantially reducing their concentration. This quenching of the dangling bonds reduces the likelihood of device failure. Since the noble metal catalyst is alloyed into the workfunction metal layer 302, it remains as a permanent part of the high-k/metal gate transistor and is not removed after the annealing process is completed.

In an alternate implementation of the invention, the annealing process may be carried out immediately after deposition of the modified workfunction metal layer 302. For instance, the high-k gate dielectric layer 102 and the modified workfunction metal layer 302 may be deposited onto the substrate 100 and an annealing process may be carried out prior to deposition of the barrier layer 106. The anneal may occur in a molecular hydrogen or deuterium ambient. The noble metal in the modified workfunction metal layer 302 may convert the molecular hydrogen or deuterium into atomic hydrogen or deuterium that treats the high-k gate dielectric layer 102. In this implementation, the anneal may be followed by deposition of the barrier layer 106 and the gate electrode layer 108. The remainder of the transistor fabrication may follow a conventional process flow.

Turning now to Figure 5A, another implementation of the invention is shown where a noble metal may be alloyed into a layer of the transistor gate stack to function as a catalyst. Figure 5A shows a substrate 100 upon which a high-k gate dielectric layer 102, a workfunction metal layer 104, a modified barrier layer 304, and a gate electrode layer 108 are formed. The modified barrier layer 304 is a barrier layer formed by alloying a noble metal into the barrier layer material (e.g., titanium nitride or tantalum nitride), thereby placing the noble metal in close proximity to the high-k gate dielectric layer 102. In some implementations of the invention, the modified barrier layer 304 may be formed using a CVD or an ALD process. In some implementations, the modified barrier layer 302 may be formed by alloying any of the barrier materials listed above with a noble metal such as palladium or platinum. In one implementation, the modified barrier layer 304 may be formed by sputtering from an alloy target, where the alloy target includes the desired barrier metal and the desired noble metal. In an alternate implementation, an ALD process may be used where pulses of a barrier metal precursor are alternated with pulses of a noble metal precursor. This ALD process may use a nitrogen containing co-reactant and the pulses of the co-reactant may be attenuated over the course of the ALD process.

Turning to Figure 5B, the high-k gate dielectric layer 102, the workfunction metal layer 104, the modified barrier layer 304, and the gate electrode layer 108 are etched to form a transistor gate stack. Spacers 110 are formed adjacent to the gate stack, source and drain regions 116 are formed in the substrate 100, and an ILD layer 112 is deposited and planarized over the structure.

Finally, turning the Figure 5C, an annealing process is carried out in the presence of molecular hydrogen or deuterium. The annealing process may take place at a temperature that falls between 400°C and 950°C for a time duration that ranges from 5 seconds to 120 seconds. The hydrogen or deuterium may be introduced into the reactor at a flow rate that ranges from 5000 SCCM to 15000 SCCM.

During the annealing process, at least a portion of the molecular hydrogen or deuterium diffuses into the transistor gate and passes through the modified barrier layer 304. As the molecular hydrogen or deuterium contacts the noble metal catalyst, at least a portion of the molecular hydrogen or deuterium is converted into atomic hydrogen or deuterium. This atomic hydrogen or deuterium is delivered down to the high-k gate dielectric layer 102 where it combines with the reactive dangling bonds, rendering them passivated and substantially reducing their concentration. This quenching of the dangling bonds reduces the likelihood of device failure. Since the noble metal catalyst is alloyed into the barrier layer 304, it remains as a permanent part of the high-k/metal gate transistor and is not removed after the annealing process is completed.

In an alternate implementation of the invention, the annealing process may be carried out immediately after deposition of the modified barrier layer 304. For instance, the high-k gate dielectric layer 102, the workfunction metal layer 104, and the modified barrier layer 304 may be deposited onto the substrate 100 and an annealing process may be carried out prior to deposition of the gate electrode layer 108. The anneal may occur in a molecular hydrogen or deuterium ambient. The noble metal in the modified barrier layer 304 may convert the molecular hydrogen or deuterium into atomic hydrogen or deuterium that treats the high-k gate dielectric layer 102. In this implementation, the anneal may be followed by deposition of the gate electrode layer 108. The remainder of the transistor fabrication may follow a conventional process flow.

Turning now to Figure 6A, yet another implementation of the invention is shown where a noble metal may be alloyed into a layer of the transistor gate stack to function as a catalyst. Figure 6A shows a substrate 100 upon which a modified high-k gate dielectric layer 306, a workfunction metal layer 104, a barrier layer 106, and a gate electrode layer 108 are formed. The modified high-k gate dielectric layer 306 is a high-k dielectric layer that has been alloyed with a noble metal, thereby placing the noble metal in direct contact with the high-k gate dielectric material. In some implementations of the invention, the modified high-k gate dielectric layer 306 may be formed using a CVD or an ALD process. In some implementations, the modified high-k gate dielectric layer 306 may be formed by alloying any of the high-k materials listed above with a noble metal such as palladium or platinum. In one implementation, the modified high-k gate dielectric layer 306 may be formed by sputtering from an alloy target, where the alloy target includes the desired high-k gate dielectric material and the desired noble metal. In an alternate implementation, an ALD process may be used where pulses of a high-k dielectric precursor are alternated with pulses of a noble metal precursor.

Turning to Figure 6B, the modified high-k gate dielectric layer 306, the workfunction metal layer 104, the barrier layer 106, and the gate electrode layer 108 are etched to form a transistor gate stack. Spacers 110 are formed adjacent to the gate stack, source and drain regions 116 are formed in the substrate 100, and an ILD layer 112 is deposited and planarized over the structure.

Finally, turning the Figure 6C, an annealing process is carried out in the presence of molecular hydrogen or deuterium. The annealing process may take place at a temperature that falls between 400°C and 950°C for a time duration that ranges from 5 seconds to 120 seconds. The hydrogen or deuterium may be introduced into the reactor at a flow rate that ranges from 5000 SCCM to 15000 SCCM.

During the annealing process, at least a portion of the molecular hydrogen or deuterium diffuses into the transistor gate and reaches the modified high-k gate dielectric layer 306. As the molecular hydrogen or deuterium contacts the noble metal catalyst, at least a portion of the molecular hydrogen or deuterium is converted into atomic hydrogen or deuterium. This atomic hydrogen or deuterium then combines with the reactive dangling bonds, rendering them passivated and substantially reducing their concentration.

This quenching of the dangling bonds reduces the likelihood of device failure. Since the noble metal catalyst is alloyed into the high-k gate dielectric layer 306, it remains as a permanent part of the high-k/metal gate transistor and is not removed after the annealing process is completed.

In an alternate implementation of the invention, the annealing process may be carried out immediately after deposition of the modified high-k gate dielectric layer 306. For instance, the modified high-k gate dielectric layer 306 may be deposited onto the substrate 100 and an annealing process may be carried out prior to deposition of the workfunction metal layer 104. The anneal may occur in a molecular hydrogen or deuterium ambient. The noble metal in the modified high-k gate dielectric layer 306 may convert the molecular hydrogen or deuterium into atomic hydrogen or deuterium that treats the high-k gate dielectric layer 306. In this implementation, the anneal may be followed by deposition of the workfunction metal layer 104, the barrier layer 106, and the gate electrode layer 108. The remainder of the transistor fabrication may follow a conventional process flow.

Accordingly, a novel process for improving the reliability of a high-k gate dielectric layer has been disclosed. Implementations of the invention improve the reliability of the high-k/metal gate transistor using atomic hydrogen or deuterium that is delivered via a noble metal catalyst layer. Improving the high-k gate dielectric layer increases the lifetime of the transistor and allows for further transistor scaling.

The above description of illustrated implementations of the invention, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific implementations of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize.

These modifications may be made to the invention in light of the above detailed description. The terms used in the following claims should not be construed to limit the invention to the specific implementations disclosed in the specification and the claims. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

CLAIMS

1. A method comprising:

providing a transistor that comprises:

a high-k gate dielectric layer,

a workfunction metal layer, and

a gate electrode layer;

depositing a noble metal layer over the transistor; and

annealing the high-k gate dielectric layer and the noble metal layer in a molecular hydrogen-containing atmosphere, thereby driving at least a portion of the hydrogen toward the high-k gate dielectric layer through the noble metal layer.

2. The method of claim 1, wherein the noble metal converts the molecular hydrogen into atomic hydrogen and wherein the atomic hydrogen treats the high-k gate dielectric layer.

3. The method of claim 1, wherein the noble metal layer comprises at least one of Pd, Pt, Ru, Rh, Os, or Ir.

4. The method of claim 1, wherein the annealing of the transistor occurs at a temperature between around 400°C and around 950°C for a time duration between around 5 seconds and around 120 seconds.

5. The method of claim 1, wherein the hydrogen comprises deuterium.

6. A method comprising:

forming high-k gate dielectric layer on a substrate;

forming a workfunction metal layer over the high-k gate dielectric layer, wherein the workfunction metal is alloyed with at least one noble metal;

forming a gate electrode over the workfunction metal layer; and

annealing the high-k gate dielectric layer and the workfunction metal layer in a molecular hydrogen-containing atmosphere, thereby driving at least a portion of the hydrogen toward the high-k gate dielectric layer through the noble metal in the workfunction metal layer.

7. The method of claim 6, wherein the noble metal converts the molecular hydrogen into atomic hydrogen and wherein the atomic hydrogen treats the high-k gate dielectric layer.

8. The method of claim 6, wherein the forming of the workfunction metal layer comprises using an ALD process to form the workfunction metal layer, wherein the ALD process

comprises alternately pulsing a workfunction metal precursor and a noble metal precursor on the high-k gate dielectric layer.

9. The method of claim 6, wherein the annealing of the high-k gate dielectric layer and the workfunction metal layer occurs at a temperature between around 400°C and around 950°C for a time duration between around 5 seconds and around 120 seconds.

10. The method of claim 6, wherein the hydrogen comprises deuterium.

11. A method comprising:

forming high-k gate dielectric layer on a substrate;

forming a workfunction metal layer over the high-k gate dielectric layer

forming a barrier metal layer on the workfunction metal layer, wherein the barrier metal is alloyed with at least one noble metal;

forming a gate electrode over the barrier metal layer; and

annealing the high-k gate dielectric layer and the barrier metal layer in a molecular hydrogen-containing atmosphere, thereby driving at least a portion of the hydrogen toward the high-k gate dielectric layer through the noble metal in the barrier metal layer.

12. The method of claim 11, wherein the noble metal converts the molecular hydrogen into atomic hydrogen and wherein the atomic hydrogen treats the high-k gate dielectric layer.

13. The method of claim 11, wherein the annealing of the high-k gate dielectric layer and the barrier metal layer occurs at a temperature between around 400°C and around 950°C for a time duration between around 5 seconds and around 120 seconds.

14. The method of claim 11, wherein the hydrogen comprises deuterium.

15. A method comprising:

forming high-k gate dielectric layer on a substrate, wherein the high-k gate dielectric is alloyed with at least one noble metal;

forming a workfunction metal layer over the high-k gate dielectric layer;

forming a gate electrode over the workfunction metal layer; and

annealing the high-k gate dielectric layer in a molecular hydrogen-containing atmosphere, thereby driving at least a portion of the hydrogen toward the high-k gate dielectric layer and the noble metal in the high-k gate dielectric layer.

16. The method of claim 15, wherein the noble metal converts the molecular hydrogen into atomic hydrogen and wherein the atomic hydrogen treats the high-k gate dielectric layer.

17. The method of claim 15, wherein the forming of the high-k gate dielectric layer comprises using a PVD process to sputter deposit the high-k dielectric and the noble metal on the substrate.

18. The method of claim 15, wherein the forming of the high-k gate dielectric layer comprises using an ALD process to form the high-k gate dielectric layer, wherein the ALD process comprises alternately pulsing a high-k dielectric precursor and a noble metal precursor on the substrate.

19. The method of claim 15, wherein the annealing of the high-k gate dielectric layer occurs at a temperature between around 400°C and around 950°C for a time duration between around 5 seconds and around 120 seconds.

20. The method of claim 15, wherein the hydrogen comprises deuterium.

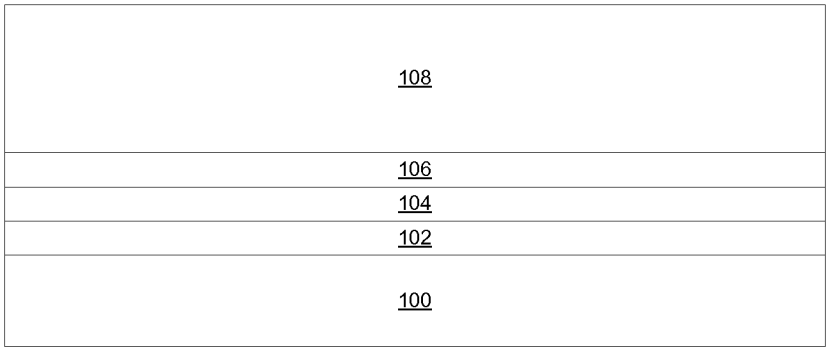

FIG._1A

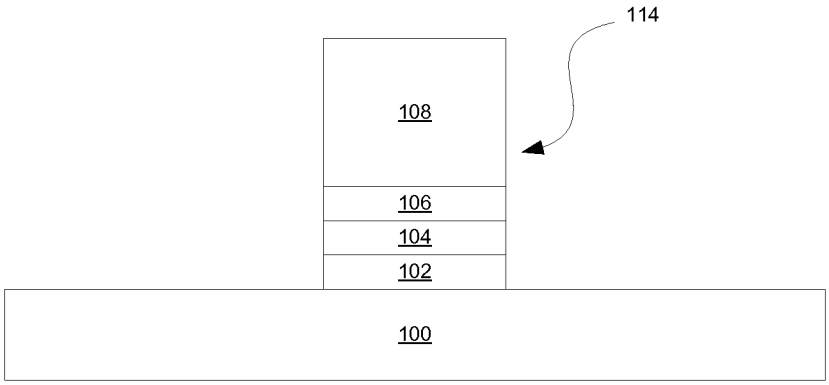

FIG._1B

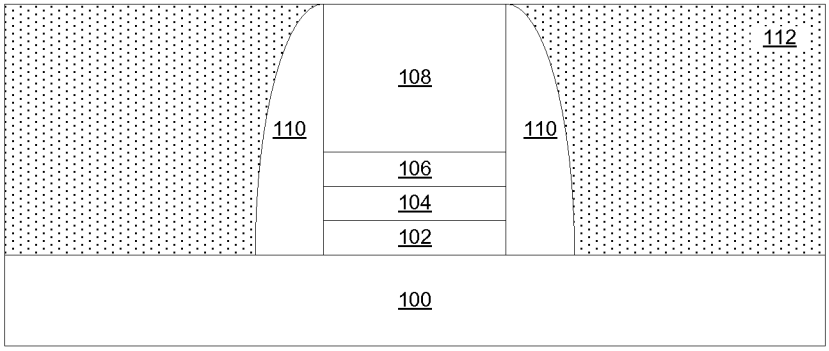

FIG._1C

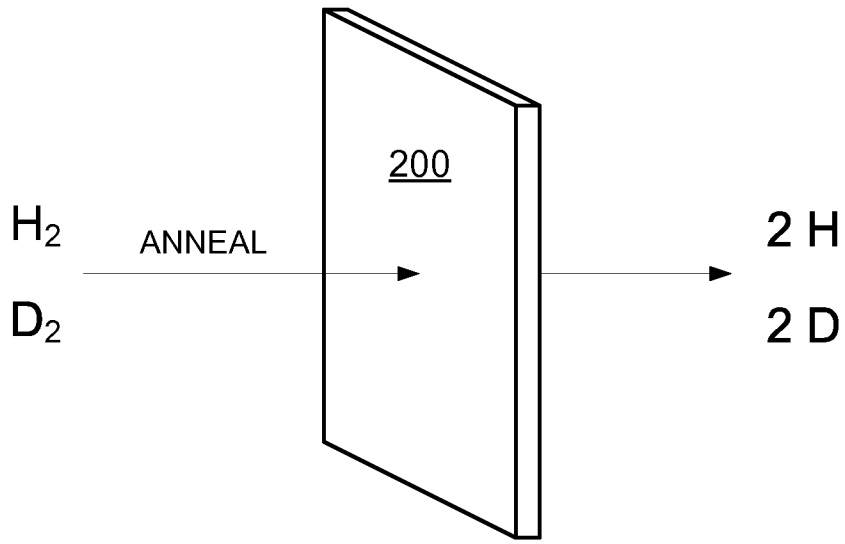

FIG._2

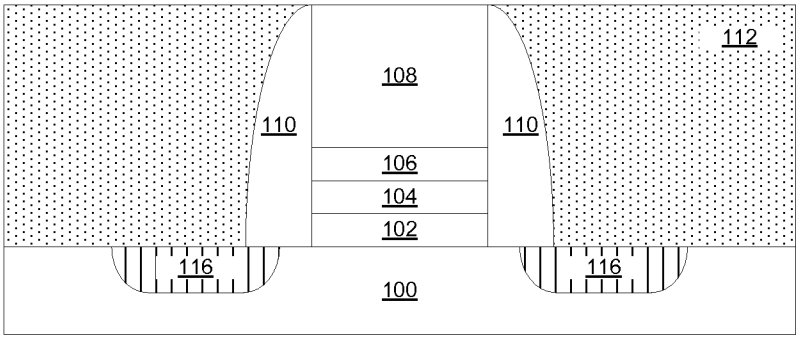

FIG._3A

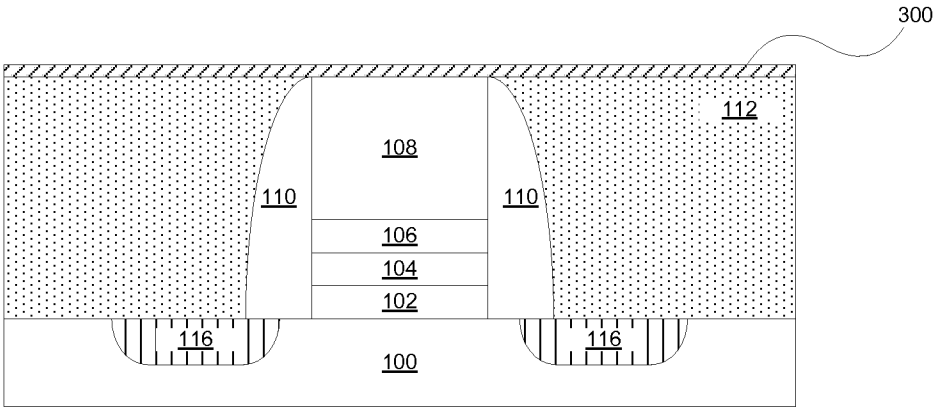

FIG._3B

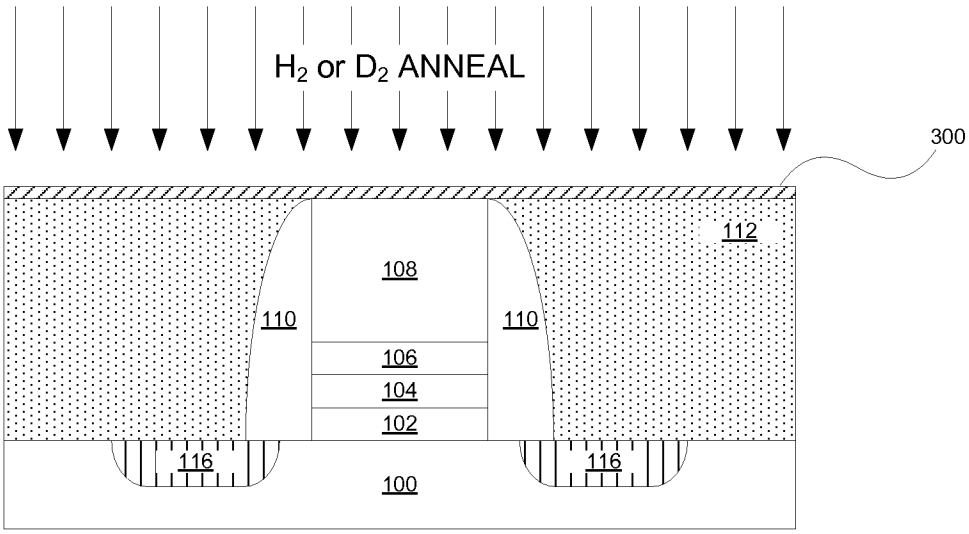

FIG._3C

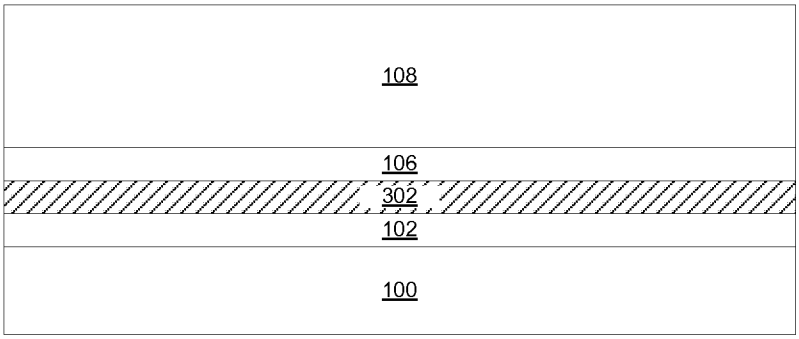

FIG._4A

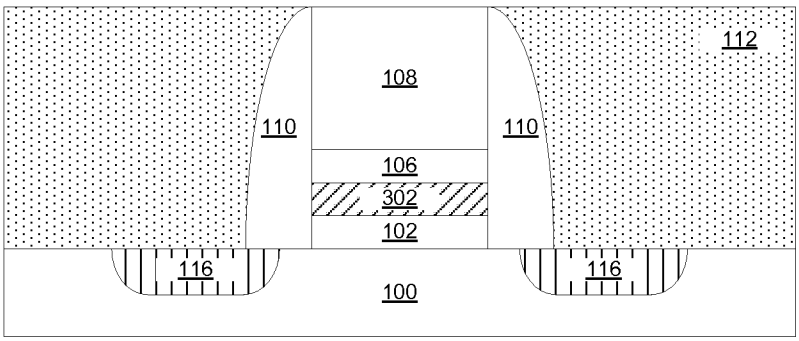

FIG._4B

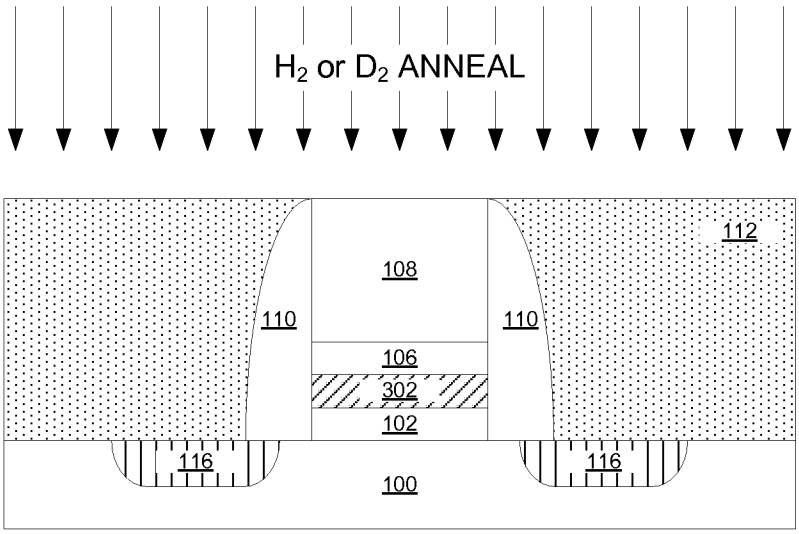

FIG._4C

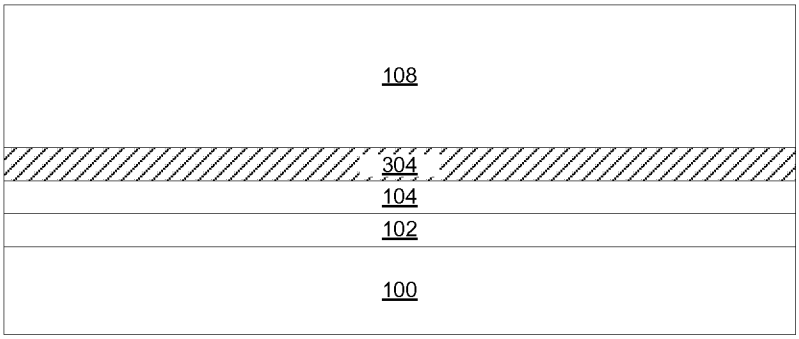

FIG._5A

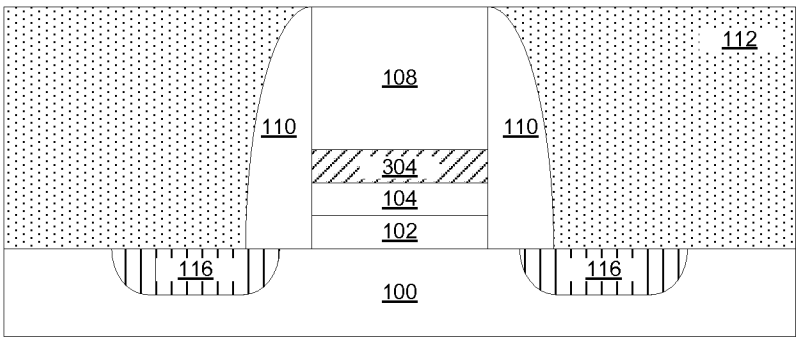

FIG._5B

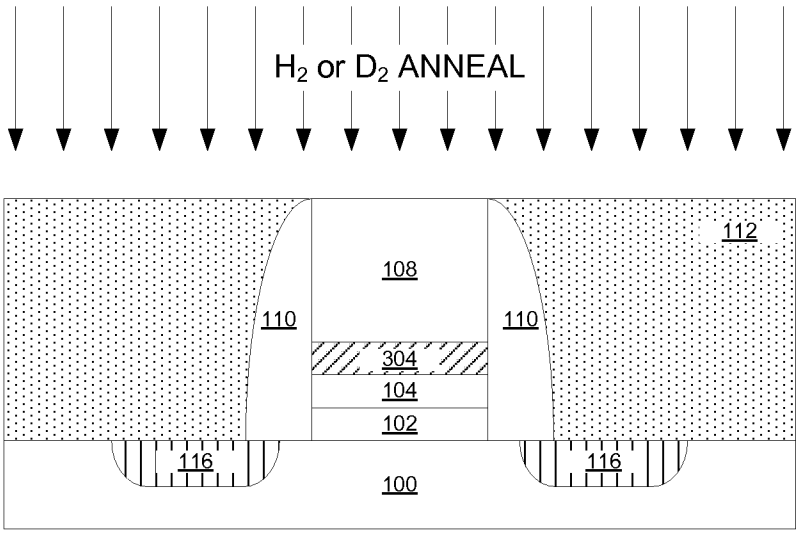

FIG._5C

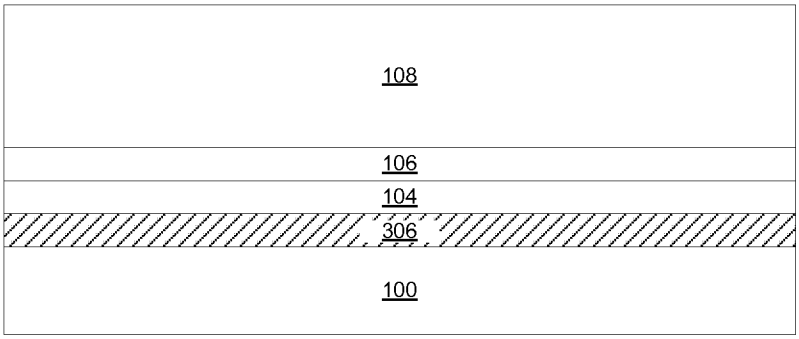

FIG._6A

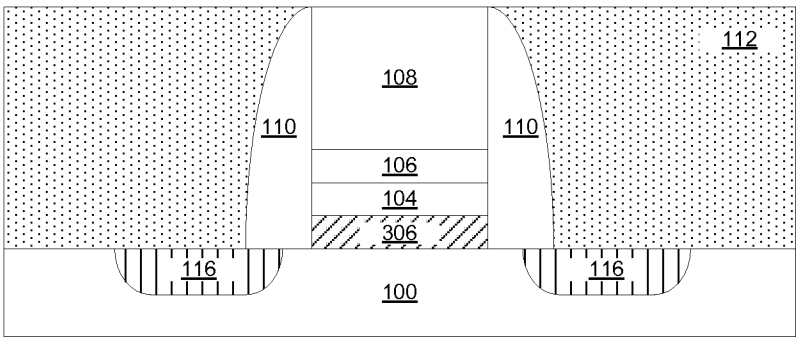

FIG._6B

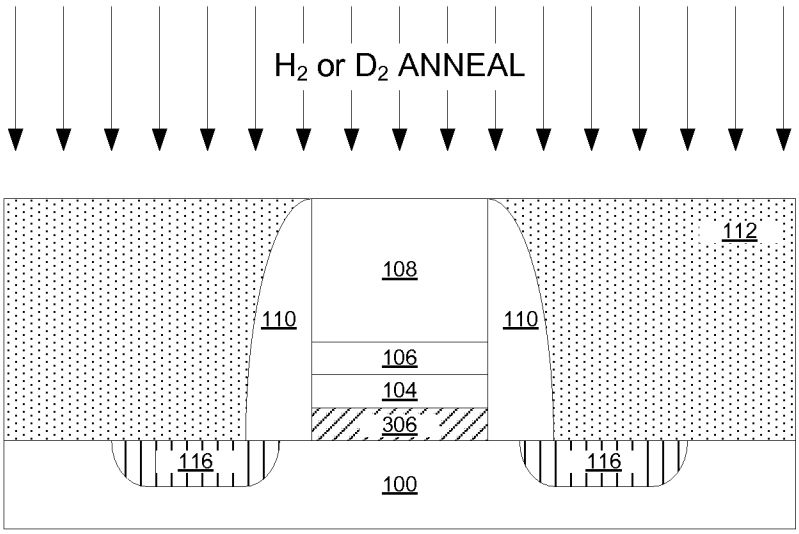

FIG._6C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2008/057551

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 8 : H01L 219/336

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Utility models and applications for Utility models since 1975

Japanese Utility models and application for Utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

e-KIPASS(KIPO internal) : "transistor", "high-k", "hydrogen", "deuterium", " noble metal"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6,326,258 B1 (Toshihiro Iizuka) 4 December 2001 See the abstract, column 2, line 17-column 3, line 59, claims 1 and figures 4,5	1-20
A	US 6,803,266 B2 (Paul M. Solomon et al.) 12 October 2004 See the abstract, column 2, line 33-column 3 line 23, and figure 1	1-20
A	US 6,913,961 B2 (Hyun Sang Hwang) 5 July 2005 See the abstract, column 1, line 22-column 2 line 15, and figure 1	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 AUGUST 2008 (18.08.2008)	**18 AUGUST 2008 (18.08.2008)**

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
Government Complex-Daejeon, 139 Seonsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

PARK, Keun Yong

Telephone No. 82-42-481-8508

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2008/057551

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		JP 3439370 B2	25.08.2003
		US 6326258 B1	04.12.2001
US 6803266 B2	12.10.2004	US 2003-0132492 A1	17.07.2003
US 6913961 B2	05.07.2005	US 2004-0266117 A1	30.12.2004