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GB 2087157 A US 4487654 A

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(54) **Process for making a printed circuit board partially coated with solder**

(57) A process for making a printed circuit board with partial land areas coated with solder has the steps of coating the printed circuit board with solder, applying print ink or dry film resist onto the land areas 30 for a tape carrier package (TCP), removing solder outside the land areas 30, applying a layer of immersion nickel/gold or anti-oxidant agent on the land areas outside the land areas 30, thus forming a printed circuit board having partial land areas coated with solder. The process overcomes the conventional drawbacks that neither the print ink nor dry film resist effectively covers circuitry and areas defining through-holes.

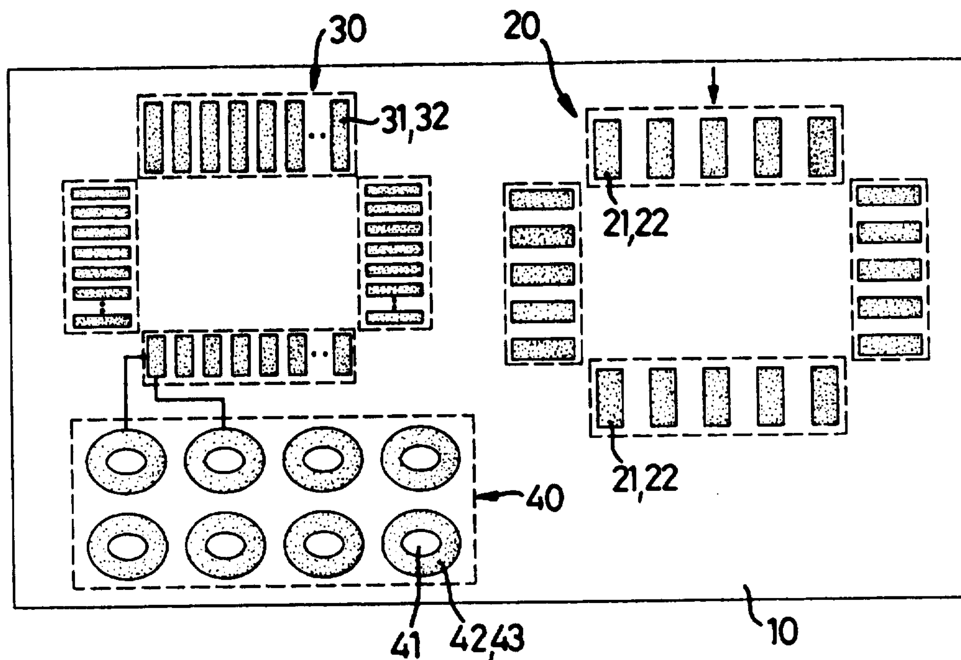

FIG.2

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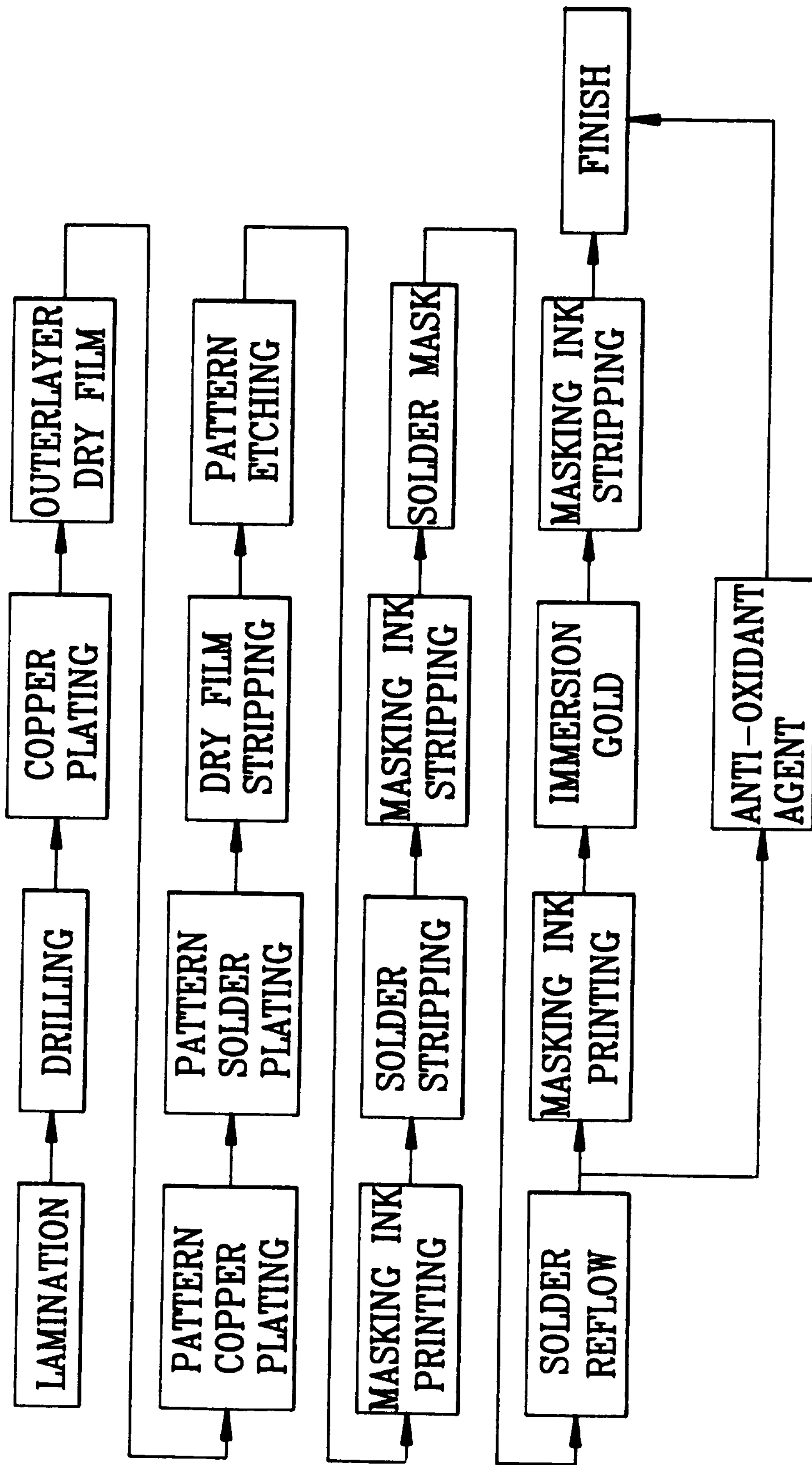

FIG. 1

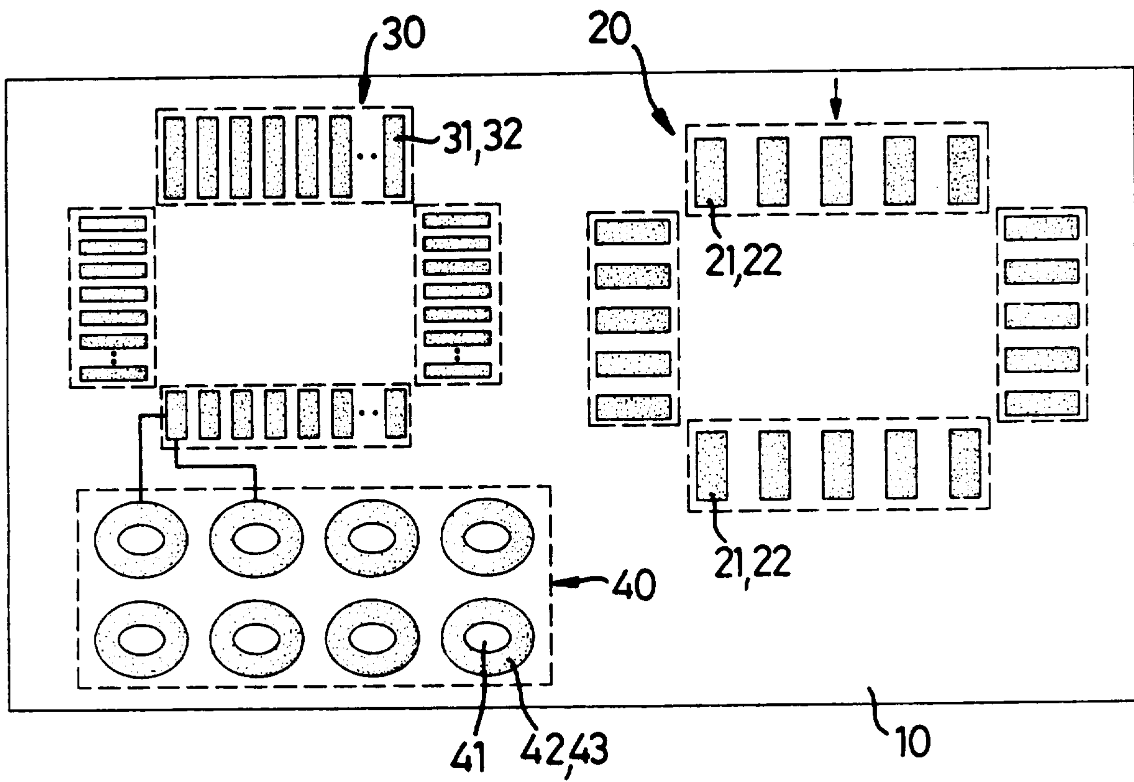

FIG.2

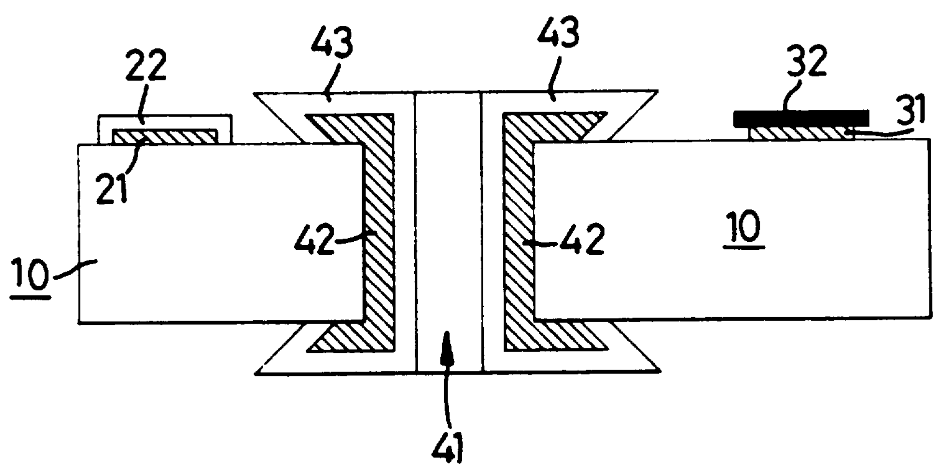

FIG.3

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Description of Invention

Process for a Printed Circuit Board partially coated with Solder

The present invention relates to a process for a printed circuit board (PCB), particularly a process for making a printed circuit board partially coated with solder.

Under the current trend of miniaturization of components, the most common semiconductor package is the type of surface mount technology (SMT). SMT components are directly soldered to PCB surface, resulting in less PCB area required and higher PCB routing density. The current most common SMT assembly process is to print solder paste onto PCB surface and then IR reflow to get eutectic solder joint. Normally, the PCB surface is coated with a thin layer of solder by hot air solder leveling (HASL) technology. Using HASL process, all component lands & through-holes will be coated by solder and which solder is thin and not uniform. The current most common finest pitch SMT in volume production is 0.020" pitch with I/O 208 pins. For greater I/O number IC packaging of SMT component by reducing component pitch (less than 0.020") or increasing component size with same pitch is difficult for most users. Finer pitch of SMT is hard to handle (fragile lead) and more difficult for solder paste printing and registration. Bigger component is too expensive. Thus, new alternatives of IC packaging for high pin count is getting more attention. One of the

potential alternative is TCP (Tape Carrier Package). Most common pitch of TCP is 0.25 mm or even 0.2 mm so that it is extremely difficult to print solder paste on each land in assembly processes to date.

Therefore, a so-called selective solder plating PCB is developed for TCP application. This selective solder plating PCB is to keep a layer of uniform and thick solder over TCP land areas and the other pads for traditional SMT or lead components will be coated by a layer of immersion gold or bare copper finish with anti-tarnish coating. This thick and uniform solder over TCP will eliminate traditional solder paste printing, and TCP components can be directly placed and soldered to these lands without solder paste required.

Key to the selective solder plating PCB is how to find a masking material to protect the solder over TCP land areas and strip the rest areas. Traditional process is to use a dry film to mask all SMT, TCP and other lead components' through-holes. Using this process, all these land areas will be coated with solder. However, the dry film is hard to get good conformation to a circuit profile due to film tension and various circuit height, so that the solder being partially stripped over these land areas. When a PCB is designed with big component holes, then it is more difficult to tent these holes by the dry film.

It is the purpose of this present invention, therefore, to mitigate and/or obviate the above-

mentioned drawbacks in the manner set forth in the detailed description of the preferred embodiment.

Accordingly, it is an object of this invention to provide a process for a printed circuit board being partially coated with solder, in which solder over TCP can be well protected. Thus, at the end of the process, only solder remains on TCP land areas.

Another object of this invention is to provide a process for a printed circuit board having partially coated solder thereon, in which the areas other than TCP land areas such as SMT and through-holes are applied by a layer of immersion gold or anti-oxidant agent.

Further objects and advantages of the present invention will become apparent as the following description proceeds, and the features of novelty which characterize the invention will be pointed out with particularity in the claims annexed to and forming a part of this application.

For a better understanding of the present invention and objects thereof, a study of the detailed description of the embodiments described hereinafter should be made in relation to the accompanying drawings.

In the drawings:

Fig. 1 is a flow chart of the process according to the present invention;

Fig. 2 is a schematic top view of TCP of PCB of

the present invention; and

Fig. 3 is a cross-sectional view of a printed circuit board of the present invention.

The present invention will be described in detail with reference to Figure 1 through 3 of the drawings showing the preferred embodiment thereof.

Referring initially to Fig. 1 and the accompanying Figs 2 and 3, a plurality of laminates (not shown) are pressed into a board 10. Then, a plurality of through-holes 41 are drilled at predetermined sites to the board 10. Walls defining the through-holes 41 of the board 10 are each panel plated by copper. Outerlayer circuitry is then defined by a dry film. After that, patterns are plated by copper and solder. Resist (dry film) is then stripped, leaving the solder plated pattern and base copper. Pattern is etched by a conventional process. TCP land areas 30 as shown by dashed blocks are covered by a layer of printed ink or dry film resist to protect these areas from being stripped in the following steps. The areas other than TCP land areas 30 are then stripped by a conventional solder stripping operation. The area of printed ink or dry film resist for protecting the TCP area 30 is removed. Next process is to print solder mask to cover all signal trace. After that, apply solder fusing to get eutectic solder alloy. After fusing, print ink is applied over TCP land areas 30 to protect these areas from being damaged during the next operation. It is

then to put on a layer of immersion nickel/gold coating over the other component areas. The layer of printed ink is removed. Alternatively, the steps from the ink printing, immersion nickel/gold and ink stripping can be replaced by covering the board 10 with a layer of anti-oxidant agent, for example ENTEK.

Fig. 2 is a schematic top view of the TCP land areas 30 of the print circuit board of the present invention, including TCP land areas 30 as shown at the left upper portion thereof, SMT land areas 20 as shown at the right portion thereof, and a through-hole area 40.

Still referring to Figs. 2 and 3, there are a plurality of rectangular portions provided at the TCP land areas 30. Similarly, a plurality of rectangular portions are provided at the SMT land areas 20. In the TCP land areas 30, the rectangular portion is a copper foil 31 which is covered by a layer of solder 32. Conversely, the rectangular portions at the SMT land areas 20 are each a copper foil 21 which is covered by a layer of an anti-oxidant agent 22. A plurality of through-holes 41 are provided at the through-hole area 40. Each through-hole 41 is defined by an inner wall which is plated with a layer of copper 42, and a surface of the layer of copper 42 is further coated with a layer of immersion gold or anti-oxidant agent 43.

Since the TCP land areas 30 in Figs. 2 and 3 are

the areas which retain solder thereon, only the application of print ink or dry film resist onto the solder of the TCP land areas 30 is needed to protect the TCP land areas 30. A step of applying print ink or dry film resist is easily performed due to small area and elimination of through holes. Masking conformation is easier assured and no inappropriate removal of solder will happen. Thus, the yield of the present process can be surely increased.

Accordingly, the present invention provides an innovative process which possesses advantages such as easy operation and convenience when compared with the conventional process for manufacturing a printed circuit board.

While the present invention has been explained in relation to its preferred embodiment, it is to be understood that various modifications thereof will be apparent to those skilled in the art upon reading this specification. Therefore, it is to be understood that the invention disclosed herein is intended to cover all such modifications as shall fall within the scope of the appended claims.

Claims:

1. A process for a printed circuit board comprising the steps:

pressing a plurality of laminates into a board (10);

drilling a plurality of through-holes (41) into said board (10) at predetermined sites;

panel plating walls defining said through holes (41) of said board (10) with copper;

applying a dry film resist on said board (10) to define a pattern;

plating said pattern with copper;

plating said pattern having copper thereon with solder;

removing said dry film resist;

etching said pattern of said board (10);

masking a tape carrier package (TCP) land area (30) with print ink or dry film resist;

stripping said solder;

removing said print ink or dry film resist;

applying a solder mask on said pattern; the improvement comprising:

reflowing said solder;

masking said TCP area (30) with dry film resist or print ink;

immersing said board (10) other than said TCP land area (30) with nickel/gold;

removing said print ink or dry film resist, so

that a print circuit board having said TCP area (30) covered with solder is formed.

2. A process according to claim 1, wherein the steps after the improvements are replaced by coating said board (10) with an anti-oxidant agent.

3. A process according to claim 2, wherein said anti-oxidant agent is ENTEK.

4. Any novel feature or combination of features disclosed herein.

Patents Act 1977 **Examiner's report to the Comptroller under Section 17** **(The Search report)**	Application number GB 9509198.9
Relevant Technical Fields (i) UK Cl (Ed.N) H1R (RAA, RAB, RAE, RAF, RAH) (ii) Int Cl (Ed.6) H05K	Search Examiner J DONALDSON Date of completion of Search 7 JUNE 1995
Databases (see below) (i) UK Patent Office collections of GB, EP, WO and US patent specifications. (ii) ONLINE: WPI	Documents considered relevant following a search in respect of Claims :- 1

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages		Relevant to claim(s)
A	GB 2087157 A	(QUASSIA) see page 2 line 85 - page 3 line 6	-
A	US 4487654	(COPPIN) see Figure 2	-

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