
(12) PATENT ABRIDGMENT (11) Document No. AU-B-47186/89
(19) AUSTRALIAN PATENT OFFICE (10) Acceptance No. 628120

(54) Title
INFORMATION PROCESSING SYSTEM AND APPARATUS

International Patent Classification(s)
(51)⁴ **G09G 001/00 G09G 003/00**

(21) Application No. : **47186/89**

(22) Application Date : **20.12.89**

(30) Priority Data

(31) Number	(32) Date	(33) Country
1-233771	08.09.89	JP JAPAN
1-236310	11.09.89	JP JAPAN

(43) Publication Date : **01.08.91**

(44) Publication Date of Accepted Application : **10.09.92**

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(57) Claim

1. An information processing system comprising:
 - a. an image information memory for storing received image information;
 - b. first control means for controlling driving of a display panel; and
 - c. second control means for controlling said image information memory so that storage of the image information in said image information memory is synchronized with transfer of the image information stored in said image information memory to a drive control circuit.

628120

S & F Ref: 116499

FORM 10

COMMONWEALTH OF AUSTRALIA

PATENTS ACT 1952

COMPLETE SPECIFICATION

(ORIGINAL)

FOR OFFICE USE:

Class Int Class

Complete Specification Lodged:
Accepted:
Published:

Priority:

Related Art:

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Complete Specification for the invention entitled:

Information Processing System and Apparatus

The following statement is a full description of this invention, including the best method of performing it known to me/us

1 ABSTRACT OF THE DISCLOSURE:

2 In information processing apparatus, transfer
3 scan line addresses are monitored within a graphic
4 microprocessor partial update routine to continuously
5 transfer image information of addresses of the same
6 scan line when a two-line simultaneous drive waveform
7 is used to increase a frame frequency. The information
8 processing system comprising an image information memory
9 for storing received image information first control
10 means for controlling driving of a display memory,
11 and second control means for controlling the image
12 information memory so that storage of the image
13 information in the image information memory and transfer
14 of the image information stored in the memory to a
15 drive control circuit are synchronized with each other.

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1 TITLE OF THE INVENTION

Information Processing System and Apparatus

BACKGROUND OF THE INVENTION

5 Field of the Invention

The present invention relates to an information processing system and apparatus and, more particularly, to an image information processing system and apparatus suitable for a display device using a ferro-electric liquid crystal.

Related Background Art

A typical conventional computer terminal display device is a refresh scan type CRT. A vector scan type CRT having a partial memory function is often used for a CAD large, high-precision display. In a vector scan type CRT, once information is displayed on its screen, the screen is not updated until the screen content is erased. Therefore, the vector scan type CRT is not suitable as a real-time man-machine interface display device for performing a cursor shift display, a shift display of an icon such as a mouse as a display of information from a pointing device, an edit display (e.g., insertion, deletion, shift, and copy) of characters and sentences. On the other hand, the refresh scan type CRT requires a refresh cycle of 60 Hz or more as a frame frequency in order to prevent flickering. In order to improve icon readability and a shift display (mouse or cursor) of intrascreen

1 information, a non-interlaced scan scheme is employed (a
television receiver has a field frequency of 60 Hz or a
frame frequency of 30 Hz in order to achieve a dynamic
image display and simplify a drive control system). For
5 this reason, when a display resolution is increased, the
display device becomes large in size. In addition, a
high power is required, and a drive controller becomes
bulky, resulting in high cost.

In recent years, a flat display panel has been
10 introduced to cope with inconvenience of a large,
high-power CRT.

Several existing drive schemes are available for
the flat display panels. For example, a time-divisional
drive system (STN) for a twisted nematic liquid crystal,
15 a monochromatic display system (NTN) as its
modification, or a plasma display system employs the
same image data transfer scheme as the CRT. In
addition, a screen update scheme also employs a
non-interlaced scan scheme having a frame frequency of
20 60 Hz or more. Therefore, the total number of scan
lines constituting one frame ranges from 400 to 480,
which cannot exceed 1,000 due to the following reason.
Since such a display panel does not have a memory
function due to the principle of driving, it requires a
25 refresh cycle having a frame frequency of 60 Hz or more
to prevent flickering. One horizontal scan interval
becomes as short as 10 to 50 μ sec or less. As a result,

1 a high contrast level cannot be obtained.

A ferro-electric liquid crystal display device has a larger screen than that of the above display devices and can perform high-precision display. However, in
5 order to cope with the man-machine interface display device at a low frame frequency, a partial update scan scheme (i.e., only scan lines within an update area are scanned) is required. The partial update scan scheme is described in U.S.P. No. 4,655,561 to Kanbe et al.

10 The partial update scan scheme is particularly suitable for the ferro-electric liquid crystal display device to perform a shift display of a mouse or cursor and a scroll display of a multi-window. However, partial update scan of different areas cannot be
15 simultaneously performed. When partial update scan is performed by designating a partial update scan start address and its end address, the shift display of a mouse or cursor cannot be performed during scrolling of the multi-window. A window scroll display and a point
20 device display are considered as examples, and their display movements are assumed. Even if the point device is moved after the scroll partial update scan is started on the display panel, update scan of the pointing device cannot be started until the end of scan of the final
25 scan line address of the window. For this reason, the pointing device is discontinuously moved in accordance with the size of the window (i.e., the number of partial

update scan lines), resulting in an unnatural shift display.

SUMMARY OF THE INVENTION:

5 It would therefore be advantageous to provide an information processing apparatus wherein transfer scan line addresses are monitored within a graphic microprocessor partial update routine to continuously transfer image information of addresses of the same scan line when a two-line simultaneous drive waveform is used to increase a frame frequency.

10 According to the present invention, there is provided an information processing system comprising:

- a. an image information memory for storing received image information;
- b. first control means for controlling driving of a display panel; and
- 15 c. second control means for controlling said image information memory so that storage of the image information in said image information memory is synchronized with transfer of the image information stored in said image information memory to a drive control circuit.



BRIEF DESCRIPTION OF THE DRAWINGS:

Figs. 1A and 1B are block diagrams showing a ferro-electric liquid crystal display device and a graphic controller;

5 Figs. 2A to 2G are timing charts of image information communication between the ferro-electric liquid crystal display device and the graphic controller;

Fig. 3 is a view showing a display screen to illustrate a plurality of graphic events;

Fig. 4 is a block diagram of a display control program;

10 Figs. 5A and 5B are block diagrams of the graphic controller used in the present invention;

Fig. 6 is a block diagram of a digital interface;

Fig. 7 is a timing chart of an interface for a display drive unit;

Figs. 8A to 8I are timing charts of an interface for



1 an FLCDC controller;

Figs. 9A and 9B show a partial update algorithm of a two-line simultaneous access waveform according to the present invention;

5 Fig. 10 is a view for explaining data mapping between scan line address information and display information in the VRAM:

Fig. 11 is a view showing a multi-window display screen;

10 Fig. 12A is a drive waveform chart used in the present invention;

Fig. 12B is a view showing a display state of pixels at that time;

Fig. 13 is a timing chart thereof;

15 Figs. 14A and 14B are drive waveform charts used in the present invention;

Figs. 15A to 15C are timing charts thereof;

Fig. 15D is a view showing a display state of pixels at that time; and

20 Figs. 16 and 17 are respectively perspective views of ferro-electric liquid crystal cells used in the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS:

[Embodiments]

25 Fig. 1A is a block diagram of a ferro-electric liquid crystal display device 101 and a graphic controller 102 arranged in a main unit such as a

1 personal computer serving as a source of display
information. Figs. 2A to 2G are communication timing
charts of image information. A display panel 103 is
arranged such that 1,120 scan electrodes and 1,280
5 information electrodes are arranged in a matrix, and a
ferro-electric liquid crystal is sealed between two
aligned glass plates. The scan lines are connected to a
scan line drive circuit 104, and the information lines
are connected to an information line drive circuit 105.

10 An operation of the above apparatus will be
described with reference to the accompanying drawings.
The graphic controller 102 transfers to a display drive
circuit (consisting of the line drive circuits 104 and
105) 104/105 of the liquid crystal display device 101
15 image information (PD0 to PD3) on the scan line
designated by scan line address information for
designating the scan electrode and its address
information. In this embodiment, in order to transfer
image information having the scan line address
20 information and the display information on one
transmission line, two types of information must be
distinguished from each other. For this purpose, an
identification signal AH/DL is used. When the signal
AH/DL is set at high level, it represents the scan line
25 address information. However, when the signal AH/DL is
set at low level, it represents display information.

The scan line address information is extracted by a

1 drive control circuit 111 in the liquid crystal display
device 101 from image information sent as image
information PD0 to image information PD3, and the
extracted signals are output to the scan line drive
5 circuit 104 at a timing for driving the designated scan
line. The scan line address information is input to a
decoder 106 in the scan line drive circuit 104, and the
scan electrode designated by the display panel 103 is
driven by a scan signal generator 107 through the
10 decoder 106. The display information is supplied to a
shift register 108 in the information line drive circuit
105 and is shifted in response to a transfer clock in
units of four pixels. When one scan line shift in the
horizontal direction is completed by the shift register
15 108, 1,280-pixel display information is transferred to a
line memory 109 arranged in parallel with the shift
register 108 and is stored within one horizontal scan
interval. The stored information is output from an
information signal generator 110 to each information
20 electrode as a display information signal.

Driving of the display panel 103 by the liquid
crystal display device 101 is asynchronous with
generation of scan line address information and display
information by the graphic controller 102. Therefore,
25 the display device 101 must be synchronized with the
controller 102 during image information in response to a
signal SYNC. The signal SYNC is generated by the drive

1 control circuit 111 in the liquid crystal display device
101 every horizontal scan interval. The graphic
controller 102 always monitors the signal SYNC. When
the signal SYNC is set at low level, image information
5 transfer is performed. However, when the signal SYNC is
set at high level, no transfer is performed at the end
of transfer of the image information of one horizontal
scan line. That is, when the graphic controller 102
detects that the signal SYNC goes low in Fig. 2, the
10 signal AH/DL is set at high level to start transfer of
the image information of one horizontal scan line. The
drive control circuit 111 in the liquid crystal display
device 101 sets the signal SYNC at high level during
transfer of the image information. After write access
15 of the display panel 103 through one predetermined
horizontal scan interval, the drive control circuit
(FLCD controller) 111 sets the signal SYNC to low level
again and can receive image information of the next scan
line.

20 Fig. 3 shows a display screen 3 obtained when a
display request for a plurality of pieces of display
information is made in a multi-window, multi-task
system.

Display request 31: a request for smoothly
25 moving a mouse font
obliquely
Display request 32: a request for selecting a

1		given window as an active screen and displaying a portion overlapping the previous window as a front layer
5	Display request 33:	a request for inserting a character input from a keyboard
	Display request 34:	a request for moving a previous character (character shift to a direction of an arrow)
10		
	Display request 35:	a request for changing a display of an overlap area
15	Display request 36:	a request for displaying a non-active window
	Display request 37	a request for scrolling and displaying the non-active window
20	Display request 38:	a request for displaying a full image field

Table 1 below represents a display priority order of graphic events corresponding to display requests 31 to 38.

Table 1

Graphic Event	Drive Mode	Display Priority Order	Drawing Operation
31 mouse shift display	partial update	highest level	
32 active window area ON			logical access area
33 character insertion display	partial update	second level	
34 character shift display	partial update	third level	
35 overlap area display change			logical VRAM operation
36 non-active window area ON			logical access area
37 non-active window area scroll display	partial update	fourth level	
38 full image field display	multi-field refresh	lowest level	

1 The "partial update" in Table 1 represents a drive
scheme for scanning only scan lines of a partial update
area, and the "multi-field refresh" represents a
one-frame scan scheme by scanning N fields ($N = 2, 4,$
5 $8, \dots, 2^N$) in multi-interlaced scanning (drive scheme
described in U.S.S.N. 271,240 filed on November 4,
1988). The "display priority order" represents an order
designated beforehand. In this embodiment, operability
of the man-machine interface has the top priority, so
10 that graphic event 31 (i.e., mouse shift display) has
the highest priority, and the priority order is lowered
in the order of graphic events 33, 34, 37, and 38. The
"drawing operation" represents an internal drawing
operation in the graphic processor.

15 The mouse shift display has the top priority
because the pointing device aims at quickly (real time)
reflecting the will of the operator in the computer.
The next important factor is a character input from the
keyboard. The character input is generally buffered,
20 and its real-time response is lower than that of the
mouse. The screen update within the window as a result
of the key input need not always be real-time with the
key input. A line subjected to key input operations has
a higher priority. A relationship between the scroll
25 display within another window and an overlap area is
changed depending on system setup specifications. Line
scroll is performed under an active window.

1 According to the present invention, a screen
display control program shown in Fig. 4 has a function
for accepting external display requests 31 to 38 through
the illustrated communication procedures and
5 transferring image information to the ferro-electric
liquid crystal display device (FLCD) 101 shown in
Fig. 1A. Once a display content update request is
generated, the screen display control program determines
an update area and drawing processing of the VRAM (image
10 information memory) required for this updating in
accordance with the display priority order, and selects
image information to be sent to the display device 101
and then transfers them thereto in synchronism
therewith.

15 A window manager 41 and an operating system (OS) 42
are used in the communication procedures in Fig. 4. An
"MS-DOS" (tradename) or a "XENIX" (tradename) available
from Microsoft Corp., U.S.A., a "UNIX" (tradename)
available from AT & T, U.S.A., or an "OS/2" (tradename)
20 available from Microsoft Corp., U.S.A. can be used as
the operating system (OS) 42. An "MS-Windows ver 1.03"
or "ver 2.0" (tradename) available from Microsoft Corp.,
U.S.A., an "OS/2 Presentation Manager" available from
Microsoft Corp., U.S.A., an "X-Window" as a public
25 domain, or a "DEC-Window" (tradename) available from
Digital Equipment Corp, U.S.A. can be used as the window
manager 41. An event emulator 43 may comprise an

1 "MS-DOS & MS-Windows" or "UNIX & X-Window".

The partial update" used in the present invention is to scan only scan lines of a partial update area. Since the FLCD has a memory function, high-speed partial
5 update can be performed. The present invention presumes that high-speed update of display information by the computer system on the full image field is not frequently performed as instantaneous operations. For example, information from, e.g., a pointing device (= mouse or the like) need only be displayed at a speed of
10 30 Hz or less. If the speed is higher than the speed of 30 Hz, human eyes cannot catch the movement of the cursor. Similarly, if the speed of smooth scroll (scroll of each line) which requires a display of the
15 highest speed is too high, human eyes cannot catch the scrolled contents. Scrolling is often performed not in units of lines but characters in practice, or performed in units of blocks. The scroll function is often used in document editing in a computer system. Scrolling
20 does not aim at smooth scrolling but at a shift from one line to another line. In this sense, a sufficient scroll speed is 10 lines/sec in units of lines in practice.

When a mouse font has a 32 x 32 dot format and
25 partial update scan for the FLCD is performed in accordance with non-interlaced scan, the following response speed can be obtained:

$$1 \quad 32 \text{ lines} \times 100 \text{ } \mu\text{sec/line} = 3.2 \text{ msec}$$

$$\approx 312 \text{ Hz} \quad \dots (1)$$

Line scrolling at 10 lines/sec corresponds to an image update speed at a non-interlaced scan frequency of 10 Hz. Although flickering occurs at a frequency of 10 Hz, strictly speaking, a change in movement of information in units of lines is larger than the magnitude of flickering, thus posing no practical problems. The number of scan lines to be non-interlaced scanned during scrolling in units of lines is given as follows:

$$(1/10 \text{ Hz})/100 \text{ } \mu\text{sec} = 1,000 \text{ (lines)} \quad \dots(2)$$

According to the present invention, a data format consisting of the image information having scan line address information and the communication sync means 15 using the signal SYNC are used to realize a liquid crystal display apparatus based on the partial update scan algorithm in the graphic controller to be described below.

20 The image information is generated by the graphic controller 102 in the main unit and is transferred to the display panel 103 by the signal transfer means shown in Figs. 1A and 2. The graphic controller 102 uses a CPU (Central Processing Unit to be referred to as a GCPU 25 112 hereinafter) and a VRAM (image information memory) 114 to control management and communication between a host CPU 113 and the liquid crystal display device 101.

1 The control method of the present invention can be
mainly realized by the graphic controller 102.

Fig. 9A shows a partial update algorithm in a
two-line simultaneous drive mode. Display information
5 (e.g., a pointing device and a pop-up menu) necessary
for partial update on the ferro-electric liquid crystal
display device is registered in a graphic microprocessor
beforehand. When partial update of information from the
host CPU 113 is required, the partial update routine is
10 started.

In the partial update routine, a scan line address
(i.e., a scan line address corresponding to the last
scan in refresh scan prior to partial update or in
partial update scan for performing an intrawindow scroll
15 display) prior to routine branching, and a remaining
scan line count are stored in a register prepared
beforehand in the graphic microprocessor. These data
are used to restore the normal refresh routine or the
partial update for the intrawindow scroll display.
20 Partial update image information is stored in the VRAM
114. In this case, the host CPU 113 is allowed to
access the VRAM 114 through the graphic microprocessor
112. The storage state address and a storage area of
the partial update image information in the VRAM 114 are
25 managed by the graphic microprocessor 112. Upon
completion of storage of the image information in the
VRAM 114, access to the VRAM 114 is inhibited to check

1 that the previously saved scan line address is different
from the partial update start scan line address. In
this case, since the two-line scan is performed [while
the Nth scan line is driven for write access, the
5 (N+ α)th ($\alpha > 1, 2, \dots$) scan line is driven for erasure],
the partial update start scan line address is
decremented or incremented by one so as to prevent the
information on the same line from being continuously
transmitted if the scan line addresses are the same.
10 Transfer of image information to the ferro-electric
liquid crystal display device 101 is started. While the
graphic microprocessor 112 monitors a request of high
priority partial update, it transfers one-line partial
update image information in the form complying with the
15 above signal transfer scheme. At the end of image
transfer in the partial update mode, the graphic
microprocessor 112 checks that the scan line address
saved at the start of partial update is different from
the scan line address of the partial update last line,
20 thereby allowing access of the VRAM 114 and hence
completing the partial update routine.

When the two-line simultaneous drive waveform is
used to increase the frame frequency in the
ferro-electric liquid crystal display device 101, the
25 graphic microprocessor monitors the transfer scan line
address within the partial update routine, thereby
preventing continuous transfer of image information on

1 the same scan line address.

Fig. 5A is a block diagram of the graphic
controller 102, Fig. 6 is a block diagram of a digital
interface, and Figs. 7 and 8 are timing charts of
5 information transfer.

The graphic controller 102 used in the present
invention is greatly different from a conventional
controller in that a graphic processor 501 has its own
system memory 502, and performs execution and management
10 of a drawing instruction for a RAM 503 in addition to
management of the RAM 503 and a ROM 504, and information
transfer from a digital interface 505 to the FLCD
controller and management of a drive method of the FLCD
can be independently programmed.

15 The digital interface 505 shown in Fig. 6 sends
information from the VRAM in the form of 5 bits/clock
(clock = data transfer clock) in the last stage in
synchronism with the drive circuits 104 and 105 of the
display panel 103 in response to an external sync signal
20 HSYNC/VSYNC from the FLCD controller 111. Fig. 7 shows
timings of full image field update of the FLCD.

Parameters in Fig. 7 are the same as those in the timing
chart of information transfer of Fig. 7. One-line image
information transfer is started when the signal HSYNC
25 (Fig. 8) becomes active (low level in this case, i.e.,
active low). The signal HSYNC is set at low level by
the FLCD controller 111, and the signal HSYNC of low

1 level represents an information request from the panel
103. The information request from the panel 103 is
received by the graphic processor 501 in Fig. 5 and is
processed herein at timings shown in Figs. 8A to 8I. In
5 the timing charts of Figs. 8A to 8I, the signal $\overline{\text{HSYNC}}$ of
the information request from the panel 103 is sampled
within one period (in other words, a low interval of a
signal VCLK) of an external video clock (CLKOUT) (in this
case, the signal VCLK is actually input to the graphic
10 processor 501, and the processor 501 samples during the
low interval). A horizontal counter HCOUNT of the
processor 501 is cleared after a lapse of 2.5-clock
interval of the signal VCLK. The parameters HESYNC and
HEBLNK in Fig. 7 are programmed to disable (high level)
15 a signal $\overline{\text{HBLNK}}$ of Fig. 7 and Figs. 8A to 8I prior to
HCOUNT = 1. In the circuit of Fig. 6, a signal DATEN
goes active (high) after a lapse of a 1/2-clock interval
of the signal VCLK, as shown in Figs. 8A to 8I. After a
further lapse of a 1/2-clock interval, i.e., after a lapse
20 of a 4.5-clock interval judging from sampling of the
signal $\overline{\text{HSYNC}}$, the next one-line data is transferred from
the VRAM to the FLCDC controller 111 every 4 bits.

Line information transferred in this case is
transferred, as indicated in the lower right portion of
25 Figs. 8A to 8I. More specifically, scan line address
information (i.e., corresponding to a scan line number)
is sent every 4 bits, and then the original one-line

1 display information is transmitted. In this case, the
FLCD controller 111 uses the signal AH/DL to distinguish
the scan line address information from the display
information. When the signal AH/DL is set at high
5 level, it represents the scan line address information.
However, when the signal AH/DL is set at low level, it
recognizes the display information. Therefore, the FLCD
selects a scan line in accordance with the scan line
address information and is written with the display
10 information. When the scan line address information
from the graphic controller of Fig. 5A is sent upon
being incremented by one, the FLCD is driven by
interlaced scan when the number of scan lines is
incremented every other number, or the FLCD is driven by
15 m-line multi-interlaced scan when the number of scan
lines is incremented every m lines. Therefore, the
drive method of the display can be controlled.

Fig. 9B shows another partial update algorithm
according to the present invention. The corresponding
20 system of the present invention is shown in Fig. 1B.
The arrangement shown in Fig. 1B is obtained by adding a
timer 115 to the system shown in Fig. 1A.

In this partial update routine, the scan line
address prior to branching (generation of a request of
25 high priority partial update, i.e., (A)) shown in
Fig. 9B and a remaining scan line count are saved in a
register prepared beforehand in a GCPU 112 as

1 information for restoring a normal refresh routine after
the end of partial update. The partial update image
information is stored in a VRAM 114. In this case, a
host CPU 113 is allowed to access the VRAM 114 only
5 through the GCPU 112. The storage state address and the
storage area of the partial update image information are
managed by the GCPU 112.

At the end of storage of the image information in
the VRAM 114, in order to synchronize storage of the
10 image information in the VRAM 114 with partial update
scan of the display panel 103, the number of partial
update scan lines is set in a timer 115. The timer
counts down the set number of partial update scan lines.
When the count reaches the set number of partial update
15 scan lines, an interrupt is sent to the GCPU 112. The
GCPU 112 inhibits or allows access of the VRAM 114 in
accordance with types of graphic events of the image
information until the interrupt is generated from the
timer 115. When an access of the VRAM 114 is inhibited,
20 transfer of the image information to a drive control
circuit 111 is started in units of lines in the form
complying with the above signal transfer scheme. When a
request of high priority partial update is not
generated, the image information is transferred to the
25 drive control circuit 111 until an interrupt
representing the end of partial update scan is generated
by the timer 115. When transfer of the partial update

1 information is completed, the GCPU 112 allows access of
the VRAM 114 to restart refresh driving.

When an access of the VRAM 114 is allowed and a
request of high priority partial update is not
5 generated, the GCPU 112 manages and executes process
processing (e.g., storage of font information in a RAM
(not shown) except for the VRAM 114, and communication
with the host CPU 113) and image information storage
processing (e.g., scroll which does not result in a
10 failure even if information from the VRAM 114 is changed
during processing). When the interrupt from the timer
115 is received by the GCPU 112, front-layer refresh
driving is started.

In the information processing system of the present
15 invention, the partial update scan interval on the
display panel 105 is managed by controlling a scan
interval (i.e., (number of partial update scan lines) x
(horizontal scan interval)). New image information can
be stored in the VRAM 114 without interfering
20 synchronization between partial update scan under
execution and the VRAM 114 within the update interval.

When a partial update of image information occurs,
the timer 115 manages the number of partial update scan
lines to synchronize the partial update scan of the
25 panel 103 with storage of the image information in the
VRAM 114. At the same time, execution of processing in
which access of the VRAM 114 is not inhibited can be

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the VRAM 114 to restart refresh driving.

 When an access of the VRAM 114 is allowed and a
request of high priority partial update is not
5 generated, the GCPU 112 manages and executes process
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10 failure even if information from the VRAM 114 is changed
during processing). When the interrupt from the timer
115 is received by the GCPU 112, front-layer refresh
driving is started.

 In the information processing system of the present
15 invention, the partial update scan interval on the
display panel 105 is managed by controlling a scan
interval (i.e., (number of partial update scan lines) x
(horizontal scan interval)). New image information can
be stored in the VRAM 114 without interfering
20 synchronization between partial update scan under
execution and the VRAM 114 within the update interval.

 When a partial update of image information occurs,
the timer 115 manages the number of partial update scan
lines to synchronize the partial update scan of the
25 panel 103 with storage of the image information in the
VRAM 114. At the same time, execution of processing in
which access of the VRAM 114 is not inhibited can be

1 performed with the partial update. The processing speed
of the GCPU 112 can be increased.

Fig. 5B is a block diagram of the graphic
controller 102 when the partial update algorithm shown
5 in Fig. 9B is used. The graphic controller 102 used in
the present invention is greatly different from a
conventional one in that the graphic processor itself
has a system memory 402, and performs execution and
management of a drawing instruction for a RAM 403 in
10 addition to management of the RAM 403 and a ROM 404,
information transfer from a digital interface 405 to the
FLCD controller and management of the drive method of
the FLCD can be independently programmed, and the timer
115 can manage the information transfer to the FLCD
15 controller.

Fig. 11 shows a multi-window display screen 110
according to the present invention. Window 1 represents
a layer obtained by expressing a summation result in a
circle graph. Window 2 represents a layer obtained by
20 expressing the summation result of window 1 in a table.
Window 3 represents a layer obtained by expressing the
summation result of window 1 in a bar graph. Window 4
represents a layer during documentation. A mouse of a
pointing device is represented by reference numeral 5.
25 Windows 1 to 3 are kept in a still state. Assume that
document editing operations such as smooth scroll,
insertion, deletion of words and clauses, and block

1 shift are performed and the mouse 5 is moved. Smooth
scroll and mouse shift use partial update scan as
necessary information in the ferro-electric liquid
crystal display device 101. When the full image field
5 is constituted by 1,120 scan lines and is scanned with
one horizontal scan time of 80 μ s, the frame frequency
becomes about 10 Hz, which cannot cope with normal mouse
movement ($\geq$ 30 Hz). However, when the algorithm of the
present invention is applied to give higher priority to
10 the partial update by the mouse shift than document edit
operations on window 4, the mouse partial update routine
is initialized upon mouse shift during scrolling, and a
mouse write operation is started. At this time, the
time required for branching the program into the mouse
15 partial update routine is a maximum of one horizontal
scan interval. For example, as exemplified in equation
(1), when a font size of the mouse has a 32 x 32 dot
matrix, a period required for writing a mouse on the
display panel 103 becomes 3.2 msec. During this period,
20 the scroll operation is disabled. However, this period
is very short not to adversely affect the scroll speed.
After the mouse is written, the partial update scan of
window 4 is restored. When a mouse shift request is
generated again, the main flow is immediately branched
25 into the mouse partial update routine, and the mouse is
written. In this manner, in a display device having a
memory function such as the ferro-electric liquid

1 crystal display device 101 and driven at a low frame
frequency, the partial update priority is set such that
the shift of the pointing device (mouse) has the top
priority, thereby realizing the multi-window, multi-task
5 display function.

The drive interval of one scan line in the FLCDD is
generally about 100 μ sec. If the drive interval of one
scan line is given as 100 μ sec and a minimum frequency
free from flickering is given as 30 Hz, no flickering
10 occurs as a still image with the following numbers of
scan lines (scan and drive):

For non-interlaced scan scheme:

$$(1/30 \text{ Hz})/100 \text{ } \mu\text{sec} \cong 333 \text{ (lines)} \quad \dots(3)$$

For interlaced scan scheme:

15 $(1/30 \text{ Hz}) \times 2/100 \text{ } \mu\text{sec} \cong 666 \text{ (lines)} \quad \dots(4)$

For m-line multi-interlaced scan scheme:

$$(1/30 \text{ Hz}) \times m/100 \text{ } \mu\text{sec} \cong 333 \times m \text{ (lines)} \quad \dots(5)$$

According to experiments of the present inventor,
20 it was found that no flickering occurred for $m = 32$.
That is, if the display panel 103 has the following
number of scanning lines:

$$(1/30 \text{ Hz}) \times 32/100 \text{ } \mu\text{sec} \cong 333 \times 32 = 10,656 \text{ (lines)} \quad \dots(6)$$

25 a display can be free from flickering. A high-precision
flat display panel can be obtained.

"74AS161A", "74AS74", "74ALS257", "74ALS878", and

1 "74AS257" in Fig. 6 are IC numbers, and numerical values
in Fig. 6 represent pin numbers.

In a preferred arrangement of the present
invention, non-interlaced scan is used as a method of
5 scanning an intrawindow scroll display and a font
display. In addition, when a still image is to be
displayed, the multi-interlaced scan to be described
below is used. Table 2 below represents the
multi-interlaced scan, and 1°, 2°, 3°, ... N° in Table 2
10 represent codes of scan electrodes from the top to the
bottom of the screen.

Fig. 12A shows waveforms of drive signals in the
liquid crystal element of the present invention. More
specifically, a waveform a represents a selection signal
15 waveform, and information signal waveforms b and c
correspond to white image information and black image
information, respectively. In the waveform b, a phase
having a pulse width t_2 and a voltage value V_5 is a
control phase, and a phase having a pulse width t_3 and a
20 voltage value $-V_4$ is an auxiliary phase. The
information signals are constituted by the above pulses
to reduce image drawbacks such as flickering during
non-selection. The selection signal waveform a consists
of an erase phase having a pulse width t_1 and a voltage
25 value V_1 and an auxiliary phase having a pulse width t_3
and a voltage value V_3 . That is, this auxiliary phase
compensates for the auxiliary phase of the waveform b.

1 The voltage value V_3 preferably falls within the range
of $0 < V_3 < V_1$, and $|V_3| = |V_4|$ is preferably
established.

5 Pixels on a scan line selected in an erase phase
are preferably simultaneously erased to obtain a black
state.

Fig. 13 shows a time-serial waveform when a display
of Fig. 12B is performed.

10 Referring to Fig. 13, scan signal waveforms S_1 to
 S_4 correspond to scan signal lines S_1 to S_4 of Fig. 12B,
and information signal waveforms I_1 and I_2 correspond to
information signal lines i_1 and i_2 of Fig. 12B.
Composite waveforms $(I_1 - S_3)$ and $(I_2 - S_2)$ are obtained
by combining the information signal waveform I_1 and the
15 scan signal waveform S_3 and combining the information
signal waveform I_2 and the scan signal waveform S_2 ,
respectively.

The sequence in Fig. 13 is preferable since the
frame frequency can be set to be low.

20 Figs. 14A and 14B show drive waveforms of a
multi-interlaced scan drive scheme used in the present
invention. Referring to Fig. 14A, scan selection
signals S_{4n-3} , S_{4n-2} , S_{4n-1} , and S_{4n} are applied to the
($4n-3$)th, ($4n-2$)th, ($4n-1$)th, and $4n$ th scan electrodes in
25 ($4M-3$)th, ($4M-2$)th, ($4M-1$)th, and $4M$ th fields F_{4M-3} , F_{4M-2} ,
 F_{4M-1} , and F_{4M} (one field is one vertical scan interval;
 $M = 1, 2, 3, \dots$), respectively. Referring to Fig. 14A,

1 the in-phase voltage polarities (voltage polarities with
respect to the voltage of the scan non-selection signal)
of the scan selection signal S_{4n-3} are opposite to each
other. The scan selection signal S_{4n-3} is disabled
5 during scan in the $(4M-2)$ th and $4M$ fields F_{4M-2} and $4M$.
The scan selection signal S_{4n-1} is similarly set. In
addition, the scan selection signals S_{4n-3} and S_{4n-1}
applied within one field interval have different voltage
waveforms, and their in-phase voltage polarities are
10 opposite to each other.

Similarly, the in-phase voltage polarities (voltage
polarities determined with reference to the voltage of
the scan non-selection signal) of the scan selection
signal S_{4n-2} are opposite to each other in the $(4M-2)$ th
15 and $4M$ th fields F_{4M-2} and F_{4M} . At the same time, the
scan selection signal S_{4n-2} is disabled during scan for
the $(4M-3)$ th and $(4M-1)$ th fields F_{4M-3} and F_{4M-1} . The
scan selection signal S_{4n} is similarly set. The scan
selection signals S_{4n-2} and S_{4n} applied within one field
20 interval have different voltage waveforms, and the
in-phase voltage polarities are opposite to each other.

In the scan drive waveforms shown in Fig. 14A, a
phase for disabling the entire screen (e.g., a voltage
of 0 V is simultaneously applied to all pixels
25 constituting the screen) is the third phase. The third
phase of the scan selection signal is set at a voltage
of 0 V (the same voltage level as that of the scan

1 non-selection signal).

Referring to Fig. 14B, as an information signal applied to the signal electrode in the $(4M-3)$ th field F_{4M-3} , a white signal (this signal is combined with the scan selection signal S_{4n-3} to apply a voltage $3V_0$ exceeding the threshold voltage of the ferro-electric liquid crystal at the second phase to form a white pixel) and a hold signal (this signal is combined with the scan selection signal S_{4n-3} to apply voltages $\pm V_0$ lower than the threshold voltage of the ferro-electric liquid crystal to a pixel) are selectively applied to the scan selection signal S_{4n-3} ; and a black signal (this signal is combined with the scan selection signal S_{4n-1} to apply a voltage $-3V_0$ exceeding the threshold voltage of the ferro-electric liquid crystal at the second phase to form a black pixel) and a hold signal (this signal is combined with the scan selection signal S_{4n-1} to apply voltages $\pm V_0$ lower than the threshold voltage of the ferro-electric liquid crystal to a pixel) are selectively applied to the scan selection signal S_{4n-1} . The scan non-selection signal is applied to the $(4n-2)$ th and $4n$ th scan electrodes, so that the information signals are applied thereto without changes.

As the information signals applied to the signal electrodes in the $(4M-2)$ th field F_{4M-2} following the $(4M-3)$ th field F_{4M-3} described above, the black signal and the hold signal are selectively applied to the scan

1 selection signal S_{4n-2} in the same manner as described
above, and the white signal and the hold signal are
selectively applied to the scan selection signal S_{4n} as
described above. The scan non-selection signal is
5 applied to the $(4n-3)$ th and $(4n-1)$ th scan electrodes, so
that the information signals are applied without
changes.

As information signals applied to the signal
electrodes in the $(4M-1)$ th field F_{4M-1} following the
10 $(4M-2)$ th field F_{4M-2} described above, the black signal
and the hold signal are selectively applied to the scan
selection signal S_{4n-3} as described above, and the white
signal and the hold signal are selectively applied to
the scan selection signal S_{4n-1} as described above. The
15 scan non-selection signal is applied to the $(4n-2)$ th and
 $4n$ th scan electrodes, so that the information signals
are applied without changes.

As information signals applied to the signal
electrodes in the $4M$ th field F_{4M} following the $(4M-1)$ th
20 field F_{4M-1} described above, the black signal and the
hold signal are selectively applied to the scan
selection signal S_{4n-2} as described above, and the white
signal and the hold signal are selectively applied to
the scan selection signal S_{4n} as described above. The
25 scan non-selection signal is applied to the $(4n-3)$ th and
 $(4n-1)$ th scan electrodes, so that the information
signals are applied without changes.

1 Figs. 15A, 15B, and 15C are timing charts obtained
when a display state of Fig. 15D is obtained by the
drive waveforms shown in Figs. 14A and 14B. A hollow
dot in Fig. 15D represents a white pixel, and a solid
5 dot represents a black pixel. I1 - S1 in Fig. 15B is a
time-serial waveform of a voltage applied to an
intersection between the scan electrode S1 and the
signal electrode I1. I2 - S1 is a time-serial waveform
of a voltage applied to an intersection between the scan
10 electrode S1 and the signal electrode I2. Similarly, I1
- S2 is a time-serial waveform of a voltage applied to
an intersection between the scan electrode S2 and the
signal electrode I1. I2 - S2 is a time-serial waveform
of a voltage applied to an intersection between the scan
15 electrode S2 and the signal electrode I2.

The present invention is not limited to the drive
waveforms described above. For example, the apparatus
may multi-interlace scan every fifth, sixth, seventh,
eighth, and preferably every ninth or more scan lines.
20 The scan selection signal may have a waveform whose
polarity is inverted every field, as shown in Fig. 14A,
or may have the same waveforms in units of fields.

According to the present invention, the drive
sequence shown in Fig. 13 can be used as
25 multi-interlaced scan drive waveforms shown in Figs. 14A
to 15B.

Fig. 16 illustrates an arrangement of a

1 ferro-electric liquid crystal cell. Substrates (glass
plates) 161a and 161b are coated with transparent
electrodes such as In_2O_3 , SnO_2 or ITO (indium-tin-oxide)
films. A liquid crystal molecular layer 162 is formed
5 between the substrates 161a and 161b such that a liquid
crystal having an SmC^* phase is aligned in a direction
perpendicular to the glass surface. A thick line 163
represents a liquid crystal molecule. This liquid
crystal molecule 163 has a bipolar moment (P_L) in a
10 direction perpendicular to the molecule. When a voltage
exceeding a predetermined threshold value is applied
across the substrates 161a and 161b, a helical structure
of the liquid molecule 163 is untwisted, and all the
bipolar moments (P_L) 164 are directed toward the
15 direction of electric field, thus changing the aligning
direction of the liquid molecules 163. Each liquid
crystal molecule has an elongated shape, and the
refractive index anisotropy in the major axis is
different from that in the minor axis. When polarizers
20 are arranged on the upper and lower surfaces of the
opposite glass plates in a positional relationship of
crossed nicols, it is easily understood that the
resultant structure serves as a liquid crystal
modulation element whose optical characteristics are
25 changed by the polarities of the applied voltages. In
addition, when the thickness of the liquid crystal cell
is sufficiently small (e.g., 1μ), even it no electric

1 field is applied, the helical structure of the liquid
crystal molecule is untwisted, and the bipolar moment P_a
or P_b is directed upward (174a) or downward (174b), as
shown in Fig. 17. When an electric field E_a or E_b (the
5 fields E_a and E_b have different polarities) having a
predetermined threshold value is applied to the cell for
a predetermined period of time, the bipolar moment is
changed to direct upward 174a or downward 174b with
respect to the electric field vector of the electric
10 field E_a or E_b , as shown in Fig. 17. Therefore, the
liquid crystal molecules are aligned in a first stable
state 173a or a second stable state 173b.

There are two advantages derived from use of a
ferro-electric liquid crystal as an optical modulation
15 element. First, a response speed is very high. Second,
the alignment of the liquid crystal molecules is
bistable. The second point will be described with
reference to Fig. 17. When the electric field E_a is
applied, the liquid crystal molecules are aligned in the
20 first stable state 173a. This state is stable even if
the electric field is withdrawn. When the counter
electric field E_b is applied to the cell, the liquid
crystal molecules are aligned in the second stable state
173b. The molecular direction is changed but is kept
25 unchanged even if the electric field is withdrawn.
Unless the electric field E_a does not exceed a
predetermined threshold value, the aligning state is

1 kept unchanged. In order to effectively achieve
high-speed operation and obtain a bistable state, the
thickness of the cell is preferably minimized, and
generally falls within the range of 0.5μ to 20μ and
5 more preferably 1μ to 5μ .

As has been described above, in the information
processing apparatus using the ferro-electric liquid
crystal display device, when the two-line simultaneous
drive waveform is used to increase the frame frequency,
10 the graphic microprocessor monitors the transfer scan
line address within the partial update routine.
Therefore, continuous transfer of the image information
of the same scan line address can be prevented.

In partial update for the display device having a
15 memory function such as a ferro-electric liquid crystal
display device, there is provided a circuit for managing
partial update scan interval of the display panel of the
graphic event. The partial update can be performed
without inhibiting the VRAM access. That is, the
20 partial update scan and storage of the image information
in the VRAM can be simultaneously performed by the GCPU.
A high-speed display application can be applied to a
display device such as a ferro-electric liquid crystal
display device having a low frame frequency. As a
25 result, smooth, high-speed shift display can be
achieved.

The claims defining the invention are as follows:

1. An information processing system comprising:

a. an image information memory for storing received image information;

5 b. first control means for controlling driving of a display panel; and

c. second control means for controlling said image information memory so that storage of the image information in said image information memory is synchronized with transfer of the image information stored in
10 said image information memory to a drive control circuit.

2. An information processing system according to claim 1, said display panel having scan lines and information lines, and said second control means storing the number of scan lines subjected to scan line scan for display and counting the number of
15 scanned scan lines, thereby controlling said image information memory such that storage of the image information in said image information memory is synchronized with transfer of the image information stored in said image information memory to said first control means.

3. An information processing system according to claim 1, said display panel having scan lines and information lines, and said second control means storing the number of scan lines subjected to scan line scan for a predetermined number of scan lines and counting the number of scanned scan lines, thereby controlling said image
20 information memory such that storage of the image information in said image information memory is synchronized with transfer of the image information stored in said image information memory to said first control means.

4. A system according to either claim 2 or claim 3 wherein the stored image information consists of scan line address information for
30 designating a scan line to be selected and display information for controlling a display information signal applied to an information line of the scan line to be selected, and further comprising means for serially transferring the image information.

5. A system according to claim 4, further comprising means for
35 storing the output scan line address information.

6. A system according to either claim 2 or claim 3 wherein a highest priority display of the display priority order of the graphic events is a shift display.



7. A system according to any one of claims 1, 2 or 3, wherein said second control means comprises means for controlling said image information memory to inhibit said image information memory to store image information which is being received when a display priority of a graphic event of the image information transferred to said first control means is higher than that of the image information which is being received.

8. A system according to any one of claims 1, 2 or 3, wherein said second control means comprises means for controlling said image information memory to inhibit said image information memory to store image information which is being received when a display priority of a graphic event of the image information transferred to said first control means is higher than that of the image information which is being received, and for controlling said image information memory to interrupt transfer of the image information to said second control means and to store the image information which is being received in said image information memory when a display priority of a graphic event of the image information transferred to said first control means is lower than that of the image information which is being received.

9. An information processing system according to claim 1, further comprising:

a. first means for controlling said image information memory so that said received image information is stored in said image information memory;

b. second means for controlling said image information memory and said drive control circuit so that the image information stored in said image information memory is transferred to said drive control circuit; and

c. third means for synchronizing storage of the image information in said image information memory with transfer of the image information stored in said image information memory to said drive control circuit.

10. A system according to claim 9, wherein said third means is a timer.

11. An information processing apparatus comprising:

a. first means for receiving image information having a plurality of graphic events;

b. second means for controlling an image information memory so that received image information is stored in said image information memory in a higher priority order of the graphic events on the basis of a



preset priority order of the graphic events;

c. third means for controlling said image information memory so that the stored image information is transferred to a drive control circuit in the higher priority order of the graphic events; and

5 d. fourth means for synchronizing storage of the image information in said image information memory with transfer of the image information stored in said image information memory to said drive control circuit.

10 12. An apparatus according to claim 11, wherein said fourth means is a timer.

13. An apparatus according to claim 11, wherein the stored image information consists of scan line address information for designating a scan line to be selected and display information for controlling a display information signal applied to an information line of the scan
15 line to be selected, and further comprising means for serially transferring the image information.

14. An apparatus according to claim 13, further comprising means for storing the output scan line address information.

20 15. An apparatus according to claim 11, wherein a highest priority display of the display priority order of the graphic events is a shift display.

16. An information processing system according to claim 1, further comprising:

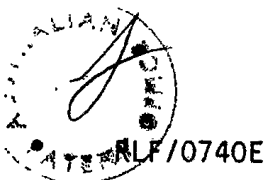
25 a. first means for controlling said image information memory so that said received image information is stored in said image information memory;

b. second means for serially receiving scan line address information for designating a scan electrode selected from said image information memory and display information for controlling a display
30 information signal applied to an information electrode on the scan electrode to be selected, and transferring the scan line address information and the display information to said drive control circuit;

c. third means for storing the scan line address information; and

35 d. fourth means for synchronizing storage of the image information in said image information memory with transfer of the image information stored in said image information memory to said drive control circuit.

17. An apparatus according to claim 16, wherein said fourth means



is a timer.

18. An apparatus according to claim 16, further comprising means for controlling said drive control circuit for separating the scan line address information and the display information.

5 19. An apparatus according to claim 16, further comprising means for synchronizing with said drive control circuit.

20. An apparatus according to claim 16, wherein the scan line address information is information for designating each scan electrode for partial update scan.

10 21. An apparatus according to claim 16, wherein the scan line address information is information for designating each of scan electrodes for performing one-frame scan.

22. An information processing system according to claim 1, further comprising:

15 a. first means for controlling said image information memory so that said received image information is stored in said image information memory and scan line address information for designating a scan line and image information corresponding to the designated scan line are output from said image information memory;

20 b. second means for controlling said image information memory and a drive control circuit so that an output from said image information memory is transferred to said drive control circuit; and

c. third means for storing first scan line address information for designating a last scan line obtained when previous scan line scan is interrupted, comparing the first scan line address information with
25 second scan line address information for designating a start scan line for new scan line scan, and decrementing or incrementing the second scan line address information when the first scan line address information is equal to the second scan line address information as a result of
30 comparison.

23. An information processing system according to claim 1, further comprising:

a. first means for controlling said image information memory so that said received image information is stored in said image information
35 memory and scan line address information for designating a scan line and image information corresponding to the designated scan line are output from said image information memory;

b. second means for controlling said image information memory and



a drive control circuit so that an output from said image information memory is transferred to said drive control circuit; and

- c. third means for storing first scan line address information for designating a last scan line of scan line scan for a predetermined number of scan lines for partial update scan, comparing the first scan line address information with second scan line address information for designating a start scan line of subsequent scan line scan for a new display, and decrementing or incrementing the second scan line address information when the first scan line address information is equal to the second scan line address information as a result of comparison.

24. An information processing system substantially as hereinbefore described with reference to the drawings.

DATED this THIRTIETH day of JUNE 1992

Canon Kabushiki Kaisha

Patent Attorneys for the Applicant
SPRUSON & FERGUSON



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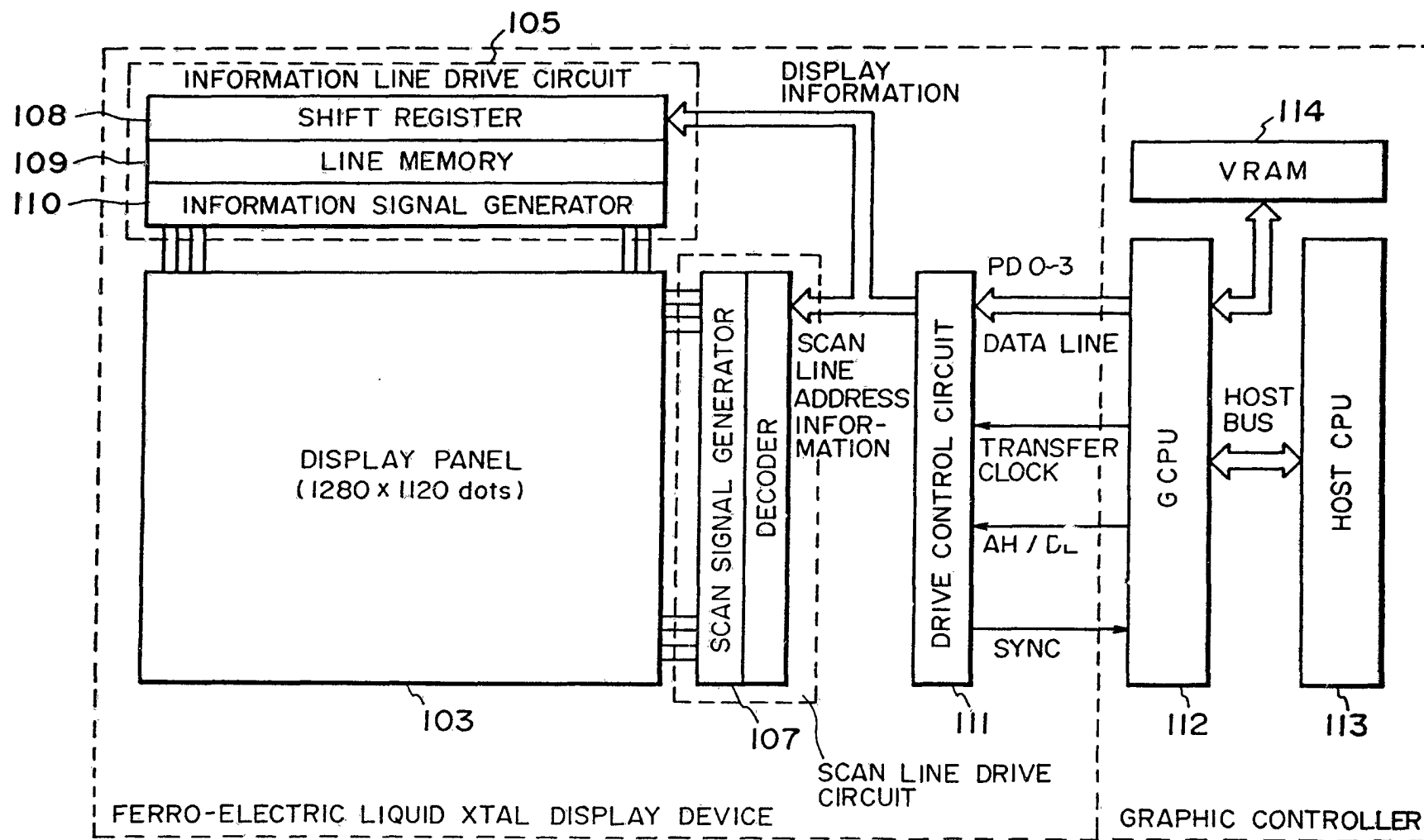


FIG. 1A

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FIG. 2A

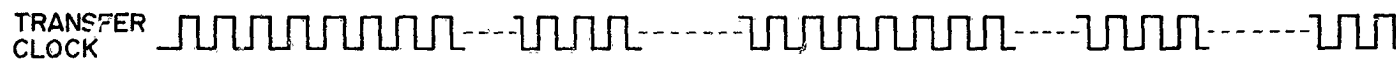


FIG. 2B



FIG. 2C

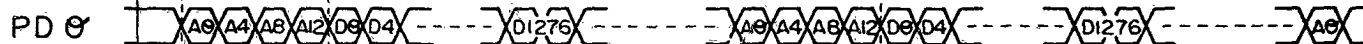


FIG. 2D



FIG. 2E

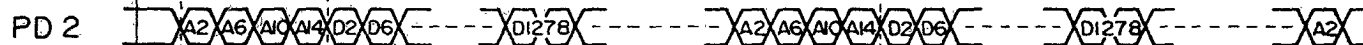


FIG. 2F

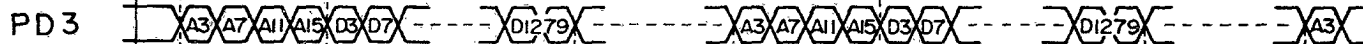
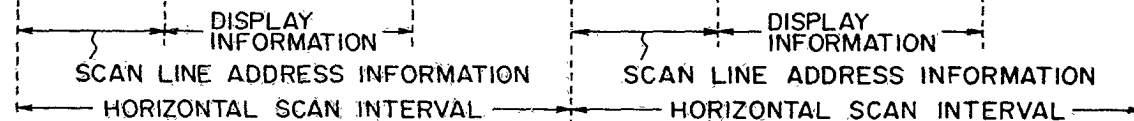
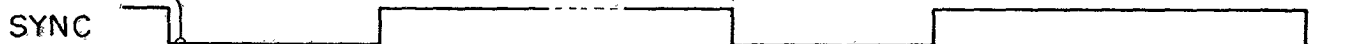


FIG. 2G



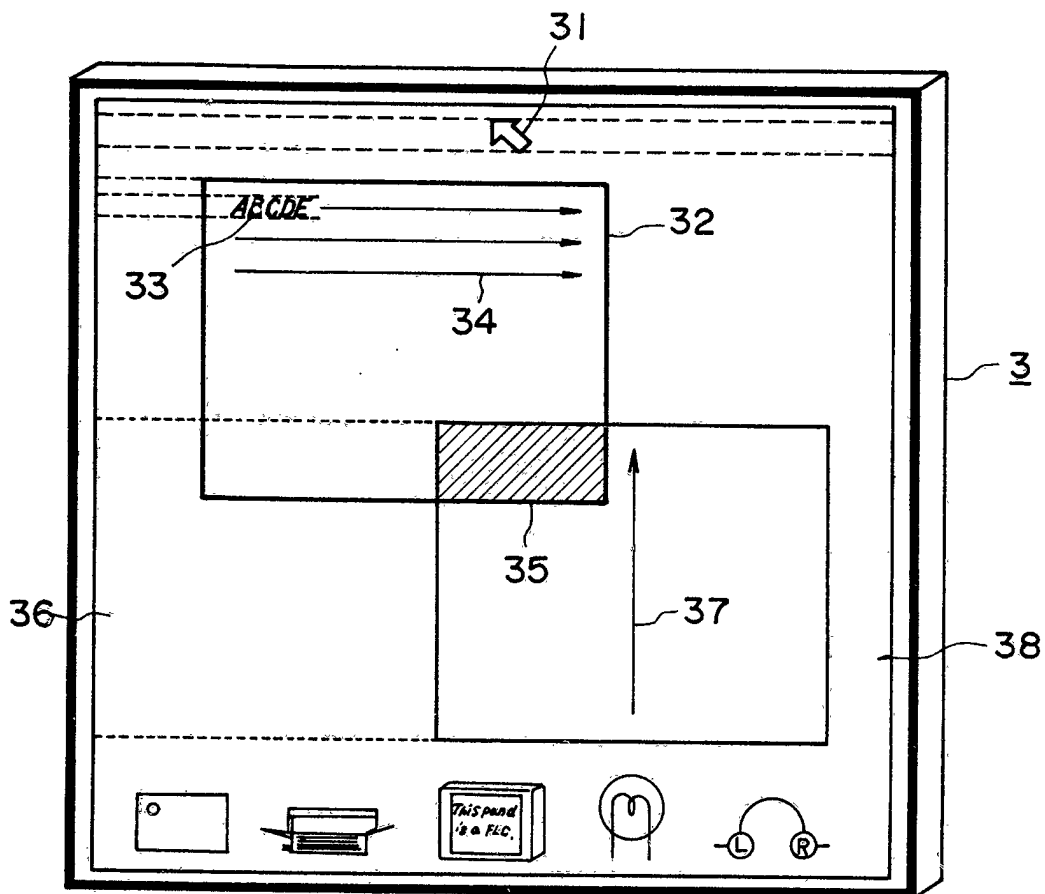


FIG. 3

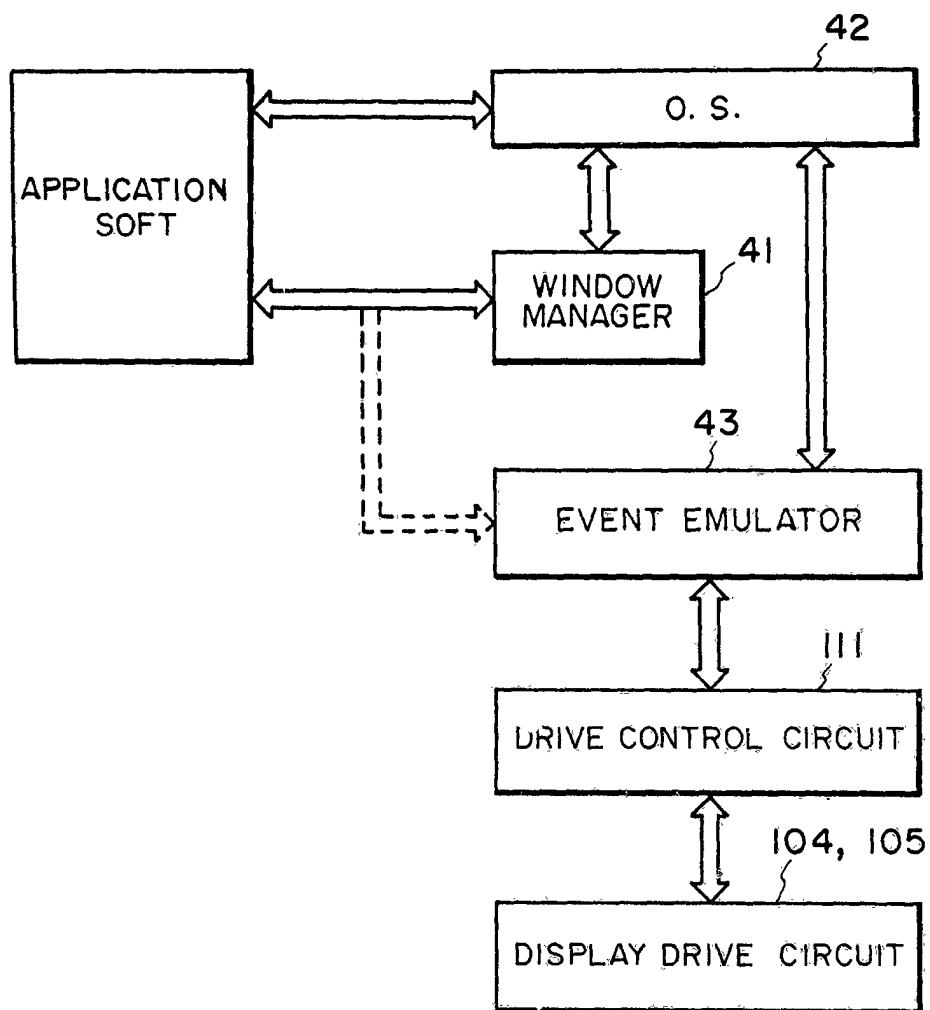


FIG. 4

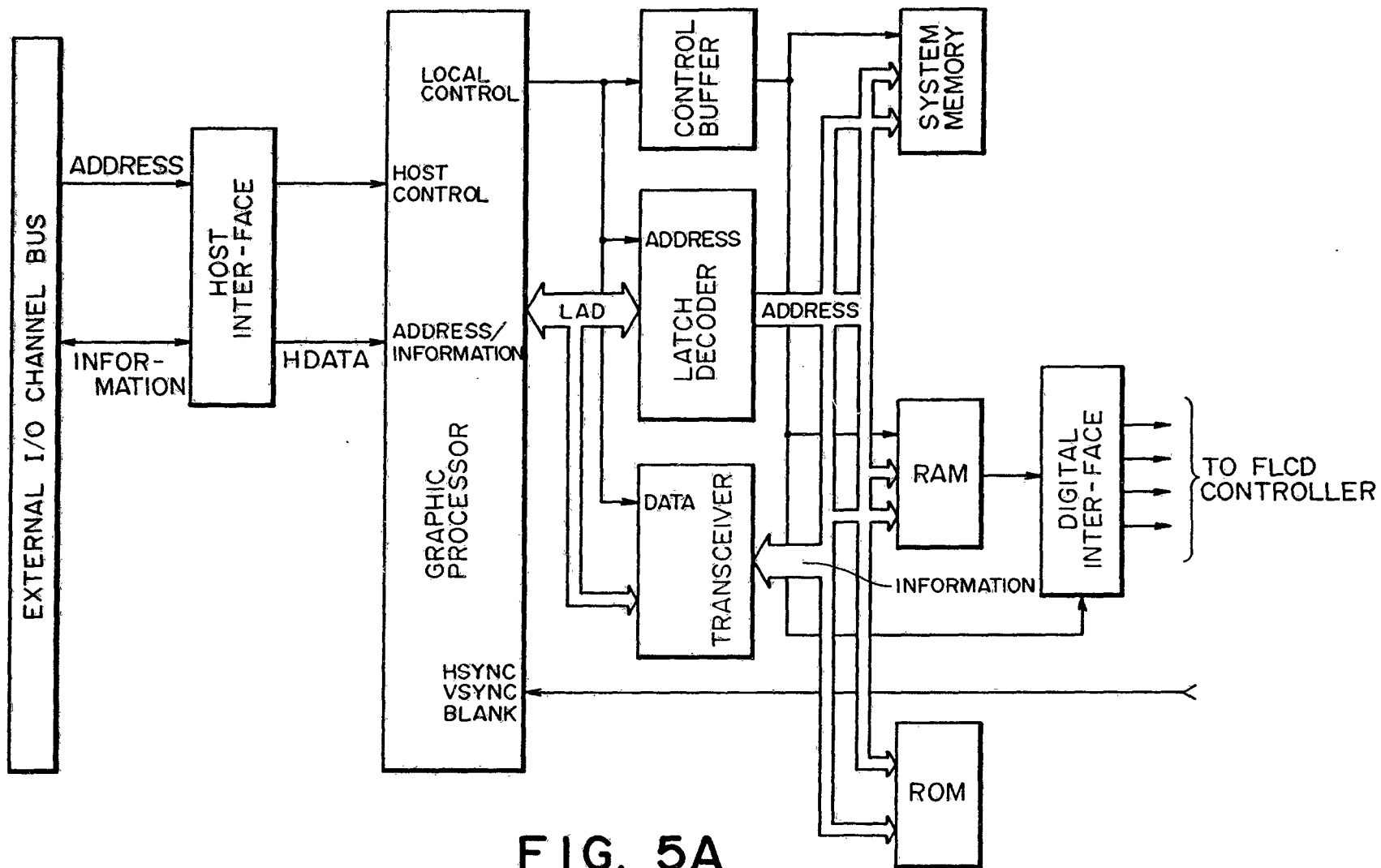


FIG. 5A

20 12 89

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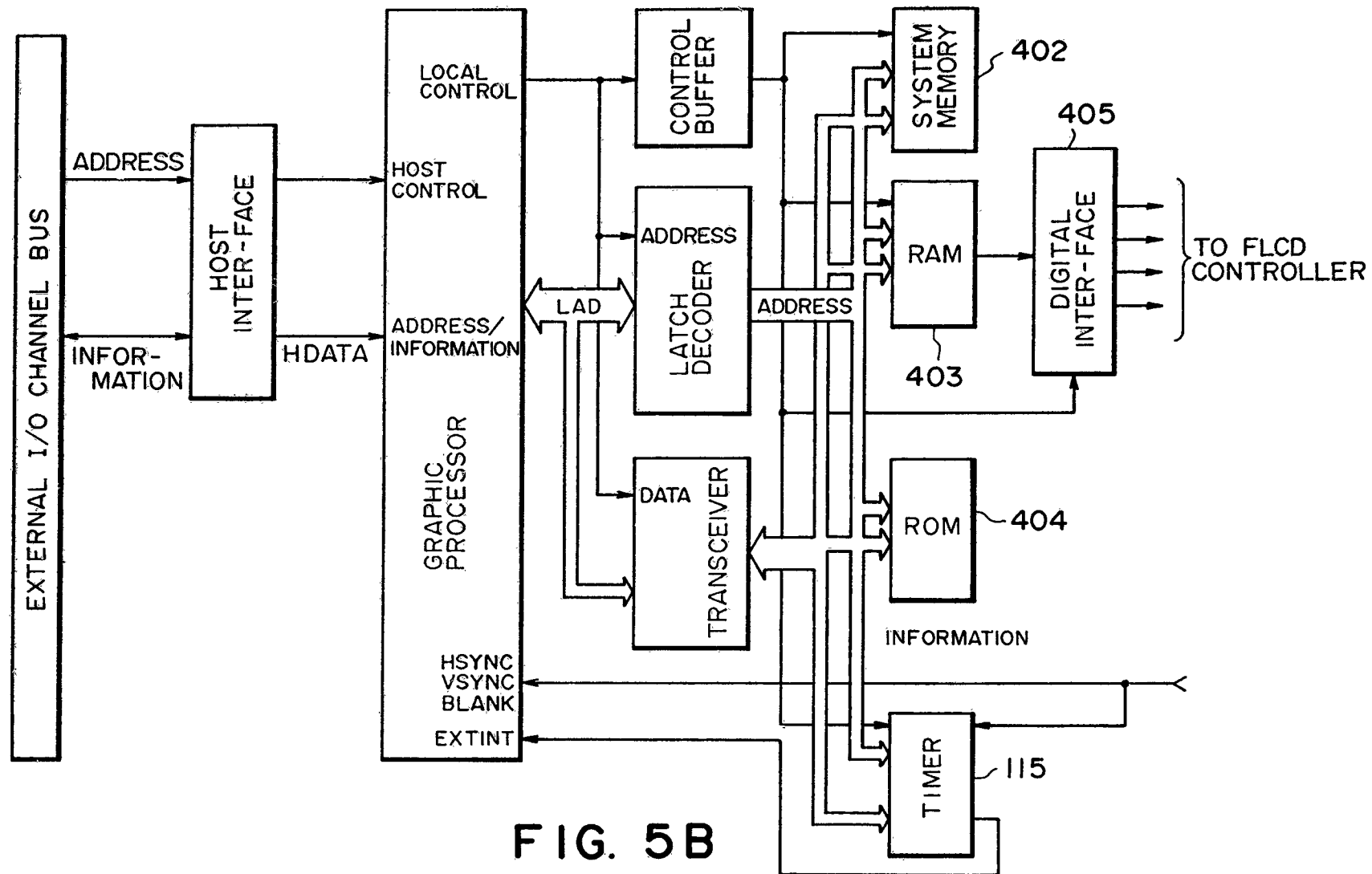


FIG. 5B

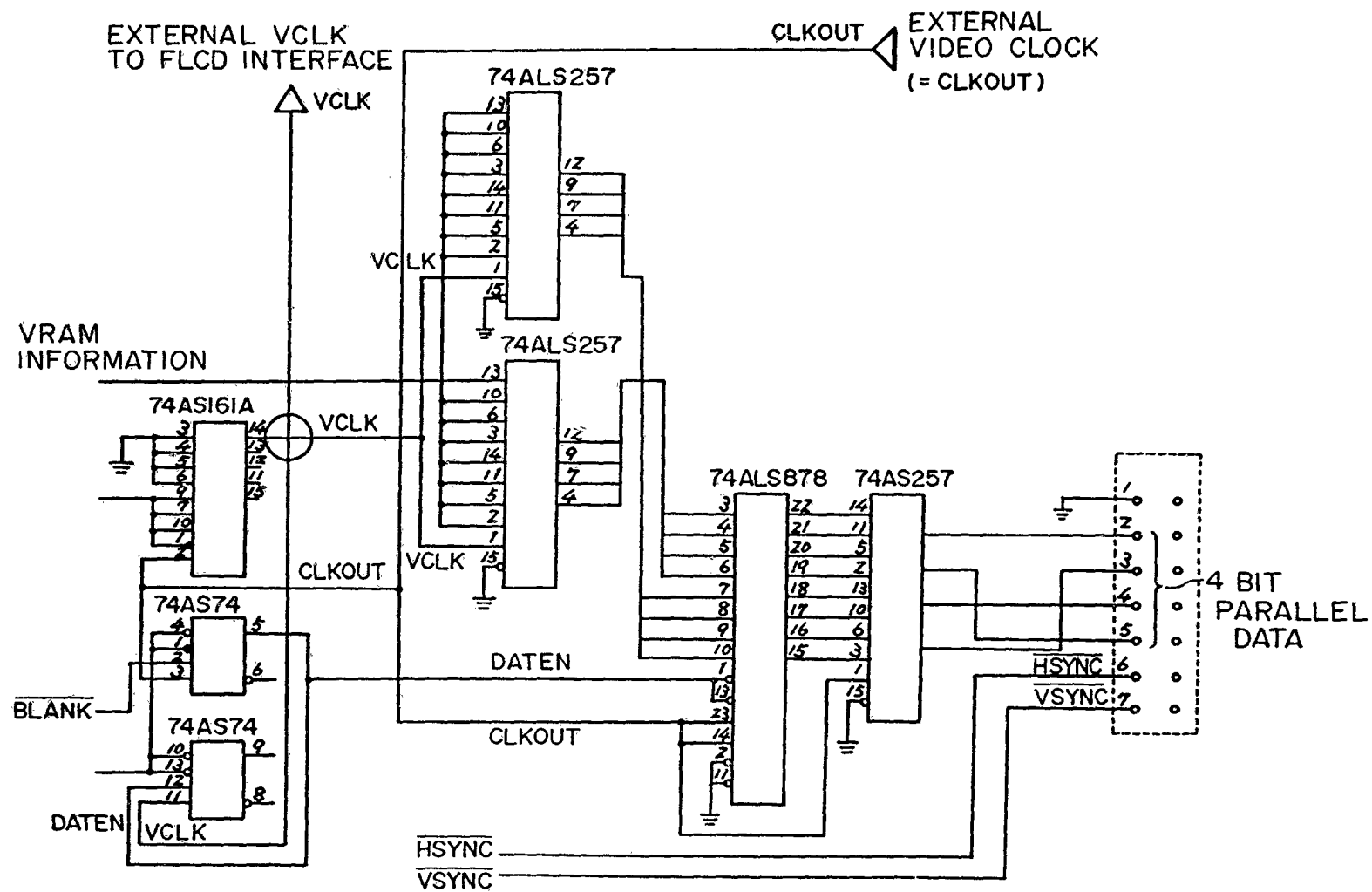


FIG. 6

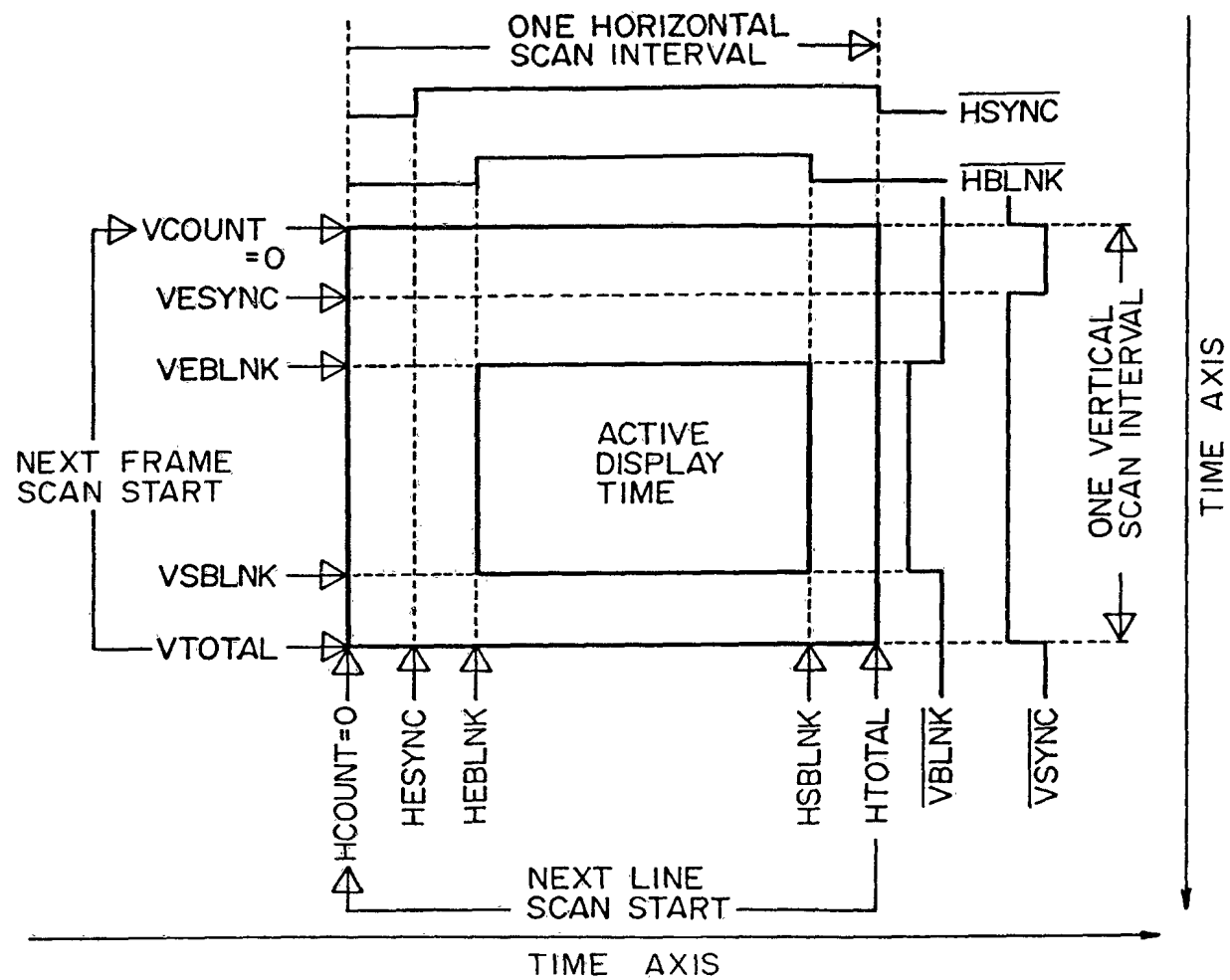


FIG. 7

FIG. 8A

FIG. 8B

FIG. 8C

FIG. 8D

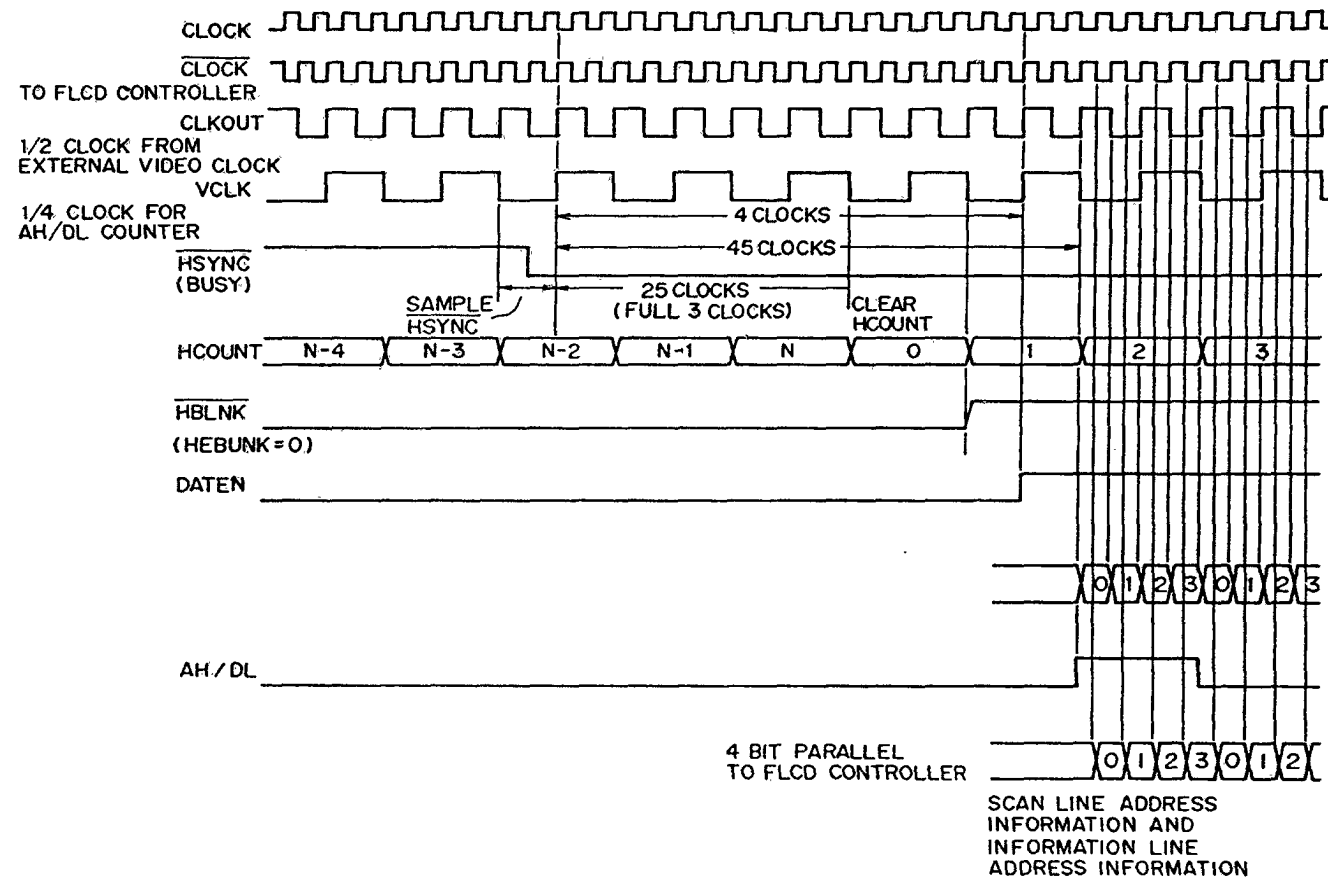
FIG. 8E

FIG. 8F

FIG. 8G

FIG. 8H

FIG. 8I



20 12 89

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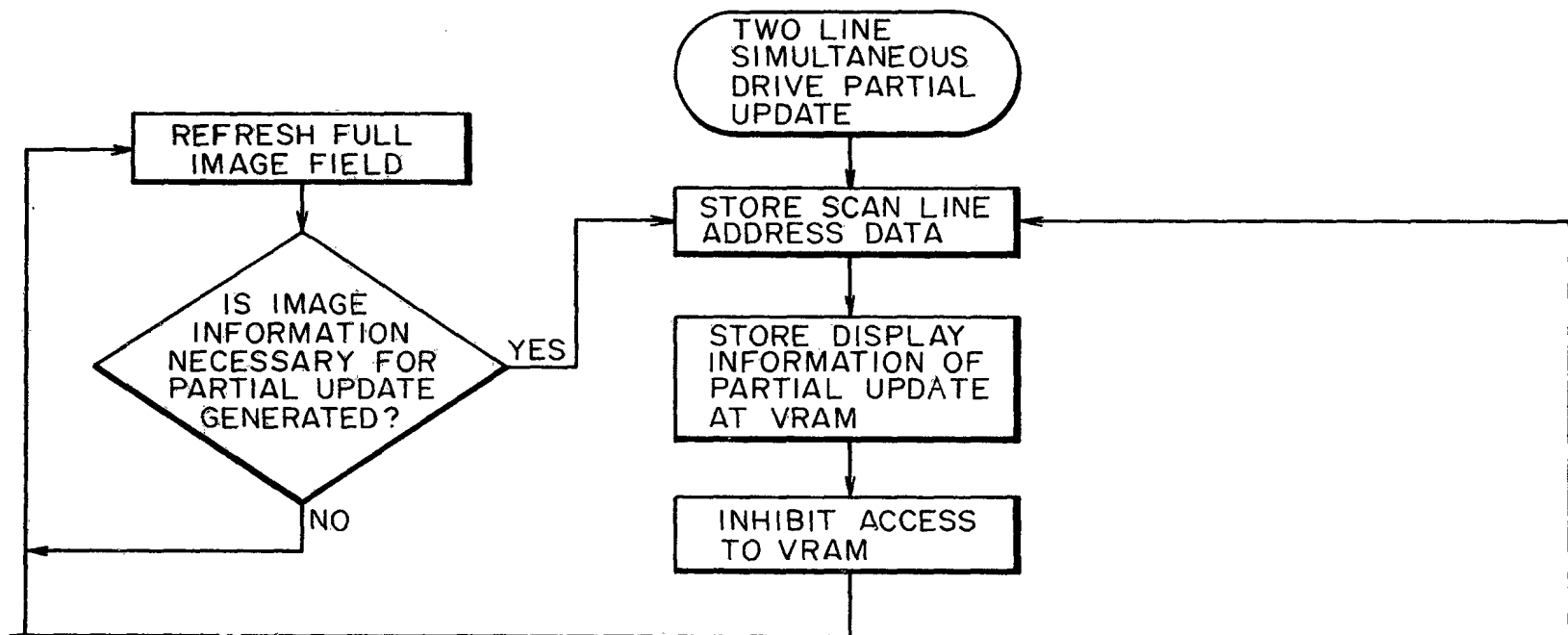


FIG. 9A-1

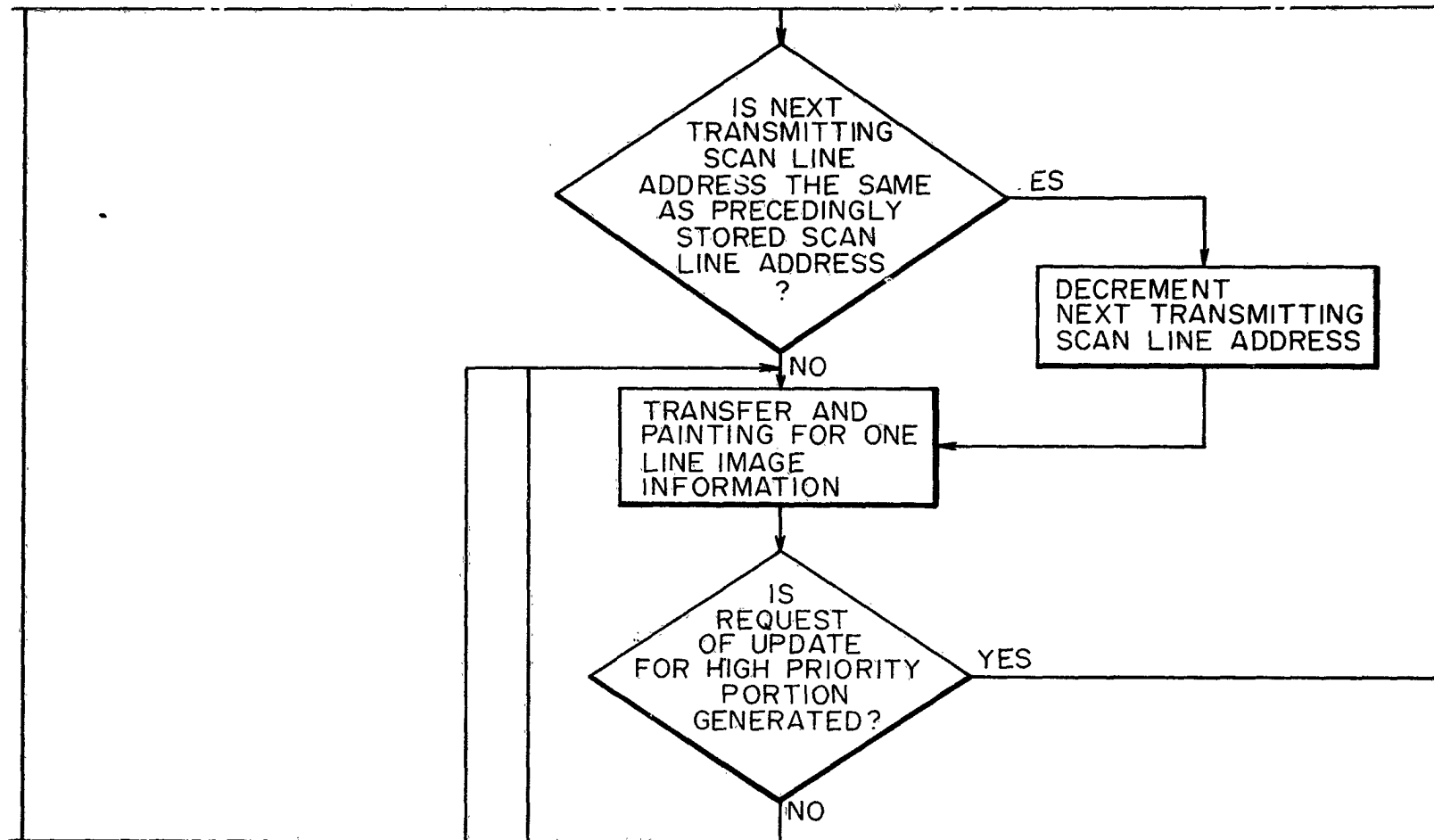


FIG. 9A-2

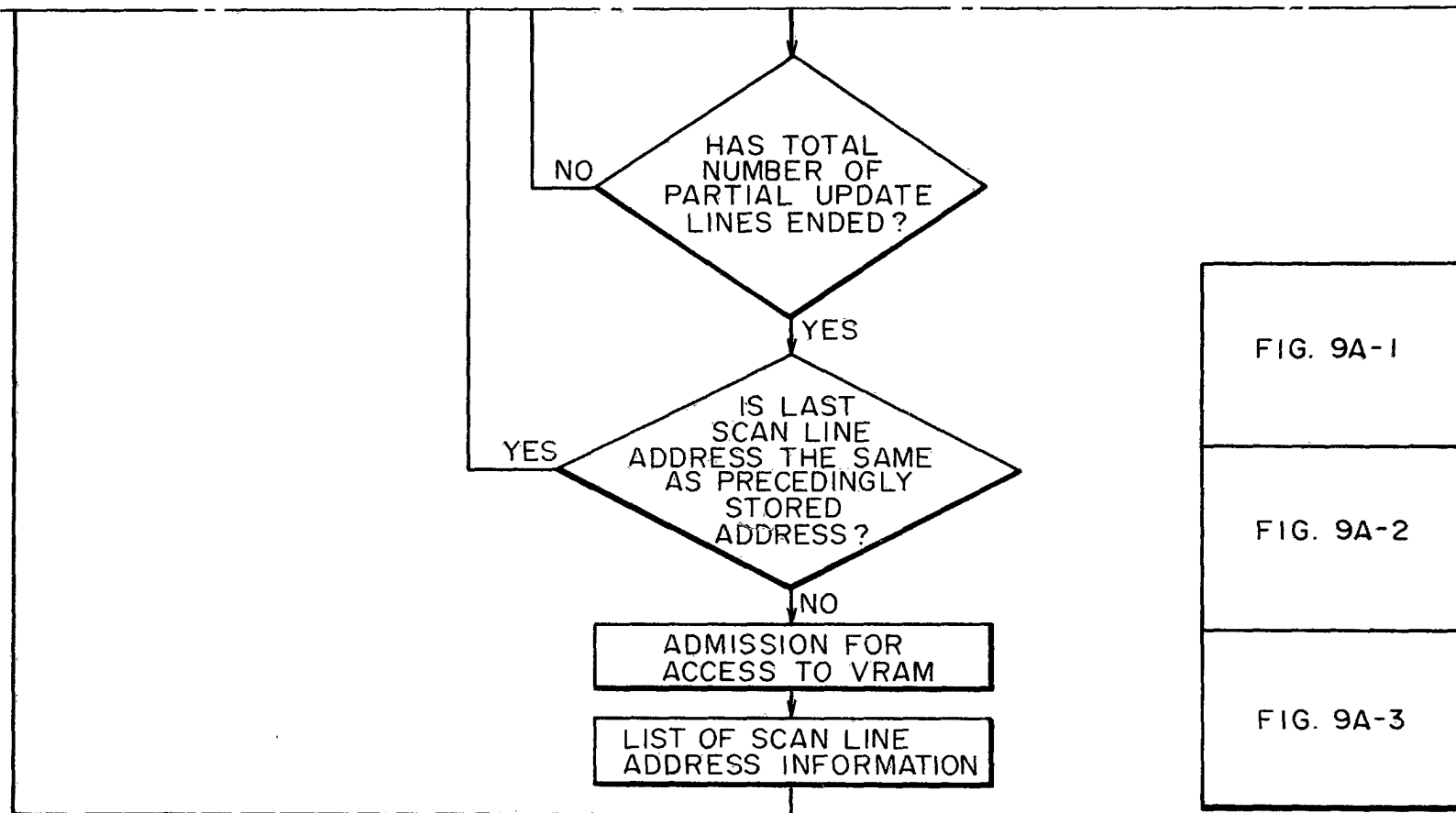


FIG. 9A-3

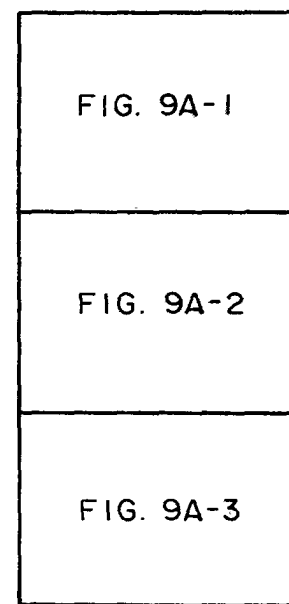


FIG. 9A

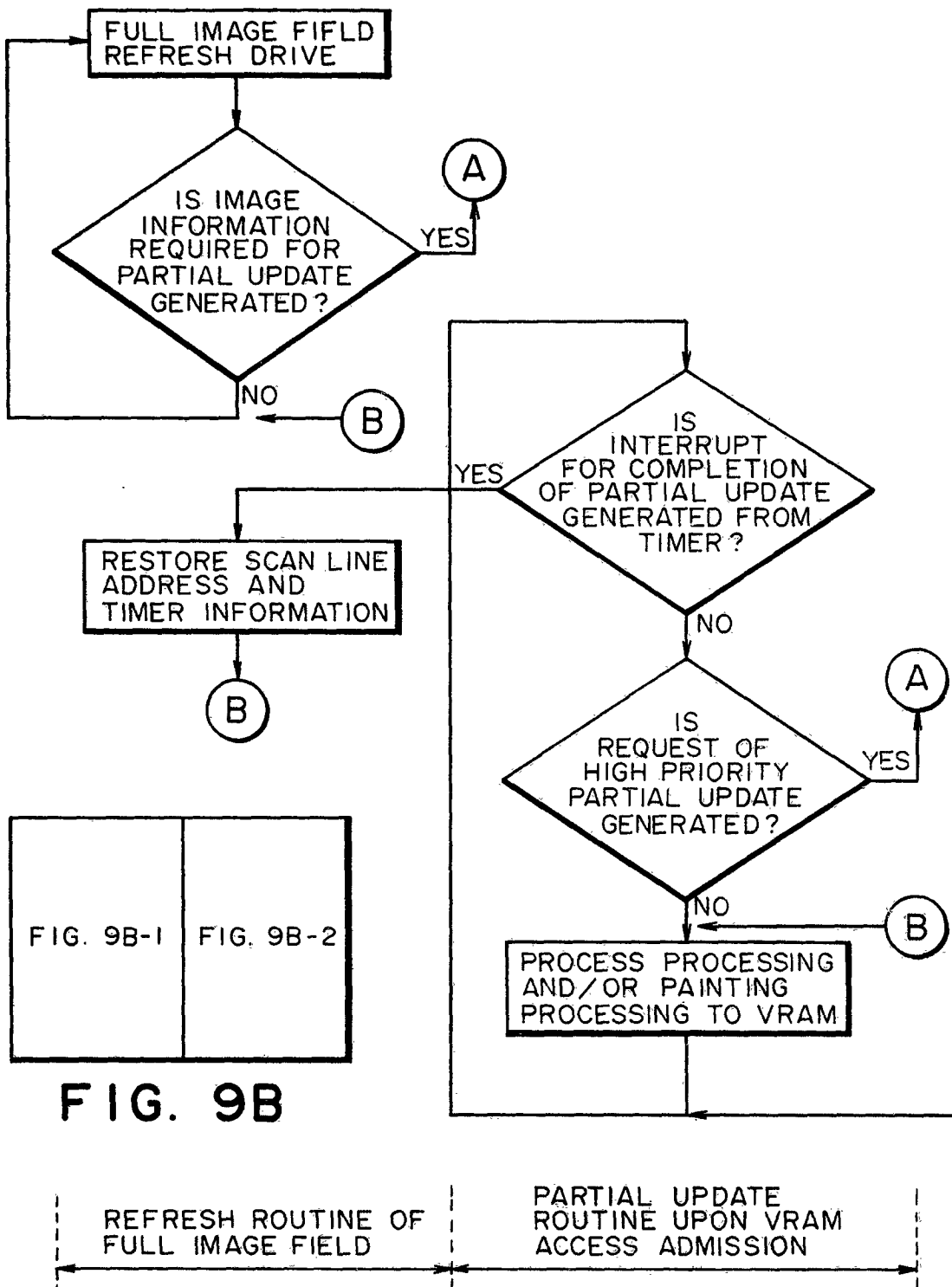


FIG. 9B-1

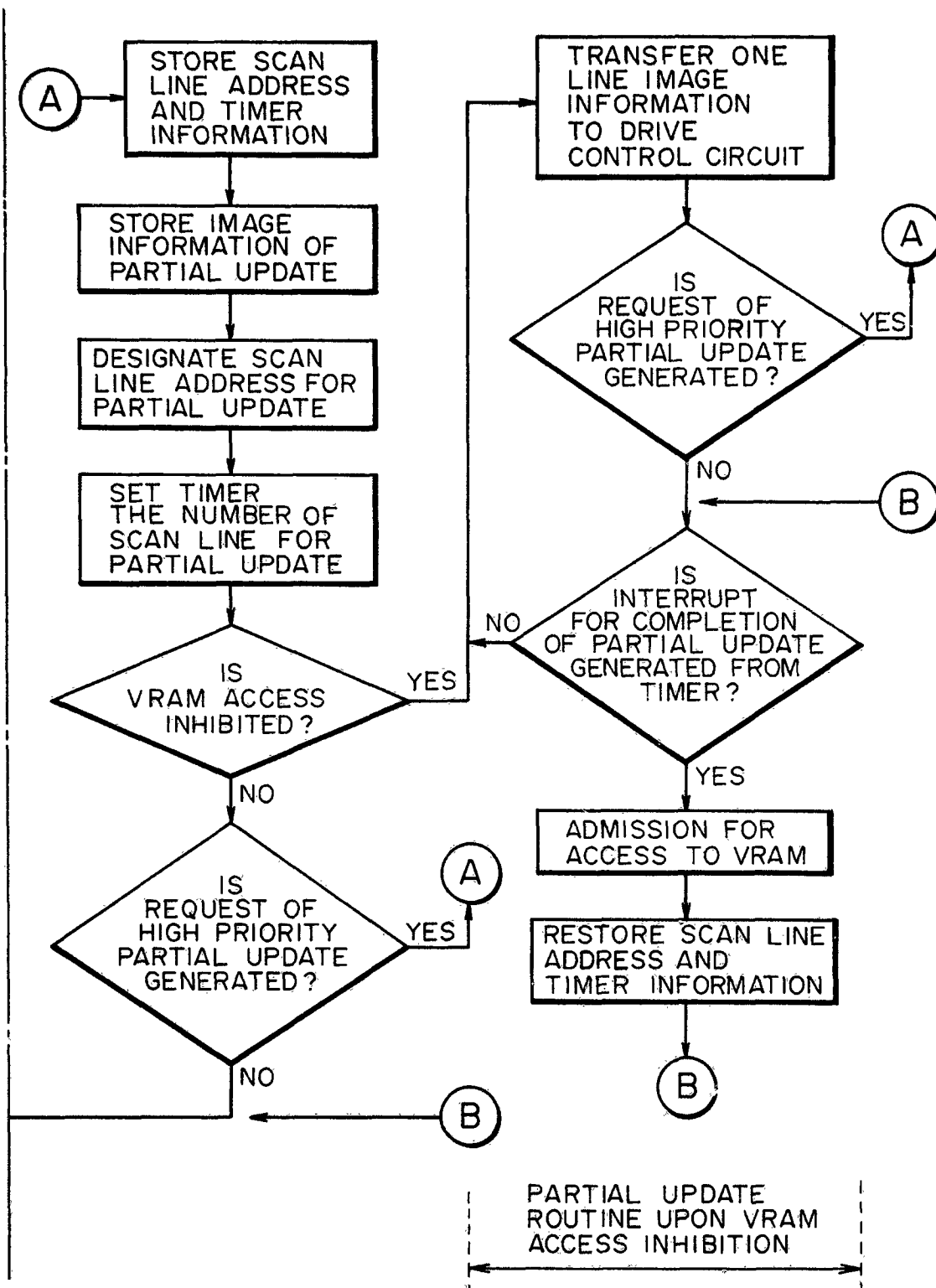


FIG. 9B-2

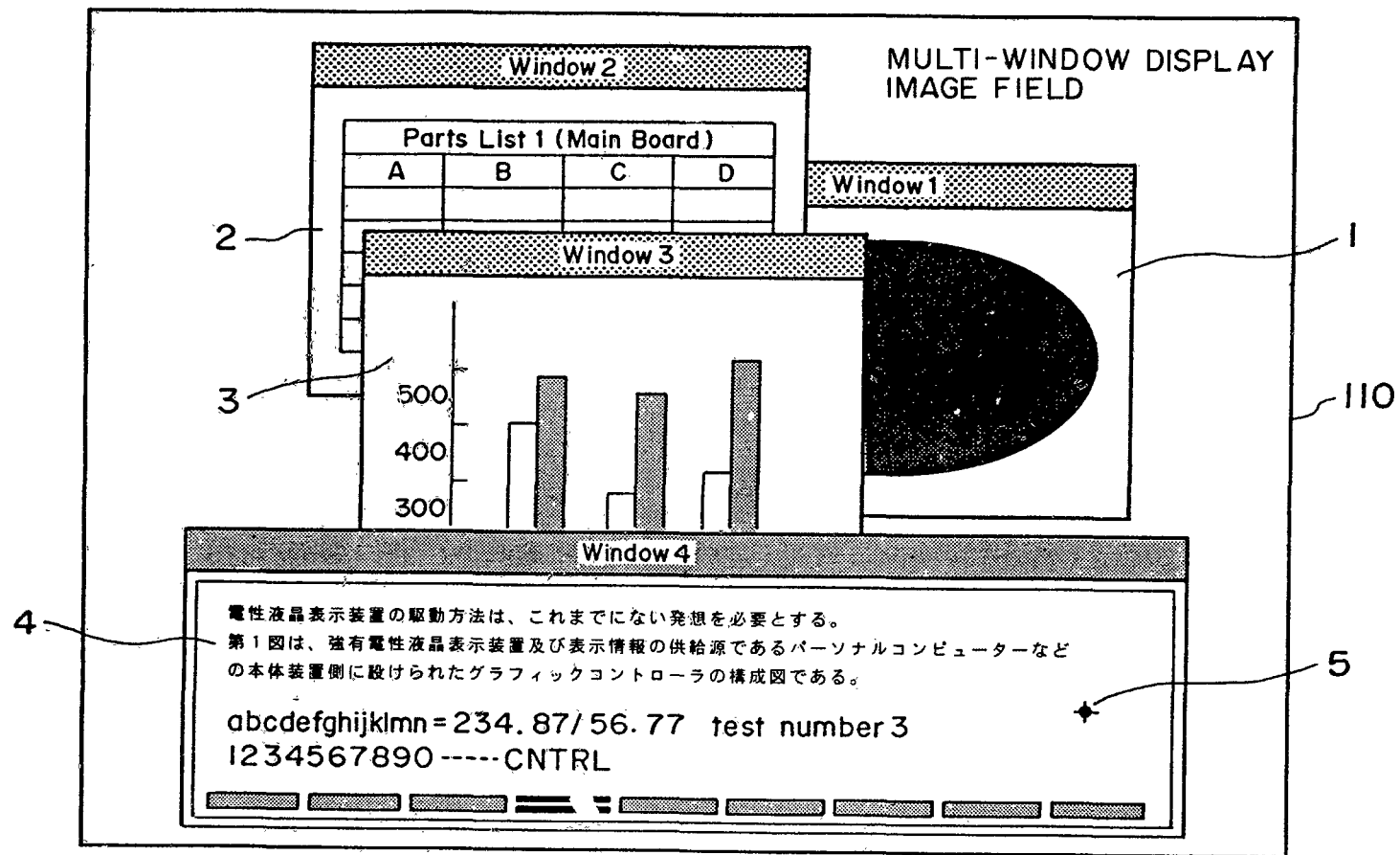


FIG. II

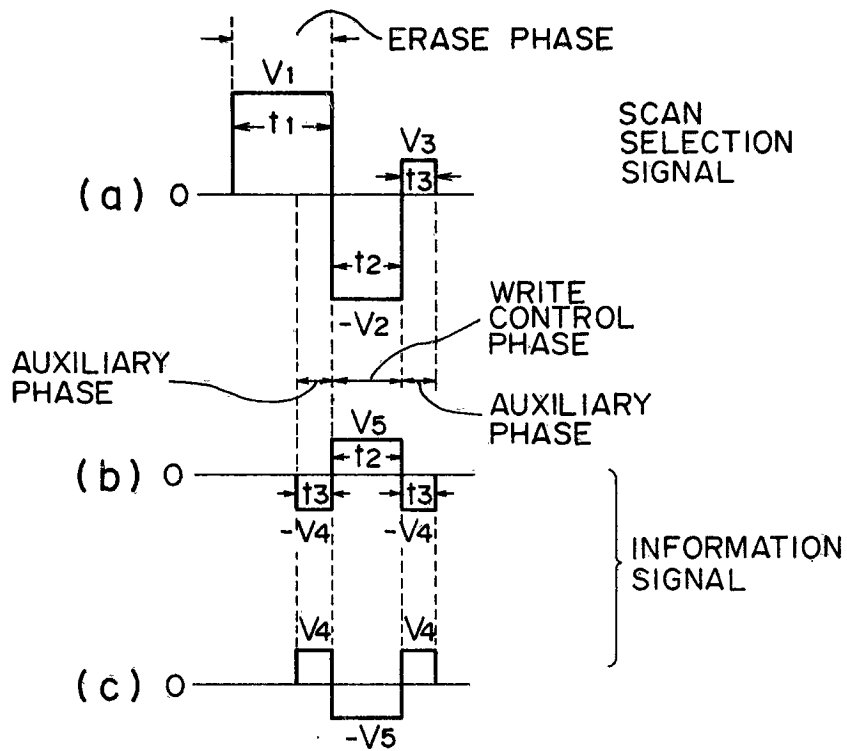


FIG. 12A

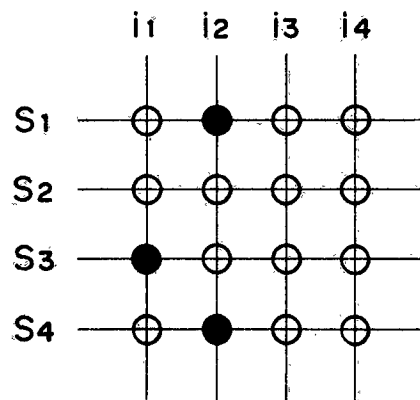


FIG. 12B

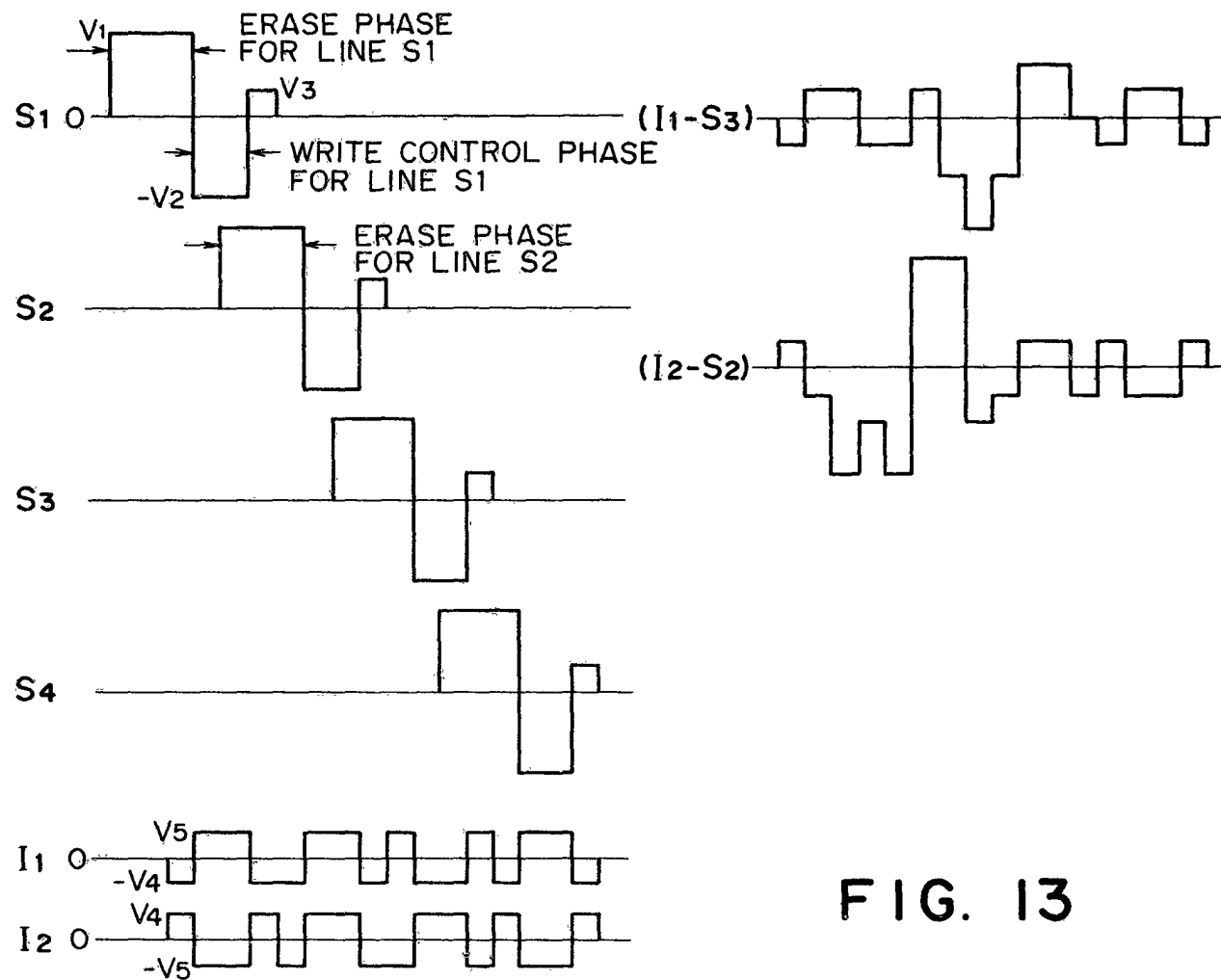


FIG. 13

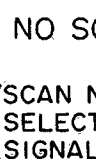
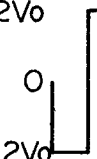
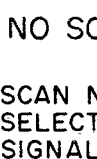
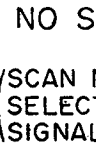
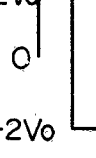
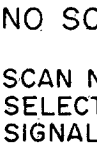
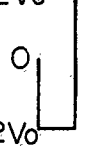
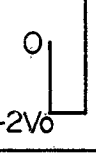
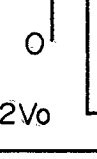
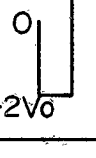
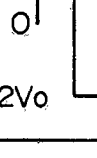
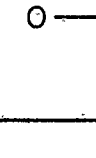
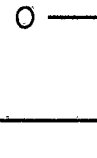
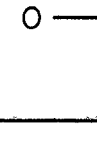
	(4M-3)FIELD F4M-3, (M=1,2,3...)	(4M-2)FIELD F4M-2, (M=1,2,3...)	(4M-1)FIELD F4M-1, (M=1,2,3...)	4M FIELD F4M, (M=1,2,3...)
SCAN SIGNAL	SCAN SELECTION SIGNAL APPLIED TO 4n-3th SCAN ELECTRODES S4n-3 (n=1,2,3,...) 	NO SCAN (SCAN NON- SELECTION SIGNAL) 		NO SCAN (SCAN NON- SELECTION SIGNAL) 
	NO SCAN (SCAN NON- SELECTION SIGNAL) 	NO SCAN (SCAN NON- SELECTION SIGNAL) 	NO SCAN (SCAN NON- SELECTION SIGNAL) 	NO SCAN (SCAN NON- SELECTION SIGNAL) 
	NO SCAN (SCAN NON- SELECTION SIGNAL) 	NO SCAN (SCAN NON- SELECTION SIGNAL) 	NO SCAN (SCAN NON- SELECTION SIGNAL) 	NO SCAN (SCAN NON- SELECTION SIGNAL) 
	NO SCAN (SCAN NON- SELECTION SIGNAL) 	NO SCAN (SCAN NON- SELECTION SIGNAL) 	NO SCAN (SCAN NON- SELECTION SIGNAL) 	NO SCAN (SCAN NON- SELECTION SIGNAL) 
	NO SCAN (SCAN NON- SELECTION SIGNAL) 	NO SCAN (SCAN NON- SELECTION SIGNAL) 	NO SCAN (SCAN NON- SELECTION SIGNAL) 	NO SCAN (SCAN NON- SELECTION SIGNAL) 
SCAN NON-SELECTION SIGNAL	0 ———	0 ———	0 ———	0 ———

FIG. 14A

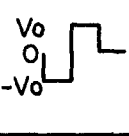
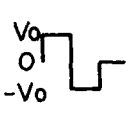
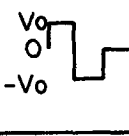
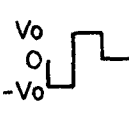
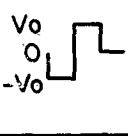
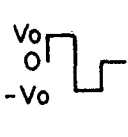
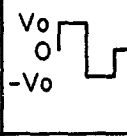
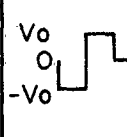
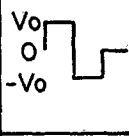
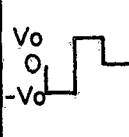
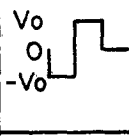
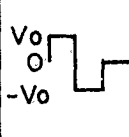
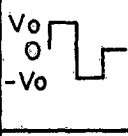
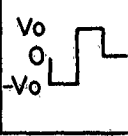
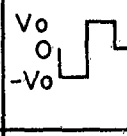
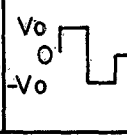
		(4M-3) FIELD F4M-3, (M=1,2,3...)	(4M-2) FIELD F4M-2, (M=1,2,3...)	(4M-1) FIELD F4M-1, M=1,2,3...	4M FIELD F4M, M=1,2,3...
INFORMATION SIGNAL	SYNCHRONIZATION WITH SCAN SELECTION SIGNAL S4n-3	WHITE SIGNAL  HOLD SIGNAL 	/		BLACK SIGNAL  HOLD SIGNAL 
	SYNCHRONIZATION WITH SCAN SELECTION SIGNAL S4n-2	/		WHITE SIGNAL  HOLD SIGNAL 	BLACK SIGNAL  HOLD SIGNAL 
	SYNCHRONIZATION WITH SCAN SELECTION SIGNAL S4n-1	BLACK SIGNAL  HOLD SIGNAL 	/		WHITE SIGNAL  HOLD SIGNAL 
	SYNCHRONIZATION WITH SCAN SELECTION SIGNAL S4n	/		BLACK SIGNAL  HOLD SIGNAL 	WHITE SIGNAL  HOLD SIGNAL 

FIG. 14B

20 12 89

4:108

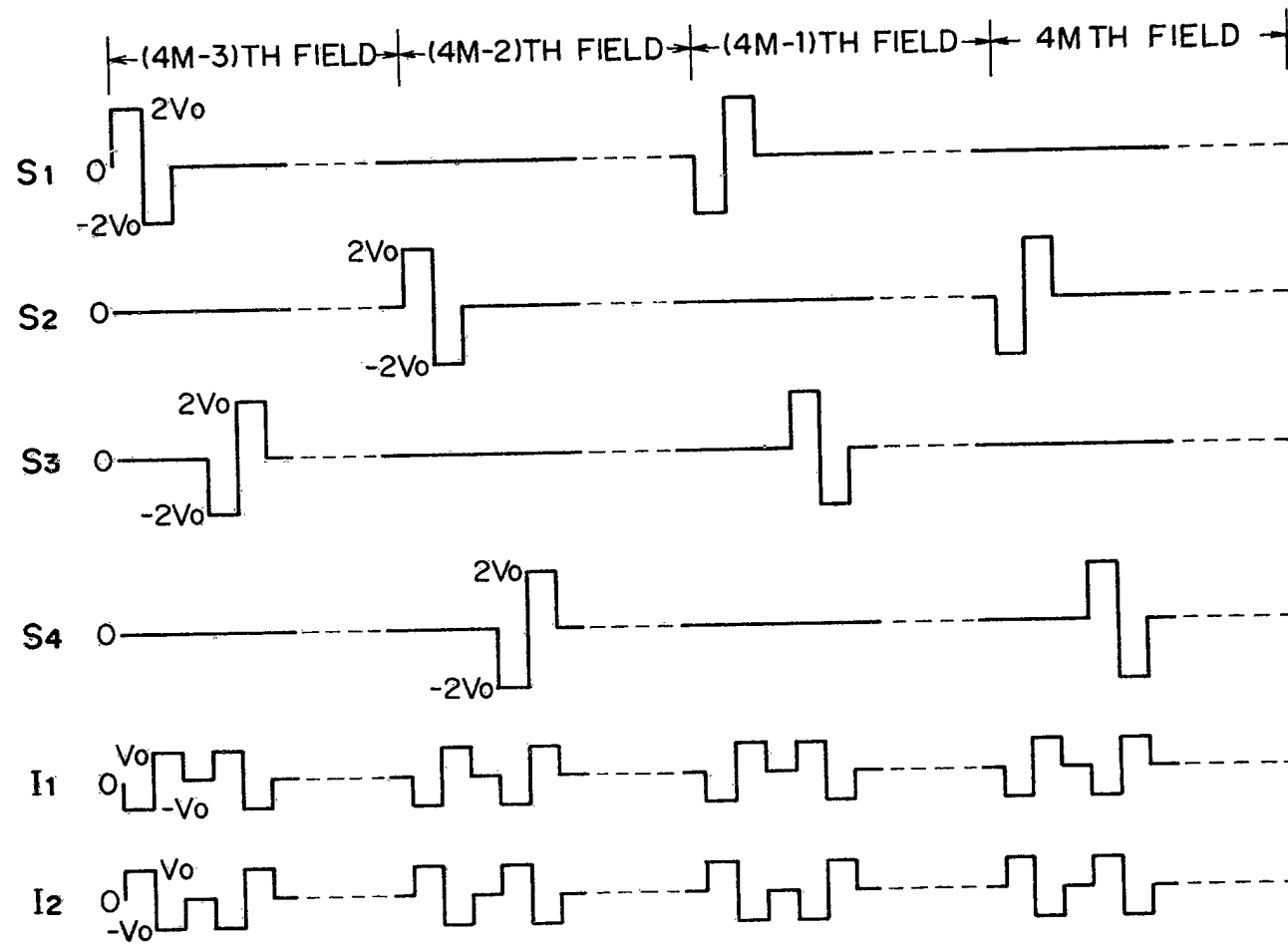


FIG. 15A

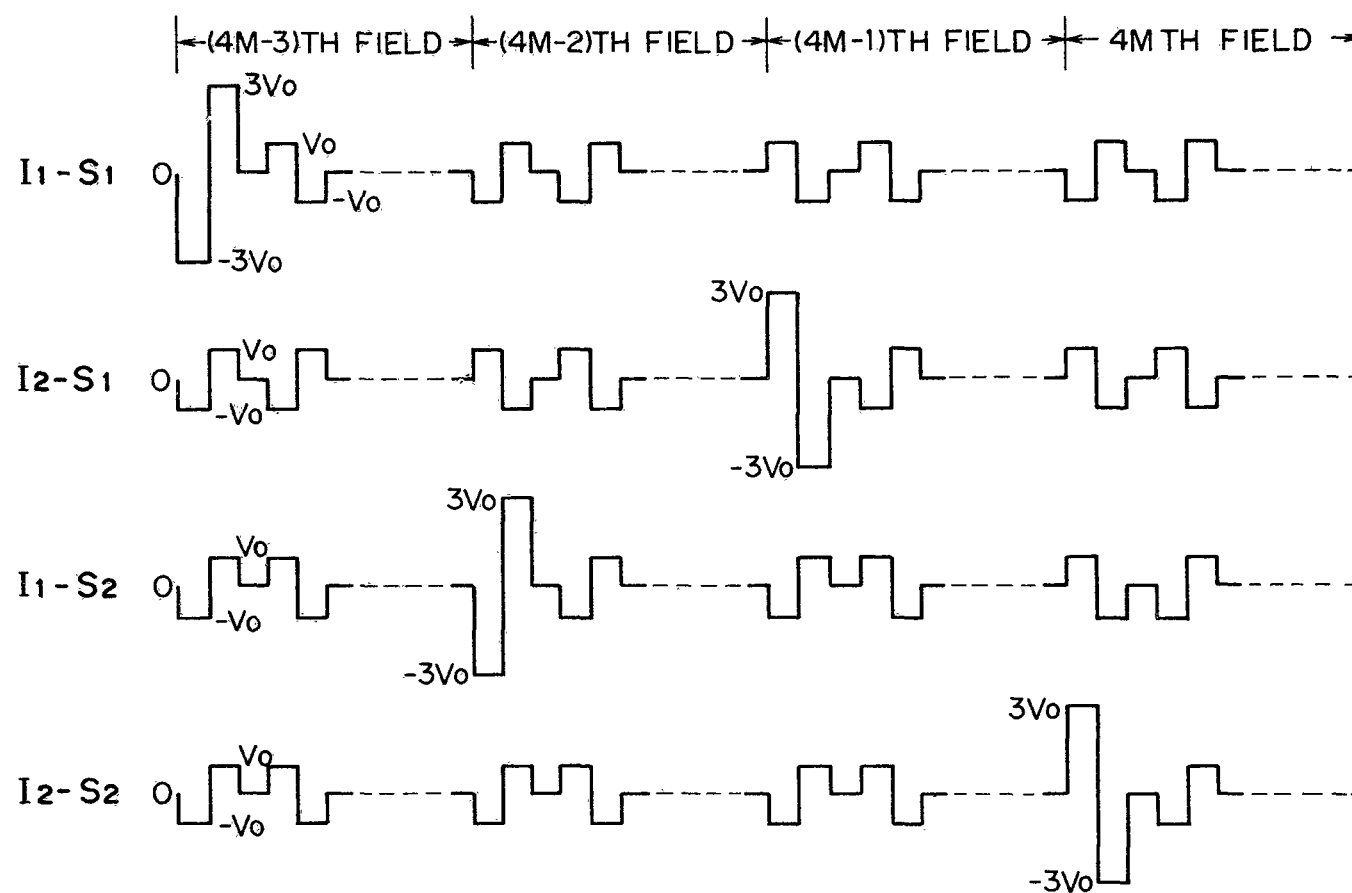


FIG. 15B

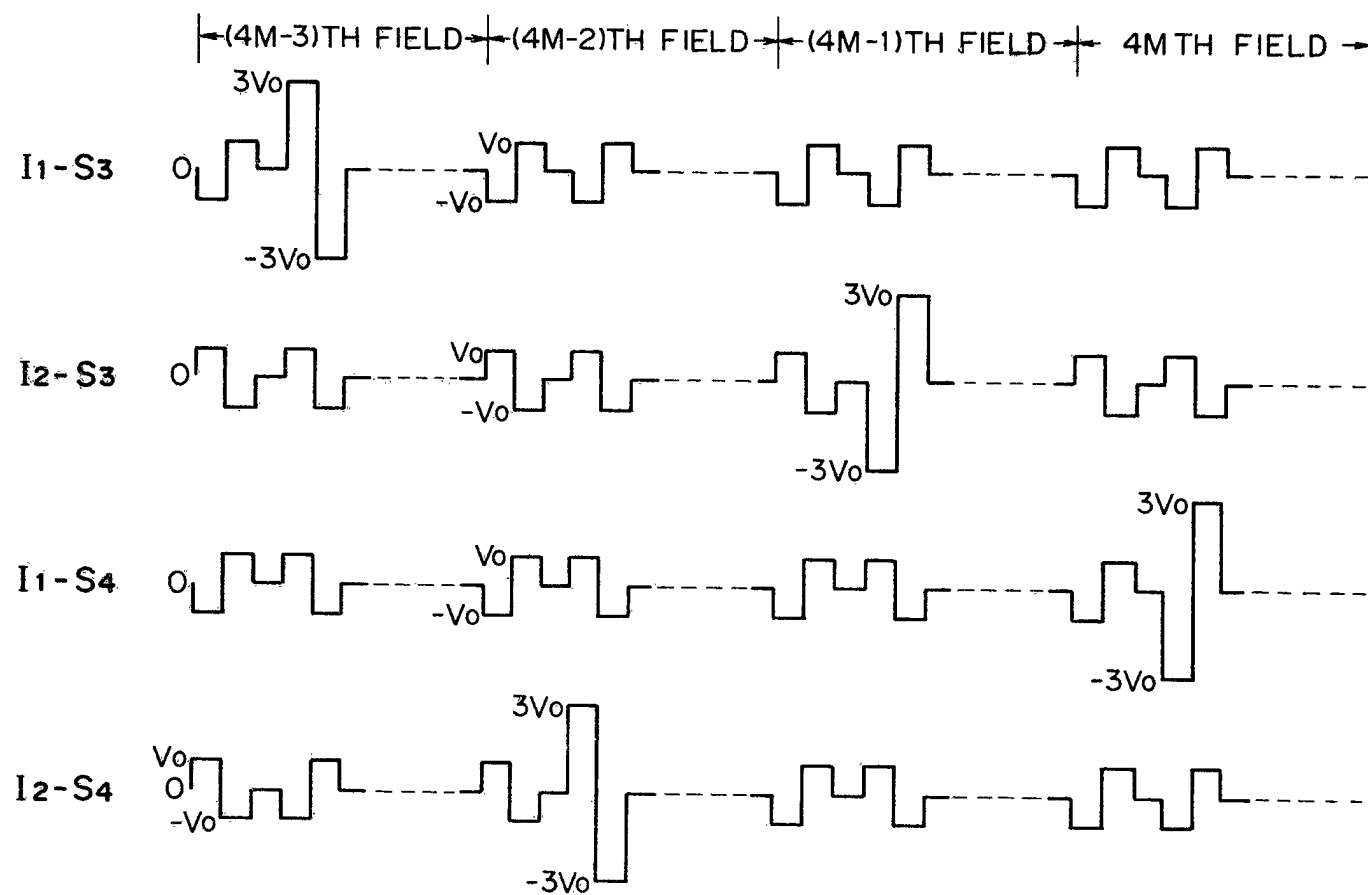


FIG. 15C

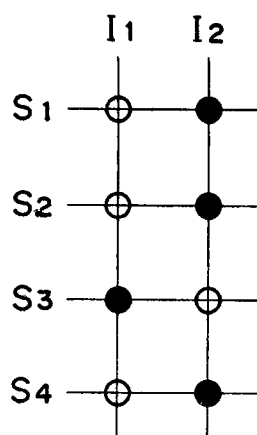


FIG. 15D

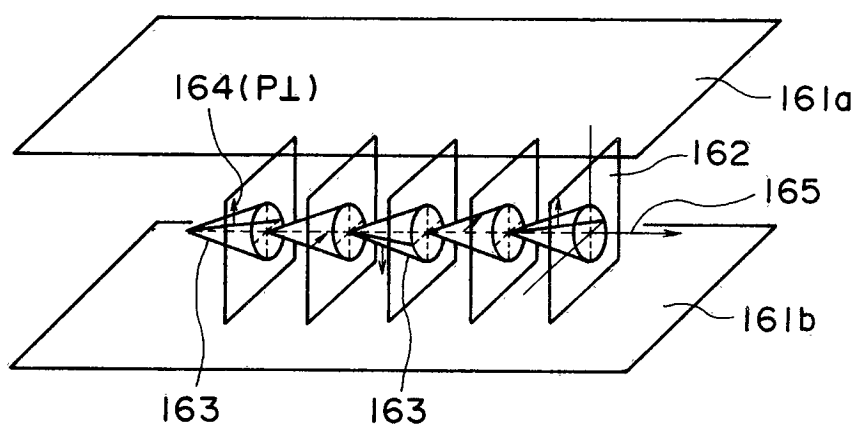


FIG. 16

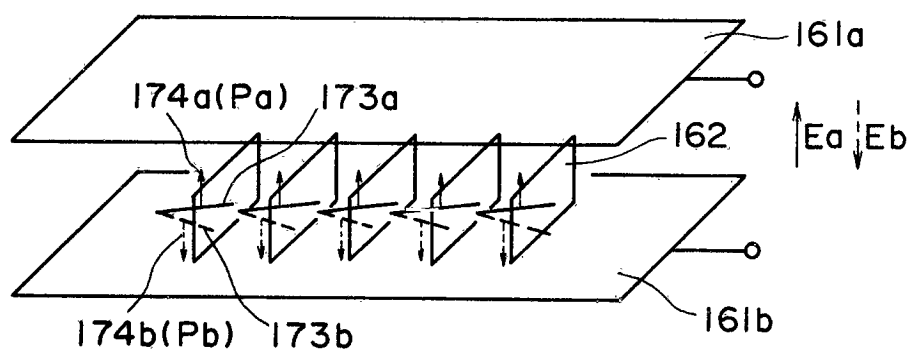


FIG. 17