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Description

DIFFERENTIAL GAIN-STAGE CIRCUIT AND METHOD FOR MULTIPLYING A VOLTAGE

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The patent application is related to a differential gain-stage circuit and to a method for multiplying a voltage.

10 A gain-stage circuit is commonly used for multiplying a voltage. An input voltage is provided to an input terminal of the gain-stage circuit and a multiplied voltage is provided as an output voltage at an output terminal of the gain-stage circuit. The gain-stage circuit may comprise a switched capacitor network. Such a gain-stage circuit can be a part of
15 a multiplying digital-to-analog converter, abbreviated MDAC. A pipelined analog-to-digital converter, abbreviated pipelined AD converter, can comprise such a MDAC.

It is an object of the present patent application to provide
20 a differential gain-stage circuit and a method for multiplying a voltage that can be used for a differential input voltage.

This object is solved by the subject matter of the
25 independent claims. Further developments and embodiments are described in the dependent claims.

In an embodiment, a differential gain-stage circuit comprises a positive and a negative input terminal, a first capacitor
30 with a first and a second electrode, a second capacitor with a first and a second electrode, a first amplifier with an input coupled to the first electrode of the first capacitor, a second amplifier with an input coupled to the first

electrode of the second capacitor, a positive output terminal coupled to an output of the first amplifier and a negative output terminal coupled to an output of the second amplifier. In a first phase, a parallel circuit of the first and the
5 second capacitor is connected to the positive and the negative input terminal.

Advantageously, a differential input voltage can be applied to the positive and the negative input terminal resulting in
10 a differential output voltage that is tapped at the positive and the negative output terminal.

In an embodiment, the first and the second amplifier are implemented as a first and a second buffer. The first and the
15 second amplifier comprise an input and an output. The gains of the first and the second amplifier may be one. Thus, the first and the second amplifier may be implemented as a first and a second unity gain buffer. The first and the second amplifier may each have exactly one input and exactly one
20 output.

In an alternative embodiment, the first and the second amplifier are implemented as a first and a second operational amplifier. The gains of the first and the second amplifier
25 may be one. The first and the second amplifier may each have an input, a further input and an output.

In an embodiment, in the first phase, the first electrode of the first capacitor and the second electrode of the second
30 capacitor are both connected to the positive input terminal. The second electrode of the first capacitor and the first electrode of the second capacitor are both connected to the negative input terminal.

In an embodiment, the differential gain-stage circuit comprises a first and a second input switch coupling the positive and the negative input terminal to the first and the second electrode of the first capacitor. Moreover, a third and a fourth input switch of the differential gain-stage circuit couple the positive and the negative input terminal to the first and the second electrode of the second capacitor.

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In an embodiment, the first input switch couples the positive input terminal to the first electrode of the first capacitor. The second input switch couples the negative input terminal to the second electrode of the first capacitor. The third input switch couples the negative input terminal to the first electrode of the second capacitor. The fourth input switch couples the positive input terminal to the second electrode of the second capacitor.

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In an embodiment, the first to the fourth input switch are set in a conducting state in the first phase and in a non-conducting state in a second phase. The second phase follows the first phase. The first and the second phase may alternate. The first and the second phase may alternate periodically.

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In an embodiment, in the first phase, the first electrode of the first capacitor and the second electrode of the second capacitor are both directly connected to the positive input terminal. In the first phase, the second electrode of the first capacitor and the first electrode of the second capacitor are both directly connected to the negative input terminal. In the first phase, there are only conducting

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switches between the first electrode of the first capacitor and the positive input terminal, between the second electrode of the second capacitor and the positive input terminal, between the second electrode of the first capacitor and the negative input terminal and between the first electrode of the second capacitor and the negative input terminal. These switches are in a non-conducting state in the second phase.

In an embodiment, the first electrode of the first capacitor is directly and permanently connected to the input of the first amplifier. The first electrode of the second capacitor is directly and permanently connected to the input of the second amplifier.

In an embodiment, in the first phase, a differential input voltage is applied both to the first capacitor and to the second capacitor. The differential input voltage is tapped between the positive input terminal and the negative input terminal.

In an embodiment, in the first phase, the parallel circuit of the first and the second capacitor is directly connected to the positive and the negative input terminal.

In an embodiment, the first and the second capacitor do not form a parallel circuit in the second phase. The first and the second capacitor may form a serial connection in the second phase.

In an embodiment, in the first phase, the first amplifier is directly connected to the positive input terminal and the second amplifier is directly connected to the negative input terminal. In the first phase, there are only conducting

switches between the first amplifier and the positive input terminal and between the second amplifier and the negative input terminal. These switches are in a non-conducting state in the second phase.

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In an embodiment, the differential gain-stage circuit comprises a first voltage node connected to the second electrode of the first capacitor and a second voltage node connected to the second electrode of the second capacitor. In a second phase, a first adder voltage is provided to the first voltage node and a second adder voltage is provided to the second voltage node. The first adder voltage may be different from the second adder voltage.

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15 In an embodiment, the differential gain-stage circuit comprises a digital-to-analog converter, abbreviated DA converter. The DA converter includes outputs coupled to the first and the second voltage node. The DA converter generates the first and the second adder voltage in the second phase. 20 The DA converter may have open outputs in the first phase. The outputs of the DA converter may be in a high-impedance state in the first phase.

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In an embodiment, the digital-to-analog converter comprises a first to a fourth converter switch, a positive reference terminal and a negative reference terminal. The positive reference terminal is coupled via the first converter switch to the first voltage node and via the second converter switch to second voltage node. The negative reference terminal is coupled via the third converter switch to the first voltage node and via the fourth converter switch to the second voltage node.

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In an embodiment, the digital-to-analog converter comprises a fifth and a sixth converter switch and a common mode terminal coupled via the fifth converter switch to the first voltage node and via the sixth converter switch to the second voltage node.

In an embodiment, the first to the sixth converter switch are set in a non-conducting state in the first phase. The first to the sixth converter switch may only be set in a conducting state in the second phase. One of the first, third and fifth converter switch and one of the second, fourth and sixth converter switch are set in a conducting state in the second phase; the other converter switches are set in a non-conducting state in the second phase.

In an embodiment, the differential gain-stage circuit realizes a gain factor of approximately two. The gain factor of the differential gain-stage circuit may be in the range of 1.8 to 2.1 or 1.85 to 1.96 or 1.9 to 2.0. The gain factor is the ratio between a differential output voltage and a differential input voltage.

In an embodiment, a multiplying digital-to-analog converter comprises the differential gain-stage circuit and an analog-to-digital converter, abbreviated AD converter. An analog input of the multiplying digital-to-analog converter is coupled to the positive and the negative input terminal of the differential gain-stage circuit and to an input of the AD converter. An output of the AD converter is coupled to an input of the digital-to-analog converter of the differential gain-stage circuit and to a digital output of the multiplying digital-to-analog converter. The positive and the negative output terminal of the differential gain-stage circuit are

coupled to an analog output of the multiplying digital-to-analog converter.

In an embodiment, a pipelined analog-to-digital converter arrangement, abbreviated pipelined AD converter arrangement, comprises a first number N of stages. At least one stage of the first number N of stages is implemented as the multiplying digital-to-analog converter.

10 The differential gain-stage circuit for a multiplying digital-to-analog converter, abbreviated MDAC, in a pipelined AD converter arrangement makes use of a differential signal, especially the differential input signal.

15 Advantageously, a gain of two is created with a switched capacitor network. The differential gain-stage circuit is implemented as a switched capacitor network. In particular, the differential gain-stage circuit implements the gain in a differential 1.5-bit MDAC in the pipelined AD converter arrangement.

Advantageously, the gain of two is implemented by a switched capacitor network and the use of only two amplifiers which may be realized as two unity gain buffers. Thus, it is avoided to consume a high amount of power due to a large number of operational amplifiers. Furthermore, the requirement for matching of the first and the second capacitor that are the sampling capacitors is low. The differential gain-stage circuit implements the gain using the differential input voltage.

In an embodiment, the influence of parasitic capacitances, in particular the bottom plate capacitances of the first and the

second capacitor, is kept low. Advantageously, the parasitic capacitances only result in a small error. This positive effect can mainly be observed at low values of the parasitic capacitances.

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In an embodiment, a first and a second channel of the differential x2 gain-stage circuit each comprises: a sampling capacitor, two sampling switches, at least one switch for the voltage to be added (for a simple gain of two without offset, this voltage might be chosen equal to the common mode voltage of the input signals), and an amplifier, to minimize the load on the sampling capacitor when the signal needs to be forwarded.

15 The differential x2 gain-stage can be used as a MDAC for a 1-bit pipelined AD converter stage, wherein three switches are necessary to implement the digital-to-analog converter of the stage.

20 Advantageously, the impact of the bottom plate capacitance is eliminated. A high gain accuracy may be achieved. Less components are used. Thus, the complexity of the circuit is kept low. The area occupied by sampling capacitors is kept low. The differential gain-stage circuit operates as a charge pump. An effective capacitance towards the voltage divider with the input capacitance of the amplifier is large. The charge redistribution is kept small. Matching of the sampling capacitors has no first order effect on the gain accuracy.

30 In an embodiment, a method for multiplying a voltage comprises providing a differential input voltage to a parallel circuit of a first capacitor and a second capacitor in a first phase, generating a positive output voltage by a

first amplifier having an input coupled to the first electrode of the first capacitor, and generating a negative output voltage by a second amplifier having an input coupled to the first electrode of the second capacitor.

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Advantageously, a differential input voltage can be applied both to the first capacitor and to the second capacitor resulting in the positive and the negative output voltage. Thus, a differential output voltage is provided from subtracting the negative output voltage from the positive output voltage.

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In an embodiment, a first adder voltage is provided to the second electrode of the first capacitor and a second adder voltage is provided to the second electrode of the second capacitor in a second phase.

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In an embodiment, the parallel circuit of the first and the second capacitor is realized by connecting the first electrode of the first capacitor to the second electrode of the second capacitor and by connecting the second electrode of the first capacitor to the first electrode of the second capacitor.

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The following description of figures of exemplary embodiments may further illustrate and explain aspects of the application. Devices and circuit parts with the same structure and the same effect, respectively, appear with equivalent reference symbols. As far as devices or circuit parts correspond to one another in terms of their function in different figures, the description thereof is not repeated for each of the following figures.

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Figures 1A to 1D show an exemplary embodiment of a differential gain-stage circuit and the corresponding phases and signals.

5 Figure 2A and 2B show a further exemplary embodiment of a differential gain-stage circuit and the corresponding phases.

10 Figure 3 shows an exemplary embodiment of a multiplying digital-to-analog converter.

Figure 4 shows an exemplary embodiment of a pipelined analog-to-digital converter arrangement.

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Figure 1A shows an exemplary embodiment of a differential gain-stage circuit 10 comprising a first capacitor 11 with a first and a second electrode 12, 13 and a second capacitor 14 with a first and a second electrode 15, 16. Moreover, the differential gain-stage circuit 10 comprises a first amplifier 17 with an input 18 and a second amplifier 19 with an input 20. The first electrode 12 of the first capacitor 11 is directly and permanently connected to the input 18 of the first amplifier 17. Correspondingly, the first electrode 15 of the second capacitor 14 is directly and permanently connected to the input 20 of the second amplifier 19. A positive output terminal 21 of the differential gain-stage circuit 10 is directly connected to an output of the first amplifier 17. Similarly, a negative output terminal 22 of the differential gain-stage circuit 10 is directly connected to an output of the second amplifier 19. The first amplifier 17 and the second amplifier 19 may be realized identical.

The first and the second amplifier 17, 19 are realized as buffers, optionally as unity gain buffers. The first and the second amplifier 17, 19 may be both configured as source follower. For example, the first and the second amplifier 17, 19 may be both implemented as p-channel metal-oxide-semiconductor source follower or may be both implemented as n-channel metal-oxide-semiconductor source follower.

Additionally, the differential gain-stage circuit 10 comprises a positive and a negative input terminal 25, 26. The differential gain-stage circuit 10 comprises a first to a fourth input switch 27 to 30. The positive input terminal 25 is coupled via the first input switch 27 to the first electrode 12 of the first capacitor 11. The negative input terminal 26 is coupled via the second input switch 28 to the second electrode 13 of the first capacitor 11. Moreover, the negative input terminal 26 is coupled via the third input switch 29 to the first electrode 15 of the second capacitor 14. The positive input terminal 25 is coupled via the fourth input switch 30 to the second electrode 16 of the second capacitor 14.

The differential gain-stage circuit 10 comprises a first voltage node 35 that is directly and permanently connected to the second electrode 13 of the first capacitor 11. A second voltage node 36 is directly and permanently connected to the second electrode 16 of the second capacitor 14.

Additionally, the differential gain-stage circuit 10 comprises a digital-to-analog converter 37, abbreviated DA converter. The DA converter 37 comprises a positive and a negative reference terminal 38, 39 that are both coupled to the first and the second voltage node 35, 36. Thus, the DA

converter 37 comprises a first to a fourth converter switch 40 to 43. The first converter switch 40 couples the positive reference terminal 38 to the first voltage node 35.

Correspondingly, the second converter switch 41 couples the positive reference terminal 38 to the second voltage node 34. The third converter switch 42 couples the negative reference terminal 39 to the first voltage node 35 and the fourth converter switch 43 couples the negative reference terminal 39 to the second voltage node 36.

Moreover, the DA converter 37 comprises a common mode terminal 44 that is coupled to the first and the second voltage node 35, 36. A fifth converter switch 45 of the DA converter 37 couples the common mode terminal 44 to the first voltage node 35. Additionally, a sixth converter switch 46 of the DA converter 37 couples the common mode terminal 44 to the second voltage node 36.

The differential gain-stage circuit 10 comprises a control logic 52 having outputs connected to the control terminals of the first to the fourth input switch 27 to 30. Moreover, further output terminals of the control logic 52 may be connected to the control terminals of the first to the sixth converter switch 40 to 43, 45, 46.

The first and the second capacitor 11, 14 have approximately the same capacitance value C_S . The first capacitor 11 and the first amplifier 17 are part of a first channel 50 that can be named p-channel or positive side channel. The second capacitor 14 and the second amplifier 19 are part of a second channel 51 that can be named n-channel or negative side channel.

A positive input voltage V_{INP} is provided to the positive input terminal 25. A negative input voltage V_{INN} is applied to the negative input terminal 26. Thus, a differential input voltage V_{IN} can be tapped between the positive input terminal 25 and the negative input terminal 26. A positive output voltage V_{OUTP} is generated by the first amplifier 17 and can be tapped at the positive output terminal 21. A negative output voltage V_{OUTN} is generated by the second amplifier 19 and can be tapped at the negative output terminal 22. A differential output voltage V_{OUT} is tapped between the positive and the negative output terminal 21, 22.

In each channel 50, 51, only one capacitor 11, 14 may be needed to create the gain, exploiting the fact that the voltage difference needed is already present in a differential system. The voltage difference is the differential input voltage V_{IN} .

Thus, a first input voltage V_{B1} is provided to the input 18 of the first amplifier 17. A second input voltage V_{B2} is applied to the input 20 of the second amplifier 19. The first and the second amplifier 17, 19 may have an amplification factor of one. Thus, the first input voltage V_{B1} is equal to the positive output voltage V_{OUTP} . The second input voltage V_{B2} is equal to the negative output voltage V_{OUTN} . A positive reference voltage V_P is provided at the positive reference terminal 38 and a negative reference voltage V_N is provided at the negative reference terminal 39. A common mode voltage V_{CM} is provided at the common mode terminal 44. The differential gain-stage circuit 10 may comprise a not-shown reference source coupled to the positive and the negative reference terminal 38, 39 and to the common mode terminal 44

generating the positive and the negative reference voltage V_P , V_N and the common mode voltage V_{CM} .

The first to the fourth input switch 27 to 30 are each
5 controlled by the same signal namely a first control signal Φ_1 . The second and the third converter switch 41, 42 are controlled by a first converter signal Φ_{2P} . The first and the fourth converter switch 40, 43 are controlled by a second converter signal Φ_{2N} . The fifth and the sixth converter
10 switch 45, 46 are both controlled by a third converter signal Φ_{2M} . The first control signal Φ_1 and the first to the third converter signals Φ_{2P} , Φ_{2N} , Φ_{2M} are generated by the control logic 52.

15 In Figure 1A, a schematic of the differential circuit is illustrated with the converter signals Φ_{2M} , Φ_{2N} , Φ_{2P} according to Figure 1C and 1D. The converter signals Φ_{2M} , Φ_{2N} , Φ_{2P} may be named clock phases.

20 Figure 1B shows exemplary phases of the differential gain-stage circuit 10 shown in Figure 1A. In Figure 1B, the method of the differential gain topology is explained. In a first phase A, the first to the fourth input switch 27 to 30 are set in a conducting state by the first control signal Φ_1 .
25 Thus, the positive input voltage V_{INP} is provided to the first electrode 12 of the first capacitor 11 and to the second electrode 16 of the second capacitor 14. Correspondingly, the negative input voltage V_{INN} is applied to the second electrode 13 of the first capacitor 11 and to
30 the first electrode 15 of the second capacitor 14. The converter switches 40 to 43, 45, 46 are set in a non-conducting state in the first phase A. Thus, the differential input voltage V_{IN} is applied across the first capacitor 11

and the second capacitor 14. The first phase A can be named sampling phase.

A second phase B follows the first phase A. The second phase
 5 B can be named amplification phase. In the second phase B, a first adder voltage VAP is provided to the first voltage node 35 and a second adder voltage VAN is provided to the second voltage node 36. Thus, the input voltage VB1 of the first
 10 amplifier 17 and the input voltage VB2 of the second amplifier 19 can be calculated according to the following equations:

$$VB1 = VAP + VIN \text{ and } VB2 = VAN - VIN$$

15 Both amplifiers 17, 19 may have a gain of one. Consequently, the positive output voltage VOUTP, the negative output voltage VOUTN and the differential output voltage VOUT can be calculated according to the following equation:

$$\begin{aligned} 20 \quad VOUTP &= VB1 = VAP + VIN, \\ VOUTN &= VB2 = VAN - VIN \text{ and} \\ VOUT &= VOUTP - VOUTN = VB1 - VB2 = VAP + 2 \cdot VIN - VAN \end{aligned}$$

The equations above are valid for each value of the
 25 differential input voltage VIN that means for each of the three regions I, II, III defined below. The first phase A and the second phase B alternate. The first to the third converter signals $\Phi2M$, $\Phi2P$, $\Phi2N$ are generated by the DA converter 37. The differential gain-stage circuit 10 is
 30 configured to perform a differential sampling.

Figures 1C and 1D show exemplary voltages VS that can be tapped in the differential gain-stage circuit 10 described in

Figures 1A and 1B. Figures 1C and 1D are diagrams of the signal generation for the first channel 50, namely the p-channel. In Figure 1C, the arrows indicate the difference between the positive input voltage V_{INP} and the negative input voltage V_{INN} . Thus, the arrows indicate the differential input voltage V_{IN} sampled at the first and at the second capacitor 11, 14. The resulting differential input voltage V_{IN} is shown on the x-axes. If the positive input voltage V_{INP} and the negative input voltage V_{INN} are equal, both input voltages V_{INP} , V_{INN} are equal to the common mode voltage V_{CM} . For example, the common mode voltage V_{CM} may be at the half of a supply voltage V_{DD} . Thus, the common mode voltage V_{CM} may be for example equal to 1.65 V. The differential input voltage V_{IN} may have positive and negative values. Thus, the differential input voltage V_{IN} may be for example out of the range from -0.5 V to +0.5 V. The relationship of the positive input voltage V_{INP} , the negative input voltage V_{INN} , the common mode voltage V_{CM} and the differential input voltage V_{IN} is as follows:

$$\begin{aligned} V_{INP} &= V_{CM} + \frac{V_{IN}}{2}, \\ V_{INN} &= V_{CM} - \frac{V_{IN}}{2}, \\ V_{IN} &= V_{INP} - V_{INN} \end{aligned}$$

In Figure 1D, the positive output voltage V_{OUTP} and the negative output voltage V_{OUTN} are illustrated as a function of the differential input voltage V_{IN} . The positive output voltage V_{OUTP} and the negative output voltage V_{OUTN} are mirrored to each other with respect to a line representing the common mode voltage V_{CM} . The length of the arrows corresponds to the value of the differential input voltage

VIN. In Figure 1D, positive values of the differential input voltage VIN result in bottom-up arrows and negative values of the differential input voltage VIN result in top-down arrows.

- 5 As indicated in Figures 1C and 1D by two vertical lines the differential input voltage VIN is separated in three regions I, II, III, wherein VTP is a positive threshold voltage and VTN is a negative threshold voltage:

10 First region I: $VTP \leq VIN$
 Second region II: $VIN \leq VTN$
 Third region III: $VTN \leq VIN \leq VTP$

In case the differential input voltage VIN is in the first
 15 region I, the first converter signal $\Phi 2P$ is set. In the first region I, the differential output voltage VOUT, the positive output voltage VOUTP and the negative output voltage VOUTN can be calculated according to the following equations:

20
$$VOUTP = VN + VIN = VCM + VIN - \Delta V,$$

$$VOUTN = VP - VIN = VCM - VIN + \Delta V,$$

$$VOUT = 2 \cdot VIN - 2 \cdot \Delta V;$$

wherein VN is the negative reference voltage, VP is the
 25 positive reference voltage, VIN is the differential input voltage and VCM is the common mode voltage. ΔV can be calculated according to the equation:

$$\Delta V = \frac{VP - VN}{2}$$

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In case the differential input voltage VIN has a value in the second region II, the second converter signal $\Phi 2N$ is set. In the second region II, the differential output voltage VOUT,

the positive output voltage V_{OUTP} and the negative output voltage V_{OUTN} can be calculated according to the following equations:

$$\begin{aligned} V_{OUTP} &= V_P + V_{IN} = V_{CM} + V_{IN} + \Delta V, \\ V_{OUTN} &= V_N - V_{IN} = V_{CM} - V_{IN} - \Delta V, \\ V_{OUT} &= 2 \cdot V_{IN} + 2 \cdot \Delta V \end{aligned}$$

In case the differential input voltage V_{IN} is in the third region III, the third converter signal $\Phi 2M$ is set. In the third region II, the differential output voltage V_{OUT} , the positive output voltage V_{OUTP} and the negative output voltage V_{OUTN} can be calculated according to the following equations:

$$\begin{aligned} V_{OUTP} &= V_{CM} + V_{IN}, \\ V_{OUTN} &= V_{CM} - V_{IN}, \\ V_{OUT} &= 2 \cdot V_{IN} \end{aligned}$$

An analog-to-digital converter 71 shown in Figure 3 may generate converter signals $\Phi 2P$, $\Phi 2M$, $\Phi 2N$.

Advantageously, the first and the second capacitor 11, 14 are directly charged with the voltage difference that is the differential input voltage V_{IN} . The voltage difference is between the negative input voltage V_{INN} and the positive input voltage V_{INP} illustrated by arrows in Figure 1C. The differential input voltage V_{IN} is then used to create each of the single ended signals again, namely the negative output voltage V_{OUTN} and the positive output voltage V_{OUTP} . As a result, the differential output voltage V_{OUT} at the two output terminals 21, 22 of the differential gain-stage circuit 10 is then proportional to the differential input voltage V_{IN} . The proportional factor may be a gain factor of

approximately two. The differential input voltage V_{IN} is used to generate a gain of two for a MDAC 70 shown in Figure 3. In Figure 1D, the output signals such as the positive and negative output voltage V_{OUTP} , V_{OUTN} are constructed adding
5 the sampled differential input voltage V_{IN} to the appropriate reference voltage, namely the positive or the negative reference voltage V_P , V_N or the common mode voltage V_{CM} .

Figure 2A shows a further exemplary embodiment of the
10 differential gain-stage circuit 10 which is a further development of the above shown embodiments. The first and the second amplifier 17, 19 are realized as operational amplifiers. The input 18 of the first amplifier 17 is realized as an inverting input, whereas a further input 60 of
15 the first amplifier 17 is implemented as a non-inverting input. The input 20 of the second amplifier 19 is realized as an inverting input, whereas a further input 61 of the second amplifier 19 is implemented as a non-inverting input.

20 The first capacitor 11 couples the input 18 of the first amplifier 17 to the output of the first amplifier 17. The second capacitor 14 is arranged between the input 20 of the second amplifier 19 and the output of the second amplifier 19. The first and the second capacitor 11, 14 may be directly
25 and permanently connected to the first and the second amplifier 17, 19. The first electrode 12 of the first capacitor 11 is connected to the input 18 of the first amplifier 17. The second electrode 13 of the first capacitor 11 is connected to the output of the first amplifier 17.
30 Correspondingly, the first electrode 15 of the second capacitor 14 is connected to the input 20 of the second amplifier 19. The second electrode 16 of the second capacitor 14 is connected to the output of the second amplifier 19. The

four input switches 27 to 30 may be connected to the first and the second capacitor 11, 14 such as shown in Figure 1A.

The first voltage node 35 is connected to the further input
5 60 of the first amplifier 17. The second voltage node 36 is connected to the further input 61 of the second amplifier 19. The first adder voltage VAP is provided via the first voltage node 35 to the further input 60 of the first amplifier 17. The second adder voltage VAN is provided via the second
10 voltage node 36 to the further input 61 of the second amplifier 19.

Figure 2B shows exemplary phases of the differential gain-stage circuit 10 shown in Figure 2A. The differential input
15 voltage VIN is sampled at the first and the second capacitor 11, 14 in the first phase A and provided between the input 18, 20 and the output of the first and second amplifier 17, 19 in the second phase B.

20 Figure 3 shows a multiplying digital-to-analog converter 70, abbreviated MDAC. The MDAC 70 comprises the differential gain-stage circuit 10 as shown in one of the Figures above. Additionally, the MDAC 70 comprises an analog-to-digital converter 71, abbreviated AD converter. The AD converter 71
25 is designed as sub AD converter. The AD converter 71 may comprise two comparators, not shown. The two comparators may compare the differential input voltage VIN with the positive threshold voltage VTP and the negative threshold voltage VTN. An analog input 72 of the MDAC 70 is coupled to an input of
30 the AD converter 71 and to the positive and the negative input terminal 25, 26. The analog input 72 may be realized as a differential input. An output of the AD converter 71 is

coupled to a digital output 73 of the MDAC 70 and to an input of the DA converter 37.

The MDAC 70 may comprise a sample-and-hold circuit 74 coupling the analog input 72 of the MDAC 70 to the AD converter 71 and the positive and negative input terminal 25, 26. The positive and the negative output terminal 21, 22 form an analog output 75 of the MDAC 70. The analog output 75 is implemented as a differential output.

The AD converter 71 generates a digital output signal SDA and provides it to the digital output 73 of the MDAC 70 and to the input of the DA converter 37. The digital output signal SDA may comprise two bits.

The differential gain-stage circuit 10 is configured for multiplication and summation. A value of the differential output voltage V_{OUT} depends on a value of the differential input voltage V_{IN} and a value of the digital output signal SDA. The value of the differential output voltage V_{OUT} corresponds to the twofold value of the differential input voltage V_{IN} which is added to the value of the digital output signal SDA. The value of the digital output signal SDA corresponds to the voltage difference between the first adder voltage V_{AP} and the second adder voltage V_{AN} . Thus, the differential output voltage V_{OUT} is a residual voltage that is further digitized by a further MDAC as shown in Figure 4. The multiplication is performed with the gain factor of approximately two.

Figure 4 shows an exemplary embodiment of a pipelined AD converter arrangement 80 that comprises the MDAC 70 shown in Figure 3. The pipelined AD converter arrangement 80 comprises

the first number N of stages 81 to 84 which are serially connected. The analog output 75 of the first stage 81 is connected to an analog input 72' of the second stage 82 and so on. At least one of the stages 81 to 84 may be implemented
5 as the MDAC 70 shown in Figure 3. Each of the first number N of stages 81 to 84 may be realized as the MDAC 70 shown in Figure 3. The digital output 73 of each of the first number N of stages 81 to 84 is connected to a digital correction
10 circuit 90 of the pipelined AD converter arrangement 80. An output of the digital correction circuit 90 forms a digital output 91 of the pipelined AD converter arrangement 80.

An analog input voltage V_A is provided to the input of the first stage 81. A digital converter output signal SDOUT is
15 generated by the use of the digital output signals SDA, SDA', SDA'', SDA''' generated by the first number N of stages 81 to 84 especially by the AD converter 71 of the first number N of stages 81 to 84.

20 Alternatively, the stages of the first number N of stages 81 to 84 may be realized by different circuits. Some stages may be realized as MDAC 70 shown in Figure 3. For example, the first stage 81 may be realized with the sample-and-hold
circuit 74. Other stages may be realized without the sample-
25 and-hold circuit 74. The last stage 84 may be implemented without the analog output 75 and without the first and the second amplifier 17, 19.

Reference numerals

	10	differential gain-stage circuit
	11	first capacitor
5	12	first electrode
	13	second electrode
	14	second capacitor
	15	first electrode
	16	second electrode
10	17	first amplifier
	18	input
	19	second amplifier
	20	input
	21	positive output terminal
15	22	negative output terminal
	25	positive input terminal
	26	negative input terminal
	27 to 30	input switch
	35	first voltage node
20	36	second voltage node
	37	digital-to-analog converter
	38	positive reference terminal
	39	negative reference terminal
	40 to 43	converter switch
25	44	common mode terminal
	45, 46	converter switch
	50	first channel
	51	second channel
	52	control logic
30	60, 61	further input
	70	multiplying digital-to-analog converter
	71	analog-to-digital converter
	72, 72', 72''	analog input

	73	digital output
	74	sample-and-hold circuit
	75, 75', 75''	analog output
	80	pipelined analog-to-digital converter
5		arrangement
	81 to 84	stage
	90	digital correction circuit
	91	digital output
	A	first phase
10	B	second phase
	SAN	analog input signal
	SDA	digital output signal
	SDOUT	digital converter output signal
	VA	analog input signal
15	VAN	second adder voltage
	VAP	first adder voltage
	VB1	first input voltage
	VB2	second input voltage
	VCM	common mode voltage
20	VIN	differential input voltage
	VINN	negative input voltage
	VINP	positive input voltage
	VOUT	differential output signal
	VOUTN	negative output voltage
25	VOUTP	positive output voltage
	VN	negative reference voltage
	VP	positive reference voltage
	VTN	negative threshold voltage
	VTP	positive threshold voltage
30	$\Phi 1$	first control signal
	$\Phi 2M$	third converter signal
	$\Phi 2N$	second converter signal
	$\Phi 2P$	first converter signal

Claims

1. Differential gain-stage circuit, comprising

- a positive and a negative input terminal (25, 26),
- 5 - a first capacitor (11) with a first and a second electrode (12, 13),
- a second capacitor (14) with a first and a second electrode (15, 16),
- a first amplifier (17) with an input (18) coupled to the
- 10 first electrode (12) of the first capacitor (11),
- a second amplifier (19) with an input (20) coupled to the first electrode (15) of the second capacitor (14),
- a positive output terminal (21) coupled to an output of the first amplifier (17), and
- 15 - a negative output terminal (22) coupled to an output of the second amplifier (19),

wherein in a first phase (A), a parallel circuit of the first and the second capacitor (11, 14) is connected to the positive and the negative input terminal (21, 22).

20

2. Differential gain-stage circuit according to claim 1, wherein the first and the second amplifier (17, 19) are implemented as a first and a second buffer.

- 25 3. Differential gain-stage circuit according to claim 1 or 2, wherein in the first phase (A), the first electrode (12) of the first capacitor (11) and the second electrode (16) of the second capacitor (14) are both connected to the positive input terminal (25) and the second electrode (13) of the
- 30 first capacitor (11) and the first electrode (15) of the second capacitor (14) are both connected to the negative input terminal (26).

4. Differential gain-stage circuit according to one of claims 1 to 3, comprising

- a first input switch (27) coupling the positive input terminal (25) to the first electrode (12) of the first capacitor (11),
- a second input switch (28) coupling the negative input terminal (26) to the second electrode (13) of the first capacitor (11),
- a third input switch (29) coupling the negative input terminal (26) to the first electrode (15) of the second capacitor (14), and
- a fourth input switch (30) coupling the positive input terminal (25) to the second electrode (16) of the second capacitor (14).

5. Differential gain-stage circuit according to claim 4, wherein the first to the fourth input switch (27 to 30) are set in a conducting state in the first phase (A) and in a non-conducting state in a second phase (B).

6. Differential gain-stage circuit according to one of claims 1 to 5,

wherein the first electrode (12) of the first capacitor (11) is directly and permanently connected to the input (18) of the first amplifier (17) and the first electrode (15) of the second capacitor (14) is directly and permanently connected to the input (20) of the second amplifier (19).

7. Differential gain-stage circuit according to one of claims 1 to 6,

comprising

- a first voltage node (35) connected to the second electrode (13) of the first capacitor (11) and

- a second voltage node (36) connected to the second electrode (16) of the second capacitor (14),
wherein in a second phase (B), a first adder voltage (VAP) is provided to the first voltage node (35) and a second adder
5 voltage (VAN) is provided to the second voltage node (36).

8. Differential gain-stage circuit according to claim 7,
comprising a digital-to-analog converter (37) with outputs
coupled to the first and the second voltage node (35, 36).

10

9. Differential gain-stage circuit according to claim 8,
wherein the digital-to-analog converter (37) comprises
- a first to a fourth converter switch (40 to 43),
- a positive reference terminal (38) coupled via the first
15 and the second converter switch (40, 41) to the first and
the second voltage node (35, 36) and
- a negative reference terminal (39) coupled via the third
and the fourth converter switch (42, 43) to the first and
the second voltage node (35, 36).

20

10. Differential gain-stage circuit according to claim 8 or
9,

wherein the digital-to-analog converter (37) comprises

- a fifth and a sixth converter switch (45, 46) and
25 - a common mode terminal (44) coupled via the fifth and the
sixth converter switch (45, 46) to the first and the
second voltage node (35, 36).

11. Differential gain-stage circuit according to one of
30 claims 1 to 10,
wherein the differential gain-stage circuit (10) realizes a
gain factor of approximately two.

12. Multiplying digital-to-analog converter (70),
comprising the differential gain-stage circuit (10) according
to one of claims 1 to 11 and an analog-to-digital converter
(71), wherein an analog input (72) of the multiplying
5 digital-to-analog converter (70) is coupled to the positive
and the negative input terminal (25, 26) of the differential
gain-stage circuit (10) and to an input of the analog-to-
digital converter (71),
wherein an output of the analog-to-digital converter (71) is
10 coupled to an input of the digital-to-analog converter (37)
of the differential gain-stage circuit (10) and to a digital
output (73) of the multiplying digital-to-analog converter
(70), and
wherein the positive and the negative output terminal (21,
15 22) of the differential gain-stage circuit (10) are coupled
to an analog output (75) of the multiplying digital-to-analog
converter (70).

13. Pipelined analog-to-digital converter arrangement (80),
20 comprising a first number N of stages (81 to 84),
wherein at least one stage of the first number N of stages
(81 to 84) is implemented as the multiplying digital-to-
analog converter (70) according to claim 12.

25 14. Method for multiplying a voltage,
- providing a differential input voltage (VIN) to a parallel
circuit of a first capacitor (11) and a second capacitor
(14) in a first phase (A),
- generating a positive output voltage (VOU_{TP}) by a first
30 amplifier (17) having an input (18) coupled to the first
electrode (12) of the first capacitor (11) and

- generating a negative output voltage (VOUTN) by a second amplifier (19) having an input (20) coupled to the first electrode (15) of the second capacitor (14).

5 15. Method for multiplying a voltage according to claim 14, wherein a first adder voltage (VAP) is provided to the second electrode (13) of the first capacitor (11) and a second adder voltage (VAN) is provided to the second electrode (16) of the second capacitor (14) in a second phase (B).

FIG 1A

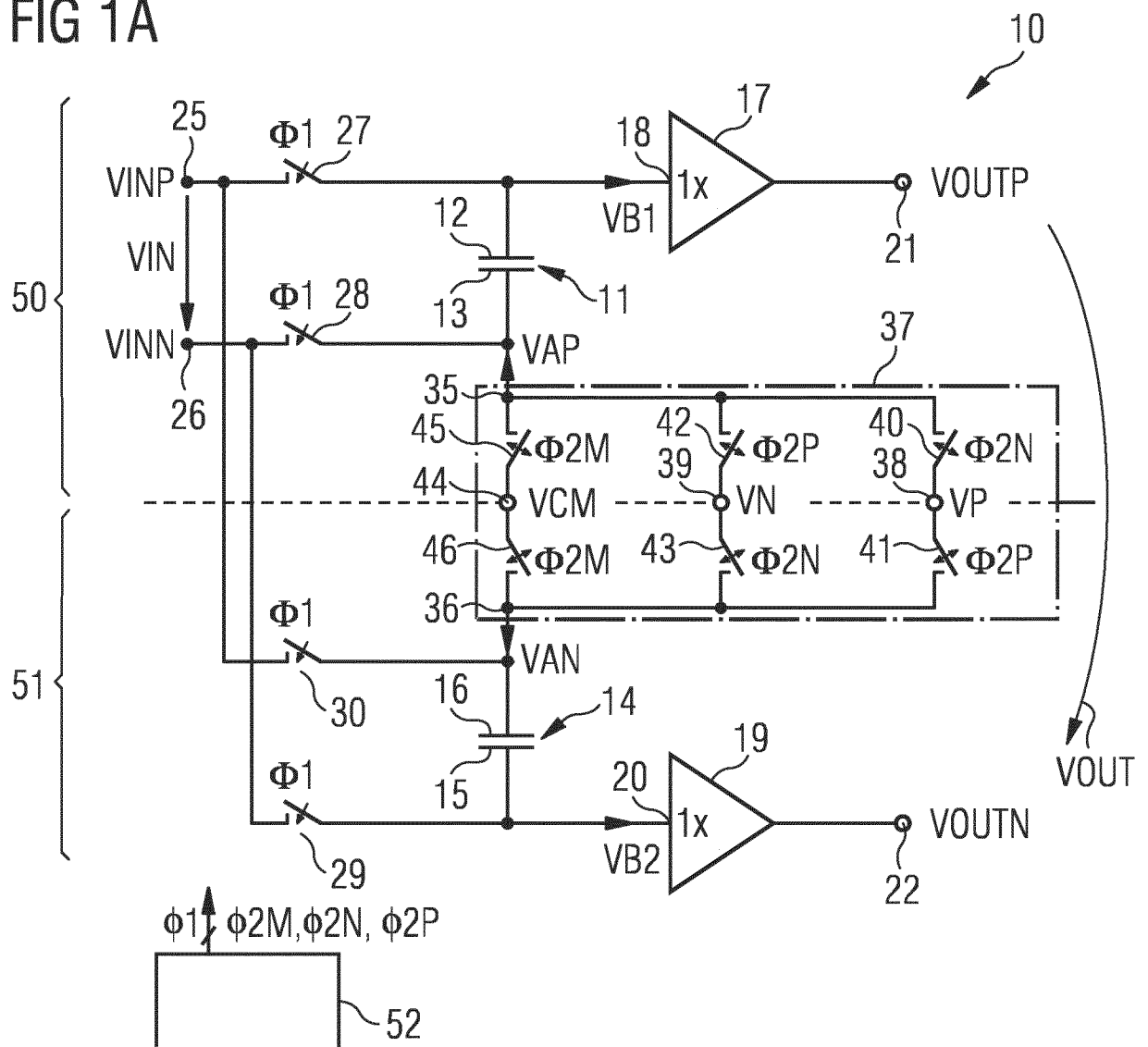
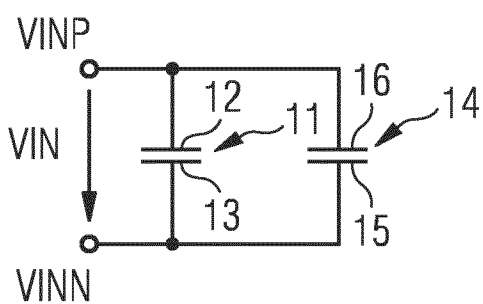


FIG 1B

A



B

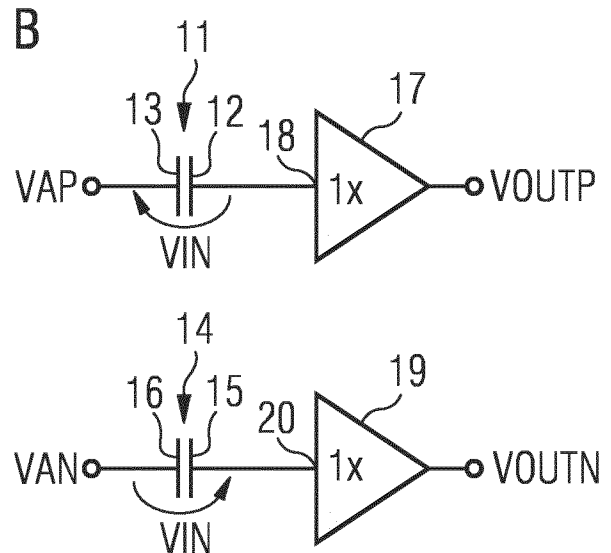


FIG 1C

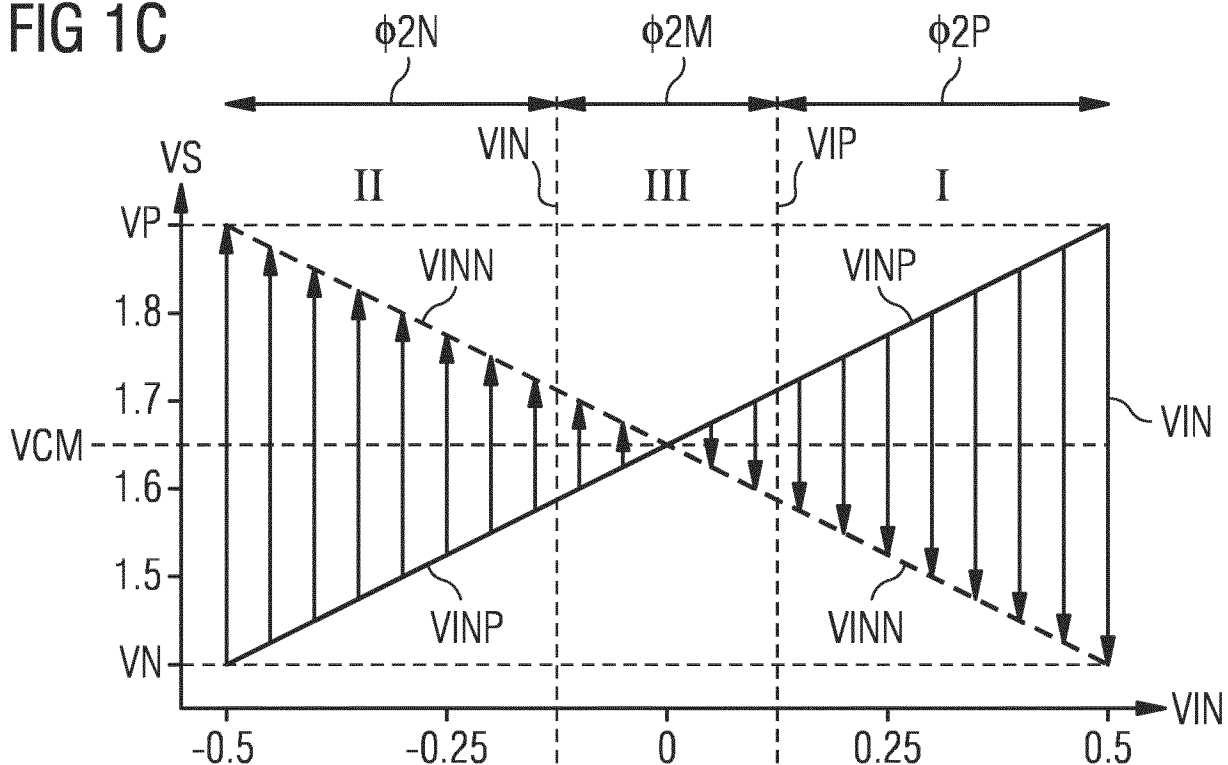


FIG 1D

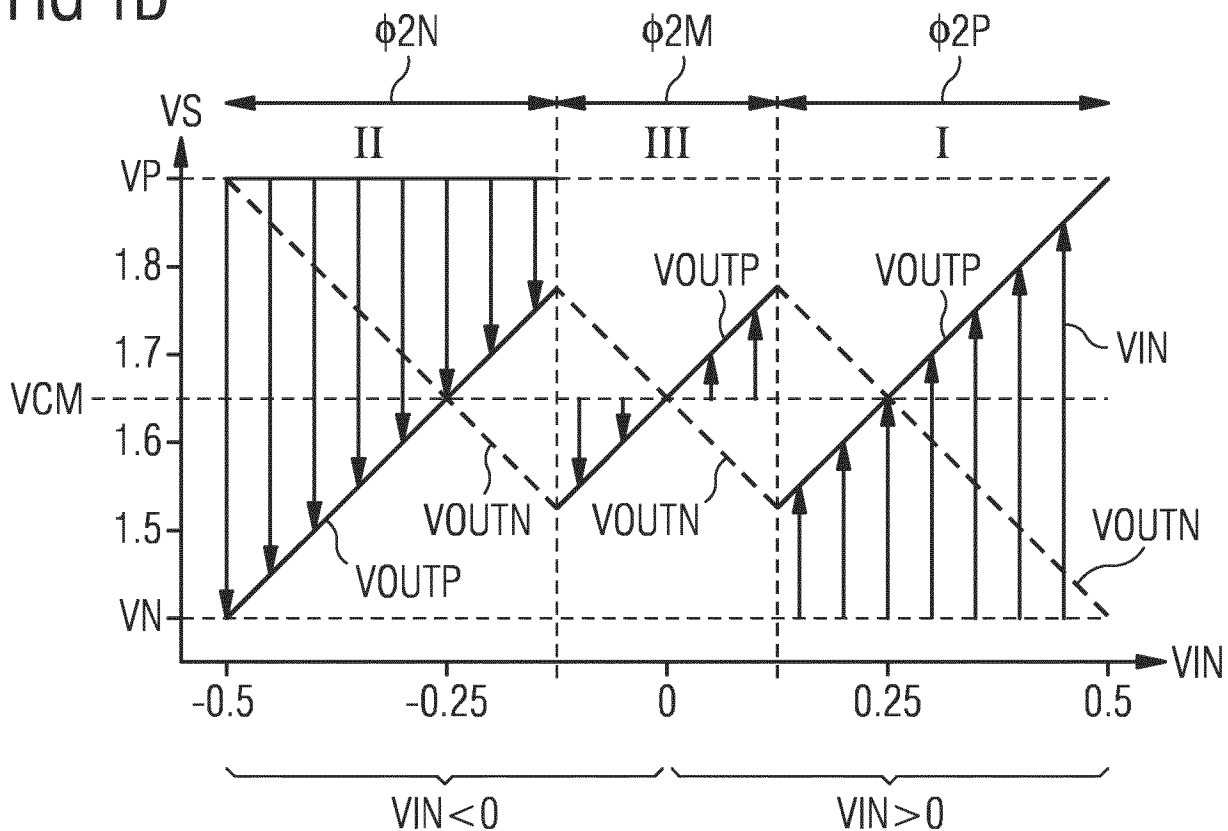


FIG 2B

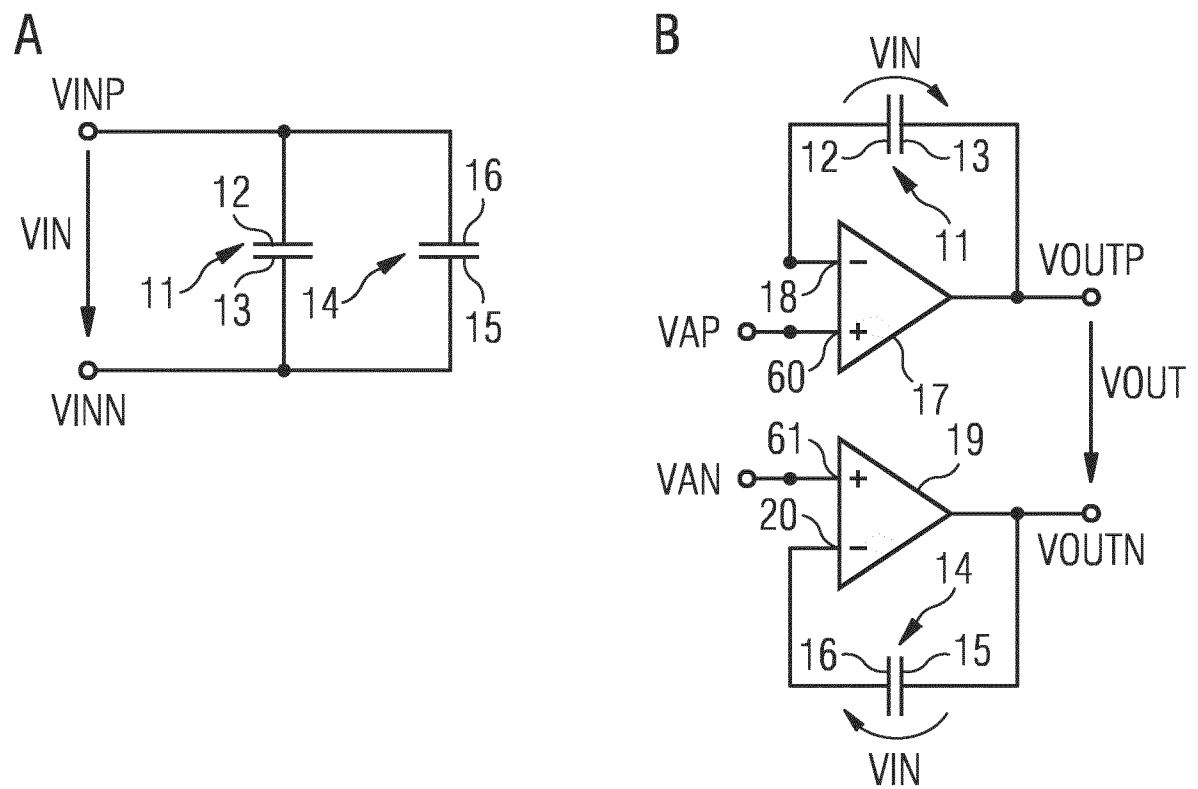


FIG 3

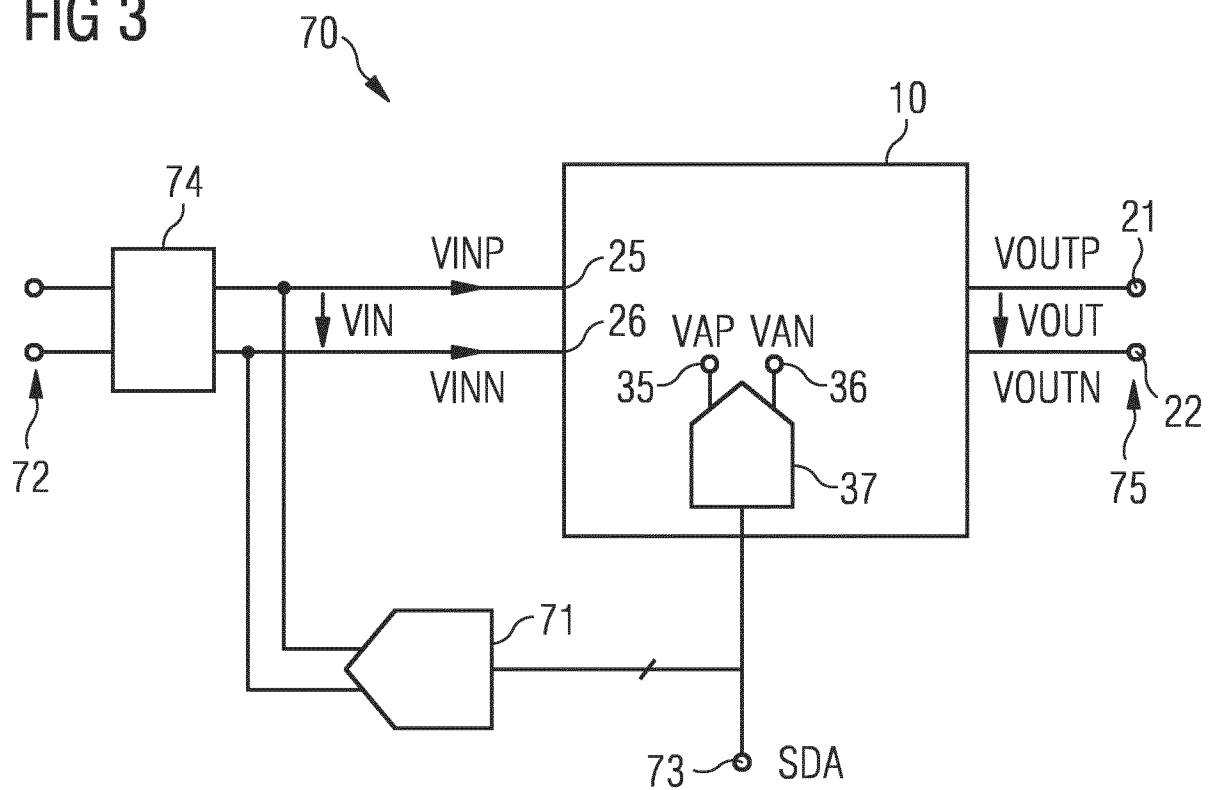
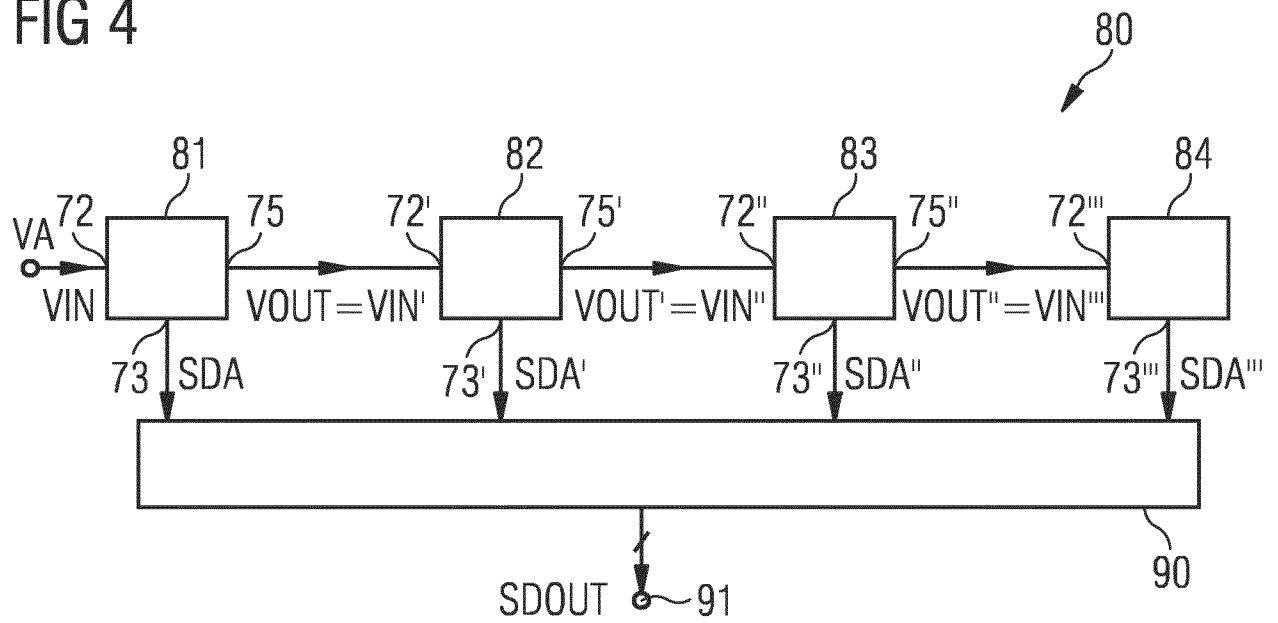


FIG 4



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2017/070066

A. CLASSIFICATION OF SUBJECT MATTER INV. H03F3/00 G11C27/02 H03F3/45 H03M1/44 ADD.		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H03F G11C H03M		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/237710 A1 (FAGG RUSSELL JOHN [US] ET AL) 23 September 2010 (2010-09-23) paragraphs [0001], [0002], [0016] - [0028]; figure 2 -----	1-15
X	US 8 299 837 B1 (LIN JIN-FU [TW]) 30 October 2012 (2012-10-30) column 3, line 3 - column 6, line 24; figure 1 -----	1-15
A	US 7 724 063 B1 (CHANG SOON-JYH [TW] ET AL) 25 May 2010 (2010-05-25) column 2, line 19 - column 3, line 6; figure 6 -----	1-15
<div style="display: flex; justify-content: space-between;"> <div> ☐ Further documents are listed in the continuation of Box C. </div> <div> ☒ See patent family annex. </div> </div>		
<div style="display: flex;"> <div style="flex: 1;"> <p>* Special categories of cited documents :</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier application or patent but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> </div> <div style="flex: 1;"> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</p> <p>"&" document member of the same patent family</p> </div> </div>		
Date of the actual completion of the international search <div style="text-align: center; font-size: 1.2em;">2 October 2017</div>		Date of mailing of the international search report <div style="text-align: center; font-size: 1.2em;">18/10/2017</div>
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer <div style="text-align: center; font-size: 1.2em;">Goethals, Filip</div>

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2017/070066

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