



(51) International Patent Classification:

H04N 1/60 (2006.01)

G06T 7/60 (2017.01)

H04N 1/32 (2006.01)

G06Q 30/00 (2012.01)

(21) International Application Number:

PCT/US2021/016337

(22) International Filing Date:

03 February 2021 (03.02.2021)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

16/890,270

02 June 2020 (02.06.2020)

US

(71) Applicant: WESTERN DIGITAL TECHNOLOGIES, INC. [US/US]; 5601 Great Oaks Parkway, San Jose, CA 95119 (US).

(72) Inventor: AGARWAL, Dinesh, Kumar; c/o Western Digital Technologies, Inc., 5601 Great Oaks Parkway, San Jose, CA 95119 (US).

(74) Agent: HETZ, Joseph, F.; Brinks Gilson & Lione, P.O. Box 10087, Chicago, IL 60610 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: STORAGE SYSTEM AND METHOD FOR HOST-ASSISTED MEMORY BLOCK COLOR CODING FOR FASTER MEDIA SEARCH

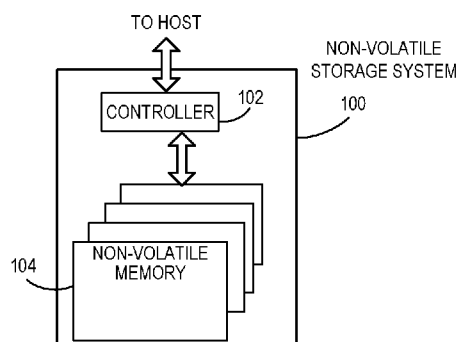


FIG. 1A

(57) Abstract: A storage system and method for host-assisted memory block color coding for faster media search are provided. In one embodiment, a controller of the storage system is configured to receive an image and color properties of the image from a host and store the image in an area of memory associated with the color properties. Other embodiments are provided.

Storage System and Method for Host-Assisted Memory Block Color Coding for Faster Media Search

Background

[0001] A host with an image capture device (e.g., a mobile phone with a digital camera or a dedicated digital camera) can capture and send images to a storage system for storage. The storage system typically stores images sequentially in the memory in the order in which they are received from the host.

Brief Description of the Drawings

[0002] Figure 1A is a block diagram of a non-volatile storage system of an embodiment.

[0003] Figure 1B is a block diagram illustrating a storage module of an embodiment.

[0004] Figure 1C is a block diagram illustrating a hierarchical storage system of an embodiment.

[0005] Figure 2A is a block diagram illustrating components of the controller of the non-volatile storage system illustrated in Figure 1A according to an embodiment.

[0006] Figure 2B is a block diagram illustrating components of the non-volatile memory storage system illustrated in Figure 1A according to an embodiment.

[0007] Figure 3 is a block diagram of a host and storage system of an embodiment.

[0008] Figure 4 is an illustration of a sequential image storage method.

[0009] Figure 5 is a block diagram of a host and storage system of an embodiment that illustrates a method for host-assisted memory block color coding for faster media search.

[0010] Figure 6 is an illustration of a memory block color coding process of an embodiment.

[0011] Figure 7 is an illustration of a method of an embodiment for storing multiple images with similar color characteristics across multiple dies/channel in memory.

[0012] Figure 8A is an illustration of a serial storage and retrieval mechanism.

[0013] Figure 8B is an illustration of a parallel storage and retrieval mechanism of an embodiment.

Detailed Description

[0014] Overview

[0015] By way of introduction, the below embodiments relate to a storage system and method for host-assisted memory block color coding for faster media search. In one embodiment, a storage system is provided comprising a memory and a controller. The controller is configured to receive an image and color properties of the image from a host and store the image in an area of the memory associated with the color properties.

[0016] In some embodiments, the color properties of the image are provided in a color histogram.

[0017] In some embodiments, the controller is further configured to designate a plurality of areas of the memory with respective color codes.

[0018] In some embodiments, the controller is further configured to identify the area of the memory to store the image by matching the color properties of the image with the color code of the area of the memory.

[0019] In some embodiments, the plurality of areas of the memory comprises blocks.

[0020] In some embodiments, the plurality of areas of the memory comprises wordlines.

[0021] In some embodiments, the controller is further configured to store images with similar color properties across multiple memory dies or channels of the memory.

[0022] In some embodiments, the controller is further configured to inform the host of a plurality of stored images with similar color properties.

[0023] In some embodiments, the memory comprises a three-dimensional memory.

[0024] In another embodiment, a method is provided that is performed in a host in communication with a storage system comprising a memory. The method comprises: determining color properties associated with an image; and sending the image and the determined color properties of the image to the storage system for storage in an area of the memory associated with the color properties.

[0025] In some embodiments, the color properties of the image are provided in a color histogram.

[0026] In some embodiments, the method further comprises receiving information from the storage system regarding a plurality of stored images with similar color properties.

[0027] In some embodiments, the method further comprises grouping the plurality of stored images together for compression.

[0028] In another embodiment, a storage system is provided comprising a memory and means for storing an image in a region of the memory associated with color characteristics of the image.

[0029] In some embodiments, the color characteristics of the image are provided in a color histogram.

[0030] In some embodiments, the storage system further comprises means for marking a plurality of regions of memory with respective color codes.

[0031] In some embodiments, the storage system further comprises means for choosing the region of the memory to store the image by matching the color characteristics of the image with the color code of the region of the memory.

[0032] In some embodiments, the storage system further comprises means for storing images with similar color characteristics across multiple memory dies or channels of the memory.

[0033] In some embodiments, the storage system further comprises means for informing the host of a plurality of stored images with similar color characteristics.

[0034] In some embodiments, the memory comprises a three-dimensional memory.

[0035] Other embodiments are possible, and each of the embodiments can be used alone or together in combination. Accordingly, various embodiments will now be described with reference to the attached drawings.

[0036] Embodiments

[0037] Storage systems suitable for use in implementing aspects of these embodiments are shown in Figures 1A-1C. Figure 1A is a block diagram illustrating a non-volatile storage system 100 according to an embodiment of the subject matter described herein. Referring to Figure 1A, non-volatile storage system 100 includes a controller 102 and non-volatile memory that may be made up of one or more non-volatile memory die 104. As used herein, the term die refers to the collection of non-volatile memory cells, and

associated circuitry for managing the physical operation of those non-volatile memory cells, that are formed on a single semiconductor substrate. Controller 102 interfaces with a host system and transmits command sequences for read, program, and erase operations to non-volatile memory die 104.

[0038] The controller 102 (which may be a non-volatile memory controller (e.g., a flash, resistive random-access memory (ReRAM), phase-change memory (PCM), or magnetoresistive random-access memory (MRAM) controller)) can take the form of processing circuitry, a microprocessor or processor, and a computer-readable medium that stores computer-readable program code (e.g., firmware) executable by the (micro)processor, logic gates, switches, an application specific integrated circuit (ASIC), a programmable logic controller, and an embedded microcontroller, for example. The controller 102 can be configured with hardware and/or firmware to perform the various functions described below and shown in the flow diagrams. Also, some of the components shown as being internal to the controller can also be stored external to the controller, and other components can be used. Additionally, the phrase “operatively in communication with” could mean directly in communication with or indirectly (wired or wireless) in communication with through one or more components, which may or may not be shown or described herein.

[0039] As used herein, a non-volatile memory controller is a device that manages data stored on non-volatile memory and communicates with a host, such as a computer or electronic device. A non-volatile memory controller can have various functionality in addition to the specific functionality described herein. For example, the non-volatile memory controller can format the non-volatile memory to ensure the memory is operating properly, map out bad non-volatile memory cells, and allocate spare cells to be substituted for future failed cells. Some part of the spare cells can be used to hold firmware to operate the non-volatile memory controller and implement other features. In operation, when a host needs to read data from or write data to the non-volatile memory, it can communicate with the non-volatile memory controller. If the host provides a logical address to which data is to be read/written, the non-volatile memory controller can convert the logical address received from the host to a physical address in the non-volatile memory. (Alternatively, the host can provide the physical address.) The non-

volatile memory controller can also perform various memory management functions, such as, but not limited to, wear leveling (distributing writes to avoid wearing out specific blocks of memory that would otherwise be repeatedly written to) and garbage collection (after a block is full, moving only the valid pages of data to a new block, so the full block can be erased and reused).

[0040] Non-volatile memory die 104 may include any suitable non-volatile storage medium, including resistive random-access memory (ReRAM), magnetoresistive random-access memory (MRAM), phase-change memory (PCM), NAND flash memory cells and/or NOR flash memory cells. The memory cells can take the form of solid-state (e.g., flash) memory cells and can be one-time programmable, few-time programmable, or many-time programmable. The memory cells can also be single-level cells (SLC), multiple-level cells (MLC), triple-level cells (TLC), or use other memory cell level technologies, now known or later developed. Also, the memory cells can be fabricated in a two-dimensional or three-dimensional fashion.

[0041] The interface between controller 102 and non-volatile memory die 104 may be any suitable flash interface, such as Toggle Mode 200, 400, or 800. In one embodiment, storage system 100 may be a card based system, such as a secure digital (SD) or a micro secure digital (micro-SD) card. In an alternate embodiment, storage system 100 may be part of an embedded storage system.

[0042] Although, in the example illustrated in Figure 1A, non-volatile storage system 100 (sometimes referred to herein as a storage module) includes a single channel between controller 102 and non-volatile memory die 104, the subject matter described herein is not limited to having a single memory channel. For example, in some storage system architectures (such as the ones shown in Figures 1B and 1C), 2, 4, 8 or more memory channels may exist between the controller and the memory device, depending on controller capabilities. In any of the embodiments described herein, more than a single channel may exist between the controller and the memory die, even if a single channel is shown in the drawings.

[0043] Figure 1B illustrates a storage module 200 that includes plural non-volatile storage systems 100. As such, storage module 200 may include a storage controller 202 that interfaces with a host and with storage system 204, which includes a plurality of non-

volatile storage systems 100. The interface between storage controller 202 and non-volatile storage systems 100 may be a bus interface, such as a serial advanced technology attachment (SATA), peripheral component interconnect express (PCIe) interface, or double-data-rate (DDR) interface. Storage module 200, in one embodiment, may be a solid state drive (SSD), or non-volatile dual in-line memory module (NVDIMM), such as found in server PC or portable computing devices, such as laptop computers, and tablet computers.

[0044] Figure 1C is a block diagram illustrating a hierarchical storage system. A hierarchical storage system 250 includes a plurality of storage controllers 202, each of which controls a respective storage system 204. Host systems 252 may access memories within the storage system via a bus interface. In one embodiment, the bus interface may be a Non-Volatile Memory Express (NVMe) or fiber channel over Ethernet (FCoE) interface. In one embodiment, the system illustrated in Figure 1C may be a rack mountable mass storage system that is accessible by multiple host computers, such as would be found in a data center or other location where mass storage is needed.

[0045] Figure 2A is a block diagram illustrating components of controller 102 in more detail. Controller 102 includes a front end module 108 that interfaces with a host, a back end module 110 that interfaces with the one or more non-volatile memory die 104, and various other modules that perform functions which will now be described in detail. A module may take the form of a packaged functional hardware unit designed for use with other components, a portion of a program code (e.g., software or firmware) executable by a (micro)processor or processing circuitry that usually performs a particular function of related functions, or a self-contained hardware or software component that interfaces with a larger system, for example. Modules of the controller 102 can be implemented in hardware and/or software (e.g., in a processor executing computer-readable program code) to implement the methods and algorithms described below.

[0046] Referring again to modules of the controller 102, a buffer manager/bus controller 114 manages buffers in random access memory (RAM) 116 and controls the internal bus arbitration of controller 102. A read only memory (ROM) 118 stores system boot code. Although illustrated in Figure 2A as located separately from the controller 102, in other embodiments one or both of the RAM 116 and ROM 118 may be located

within the controller. In yet other embodiments, portions of RAM and ROM may be located both within the controller 102 and outside the controller.

[0047] Front end module 108 includes a host interface 120 and a physical layer interface (PHY) 122 that provide the electrical interface with the host or next level storage controller. The choice of the type of host interface 120 can depend on the type of memory being used. Examples of host interfaces 120 include, but are not limited to, SATA, SATA Express, serially attached small computer system interface (SAS), Fibre Channel, universal serial bus (USB), PCIe, and NVMe. The host interface 120 typically facilitates transfer for data, control signals, and timing signals.

[0048] Back end module 110 includes an error correction code (ECC) engine 124 that encodes the data bytes received from the host, and decodes and error corrects the data bytes read from the non-volatile memory. A command sequencer 126 generates command sequences, such as program and erase command sequences, to be transmitted to non-volatile memory die 104. A RAID (Redundant Array of Independent Drives) module 128 manages generation of RAID parity and recovery of failed data. The RAID parity may be used as an additional level of integrity protection for the data being written into the memory device 104. In some cases, the RAID module 128 may be a part of the ECC engine 124. A memory interface 130 provides the command sequences to non-volatile memory die 104 and receives status information from non-volatile memory die 104. In one embodiment, memory interface 130 may be a double data rate (DDR) interface, such as a Toggle Mode 200, 400, or 800 interface. A flash control layer 132 controls the overall operation of back end module 110.

[0049] The storage system 100 also includes other discrete components 140, such as external electrical interfaces, external RAM, resistors, capacitors, or other components that may interface with controller 102. In alternative embodiments, one or more of the physical layer interface 122, RAID module 128, media management layer 138 and buffer management/bus controller 114 are optional components that are not necessary in the controller 102.

[0050] Figure 2B is a block diagram illustrating components of non-volatile memory die 104 in more detail. Non-volatile memory die 104 includes peripheral circuitry 141 and non-volatile memory array 142. Non-volatile memory array 142 includes the non-

volatile memory cells used to store data. The non-volatile memory cells may be any suitable non-volatile memory cells, including ReRAM, MRAM, PCM, NAND flash memory cells and/or NOR flash memory cells in a two dimensional and/or three dimensional configuration. Non-volatile memory die 104 further includes a data cache 156 that caches data. Peripheral circuitry 141 includes a state machine 152 that provides status information to the controller 102.

[0051] Returning again to Figure 2A, the flash control layer 132 (which will be referred to herein as the flash translation layer (FTL) or, more generally, the “media management layer,” as the memory may not be flash) handles flash errors and interfaces with the host. In particular, the FTL, which may be an algorithm in firmware, is responsible for the internals of memory management and translates writes from the host into writes to the memory 104. The FTL may be needed because the memory 104 may have limited endurance, may only be written in multiples of pages, and/or may not be written unless it is erased as a block. The FTL understands these potential limitations of the memory 104, which may not be visible to the host. Accordingly, the FTL attempts to translate the writes from host into writes into the memory 104.

[0052] The FTL may include a logical-to-physical address (L2P) map and allotted cache memory. In this way, the FTL translates logical block addresses (“LBAs”) from the host to physical addresses in the memory 104. The FTL can include other features, such as, but not limited to, power-off recovery (so that the data structures of the FTL can be recovered in the event of a sudden power loss) and wear leveling (so that the wear across memory blocks is even to prevent certain blocks from excessive wear, which would result in a greater chance of failure).

[0053] Turning again to the drawings, Figure 3 is a block diagram of a host 300 and storage system (sometimes referred to herein as a device) 100 of an embodiment. The host 300 can take any suitable form, including, but not limited to, a computer, a mobile phone, a digital camera, a tablet, a wearable device, a digital video recorder, a surveillance system, etc. In one embodiment, the host 300 comprises an image capture device 390 (e.g., a camera) to take a picture, and the processor 330 generates a digital image representing that picture. The image can be stored in the memory 340 prior to

sending the image to the storage system 100 (e.g., a memory card or an embedding storage device) for storage.

[0054] As mentioned above, a host with an image capture device (e.g., a mobile phone with a digital camera or a dedicated digital camera) can capture and send images to a storage system for storage. The storage system typically stores images sequentially in the memory in the order in which they are received from the host. However, the host can read any set of images in any order. With increasing storage system (e.g., card/drive/solid-state drive (SSD)) capacity, the time to access the memory (media) becomes increasingly important. If images are not organized properly in the memory, access to the images can become serial, which is time consuming. For example, as shown in Figure 4, images received from a host that are stored sequentially over two blocks in memory may not be optimal for future host reads.

[0055] The following embodiments can be used to organize images in the memory better from the start of media writes by storing similar images in a similar set of blocks. This makes it easier to later access the content at a faster rate, and the properties used to identify which areas of memory to store the images can be utilized by various applications to optimize usage of the storage system.

[0056] In general, in this embodiment, the controller 102 of the storage system 100 marks units of memory (e.g., blocks) with a color code. When providing an image to the storage system 100 for storage in the memory 104, the host 300 also provides color characteristics or properties of the image. The color characteristics or properties can be presented in a color histogram, which is a representation of the distribution of colors in an image. For a digital image, a color histogram can represent the number of pixels that have colors in each of a fixed list of color ranges that span the image's color space (i.e., the set of all possible colors). While a color histogram will be used in the below examples, it should be understood that color characteristics or properties can be presented in other ways.

[0057] The controller 102 in the storage system 100 then identifies a block in the memory 104 to store the image by searching blocks whose color code matches the image's color properties. The match can be an exact match or a match within a certain tolerance level. The controller 102 then routes and stores the image in the corresponding

set of color coded blocks. In this way, a set of blocks is marked with a certain color code will contain images with a matching color code. As will be discussed in more detail below, the controller 102 can store images with similar content/color codes across multiple dies/channels in the memory 104 to provide parallelism for future usage.

[0058] The following paragraphs described one example implementation of these embodiments for utilizing color properties of an image to organize the images in memory; specifically, by using host-provided color hints to route images to blocks with the best-matching color code. It should be understood that this is merely an example, and other implementations can be used.

[0059] Returning to the drawings, Figure 5 is a block diagram of a host 300 and storage system 100 of an embodiment for host-assisted memory block color coding for faster media search. As shown in Figure 5, when the host 300 sends an image to the storage system 100 for storage (act 510), the host 300 also provides an indication about the color properties (e.g., a color histogram) of the image (act 520). The controller 102 in the storage system 100 uses this indication to store the image in the appropriate block in the memory 104. Later, an application in the host 300 sends a request to the storage system 100 to retrieve the image. In response, the controller 102 retrieves the image from the memory 104 and provides it to the host 300 (act 540). As will be discussed in more detail below, the controller 102 can perform predictive loading in parallel and send a hint to the host 300. For example, when the storage system 100 has multiple sets of images with similar content/color properties, optionally, it can notify the host 300 to take some action.

[0060] As mentioned above, in one embodiment, the controller 102 of the storage system 100 color codes blocks of the memory 104. Figure 6 illustrates an example color coding process. As shown in Figure 6, in this example, for each block, the color property keeps varying. If the memory 104 has a large number of blocks, then color coding can be done at a very-fine granularity for better prediction. For example, the granularity can go to the wordline level. However, managing color coding at the block level may be easier if it is the erase unit of the memory 104.

[0061] As also mentioned above and as shown in Figure 7, when multiple images with similar color characteristic are written to the memory 104, the image can be written

across multiple dies/channel in the memory 104 in anticipation that these images will be later requested simultaneously. By writing the images to provide for maximum parallelism, the storage system 100 can send the images to the host 300 with minimal latencies. An example of this is discussed in more detail below.

[0062] As can be seen by the above example, utilizing the color properties of an image and routing the image to the appropriate blocks in the memory 104 organizes the images better in the memory 104 for faster host access. Figures 8A and 8B are diagrams that illustrate this comparison. Figure 8A is an illustration of a serial storage and retrieval mechanism. As shown in Figure 8A, images 1-4 are stored serially in the memory. Thus, when the images are retrieved, they are transferred to the host serially. This requires a relatively long time. Figure 8B is an illustration of a parallel storage and retrieval mechanism of an embodiment. As shown in Figure 8B, images having similar color characteristics are stored together and across memory dies/channels. This allows for parallel loading and transfer, which provides faster access than the serial method.

[0063] There are several advantages associated with these embodiments. For example, these embodiments can be extended to multiple media types by using similar properties and are applicable for mixed content as well as where a specific set of blocks are used for media, and other blocks can be used normally.

[0064] Once the host 300 knows about the similar content, it can use a hint provided by the storage system 100 to perform an image search better and can apply more complex algorithms for compression and other similar applications. For example, regarding faster image search for similar content, as shown in the above example, if img1 to img4 were stored randomly, loading and transfer time is very high. So, by storing images with the method of these embodiments, the storage system 100 can transfer data at a faster rate. Further, generally speaking, the browsing of images also involves loading similar images to display next to each other, so the accelerated loading benefite can make that user experience better. Also, as noted above, these embodiments can provide better compression. If the host 300 wants to compress images, the storage system 100 can provide the host 300 with a hint regarding which images can be clubbed for better compression. Addiiontally, these emboidments can provide an image recovery

mechanism. For example, if multiple dies store similar images, a similar image can be used from another die if one of the dies fails.

[0065] There are several alternatives that can be used with these embodiments. For example, if for some images, the color information from the host is not available at write time, these images can be written at a temporary location and can be routed to the appropriate blocks later in the background when the information is available either via the host, or the device can itself determine it. The same is true if there is not enough space blocks available in the appropriate color coded blocks. In another alternative, the color coding of the blocks is not fixed and can be changed dynamically based on device usage. For instance, if one color-specific image is written more than others, more blocks can be allocated to cover that range.

[0066] Finally, as mentioned above, any suitable type of memory can be used. Semiconductor memory devices include volatile memory devices, such as dynamic random access memory (“DRAM”) or static random access memory (“SRAM”) devices, non-volatile memory devices, such as resistive random access memory (“ReRAM”), electrically erasable programmable read only memory (“EEPROM”), flash memory (which can also be considered a subset of EEPROM), ferroelectric random access memory (“FRAM”), and magnetoresistive random access memory (“MRAM”), and other semiconductor elements capable of storing information. Each type of memory device may have different configurations. For example, flash memory devices may be configured in a NAND or a NOR configuration.

[0067] The memory devices can be formed from passive and/or active elements, in any combinations. By way of non-limiting example, passive semiconductor memory elements include ReRAM device elements, which in some embodiments include a resistivity switching storage element, such as an anti-fuse, phase change material, etc., and optionally a steering element, such as a diode, etc. Further by way of non-limiting example, active semiconductor memory elements include EEPROM and flash memory device elements, which in some embodiments include elements containing a charge storage region, such as a floating gate, conductive nanoparticles, or a charge storage dielectric material.

[0068] Multiple memory elements may be configured so that they are connected in series or so that each element is individually accessible. By way of non-limiting example, flash memory devices in a NAND configuration (NAND memory) typically contain memory elements connected in series. A NAND memory array may be configured so that the array is composed of multiple strings of memory in which a string is composed of multiple memory elements sharing a single bit line and accessed as a group. Alternatively, memory elements may be configured so that each element is individually accessible, e.g., a NOR memory array. NAND and NOR memory configurations are examples, and memory elements may be otherwise configured.

[0069] The semiconductor memory elements located within and/or over a substrate may be arranged in two or three dimensions, such as a two dimensional memory structure or a three dimensional memory structure.

[0070] In a two dimensional memory structure, the semiconductor memory elements are arranged in a single plane or a single memory device level. Typically, in a two dimensional memory structure, memory elements are arranged in a plane (e.g., in an x-z direction plane) which extends substantially parallel to a major surface of a substrate that supports the memory elements. The substrate may be a wafer over or in which the layer of the memory elements are formed or it may be a carrier substrate which is attached to the memory elements after they are formed. As a non-limiting example, the substrate may include a semiconductor such as silicon.

[0071] The memory elements may be arranged in the single memory device level in an ordered array, such as in a plurality of rows and/or columns. However, the memory elements may be arrayed in non-regular or non-orthogonal configurations. The memory elements may each have two or more electrodes or contact lines, such as bit lines and wordlines.

[0072] A three dimensional memory array is arranged so that memory elements occupy multiple planes or multiple memory device levels, thereby forming a structure in three dimensions (i.e., in the x, y and z directions, where the y direction is substantially perpendicular and the x and z directions are substantially parallel to the major surface of the substrate).

[0073] As a non-limiting example, a three dimensional memory structure may be vertically arranged as a stack of multiple two dimensional memory device levels. As another non-limiting example, a three dimensional memory array may be arranged as multiple vertical columns (e.g., columns extending substantially perpendicular to the major surface of the substrate, i.e., in the y direction) with each column having multiple memory elements in each column. The columns may be arranged in a two dimensional configuration, e.g., in an x-z plane, resulting in a three dimensional arrangement of memory elements with elements on multiple vertically stacked memory planes. Other configurations of memory elements in three dimensions can also constitute a three dimensional memory array.

[0074] By way of non-limiting example, in a three dimensional NAND memory array, the memory elements may be coupled together to form a NAND string within a single horizontal (e.g., x-z) memory device levels. Alternatively, the memory elements may be coupled together to form a vertical NAND string that traverses across multiple horizontal memory device levels. Other three dimensional configurations can be envisioned wherein some NAND strings contain memory elements in a single memory level while other strings contain memory elements which span through multiple memory levels. Three dimensional memory arrays may also be designed in a NOR configuration and in a ReRAM configuration.

[0075] Typically, in a monolithic three dimensional memory array, one or more memory device levels are formed above a single substrate. Optionally, the monolithic three dimensional memory array may also have one or more memory layers at least partially within the single substrate. As a non-limiting example, the substrate may include a semiconductor such as silicon. In a monolithic three dimensional array, the layers constituting each memory device level of the array are typically formed on the layers of the underlying memory device levels of the array. However, layers of adjacent memory device levels of a monolithic three dimensional memory array may be shared or have intervening layers between memory device levels.

[0076] Then again, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device having multiple layers of memory. For example, non-monolithic stacked memories can be constructed by forming

memory levels on separate substrates and then stacking the memory levels atop each other. The substrates may be thinned or removed from the memory device levels before stacking, but as the memory device levels are initially formed over separate substrates, the resulting memory arrays are not monolithic three dimensional memory arrays. Further, multiple two dimensional memory arrays or three dimensional memory arrays (monolithic or non-monolithic) may be formed on separate chips and then packaged together to form a stacked-chip memory device.

[0077] Associated circuitry is typically required for operation of the memory elements and for communication with the memory elements. As non-limiting examples, memory devices may have circuitry used for controlling and driving memory elements to accomplish functions such as programming and reading. This associated circuitry may be on the same substrate as the memory elements and/or on a separate substrate. For example, a controller for memory read-write operations may be located on a separate controller chip and/or on the same substrate as the memory elements.

[0078] One of skill in the art will recognize that this invention is not limited to the two dimensional and three dimensional structures described but cover all relevant memory structures within the spirit and scope of the invention as described herein and as understood by one of skill in the art.

[0079] It is intended that the foregoing detailed description be understood as an illustration of selected forms that the invention can take and not as a definition of the invention. It is only the following claims, including all equivalents, that are intended to define the scope of the claimed invention. Finally, it should be noted that any aspect of any of the embodiments described herein can be used alone or in combination with one another.

What is claimed is:

1. A storage system comprising:
a memory; and
a controller configured to:
receive an image and color properties of the image from a host; and
store the image in an area of the memory associated with the color properties.
2. The storage system of Claim 1, wherein the color properties of the image are provided in a color histogram.
3. The storage system of Claim 1, wherein the controller is further configured to designate a plurality of areas of the memory with respective color codes.
4. The storage system of Claim 3, wherein the controller is further configured to identify the area of the memory to store the image by matching the color properties of the image with the color code of the area of the memory.
5. The storage system of Claim 3, wherein the plurality of areas of the memory comprises blocks.
6. The storage system of Claim 3, wherein the plurality of areas of the memory comprises wordlines.

7. The storage system of Claim 1, wherein the controller is further configured to store images with similar color properties across multiple memory dies or channels of the memory.
8. The storage system of Claim 1, wherein the controller is further configured to inform the host of a plurality of stored images with similar color properties.
9. The storage system of Claim 1, wherein the memory comprises a three-dimensional memory.
10. A method comprising:
 - performing the following in a host in communication with a storage system comprising a memory:
 - determining color properties associated with an image; and
 - sending the image and the determined color properties of the image to the storage system for storage in an area of the memory associated with the color properties.
11. The method of Claim 10, wherein the color properties of the image are provided in a color histogram.

12. The method of Claim 10, further comprising receiving information from the storage system regarding a plurality of stored images with similar color properties.
13. The method of Claim 12, further comprising grouping the plurality of stored images together for compression.
14. A storage system comprising:
a memory; and
means for storing an image in a region of the memory associated with color characteristics of the image.
15. The storage system of Claim 14, wherein the color characteristics of the image are provided in a color histogram.
16. The storage system of Claim 14, further comprising means for marking a plurality of regions of memory with respective color codes.
17. The storage system of Claim 16, further comprising means for choosing the region of the memory to store the image by matching the color characteristics of the image with the color code of the region of the memory.

18. The storage system of Claim 14, further comprising means for storing images with similar color characteristics across multiple memory dies or channels of the memory.

19. The storage system of Claim 14, further comprising means for informing the host of a plurality of stored images with similar color characteristics.

20. The storage system of Claim 14, wherein the memory comprises a three-dimensional memory.

1/9

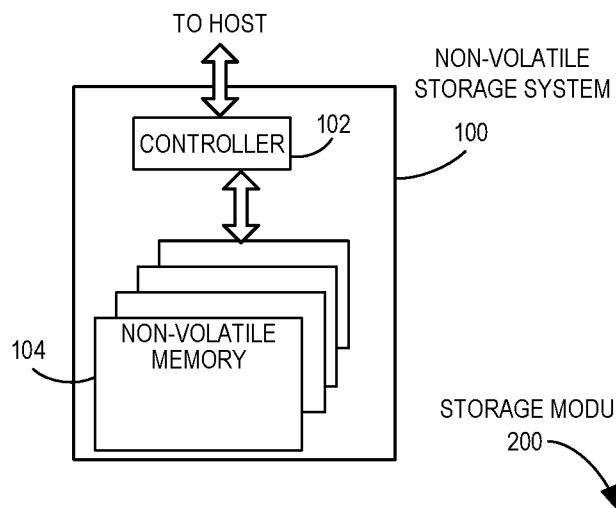


FIG. 1A

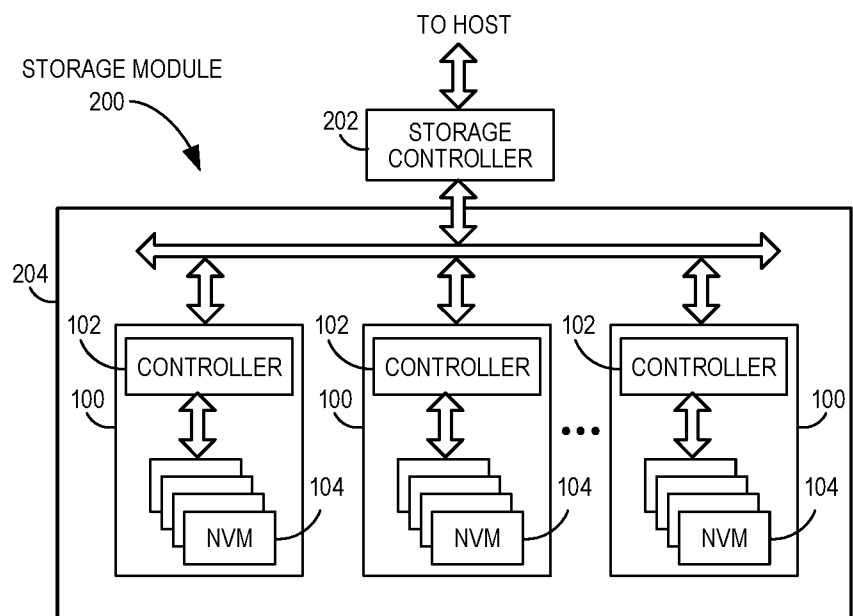


FIG. 1B

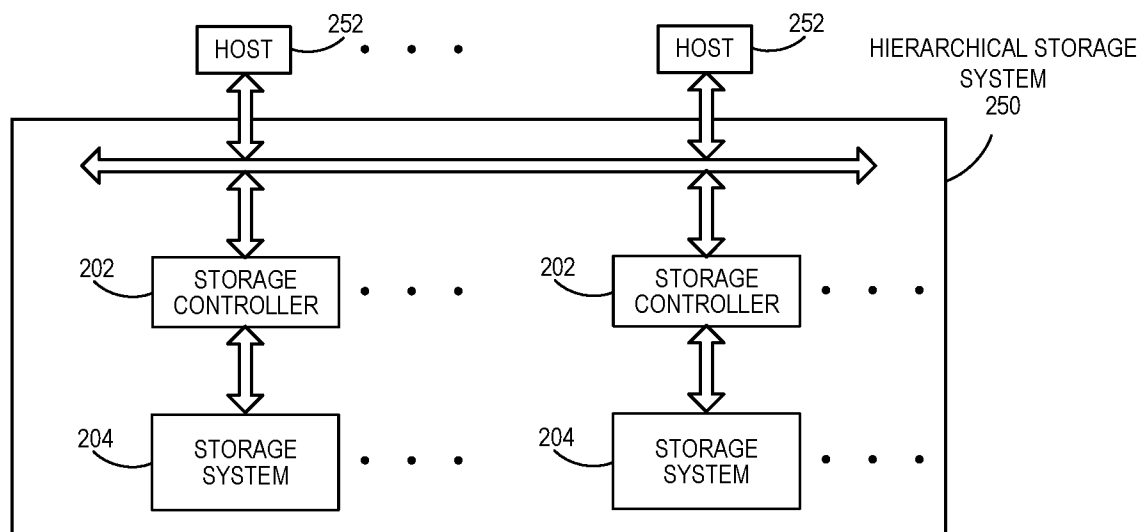


FIG. 1C

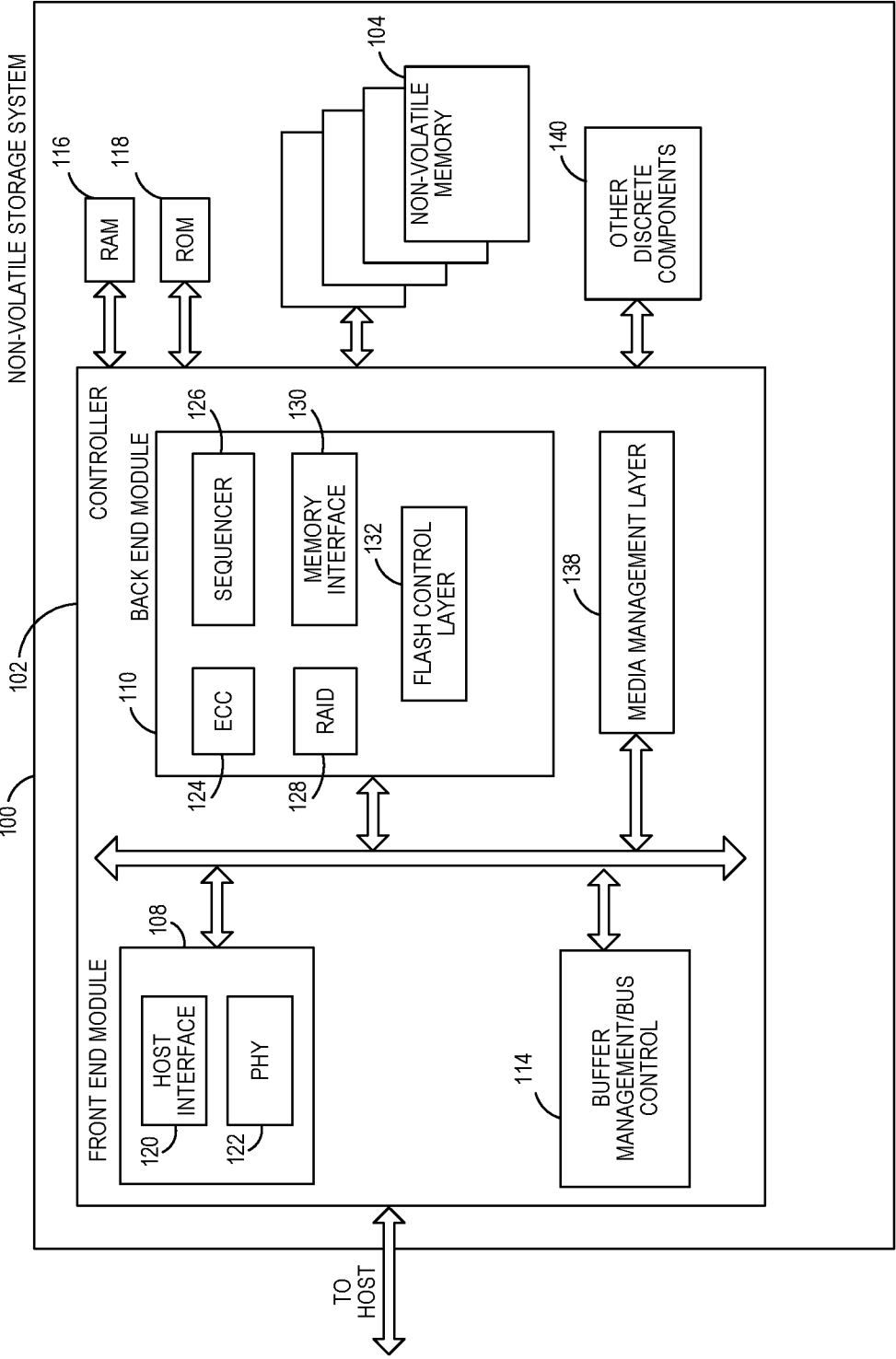


FIG. 2A

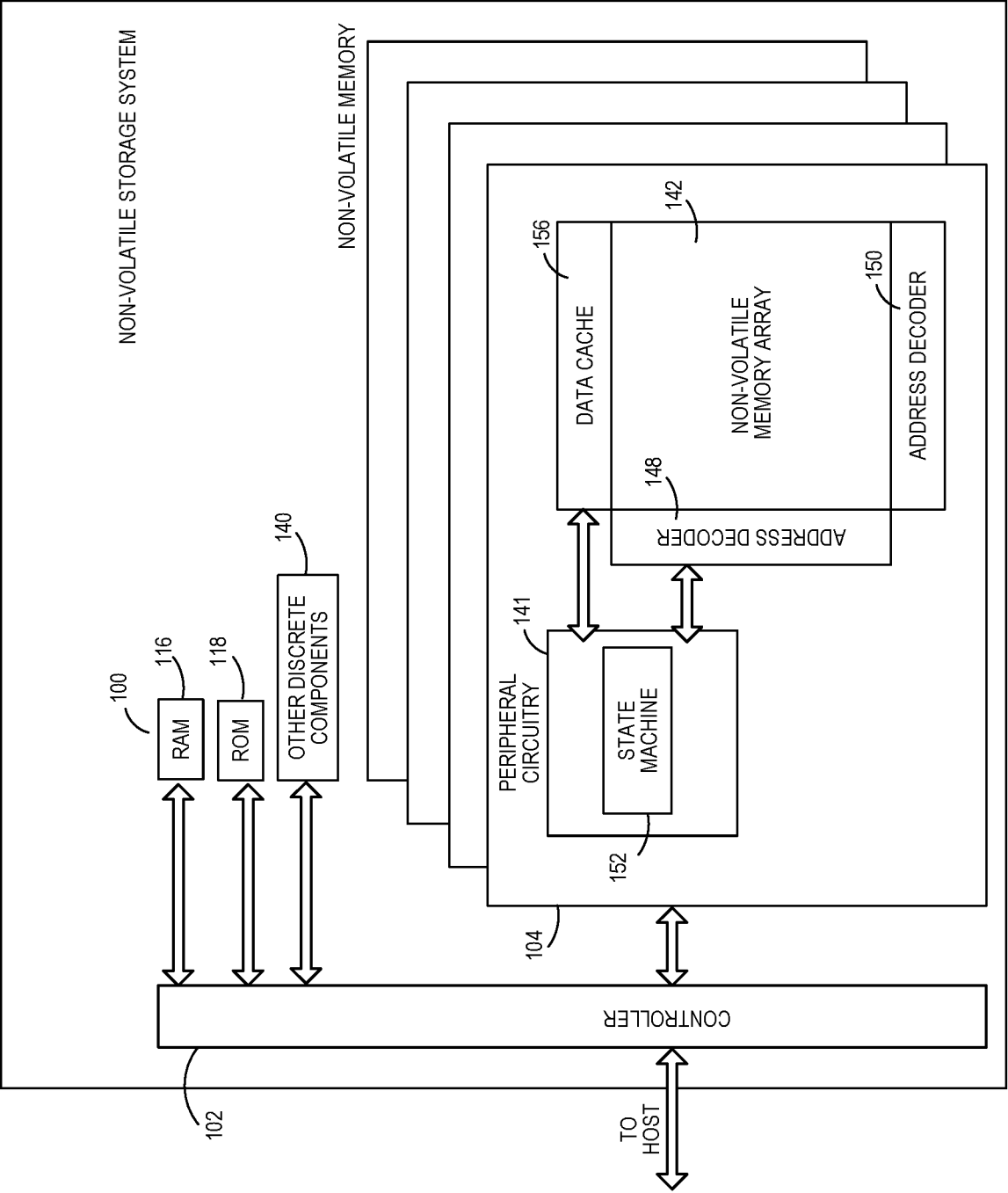


FIG. 2B

4/9

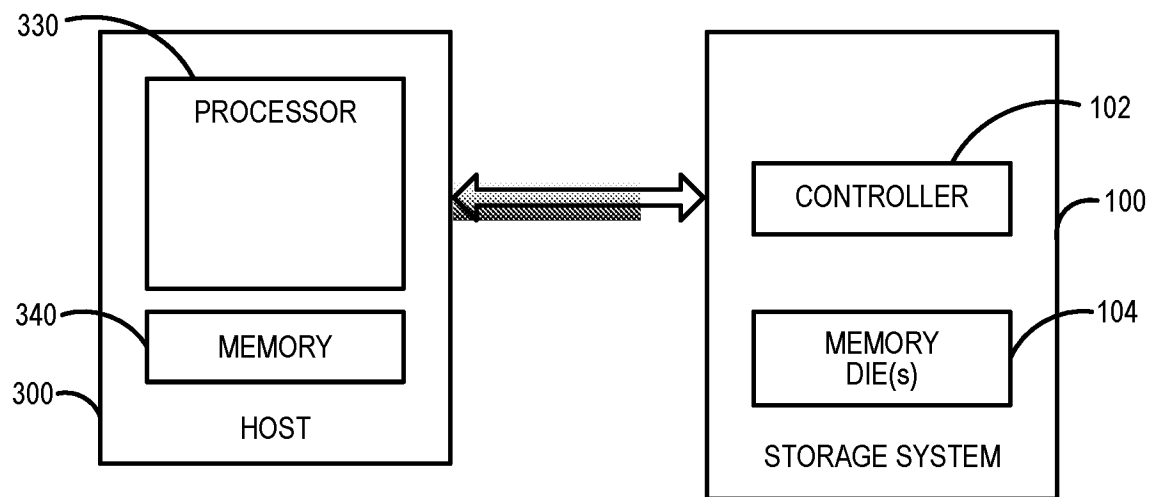


FIG. 3

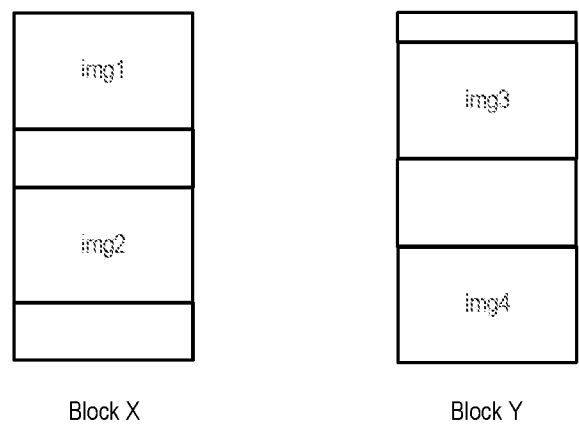


FIG. 4

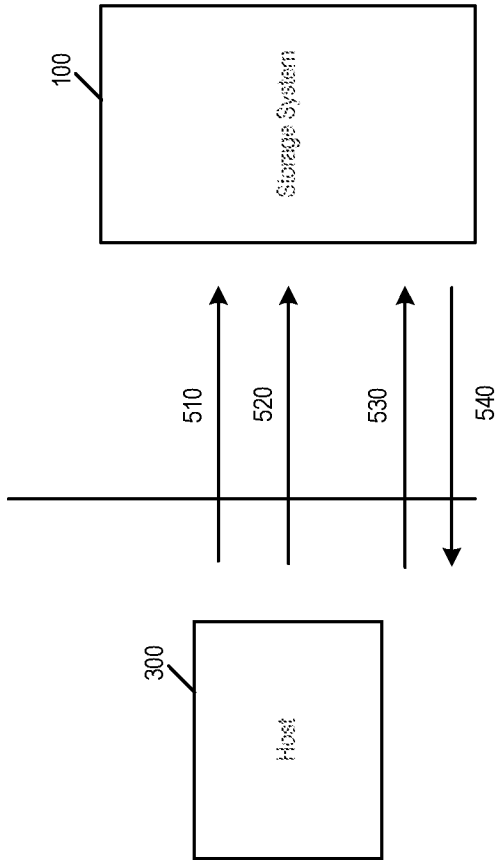


FIG. 5

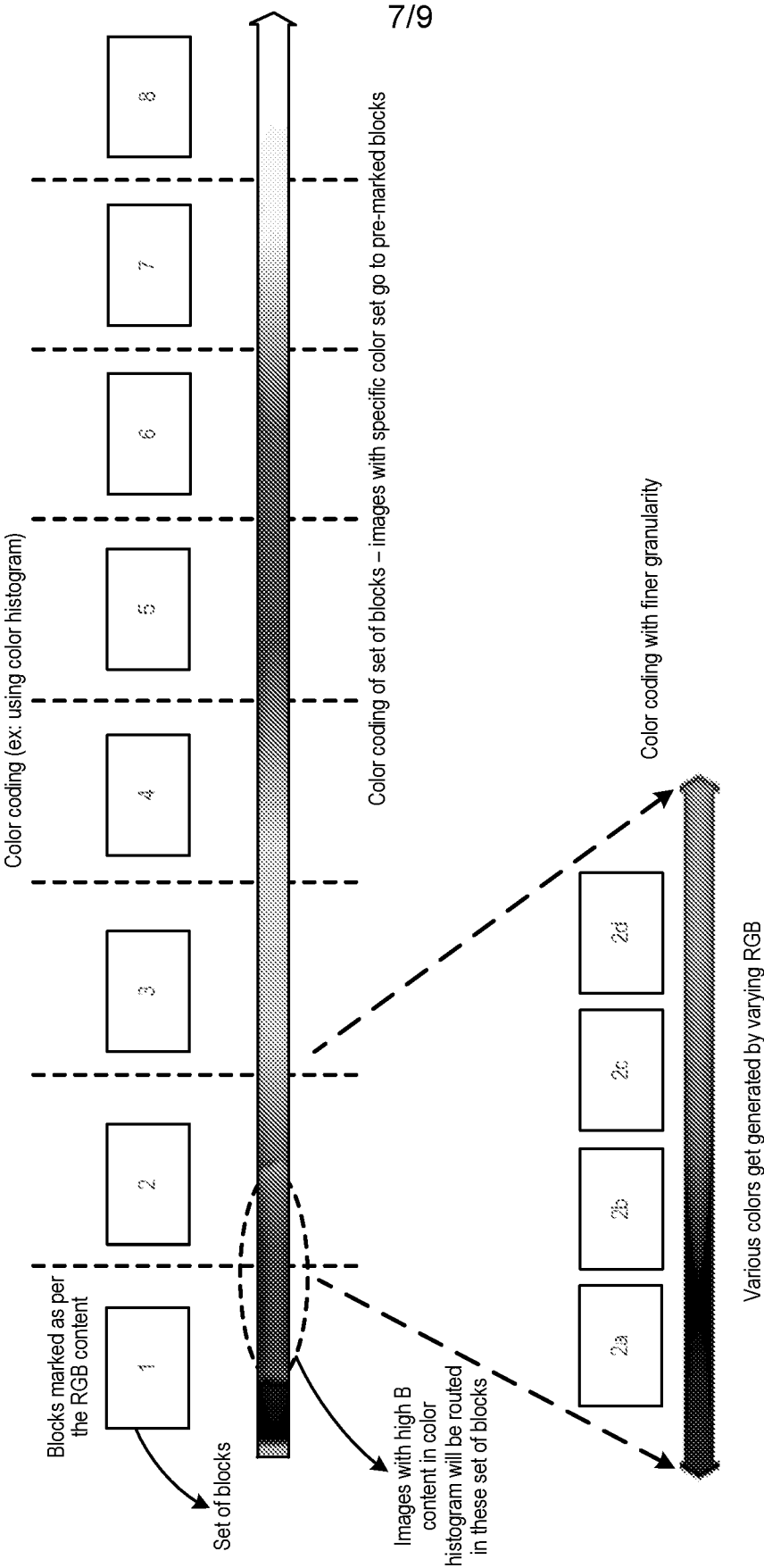


FIG. 6

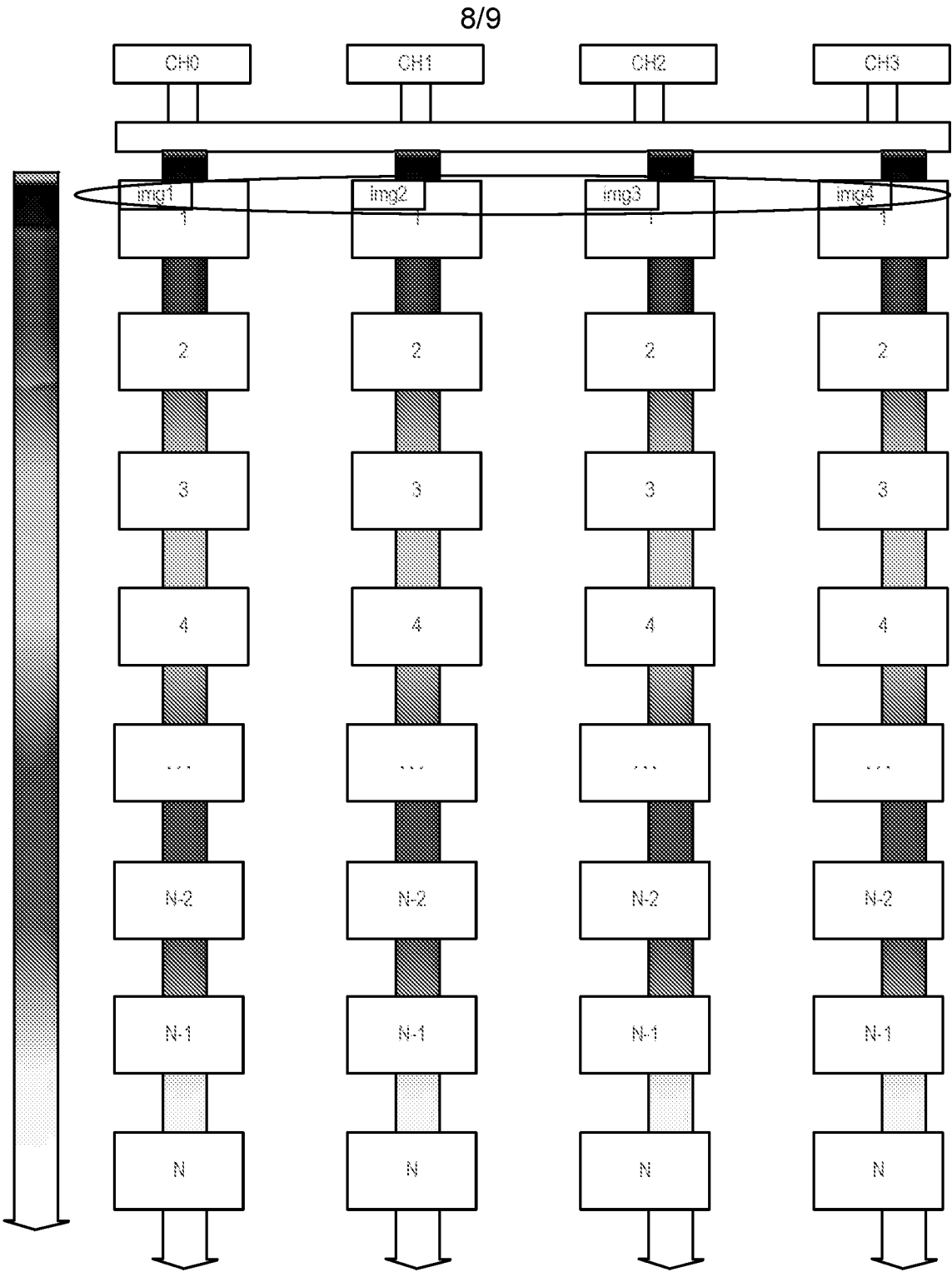


FIG. 7

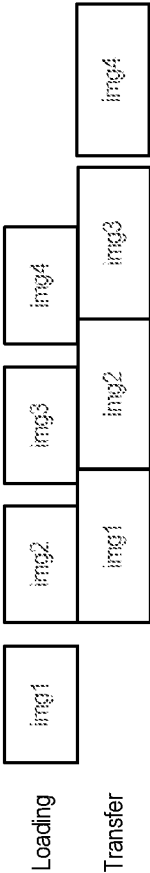


FIG. 8A

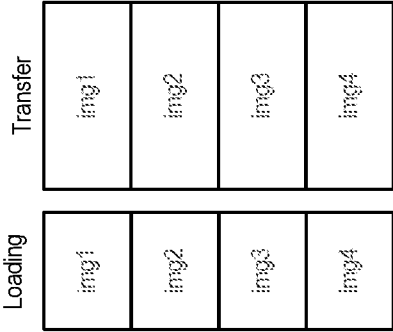


FIG. 8B

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2021/016337

A. CLASSIFICATION OF SUBJECT MATTER IPC (20210101) H04N 1/60, H04N 1/32, G06T 7/60, G06Q 30/00 CPC (20130101) H04N 1/60, H04N 1/32, G06T 7/60, G06Q 30/00 According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) IPC (20210101) H04N 1/60, H04N 1/32, G06T 7/60, G06Q 30/00 CPC (20130101) H04N 1/60, H04N 1/32, G06T 7/60, G06Q 30/00 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) Databases consulted: Esp@cenet, Google Patents, Orbit, Similari (AI-based)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Gong, Y., Chuan, C. H., & Xiaoyi, G. (1996). Image indexing and retrieval based on color histograms. Multimedia Tools and Applications, 2(2), 133-156 01 Mar 1996 (1996/03/01) The Whole document	1-20
A	AU 2019201268 B2 ZAZZLE INC 14 Mar 2019 (2019/03/14) The Whole document	1-20
A	CN 102905053 A CANON KK 30 Jan 2019 (2019/01/30) The Whole document	1-20
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "D" document cited by the applicant in the international application "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 27 May 2021		Date of mailing of the international search report 27 May 2021
Name and mailing address of the ISA: Israel Patent Office Technology Park, Bldg.5, Malcha, Jerusalem, 9695101, Israel Email address: pctoffice@justice.gov.il		Authorized officer LAHAV Ronen Telephone No. 972-73-3927215

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2021/016337

Patent document cited search report			Publication date	Patent family member(s)			Publication Date
AU	2019201268	B2	14 Mar 2019	AU	2019201268	A1	14 Mar 2019
				AU	2019201268	B2	12 Mar 2020
				AU	2014201404	A1	02 Oct 2014
				AU	2014201404	B2	22 Nov 2018
				BR	102014005996	A2	13 Dec 2016
				CA	2845601	A1	14 Sep 2014
				CN	104050657	A	17 Sep 2014
				EP	2779094	A2	17 Sep 2014
				EP	2779094	A3	29 Oct 2014
				EP	3660784	A1	03 Jun 2020
				JP	2014179090	A	25 Sep 2014
				JP	6382538	B2	29 Aug 2018
				US	8712566	B1	29 Apr 2014
				US	2014270506	A1	18 Sep 2014
				US	8958633	B2	17 Feb 2015
				US	2015262371	A1	17 Sep 2015
				US	9530217	B2	27 Dec 2016
				US	2017103539	A1	13 Apr 2017
				US	9905012	B2	27 Feb 2018
				US	2018182104	A1	28 Jun 2018
				US	10083517	B2	25 Sep 2018
CN	102905053	A	30 Jan 2019	CN	102905053	A	30 Jan 2013
				CN	102905053	B	27 Jan 2016
				CN	101867673	A	20 Oct 2010
				CN	101867673	B	14 Nov 2012
				JP	2010252037	A	04 Nov 2010
				JP	5538743	B2	02 Jul 2014
				US	2010265524	A1	21 Oct 2010
				US	9036199	B2	19 May 2015