

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
25 September 2008 (25.09.2008)

PCT

(10) International Publication Number
WO 2008/115213 A2

(51) International Patent Classification:
H01L 33/00 (2006.01)

(21) International Application Number:
PCT/US2007/024367

(22) International Filing Date:
20 November 2007 (20.11.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/656,759 22 January 2007 (22.01.2007) US

(71) Applicant (for all designated States except US): **CREE, INC.** [US/US]; 4600 Silicon Drive, Durham, NC 27703 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **CHITNIS, Ashay** [IN/US]; 7220 Davenport, Apartment 101, Goleta, CA 93117 (US). **IBBETSON, James** [GB/US]; 910 Randolph Road, Santa Barbara, CA 93111 (US). **CHAKRABORTY, Arpan** [IN/US]; 777 Madrona Walk #a, Goleta, CA 93117 (US). **TARSA, Eric, J.** [US/US]; 105 Dearborn Place #41, Goleta, CA 93117 (US). **KELLER, Bernd** [DE/US]; 1355 San Antonio Creek Road, Santa Barbara, CA 93111 (US). **SERUTO, James** [US/US]; 7056 Madera Drive, Goleta,

CA 93117 (US). **FU, Yankun** [CN/US]; 7822 Spungold Street, Raleigh, NC 27617 (US).

(74) Agents: **PHILPOTT, Brian, J.** et al.; Koppel, Patrick, Heybl & Dawson, 555 St. Charles Drive, Suite 107, Thousand Oaks, CA 91360 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: WAFER LEVEL PHOSPHOR COATING METHOD AND DEVICES FABRICATED UTILIZING METHOD

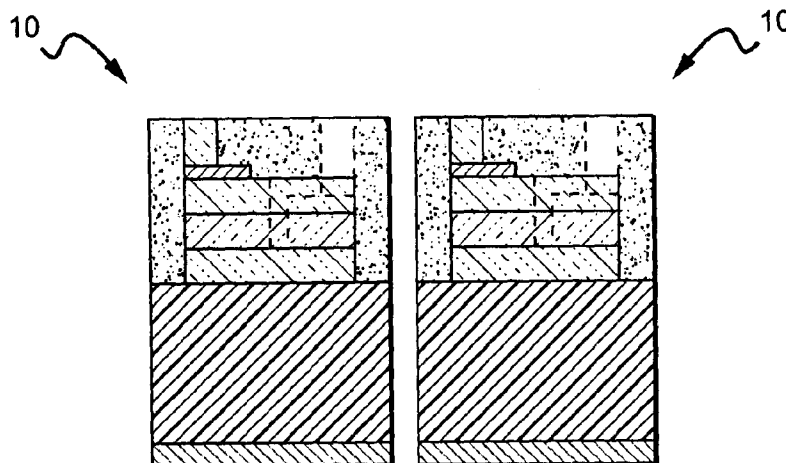


FIG. 1e

(57) Abstract: Methods for fabricating light emitting diode (LED) chips comprising providing a plurality of LEDs typically on a substrate. Pedestals are deposited on the LEDs with each of the pedestals in electrical contact with one of the LEDs. A coating is formed over the LEDs with the coating burying at least some of the pedestals. The coating is then planarized to expose at least some of the buried pedestals while leaving at least some of said coating on said LEDs. The exposed pedestals can then be contacted such as by wire bonds. The present invention discloses similar methods used for fabricating LED chips having LEDs that are flip-chip bonded on a carrier substrate and for fabricating other semiconductor devices. LED chip wafers and LED chips are also disclosed that are fabricated using the disclosed methods.

WO 2008/115213 A2



Published:

- *without international search report and to be republished
upon receipt of that report*

**WAFER LEVEL PHOSPHOR COATING METHOD AND DEVICES
FABRICATED UTILIZING METHOD**

This invention was made with Government support under Contract USAF 05-2-5507. The Government has certain rights in this invention

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates to methods for fabricating semiconductor devices and in particular methods for wafer level coating of light emitting diodes.

Description of the Related Art

[0002] Light emitting diodes (LED or LEDs) are solid state devices that convert electric energy to light, and generally comprise one or more active layers of semiconductor material sandwiched between oppositely doped layers. When a bias is applied across the doped layers, holes and electrons are injected into the active layer where they recombine to generate light. Light is emitted from the active layer and from all surfaces of the LED.

[0003] Conventional LEDs cannot generate white light from their active layers. Light from a blue emitting LED has been converted to white light by surrounding the LED with a yellow phosphor, polymer or dye, with a typical

phosphor being cerium-doped yttrium aluminum garnet (Ce:YAG). [See Nichia Corp. white LED, Part No. NSPW300BS, NSPW312BS, etc.; See also U.S. Patent No. 5959316 to Lowrey, "Multiple Encapsulation of Phosphor-LED Devices"]. The surrounding phosphor material "downconverts" the wavelength of some of the LED's blue light, changing its color to yellow. Some of the blue light passes through the phosphor without being changed while a substantial portion of the light is downconverted to yellow. The LED emits both blue and yellow light, which combine to provide a white light. In another approach light from a violet or ultraviolet emitting LED has been converted to white light by surrounding the LED with multicolor phosphors or dyes.

[0004] One conventional method for coating an LED with a phosphor layer utilizes a syringe or nozzle for injecting a phosphor mixed with epoxy resin or silicone polymers over the LED. Using this method, however, it can be difficult to control the phosphor layer's geometry and thickness. As a result, light emitting from the LED at different angles can pass through different amounts of conversion material, which can result in an LED with non-uniform color temperature as a function of viewing angle. Because the geometry and thickness is hard to control, it can also be difficult to consistently reproduce LEDs with the same or similar emission characteristics.

[0005] Another conventional method for coating an LED is by stencil printing, which is described in European Patent Application EP 1198016 A2 to Lowery. Multiple light emitting semiconductor devices are arranged on a substrate with a desired distance between adjacent LEDs. The stencil is provided having openings that align with the LEDs, with the holes being slightly larger than the

LEDs and the stencil being thicker than the LEDs. A stencil is positioned on the substrate with each of the LEDs located within a respective opening in the stencil. A composition is then deposited in the stencil openings, covering the LEDs, with a typical composition being a phosphor in a silicone polymer that can be cured by heat or light. After the holes are filled, the stencil is removed from the substrate and the stenciling composition is cured to a solid state.

[0006] Like the syringe method above, using the stencil method can be difficult to control the geometry and layer thickness of the phosphor containing polymer. The stenciling composition may not fully fill the stencil opening such that the resulting layer is not uniform. The phosphor containing composition can also stick to the stencil opening which reduces the amount of composition remaining on the LED. The stencil openings may also be misaligned to the LED. These problems can result in LEDs having non-uniform color temperature and LEDs that are difficult to consistently reproduce with the same or similar emission characteristics.

[0007] Various coating processes of LEDs have been considered, including spin coating, spray coating, electrostatic deposition (ESD), and electrophoretic deposition (EPD). Processes such as spin coating or spray coating typically utilize a binder material during the phosphor deposition, while other processes require the addition of a binder immediately following their deposition to stabilize the phosphor particles/powder.

[0008] With these approaches the key challenge is accessing the wire bond pad on the device after the coating process. Accessing the wire bond by standard

wafer fabrication techniques is difficult with typical silicone binding material, as well as other binder materials such as epoxies or glass. Silicones are not compatible with commonly used wafer fabrication materials such as acetone, as well as some developers, and resist strippers. This can limit the options and choices for the particular silicones and process steps. Silicones are also cured at high temperature (greater than 150° C), which is beyond the glass transition temperature of commonly used photoresists. Cured silicone films with phosphor are also difficult to etch and have a very slow etch rate in chlorine and CF₄ plasma, and wet etching of cured silicones is typically inefficient.

SUMMARY OF THE INVENTION

[0009] The present invention discloses new methods for fabricating semiconductor devices such as LED chips at the wafer level, and discloses LED chips and LED chip wafers fabricated using the methods. One method for fabricating light emitting diode (LED) chips according to the present invention comprises providing a plurality of LEDs typically on a substrate. Pedestals are formed on the LEDs with each of the pedestals in electrical contact with one of the LEDs. A coating is formed over said LEDs, with the coating burying at least some of the pedestals. The coating is then planarized leaving some of said coating material on said LEDs while exposing at least some of the buried pedestals, making them available for contacting. The present invention discloses similar methods used for fabricating LED chips comprising LEDs flip chip mounted on a carrier substrate. Similar methods according to the present invention can also be used for fabricating other semiconductor devices.

[0010] One embodiment of a light emitting diode (LED) chip wafer fabricated using methods according to the present invention comprises a plurality of LEDs on a substrate wafer and a plurality of pedestals, each of which is in electrical contact with one of the LEDs. A coating at least partially covers the LEDs with at least some of the pedestals extending through and to the surface of the coating. The pedestals are exposed at the surface of the coating.

[0011] One embodiment of a light emitting diode (LED) chip manufactured using methods according to the present invention comprises an LED on a substrate and a pedestal in electrical contact with the LED. A coating at least partially covering the LED, with the pedestal extending through and to the surface of the coating and exposed at the surface of the coating.

[0012] In accordance with certain aspects of the present invention, the coating can include phosphor particles that downconvert at least some of the light emitted from the active region of the LED chip to produce white light, thereby producing a white LED chip.

[0013] These and other aspects and advantages of the invention will become apparent from the following detailed description and the accompanying drawings which illustrate by way of example the features of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIGs. 1a through 1e are sectional views of one embodiment of an LED chip wafer at fabrication steps in one method according to the present invention;

[0015] FIG. 2 is a sectional view of another embodiment of an LED chip wafer according to the present invention having a reflective layer;

[0016] FIGs. 3 through 3e are sectional views of one embodiment of an flip-wafer bonded LED chip wafer at fabrication steps in another method according to the present invention;

[0017] FIG. 4 is a sectional view of another embodiment of an LED chip wafer according to the present invention having a reflective layer;

[0018] FIGs. 5a through 5d are sectional views of another embodiment of an LED chip wafer at fabrication steps in a method according to the present invention utilizing a prefabricated coating;

[0019] FIGs. 6a through 6c are sectional views of another embodiment of an LED chip wafer at fabrication steps in a method according to the present invention having recesses in the coating;

[0020] FIG. 7 is a sectional view of another embodiment of an LED chip wafer according to the present invention;

[0021] FIG. 8 is also a sectional view of another embodiment of an LED chip wafer according to the present invention;

[0022] FIG. 9 is a sectional view of one embodiment of an LED array according to the present invention;

[0023] FIG. 10 is a sectional view of another embodiment of an LED array according to the present invention;

[0024] FIG. 11 is a sectional view of an embodiment of an LED chip wafer according to the present invention having a transparent substrate;

[0025] FIG. 12 is a sectional view of another embodiment of an LED chip wafer according to the present invention having a transparent substrate;

[0026] FIG. 13 is a sectional view of another embodiment of an flip-chip LED chip wafer according to the present invention;

[0027] FIG. 14 is a sectional view of another embodiment of an LED chip having a phosphor loading carrier substrate;

[0028] FIGS. 15a through 15d are sectional views of another embodiment of an LED chip wafer at fabrication steps in a method according to the present invention utilizing a trenched substrate.

DETAILED DESCRIPTION OF THE INVENTION

[0029] The present invention provides fabrication methods that are particularly applicable to wafer level coating of semiconductor devices such as LEDs. The present invention also provides semiconductor devices, such as LEDs fabricated using these methods. The present invention allows coating of LEDs at the wafer level with a down-converter layer (e.g. phosphor loaded silicone) while still allowing access to one or more of the contacts for wire bonding. According to one aspect of the present invention, electrically conducting pedestals/posts are formed on one or both of the LED contacts (bond pads) while the LEDs are at the wafer level. These pedestals can be fabricated using known techniques such as electroplating, electroless plating,

stud bumping, or vacuum deposition. The wafer can then be blanket coated with a down-converter coating layer, burying the LEDs, contacts and pedestals. Each of the pedestals act as a vertical extension of its contact, and although the blanket coating with the down-converter coating temporarily covers the pedestals, the coating can be planarized and thinned to expose the top surface or top portion of the pedestals. The pedestals should be tall enough (10-100 μm) to project through the desired final coating thickness. After planarizing the pedestals are exposed for external connection such as by wire bonding. This process occurs at the wafer level and as a subsequent fabrication step, the individual LEDs chips can be separated/singulated from the wafer using known processes.

[0030] The present invention eliminates complex wafer fabrication processes to access wire bond pads after blanket coating. Instead a simple and cost effective approach is utilized. It allows for wafer level coating of semiconductor devices without the need for alignment. A wide variety of coating technologies can be used such as spin-coating of phosphor loaded silicone mixture, or electrophoretic deposition of phosphor followed by blanket coating of silicone or other binding material. Mechanical planarization allows thickness uniformity over the wafer and thickness uniformity of the coat can be achieved over a wide thickness range (e.g. 1 to 100 μm). White LED chip color point may be fine tuned by controlling the final coat thickness, including using an iterative approach (e.g. grind, test, grind, etc.) which will result in tightly binned white LEDs. This approach is also scalable to large wafer sizes.

[0031] The present invention is described herein with reference to certain embodiments but it is understood that the invention can be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. In particular, the present invention is described below in regards to coating LEDs with a down-converter coating that typically comprises a phosphor loaded binder ("phosphor/binder coating"), but it is understood that the present invention can be used to coat LEDs with other materials for down-conversion, protection, light extraction or scattering. It is also understood that the phosphor binder can have scattering or light extraction particles or materials, and that the coating can be electrically active. The methods according to the present invention can also be used for coating other semiconductor devices with different materials. Additionally, single or multiple coatings and/or layers can be formed on the LEDs. A coating can include no phosphors, one or more phosphors, scattering particles and/or other materials. A coating may also comprise a material such as an organic dye that provides down-conversion. With multiple coatings and/or layers, each one can include different phosphors, different scattering particles, different optical properties, such as transparency, index of refraction, and/or different physical properties, as compared to other layers and/or coatings.

[0032] It is also understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. Furthermore, relative terms such as "inner", "outer", "upper", "above", "lower", "beneath", and "below", and similar

terms, may be used herein to describe a relationship of one layer or another region. It is understood that these terms are intended to encompass different orientations of the device in addition to the orientation depicted in the figures.

[0033] Although the terms first, second, etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the present invention.

[0034] Embodiments of the invention are described herein with reference to cross-sectional view illustrations that are schematic illustrations of idealized embodiments of the invention. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances are expected. Embodiments of the invention should not be construed as limited to the particular shapes of the regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. A region illustrated or described as square or rectangular will typically have rounded or curved features due to normal manufacturing tolerances. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region of a device and are not intended to limit the scope of the invention.

[0035] FIGs. 1a through 1e show one embodiment of wafer level LED chips 10 manufactured using a method according to the present invention. Referring now to FIG. 1a, the LEDs chips 10 are shown at a wafer level of their fabrication process. That is, the LEDs chips 10 have not been through all the steps necessary before being separated/singulated from wafer into individual LED chips. Phantom lines are included to show separation or dicing line between the LED chips 10 and following additional fabrication steps, and as shown in FIG. 1e the LEDs chips can be separated into individual devices. FIGs. 1a through 1e also show only two devices at the wafer level, but it is understood that many more LED chips can be formed from a single wafer. For example, when fabricating LED chips having a 1 millimeter (mm) square size, up to 4500 LED chips can be fabricated on a 3 inch wafer.

[0036] Each of the LED chips 10 comprises a semiconductor LED 12 that can have many different semiconductor layers arranged in different ways. The fabrication and operation of LEDs is generally known in the art and only briefly discussed herein. The layers of the LED 10 can be fabricated using known processes with a suitable process being fabrication using metal organic chemical vapor deposition (MOCVD). The layers of the LEDs 12 generally comprise an active layer/region 14 sandwiched between first and second oppositely doped epitaxial layers 16, 18, all of which are formed successively on a substrate 20. In this embodiment the LEDs 12 are shown as separate devices on the substrate 20. This separation can be achieved by having portions of the active region 14 and doped layers 16, 18 etched down to the substrate 20 to form the open areas between the

LEDs 12. In other embodiments and as described in more detail below, the active layer 14 and doped layers 16, 18 can remain continuous layers on the substrate 20 and can be separated into individual devices when the LED chips are singulated.

[0037] It is understood that additional layers and elements can also be included in the LED 12, including but not limited to buffer, nucleation, contact and current spreading layers as well as light extraction layers and elements. The active region 14 can comprise single quantum well (SQW), multiple quantum well (MQW), double heterostructure or super lattice structures. In one embodiment, the first epitaxial layer 16 is an n-type doped layer and the second epitaxial layer 18 is a p-type doped layer, although in other embodiments the first layer 16 can be p-type doped and the second layer 18 n-type doped. The first and second epitaxial layers 16, 18 are hereinafter referred to as n-type and p-type layers, respectively.

[0038] The region 14 and layers 16, 18 of the LEDs 12 may be fabricated from different material systems, with preferred material systems being Group-III nitride based material systems. Group-III nitrides refer to those semiconductor compounds formed between nitrogen and the elements in the Group III of the periodic table, usually aluminum (Al), gallium (Ga), and indium (In). The term also refers to ternary and quaternary compounds such as aluminum gallium nitride (AlGa_N) and aluminum indium gallium nitride (AlInGa_N). In a preferred embodiment, the n- and p-type layers 16, 18 are gallium nitride (Ga_N) and the active region 14 is InGa_N. In alternative embodiments the n- and p-type layers 16, 18 may be AlGa_N,

aluminum gallium arsenide (AlGaAs) or aluminum gallium indium arsenide phosphide (AlGaInAsP).

[0039] The substrate 20 can be made of many materials such as sapphire, silicon carbide, aluminum nitride (AlN), GaN, with a suitable substrate being a 4H polytype of silicon carbide, although other silicon carbide polytypes can also be used including 3C, 6H and 15R polytypes. Silicon carbide has certain advantages, such as a closer crystal lattice match to Group III nitrides than sapphire and results in Group III nitride films of higher quality. Silicon carbide also has a very high thermal conductivity so that the total output power of Group-III nitride devices on silicon carbide is not limited by the thermal dissipation of the substrate (as may be the case with some devices formed on sapphire). SiC substrates are available from Cree Research, Inc., of Durham, North Carolina and methods for producing them are set forth in the scientific literature as well as in a U.S. Patents, Nos. Re. 34,861; 4,946,547; and 5,200,022. In the embodiment shown, the substrate 20 is at the wafer level, with the plurality of LEDs 12 formed on the wafer substrate 20.

[0040] Each of the LEDs 12 can have first and second contacts 22, 24. In the embodiment shown, the LEDs have a vertical geometry with the first contact 22 on the substrate 20 and the second contact 24 on the p-type layer 18. The first contact 22 is shown as one layer on the substrate, but when the LED chips are singulated from the wafer the first contact 22 will also be separated such that each LED chip 10 has its own portion of the first contact 22. An electrical signal applied to the first contact 22 spreads into the n-type layer 16 and a signal applied to the second contact 24 spreads into the

p-type layer 18. In the case of Group-III nitride devices, it is well known that a thin semitransparent current spreading layer typically covers some or all of the p-type layer 18. It is understood that the second contact 24 can include such a layer which is typically a metal such as platinum (Pt) or a transparent conductive oxide such as indium tin oxide (ITO). The first and second contacts 22, 24 are hereinafter referred to as the n-type and p-type contacts respectively.

[0041] The present invention can also be used with LEDs having lateral geometry wherein both contacts are on the top of the LEDs. A portion of the p-type layer 18 and active region is removed, such as by etching to expose a contact mesa on the n-type layer 16. The boundary of the removed portion of the of the active region 14 and p-type layer 18 is designated by vertical phantom line 25. A second lateral n-type contact 26 (also shown in phantom) is provided on the mesa of the n-type layer 16. The contacts can comprise known materials deposited using known deposition techniques.

[0042] Referring now to FIG. 1b, and according to the present invention, a p-type contact pedestal 28 is formed on the p-type contact 24 that is utilized to make electrical contact to the p-type contact 24 after coating of the LEDs 12. The pedestal 28 can be formed of many different electrically conductive materials and can be formed using many different known physical or chemical deposition processes such as electroplating, electroless plating, or stud bumping, with the preferred contact pedestal being gold (Au) and formed using stud bumping. This method is typically the easiest and most cost effective approach. The pedestal 28 can be made of other

conductive materials beyond Au, such as copper (Cu) or nickel (Ni) or Indium, or combinations thereof.

[0043] The process of forming stud bumps is generally known and only discussed briefly herein. Stud bumps are placed on the contacts (bond pads) through a modification of the "ball bonding" process used in conventional wire bonding. In ball bonding, the tip of the bond wire is melted to form a sphere. The wire bonding tool presses this sphere against the contact, applying mechanical force, heat, and/or ultrasonic energy to create a metallic connection. The wire bonding tool next extends the gold wire to the connection pad on the board, substrate, or lead frame, and makes a "stitch" bond to that pad, and finishes by breaking off the bond wire to begin another cycle. For stud bumping, the first ball bond is made as described, but the wire is then broken close above the ball. The resulting gold ball, or "stud bump" remains on the contact and provides a permanent, reliable connection through to the underlying contact metal. The stud bumps can then be flattened (or "coined") by mechanical pressure to provide a flatter top surface and more uniform bump heights, while at the same time pressing any remaining wire into the ball.

[0044] The height of the pedestal 28 can vary depending on the desired thickness of the phosphor loaded binder coating and should be high enough to match or extend above the top surface of the phosphor loaded binder coating from the LED. The height can exceed 200 μm , with typical pedestal height in the range of 20 to 60 μm . In some embodiments, more than one stud bump can be stacked to achieve the desired pedestal height. The stud bumps or other forms of the pedestal 28 can also have a reflecting

layer or can be made of a reflective material to minimize optical losses.

[0045] For the vertical geometry type LEDs 12 shown, only one pedestal 28 is needed for the p-type contact 24. For alternative lateral geometry LEDs a second n-type pedestal 30 (shown in phantom) is formed on the lateral geometry n-type contact 26, typically of the same materials, to substantially the same height as the p-type pedestal 28, and formed using the same processes.

[0046] Referring now to FIG. 1c, the wafer is blanketed by a phosphor/binder coating 32 that covers each of the LEDs 12, and its contact 22, and has a thickness such that it covers/buries the pedestal 28. For lateral geometry devices, the contact 26 and pedestal 30 are also buried. The present invention provides the advantage of depositing the phosphor coating over the LEDs 12 at the wafer level without the need for alignment over particular devices or features. Instead, the entire wafer is covered, which provides for a simpler and more cost effective fabrication process. The phosphor coating can be applied using different processes such as spin coating, electrophoretic deposition, electrostatic deposition, printing, jet printing or screen printing.

[0047] In a preferred embodiment, the phosphor can be deposited over the wafer in a phosphor/binder mixture using spin coating. Spin coating is generally known in the art and generally comprises depositing the desired amount of binder and phosphor mixture at the center of the substrate and spinning the substrate at high speed. The centrifugal acceleration causes the mixture to spread to and eventually off the edge of the substrate. Final layer thickness and other properties depend on the nature

of the mixture (viscosity, drying rate, percent phosphor, surface tension, etc.) and the parameters chosen for the spin process. For large wafers it may be useful to dispense the phosphor/binder mixture over the substrate before spinning the substrate at high speed.

[0048] In another embodiment, the phosphor is deposited on the wafer using known electrophoretic deposition methods. The wafer and its LEDs are exposed to a solution containing phosphor particles suspended in a liquid. An electrical signal is applied between the solution and the LEDs which creates an electrical field that causes the phosphor particles to migrate to and deposit on the LEDs. The process typically leaves the phosphor blanketed over the LEDs in powder form. A binder can then be deposited over the phosphor with the phosphor particles sinking into the binder to form the coating 32. The binder coating can be applied using many known methods and in one embodiment, the binder coating can be applied using spin coating.

[0049] The phosphor/binder coating 32 can then be cured using many different curing methods depending on different factors such as the type of binder used. Different curing methods include but are not limited to heat, ultraviolet (UV), infrared (IR) or air curing.

[0050] Different factors determine the amount of LED light that will be absorbed by the phosphor/binder coating in the final LED chips, including but not limited to the size of the phosphor particles, the percentage of phosphor loading, the type of binder material, the efficiency of the match between the type of phosphor and wavelength of emitted light, and the thickness of the phosphor/binding layer. These different factors can be

controlled to control the emission wavelength of the LED chips according to the present invention.

[0051] Different materials can be used for the binder, with materials preferably being robust after curing and substantially transparent in the visible wavelength spectrum. Suitable material include silicones, epoxies, glass, spin-on glass, BCB, polyimides and polymers, with the preferred material being silicone because of its high transparency and reliability in high power LEDs. Suitable phenyl- and methyl-based silicones are commercially available from Dow® Chemical. In other embodiments, the binder material can be engineered to be index matched with the features such as the chip (semiconductor material) and growth substrate, which can reduce total internal reflection (TIR) and improve light extraction.

[0052] Many different phosphors can be used in the coating 32 according to the present invention. The present invention is particularly adapted to LED chips emitting white light. In one embodiment according to the present invention LEDs 12 emit light in the blue wavelength spectrum and the phosphor absorbs some of the blue light and re-emits yellow. The LED chips 10 emit a white light combination of blue and yellow light. In one embodiment the phosphor comprises commercially available YAG:Ce, although a full range of broad yellow spectral emission is possible using conversion particles made of phosphors based on the $(\text{Gd}, \text{Y})_3(\text{Al}, \text{Ga})_5\text{O}_{12}:\text{Ce}$ system, such as the $\text{Y}_3\text{Al}_5\text{O}_{12}:\text{Ce}$ (YAG). Other yellow phosphors that can be used for white emitting LED chips include:

$\text{Tb}_{3-x}\text{RE}_x\text{O}_{12}:\text{Ce}$ (TAG); RE=Y, Gd, La, Lu; or

$\text{Sr}_{2-x-y}\text{Ba}_x\text{Ca}_y\text{SiO}_4:\text{Eu}$.

[0053] First and second phosphors can also be combined for higher CRI white of different white hue (warm white) with the yellow phosphors above combined with red phosphors. Different red phosphors can be used including:
 $\text{Sr}_x\text{Ca}_{1-x}\text{S}:\text{Eu}$, Y; Y=halide;
 $\text{CaSiAlN}_3:\text{Eu}$; or
 $\text{Sr}_{2-y}\text{Ca}_y\text{SiO}_4:\text{Eu}$

[0054] Other phosphors can be used to create saturated color emission by converting substantially all light to a particular color. For example, the following phosphors can be used to generate green saturated light:

$\text{SrGa}_2\text{S}_4:\text{Eu}$;
 $\text{Sr}_{2-y}\text{Ba}_y\text{SiO}_4:\text{Eu}$; or
 $\text{SrSi}_2\text{O}_2\text{N}_2:\text{Eu}$.

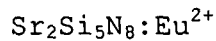
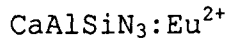
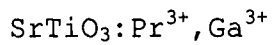
[0055] The following lists some additional suitable phosphors used as conversion particles in an LED chips 10, although others can be used. Each exhibits excitation in the blue and/or UV emission spectrum, provides a desirable peak emission, has efficient light conversion, and has acceptable Stokes shift:

YELLOW/GREEN

$(\text{Sr}, \text{Ca}, \text{Ba}) (\text{Al}, \text{Ga})_2\text{S}_4 : \text{Eu}^{2+}$
 $\text{Ba}_2(\text{Mg}, \text{Zn})\text{Si}_2\text{O}_7 : \text{Eu}^{2+}$
 $\text{Gd}_{0.46}\text{Sr}_{0.31}\text{Al}_{1.23}\text{O}_x\text{F}_{1.38} : \text{Eu}^{2+}_{0.06}$
 $(\text{Ba}_{1-x-y}\text{Sr}_x\text{Ca}_y)\text{SiO}_4 : \text{Eu}$
 $\text{Ba}_2\text{SiO}_4 : \text{Eu}^{2+}$

RED

$\text{Lu}_2\text{O}_3 : \text{Eu}^{3+}$
 $(\text{Sr}_{2-x}\text{La}_x) (\text{Ce}_{1-x}\text{Eu}_x) \text{O}_4$
 $\text{Sr}_2\text{Ce}_{1-x}\text{Eu}_x\text{O}_4$
 $\text{Sr}_{2-x}\text{Eu}_x\text{CeO}_4$



[0056] Different sized phosphor particles can be used including but not limited to 10-100 nanometer(nm)-sized particles to 20-30 μm sized particles, or larger. Smaller particle sizes typically scatter and mix colors better than larger sized particles to provide a more uniform light. Larger particles are typically more efficient at converting light compared to smaller particles, but emit a less uniform light. In one embodiment, the particle sizes are in the range of 2-5 μm . In other embodiments, the coating 32 can comprise different types of phosphors or can comprise multiple phosphor coatings for monochromatic or polychromatic light sources.

[0057] The coating 32 can also have different concentrations or loading of phosphor materials in the binder, with a typical concentration being in range of 30-70% by weight. In one embodiment, the phosphor concentration is approximately 65% by weight, and is preferably uniformly dispersed throughout the binder. Still in other embodiments the coating can comprise multiple layers of different concentrations of types of phosphors, or a first coat of clear silicone can be deposited followed by phosphor loaded layers.

[0058] As discussed above, the pedestal 28 (and pedestal 30 for lateral devices) are buried by the coating 32, which allows for the LED chips 10 to be coated without the need for alignment. After the initial coating of the LED chips, further processing is needed to expose the pedestal 28. Referring now the FIG. 1d, the coating 32 is thinned or planarized so that the pedestals 28 are

exposed through the coating's top surface. Many different thinning processes can be used including known mechanical processes such as grinding, lapping or polishing, preferably after the binder has cured. Other fabrication methods can comprise a squeegee to thin the coating before cured or pressure planarization can also be used before the coating is cured. Still in other embodiments the coating can be thinned using physical or chemical etching, or ablation. The thinning process not only exposes the pedestals, but also allows for planarizing of the coating and for control of the final thickness of the coating.

[0059] Following planarization, the surface root mean squared roughness of the coating should be approximately 10 nm or less, although the surface can have other surface roughness measurements. In some embodiments the surface can be textured during planarization. In other embodiments, after planarization the coating or other surfaces, can be textured such as by laser texturing, mechanical shaping, etching (chemical or plasma), or other processes, to enhance light extraction. Texturing results in surface features that are 0.1-5 μm tall or deep, and preferably 0.2-1 μm . In other embodiments, the surface of the LEDs 12 can also be textured or shaped for improved light extraction.

[0060] Referring now to FIG. 1e, the individual LED chips 10 can be singulated from the wafer using known methods such as dicing, scribe and breaking, or etching. The singulating process separates each of the LED chips 10 with each having substantially the same thickness of coating 32, and as a result, substantially the same amount of phosphor and emission characteristics. This allows for reliable and consistent fabrication of LED

chips 10 having similar emission characteristics. Following singulating the LED chips can be mounted in a package, or to a submount or printed circuit board (PCB) without the need for further processing to add phosphor. In one embodiment the package/submount/PCB can have conventional package leads with the pedestals electrically connected to the leads. A conventional encapsulation can then surround the LED chip and electrical connections. In another embodiment, the LED chip can be enclosed by a hermetically sealed cover with an inert atmosphere surrounding the LED chip at or below atmospheric pressure.

[0061] For the LED chips 10, light from the LED 12 that is emitted toward substrate 20 can pass out of the LED chip 10 through the substrate without passing through the phosphor/binder coating 32. This can be acceptable for generating certain colors or hues of light. In embodiments where this substrate emission is to be prevented or minimized, the substrate 20 can be opaque so that light from the LED 12 emitted toward the substrate 20 is blocked or absorbed so that most light emitting from the LED chip 10 comes from light passing through the coating 32.

[0062] FIG. 2 shows another embodiment of a LED chips 40 that are similar to the LED chips 10 described above and shown in FIGs. 1a through 1e, but having additional features to encourage emission of LED chip light toward the top of the LED chips 40 and minimize light passing into the substrate 20. For similar features as those in LED chips 10, the same reference numbers will be used herein. Each of the LED chips 40 comprises LEDs 12 formed on a substrate 20 and having n-type layer 16, active region 14 and p-type layer 18 formed successively on the

substrate 20. LED chips 40 further comprise n-type contact 22, p-type contact 24, p-type pedestal 28 and coating 32. The coating 32 is planarized to expose the pedestal 28. The LED chips 40 can alternatively have lateral geometry with the additional pedestal 30

[0063] LED chips 40 also comprise a reflective layer 42 that is arranged to reflect light emitted from the active region toward the substrate 20, back toward the top of the LED chips 40. This reflective layer 42 reduces the emission of light from the LEDs 12 that does not pass through conversion material before emitting from the LED chips 40, such as through the substrate 20 and encourages emission toward the top of the LED chips 40 and through the coating 32.

[0064] The reflective layer 42 can be arranged in different ways and in different locations in the LED chip 40, with the layer 42 as shown arranged between the n-type layer 16 and the substrate 20. The layer can also extend on the substrate 20 beyond the vertical edge of the LED chips 12. In other embodiments the reflective layer is only between the n-type layer 16 and the substrate. The layer 42 can comprise different materials including but not limited to a metal or a semiconductor reflector such as a distributed Bragg reflector (DBR).

[0065] As mentioned above, in some embodiments the active region 14 and the n- and p-type layers 16, 18 can be continuous layers on the substrate 20 as shown by phantom lines between the LEDs 12. In these embodiments, the LEDs are not separated until the step when the LED chips 40 are singulated. Accordingly, the resulting LED chips may have a layer of the coating 32 over the top surface of the LEDs. This can allow for emission of the active

region light out the side surfaces of the LEDs 12, but in embodiments utilizing this LEDs in relation to the surrounding features, this emission of light without encountering phosphor material can be minimal compared to the amount of light passing through the phosphor material.

[0066] The methods according to the present invention can be used to coat many different devices and LEDs. FIGs. 3a through 3e show a different LED chip 60 having a structure different from the LED chip 10 described above and shown in FIGs. 1a through 1e. Referring first to FIG. 3a, the LED chip 60 is also at wafer level and shown prior to singulating. It comprises LEDs 62 that are not on a growth substrate, but are instead flip-wafer bonded to a carrier substrate 64. In this embodiment, the growth substrate can comprise the materials described above for growth substrate 20 in FIGs. 1a through 1e, but in this embodiment the growth substrate is removed after (or before) flip-wafer bonding, with the substrate removed using known grinding and/or etching processes. The LEDs 62 are mounted to the carrier substrate 64 by layer 66, which is typically one or more bond/metal layers, and which also serve to reflect light incident on it. In other embodiments, the growth substrate or at least portions thereof remain. The growth substrate or the remaining portions can be shaped or textured to enhance light extraction from the LEDs 62.

[0067] Many different material systems can be used for the LEDs, with a preferred material system being the Group-III nitride material system grown using known processes as described above. Like the LEDs 12 in FIGs. 1-5, each of the LEDs 62 generally comprises an active region 68 sandwiched between n-type and p-type epitaxial

layers 70, 72 although other layers can also be included. Because LEDs 62 are flip-wafer bonded, the top layer is the n-type layer 70, while the p-type layer 72 is the bottom layer arranged between the active region 68 and the bond/metal layer 66. The carrier substrate can be many different known materials, with a suitable material being silicon.

[0068] For vertical geometry LED chips 60, an n-type contact 74 can be included on top surface of each of the LEDs, and a p-type contact 76 can be formed on the carrier substrate 64. The n- and p-type contacts 74, 76 can also be made of conventional conductive materials deposited using known techniques similar to the first and second contacts 22, 24 shown in FIGs 1a through 1e and described above. As also described above, the LEDs can have a lateral geometry with the n- and p-type contacts on the top of the LEDs.

[0069] Referring now to FIG. 3b, each of the LED chips 60 can have a pedestal 78 formed on its first contact 70, with each pedestal being formed of the same material and using the same methods as those described above for pedestal 28 in FIGs. 1b through 1e. As shown in FIG. 3c the LED chip wafer can then be covered by a blanket coating 80 preferably comprising a phosphor loaded binder. The same phosphors and binder can be used as those for the coating 32 described above and shown in FIGs. 1c through 1e, and can be deposited using the same methods. The coating 80 covers and buries the LEDs 62, their first contacts 74 and the pedestals 78, with the coating 80 being deposited without alignment steps.

[0070] Referring now to FIG. 3d, the coating 80 can be planarized or thinned to expose the pedestals 78 and to

control thickness of the coating 80 using the methods described above. Referring now to FIG. 3e, the individual LED chips 60 can be singulated from the wafer using the methods described above. These devices can then be packaged or mounted to a submount or PCB. In other embodiments the carrier substrate can be removed, leaving a coated LED that can then be packaged or mounted to a submount or PCB.

[0071] The flip-wafer bonded LEDs can also have reflective elements or layers to encourage light emission in the desired direction. FIG. 4 shows LED chips 90 at the wafer level that are similar to the LED chips 60 shown in FIGs. 3a through 3e and described above. For similar features the same reference numbers are used herein, and although LED chips 90 are shown having vertical geometry LEDs 62, it is understood that lateral geometry LEDs can also be used. The LED chips 90 comprise LEDs 62 mounted to a substrate 64 that can either be a carrier or growth substrate. Each of the LEDs 62 comprises an active layer 68, n-type layer 70, p-type layer 72, p-type contact 76, n-type contact 74, and pedestal 78 as described above, and a phosphor loaded binder coating 80 is formed over the LEDs also as described above. In this embodiment, however, a reflective layer 92 is included between the LEDs 62 and the substrate 64 that can comprise a highly reflective metal or reflective semiconductor structures such as a DBR. The reflective layer 92 reflects LED light that is emitted toward the substrate 64 and helps prevent light from passing into the substrate where at least some of the light can be absorbed by the substrate 64. This also encourages light emission from the LED chips 90 toward the top of the LED chips 90. It is understood that a

bond/metal layer (not shown) can also be included below the reflective layer or in other locations, particularly in the embodiments where the substrate 64 is a carrier substrate. The LED chips 90 can also comprise a p-contact layer adjacent to the p-type layer 72 to encourage ohmic contact to the layers below.

[0072] FIGs. 5a through 5d show another embodiment of LED chips 100 fabricated according to the present invention that are similar to the LED chips 60 described above and shown in FIGs. 3a through 3e. It is understood, however, that this method can also be used with non flip-wafer bonded embodiments such as the embodiment described above and shown in FIGs. 1a through 1e. Referring first to FIG. 5a, the LED chips 100 comprise vertical LEDs 62 mounted to a substrate 64 that in this case is a carrier substrate. It is understood that lateral LEDs can also be used as described above. Each of the LEDs 62 comprises active layer 68, n-type layer 70, p-type layer 72, p-type contact 76, n-type contact 74, and pedestal 78 as described above. For LED chips 100, however, are covered by a prefabricated coating layer 102 that can have the phosphor (and other) materials described above fixed in a binder also made of the materials described above.

[0073] Referring now to FIG. 5b, the layer 102 is placed over and covering the LEDs 62 and their pedestals 78 to provide a conformal coating. In one embodiment a bonding material can be included between the layer 102 and the LED chips 100 for adhesion, with typical adhesives being used such as silicones or epoxies. To further encourage conformal coating, the layer 102 can be heated or a vacuum can be applied to pull the layer 102 down over the LED chips 100. The layer 102 can also be provided in a state where the binder is not fully cured so that the

layer 102 more readily conforms to the LED chips. Following conformal placement of the layer 102, the binder can be exposed to its final curing.

[0074] Referring now to FIG. 5c, the layer 102 can be planarized using the methods described above to expose the pedestals 78, making them available for contacting. As shown in FIG. 5d, the LED chips 100 can then be singulated using the methods described above.

[0075] The fabrication method for LED chips 100 allows for the thickness of the phosphor/binder to be accurately controlled by controlling the thickness of the layer 102. This method also allows for the use of different layer thicknesses and composition for different desired emission characteristics for the LED chips 100.

[0076] FIGs. 6a through 6c show still another embodiment of LED chips 110 according to the present invention similar to LED chips 60. Referring first to FIG. 6a, each of the LED chips 110 has vertical LEDs 62 mounted to a substrate 64 that can either be a carrier or growth substrate. Each of the LEDs 62 comprises active layer 68, n-type layer 70, p-type layer 72, p-type contact 76, n-type contact 74, and pedestal 78 as described above. A coating 112 made of the materials described above is included over the LEDs 62, burying the pedestals 78.

[0077] Referring to FIG. 6b, in this embodiment the coating 112 is not planarized to expose the pedestals 78. Instead, the coating remains at a level higher than the pedestals and a portion of the coating 112 burying the pedestal 78 is removed leaving recessed portions 114 in the coating 112. The pedestals 78 are exposed through the recessed portions 114 for contacting. Many different methods can be used to remove the coating such as

conventional patterning or etching processes. Referring now to FIG. 6c, the LED chips 110 can then be singulated using the methods described above.

[0078] This method of forming recessed portions 114 can be used in conjunction with planarizing of the coating 112. The layer 112 can be planarized to the level that provides the desired emission characteristics of the LED chip 110, which may be above the pedestals 78. The recessed portions 114 can then be formed to access the pedestals. This allows for forming pedestals of reduced height lower than the coating, which can reduce fabrication costs related to forming the pedestals 78. This process can require some alignment with forming the recessed portions, but the coating 112 is still applied without the need for alignment.

[0079] The pedestals in the LED chips embodiments above are described as comprising a conductive material such as Au, Cu, Ni or In, preferably formed using stud bumping processes. Alternatively, the pedestals can be made of different materials and can be formed using different methods. FIG 7 shows another embodiment of LED chips 120 comprising LEDs 122 flip-wafer bonded on a carrier substrate 124. In this embodiment, the pedestal 136 comprises a semiconductor material 138 formed generally in the shape of a pedestal 136. The semiconductor material 138 can be on the first contact, or as shown can be on the first epitaxial layer 130. A pedestal layer 140 of conductive material is included on the top surface of the semiconductor material 138 and extending to the top surface of the first epitaxial layer 130 and forming an n-type contact.

[0080] The semiconductor material 138 can be formed in many different ways and can comprise many different materials, such as the material comprising the LED epitaxial layers or the growth substrate material, e.g. GaN, SiC, sapphire, Si, etc. In one embodiment, the semiconductor material 138 can be etched from the epitaxial layers, and then coated with the pedestal layer 140. In other embodiments, portions of the growth substrate can remain on the epitaxial layers during removal of the growth substrate from the LEDs 122. The remaining growth substrate portions can then be covered by the pedestal layer 140.

[0081] FIG. 8 shows another embodiment of LED chips 150 still in wafer form that are similar to the LED chips 120 in FIG. 7, and the same reference numbers are used for similar features herein. The LED chips 150 comprise LEDs 122 flip-wafer bonded on a carrier substrate 124 by bond/metal layer 126. A pedestal 154 is formed on each of the LEDs 122, preferably on the n-type contact 155. The pedestal 154 comprises a patternable material 156 in substantially the shape of the pedestal 154 that is covered with a pedestal layer 158 of conductive material that extends to the first contact 152. The patternable material 156 can comprise different materials compatible with LED fabrication and operation such as BCB, polyimides and dielectrics. These materials can be formed on the LEDs 112 using known processes. Alternatively, pedestal 154 can be formed using patternable and electrically conducting materials such as silver epoxy or printable inks, in which case layer 158 may not be required. Other methods and approaches for fabricating pedestals can be used, some of which are described in John Lau, "Flip-Chip Technologies", McGraw Hill, 1996.

[0082] Like the embodiments above, the wafer comprising the LED chips 120 and 150 can be blanketed by a layer of coating material, burying the LED chips and their pedestals. The coating material can comprise the phosphors and binders described above, and can be thinned using the methods described above to expose the pedestals through the coating materials. The LED chips can then be singulated using the methods described above.

[0083] The present invention can also be used to fabricate wafer level emitter arrays. FIG. 9 shows one embodiment of wafer level LED array 170 that comprises LEDs 172 flip-wafer bonded on a carrier substrate 174 by a bond/metal layer 176. The LEDs comprise an active region 178 between first and second epitaxial layers 180, 182 with a first contact 184 on the first epitaxial layer 180. A pedestal 186 is included on the first contact 184 and a coating 188 of phosphor loaded binder coating blankets the LEDs 172, contacts 184 and pedestals 186, with the coating being thinned to expose the top of the pedestals 186. For the LED array 170 however, the individual LED chips are not singulated. Instead, an interconnecting metal pad 190 is included on the surface of the LED 172, interconnecting the exposed tops of the pedestals 186 in a parallel fashion. An electrical signal applied to the metal pad 190 conducts to the LEDs having their pedestals 186 coupled to the metal pad 190, illuminating the LEDs in an array. It is understood that the LED array can comprise many different numbers of LEDs arranged in different ways, such as in a row or block, depending on the LEDs that are interconnected by the metal pad 190.

[0084] FIG. 10 shows another embodiment of an LED array 200 according to the present invention also having LEDs

202 flip-wafer bonded to a carrier substrate 204, with each of the LEDs 202 comprising an active region 208 between first and second epitaxial layers 210, 212. A first contact 214 is on the first epitaxial layer 210 with a pedestal 216 formed on the first contact 214. A phosphor loaded binder coating 218 is included over the LEDs 202, first contacts 214 and pedestals 216, with the top surface of the pedestals 216 exposed. The LEDs 202 are mounted to the carrier substrate 204 by an electrically insulating bond layer 220 and a p-contact 222 is between each of the LEDs 202 and the insulating bond layer 220. Conductive vias 224 run between the p-contact and the surface of the coating 218 between the LEDs 202, and respective metal pads 226 run on the surface of the coating 218 between each of the vias 224 and a respective adjacent pedestal 216. This arrangement provides for a conductive path between the LEDs 202 such that the LEDs 202 are connected in series array, with the conductive path between the LEDs isolated from the substrate by the insulating bond layer 220. An electrical signal applied to the metal pads runs through each of the LEDs causing them to emit light in an array. It is understood that the LED array 200 can comprise many different numbers of LEDs arranged in different ways, such as in a row or block, depending on the LEDs that are interconnected by the metal pads 226.

[0085] Many different LED chips having different structures can be fabricated according to the present invention. FIG. 11 shows another embodiment of LED chips 350 according to the present invention arranged similarly to the LED chips 10 shown in FIGS. 1a through 1e and described above, and for similar features the same reference numbers are used herein. The LED chips 350 have

vertical geometry and comprise LEDs 12 each of which comprise an active region 14 between n-type and p-type epitaxial layers 16, 18. A pedestal 28 is formed on the p-type contact 24 with a phosphor loaded binder coating 32 covering the LEDs 12. In this embodiment however, the LEDs 12 are on a transparent substrate 352, which allows for a reflective layer 354 to be formed on the substrate 352 opposite the LEDs 12. Light from the LEDs 12 can pass through the substrate 352 and reflect back from the reflective layer 354 while experiencing minimal losses. The reflective layer 354 is shown between the contact 22 and the substrate 352, but it is understood that the reflective layer 354 can be arranged differently, such as being the bottommost layer with the contact 22 between the reflective layer 354 and the substrate 352.

[0086] FIG. 12 also shows another embodiment of LED chips 370 according to the present invention also arranged similar to the LED chips in FIGs. 1a through 1e. The LED chips 370 in this embodiment have lateral geometry and comprise LEDs 12 each of which comprise an active region 14 between n-type and p-type epitaxial layers 16, 18. A portion of the p-type layer 18 and the active region 14 is etched to reveal the n-type layer 16, with p-type contact 24 on the p-type layer 18 and the n-type contact 26 on the n-type layer 16. A p-type pedestal 28 is on the p-type contact 24 and n-type pedestal 30 is on the n-type contact 26. A phosphor loaded binder coating 32 covers the LEDs 12 with the pedestals 28, 30 exposed through the coating 32. The LEDs 12 are on a transparent substrate 372 and a reflective layer 374 included on the substrate 372 opposite the LEDs 12. The LEDs 12 have a lateral geometry with an p-type contact 24 and p-type pedestal 28 on the top of each of the LEDs 12. The reflective layer

374 also reflects light from the LEDs with the light experiencing minimal loss through the substrate 372.

[0087] Many different variations to the LED chips can be fabricated according to the present invention and FIG. 13 shows another embodiment of LED chips 400 having LEDs 402 having an active region 405 between n- and p-type layers 406, 408, on a growth substrate 404. It is understood that the LEDs 402 can also be provided with the growth substrate thinned or after the growth substrate has been removed. The LEDs also have n-type and p-type contacts 407, 409. The LEDs 402 are diced or singulated and flip-chip bonded to a submount/carrier wafer 410. Conductive traces 412 are formed on the submount/carrier wafer 410 with each of the LEDs 402 mounted on the traces 412, with the first trace 412a in electrical contact with the n-type layer 406 and the second trace 412b in contact with the p-type layer 408. Conventional traces can be used comprising aluminum (Al) or Au deposited using known techniques such as sputtering. The LED 402 is mounted to the traces 412 by flip-chip bonds 413 that can be arranged in conventional ways using known materials such as Au, or gold/tin solder bumps or stud bumps.

[0088] It is further understood that the pedestals in FIG. 13, and in the embodiments discussed above and below, can also be made of an insulating material coated by a conductive layer. In one embodiment, the pedestals can comprise substrate material or submount/carrier wafer material. For the LED chips 400, the submount/carrier wafer can be fabricated with pedestals with each of the LEDs mounted between pedestals. A conductive layer can be formed over the pedestals in contact with the conductive traces or in contact with the LED using other arrangements. It is further understood that the pedestals

can have many different shapes and sizes, and in one embodiment can comprise a reflective cup with an LED mounted within the cup. The cup can be coated with a conductive layer in contact with the conductive traces or the LED using other arrangements. During planarization of the phosphor binder coating, the top of the cups can be exposed for contacting. In still other embodiments, the cup can have its own pedestals that can be exposed during planarization.

[0089] An n-type pedestal 414 is formed on the first trace 412a and a p-type pedestal 416 is formed on the second trace 412b, with both pedestals being formed using the methods described above. A phosphor/binder coating 418 is included over the LEDs 402, burying the pedestals 414, 416. The coating 418 can then be planarized to expose the pedestals 414, 416 for contacting, or in other embodiments the recesses can be formed in the coating to expose the pedestals 414, 416. The LED chips can then be singulated using the processes described above.

[0090] The fabrication method described in conjunction with LED chips 400 allows for the use of good quality singulated LEDs 402 with the desired emission characteristics to be selected for mounting to the wafer 404. The arrangement also allows for the mounting of LEDs 402 to the wafer with larger spaces between the LEDs 402 while not wasting valuable epitaxial material through etching of the material to form the spaces.

[0091] FIG. 14 shows still another embodiment of LED chips 500 according to the present invention having singulated lateral geometry LEDs 502 mounted to a carrier substrate. Each of the LEDs 502 comprises an active region 504 between n- and p-type layers 506, 508, all

formed successively on a growth substrate 510. The substrate 510 can be many different materials, with the preferred substrate being a transparent material such as sapphire. The LEDs 502 are singulated with at least a portion of the growth substrate 510 remaining.

[0092] The LEDs 502 are then mounted to a carrier substrate 512 with the substrate down. The carrier substrate 512 comprises a first phosphor/binder coating 514 on a transparent substrate 516. The first coating 514 can be adhesive to hold the LEDs 502 or an additional adhesive materials can be used.

[0093] A p-type contact 518 is provided on the p-type layer 508 and an n-type contact 520 is provided on the n-type layer 506. The contacts 518, 520 can comprise many different materials, with the preferred material being reflective. By being reflective, the contacts 518, 520 reflect active region light making the carrier substrate 512 the primary emission surface. P-type pedestal 522 is formed on the p-type contact 518, and n-type pedestal 524 is formed on the n-type contact 520 as described above. A second phosphor/binder coating 526 is formed over the LEDs 502, burying the pedestals 522, 524. As described above, the second coating 526 can then be planarized to reveal the pedestals 522, 524.

[0094] The LED chips 500 can then be singulated and this arrangement provides LED chips 500 having LEDs 502 that are surrounded by a phosphor layer provided by the first and second coating 514, 526. The singulated LED chips 500 can also be packaged as a conventional flip-chip device except with the first and second coatings providing a white-emitting LED flip chip without further phosphor processing. This embodiment provides the further

advantage of ability to use good quality singulated LEDs 502 with the desired emission characteristics for mounting to the wafer carrier wafer 512, such that the resulting LED chips 502 are of good quality. The LEDs 502 can also be mounted to the wafer with larger spaces between the LEDs 502 while not wasting valuable epitaxial material through etching of the material to form the spaces.

[0095] FIGs. 15a through 15d show still another embodiment of LED chips 600 according to the present invention. Referring first to FIG. 15a, each of the LED chips comprises LEDs 602 each of which has an active region 604 between n- and p-type layers 606, 608, all formed successively on a growth substrate 610 that is preferably a transparent material such as sapphire. The LEDs 602 have a lateral geometry with a reflective n-type contact 612 on the n-type layer 606 and a reflective p-type contact 614 on the p-type layer 608. An n-type pedestal 616 is formed on the n-type contact 612, and a p-type pedestal 618 is formed on the p-type contact 614. A first phosphor/binder coating 620 is provided over the LEDs 602, initially burying the pedestals 616, 618, with coating then planarized to reveal the pedestal.

[0096] Referring now to FIG. 15b, trenches 622 are formed through the substrate 610 and partially into the coating 620, with the trenches arranged between the LEDs 602. The trenches 622 can be formed using many different methods such as by etching or cutting. Referring now to FIG. 15c, a second phosphor/binder coating 624 can be formed over the trench side of the substrate 610, filling the trenches 622. The second coating can then be planarized as desired. Referring to FIG. 15d, the LED chips 600 can be singulated with the LEDs 602 being surrounded by a

phosphor layer provided by the first and second coatings 620, 624. The LED chips 600 provide similar advantages as the LED chips 500 in FIG. 14, and provides good quality flip-chip devices that can provide white light emission without additional phosphor processing.

[0097] Referring again to FIGs. 15a and 15b, as an alternative to forming trenches 622, the growth substrate 610 can be removed entirely to expose the bottom surface of the n-type layer 606. The second phosphor/binder coating 624 can then be formed over the exposed n-type layer, and planarized as desired.

[0098] The present invention can also be used to cover individual LEDs instead of those on formed in an LED chip wafer. In these embodiments, the LED chips can be singulated and then mounted in a package or to a submount or PCB. The LED chips can then be coated and planarized according to the present invention to expose the pedestal(s) for contacting.

[0099] Although the present invention has been described in detail with reference to certain preferred configurations thereof, other versions are possible. Therefore, the spirit and scope of the invention should not be limited to the versions described above.

WE CLAIM:

1. A method for fabricating light emitting diode (LED) chips, comprising:

providing a plurality of LEDs;

depositing pedestals on said LEDs, each of said pedestals in electrical contact with one of said LEDs;

forming a coating over said LEDs, said coating burying at least some of said pedestals; and

planarizing said coating leaving at least some of said coating on said LEDs while exposing at least some of said buried pedestals.

2. The method of claim 1, wherein said LED chips emit white light.

3. The method of claim 1, further comprising depositing a contact on each said LEDs said pedestals formed on said contacts.

4. The method of claim 1, wherein said LEDs are provided on a growth substrate.

5. The method of claim 1, wherein said LEDs are mounted on a carrier substrate.

6. The method of claim 5, wherein said carrier substrate comprises a phosphor layer.

7. The method of claim 1, wherein said LEDs comprise at least a portion of a growth substrate.

8. The method of claim 7, wherein said substrate is shaped or textured.

9. The method of claim 1, wherein said step of forming a coating over said LEDs comprises providing a prefabricated coating layer and placing it over said LEDs.

10. The method of claim 1, wherein said LEDs are provided on a substrate, further comprising forming trenches in said substrate and forming a second coating filling said trenches.

11. The method of claim 1, further comprising curing said coating prior to planarizing.

12. The method of claim 1, further comprising curing said coating following planarizing.

13. The method of claim 1, further comprising forming a surface texture on said coating.

14. The method of claim 13, wherein said surface texture is formed during said planarizing.

15. The method of claim 13, wherein said surface texture is formed by laser texturing.

16. The method of claim 1, further comprising singulating said LEDs.

17. The method of claim 1, wherein said coating comprises a phosphor loaded binder.

18. The method of claim 17, wherein said phosphor loaded binder comprises multiple phosphors.

19. The method of claim 1, wherein said coating comprises scattering particles.

20. The method of claim 1, wherein said coating comprises multiple layers with different compositions.

21. The method of claim 17, wherein said binder comprises one of the materials from the group consisting of silicone, epoxy, glass, spin-on glass, BCB, polyimides and polymers.

22. The method of claim 17, wherein said phosphor comprises YAG:Ce.

23. The method of claim 17, wherein said phosphor comprises a material from the group consisting of $\text{Y}_3\text{Al}_5\text{O}_{12}:\text{Ce}$ (YAG), $\text{Tb}_{3-x}\text{RE}_x\text{O}_{12}:\text{Ce}$ (TAG); RE= Y, Gd, La, Lu, and $\text{Sr}_{2-x-y}\text{Ba}_x\text{Ca}_y\text{SiO}_4:\text{Eu}$.

24. The method of claim 1, wherein said planarizing comprises one of the methods from the group consisting of grinding, lapping and polishing.

25. The method of claim 1, wherein said planarizing comprises one or more methods from the group consisting of squeegee, pressure planarization, etching and ablation.

26. The method of claim 1, wherein said coating covers said LEDs by one of the methods from the group consisting of spin coating, electrophoretic deposition,

electrostatic deposition, printing, jet printing and screen printing.

27. The method of claim 1, wherein said pedestal is formed using stud bumping.

28. The method of claim 1, further comprising the step of forming a second coating around at least part of said LEDs.

29. The method of claim 28, wherein said second coating has a different composition than said coating.

30. The method of claim 28, further comprising the step of planarizing said second coating.

31. The method of claim 1, further comprising depositing a metal pad on said planarized coating interconnecting at least some of said pedestals to form an LED array.

32. The method of claim 16, further comprising sealing one of said singulated LEDs in a encapsulant.

33. The method of claim 16, further comprising mounting one of said LEDs to a submount or printed circuit board (PCB).

34. The method of claim 1, wherein said planarizing results in a uniform coating thickness.

35. The method of claim 1, wherein said coating has a total thickness variation of less than 50% of the average coating thickness.

36. A method for fabricating LED chips, comprising:
flip-chip bonding a plurality of LEDs on a carrier substrate;
forming a conductive pedestal in electrical contact with each of the LEDs;
forming a blanket coating over said LEDs, said coating burying at least some of said pedestals; and
planarizing said coating to expose at least some of said buried pedestals.

37. The method of claim 36, wherein said carrier substrate comprises electrical traces, said LEDs mounted in contact with said electrical traces.

38. The method of claim 37, wherein said pedestals are formed on said electrical traces.

39. The method of claim 36, wherein said LED chips emit white light.

40. A method for fabricating coated semiconductor devices, comprising:

providing a plurality of semiconductor devices on a substrate;

depositing pedestals on said semiconductor devices, each of which is in electrical contact with one of said semiconductor devices;

forming a blanket coating over said semiconductor devices, said coating burying at least some of said pedestals; and

planarizing said coating leaving at least some of said coating material on said semiconductor devices while exposing at least some of said buried pedestals for contacting.

41. A light emitting diode (LED) chip wafer, comprising:
a plurality of LEDs;
a plurality of pedestals, each of which is in electrical contact with one of said LEDs; and
a coating at least partially covering said LEDs, at least some of said pedestals extending through and to the surface of said coating and exposed at the surface of said coating.
42. The LED chip wafer of claim 41, wherein said LEDs are on a substrate wafer.
43. The LED chip wafer of claim 41, further comprising a plurality of contacts, each of which is on one of said LEDs, at least some of said pedestals formed on said contacts.
44. The LED chip wafer of claim 41, wherein said substrate wafer is capable of being separated into LED chips.
45. The LED chip wafer of claim 41, wherein said coating has a uniform thickness.
46. The LED chip wafer of claim 41, wherein said coating has a total thickness variation of <50% of the average coating thickness.
47. The LED chip wafer of claim 41, wherein said coating has a textured surface.
48. The LED chip wafer of claim 41, wherein said coating comprises multiple phosphors.

49. The LED chip wafer of claim 41, wherein said coating comprises scattering particles.

50. The LED chip wafer of claim 41, wherein said coating comprises a phosphor loaded binder.

51. The LED chip wafer of claim 50, wherein said binder comprises one of the materials from the group consisting of silicone, epoxy, glass, spin-on glass, BCB, polyimides and polymers.

52. The LED chip wafer of claim 50, wherein said phosphor comprises YAG:Ce.

53. The LED chip wafer of claim 41, wherein said pedestals comprise one or more stud bumps.

54. The LED chip wafer of claim 41, wherein said LEDs are made of materials from the Group-III nitride material system.

55. The LED chip wafer of claim 42, wherein said substrate wafer comprises a growth substrate.

56. The LED chip wafer of claim 42, wherein said substrate wafer comprises a carrier substrate.

57. The LED chip wafer of claim 41, wherein said LEDs are interconnected in an LED array.

58. The LED chip wafer of claim 41, a metal pad on the surface of said coating interconnecting at least some of said exposed pedestals to form an LED array.

59. The LED chip wafer of claim 41, further comprising a reflective layer formed integral to said substrate wafer.

60. The LED chip wafer of claim 42, wherein said substrate wafer comprises a phosphor loaded binder layer.

61. The LED chip wafer of claim 41, wherein said LEDs comprise at least a portion of a growth substrate.

62. The LED chip wafer of claim 41, wherein said LEDs are provided on a substrate, further comprising trenches in said substrate and a second coating filling said trenches.

63. The LED chip wafer of claim 41, wherein said coating comprises multiple layers with different compositions.

64. The LED chip wafer of claim 41, further comprising the step of forming a second coating around at least part of said LEDs.

65. The LED chip wafer of claim 64, wherein said second coating has a different composition than said coating.

66. The LED chip wafer of claim 41, capable of emitting white light from said LEDs and coating.

67. An light emitting diode (LED) chip, comprising:
an LED;
a pedestal in electrical contact with said LED; and
a coating at least partially covering said LED, said pedestal extending through and to the surface of said coating and exposed at the surface of said coating.

68. The LED chip of claim 67, wherein said LED emits white light.

69. The LED chip of claim 67, wherein said LED is on a substrate.

70. The LED chip of claim 67, further comprising a contact on said LED, said pedestals formed on said contact.

71. The LED chip of claim 67, wherein said coating comprises a phosphor loaded binder.

72. The LED chip of claim 67, wherein said pedestal comprises one or more stud bumps.

73. The LED chip of claim 67, wherein said LED comprises materials from the Group-III nitride material system.

74. The LED chip of claim 69, wherein said substrate comprises a growth substrate.

75. The LED chip of claim 67, wherein said substrate wafer comprises a carrier substrate.

76. The LED chip wafer of claim 67, further comprising a reflective layer formed integral to said substrate.

77. A light emitting diode (LED) package comprising:
 an LED chip;
 a pedestal in electrical contact with said LED chips; and

a coating at least partially covering said LED chip, said pedestal extending through and to the surface of said coating and exposed at the surface of said coating; package leads, said pedestal in electrical connection with one of said package leads; and encapsulation surrounding said LED chip and electrical connections.

78. A light emitting diode (LED) package comprising:
an LED chip;
a pedestal in electrical contact with said LED chips; and
a coating at least partially covering said LED chip, said pedestal extending through and to the surface of said coating and exposed at the surface of said coating; and
package leads, said pedestal in electrical connection with one of said package leads, wherein the chip is enclosed by a hermetically sealed cover.

79. The LED package of claim 78, wherein an inert atmosphere surrounds the LED chip at or below atmospheric pressure.

1/11

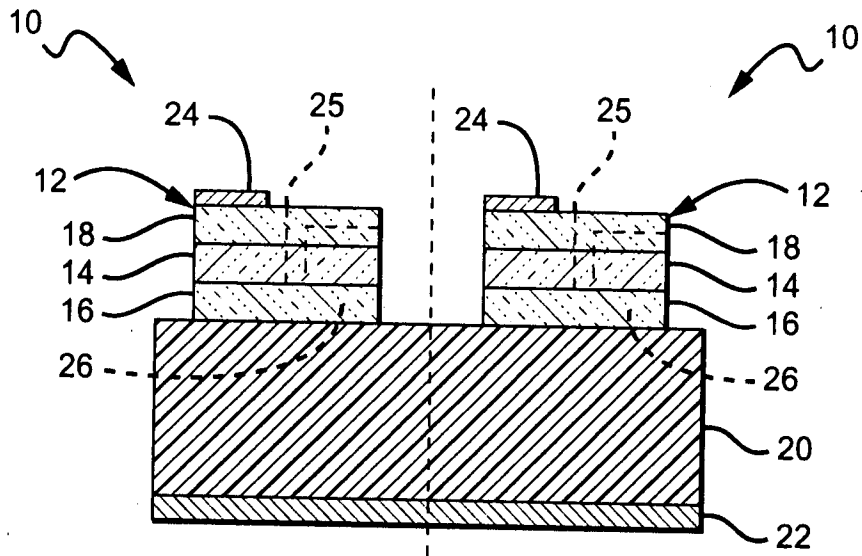


FIG. 1a

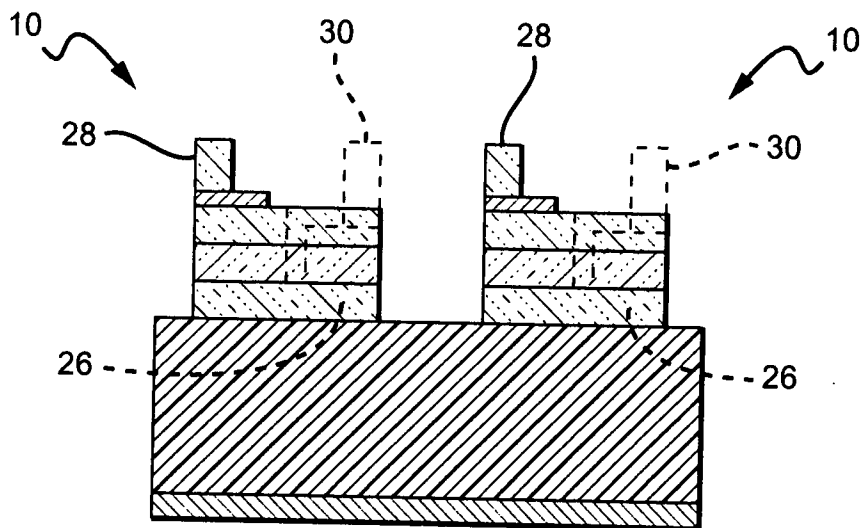


FIG. 1b

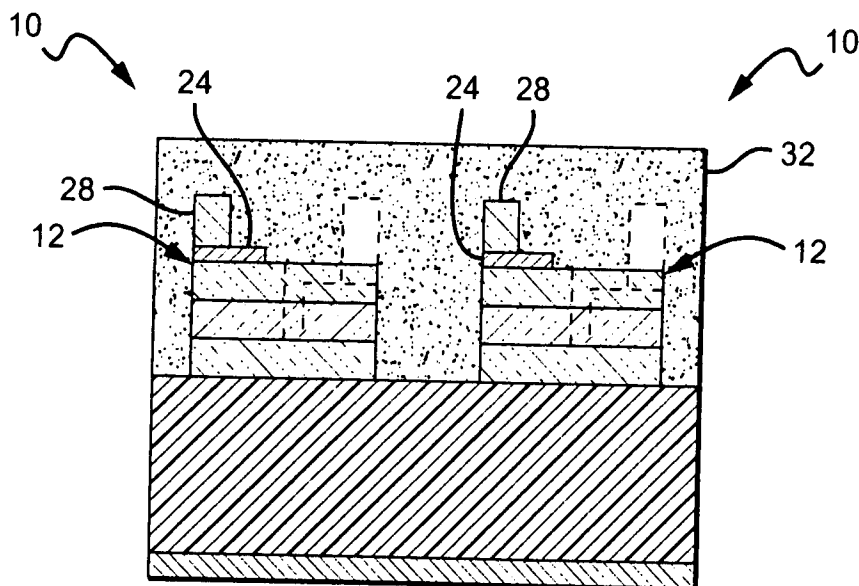


FIG. 1c

2/11

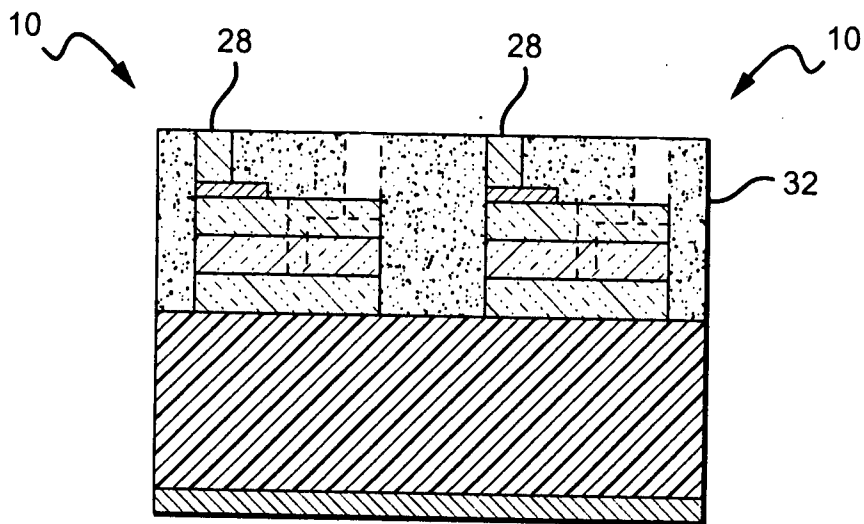


FIG. 1d

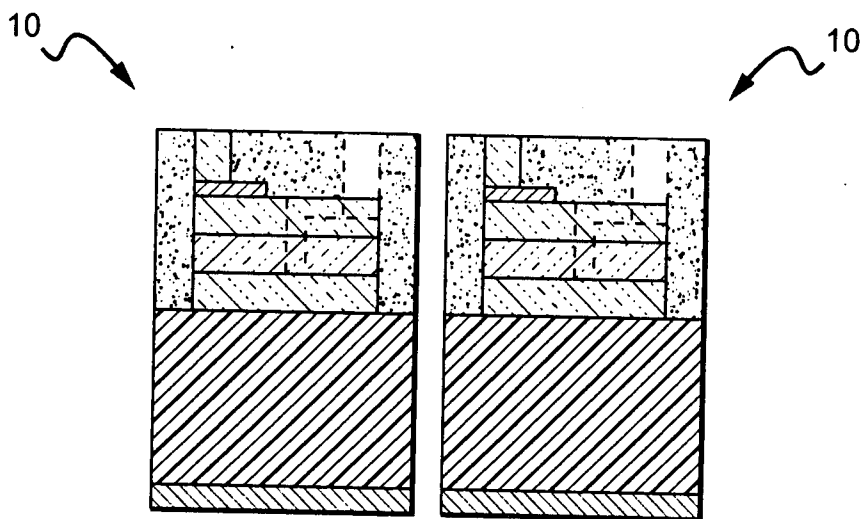


FIG. 1e

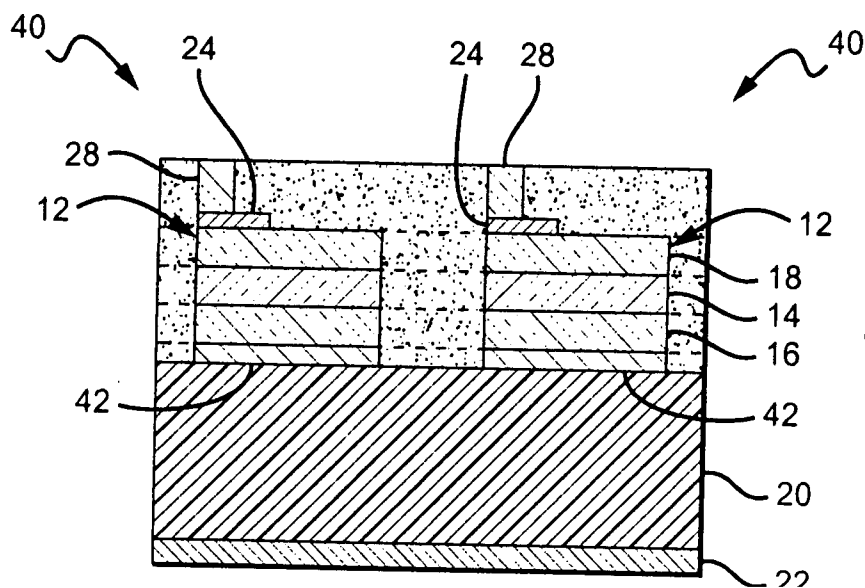


FIG. 2

3/11

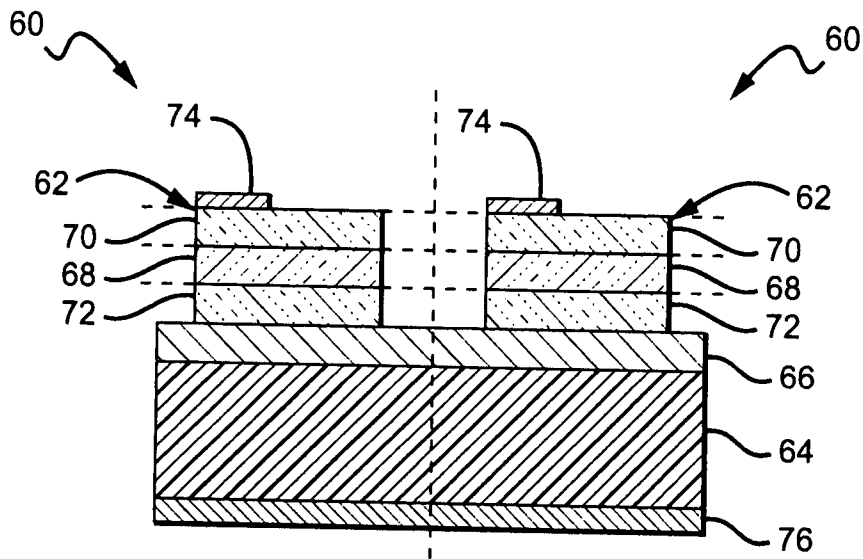


FIG. 3a

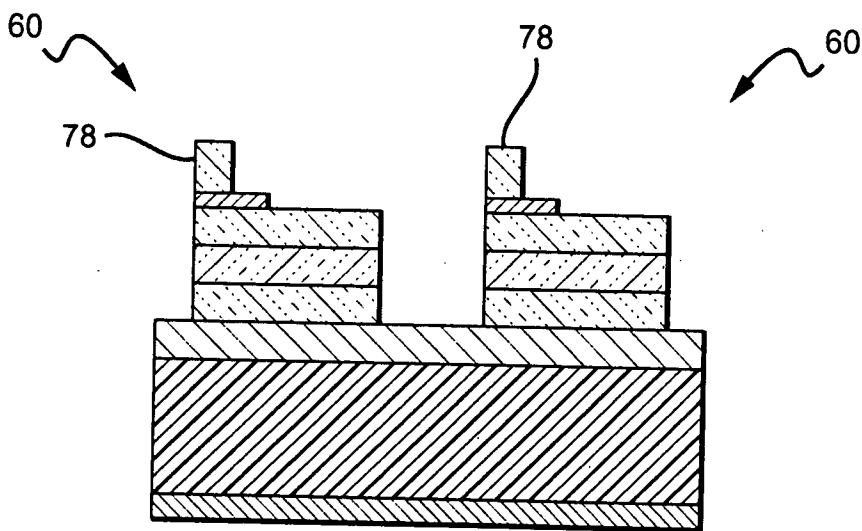


FIG. 3b

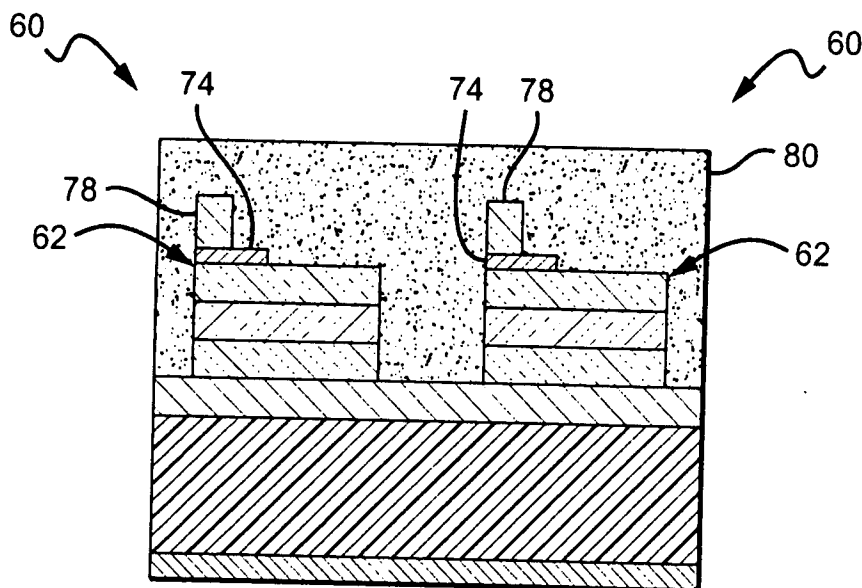


FIG. 3c

4/11

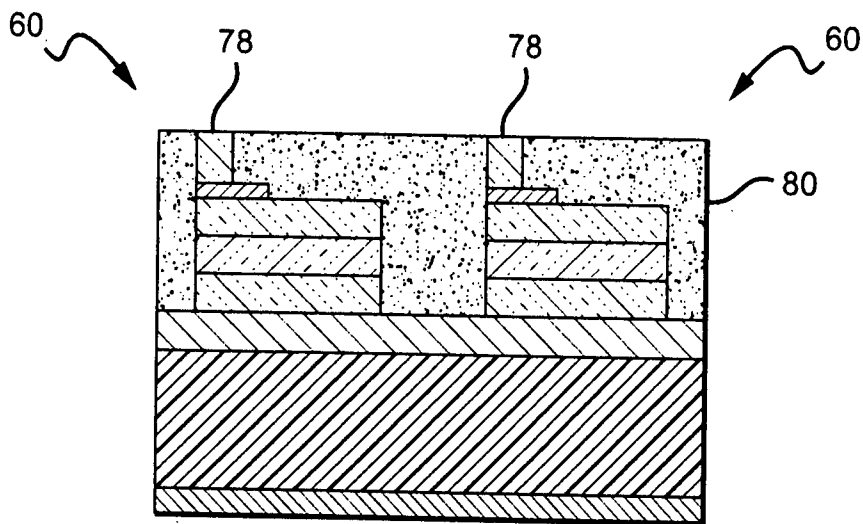


FIG. 3d

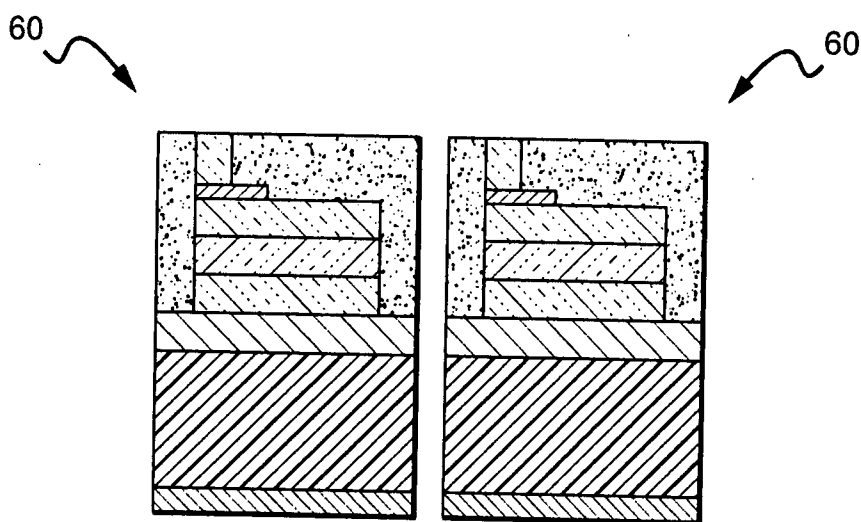


FIG. 3e

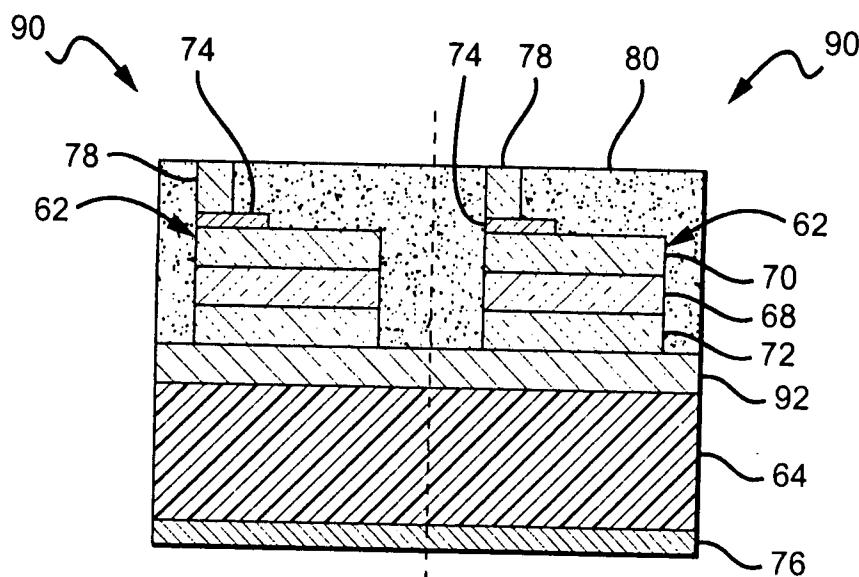
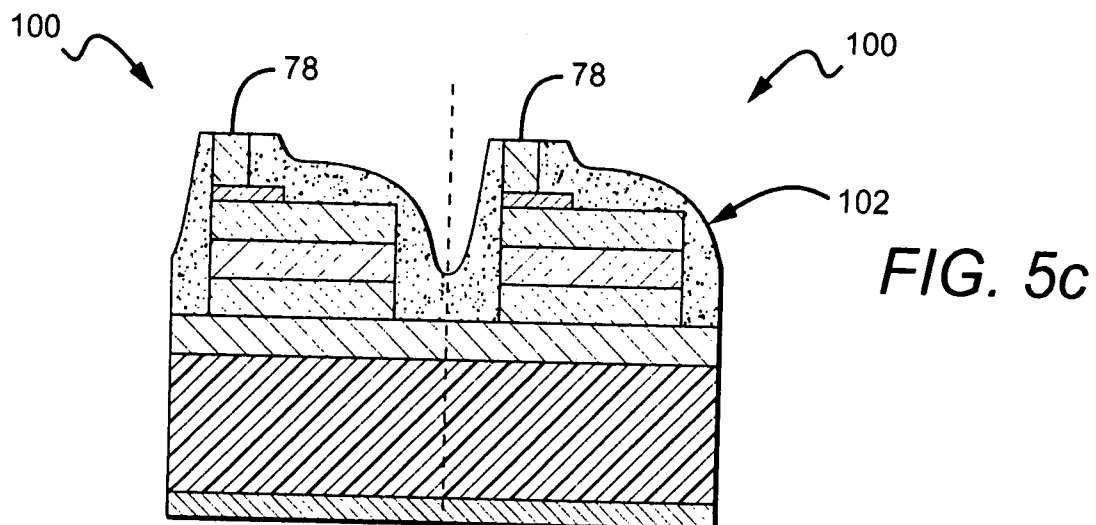
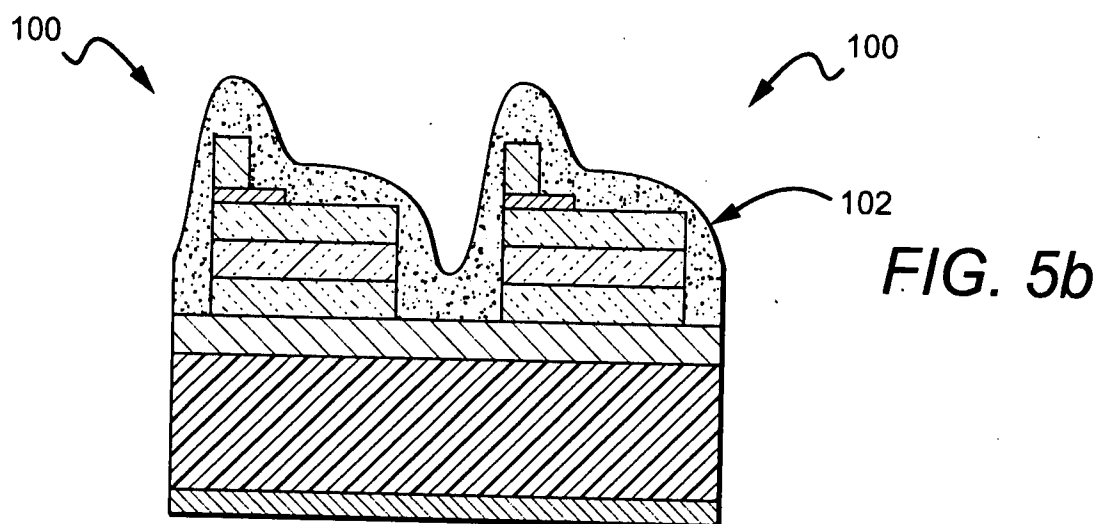
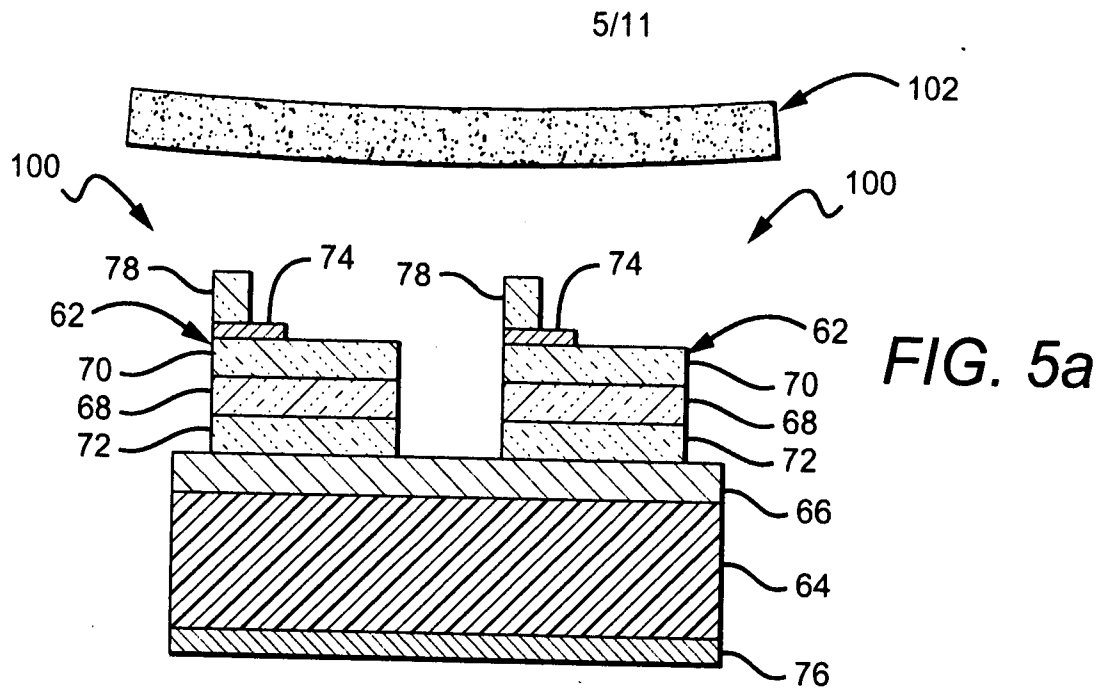


FIG. 4



6/11

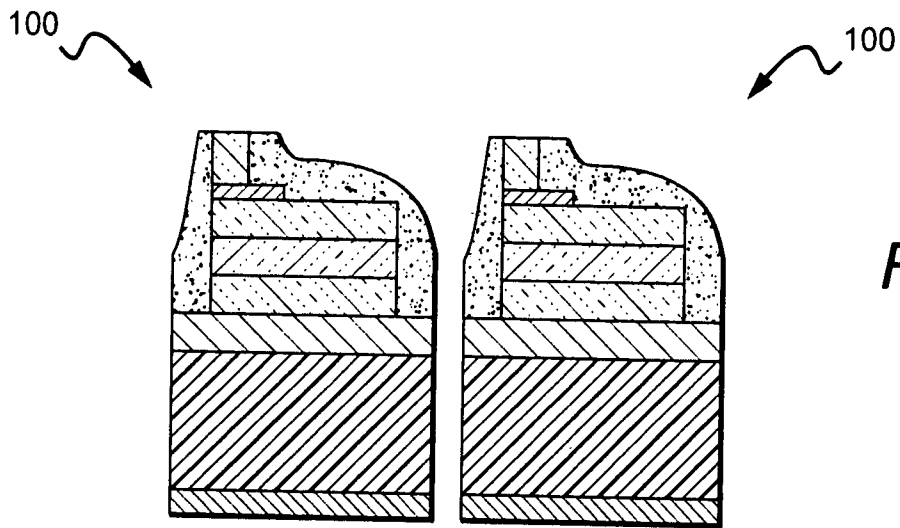


FIG. 5d

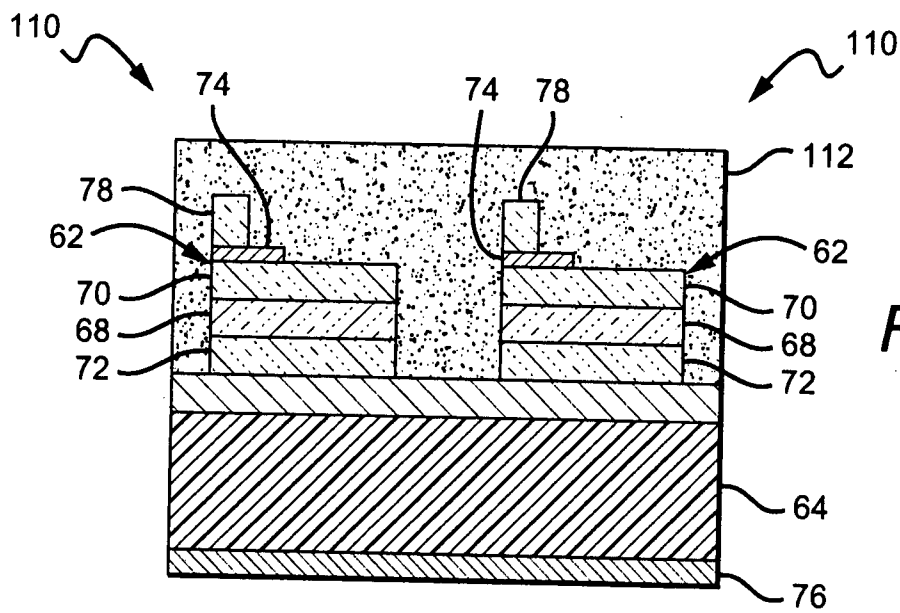


FIG. 6a

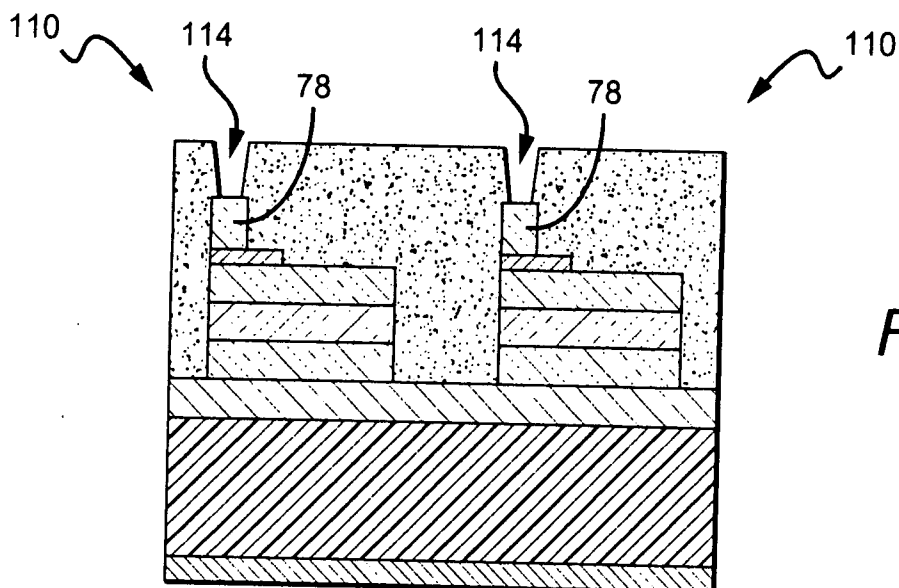


FIG. 6b

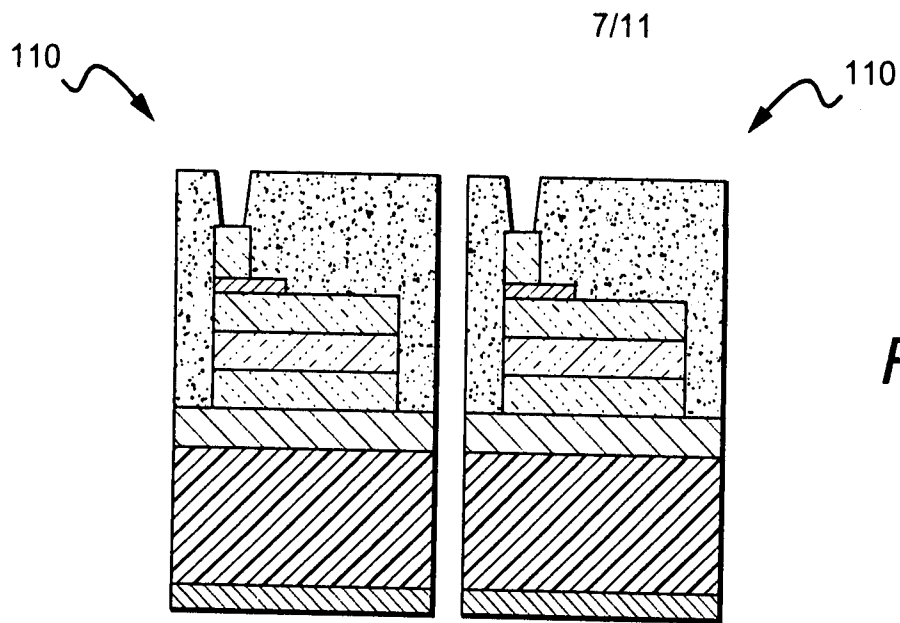


FIG. 6c

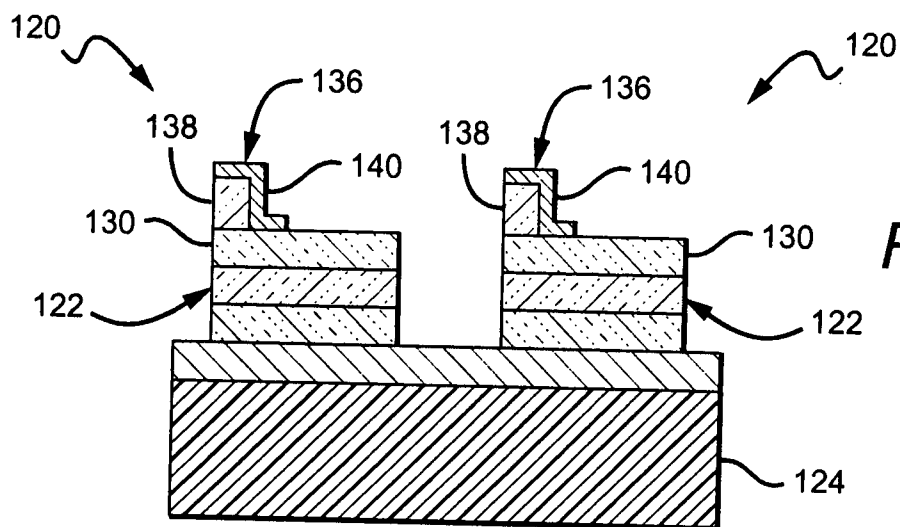


FIG. 7

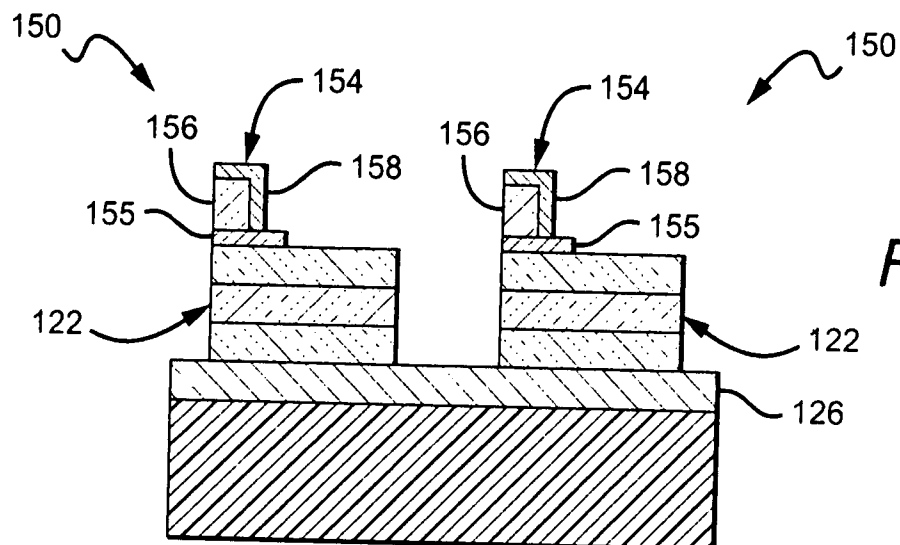


FIG. 8

FIG. 9

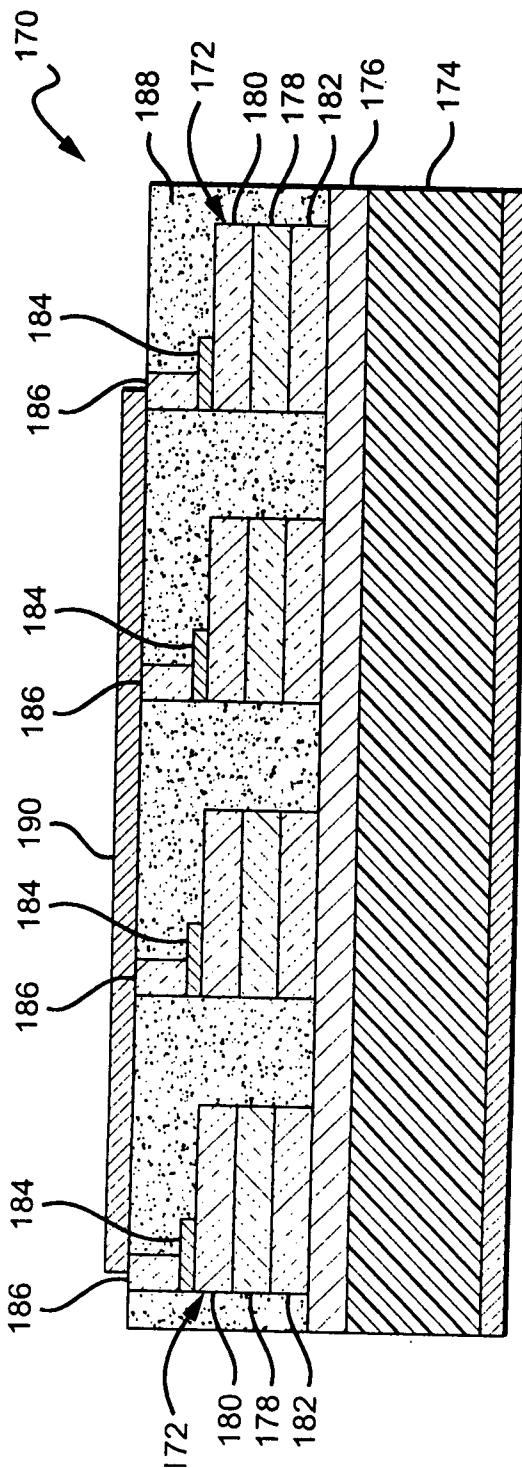
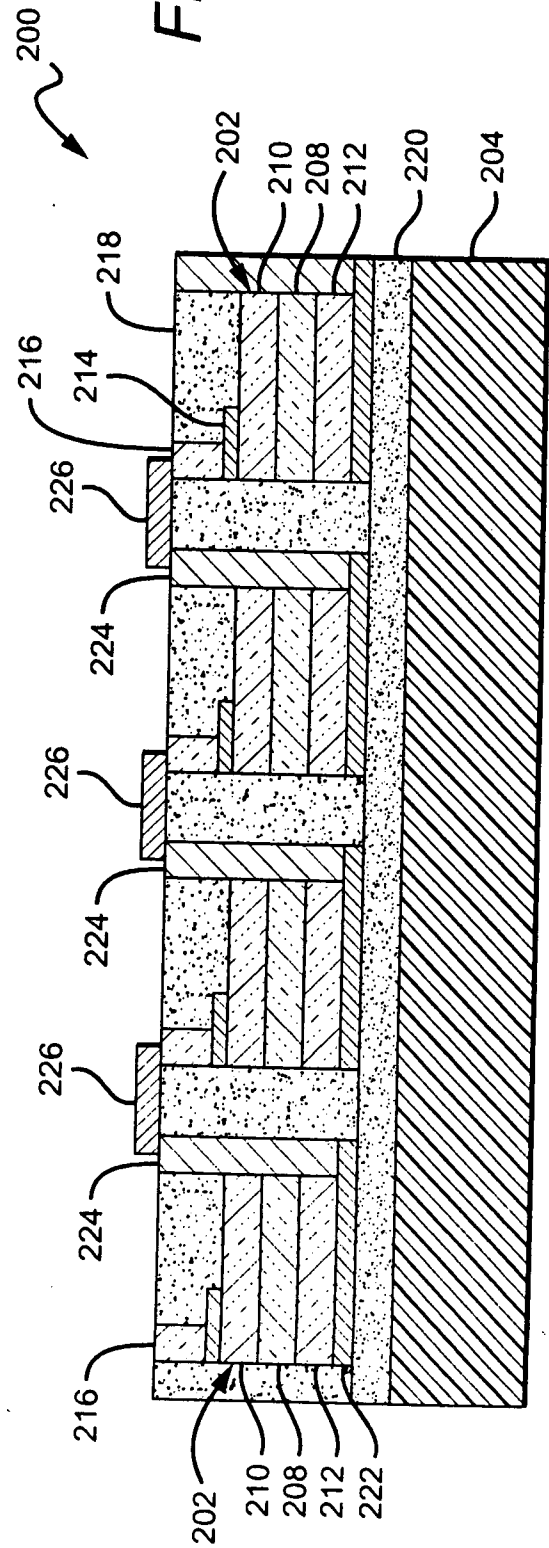


FIG. 10



9/11

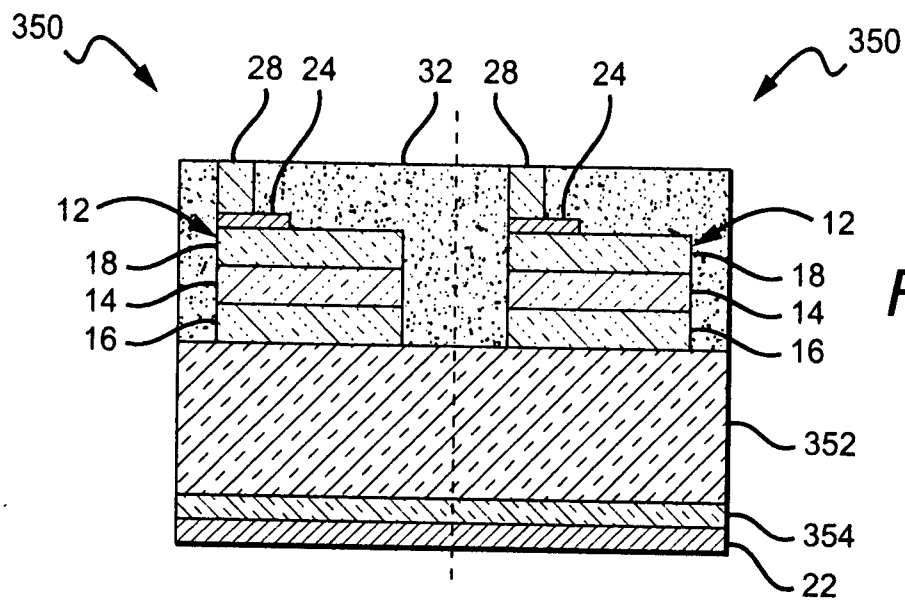


FIG. 11

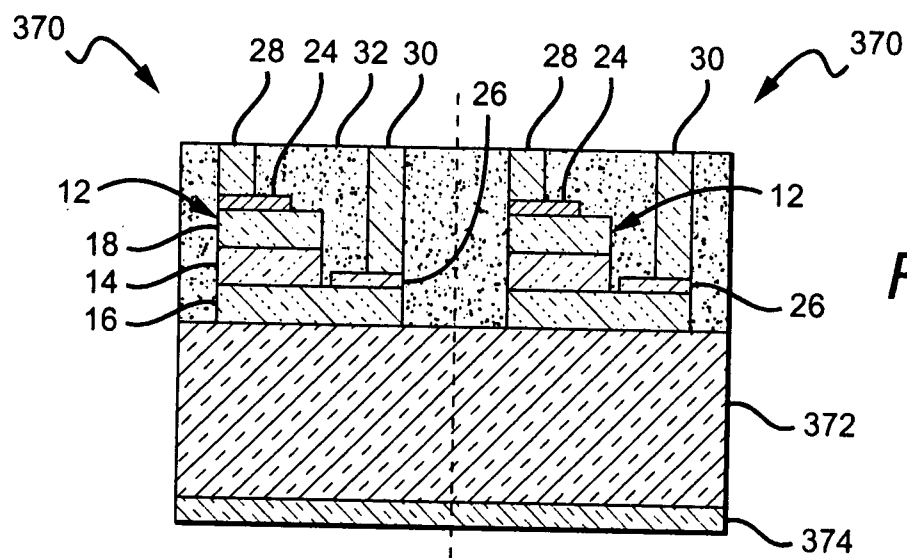


FIG. 12

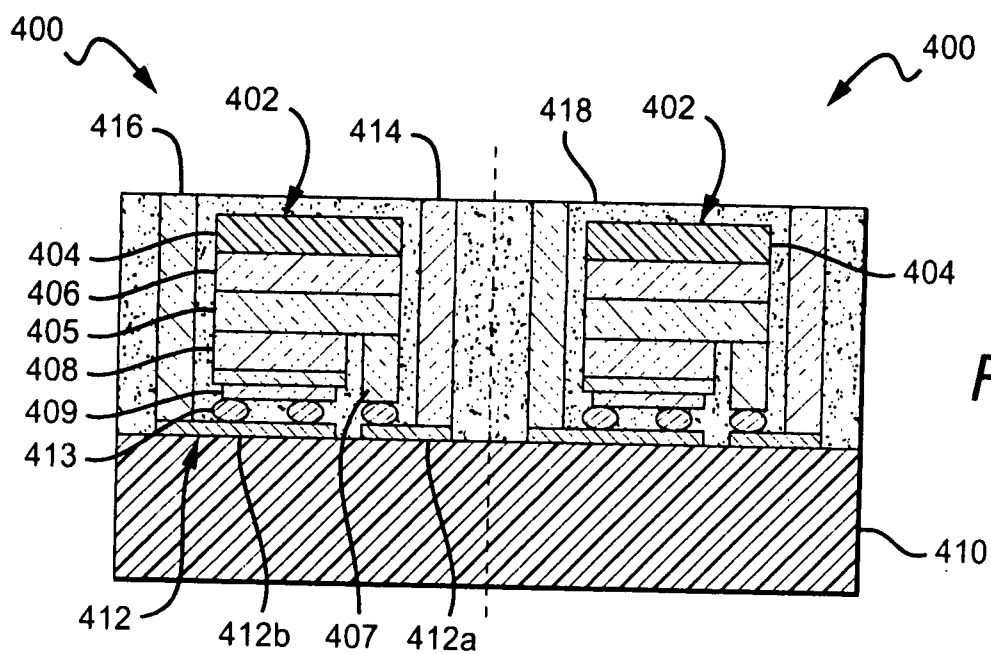


FIG. 13

10/11

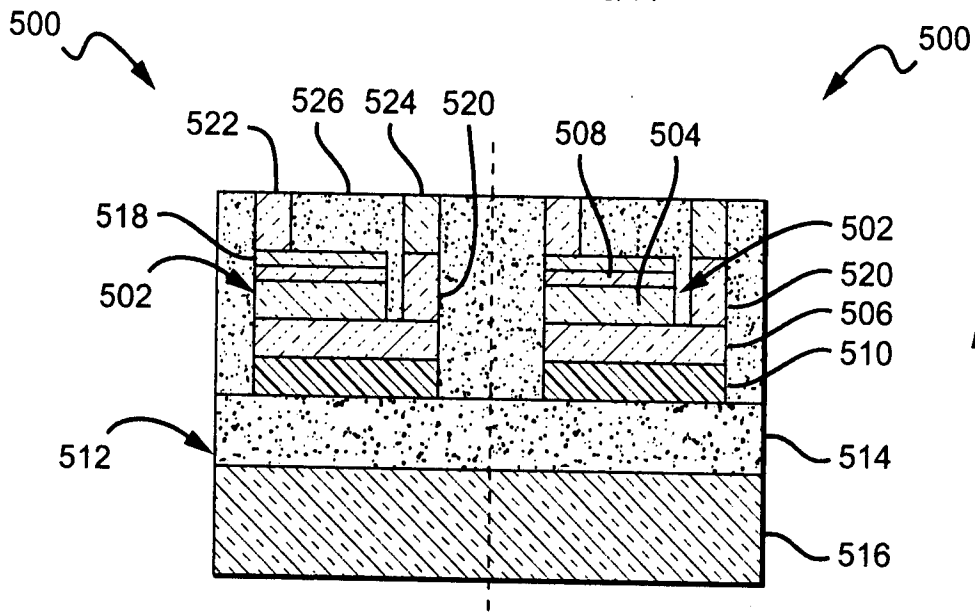


FIG. 14

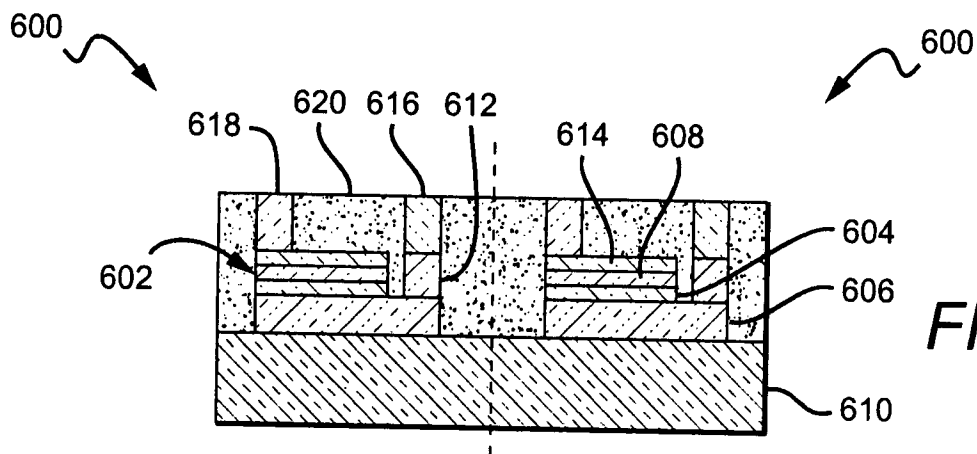


FIG. 15a

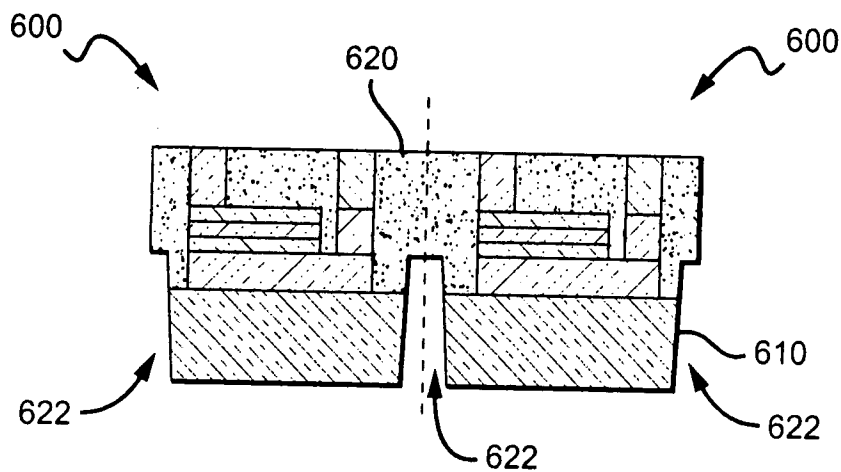


FIG. 15b

11/11

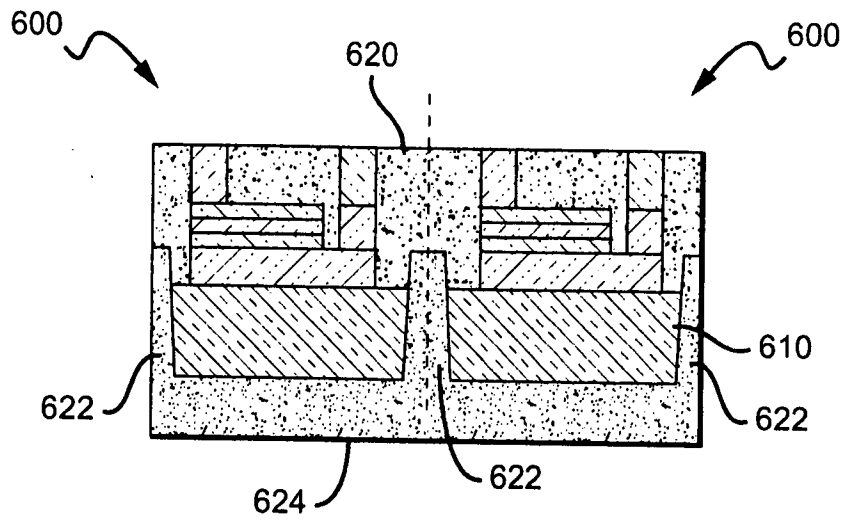


FIG. 15c

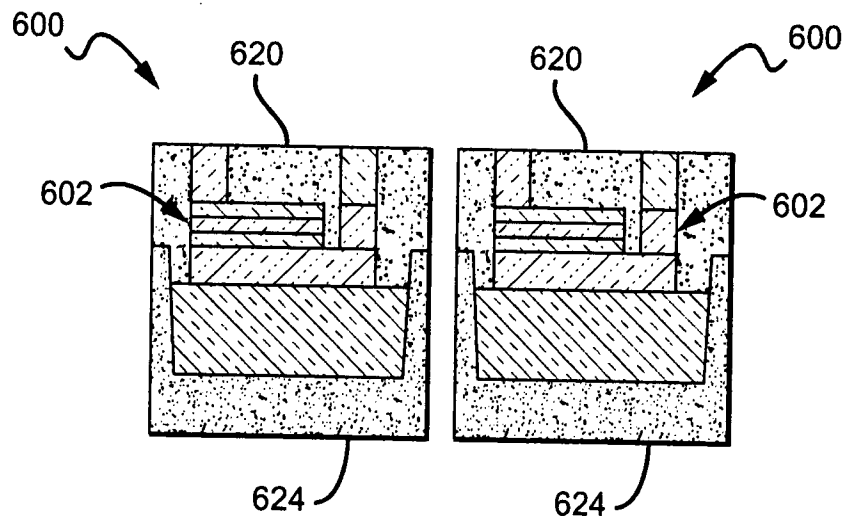


FIG. 15d