(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 4 524 943 A1**

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
19.03.2025 Bulletin 2025/12

(21) Application number: **23197615.0**

(22) Date of filing: **15.09.2023**

(51) International Patent Classification (IPC):
G09G 3/32 *(2016.01)*

(52) Cooperative Patent Classification (CPC):
G09G 3/32; G09G 3/3233; G09G 2300/0426; G09G 2300/0814; G09G 2310/0275

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC ME MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA
Designated Validation States:
KH MA MD TN

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Remarks:
Amended claims in accordance with Rule 137(2) EPC.

(54) DRIVING CIRCUIT AND METHOD FOR DRIVING A PIXEL

(57) A driving circuit (100) is provided for driving a pixel of a display. The driving circuit comprises at least one pMOS type transistor (110) comprising a gate terminal (111), a source terminal (112), and a drain terminal (113); at least one nMOS type transistor (120) comprising a gate terminal (121), a source terminal (122), and a drain terminal (123); and a metal base (130) comprising an output terminal (131). In this regard, the metal base (130) is configured to connect the drain terminal (113) of the at least one pMOS type transistor (110) or the drain terminal (123) of the at least one nMOS type transistor (120) to the output terminal (131) to output a driving signal (132) for driving the pixel.

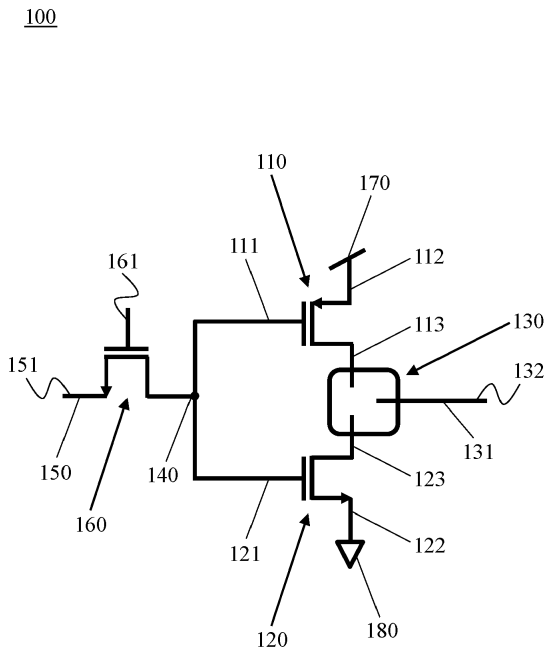

Fig. 1

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Description

[0001] The invention relates to pixel driving circuitry, especially to display drivers for driving pixels of a display.

[0002] Generally, for displays, common-cathode configuration of the light-emitting elements, e.g., light-emitting diodes (LEDs), is widely used due to their availability in a higher quality, e.g., in Thin Film Transistor (TFT) technology, and ease of manufacturing, e.g., in Organic Light-Emitting Diode (OLED) technology. However, new display technologies, such as micro LEDs (uLED), are more amenable to common-anode configuration in view of process technology.

[0003] For example, the document EP 2 642 476 B1 discloses separate pixel driving circuits for driving OLED pixels with common-anode and common-cathode configurations. However, the separate driver circuitry may limit the flexibility to select the display configurations based on a target application. Furthermore, designing a completely new driver circuitry tailor-made for the available or selected display configuration may be time consuming and cost-intensive.

[0004] Accordingly, an object of the invention is to provide a driving circuit and a method to facilitate a unified pixel driver that can drive either a common-cathode or common-anode configured LED display, in order to address the above-mentioned limitations.

[0005] The object is solved by the features of the first independent claim for the driving circuit and by the features of the second independent claim for the method. The dependent claims contain further developments.

[0006] According to a first aspect of the invention, a driving circuit is provided for driving a pixel of a display. The driving circuit comprises at least one pMOS type transistor comprising a gate terminal, a source terminal, and a drain terminal; at least one nMOS type transistor comprising a gate terminal, a source terminal, and a drain terminal; and a metal base comprising an output terminal.

[0007] In this regard, the metal base is configured to connect the drain terminal of the at least one pMOS type transistor or the drain terminal of the at least one nMOS type transistor to the output terminal to output a driving signal for driving the pixel.

[0008] Therefore, the invention solves the problem of driving LED displays with common-anode or common-cathode configurations using a single, unified CMOS ASIC driver design, which advantageously facilitates a far more flexibility in selecting the display configuration based on the target application.

[0009] Furthermore, the metal base may be modified or fixed, e.g., for the drain to output terminal connection based on the selected or available display configuration, at the CMOS processing fabrication, which may allow switching between the two configurations with minimal cost.

[0010] Preferably, the driving circuit further comprises an input node configured to connect the gate terminal of the at least one pMOS type transistor and the gate terminal of the at least one nMOS type transistor, and an input terminal connected to the input node. The input terminal is configured to input an input signal to the input node to drive the at least one pMOS type transistor or the at least one nMOS type transistor.

[0011] For example, the input signal may be of polarity suitable, e.g., for the nMOS type transistor and the common-anode configuration, and for the pMOS type transistor and the common-cathode configuration.

[0012] Preferably, the driving circuit further comprises a switching arrangement configured to connect the input terminal to the input node in a switchable manner. In this regard, the switching arrangement comprises or is a high voltage switch, preferably a high voltage transistor, more preferably a high voltage nMOS transistor.

[0013] For example, the high voltage transistor switch may be advantageous when the drive transistors operate in saturation or current mode. The high voltage transistor switch may help to transfer both low and high, e.g., 0 and 1, input values perfectly to the gate of the drive transistors. Furthermore, the use of a single transistor may reduce one transistor from the commonly used transmission gate data switches.

[0014] Preferably, the source terminal of the at least one pMOS type transistor is connected to a reference potential and the source terminal of the at least one nMOS type transistor is connected to a ground potential.

[0015] Advantageously, for instance, a fast and reliable switching between the drive transistors can be achieved based on the selected display configuration, especially during the display driver manufacturing process.

[0016] Preferably, the pixel corresponds to a pixel of a common-anode display, and the source terminal and the drain terminal of the at least one pMOS type transistor are interconnected (i.e., the excluded or unused transistor).

[0017] Alternatively, the pixel corresponds to a pixel of a common-cathode display, and the source terminal and the drain terminal of the at least one nMOS type transistor are interconnected (i.e., the excluded or unused transistor).

[0018] Advantageously, for instance, the interconnection between the source and drain terminals of an unused transistor may increase the implicit storage capacitance, thereby improving the display performance. Furthermore, such an interconnection may prevent an open drain connection of the unused transistor.

[0019] Preferably, the driving circuit comprises a further metal base and an inverter, the further metal base is configured to connect the input terminal to the input node or to connect the input terminal to the input node via the inverter.

[0020] For example, the input signal may be of polarity suitable for the nMOS type transistor, and the further metal base may connect the input terminal to the input node for the common-anode configuration. For the common-cathode configuration, the further metal base may connect the input terminal to the input node via the inverter in order to correct the polarity for the pMOS type

transistor.

[0021] Preferably, the metal base comprises a first stacked via arranged at a metal layer corresponding to the drain terminal of the at least one pMOS type transistor, a second stacked via arranged at a metal layer corresponding to the drain terminal of the at least one nMOS type transistor, and a single metal layer connecting the first stacked via or the second stacked via to the output terminal.

[0022] For instance, the metal layers corresponding to the drain terminals may involve different metal layers within the area of the metal base. The respective stacked via or via-stacks may advantageously bring up the different metal layers to the metal layer of the output terminal, preferably at the top metal layer.

[0023] This may facilitate a top-level design where only one metal network connects the correct data lines to the common connection of the LEDs. The use of only one metal network may further reduce metal congestion across the display, parasitics, power consumption, and area, and may improve the speed of operation.

[0024] According to a second aspect of the invention, a display system is provided. The display system comprises a common-anode display comprising a plurality of pixels; each of the plurality of pixels comprises at least one light emitting device, and a plurality of driving circuits according to the first aspect of the invention.

[0025] In this regard, each of the output terminal of the plurality of driving circuits being connected to the at least one light emitting device of the respective plurality of pixels of the common-anode display and further to the drain terminal of the respective nMOS type transistor, especially via the metal base.

[0026] According to a third aspect of the invention, a further display system is provided. The display system comprises a common-cathode display comprising a plurality of pixels; each of the plurality of pixels comprises at least one light emitting device, and a plurality of driving circuits according to the first aspect of the invention.

[0027] In this regard, each of the output terminal of the plurality of driving circuits being connected to the at least one light emitting device of the respective plurality of pixels of the common-cathode display and further to the drain terminal of the respective pMOS type transistor, especially via the metal base.

[0028] According to a fourth aspect of the invention, a method is provided for driving a pixel of a display, especially for forming/realizing a driving circuit, such as the driving circuit according to the first aspect of the invention, to drive the pixel of the display.

[0029] The method comprises the steps of providing at least one pMOS type transistor comprising a gate terminal, a source terminal, and a drain terminal; providing at least one nMOS type transistor comprising a gate terminal, a source terminal, and a drain terminal; connecting the drain terminal of the at least one pMOS type transistor or the drain terminal of the at least one nMOS type transistor to an output terminal of a metal base; and outputting a driving signal via the output terminal for driving the pixel.

[0030] Preferably, the method further comprises the steps of connecting the gate terminal of the at least one pMOS type transistor and the gate terminal of the at least one nMOS type transistor to an input node; and inputting or connecting an input signal to the input node via an input terminal connected to the input node to drive the at least one pMOS type transistor or the at least one nMOS type transistor.

[0031] Preferably, the pixel corresponds to a pixel of a common-anode display, and the method further comprises the step of interconnecting the source terminal and the drain terminal of the at least one pMOS type transistor. Alternatively, the pixel corresponds to a pixel of a common-cathode display, and the method further comprises the step of interconnecting the source terminal and the drain terminal of the at least one nMOS type transistor.

[0032] Preferably, the method further comprises the steps of arranging a first stacked via at a metal layer corresponding to the drain terminal of the at least one pMOS type transistor; arranging a second stacked via at a metal layer corresponding to the drain terminal of the at least one nMOS type transistor; and connecting the first stacked via or the second stacked via to the output terminal using a single metal layer.

[0033] It is to be noted that the display system according to the second aspect, the display system according to the third aspect, and the method according to the fourth aspect correspond to the driving circuit according to the first aspect and its implementation forms. Accordingly, the display system according to the second aspect, the display system according to the third aspect, and the method according to the fourth aspect may have corresponding implementation forms.

[0034] Exemplary embodiments of the invention are now further explained with respect to the drawings by way of example only, and not for limitation. In the drawings:

Fig. 1 shows a first exemplary embodiment of the driving circuit according to the first aspect of the invention;

Fig. 2A shows a first exemplary embodiment of the metal base;

Fig. 2B shows a second exemplary embodiment of the metal base;

Fig. 3A shows a first exemplary pixel connection scheme;

Fig. 3B shows a second exemplary pixel connection scheme;

Fig. 4A shows a third exemplary pixel connection scheme;

Fig. 4B shows a fourth exemplary pixel connection scheme;

Fig. 5 shows a second exemplary embodiment of the driving circuit according to the first aspect of the invention;

Fig. 6A shows a first exemplary embodiment of the display system according to the second aspect of the invention;

Fig. 6B shows a first exemplary embodiment of the display system according to the third aspect of the invention;

Fig. 7A shows a second exemplary embodiment of the display system according to the second aspect of the invention;

Fig. 7B shows a second exemplary embodiment of the display system according to the third aspect of the invention;

Fig. 8A shows a third exemplary embodiment of the display system according to the second aspect of the invention;

Fig. 8B shows a third exemplary embodiment of the display system according to the third aspect of the invention; and

Fig. 9 shows an exemplary embodiment of the method according to the fourth aspect of the invention.

[0035] Reference will now be made in detail to the embodiments of the present invention, examples of which are illustrated in the accompanying drawings. However, the following embodiments of the present invention may be variously modified and the range of the present invention is not limited by the following embodiments.

[0036] In Fig. 1, a first exemplary embodiment of the driving circuit 100 according to the first aspect of the invention is illustrated. The driving circuit 100 may comprise a pMOS transistor 110 comprising a gate terminal 111, a source terminal 112, and a drain terminal 113. The driving circuit may further comprise an nMOS transistor 120 comprising a gate terminal 121, a source terminal 122, and a drain terminal 123.

[0037] Furthermore, the driving circuit 100 may comprise a metal base or a metal fix 130, where the drain terminal 113 of the pMOS transistor 110 and the drain terminal 123 of the nMOS transistor 120 may be arranged on or in relation to the metal base 130. Additionally, the metal base 130 may comprise an output terminal 131 to be connected to a pixel, e.g., an LED, of a display, especially to drive the pixel.

[0038] For instance, the driving circuit 100 may comprise an input node 140 that may connect the gate terminal 111 of the pMOS transistor 110 and the gate terminal 121 of the nMOS transistor 120. In addition, an input terminal 150 may be provided, e.g., to input an input signal or data signal 151 to drive the respective gate terminals 111, 121 of the pMOS transistor 110 or the nMOS transistor 120, especially to generate a driving signal 132 for driving the pixel.

[0039] In this regard, the driving circuit 100 may comprise a switch 160 that may connect the input terminal 150 to the input node 140 in a switching manner, e.g., via a switch control signal or switch signal 161. For example, the switch 160 may comprise one or more transistors, e.g., an nMOS transistor as illustrated herein. Alternatively, the switch 160 may comprise or be a high-voltage transistor, e.g., a high-voltage nMOS transistor.

[0040] For instance, the source terminal 112 of the pMOS transistor 110 may be connected to a reference potential or supply 170, and the source terminal 122 of the nMOS transistor 120 may be connected to a ground potential or ground 180.

[0041] In Fig. 2A, a first exemplary embodiment of the metal base 130A is illustrated. For instance, the metal base 130A may be formed to drive a pixel of a common-cathode display, i.e., the pixel should be driven by the pMOS transistor 110.

[0042] For example, the metal line corresponding to the drain terminal 113 of the pMOS transistor 110 and the metal line corresponding to the drain terminal 123 of the nMOS transistor 120 may correspond to a metal layer $Metal_X$. A first stacked via 133 may be arranged at the metal line of the drain terminal 113 at the $Metal_X$ layer, and a second stacked via 134 may be arranged at the metal line of the drain terminal 123 at the $Metal_X$ layer, especially to raise the $Metal_X$ layer by a number of Y layers to arrive at a top level layer $Metal_{X+Y}$.

[0043] For instance, the output terminal 131, especially to connect to the LED pin, may be arranged at the $Metal_{X+Y}$ layer. In this regard, a single metal layer 135A may be realized to connect the first stacked via 133 to the output terminal 131, i.e., to connect the drain terminal 113 of the pMOS transistor 110 to the output terminal 131 at the $Metal_{X+Y}$ layer.

[0044] In Fig. 2B, a second exemplary embodiment of the metal base 130B is illustrated. For instance, the metal base 130B may be formed to drive a pixel of a common-anode display, i.e., the pixel should be driven by the nMOS transistor 120.

[0045] For example, the metal line corresponding to the drain terminal 113 of the pMOS transistor 110 and the metal line corresponding to the drain terminal 123 of the nMOS transistor 120 may correspond to a metal layer $Metal_X$. A first stacked via 133 may be arranged at the metal line of the drain terminal 113 at the $Metal_X$ layer, and a second stacked via 134 may be arranged at the metal line of the drain terminal 123 at the $Metal_X$ layer, especially to raise the $Metal_X$ layer by a number of Y layers to

arrive at a top level layer $Metal_{X+Y}$.

[0046] For instance, the output terminal 131, especially to connect to the LED pin, may be arranged at the $Metal_{X+Y}$ layer. In this regard, a single metal layer 135B may be realized to connect the second stacked via 134 to the output terminal 131, i.e., to connect the drain terminal 123 of the nMOS transistor 120 to the output terminal 131 at the $Metal_{X+Y}$ layer.

[0047] As such, the metal base 130A, 130B may initially comprise the first stacked via 133 arranged at the drain terminal 113 of the pMOS transistor 110 at the $Metal_X$ layer to raise the terminal connection to the $Metal_{X+Y}$ layer, the second stacked via 134 arranged at the drain terminal 123 of the nMOS transistor 120 at the $Metal_X$ layer to raise the terminal connection to the $Metal_{X+Y}$ layer, and the output terminal 131 arranged at the $Metal_{X+Y}$ layer.

[0048] After the selection of the type of display, e.g., a common-cathode display or a common-anode display, the respective single metal layer or line 135A, 135B may be formed, i.e., the single metal layer 135A for the common-cathode display or the single metal layer 135B for the common-anode display.

[0049] In Fig. 3A, a first exemplary pixel connection scheme, especially to drive a pixel of a common-anode display, is illustrated. For example, an LED 301 of a pixel of the common-anode display may be connected to the supply 170, i.e., the common-anode rail, and be driven by an nMOS transistor.

[0050] In this regard, the driving circuit 100 may be arranged such that the drain terminal 123 of the nMOS transistor 120 may be connected to the output terminal 131 connecting the LED pin, especially to drive the LED 301 by providing the driving signal 132.

[0051] For instance, the connection between the drain terminal 123 of the nMOS transistor 120 and the output terminal 131 may be realized via the metal base 130B, especially via the single metal layer 135B, where the drain terminal 113 of the pMOS transistor 110 being disconnected, thereby excluding the pMOS transistor 110 (as shown in gray).

[0052] In Fig. 3B, a second exemplary pixel connection scheme, especially to drive a pixel of a common-cathode display, is illustrated. For example, an LED 302 of a pixel of the common-cathode display may be connected to the ground 170, i.e., the common-cathode ground, and be driven by a pMOS transistor.

[0053] In this regard, the driving circuit 100 may be arranged such that the drain terminal 113 of the pMOS transistor 110 may be connected to the output terminal 131 connecting the LED pin, especially to drive the LED 302 by providing the driving signal 132.

[0054] For instance, the connection between the drain terminal 113 of the pMOS transistor 110 and the output terminal 131 may be realized via the metal base 130A, especially via the single metal layer 135A, where the drain terminal 123 of the nMOS transistor 120 being disconnected, thereby excluding the nMOS transistor 120 (as shown in gray).

[0055] In Fig. 4A, a third exemplary pixel connection scheme, especially to drive a pixel of a common-anode display, is illustrated. As such, the LED 301 of a pixel of the common-anode display may be connected to the supply 170 and be driven by an nMOS transistor.

[0056] The connection scheme differs from the connection scheme of Fig. 3A in that the source terminal 112 and the drain terminal 113 of the pMOS transistor 110, i.e., of the excluded pMOS transistor 110 shown in grey, may be connected together, and to the supply 170 via a first interconnection 401.

[0057] In this regard, the connection between the drain terminal 123 of the nMOS transistor 120 and the output terminal 131 may be realized via the metal base 130B, especially via the single metal layer 135B. Additionally, the source terminal 112 of the pMOS transistor 110 may be raised to $Metal_{X+Y}$ layer, e.g., by means of a further stacked via. Accordingly, the interconnection 401 may be realized, e.g., by means of a further metal line connecting the stacked vias, at the $Metal_{X+Y}$ layer to interconnect the source terminal 112 and the drain terminal 113 of the pMOS transistor 110.

[0058] In Fig. 4B, a fourth exemplary pixel connection scheme, especially to drive a pixel of a common-cathode display, is illustrated. As such, the LED 302 of a pixel of the common-cathode display may be connected to the ground 180 and be driven by a pMOS transistor.

[0059] The connection scheme differs from the connection scheme of Fig. 3B in that the source terminal 122 and the drain terminal 123 of the nMOS transistor 120, i.e., of the excluded nMOS transistor 120 shown in grey, may be connected together, and to the ground 180 via a second interconnection 402.

[0060] In this regard, the connection between the drain terminal 113 of the pMOS transistor 110 and the output terminal 131 may be realized via the metal base 130A, especially via the single metal layer 135A. Additionally, the source terminal 122 of the nMOS transistor 120 may be raised to $Metal_{X+Y}$ layer, e.g., by means of a further stacked via. Accordingly, the interconnection 402 may be realized, e.g., by means of a further metal line connecting the stacked vias, at the $Metal_{X+Y}$ layer to interconnect the source terminal 122 and the drain terminal 123 of the nMOS transistor 120.

[0061] In Fig. 5, a second exemplary embodiment of the driving circuit 500 according to the first aspect of the invention is illustrated. The driving circuit 500 differs from the driving circuit 100 in that the driving circuit 500 may comprise a further metal base or metal fix 501 and an inverter arrangement.

[0062] In this regard, the input terminal 150 may be split into a first path comprising an inverter 502 and a second path or direct path 503, especially connected to the switch 160 via the further metal base 501.

[0063] For example, the first path connected to the further metal base 501, especially the connection to the inverter 502, may be raised to the $Metal_{X+Y}$ layer,

e.g., by means of a stacked via, and the second path 503 connected to the further metal base 501, especially the connection to the second path 503, may be raised to the $Metal_{X+Y}$ layer.

[0064] As such, the further metal base 501 may initially comprise a stacked via arranged at the first path to raise the terminal connection of the inverter 502 to the $Metal_{X+Y}$ layer, a stacked via arranged at the second path 503 to raise the terminal connection of the second path 503 to the $Metal_{X+Y}$ layer, and a terminal arranged at the $Metal_{X+Y}$ layer to connect the switch 160.

[0065] After the selection of the type of display, e.g., a common-cathode display or a common-anode display, a respective single metal layer or line may be formed, i.e., a single metal layer for the common-cathode display connecting the inverter 502 to the switch 160 or a single metal layer for the common-anode display connecting the direct path 503 to the switch 160.

[0066] For example, for the common-cathode display, the single metal layer 135A and the single metal layer connecting the inverter 502 to the switch 160 may be formed simultaneously. Analogously, for the common-anode display, the single metal layer 135B and the single metal layer connecting the direct path 503 to the switch 160 may be formed simultaneously. The single metal layers may be realized via one or two masks, e.g., two mask sets different by only one metal layer, especially switched at process foundry, based on the selection of the type of the display. The minimal mask updates may save costs and complexity.

[0067] In Fig. 6A, a first exemplary embodiment of the display system 600A according to the second aspect of the invention is illustrated. The display system 600A may comprise a plurality of pixels in a common-anode configuration, especially in a two-dimensional array, where each of the pixels may comprise a respective LED 601_{11}-601_{mn}.

[0068] For driving the LEDs 601_{11}-601_{mn}, a respective driving circuit 100_{11}-100_{mn} may be provided, where for each of the driving circuits 100_{11}-100_{mn}, the pMOS transistor 110 may be excluded while connecting the drain terminal 123 of the nMOS transistor 120 to the respective LED pin of the LEDs 601_{11}-601_{mn}.

[0069] Furthermore, a common data line D_1-D_m may be arranged per row connecting the input terminals 150 of the respective driving circuits 100_{11}-100_{mn}, arranged in said row. Moreover, a common switch line SW_1-SW_n may be arranged per column connecting the switches 160 of the respective driving circuits 100_{11}-100_{mn}, arranged in said column.

[0070] In Fig. 6B, a first exemplary embodiment of the display system 600B according to the third aspect of the invention is illustrated. The display system 600B may comprise a plurality of pixels in a common-cathode configuration, especially in a two-dimensional array, where each of the pixels may comprise a respective LED 602_{11}-602_{mn}.

[0071] For driving the LEDs 602_{11}-602_{mn}, a respective driving circuit 100_{11}-100_{mn} may be provided, where for each of the driving circuits 100_{11}-100_{mn}, the nMOS transistor 120 may be excluded while connecting the drain terminal 113 of the pMOS transistor 110 to the respective LED pin of the LEDs 602_{11}-602_{mn}.

[0072] Furthermore, a common data line D_1-D_m may be arranged per row connecting the input terminals 150 of the respective driving circuits 100_{11}-100_{mn}, arranged in said row. Moreover, a common switch line SW_1-SW_n may be arranged per column connecting the switches 160 of the respective driving circuits 100_{11}-100_{mn}, arranged in said column.

[0073] In Fig. 7A, a second exemplary embodiment of the display system 700A according to the second aspect of the invention in a common-anode configuration is illustrated. The display system 700A may differ from the display system 600A in that the display system 700A may additionally comprise the inverter arrangement of Fig. 5, especially realized such that only one inverter arrangement may be implemented per row of the driving circuits 100_{11}-100_{mn}.

[0074] For instance, the respective driving circuit 100_{11}-100_{mn}, may be replaced with the driving circuit 500 such that one further metal base 501 and one inverter arrangement comprising the inverter 502 and the direct path 503 may be arranged per row. In this regard, a common output line may be provided from the further metal base 501 connecting the direct path 503 to the respective switches 160 of the driving circuits 500 arranged in said row.

[0075] In Fig. 7B, a second exemplary embodiment of the display system 700B according to the third aspect of the invention in a common-cathode configuration is illustrated. The display system 700B may differ from the display system 600B in that the display system 700B may additionally comprise the inverter arrangement of Fig. 5, especially realized such that only one inverter arrangement may be implemented per row of the driving circuits 100_{11}-100_{mn}.

[0076] For instance, the respective driving circuit 100_{11}-100_{mn}, may be replaced with the driving circuit 500 such that one further metal base 501 and one inverter arrangement comprising the inverter 502 and the direct path 503 may be arranged per row. In this regard, a common output line may be provided from the further metal base 501 connecting the inverter 502 to the respective switches 160 of the driving circuits 500 arranged in said row.

[0077] In Fig. 8A, a third exemplary embodiment of the display system 800A according to the second aspect of the invention in a common-anode configuration is illustrated. The display system 800A may differ from the display system 600A in that the display system 800A may additionally comprise the inverter arrangement of Fig. 5, especially realized such that each of the driving circuits 100_{11}-100_{mn}, may comprise the inverter arrangement.

[0078] For instance, the respective driving circuit 100_{11}-100_{mn}, may be replaced with the driving circuit

500 such that one further metal base 501 and one inverter arrangement comprising the inverter 502 and the direct path 503 may be arranged per driving circuit 100_{11}-100_{mn}. In this regard, the common data line D_1-D_m per row may be connected to the respective input terminals 150 of the inverter arrangements of the respective driving circuits arranged in said row. In this regard, the metal base 501 may connect the direct path 503 to the input terminals 150.

[0079] In Fig. 8B, a third exemplary embodiment of the display system 800B according to the third aspect of the invention in a common-cathode configuration is illustrated. The display system 800B may differ from the display system 600B in that the display system 800B may additionally comprise the inverter arrangement of Fig. 5, especially realized such that each of the driving circuits 100_{11}-100_{mn}, may comprise the inverter arrangement.

[0080] For instance, the respective driving circuit 100_{11}-100_{mn}, may be replaced with the driving circuit 500 such that one further metal base 501 and one inverter arrangement comprising the inverter 502 and the direct path 503 may be arranged per driving circuit 100_{11}-100_{mn}. In this regard, the common data line D_1-D_m per row may be connected to the respective input terminals 150 of the inverter arrangements of the respective driving circuits arranged in said row. In this regard, the metal base 501 may connect the inverter 502 to the input terminals 150.

[0081] In Fig. 9, an exemplary embodiment of the method 900 according to the fourth aspect of the invention is illustrated. In a first step 901, at least one pMOS type transistor comprising a gate terminal, a source terminal, and a drain terminal is provided. In a second step 902, at least one nMOS type transistor comprising a gate terminal, a source terminal, and a drain terminal is provided.

[0082] In a third step 903, the drain terminal of the at least one pMOS type transistor (in common-cathode display configuration) or the drain terminal of the at least one nMOS type transistor (in common-anode display configuration) is connected to an output terminal of a metal base. In a fourth step 904, a driving signal is outputted via the output terminal for driving the pixel.

[0083] It is important to note that, in the description as well as in the claims, the word "comprising" does not exclude other elements or steps and the indefinite article "a" or "an" does not exclude a plurality. A single element or other unit may fulfill the functions of several entities or items recited in the claims. Furthermore, the word "connected" implies that the elements may be directly connected together or may be coupled through one or more intervening elements. Moreover, the disclosure with regard to any of the aspects is also relevant with regard to the other aspects of the disclosure.

[0084] Although the invention has been illustrated and described with respect to one or more implementations, equivalent alterations and modifications will occur to others skilled in the art upon the reading and understanding of this specification and the annexed drawings. In addition, while a particular feature of the invention may have been disclosed with respect to only one of several implementations, such feature may be combined with one or more other features of the other implementations as may be desired and advantageous for any given or particular application.

Claims

1. A driving circuit (100, 500) for driving a pixel of a display, comprising:

at least one pMOS type transistor (110) comprising a gate terminal (111), a source terminal (112), and a drain terminal (113);
at least one nMOS type transistor (120) comprising a gate terminal (121), a source terminal (122), and a drain terminal (123); and
a metal base (130) comprising an output terminal (131), wherein the metal base (130) is configured to connect the drain terminal (113) of the at least one pMOS type transistor (110) or the drain terminal (123) of the at least one nMOS type transistor (120) to the output terminal (131) to output a driving signal (132) for driving the pixel.

2. The driving circuit according to claim 1,
wherein the driving circuit further comprises:

an input node (140) configured to connect the gate terminal (111) of the at least one pMOS type transistor (110) and the gate terminal (121) of the at least one nMOS type transistor (120); and
an input terminal (150) connected to the input node (140), the input terminal (150) is configured to input an input signal (151) to the input node (140) to drive the at least one pMOS type transistor (110) or the at least one nMOS type transistor (120).

3. The driving circuit according to claim 2,
wherein the driving circuit further comprises a switching arrangement (160) configured to connect the input terminal (150) to the input node (140) in a switchable manner.

4. The driving circuit according to claim 3,
wherein the switching arrangement (160) comprises a high voltage switch, preferably a high voltage transistor.

5. The driving circuit according to any of claims 1 to 4,
wherein the source terminal (112) of the at least one pMOS type transistor (110) is connected to a reference potential (170) and the source terminal (122) of

the at least one nMOS type transistor (120) is connected to a ground potential (180) .

6. The driving circuit according to any of claims 1 to 5, wherein the pixel corresponds to a pixel (301) of a common-anode display, and the source terminal (112) and the drain terminal (113) of the at least one pMOS type transistor (110) are interconnected.

7. The driving circuit according to any of claims 1 to 5, wherein the pixel corresponds to a pixel (302) of a common-cathode display, and the source terminal (122) and the drain terminal (123) of the at least one nMOS type transistor (120) are interconnected.

8. The driving circuit according to claim 2,
wherein the driving circuit comprises a further metal base (501) and an inverter (502), the further metal base (501) is configured to connect the input terminal (150) to the input node (140) or to connect the input terminal (150) to the input node (140) via the inverter (502).

9. The driving circuit according to any of claims 1 to 8, wherein the metal base (130) comprises:

a first stacked via (133) arranged at a metal layer corresponding to the drain terminal (113) of the at least one pMOS type transistor (110);
a second stacked via (134) arranged at a metal layer corresponding to the drain terminal (123) of the at least one nMOS type transistor (120); and
a single metal layer (135A, 135B) connecting the first stacked via (133) or the second stacked via (134) to the output terminal (131).

10. A display system (600A, 700A, 800A) comprising:

a common-anode display comprising a plurality of pixels (601), each of the plurality of pixels (601) comprises at least one light emitting device; and
a plurality of driving circuits (100) according to any of claims 1 to 9, each of the output terminal of the plurality of driving circuits (100) being connected to the at least one light emitting device of the respective plurality of pixels (601) of the common-anode display and further to the drain terminal of the respective nMOS type transistor.

11. A display system (600B, 700B, 800B) comprising:

a common-cathode display comprising a plurality of pixels (602), each of the plurality of pixels (602) comprises at least one light emitting device; and
a plurality of driving circuits (100) according to any of claims 1 to 9, each of the output terminal of the plurality of driving circuits (100) being connected to the at least one light emitting device of the respective plurality of pixels (602) of the common-cathode display and further to the drain terminal of the respective pMOS type transistor.

12. A method (900) for driving a pixel of a display comprising:

providing (901) at least one pMOS type transistor comprising a gate terminal, a source terminal, and a drain terminal;
providing (902) at least one nMOS type transistor comprising a gate terminal, a source terminal, and a drain terminal;
connecting (903) the drain terminal of the at least one pMOS type transistor or the drain terminal of the at least one nMOS type transistor to an output terminal of a metal base; and
outputting (904) a driving signal via the output terminal for driving the pixel.

13. The method according to claim 12,
wherein the method further comprising:

connecting the gate terminal of the at least one pMOS type transistor and the gate terminal of the at least one nMOS type transistor to an input node; and
inputting an input signal to the input node via an input terminal connected to the input node to drive the at least one pMOS type transistor or the at least one nMOS type transistor.

14. The method according to claim 12 or 13,

wherein the pixel corresponds to a pixel of a common-anode display, and the method further comprising interconnecting the source terminal and the drain terminal of the at least one pMOS type transistor, or
wherein the pixel corresponds to a pixel of a common-cathode display, and the method further comprising interconnecting the source terminal and the drain terminal of the at least one nMOS type transistor.

15. The method according to any of claims 11 to 14,
wherein the method further comprising:

arranging a first stacked via at a metal layer corresponding to the drain terminal of the at least one pMOS type transistor;
arranging a second stacked via arranged at a metal layer corresponding to the drain terminal of the at least one nMOS type transistor; and

connecting the first stacked via or the second stacked via to the output terminal using a single metal layer.

Amended claims in accordance with Rule 137(2) EPC.

1. A driving circuit (100, 500) for driving a pixel of a display, comprising:

at least one pMOS type transistor (110) comprising a gate terminal (111), a source terminal (112), and a drain terminal (113);
at least one nMOS type transistor (120) comprising a gate terminal (121), a source terminal (122), and a drain terminal (123); and
a metal base (130) comprising an output terminal (131), wherein the metal base (130) connects either the drain terminal (113) of the at least one pMOS type transistor (110) to the output terminal (131) or the drain terminal (123) of the at least one nMOS type transistor (120) to the output terminal (131) in order to output a driving signal (132) for driving the pixel.

2. The driving circuit according to claim 1, wherein the driving circuit further comprises:

an input node (140) connecting the gate terminal (111) of the at least one pMOS type transistor (110) and the gate terminal (121) of the at least one nMOS type transistor (120); and
an input terminal (150) connected to the input node (140), wherein the input terminal (150) inputs an input signal (151) to the input node (140) to drive the at least one pMOS type transistor (110) or the at least one nMOS type transistor (120).

3. The driving circuit according to claim 2, wherein the driving circuit further comprises a switching arrangement (160) configured to connect the input terminal (150) to the input node (140) in a switchable manner.

4. The driving circuit according to claim 3, wherein the switching arrangement (160) comprises a high voltage switch, preferably a high voltage transistor.

5. The driving circuit according to any of claims 1 to 4, wherein the source terminal (112) of the at least one pMOS type transistor (110) is connected to a reference potential (170) and the source terminal (122) of the at least one nMOS type transistor (120) is connected to a ground potential (180) .

6. The driving circuit according to any of claims 1 to 5, wherein the pixel corresponds to a pixel (301) of a common-anode display, and the source terminal (112) and the drain terminal (113) of the at least one pMOS type transistor (110) are interconnected.

7. The driving circuit according to any of claims 1 to 5, wherein the pixel corresponds to a pixel (302) of a common-cathode display, and the source terminal (122) and the drain terminal (123) of the at least one nMOS type transistor (120) are interconnected.

8. The driving circuit according to claim 2, wherein the driving circuit comprises a further metal base (501) and an inverter (502), the further metal base (501) is configured to connect the input terminal (150) to the input node (140) or to connect the input terminal (150) to the input node (140) via the inverter (502).

9. The driving circuit according to any of claims 1 to 8, wherein the metal base (130) comprises:

a first stacked via (133) arranged at a metal layer corresponding to the drain terminal (113) of the at least one pMOS type transistor (110);
a second stacked via (134) arranged at a metal layer corresponding to the drain terminal (123) of the at least one nMOS type transistor (120); and
a single metal layer (135A, 135B) connecting the first stacked via (133) or the second stacked via (134) to the output terminal (131).

10. A display system (600A, 700A, 800A) comprising:

a common-anode display comprising a plurality of pixels (601), each of the plurality of pixels (601) comprises at least one light emitting device; and
a plurality of driving circuits (100) according to any of claims 1 to 9, each of the output terminal of the plurality of driving circuits (100) being connected to the at least one light emitting device of the respective plurality of pixels (601) of the common-anode display and further to the drain terminal of the respective nMOS type transistor.

11. A display system (600B, 700B, 800B) comprising:

a common-cathode display comprising a plurality of pixels (602), each of the plurality of pixels (602) comprises at least one light emitting device; and
a plurality of driving circuits (100) according to any of claims 1 to 9, each of the output terminal of the plurality of driving circuits (100) being connected to the at least one light emitting device of the respective plurality of pixels (602) of the

common-cathode display and further to the drain terminal of the respective pMOS type transistor.

12. A method (900) for driving a pixel of a display comprising:

providing (901) at least one pMOS type transistor comprising a gate terminal, a source terminal, and a drain terminal;
providing (902) at least one nMOS type transistor comprising a gate terminal, a source terminal, and a drain terminal;
connecting (903) either the drain terminal of the at least one pMOS type transistor or the drain terminal of the at least one nMOS type transistor to an output terminal of a metal base; and
outputting (904) a driving signal via the output terminal for driving the pixel.

13. The method according to claim 12, wherein the method further comprising:

connecting the gate terminal of the at least one pMOS type transistor and the gate terminal of the at least one nMOS type transistor to an input node; and
inputting an input signal to the input node via an input terminal connected to the input node to drive the at least one pMOS type transistor or the at least one nMOS type transistor.

14. The method according to claim 12 or 13,

wherein the pixel corresponds to a pixel of a common-anode display, and the method further comprising interconnecting the source terminal and the drain terminal of the at least one pMOS type transistor, or
wherein the pixel corresponds to a pixel of a common-cathode display, and the method further comprising interconnecting the source terminal and the drain terminal of the at least one nMOS type transistor.

15. The method according to any of claims 11 to 14, wherein the method further comprising:

arranging a first stacked via at a metal layer corresponding to the drain terminal of the at least one pMOS type transistor;
arranging a second stacked via arranged at a metal layer corresponding to the drain terminal of the at least one nMOS type transistor; and
connecting the first stacked via or the second stacked via to the output terminal using a single metal layer.

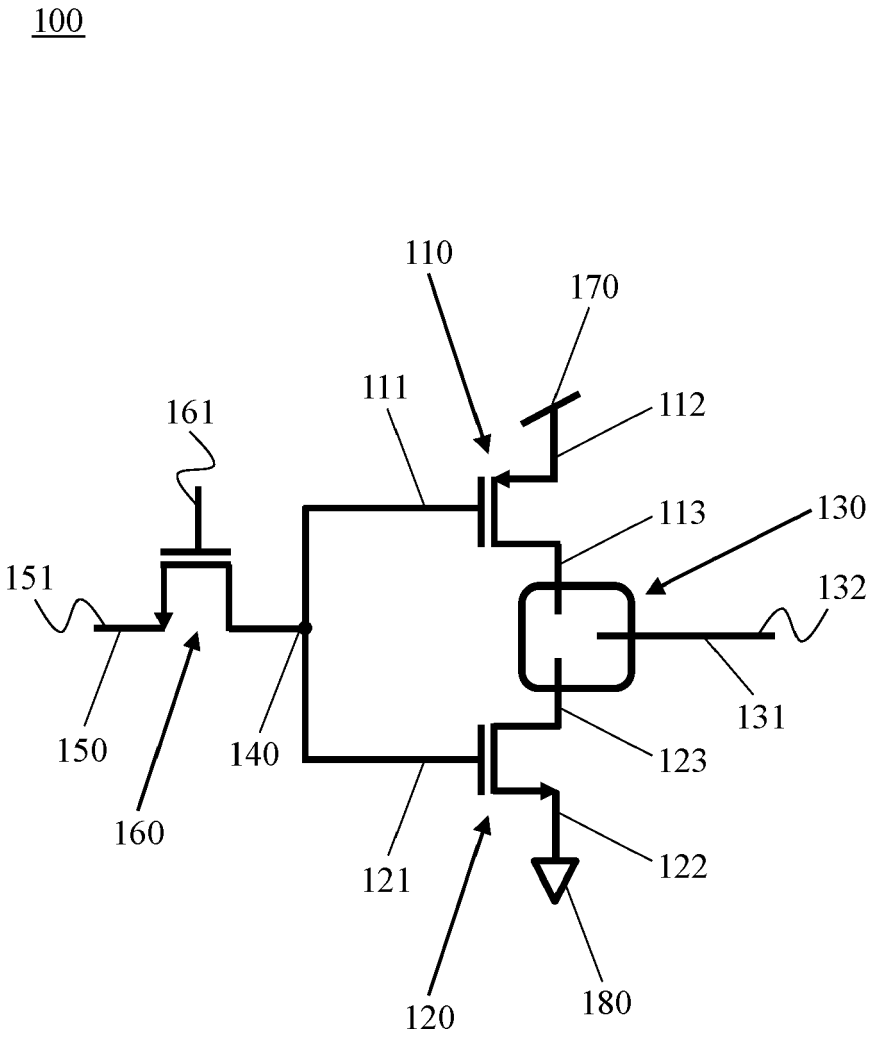
100
110
170
111
112
161
113
130
151
132
131
150
140
123
160
121
122
120
180

Fig. 1

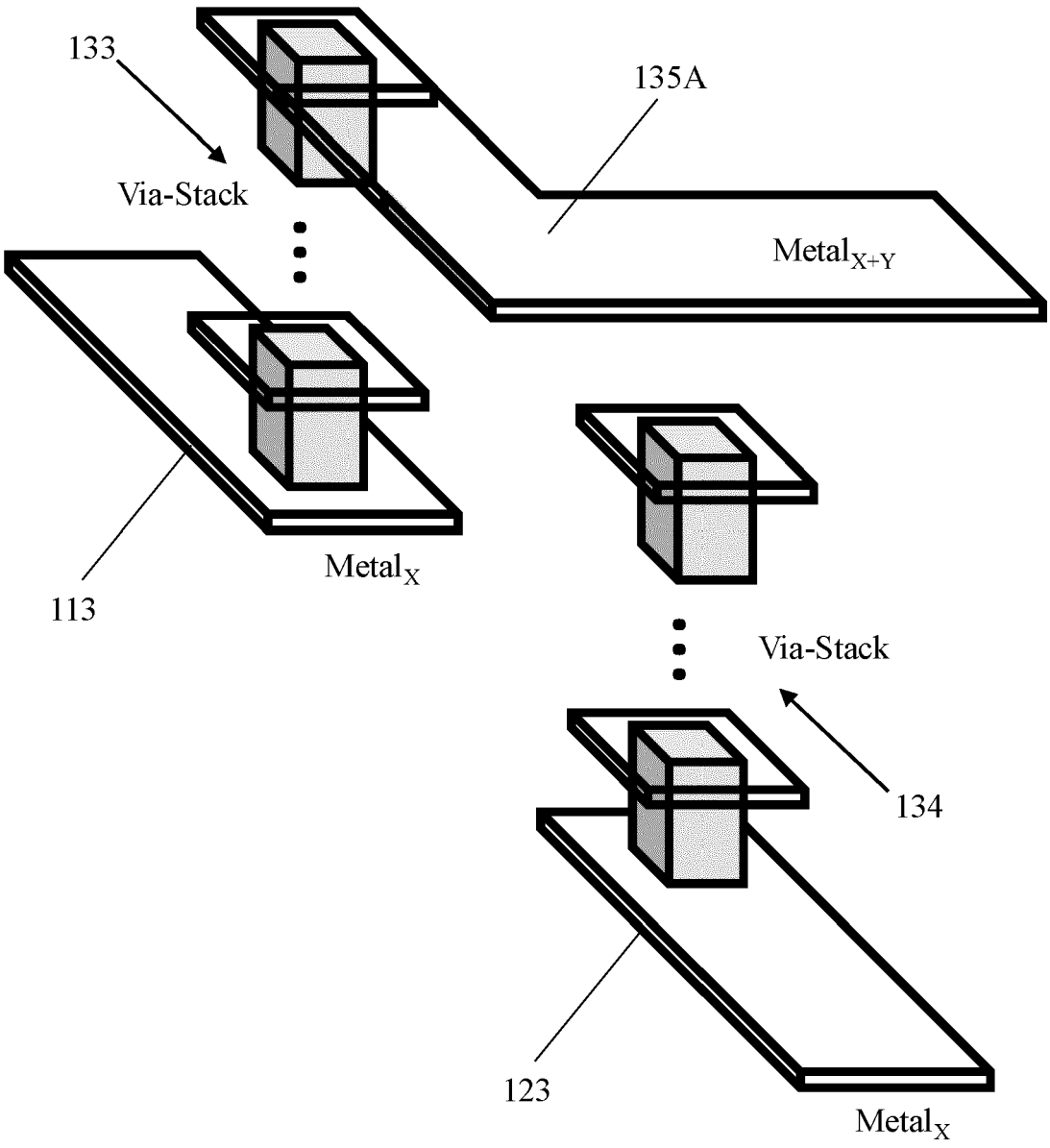
130A
133
Via-Stack
135A
Metal$_{X+Y}$
Metal$_X$
113
Via-Stack
134
123
Metal$_X$

Fig. 2A

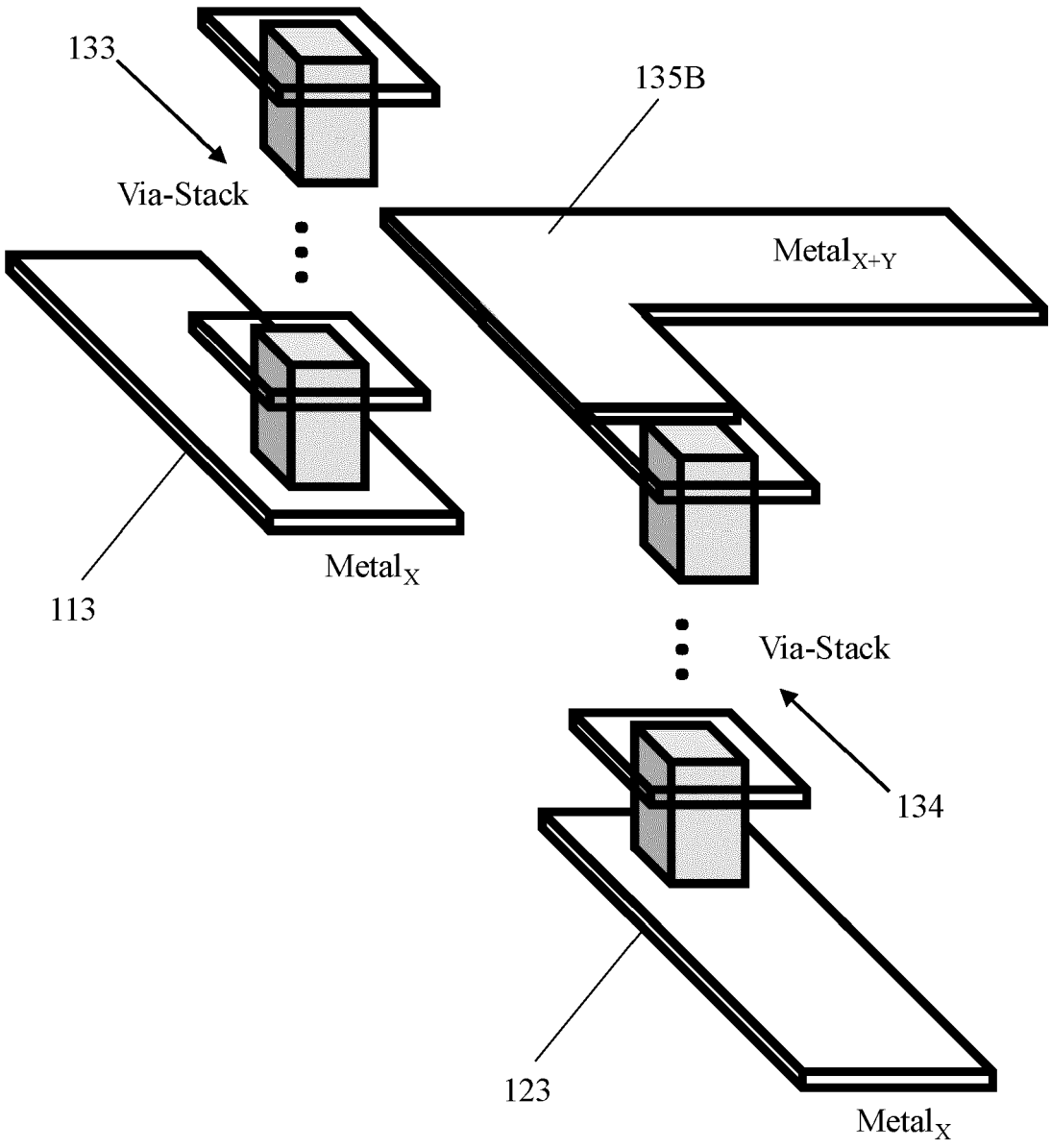
130B
133
Via-Stack
135B
Metal$_{X+Y}$
Metal$_X$
113
Via-Stack
134
123
Metal$_X$

Fig. 2B

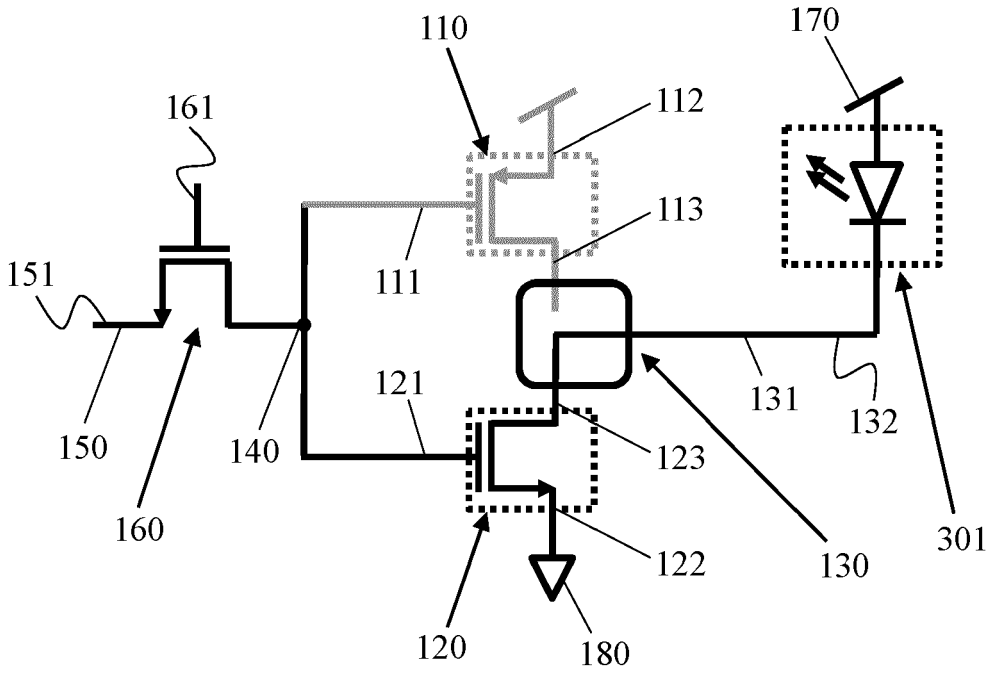
110
170
161
112
113
151
111
121
131
132
150
140
123
160
130
301
122
120
180

Fig. 3A

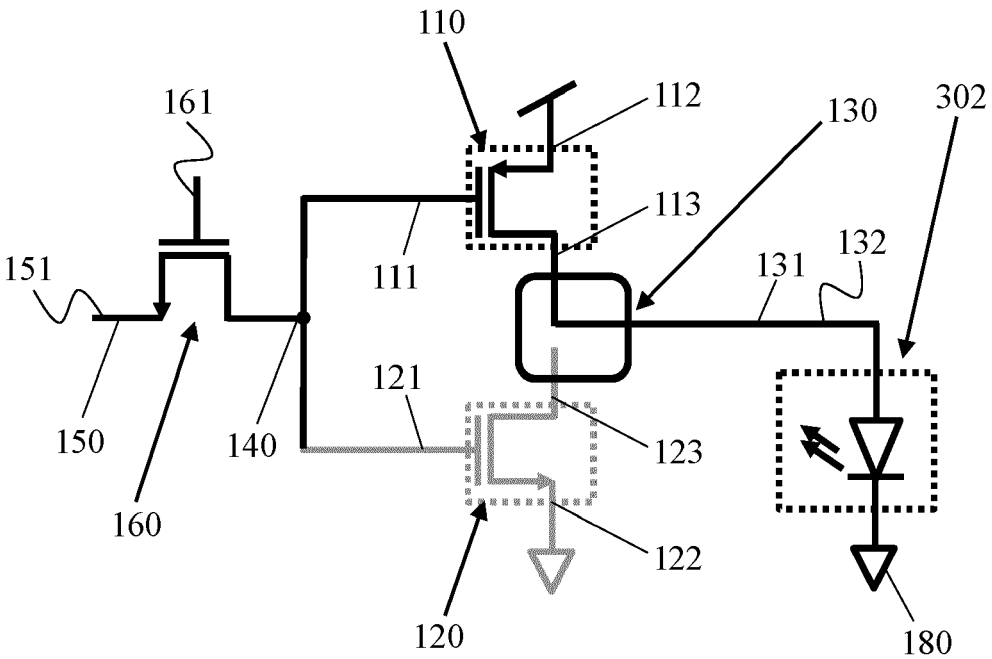
110
161
112
130
302
113
151
111
131
132
121
150
140
123
160
122
120
180

Fig. 3B

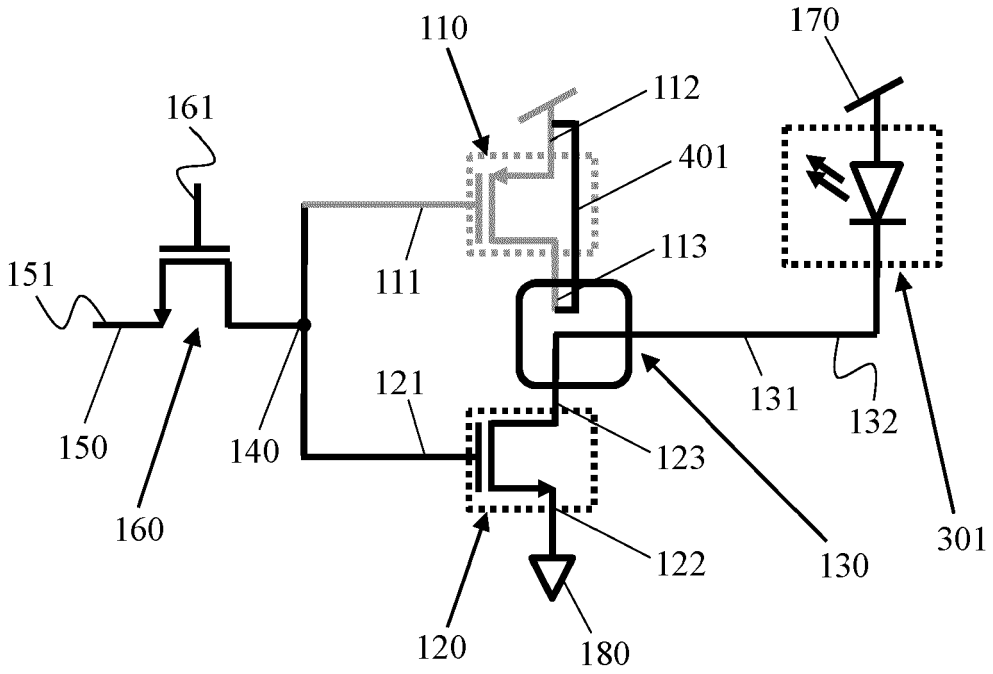
110
170
161
112
401
151
111
113
121
131
132
150
140
123
160
130
301
122
120
180

Fig. 4A

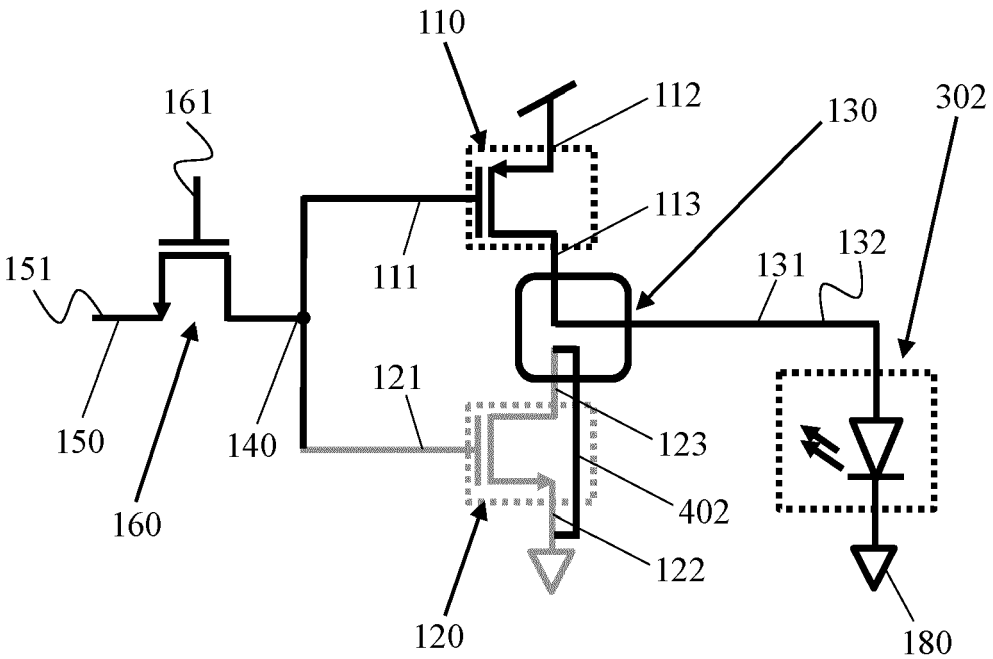
110
161
112
130
302
113
151
111
131
132
121
150
140
123
402
160
122
120
180

Fig. 4B

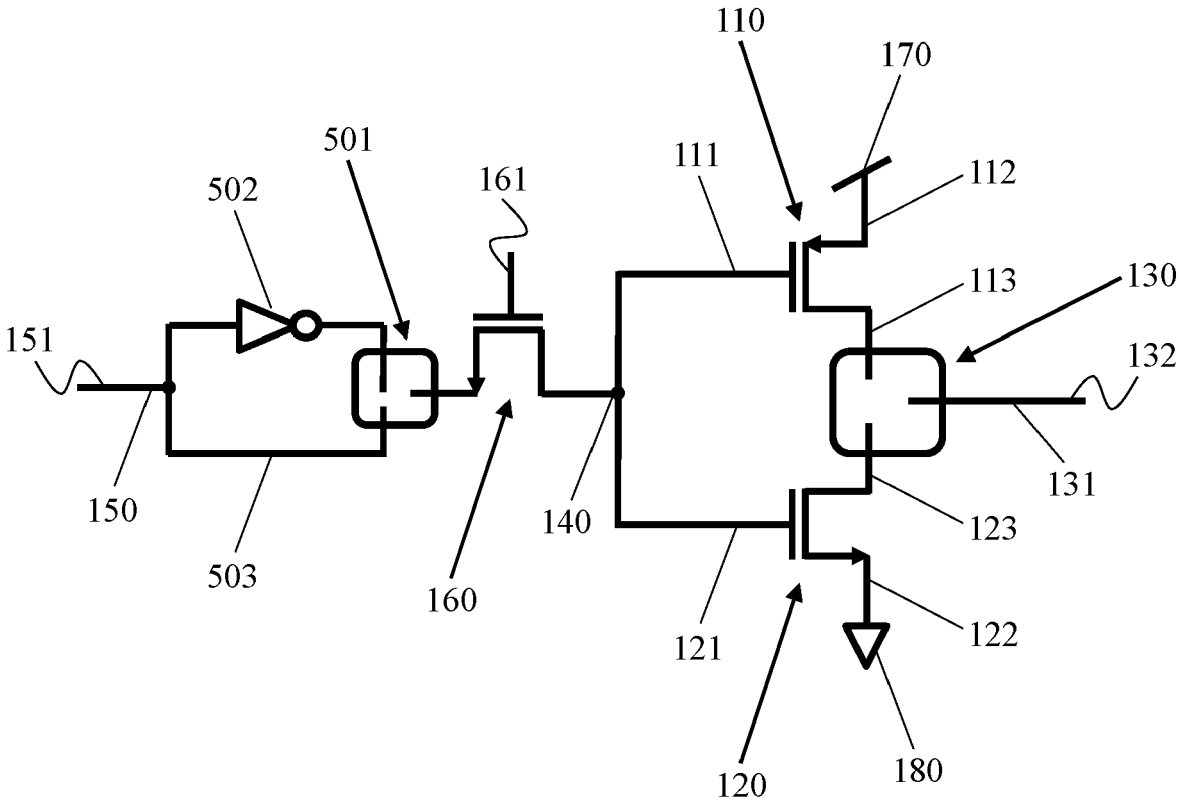
500
110
170
501
111
112
502
161
113
130
151
132
150
131
140
123
503
160
121
122
120
180

Fig. 5

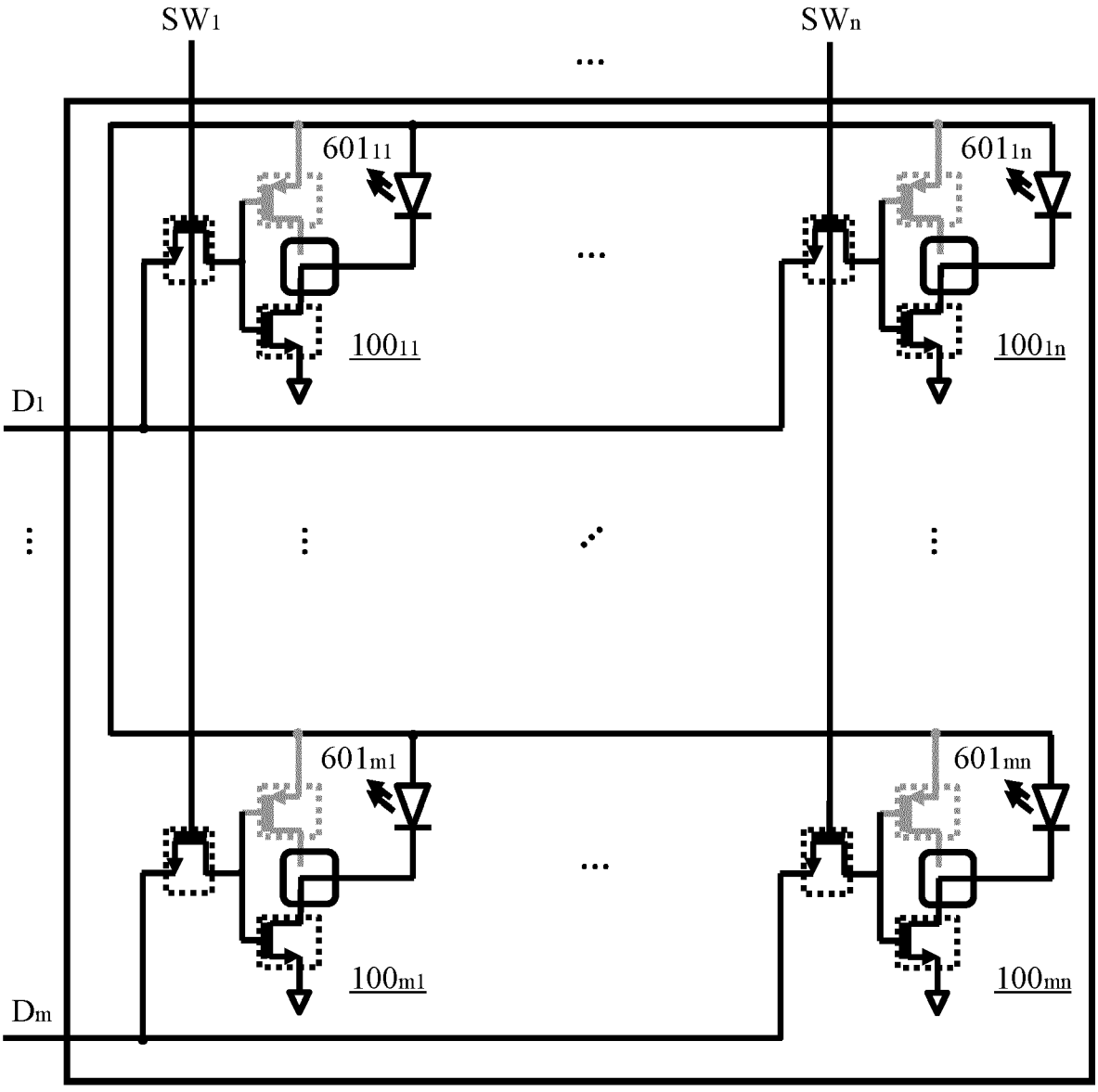
600A
SW1
SWn
601₁₁
601₁n
100₁₁
100₁n
D1
601m1
601mn
100m1
100mn
Dm

Fig. 6A

600B

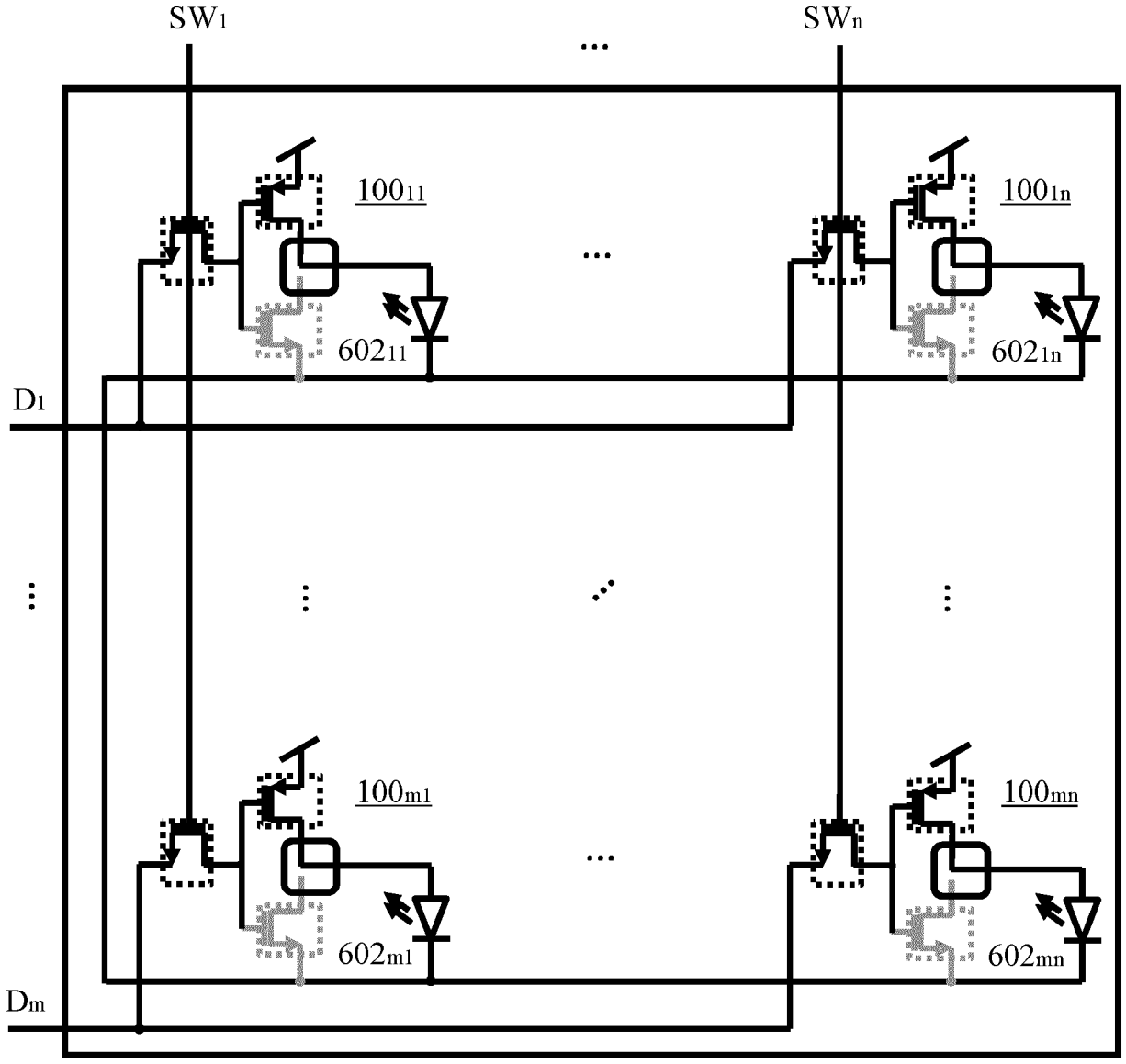
SW1
SWn
100₁₁
100₁n
602₁₁
602₁n
D1
100m1
100mn
602m1
602mn
Dm

Fig. 6B

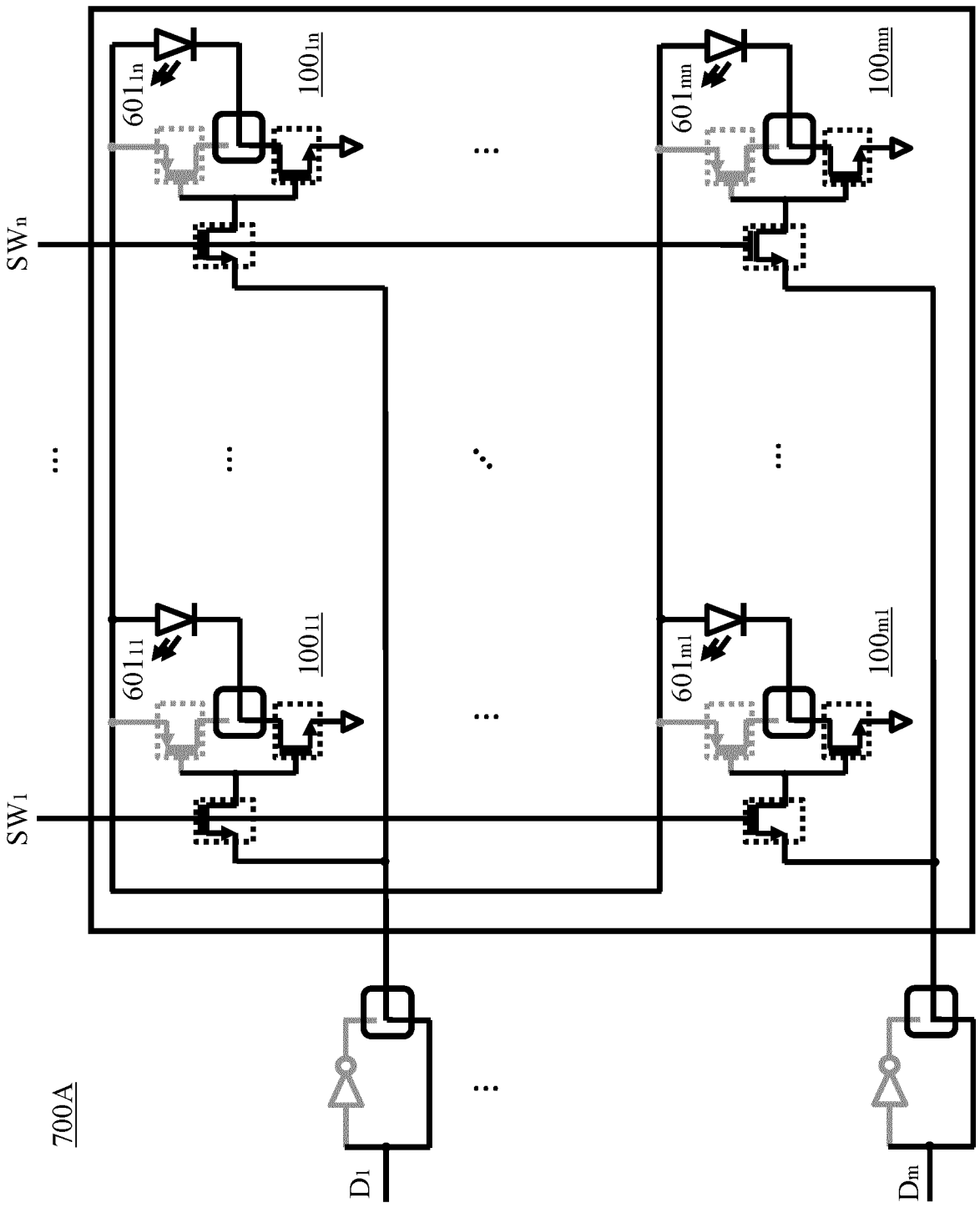
601ln
100ln
601mn
100mn
SWn
601l1
100l1
601m1
100m1
SW1
700A
D1
Dm

Fig. 7A

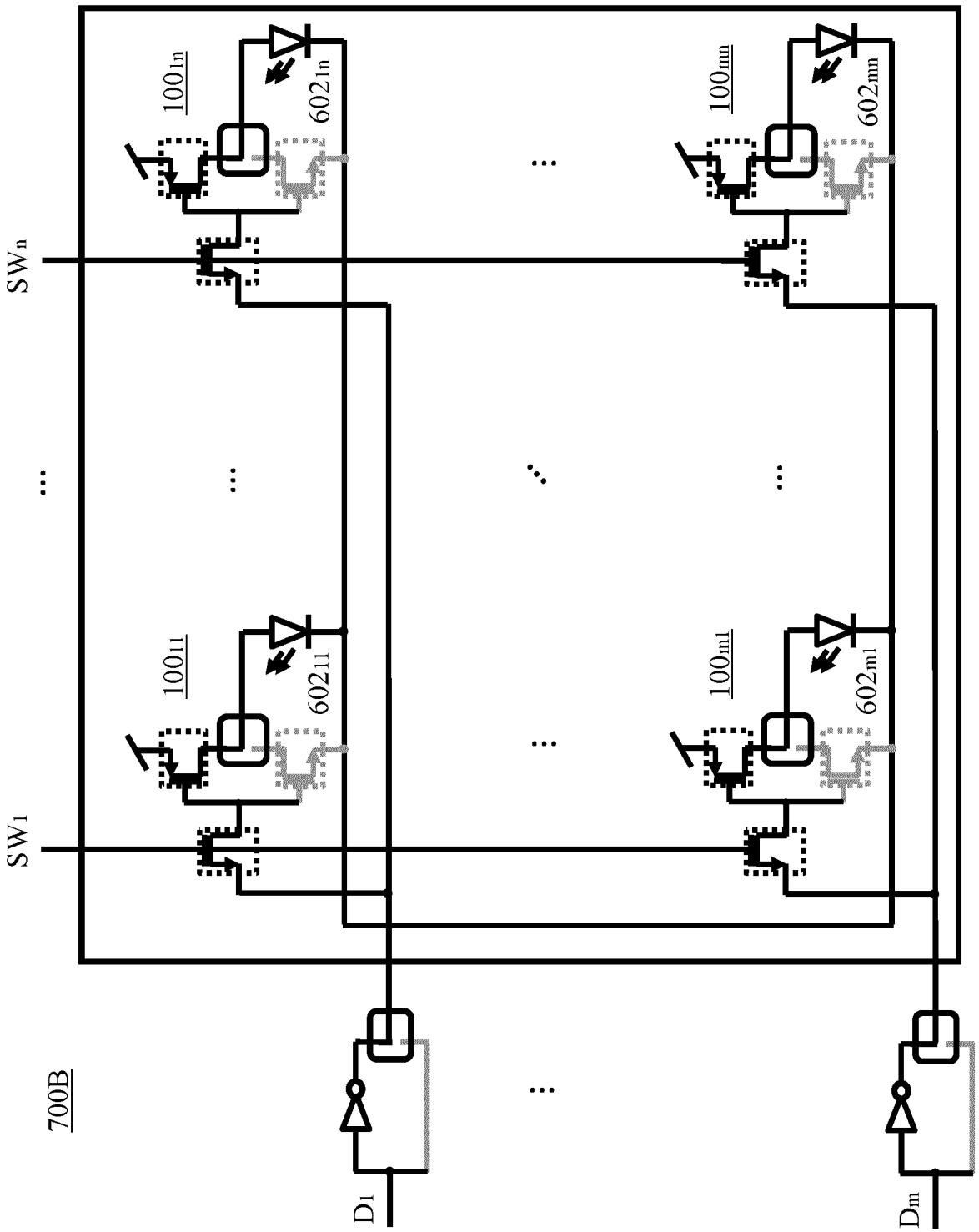
100_{1n}
602_{1n}
100_{mn}
602_{mn}
SW_n
100_{11}
602_{11}
100_{m1}
602_{m1}
SW_1
700B
D_1
D_m

Fig. 7B

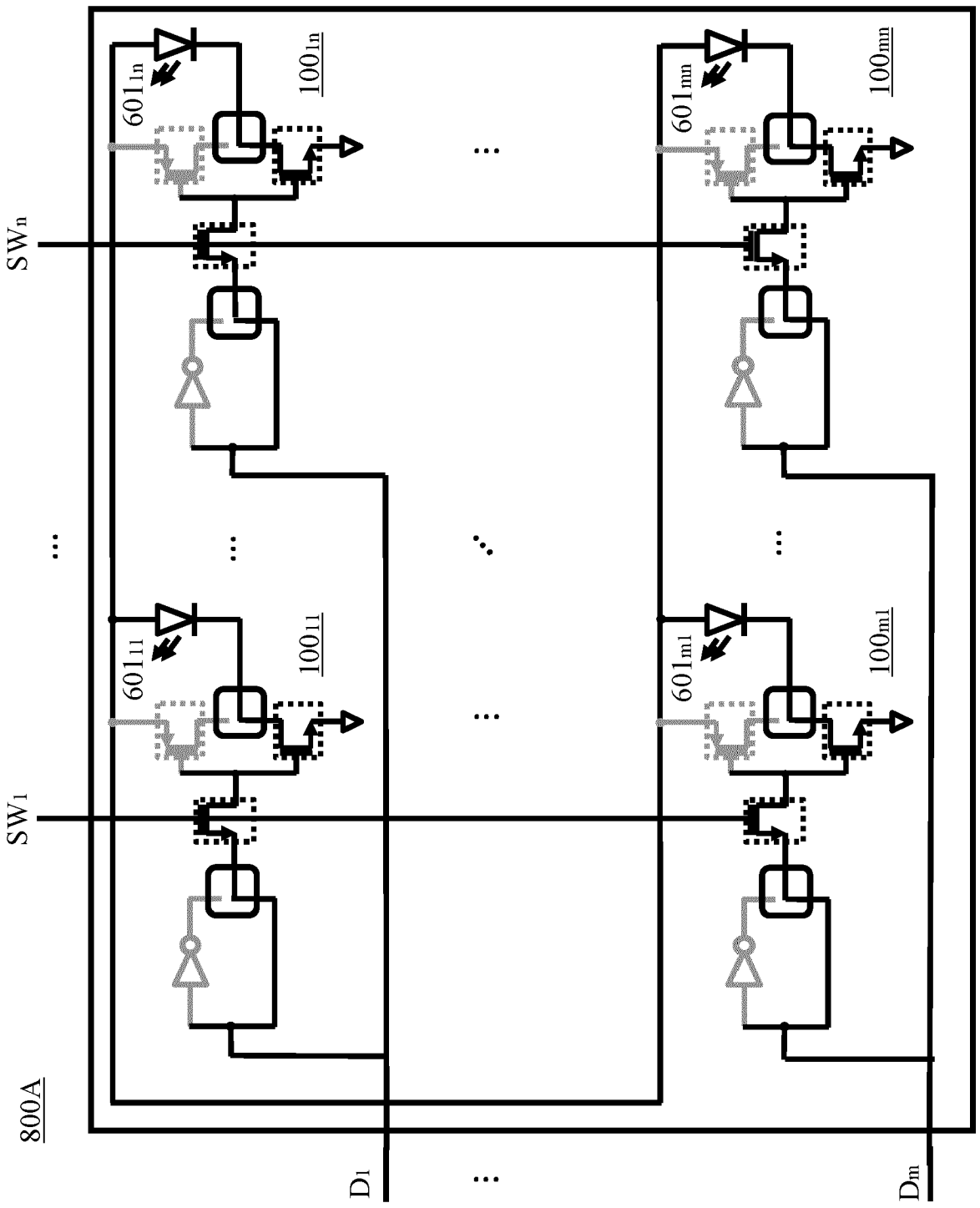
601ln
100ln
601mn
100mn
SWn
601l1
100l1
601m1
100m1
SW1
800A
D1
Dm

Fig. 8A

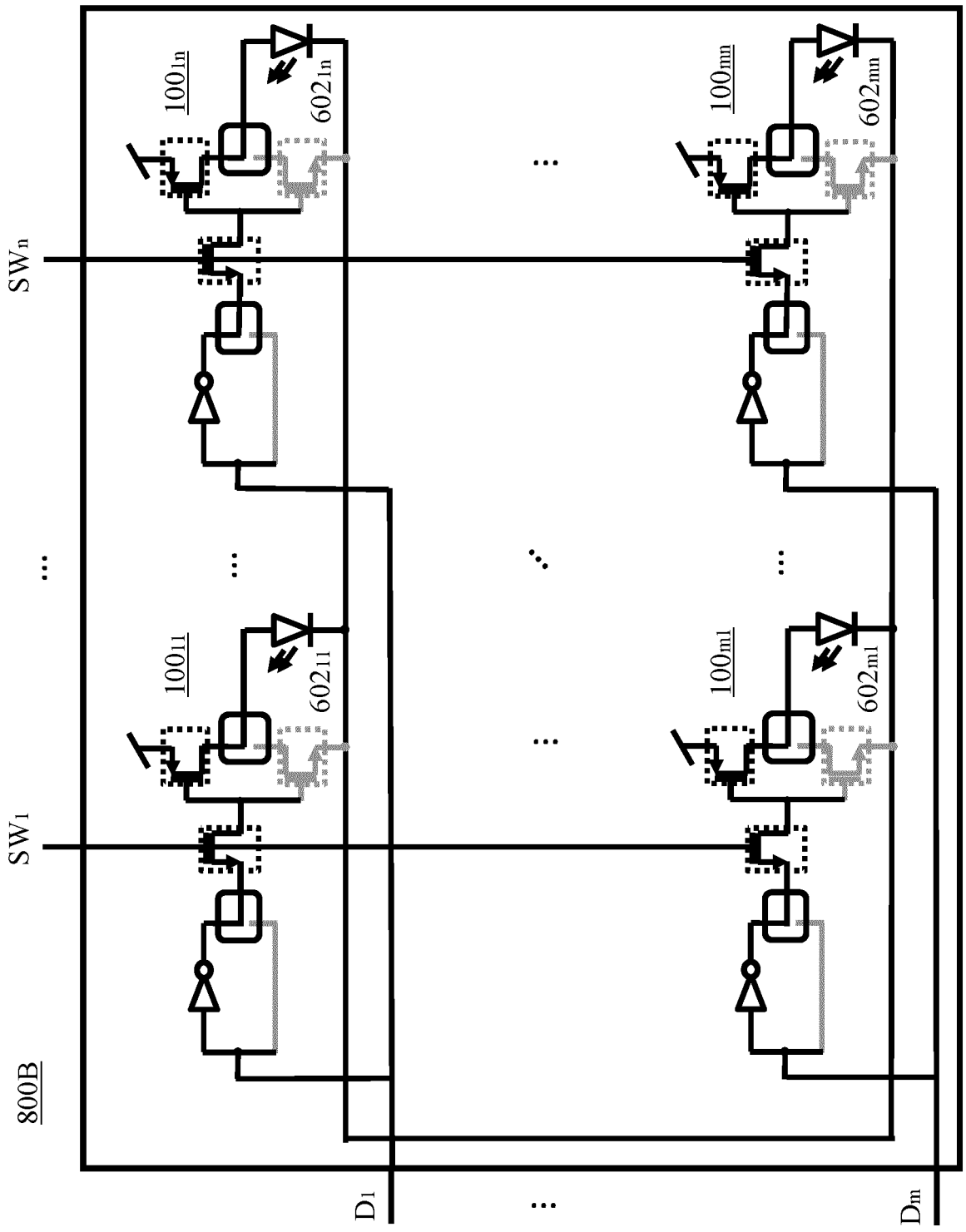
100ln
602ln
100mn
602mn
SWn
100l1
602l1
100ml
602ml
SW1
800B
D1
Dm

Fig. 8B

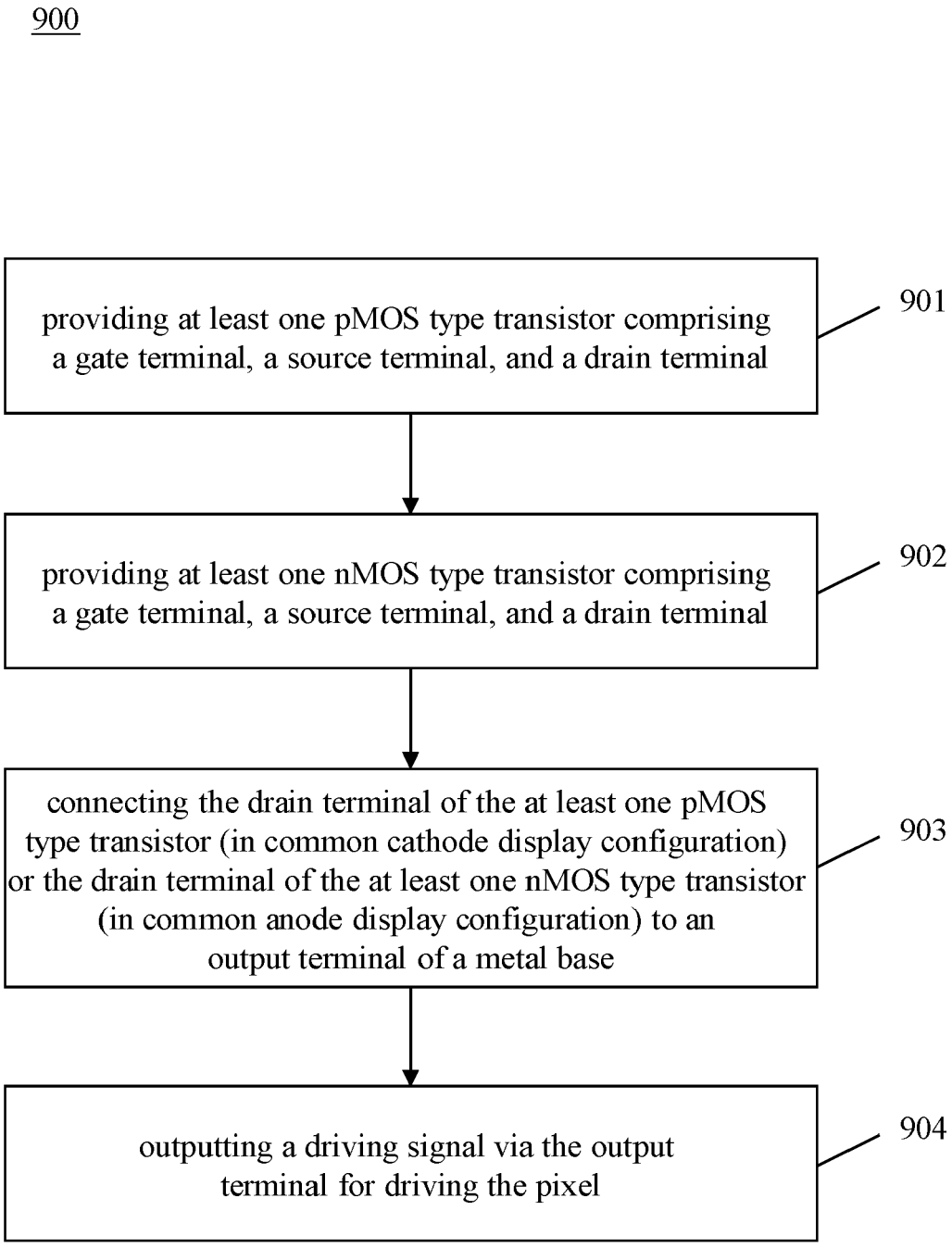
900
providing at least one pMOS type transistor comprising a gate terminal, a source terminal, and a drain terminal
901
providing at least one nMOS type transistor comprising a gate terminal, a source terminal, and a drain terminal
902
connecting the drain terminal of the at least one pMOS type transistor (in common cathode display configuration) or the drain terminal of the at least one nMOS type transistor (in common anode display configuration) to an output terminal of a metal base
903
outputting a driving signal via the output terminal for driving the pixel
904

Fig. 9

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EUROPEAN SEARCH REPORT

Application Number
EP 23 19 7615

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	11 March 2024	Harke, Michael

CATEGORY OF CITED DOCUMENTS

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EUROPEAN SEARCH REPORT

Application Number
EP 23 19 7615

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	11 March 2024	Harke, Michael

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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