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DESCRIPTION

Field

[0001] The present application relates to the field of microelectronic technology, and particularly to an enhancement mode switching device and a method for fabricating the enhancement mode switching device.

Background

[0002] Gallium nitride, which is semiconductor material, has become a hot topic of research due to its properties such as a wide band gap, a high electron saturated drift velocity, a high breakdown field strength and good thermal conductivity. Gallium nitride material, compared with silicon or gallium arsenide, is more suitable for fabricating high-temperature, high-frequency, high-voltage and high-power electronic devices. Therefore, the gallium nitride-based electronic device has good application prospects.

[0003] Because of strong two-dimensional electron gas in an AlGaN/GaN heterostructure, an AlGaN/GaN HEMT is usually a depletion mode device, and an enhancement mode device is difficult to be achieved. However, applications of the depletion device are limited in many situations; for example, an enhancement mode (normally-off) switching device is required as a power switching device. An enhancement mode gallium nitride switching device is mostly used in high-frequency devices, power switching devices and digital circuits, etc. Therefore, research on the enhancement mode gallium nitride switching device has great significance.

[0004] To achieve an enhancement mode gallium nitride switching device, an appropriate method is required to reduce channel carrier concentration under the gate region at zero gate bias, and the methods currently reported include recessing in the gate region, injecting fluorine ions into the barrier layer under the gate, and adopting a thin barrier layer, etc.

[0005] Recessing in the gate region is achieved by making slight changes in a structure of a conventional depletion mode AlGaN/GaN HEMT device. A E-beam gate is not directly formed but etching in a pre-deposited gate region is done first and then a Schottky gate is formed in the recessed gate window, where the electron density of electron gas in a channel is reduced by thinning down the barrier layer thickness. To pinch off the channel at zero gate voltage, the thickness of the barrier layer is reduced to less than 5 nm, and in this case, no effective quantum confinement is generated at a positive gate voltage and surface traps are formed, which causes the channel not to be completely opened at a positive gate voltage. In addition, gate leakage current is increased due to electrons in the surface traps. The method of a recessed gate is proposed in 2001 by Kumar et al. in University of Illinois in the United States, referring to Kumar, V., et al., "Recessed 0.25 mm gate AlGaN/GaN HEMTs on SiC with high

gate-drain breakdown voltage using ICP-RIE", Electron. Lett.2001, 37, pp.1483-1485.

[0006] In case of fluorine implantation, negatively charged ions, such as fluorine ions, are injected into a barrier layer and the two-dimensional electron gas in the conductive channel can be depleted by controlling the dose of the injected ions. A high dose of anions is required to pinch-off the channel. Therefore, a current when the channel is opened is reduced. Y. Cai et al. at Hong Kong University of Science and Technology successfully developed a high performance enhancement mode AlGaN/GaN HEMT in 2005 by using fluoride-based plasma treatment technology, referring to Y. Cai et al., "High-performance enhancement-mode AlGaN/GaN HEMTs using fluoride-based plasma treatment", IEEE Electron Lett., vol.2, no.7, pp.435-437, 2005.

[0007] In case of a thin barrier layer, the electron density of two-dimensional electron gas in a channel is reduced by adapting a thin AlGaN barrier layer. Akira ENDOH et al. at Osaka University in Japan prepare an enhancement-mode device using this method, with a threshold voltage of the prepared enhancement-mode device being zero, referring to Akira ENDOH_et al., "Non-Recessed-Gate Enhancement-Mode AlGaN/GaN High Electron Mobility Transistors with High RF Performance", JJAP, Vol.43, No.4B, 2004, pp.2255-2258.

[0008] The methods introduced above all belong to technology of a Schottky gate field-effect transistor and the threshold voltage is generally about 0V-1V, which does not reach the threshold voltage of 3V-5V for application. and the gate leakage current of the Schottcky gate technology is much larger than that of a metal insulator semiconductor field-effect transistor. In addition, plasma treatment is used in both of the method for recessing in the gate region and the method for injecting fluorine ions into a barrier layer under a gate region. However, the plasma treatment will destroy a lattice structure and damage an active region of a device, and repetitive control of the process is poor, therefore, stability and reliability of the device are affected.

[0009] Reference US2010155720 A1 discloses a heterojunction field-effect semiconductor device which has a main semiconductor region comprising two layers of dissimilar materials such that a two-dimensional electron gas layer is generated along the heterojunction between the two layers. A source and a drain electrode are placed in spaced positions on a major surface of the main semiconductor region and electrically coupled to the 2DEG layer. Between these electrodes, a gate electrode is received in a recess in the major surface of the main semiconductor region via a p-type metal oxide semiconductor film and insulating film, whereby a depletion zone is normally created in the 2DEG layer, making the device normally off. The p-type metal oxide semiconductor film of high hole concentration serves for the normally-off performance of the device with low gate leak current, and the insulating film for further reduction of gate leak current.

[0010] Reference EP2385544 (A2) discloses the formation of enhancement-mode (e-mode) gate injection high electron mobility transistors (HEMT). Embodiments can include GaN, AlGaN, and InAlN based HEMTs. Embodiments also can include self-aligned P-type gate and

field plate structures. The gates can be self-aligned to the source and drain, which can allow for precise control over the gate-source and gate-drain spacing. Additional embodiments include the addition of a GaN cap structure, an AlGaN buffer layer, AlN, recess etching, and/or using a thin oxidized AlN layer. In manufacturing the HEMTs according to present teachings, selective epitaxial growth (SEG) and epitaxial lateral overgrowth (ELO) can both be utilized to form gates.

Summary

[0011] The application is to provide a method for fabricating an enhancement mode switching device. By forming a dielectric layer on a nitride transistor structure, forming a groove structure by locally thinning a gate region of the dielectric layer, and arranging p-type semiconductor material in the groove in the gate region, an n-type conductive layer below the gate is pinched off.

[0012] To achieve the above purpose, an enhancement mode switching device is provided according to claim 1.

[0013] Preferably, in the above enhancement mode switching device, the nitride transistor structure includes:

a nitride nucleation layer located on the substrate;

a nitride buffer layer located on the nitride nucleation layer; and

a nitride channel layer located on the nitride buffer layer.

[0014] Preferably, in the above enhancement mode switching device, the nitride channel layer is non-doped or n-type doped.

[0015] Preferably, in the above enhancement mode switching device, the nitride transistor structure further includes a nitride barrier layer arranged on the nitride channel layer.

[0016] Preferably, in the above enhancement mode switching device, the nitride transistor structure further includes a nitride cap layer formed on the nitride barrier layer.

[0017] Preferably, in the above enhancement mode switching device, nitride in the nitride cap is gallium nitride or aluminum gallium nitride.

[0018] Preferably, in the above enhancement mode switching device, the p-type semiconductor material is selected from p-type diamond, p-type NiO, p-type GaN or p-type polycrystalline GaN.

[0019] Preferably, in the above enhancement mode switching device, the enhancement mode switching device further includes a conductive metal layer formed on the p-type semiconductor material.

[0020] A method for fabricating an enhancement mode switching device is further disclosed in this application, the method being defined in claim 9.

[0021] Preferably, the above method for fabricating the enhancement mode switching device further includes forming a conductive metal layer on the p-type semiconductor material after forming the p-type semiconductor material in the groove.

[0022] Preferably, in the above method for fabricating the enhancement mode switching device, the step of forming the nitride transistor includes:

forming a nitride nucleation layer on the substrate;

forming a nitride buffer layer on the nitride nucleation layer; and

forming a nitride channel layer on the nitride buffer layer, where the nitride channel layer is non-doped or n-type doped; and

forming a nitride barrier layer on the nitride channel layer.

[0023] Preferably, the above method for fabricating the enhancement mode switching device further includes forming a nitride cap layer on the nitride barrier layer, where nitride in the nitride cap is gallium nitride or aluminum gallium nitride.

[0024] Preferably, the above method for fabricating the enhancement mode switching device further includes performing oxidation treatment on the dielectric layer before forming p-type semiconductor material in the groove.

[0025] Compared with the conventional technology, an n-type conductive layer below the gate is pinched off by forming a dielectric layer on a nitride transistor structure, forming a groove structure in a gate region of the dielectric layer and arranging p-type semiconductor material in the groove in the application. Therefore, a gallium nitride enhancement mode switching device is achieved with a simple process, and the fabricated device is stable and reliable. Conductivity can be increased by forming a conductive metal layer on the p-type semiconductor material.

Brief Description of the Drawings

[0026] For clarity of description of solutions in embodiments of the application or conventional solutions, drawings for description of the embodiments and the conventional technology are

briefly described below. Obviously, the drawings described below are merely a few embodiments of the application. Other drawings may be obtained by those skilled in the art according to these drawings without paying any creative work.

Figure 1a - Figure 1e are cross sections illustrating an enhancement mode switching device and a series of processes of a method for fabricating the same according to a first embodiment of the application.

Figure 2a - Figure 2g are cross sections illustrating an enhancement mode switching device and a series of processes of a method for fabricating the same according to a second embodiment of the application.

Figure 3a - Figure 3e are cross sections illustrating an enhancement mode switching device and a series of processes of a method for fabricating the same according to a third embodiment of the application.

Figure 4a - Figure 4f are cross sections illustrating an enhancement mode switching device and a series of processes of a method for fabricating the same according to a fourth embodiment of the application.

Figure 5a - Figure 5f are cross sections illustrating an enhancement mode switching device and a series of processes of a method for fabricating the same according to a fifth embodiment of the application.

Figure 6a - Figure 6f are cross sections illustrating an enhancement mode switching device and a series of processes of a method for fabricating the same according to a sixth embodiment of the application.

Figure 7a - Figure 7f are cross sections illustrating an enhancement mode switching device and a series of processes of a method for fabricating the same according to a seventh embodiment of the application.

Figure 8a - Figure 8e are cross sections illustrating an enhancement mode switching device and a series of processes of a method for fabricating the same according to an eighth embodiment of the application.

Figure 9a - Figure 9f are cross sections illustrating an enhancement mode switching device and a series of processes of a method for fabricating the same according to a ninth embodiment of the application.

Figure 10a - Figure 10e are cross sections illustrating an enhancement mode switching device and a series of processes of a method for fabricating the same according to a tenth embodiment of the application.

Figure 11a - Figure 11g are cross sections illustrating an enhancement mode switching device and a series of processes of a method for fabricating the same according to an eleventh embodiment of the application.

[0027] Only the first and third to tenth embodiments are hereby covered by the claims.

Detailed Description

[0028] The application is described below in detail with the embodiments shown in the drawings. However, the embodiments are not to limit the application. Modifications in structure, manner or function made by those skilled in the art according to the embodiments are within the protection scope of the application.

[0029] In addition, a same numeral or sign may be used in different embodiments. The reuse is merely for simplicity and clarity of description of the application, but indicates no relevancy among the various embodiments and/or structures.

[0030] Referring to Figure 1e, in a first embodiment of the application, an enhancement mode switching device includes: a substrate 1, and a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4, a nitride barrier layer 5 and a silicon nitride layer 6 which are formed on the substrate 1 in sequence. A groove H1 is arranged in a gate region of the silicon nitride layer 6 (referring to Figure 1b). A height of the groove H1 is less than a thickness of the silicon nitride layer 6. P-type semiconductor material 9 is formed on an inner wall of the groove H1 and on the gate region. A source electrode 10 and a drain electrode 11 are arranged at two sides of the gate region, respectively. Each of the source electrode 10 and the drain electrode 11 is through the silicon nitride layer 6 in a vertical direction, and contacts with the nitride barrier layer 5.

[0031] Figure 1a - Figure 1e are cross sections illustrating the enhancement mode switching device and a series of processes of a method for fabricating the same according to the first embodiment of the application.

[0032] Referring to Figure 1a, a substrate 1 is provided at first. The substrate 1 may be selected from semiconductor material, ceramic material or macromolecular material, etc. In this embodiment, the substrate 1 is preferably selected from sapphire, silicon carbide, silicon, lithium niobate, silicon-on-insulator substrate (SOI), gallium nitride or aluminum nitride.

[0033] A nitride transistor structure is then prepared on the substrate 1. The nitride here is preferably AlInGaN. Specifically, a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4 and a nitride barrier layer 5 are grown on the substrate 1 in sequence. Here, material of the nitride nucleation layer 2, the nitride buffer layer 3, the nitride channel layer 4 and the nitride barrier layer 5 may be any Group III nitride or any combination of Group III nitrides. In the embodiment, the nitride nucleation layer 2 may be, for example, AlInGaN. The nitride buffer layer 3 may be, for example, AlGaN. The nitride channel layer 4 may be, for example, GaN. The nitride barrier layer 5 may be, for example, AlGaN. In other embodiments,

the nitride barrier layer 5 may not be arranged, and in this case, the nitride channel layer 4 is non-doped or n-doped.

[0034] A dielectric layer is then grown on the accomplished nitride transistor structure. A gate region is defined on the dielectric layer. Specifically, a silicon nitride layer 6 is grown on the accomplished nitride transistor structure. In the embodiment, the dielectric layer may be grown in situ or may be grown by Atomic Layer Deposition (ALD), Chemical Vapor Deposition (CVD), Molecular Beam Epitaxy (MBE), Plasma Enhanced Chemical Vapor Deposition (PECVD) or Low Pressure Chemical Vapor Deposition (LPCVD), or a combination thereof. It should be understood that the methods for forming the dielectric layer described herein are merely for illustration. In the application, the dielectric layer may be formed by any method known to those skilled in the art. The dielectric layer includes a silicon nitride layer, and/or a silicon dioxide layer, and/or an aluminum silicon nitride layer, and/or an aluminum oxide layer, and/or an aluminum oxynitride layer, and/or hafnium oxide, and/or silicon oxynitride, and/or hafnium aluminum oxide.

[0035] Referring to Figure 1b, a groove H1 partially through the dielectric layer is formed by etching a gate region of the dielectric layer. Here the partially through indicates that the bottom of the groove is located within the dielectric layer. In the embodiment, the etching may be fluorine-based plasma etching, for example.

[0036] Referring to Figure 1c, p-type semiconductor material 9 is deposited in the groove H1 formed by etching. The p-type semiconductor material 9 may be selected from p-type diamond, p-type NiO, p-type GaN or p-type polycrystalline GaN.

[0037] Referring to Figure 1d, the p-type semiconductor material 9 on the dielectric layer except for the gate region is removed. In the embodiment, for example, the p-type semiconductor material 9 is p-type diamond, then the p-type diamond in the gate region is retained, and the p-type diamond in other region may be etched away with plasma. In this case, the p-type semiconductor material 9 is actually the gate of the enhancement mode switching device in the application. Conductivity of the gate can be improved with an additional conductive metal layer.

[0038] Referring to Figure 1e, the nitride transistor structure is exposed by etching the dielectric layer except for the gate region. In the embodiment, the nitride barrier layer 5 may be exposed, for example, by dry etching, or the nitride barrier layer 5 may even be etched through, to form two ohmic contact regions. Finally, a source electrode 10 is formed on one ohmic contact region, and a drain electrode 11 is formed on the other ohmic contact region.

[0039] Referring to Figure 2g, in a second embodiment of the application, an enhancement mode switching device includes: a substrate 1, and a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4, a nitride barrier layer 5 and a silicon nitride layer 6 which are formed on the substrate 1 in sequence. A groove H2 is arranged in a gate region of the silicon nitride layer 6 (referring to Figure 2c). An additional dielectric layer 14 is formed on an inner

wall of the groove H2 and on the silicon nitride layer 6. P-type semiconductor material 9 is formed on a gate region of the additional dielectric layer 14. A source electrode 10 and a drain electrode 11 are arranged at two sides of the gate region, respectively. Each of the source electrode 10 and the drain electrode 11 is through the additional dielectric layer 14 and the silicon nitride layer 6 in a vertical direction, and contacts with the nitride barrier layer 5.

[0040] Figure 2a - Figure 2g are cross sections illustrating the enhancement mode switching device and a series of processes of a method for fabricating the same according to the second embodiment of the application.

[0041] Referring to Figure 2a, a substrate 1 is provided at first. The substrate 1 may be selected from semiconductor material, ceramic material or macromolecular material, etc. In this embodiment, the substrate 1 is preferably selected from sapphire, silicon carbide, silicon, lithium niobate, silicon-on-insulator substrate (SOI), gallium nitride or aluminum nitride.

[0042] A nitride transistor structure is then prepared on the substrate 1. The nitride here is preferably AlInGaN. Specifically, a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4 and a nitride barrier layer 5 are grown on the substrate 1 in sequence. Here, material of the nitride nucleation layer 2, the nitride buffer layer 3, the nitride channel layer 4 and the nitride barrier layer 5 may be any Group III nitride or any combination of Group III nitrides. In the embodiment, the nitride nucleation layer 2 may be, for example, AlInGaN. The nitride buffer layer 3 may be, for example, AlGaN. The nitride channel layer 4 may be, for example, GaN. The nitride barrier layer 5 may be, for example, AlGaN. In other embodiments, the nitride barrier layer 5 may not be arranged, and in this case, the nitride channel layer 4 is non-doped or n-doped.

[0043] A dielectric layer is then grown on the accomplished nitride transistor structure. A gate region is defined on the dielectric layer. Specifically, a silicon nitride layer 6 is grown on the accomplished nitride transistor structure. In the embodiment, the dielectric layer may be grown in situ or may be grown by Atomic Layer Deposition (ALD), Chemical Vapor Deposition (CVD), Molecular Beam Epitaxy (MBE), Plasma Enhanced Chemical Vapor Deposition (PECVD) or Low Pressure Chemical Vapor Deposition (LPCVD), or a combination thereof. It should be understood that the methods for forming the dielectric layer described herein are merely for illustration. In the application, the dielectric layer may be formed by any method known to those skilled in the art. In other embodiments, the dielectric layer may also include a silicon nitride layer, and/or a silicon dioxide layer, and/or an aluminum nitride layer, and/or an aluminum silicon nitride layer, and/or an aluminum oxide layer, and/or an aluminum oxynitride layer, and/or hafnium oxide, and/or silicon oxynitride, and/or hafnium aluminum oxide.

[0044] Referring to Figure 2b - Figure 2c, a groove H2 at least partially through the dielectric layer is formed by etching the gate region of the dielectric layer. Referring to Figure 2d, an additional dielectric layer 14 is deposited in the groove H2 formed by etching. Material of the additional dielectric layer 14 may include, for example, Al_2O_3 or AlON. The additional dielectric layer 14 may be grown by Atomic Layer Deposition, Chemical Vapor Deposition, Molecular

Beam Epitaxy, Plasma Enhanced Chemical Vapor Deposition or Low Pressure Chemical Vapor Deposition, or a combination thereof. It should be understood that the methods for forming the additional dielectric layer described herein are merely for illustration. In the application, the additional dielectric layer may be formed by any method known to those skilled in the art. Material of the additional dielectric layer may also be selected from one or any combination of SiN, SiON, SiO_2 and HfO_2.

[0045] Referring to Figure 2e, p-type semiconductor material 9 is deposited on the additional dielectric layer 14 in the groove H2 formed by etching. The p-type semiconductor material 9 may be selected from p-type diamond, p-type NiO, p-type GaN or p-type polycrystalline GaN, for example.

[0046] Referring to Figure 2f, the p-type semiconductor material 9 on the additional dielectric layer 14 except for the gate region is removed. In the embodiment, for example, the p-type semiconductor material 9 is p-type diamond, then the p-type diamond in the gate region is retained, and the p-type diamond in other region may be etched away with plasma. In this case, the p-type semiconductor material 9 is actually the gate of the enhancement mode switching device in the application. Conductivity of the gate can be improved with an additional metal layer.

[0047] Referring to Figure 2g, the nitride transistor structure is exposed by etching the dielectric layer except for the gate region. In the embodiment, the nitride barrier layer 5 may be exposed, for example, by dry etching, or the nitride barrier layer 5 may even be etched through, to form two ohmic contact regions. Finally, a source electrode 10 is formed on one ohmic contact region, and a drain electrode 11 is formed on the other ohmic contact region.

[0048] Referring to Figure 3e, in a third embodiment of the application, an enhancement mode switching device includes: a substrate 1, and a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4, a nitride barrier layer 5, a silicon nitride layer 6, an aluminum nitride layer 7 and a silicon nitride layer 8 which are formed on the substrate 1 in sequence. A groove H3 is arranged in a gate region of the silicon nitride layer 8 (referring to Figure 3b). A height of the groove H3 is equal to a thickness of the silicon nitride layer 8. P-type semiconductor material 9 is formed on an inner wall of the groove H3 and on the gate region. A source electrode 10 and a drain electrode 11 are arranged at two sides of the gate region, respectively. Each of the source electrode 10 and the drain electrode 11 is through the silicon nitride layer 8, the aluminum nitride layer 7 and the silicon nitride layer 6 in a vertical direction, and contacts with the nitride barrier layer 5.

[0049] Figure 3a - Figure 3e are cross sections illustrating the enhancement mode switching device and a series of processes of a method for fabricating the same according to the third embodiment of the application.

[0050] Referring to Figure 3a, a substrate 1 is provided at first. The substrate 1 may be selected from semiconductor material, ceramic material or macromolecular material, etc. In

this embodiment, the substrate 1 is preferably selected from sapphire, silicon carbide, silicon, lithium niobate, silicon-on-insulator substrate (SOI), gallium nitride or aluminum nitride.

[0051] A nitride transistor structure is then prepared on the substrate 1. The nitride here is preferably AlInGaN. Specifically, a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4 and a nitride barrier layer 5 are grown on the substrate 1 in sequence. Here, material of the nitride nucleation layer 2, the nitride buffer layer 3, the nitride channel layer 4 and the nitride barrier layer 5 may be any Group III nitride or any combination of Group III nitrides. In the embodiment, the nitride nucleation layer 2 may be AlInGaN. The nitride buffer layer 3 may be, for example, AlGaN. The nitride channel layer 4 may be, for example, GaN. The nitride barrier layer 5 may be, for example, AlGaN. In other embodiments, the nitride barrier layer 5 may not be arranged, and in this case, the nitride channel layer 4 is non-doped or n-doped.

[0052] A dielectric layer is then grown on the accomplished nitride transistor structure. A gate region is defined on the dielectric layer. Specifically, a silicon nitride layer 6, an aluminum nitride layer 7 and a silicon nitride layer 8 are grown on the accomplished nitride transistor structure in sequence. In the embodiment, the dielectric layer may be grown in situ or may be grown by Atomic Layer Deposition (ALD), Chemical Vapor Deposition (CVD), Molecular Beam Epitaxy (MBE), Plasma Enhanced Chemical Vapor Deposition (PECVD) or Low Pressure Chemical Vapor Deposition (LPCVD), or a combination thereof. It should be understood that the methods for forming the dielectric layer described herein are merely for illustration. In the application, the dielectric layer may be formed by any method known to those skilled in the art. The dielectric layer includes a silicon nitride layer, and/or a silicon dioxide layer, and/or an aluminum silicon nitride layer, and/or an aluminum oxide layer, and/or an aluminum oxynitride layer, and/or hafnium oxide, and/or silicon oxynitride, and/or hafnium aluminum oxide.

[0053] Referring to Figure 3b, a groove H3 partially through the dielectric layer is formed by etching the gate region of the dielectric layer. Here, the partially through indicates that the bottom of the groove is located within the dielectric layer. In the embodiment, fluorine-based plasma etching, for example, may be adopted in the etching process. Due to selective etching by the fluorine-based plasma etching treatment, the etching process stops when reaching the aluminum nitride layer 7.

[0054] Referring to Figure 3c, p-type semiconductor material 9 is deposited in the groove H3 formed by etching. The p-type semiconductor material 9 may be selected from p-type diamond, p-type NiO, p-type GaN, or p-type polycrystalline GaN, etc.

[0055] Referring to Figure 3d, the p-type semiconductor material 9 on the dielectric layer except for the gate region is removed. In the embodiment, for example, the p-type semiconductor material 9 is p-type diamond, then the p-type diamond in the gate region is retained, and the p-type diamond in other region may be etched away with plasma. In this case, the p-type semiconductor material 9 is actually the gate of the enhancement mode switching device in the application. Conductivity of the gate can be improved with an additional

metal layer.

[0056] Referring to Figure 3e, the nitride transistor structure is exposed by etching the dielectric layer except for the gate region. In the embodiment, the nitride barrier layer 5 may be exposed, for example, by dry etching, or the nitride barrier layer 5 may even be etched through, to form two ohmic contact regions. Finally, a source electrode 10 is formed on one ohmic contact region, and a drain electrode 11 is formed on the other ohmic contact region.

[0057] Referring to Figure 4f, in a fourth embodiment of the application, an enhancement mode switching device includes: a substrate 1, and a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4, a nitride barrier layer 5, a silicon nitride layer 6, an aluminum nitride layer 7 and a silicon nitride layer 8 which are formed on the substrate 1 in sequence. A groove H4 is arranged in a gate region of the silicon nitride layer 8 (referring to Figure 4c). A height of the groove H4 is equal to a sum of a thickness of the silicon nitride layer 8 and a thickness of the aluminum nitride layer 7. P-type semiconductor material 9 is formed on an inner wall of the groove H4 and on the gate region. A source electrode 10 and a drain electrode 11 are arranged at two sides of the gate region, respectively. Each of the source electrode 10 and the drain electrode 11 is through the silicon nitride layer 8, the aluminum nitride layer 7 and the silicon nitride layer 6 in a vertical direction, and contacts with the nitride barrier layer 5.

[0058] Figure 4a - Figure 4f are cross sections illustrating the enhancement mode switching device and a series of processes of a method for fabricating the same according to the fourth embodiment of the application.

[0059] Referring to Figure 4a, a substrate 1 is provided at first. The substrate 1 may be selected from semiconductor material, ceramic material or macromolecular material, etc. In this embodiment, the substrate 1 is preferably selected from sapphire, silicon carbide, silicon, lithium niobate, silicon-on-insulator substrate (SOI), gallium nitride or aluminum nitride.

[0060] A nitride transistor structure is then prepared on the substrate 1. The nitride here is preferably AlInGaN. Specifically, a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4 and a nitride barrier layer 5 are grown on the substrate 1 in sequence. Here, material of the nitride nucleation layer 2, the nitride buffer layer 3, the nitride channel layer 4 and the nitride barrier layer 5 may be any Group III nitride or any combination of Group III nitrides. In the embodiment, the nitride nucleation layer 2 may be, for example, AlInGaN. The nitride buffer layer 3 may be, for example, AlGaN. The nitride channel layer 4 may be, for example, GaN. The nitride barrier layer 5 may be, for example, AlGaN. In other embodiments, the nitride barrier layer 5 may not be arranged, and in this case, the nitride channel layer 4 is non-doped or n-doped.

[0061] A dielectric layer is then grown on the accomplished nitride transistor structure. A gate region is defined on the dielectric layer. Specifically, a silicon nitride layer 6, an aluminum nitride layer 7 and a silicon nitride layer 8 are grown on the accomplished nitride transistor

structure in sequence. In the embodiment, the dielectric layer may be grown in situ or may be grown by Atomic Layer Deposition (ALD), Chemical Vapor Deposition (CVD), Molecular Beam Epitaxy (MBE), Plasma Enhanced Chemical Vapor Deposition (PECVD) or Low Pressure Chemical Vapor Deposition (LPCVD), or a combination thereof. It should be understood that the methods for forming the dielectric layer described herein are merely for illustration. In the application, the dielectric layer may be formed by any method known to those skilled in the art. The dielectric layer includes a silicon nitride layer, and/or a silicon dioxide layer, and/or an aluminum silicon nitride layer, and/or an aluminum oxide layer, and/or an aluminum oxynitride layer, and/or hafnium oxide, and/or silicon oxynitride, and/or hafnium aluminum oxide.

[0062] Referring to Figure 4b and Figure 4c, a groove H4 partially through the dielectric layer is formed by etching a gate region of the dielectric layer. Here, the partially through indicates that the bottom of the groove is located within the dielectric layer. In the embodiment, fluorine-based plasma etching, for example, may be adopted in the etching process. Due to selective etching by the fluorine-based plasma etching treatment, the etching process stops when reaching the aluminum nitride layer 7. The aluminum nitride layer is then etched through by wet etching or dry etching, to form the groove H4.

[0063] Referring to Figure 4d, p-type semiconductor material 9 is deposited in the groove H4 formed by etching. The p-type semiconductor material 9 may be selected from p-type diamond, p-type NiO, p-type GaN, or p-type polycrystalline GaN, etc.

[0064] Referring to Figure 4e, the p-type semiconductor material 9 on the dielectric layer except for the gate region is removed. In the embodiment, for example, the p-type semiconductor material 9 is p-type diamond, then the p-type diamond in the gate region is retained, and the p-type diamond in other region may be etched away with plasma. In this case, the p-type semiconductor material 9 is actually the gate of the enhancement mode switching device in the application. Conductivity of the gate can be improved with an additional conductive metal layer.

[0065] Referring to Figure 4f, the nitride transistor structure is exposed by etching the dielectric layer except for the gate region. In the embodiment, the nitride barrier layer 5 may be exposed, for example, by dry etching, or the nitride barrier layer 5 may even be etched through, to form two ohmic contact regions. Finally, a source electrode 10 is formed on one ohmic contact region, and a drain electrode 11 is formed on the other ohmic contact region.

[0066] Referring to Figure 5f, in a fifth embodiment of the application, an enhancement mode switching device includes: a substrate 1, and a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4, a nitride barrier layer 5, a silicon nitride layer 6, an aluminum nitride layer 7 and a silicon nitride layer 8 which are formed on the substrate 1 in sequence. A groove H5 is arranged in a gate region of the silicon nitride layer 8 (referring to Figure 5b). A height of the groove H5 is equal to a thickness of the silicon nitride layer 8. P-type semiconductor material is formed on an inner wall of the groove H5 and on the gate region. A source electrode 10 and a drain electrode 11 are arranged at two sides of the gate region,

respectively. Each of the source electrode 10 and the drain electrode 11 is through the silicon nitride layer 8, the aluminum nitride layer 7 and the silicon nitride layer 6 in a vertical direction, and contacts with the nitride barrier layer 5. An Al_2O_3 layer 12 or an AlON layer 12 is further arranged between the bottom of the groove H5 and the silicon nitride layer 6.

[0067] Figure 5a - Figure 5f are cross sections illustrating the enhancement mode switching device and a series of processes of a method for fabricating the same according to the fifth embodiment of the application.

[0068] Referring to Figure 5a, a substrate 1 is provided at first. The substrate 1 may be selected from semiconductor material, ceramic material or macromolecular material, etc. In this embodiment, the substrate 1 is preferably selected from sapphire, silicon carbide, silicon, lithium niobate, silicon-on-insulator substrate (SOI), gallium nitride or aluminum nitride.

[0069] A nitride transistor structure is then prepared on the substrate 1. The nitride here is preferably AlInGaN. Specifically, a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4 and a nitride barrier layer 5 are grown on the substrate 1 in sequence. Here, material of the nitride nucleation layer 2, the nitride buffer layer 3, the nitride channel layer 4 and the nitride barrier layer 5 may be any Group III nitride or any combination of Group III nitrides. In the embodiment, the nitride nucleation layer 2 may be, for example, AlInGaN. The nitride buffer layer 3 may be, for example, AlGaN. The nitride channel layer 4 may be, for example, GaN. The nitride barrier layer 5 may be, for example, AlGaN. In other embodiments, the nitride barrier layer 5 may not be arranged, and in this case, the nitride channel layer 4 is non-doped or n-doped.

[0070] A dielectric layer is then grown on the accomplished nitride transistor structure. A gate region is defined on the dielectric layer. Specifically, a silicon nitride layer 6, an aluminum nitride layer 7 and a silicon nitride layer 8 are grown on the accomplished nitride transistor structure in sequence. In the embodiment, the dielectric layer may be grown in situ or may be grown by Atomic Layer Deposition (ALD), Chemical Vapor Deposition (CVD), Molecular Beam Epitaxy (MBE), Plasma Enhanced Chemical Vapor Deposition (PECVD) or Low Pressure Chemical Vapor Deposition (LPCVD), or a combination thereof. It should be understood that the methods for forming the dielectric layer described herein are merely for illustration. In the application, the dielectric layer may be formed by any method known to those skilled in the art. The dielectric layer includes a silicon nitride layer, and/or a silicon dioxide layer, and/or an aluminum silicon nitride layer, and/or an aluminum oxide layer, and/or an aluminum oxynitride layer, and/or hafnium oxide, and/or silicon oxynitride, and/or hafnium aluminum oxide.

[0071] Referring to Figure 5b, a groove H5 partially through the dielectric layer is formed by etching the gate region of the dielectric layer. Here, the partially through indicates that the bottom of the groove is located within the dielectric layer. In the embodiment, fluorine-based plasma etching, for example, may be adopted in the etching process. Due to selective etching by the fluorine-based plasma etching treatment, the etching process stops when reaching the aluminum nitride layer 7.

[0072] Referring to Figure 5c, after the etching is completed, the aluminum nitride layer corresponding to the groove H5 may be oxidized by a method of thermal oxidation, wet oxidation, oxygen ions, or ozone, etc. In the embodiment, the aluminum nitride layer herein may be converted into an Al_2O_3 layer 12 or an AlON layer 12.

[0073] Referring to Figure 5d, p-type semiconductor material 9 is deposited in the groove H5 formed by etching. The p-type semiconductor material 9 may be selected from p-type diamond, p-type NiO, p-type GaN, or p-type polycrystalline GaN, etc.

[0074] Referring to Figure 5e, the p-type semiconductor material 9 on the dielectric layer except for the gate region is removed. In the embodiment, for example, the p-type semiconductor material 9 is p-type diamond, then the p-type diamond in the gate region is retained, and the p-type diamond in other region may be etched away with plasma. In this case, the p-type semiconductor material 9 is actually the gate of the enhancement mode switching device in the application. Conductivity of the gate can be improved with an additional conductive metal layer.

[0075] Referring to Figure 5f, the nitride transistor structure is exposed by etching the dielectric layer except for the gate region. In the embodiment, the nitride barrier layer 5 may be exposed, for example, by dry etching, or the nitride barrier layer 5 may even be etched through, to form two ohmic contact regions. Finally, a source electrode 10 is formed on one ohmic contact region, and a drain electrode 11 is formed on the other ohmic contact region.

[0076] Referring to Figure 6f, in a sixth embodiment of the application, an enhancement mode switching device includes: a substrate 1, and a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4, a nitride barrier layer 5, a silicon nitride layer 6, an aluminum silicon nitride layer 13 and a silicon nitride layer 8 which are formed on the substrate 1 in sequence. A groove H6 is arranged in a gate region of the silicon nitride layer 8 (referring to Figure 6c). A height of the groove H6 is equal to a sum of a thickness of the silicon nitride layer 8 and a thickness of the aluminum silicon nitride layer 13. P-type semiconductor material is formed on an inner wall of the groove H4 and on the gate region. A source electrode 10 and a drain electrode 11 are arranged at two sides of the gate region, respectively. Each of the source electrode 10 and the drain electrode 11 is through the silicon nitride layer 8, the aluminum silicon nitride layer 13 and the silicon nitride layer 6 in a vertical direction, and contacts with the nitride barrier layer 5.

[0077] Figure 6a - Figure 6f are cross sections illustrating the enhancement mode switching device and a series of processes of a method for fabricating the same according to the sixth embodiment of the application.

[0078] Referring to Figure 6a, a substrate 1 is provided at first. The substrate 1 may be selected from semiconductor material, ceramic material or macromolecular material, etc. In this embodiment, the substrate 1 is preferably selected from sapphire, silicon carbide, silicon,

lithium niobate, silicon-on-insulator substrate (SOI), gallium nitride or aluminum nitride.

[0079] A nitride transistor structure is then prepared on the substrate 1. The nitride here is preferably AlInGaN. Specifically, a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4 and a nitride barrier layer 5 are grown on the substrate I in sequence. Here, material of the nitride nucleation layer 2, the nitride buffer layer 3, the nitride channel layer 4 and the nitride barrier layer 5 may be any Group III nitride or any combination of Group III nitrides. In the embodiment, the nitride nucleation layer 2 may be, for example, AlInGaN. The nitride buffer layer 3 may be, for example, AlGaN. The nitride channel layer 4 may be, for example, GaN. The nitride barrier layer 5 may be, for example, AlGaN. In other embodiments, the nitride barrier layer 5 may not be arranged, and in this case, the nitride channel layer 4 is non-doped or n-doped.

[0080] A dielectric layer then is grown on the accomplished nitride transistor structure. A gate region is defined on the dielectric layer. Specifically, a silicon nitride layer 6, an aluminum silicon nitride layer 13 and a silicon nitride layer 8 are grown on the accomplished nitride transistor structure in sequence. In the embodiment, the dielectric layer may be grown in situ or may be grown by Atomic Layer Deposition (ALD), Chemical Vapor Deposition (CVD), Molecular Beam Epitaxy (MBE), Plasma Enhanced Chemical Vapor Deposition (PECVD) or Low Pressure Chemical Vapor Deposition (LPCVD), or a combination thereof. It should be understood that the methods for forming the dielectric layer described herein are merely for illustration. In the application, the dielectric layer may be formed by any method known to those skilled in the art. The dielectric layer includes a silicon nitride layer, and/or a silicon dioxide layer, and/or an aluminum silicon nitride layer, and/or an aluminum oxide layer, and/or an aluminum oxynitride layer, and/or hafnium oxide, and/or silicon oxynitride, and/or hafnium aluminum oxide.

[0081] Referring to Figure 6b and Figure 6c, a groove H6 partially through the dielectric layer is formed by etching the gate region of the dielectric layer. Here, the partially through indicates that the bottom of the groove is located within the dielectric layer. In the embodiment, fluorine-based plasma etching, for example, may be adopted in the etching process. Due to selective etching by the fluorine-based plasma etching treatment, the etching process stops when reaching the aluminum silicon nitride layer 13. The aluminum silicon nitride layer is then etched through by wet etching or dry etching, to form the groove H6.

[0082] Referring to Figure 6d, p-type semiconductor material 9 is deposited in the groove H6 formed by etching. The p-type semiconductor material 9 may be selected from p-type diamond, p-type NiO, p-type GaN, or p-type polycrystalline GaN, etc.

[0083] Referring to Figure 6e, the p-type semiconductor material 9 on the dielectric layer except for the gate region is removed. In the embodiment, for example, the p-type semiconductor material 9 is p-type diamond, then the p-type diamond in the gate region is retained, and the p-type diamond in other region may be etched away with plasma. In this case, the p-type semiconductor material 9 is actually the gate of the enhancement mode

switching device in the application. Conductivity of the gate can be improved with an additional conductive metal layer.

[0084] Referring to Figure 6f, the nitride transistor structure is exposed by etching the dielectric layer except for the gate region. In the embodiment, the nitride barrier layer 5 may be exposed, for example, by dry etching, or the nitride barrier layer 5 may even be etched through, to form two ohmic contact regions. Finally, a source electrode 10 is formed on one ohmic contact region, and a drain electrode 11 is formed on the other ohmic contact region.

[0085] Referring to Figure 7f, in a seventh embodiment of the application, an enhancement mode switching device includes: a substrate 1, and a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4, a nitride barrier layer 5, an aluminum silicon nitride layer 13, an aluminum nitride layer 7 and a silicon nitride layer 8 which are formed on the substrate 1 in sequence. A groove H7 is arranged in a gate region of the silicon nitride layer 8 (referring to Figure 7c). A height of the groove H7 is equal to a sum of a thickness of the silicon nitride layer 8 and a thickness of the aluminum nitride layer 7. P-type semiconductor material is formed on an inner wall of the groove H5 and on the gate region. A source electrode 10 and a drain electrode 11 are formed at two sides of the gate region, respectively. Each of the source electrode 10 and the drain electrode 11 is through the silicon nitride layer 8, the aluminum nitride layer 7 and the aluminum silicon nitride layer 13 in a vertical direction, and contacts with the nitride barrier layer 5.

[0086] Figure 7a - Figure 7f are cross sections illustrating the enhancement mode switching device and a series of processes of a method for fabricating the same according to the seventh embodiment of the application.

[0087] Referring to Figure 7a, a substrate 1 is provided at first. The substrate 1 may be selected from semiconductor material, ceramic material or macromolecular material, etc. In this embodiment, the substrate 1 is preferably selected from sapphire, silicon carbide, silicon, lithium niobate, silicon-on-insulator substrate (SOI), gallium nitride or aluminum nitride.

[0088] A nitride transistor structure is then prepared on the substrate 1. The nitride here is preferably AlInGaN. Specifically, a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4 and a nitride barrier layer 5 are grown on the substrate 1 in sequence. Here, material of the nitride nucleation layer 2, the nitride buffer layer 3, the nitride channel layer 4 and the nitride barrier layer 5 may be any Group III nitride or any combination of Group III nitrides. In the embodiment, the nitride nucleation layer 2 may be, for example, AlInGaN. The nitride buffer layer 3 may be, for example, AlGaN. The nitride channel layer 4 may be, for example, GaN. The nitride barrier layer 5 may be, for example, AlGaN. In other embodiments, the nitride barrier layer 5 may not be arranged, and in this case, the nitride channel layer 4 is non-doped or n-doped.

[0089] A dielectric layer is then grown on the accomplished nitride transistor structure. A gate region is defined on the dielectric layer. Specifically, an aluminum silicon nitride layer 13, an

aluminum nitride layer 7 and a silicon nitride layer 8 are grown on the accomplished nitride transistor structure in sequence. In the embodiment, the dielectric layer may be grown in situ or may be grown by Atomic Layer Deposition (ALD), Chemical Vapor Deposition (CVD), Molecular Beam Epitaxy (MBE), Plasma Enhanced Chemical Vapor Deposition (PECVD) or Low Pressure Chemical Vapor Deposition (LPCVD), or a combination thereof. It should be understood that the methods for forming the dielectric layer described herein are merely for illustration. In the application, the dielectric layer may be formed by any method known to those skilled in the art. The dielectric layer includes a silicon nitride layer, and/or a silicon dioxide layer, and/or an aluminum silicon nitride layer, and/or an aluminum oxide layer, and/or an aluminum oxynitride layer, and/or hafnium oxide, and/or silicon oxynitride, and/or hafnium aluminum oxide.

[0090] Referring to Figure 7b and Figure 7c, a groove H7 partially through the dielectric layer is formed by etching the gate region of the dielectric layer. Here, the partially through indicates that the bottom of the groove is located within the dielectric layer. In the embodiment, fluorine-based plasma etching, for example, may be adopted in the etching process. Due to selective etching by the fluorine-based plasma etching treatment, the etching process stops when reaching the aluminum nitride layer 7. The aluminum nitride layer is then etched through by wet etching or dry etching, to form the groove H7.

[0091] Referring to Figure 7d, p-type semiconductor material 9 is deposited in the groove H5 formed by etching. The p-type semiconductor material 9 may be selected from p-type diamond, p-type NiO, p-type GaN, or p-type polycrystalline GaN, etc.

[0092] Referring to Figure 7e, the p-type semiconductor material 9 on the dielectric layer except for the gate region is removed. In the embodiment, for example, the p-type semiconductor material 9 is p-type diamond, then the p-type diamond in the gate region is retained, and the p-type diamond in other region may be etched away with plasma. In this case, the p-type semiconductor material 9 is actually the gate of the enhancement mode switching device in the application. Conductivity of the gate can be improved with an additional conductive metal layer.

[0093] Referring to Figure 7f, the nitride transistor structure is exposed by etching the dielectric layer except for the gate region. In the embodiment, the nitride barrier layer 5 may be exposed, for example, by dry etching, or the nitride barrier layer 5 may even be etched through, to form two ohmic contact regions. Finally, a source electrode 10 is formed on one ohmic contact region, and a drain electrode 11 is formed on the other ohmic contact region.

[0094] Referring to Figure 8e, in an eighth embodiment of the application, an enhancement mode switching device includes: a substrate 1, and a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4, a nitride barrier layer 5, an aluminum silicon nitride layer 13 and a silicon nitride layer 8 which are formed on the substrate 1 in sequence. A groove H8 is arranged in a gate region of the silicon nitride layer 8 (referring to Figure 8b). A height of the groove H8 is equal to a thickness of the silicon nitride layer 8. P-type semiconductor material 9

is formed on an inner wall of the groove H8 and on the gate region. A source electrode 10 and a drain electrode 11 are arranged at two sides of the gate region, respectively. Each of the source electrode 10 and the drain electrode 11 is through the silicon nitride layer 8 and the aluminum silicon nitride layer 13 in a vertical direction, and contacts with the nitride barrier layer 5.

[0095] Figure 8a - Figure 8e are cross sections illustrating the enhancement mode switching device and a series of processes of a method for fabricating the same according to the eighth embodiment of the application.

[0096] Referring to Figure 8a, a substrate 1 is provided at first. The substrate 1 may be selected from semiconductor material, ceramic material or macromolecular material, etc. In this embodiment, the substrate 1 is preferably selected from sapphire, silicon carbide, silicon, lithium niobate, silicon-on-insulator substrate (SOI), gallium nitride or aluminum nitride.

[0097] A nitride transistor structure is then prepared on the substrate 1. The nitride here is preferably AlInGaN. Specifically, a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4 and a nitride barrier layer 5 are grown on the substrate 1 in sequence. Here, material of the nitride nucleation layer 2, the nitride buffer layer 3, the nitride channel layer 4 and the nitride barrier layer 5 may be any Group III nitride or any combination of Group III nitrides. In the embodiment, the nitride nucleation layer 2 may be, for example, AlInGaN. The nitride buffer layer 3 may be, for example, AlGaN. The nitride channel layer 4 may be, for example, GaN. The nitride barrier layer 5 may be, for example, AlGaN. In other embodiments, the nitride barrier layer 5 may not be arranged, and in this case, the nitride channel layer 4 is non-doped or n-doped.

[0098] A dielectric layer is then grown on the accomplished nitride transistor structure. A gate region is defined on the dielectric layer. Specifically, an aluminum silicon nitride layer 13 and a silicon nitride layer 8 are grown on the accomplished nitride transistor structure in sequence. In the embodiment, the dielectric layer may be grown in situ or may be grown by Atomic Layer Deposition (ALD), Chemical Vapor Deposition (CVD), Molecular Beam Epitaxy (MBE), Plasma Enhanced Chemical Vapor Deposition (PECVD) or Low Pressure Chemical Vapor Deposition (LPCVD), or a combination thereof. It should be understood that the methods for forming the dielectric layer described herein are merely for illustration. In the application, the dielectric layer may be formed by any method known to those skilled in the art. The dielectric layer includes a silicon nitride layer, and/or a silicon dioxide layer, and/or an aluminum silicon nitride layer, and/or an aluminum oxide layer, and/or an aluminum oxynitride layer, and/or hafnium oxide, and/or silicon oxynitride, and/or hafnium aluminum oxide.

[0099] Referring to Figure 8b, a groove H8 partially through the dielectric layer is formed by etching the gate region of the dielectric layer. Here, the partially through indicates that the bottom of the groove is located within the dielectric layer. In the embodiment, fluorine-based plasma etching, for example, may be adopted in the etching process. Due to selective etching by the fluorine-based plasma etching treatment, the etching process stops when reaching the

aluminum silicon nitride layer 13, to form the groove H8.

[0100] Referring to Figure 8c, p-type semiconductor material 9 is deposited in the groove H8 formed by etching. The p-type semiconductor material 9 may be selected from p-type diamond, p-type NiO, p-type GaN, or p-type polycrystalline GaN, etc.

[0101] Referring to Figure 8e, the p-type semiconductor material 9 on the dielectric layer except for the gate region is removed. In the embodiment, for example, the p-type semiconductor material 9 is p-type diamond, then the p-type diamond in the gate region is retained, and the p-type diamond in other region may be etched away with plasma. In this case, the p-type semiconductor material 9 is actually the gate of the enhancement mode switching device in the application. Conductivity of the gate can be improved with an additional conductive metal layer.

[0102] Referring to Figure 8e, the nitride transistor structure is exposed by etching the dielectric layer except for the gate region. In the embodiment, the nitride barrier layer 5 may be exposed, for example, by dry etching, or the nitride barrier layer 5 may even be etched through, to form two ohmic contact regions. Finally, a source electrode 10 is formed on one ohmic contact region, and a drain electrode 11 is formed on the other ohmic contact region.

[0103] Referring to Figure 9f, in a ninth embodiment of the application, an enhancement mode switching device includes: a substrate 1, and a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4, a nitride barrier layer 5, an aluminum silicon nitride layer 13 and a silicon nitride layer 8 which are formed on the substrate 1 in sequence. A groove H9 is arranged in a gate region of the silicon nitride layer 8 (referring to Figure 9b). A height of the groove H9 is equal to a thickness of the silicon nitride layer 8. An additional dielectric layer 14 is formed on an inner wall of the groove H9 and on the silicon nitride layer 8. P-type semiconductor material 9 is formed on a gate region of the additional dielectric layer 14. A source electrode 10 and a drain electrode 11 are arranged at two sides of the gate region, respectively. Each of the source electrode 10 and the drain electrode 11 is through the additional dielectric layer 14, the silicon nitride layer 8 and the aluminum silicon nitride layer 13 in a vertical direction, and contacts with the nitride barrier layer 5.

[0104] Figure 9a - Figure 9f are cross sections illustrating the enhancement mode switching device and a series of processes of a method for fabricating the same according to the ninth embodiment of the application.

[0105] Referring to Figure 9a, a substrate 1 is provided at first. The substrate 1 may be selected from semiconductor material, ceramic material or macromolecular material, etc. In this embodiment, the substrate 1 is preferably selected from sapphire, silicon carbide, silicon, lithium niobate, silicon-on-insulator substrate (SOI), gallium nitride or aluminum nitride.

[0106] A nitride transistor structure is then prepared on the substrate 1. The nitride here is preferably AlInGaN. Specifically, a nitride nucleation layer 2, a nitride buffer layer 3, a nitride

channel layer 4 and a nitride barrier layer 5 are grown on the substrate 1 in sequence. Here, material of the nitride nucleation layer 2, the nitride buffer layer 3, the nitride channel layer 4 and the nitride barrier layer 5 may be any Group III nitride or any combination of Group III nitrides. In the embodiment, the nitride nucleation layer 2 may be, for example, AlInGaN. The nitride buffer layer 3 may be, for example, AlGaN. The nitride channel layer 4 may be, for example, GaN. The nitride barrier layer 5 may be, for example, AlGaN. In other embodiments, the nitride barrier layer 5 may not be arranged, and in this case, the nitride channel layer 4 is non-doped or n-doped.

[0107] A dielectric layer is then grown on the accomplished nitride transistor structure. A gate region is defined on the dielectric layer. Specifically, an aluminum silicon nitride layer 13 and a silicon nitride layer 8 are grown on the accomplished nitride transistor structure in sequence. In the embodiment, the dielectric layer may be grown in situ or may be grown by Atomic Layer Deposition (ALD), Chemical Vapor Deposition (CVD), Molecular Beam Epitaxy (MBE), Plasma Enhanced Chemical Vapor Deposition (PECVD) or Low Pressure Chemical Vapor Deposition (LPCVD), or a combination thereof. It should be understood that the methods for forming the dielectric layer described herein are merely for illustration. In the application, the dielectric layer may be formed by any method known to those skilled in the art. The dielectric layer includes a silicon nitride layer, and/or a silicon dioxide layer, and/or an aluminum silicon nitride layer, and/or an aluminum oxide layer, and/or an aluminum oxynitride layer, and/or hafnium oxide, and/or silicon oxynitride, and/or hafnium aluminum oxide.

[0108] Referring to Figure 9b, a groove H9 partially through the dielectric layer is formed by etching the gate region of the dielectric layer. Here, the partially through indicates that the bottom of the groove is located within the dielectric layer. In the embodiment, fluorine-based plasma etching, for example, may be adopted in the etching process. Due to selective etching by the fluorine-based plasma etching treatment, the etching process stops when reaching the aluminum silicon nitride layer 13, to form the groove H9.

[0109] Referring to Figure 9c, an additional dielectric layer 14 is deposited in the groove H9 formed by etching. Material of the additional dielectric layer 14 may include, for example, Al_2O_3 or AlON. The additional dielectric layer 14 may be grown by Atomic Layer Deposition, Chemical Vapor Deposition, Molecular Beam Epitaxy, Plasma Enhanced Chemical Vapor Deposition or Low Pressure Chemical Vapor Deposition, or a combination thereof. It should be understood that the methods for forming the additional dielectric layer described herein are merely for illustration. In the application, the additional dielectric layer may be formed by any method known to those skilled in the art. Material of the additional dielectric layer may also be selected from one or any combination of SiN, SiON, SiO_2 and HfO_2.

[0110] Referring to Figure 9d, p-type semiconductor material 9 is deposited on the additional dielectric layer 14 in the groove H9 formed by etching. The p-type semiconductor material 9 may be selected from p-type diamond, p-type NiO, p-type GaN, or p-type polycrystalline GaN, etc.

[0111] Referring to Figure 9e, the p-type semiconductor material 9 on the additional dielectric layer 14 except for the gate region is removed. In the embodiment, for example, the p-type semiconductor material 9 is p-type diamond, then the p-type diamond in the gate region is retained, and the p-type diamond in other region may be etched away with plasma. In this case, the p-type semiconductor material 9 is actually the gate of the enhancement mode switching device in the application. Conductivity of the gate can be improved with an additional conductive metal layer.

[0112] Referring to Figure 9f, the nitride transistor structure is exposed by etching the dielectric layer except for the gate region. In the embodiment, the nitride barrier layer 5 may be exposed, for example, by dry etching, or the nitride barrier layer 5 may even be etched through, to form two ohmic contact regions. Finally, a source electrode 10 is formed on one ohmic contact region, and a drain electrode 11 is formed on the other ohmic contact region.

[0113] Referring to Figure 10e, in a tenth embodiment of the application, an enhancement mode switching device includes: a substrate 1, and a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4, a nitride barrier layer 5, a cap layer 15, an aluminum oxide layer 16 (or an aluminum oxynitride layer 16) and a silicon nitride layer 8 which are formed on the substrate 1 in sequence. A groove H10 is arranged in a gate region of the silicon nitride layer 8 (referring to Figure 10b). A height of the groove H10 is equal to a thickness of the silicon nitride layer 8. P-type semiconductor material 9 is formed on an inner wall of the groove H10 and on a gate region. A source electrode 10 and a drain electrode 11 are arranged at two sides of the gate region, respectively. Each of the source electrode 10 and the drain electrode 11 is through the silicon nitride layer 8, the aluminum oxide layer 16 (or the aluminum oxynitride layer 16) and the cap layer 15, and contacts with the nitride barrier layer 5.

[0114] Figure 10a - Figure 10e are cross sections illustrating the enhancement mode switching device and a series of processes of a method for fabricating the same according to the tenth embodiment of the application.

[0115] Referring to Figure 10a, a substrate 1 is provided at first. The substrate 1 may be selected from semiconductor material, ceramic material or macromolecular material, etc. In this embodiment, the substrate 1 is preferably selected from sapphire, silicon carbide, silicon, lithium niobate, silicon-on-insulator substrate (SOI), gallium nitride or aluminum nitride.

[0116] A nitride transistor structure is then prepared on the substrate 1. The nitride is preferably AlInGaN. Specifically, a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4, a nitride barrier layer 5 and a cap layer 15 are grown on the substrate 1 in sequence. Here, material of the nitride nucleation layer 2, the nitride buffer layer 3, the nitride channel layer 4 and the nitride barrier layer 5 may be any Group III nitride or any combination of Group III nitrides. In the embodiment, the nitride nucleation layer 2 may be, for example, AlInGaN. The nitride buffer layer 3 may be, for example, AlGaN. The nitride channel layer 4 may be, for example, GaN. The nitride barrier layer 5 may be, for example, AlGaN. The cap layer 15 may be gallium nitride, or may also include aluminum (aluminum gallium nitride),

where a compositional ratio of aluminum may be a constant or decrease gradually or increase first and then decrease, or a super lattice structure is formed with a compositional ratio of aluminum varying periodically. In other embodiments, the nitride barrier layer 5 may not be arranged, and in this case, the nitride channel layer 4 is non-doped or n-doped.

[0117] A dielectric layer is then grown on the accomplished nitride transistor structure. A gate region is defined on the dielectric layer. Specifically, an aluminum oxide layer 16 (or an aluminum oxynitride layer 16) and a silicon nitride layer 8 are grown on the accomplished nitride transistor structure in sequence. In the embodiment, the dielectric layer may be grown in situ or may be grown by Atomic Layer Deposition (ALD), Chemical Vapor Deposition (CVD), Molecular Beam Epitaxy (MBE), Plasma Enhanced Chemical Vapor Deposition (PECVD) or Low Pressure Chemical Vapor Deposition (LPCVD), or a combination thereof. It should be understood that the methods for forming the dielectric layer described herein are merely for illustration. In the application, the dielectric layer may be formed by any method known to those skilled in the art. The dielectric layer includes a silicon nitride layer, and/or a silicon dioxide layer, and/or an aluminum silicon nitride layer, and/or an aluminum oxide layer, and/or an aluminum oxynitride layer, and/or hafnium oxide, and/or silicon oxynitride, and/or hafnium aluminum oxide.

[0118] Referring to Figure 10b, a groove H10 partially through the dielectric layer is formed by etching the gate region of the dielectric layer. Here, the partially through indicates that the bottom of the groove is located within the dielectric layer. In the embodiment, fluorine-based plasma etching, for example, may be adopted in the etching process. Due to selective etching by the fluorine-based plasma etching treatment, the etching process stops when reaching the aluminum oxide layer 16 (or the aluminum oxynitride layer 16), to form the groove H10.

[0119] Referring to Figure 10c, p-type semiconductor material 9 is deposited in the groove H8 formed by etching. The p-type semiconductor material 9 may be selected from p-type diamond, p-type NiO, p-type GaN, or p-type polycrystalline GaN, etc.

[0120] Referring to Figure 10d, the p-type semiconductor material 9 on the dielectric layer except for the gate region is removed. In the embodiment, for example, the p-type semiconductor material 9 is p-type diamond, then the p-type diamond in the gate region is retained, and the p-type diamond in other region may be etched away with plasma. In this case, the p-type semiconductor material 9 is actually the gate of the enhancement mode switching device in the application. Conductivity of the gate can be improved with an additional conductive metal layer.

[0121] Referring to Figure 10e, the nitride transistor structure is exposed by etching the dielectric layer except for the gate region. In the embodiment, the nitride barrier layer 5 may be exposed, for example, by dry etching, or the nitride barrier layer 5 may even be etched through, to form two ohmic contact regions. Finally, a source electrode 10 is formed on one ohmic contact region, and a drain electrode 11 is formed on the other ohmic contact region.

[0122] Referring to Figure 11g, in an eleventh embodiment of the application, an enhancement mode switching device includes: a substrate 1, and a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4, a nitride barrier layer 5, a cap layer 15, an aluminum oxide layer 16 (or an aluminum oxynitride layer 16) and a silicon nitride layer 8 which are formed on the substrate 1 in sequence. A groove H11 is arranged in a gate region of the silicon nitride layer 8 (referring to Figure 11c). A height of the groove H11 is equal to a sum of a thickness of the silicon nitride layer 8, a thickness of the aluminum oxide layer 16 (or the aluminum oxynitride layer 16) and a thickness of the cap layer 15. An additional dielectric layer 14 is formed on an inner wall of the groove H11 and on the silicon nitride layer 8. P-type semiconductor material 9 is formed on a gate region of the additional dielectric layer 14. A source electrode 10 and a drain electrode 11 are arranged at two sides of the gate region, respectively. Each of the source electrode 10 and the drain electrode 11 is through the additional dielectric layer 14, the silicon nitride layer 8, the aluminum oxide layer 16 (or the aluminum oxynitride layer 16) and the cap layer 15, and contacts with the nitride barrier layer 5.

[0123] Figure 11a - Figure 11g are cross sections illustrating the enhancement mode switching device and a series of processes of a method for fabricating the same according to the eleventh embodiment of the application.

[0124] Referring to Figure 11a, a substrate 1 is provided at first. The substrate 1 may be selected from semiconductor material, ceramic material or macromolecular material, etc. In this embodiment, the substrate 1 is preferably selected from sapphire, silicon carbide, silicon, lithium niobate, silicon-on-insulator substrate (SOI), gallium nitride or aluminum nitride.

[0125] A nitride transistor structure is then prepared on the substrate 1. The nitride here is preferably AlInGaN. Specifically, a nitride nucleation layer 2, a nitride buffer layer 3, a nitride channel layer 4, a nitride barrier layer 5 and a cap layer 15 are grown on the substrate 1 in sequence. Here, material of the nitride nucleation layer 2, the nitride buffer layer 3, the nitride channel layer 4 and the nitride barrier layer 5 may be any Group III nitride or any combination of Group III nitrides. In the embodiment, the nitride nucleation layer 2 may be, for example, AlInGaN. The nitride buffer layer 3 may be, for example, AlGaN. The nitride channel layer 4 may be, for example, GaN. The nitride barrier layer 5 may be, for example, AlGaN. The cap layer 15 may be gallium nitride, or may also include aluminum (aluminum gallium nitride), where a compositional ratio of aluminum may be a constant or decrease gradually or increase first and then decrease, or a super lattice structure is formed with a compositional ratio of aluminum varying periodically. In other embodiments, the nitride barrier layer 5 may not be arranged, and in this case, the nitride channel layer 4 is non-doped or n-doped.

[0126] A dielectric layer is then grown on the accomplished nitride transistor structure. A gate region is defined on the dielectric layer. Specifically, an aluminum oxide layer 16 (or an aluminum oxynitride layer 16) and a silicon nitride layer 8 are grown on the accomplished nitride transistor structure in sequence. In the embodiment, the dielectric layer may be grown in situ or may be grown by Atomic Layer Deposition (ALD), Chemical Vapor Deposition (CVD),

Molecular Beam Epitaxy (MBE), Plasma Enhanced Chemical Vapor Deposition (PECVD) or Low Pressure Chemical Vapor Deposition (LPCVD), or a combination thereof. It should be understood that the methods for forming the dielectric layer described herein are merely for illustration. In the application, the dielectric layer may be formed by any method known to those skilled in the art. In other embodiments, the dielectric layer may also include a silicon nitride layer, and/or a silicon dioxide layer, and/or an aluminum nitride layer, and/or an aluminum silicon nitride layer, and/or an aluminum oxide layer, and/or an aluminum oxynitride layer, and/or hafnium oxide, and/or silicon oxynitride, and/or hafnium aluminum oxide.

[0127] Referring to Figure 11b-11c, a groove H11 at least partially through the dielectric layer is formed by etching the gate region of the dielectric layer. In the embodiment, fluorine-based plasma etching, for example, may be adopted in the etching process. Due to selective etching by the fluorine-based plasma etching treatment, the etching process stops when reaching the aluminum oxide layer 16 (or the aluminum oxynitride layer 16). The aluminum oxide layer 16 (or the aluminum oxynitride layer 16) and part or all of the cap layer 15 is etched by wet etching or dry etching, to form the groove H10.

[0128] Referring to Figure 11d, an additional dielectric layer 14 is deposited in the groove H11 formed by etching. Material of the additional dielectric layer 14 may include, for example, Al_2O_3 or AlON. The additional dielectric layer 14 may be grown by Atomic Layer Deposition, Chemical Vapor Deposition, Molecular Beam Epitaxy, Plasma Enhanced Chemical Vapor Deposition or Low Pressure Chemical Vapor Deposition, or a combination thereof. It should be understood that the methods for forming the additional dielectric layer described herein are merely for illustration. In the application, the additional dielectric layer may be formed by any method known to those skilled in the art. Material of the additional dielectric layer may also be selected from one or any combination of SiN, SiON, SiO_2 and HfO_2.

[0129] Referring to Figure 11e, p-type semiconductor material 9 is deposited on the additional dielectric layer 14 in the groove H11 formed by etching. The p-type semiconductor material 9 may be selected from p-type diamond, p-type NiO, p-type GaN, or p-type polycrystalline GaN, etc.

[0130] Referring to Figure 11f, the p-type semiconductor material 9 on the additional dielectric layer 14 except for the gate region is removed. In the embodiment, for example, the p-type semiconductor material 9 is p-type diamond, then the p-type diamond in the gate region is retained, and the p-type diamond in other region may be etched away with plasma. In this case, the p-type semiconductor material 9 is actually the gate of the enhancement mode switching device in the application. Conductivity of the gate can be improved with an additional conductive metal layer.

[0131] Referring to Figure 11g, the nitride transistor structure is exposed by etching the dielectric layer except for the gate region. In the embodiment, the nitride barrier layer 5 may be exposed, for example, by dry etching, or the nitride barrier layer 5 may even be etched through, to form two ohmic contact regions. Finally, a source electrode 10 is formed on one

ohmic contact region, and a drain electrode 11 is formed on the other ohmic contact region.

[0132] By the aforesaid embodiments, advantages of the enhancement mode switching device fabricated by the method for fabricating the enhancement mode switching device are as follows.

[0133] By forming a dielectric layer on a nitride transistor structure, forming a groove structure by locally thinning a gate region of the dielectric layer, and arranging p-type semiconductor material in the groove, an n-type conductive layer below the gate can be pinched off. Therefore, a gallium nitride enhancement mode switching device is achieved with a simple process, and the fabricated device is stable and reliable.

[0134] It should be understood that, although the specification is described by the embodiments, it is not indicates that each embodiment includes only one independent technical solution. The way of description is merely for clarity. Those skilled in the art should consider the specification as a whole. Solutions in various embodiments may be combined appropriately to form other embodiments understandable to those skilled in the art.

[0135] The series of detailed description listed above are merely detailed description for feasible embodiments of the application, which are not to limit the scope of the application.

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

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- EP2385544A2 [0010]

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- **KUMAR, V. et al.**Recessed 0.25 mm gate AlGaN/GaN HEMTs on SiC with high gate-drain breakdown voltage using ICP-RIEElectron. Lett., 2001, vol. 37, 1483-1485 [0005]

- **Y. CAI et al.**High-performance enhancement-mode AlGaN/GaN HEMTs using fluoride-based plasma treatmentIEEE Electron Lett., 2005, vol. 2, 7435-437 [0006]
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Patentkrav

1. Forbedringsmodusafbryderindretning, omfattende:
et substrat (1);
en nitridtransistorstruktur indrettet på substratet (1);
et dielektrisk lag (6), der er dannet på nitridtransistorstrukturen, hvor et portområde og to ohmske kontaktområder, der er anbragt på en respektiv side af portområdet, er defineret på det dielektriske lag (6), og hvert af de to ohmske kontaktområder går gennem det dielektriske lag (6);
en rille (H1), der er dannet i portområdet og delvist går gennem det dielektriske lag (6);
p-type-halvledermateriale (9), der er dannet i rillen (H1); og
en source-elektrode (10) og en drain-elektrode (11), der er anbragt ved de to ohmske kontaktområder,
hvor det dielektriske lag (6) omfatter et siliciumnitridlag og/eller et siliciumdioxidlag og/eller et aluminium-siliciumnitridlag og/eller et aluminium-oxidlag og/eller et aluminium-oxynitridlag og/eller hafniumoxid og/eller siliciumoxynitrid og/eller hafniumaluminiumoxid;
og hvor, i portområdet, nitridtransistorstrukturen ikke er udsat for p-type-halvledermaterialet.

2. Forbedringsmodusafbryderindretning ifølge krav 1, hvor nitridtransistorstrukturen omfatter:
et nitridnukleationlag (2), der er anbragt på substratet (1);
et nitridbufferlag (3), der er anbragt på nitridnukleationlaget (2); og
et nitridkanallag (4), der er anbragt på nitridbufferlaget (3).

3. Forbedringsmodusafbryderindretning ifølge krav 2, hvor nitridkanallaget (4) er ikke-doteret eller n-type-doteret.

4. Forbedringsmodusafbryderindretning ifølge krav 2, hvor nitridtransistorstrukturen endvidere omfatter et nitridbarrierelag (5), der er indrettet på nitridkanallaget (4).

5. Forbedringsmodusafbryderindretning ifølge krav 4, hvor nitridtransistorstrukturen endvidere omfatter et nitriddæklag (15), der er dannet på nitridbarrierelaget (5).

6. Forbedringsmodusafbryderindretning ifølge krav 5, hvor nitriden i nitriddæklaget (15) er galliumnitrid eller aluminiumgalliumnitrid.

7. Forbedringsmodusafbryderindretning ifølge krav 1, hvor p-type-halvledermaterialet (9) er udvalgt blandt p-type-diamant, p-type-NiO, p-type-GaN eller p-type-polykrystallinsk GaN.

8. Forbedringsmodusafbryderindretning ifølge krav 1, yderligere omfattende et ledende metallag, der er dannet på p-type-halvledermaterialet (9).

9. Fremgangsmåde til at fremstille en forbedringsmodusafbryderindretning, omfattende følgende trin:
at tilvejebringe et substrat (1) og danne en nitridtransistorstruktur på substratet (1);
at danne et dielektrisk lag (6) på nitridtransistorstrukturen, hvor et portområde er defineret på det dielektriske lag (6);
i portområdet at danne en rille (H1), der strækker sig mod nitridtransistorstrukturen, hvor rillen (H1) delvist går gennem det dielektriske lag (6);
at afsætte p-type-halvledermateriale (9) i rillen (H1);
at ætse det dielektriske lag (6) for at danne to ohmske kontaktområder, der er anbragt på en respektiv side af portområdet, hvor hvert af de to ohmske kontaktområder går gennem det dielektriske lag (6); og
at danne en source-elektrode (10) og en drain-elektrode (11) ved de to ohmske kontaktområder,
hvor det dielektriske lag (6) omfatter et siliciumnitridlag og/eller et siliciumdioxidlag og/eller et aluminium-siliciumnitridlag og/eller et aluminium-oxidlag og/eller et aluminium-oxynitridlag og/eller hafniumoxid og/eller siliciumoxynitrid og/eller hafnium-aluminiumoxid;
og hvor, i portområdet, nitridtransistorstrukturen ikke er udsat for p-type-halvledermaterialet.

10. Fremgangsmåde til at fremstille forbedringsmodusafbryderindretningen ifølge krav 9, yderligere omfattende at danne et ledende metallag på p-type-halvledermaterialet (9) efter dannelse af p-type-halvledermaterialet (9) i rillen (H1, H2).

11. Fremgangsmåde til at fremstille forbedringsmodusafbryderindretningen ifølge krav 9, hvor trinnet med at danne nitridtransistorstrukturen omfatter:
at danne et nitridnukleationlag (2) på substratet (1);
at danne et nitridbufferlag (3) på nitridnukleationlaget (2); og
at danne et nitridkanallag (4) på nitridbufferlaget (3), hvor nitridkanallaget (4) er ikke-doteret eller n-type-doteret; og
at danne et nitridbarrierelag (5) på nitridkanallaget (4).

DRAWINGS

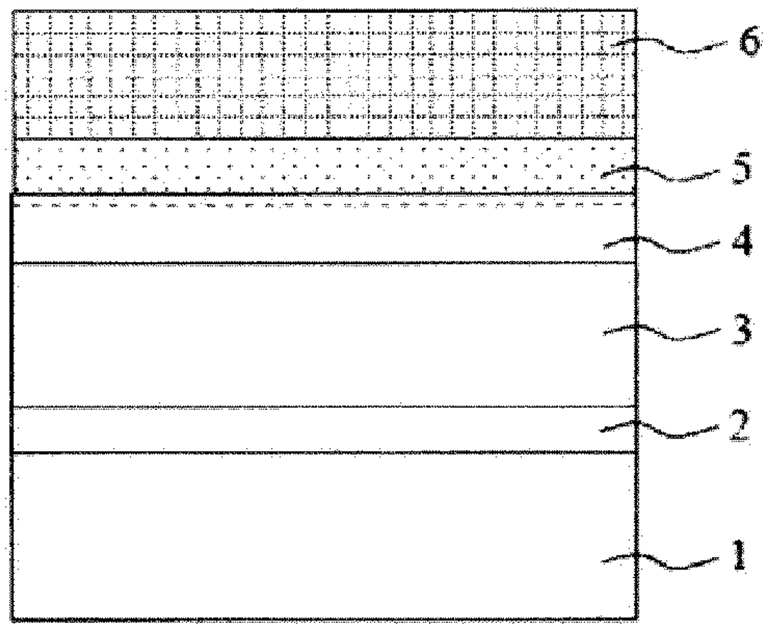

FIG.1a

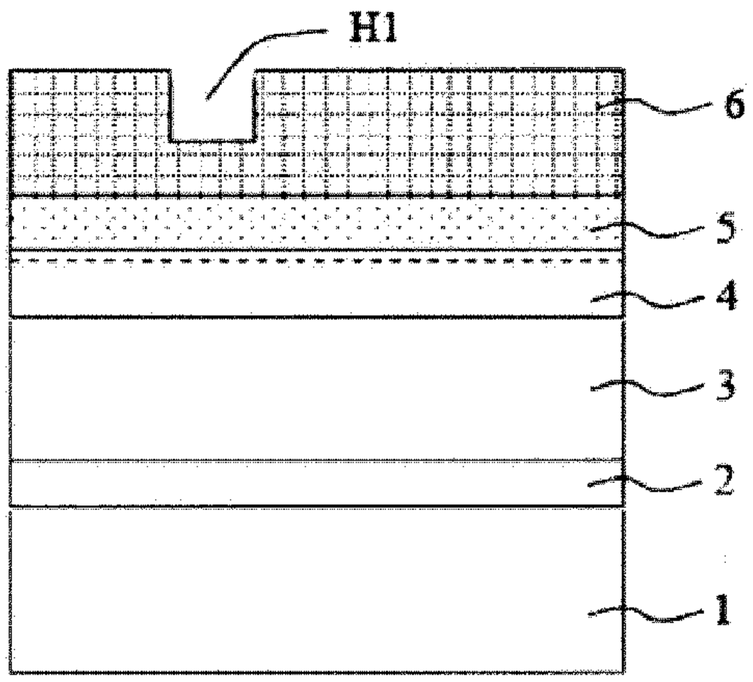

FIG.1b

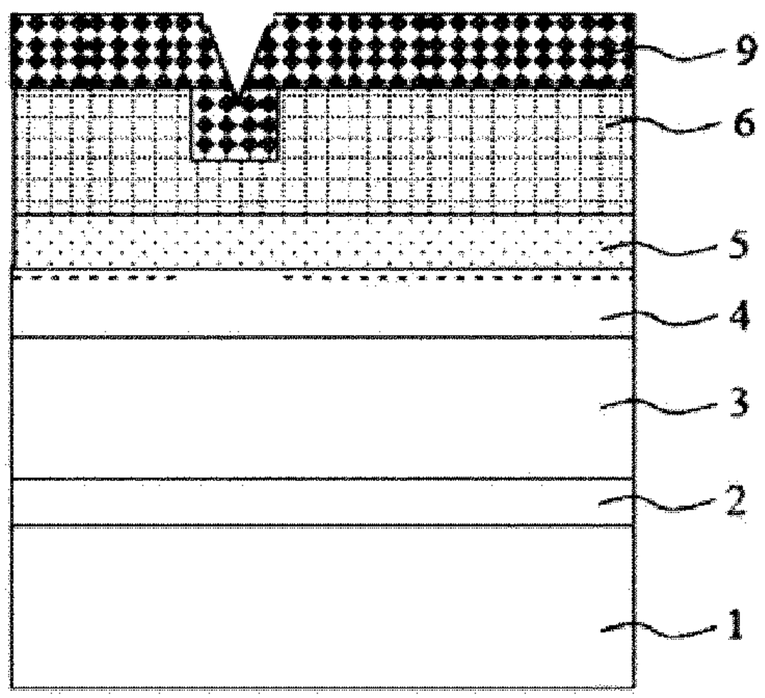

FIG.1c

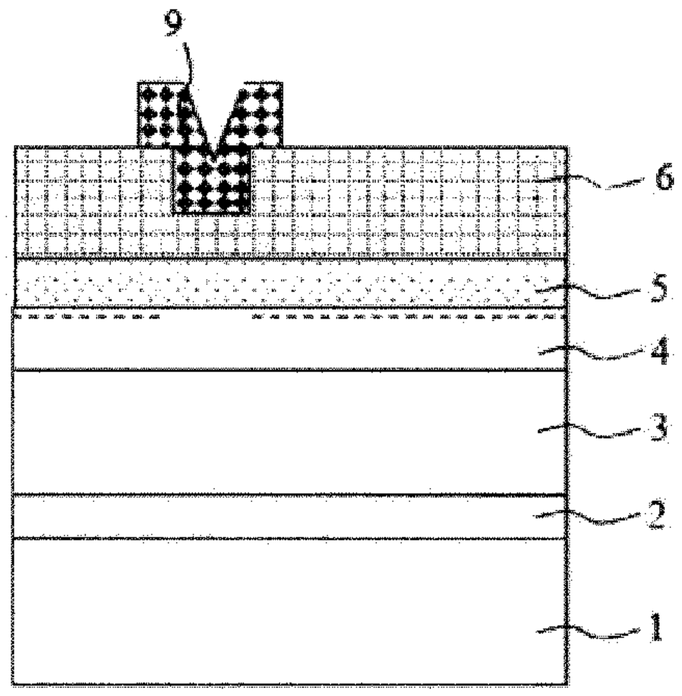

FIG.1d

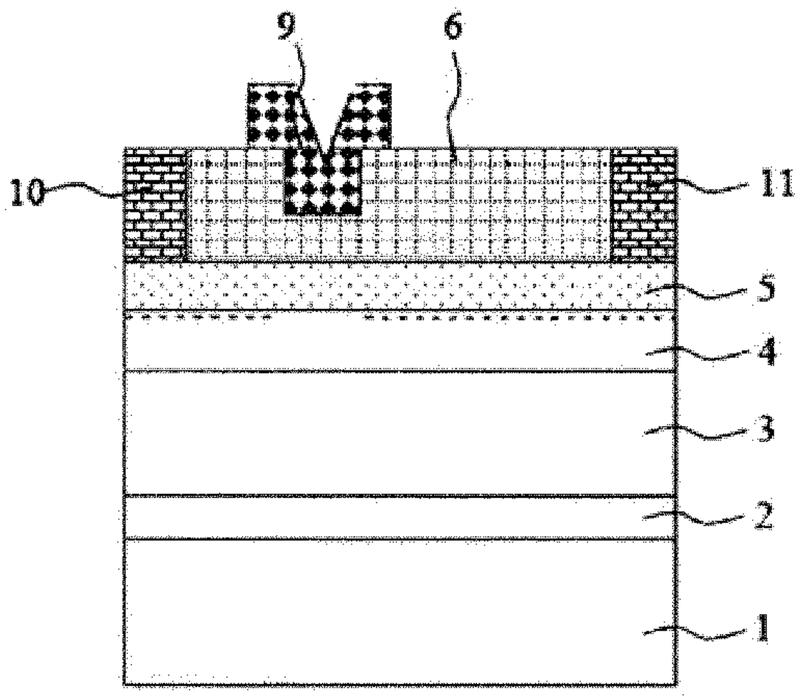

FIG.1e

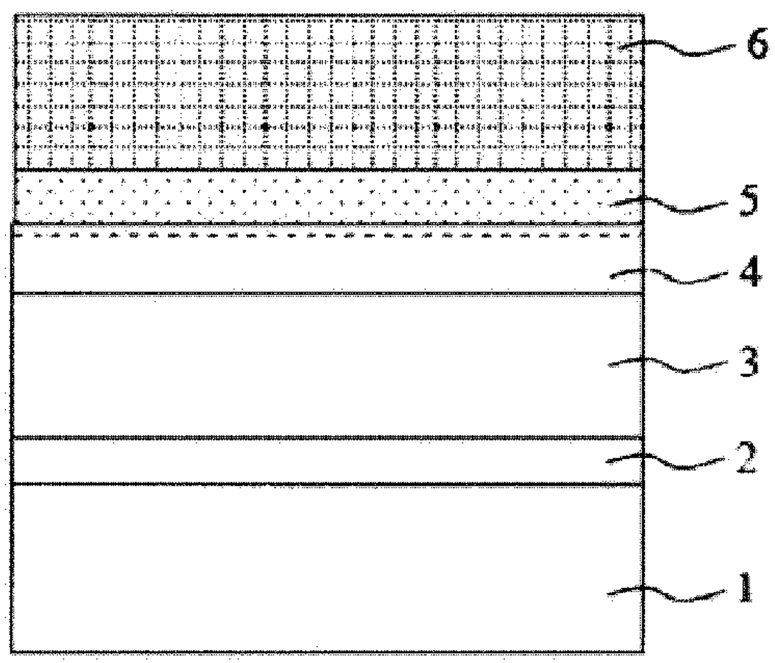

FIG.2a

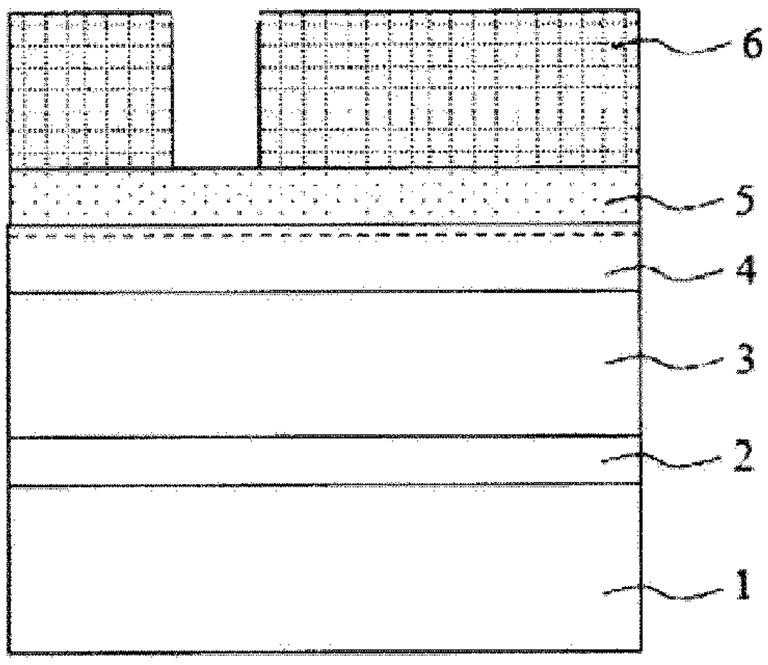

FIG.2b

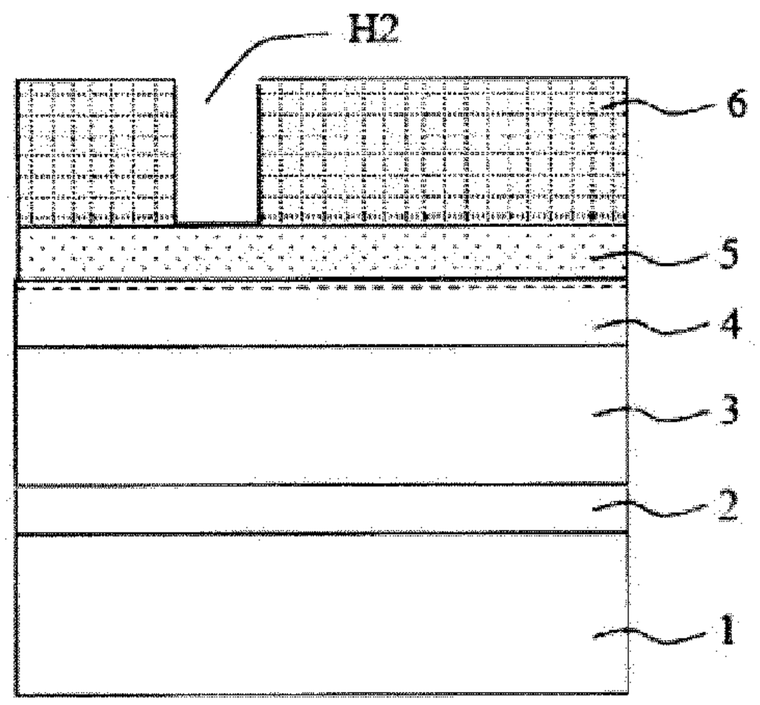

FIG.2c

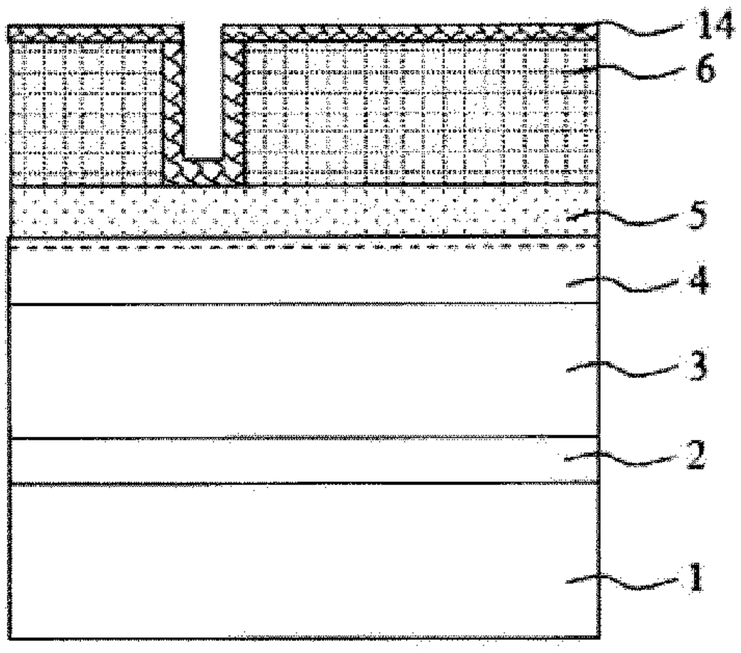

FIG.2d

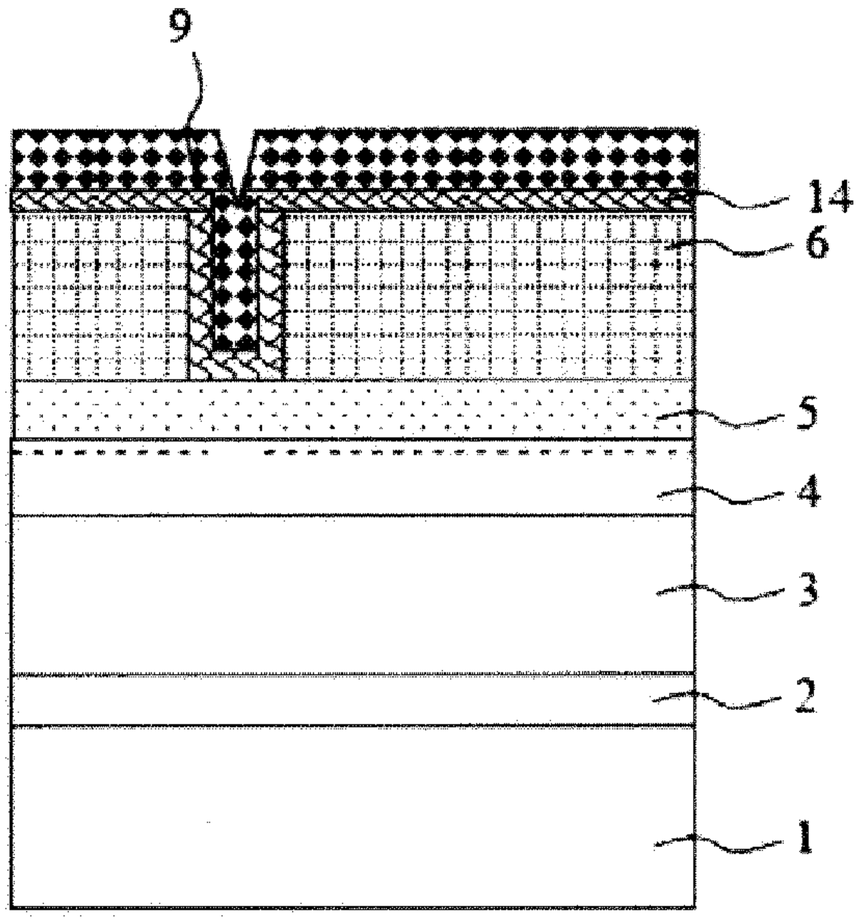

FIG.2e

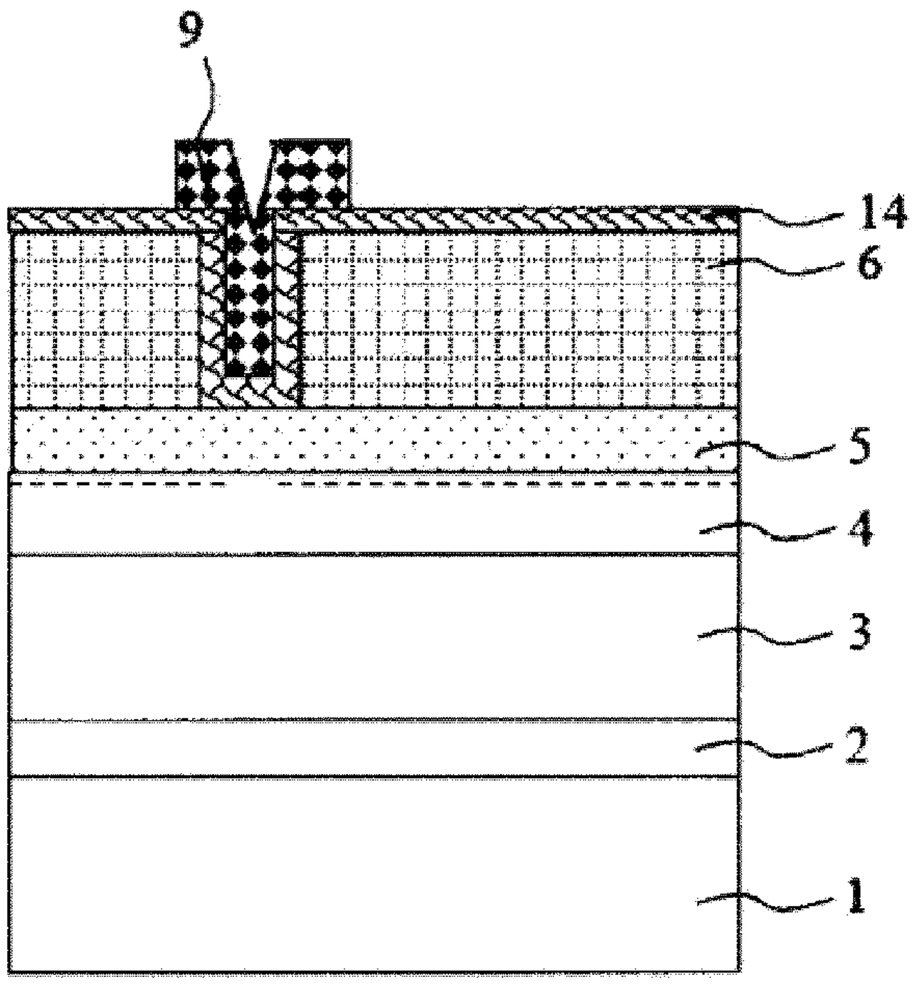

FIG.2f

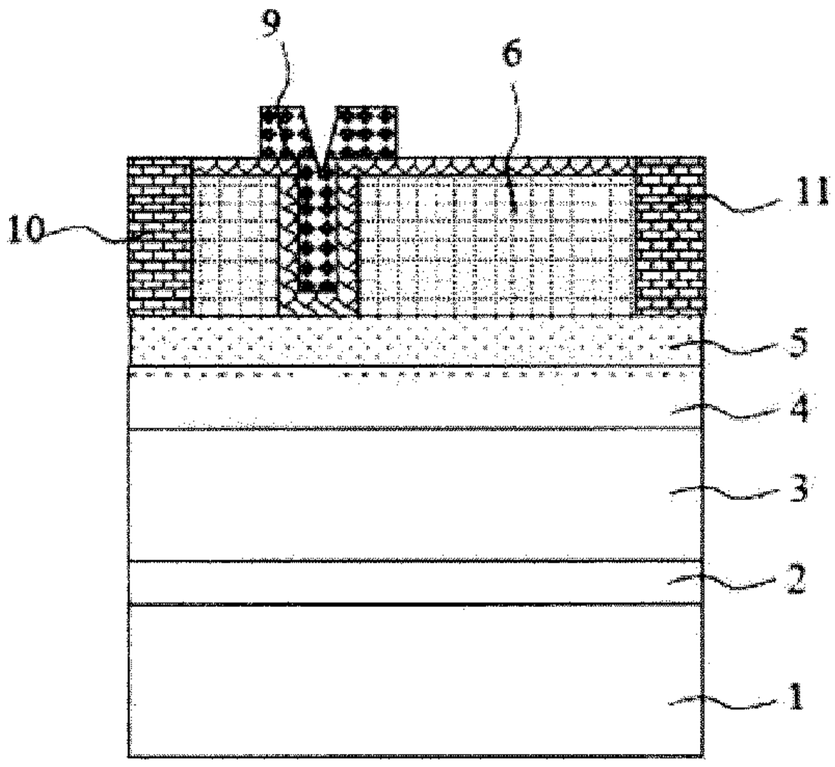

FIG.2g

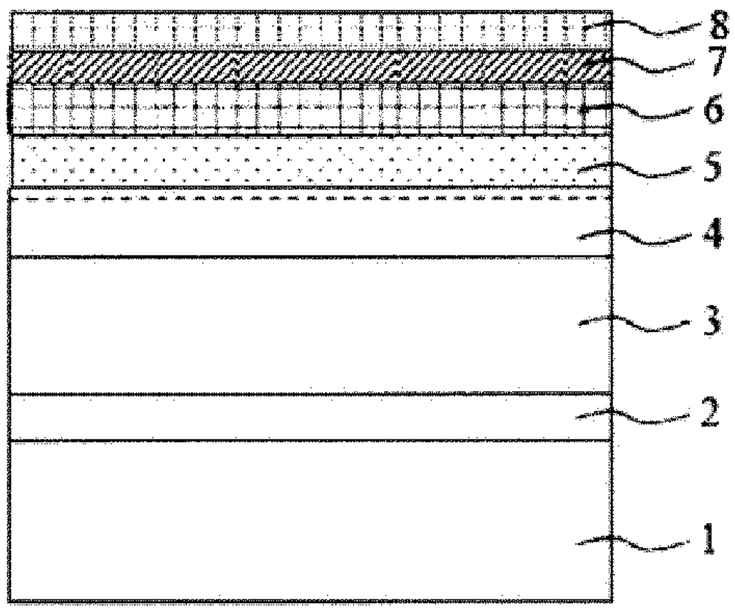

FIG.3a

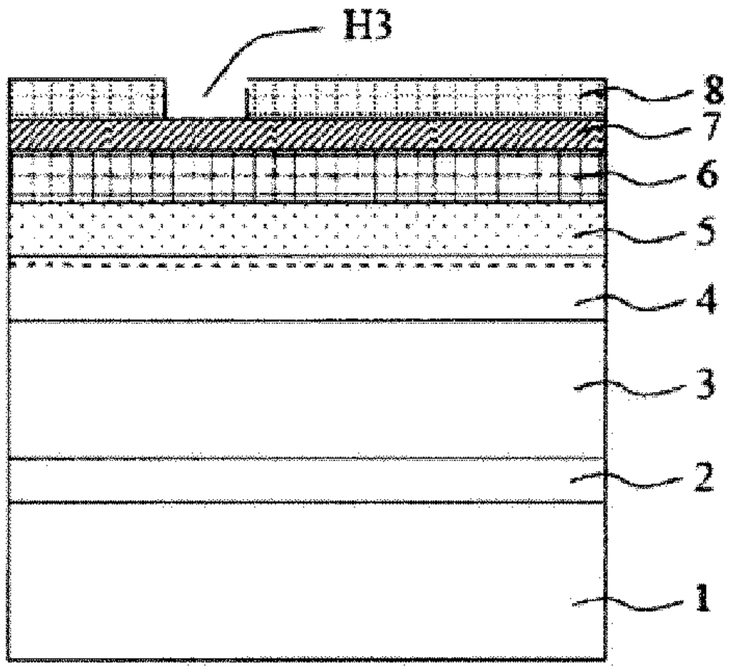

FIG.3b

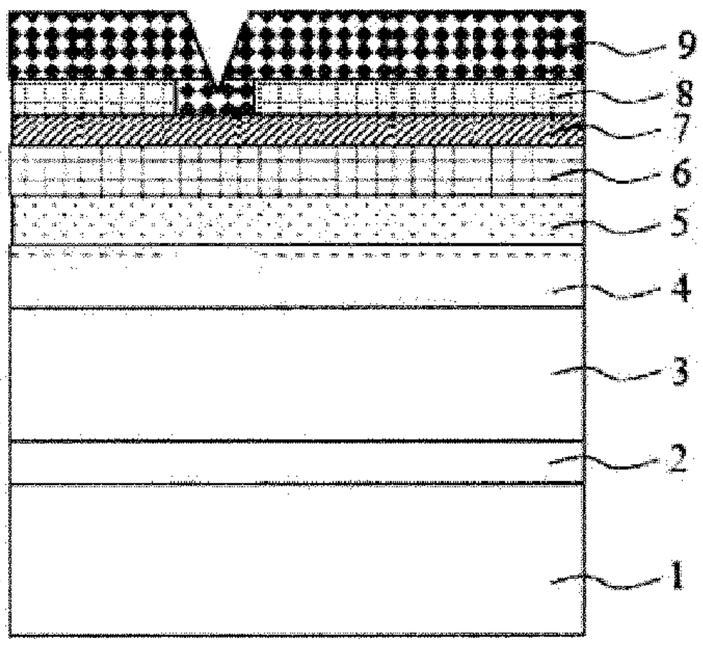

FIG.3c

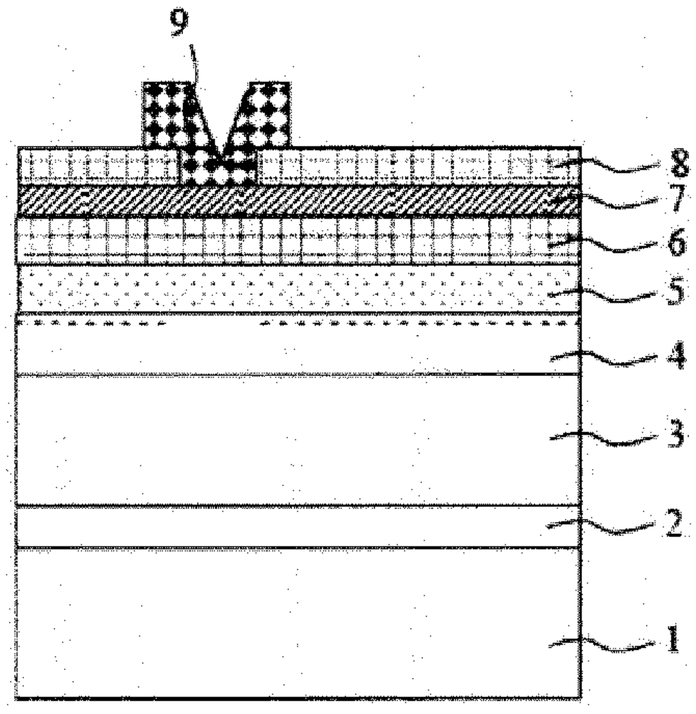

FIG.3d

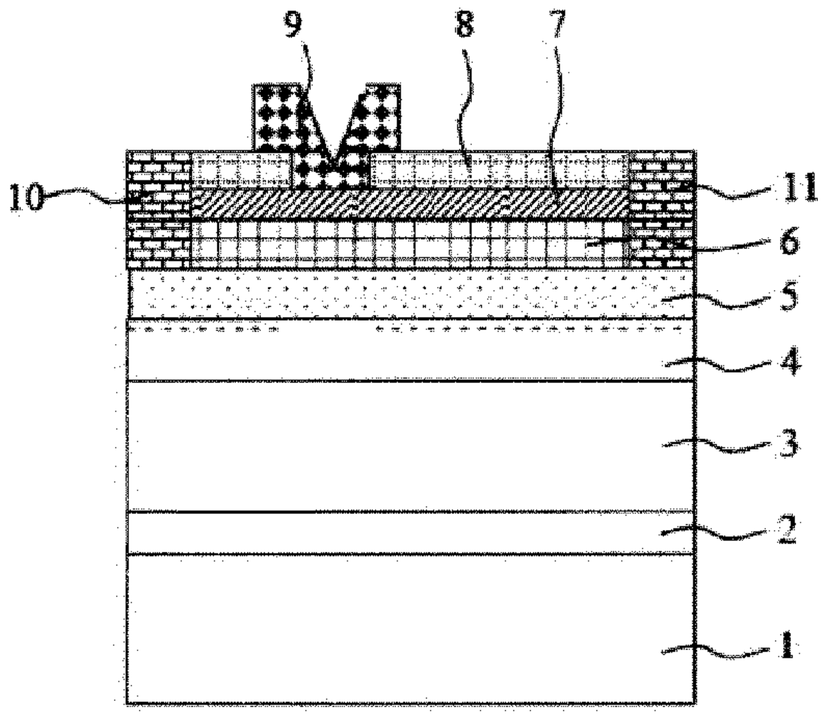

FIG.3e

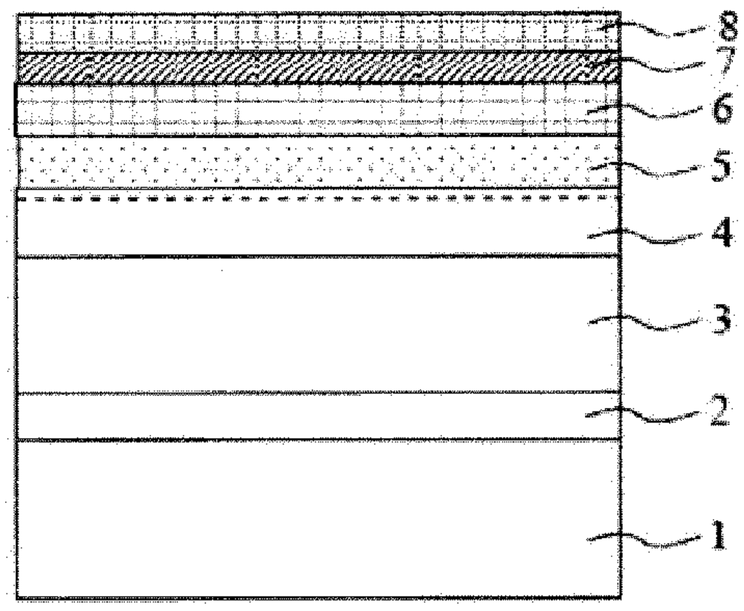

FIG.4a

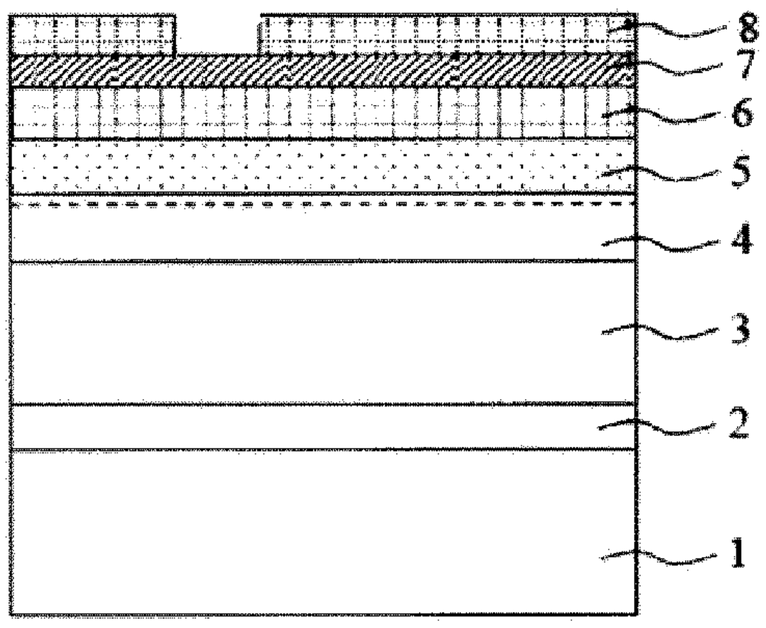

FIG.4b

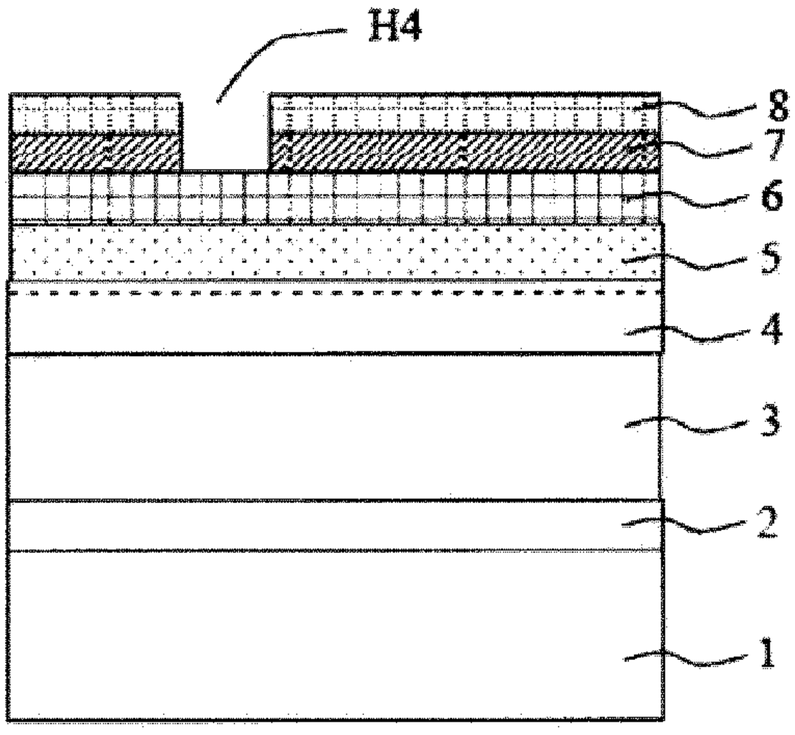

FIG.4c

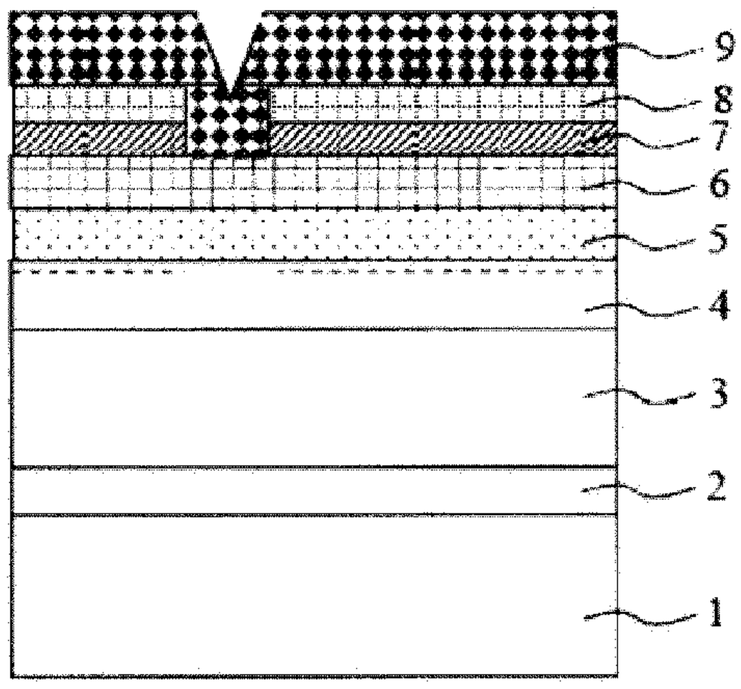

FIG.4d

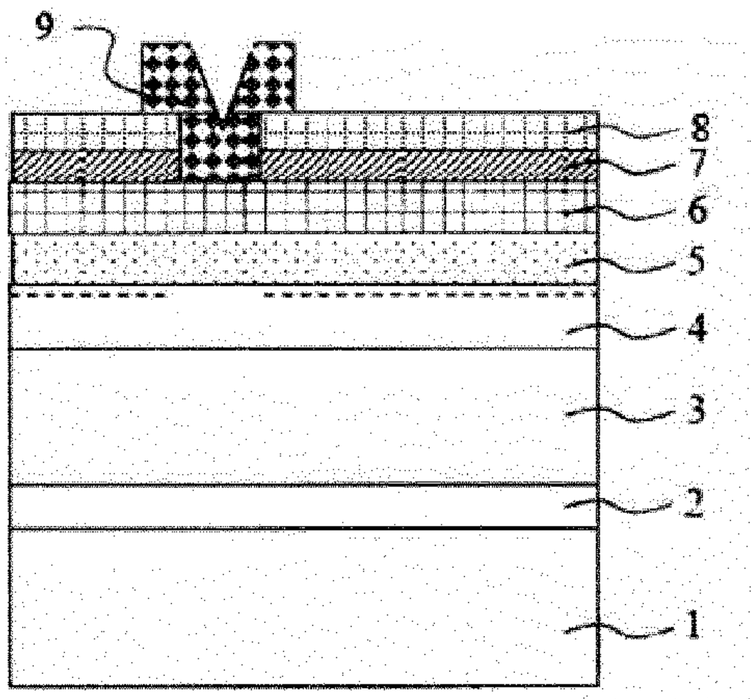

FIG.4e

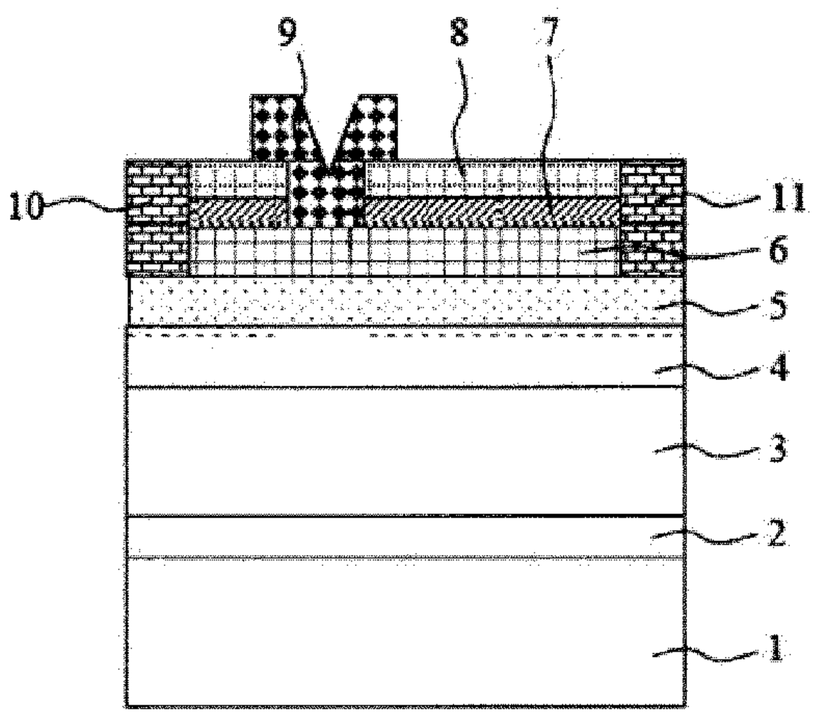

FIG.4f

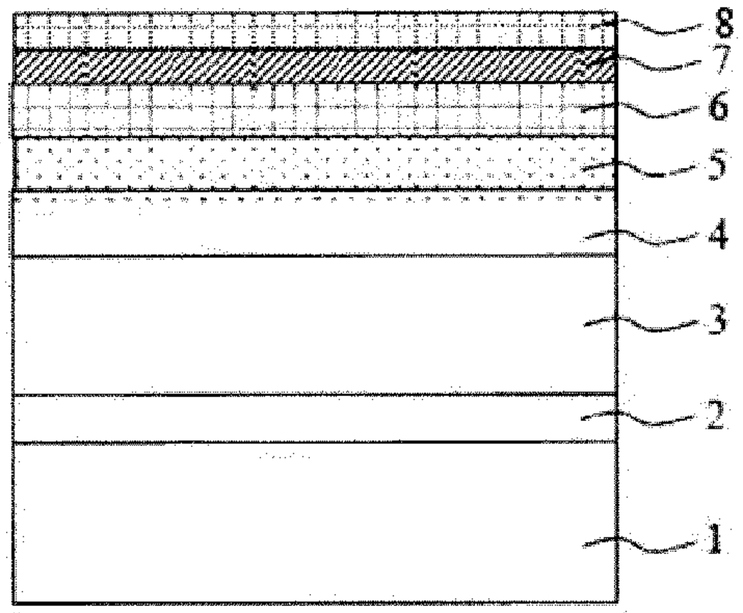

FIG.5a

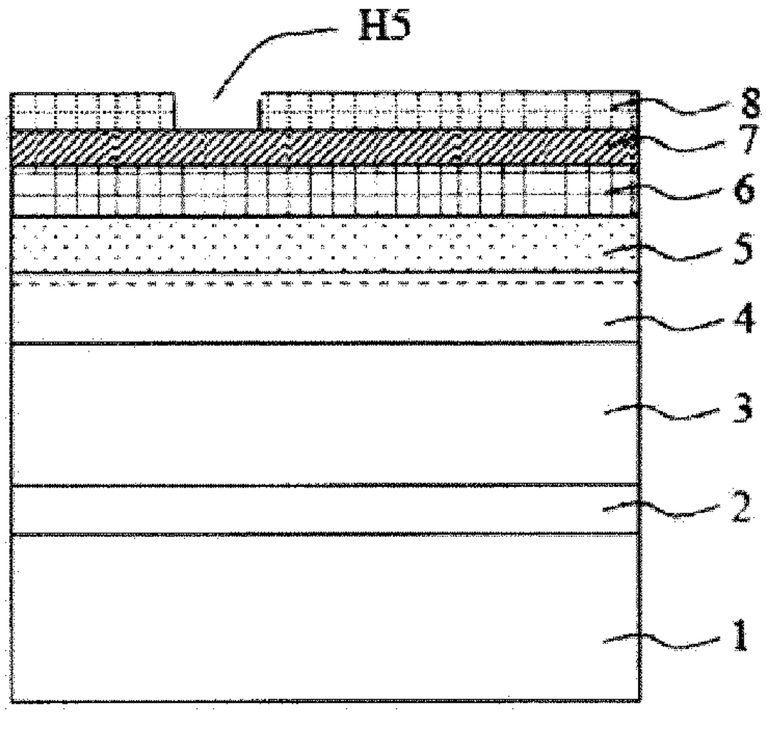

FIG.5b

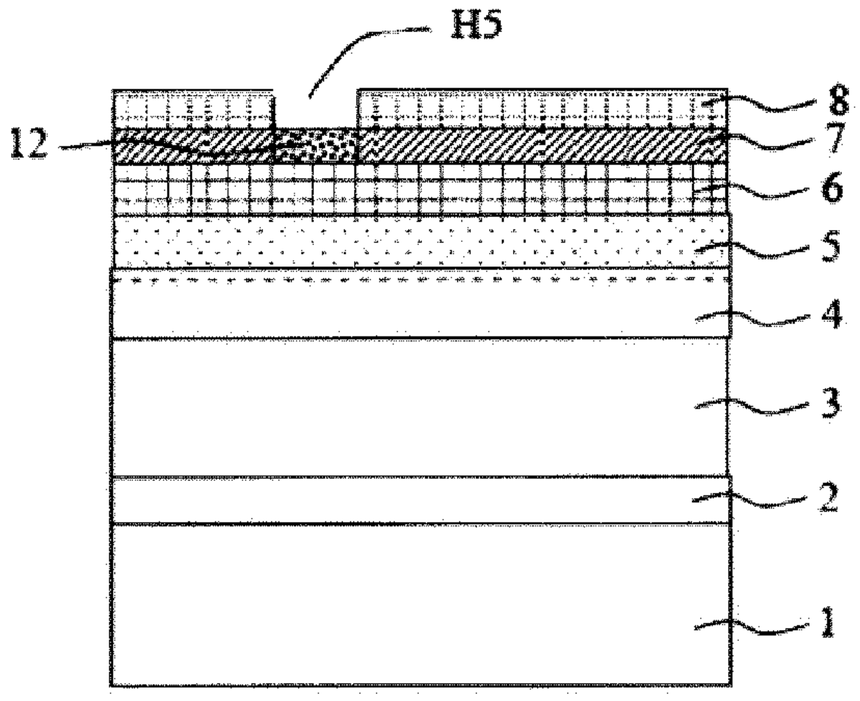

FIG.5c

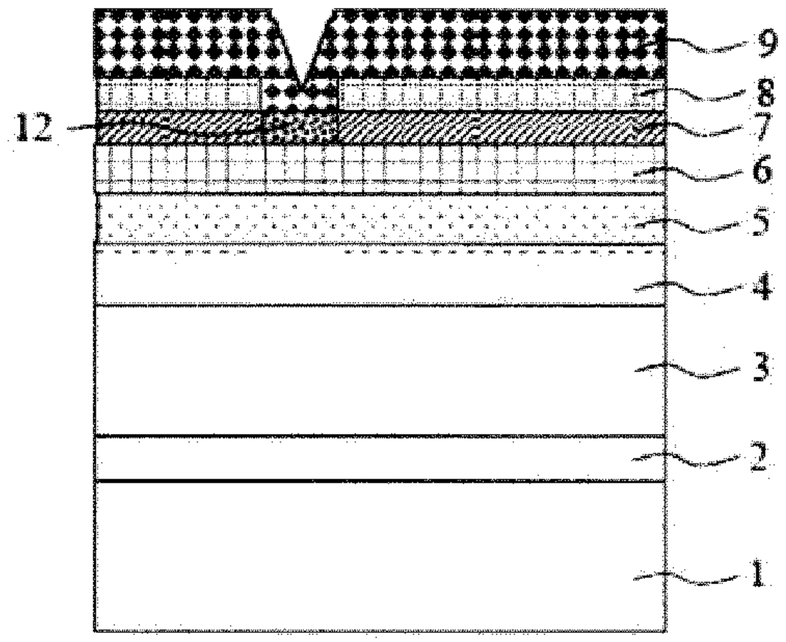

FIG.5d

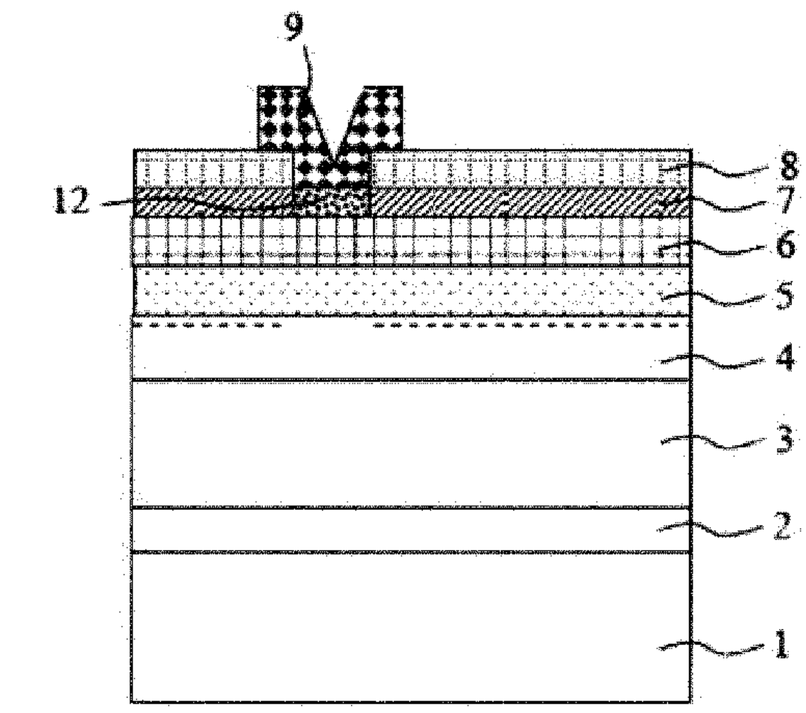

FIG.5e

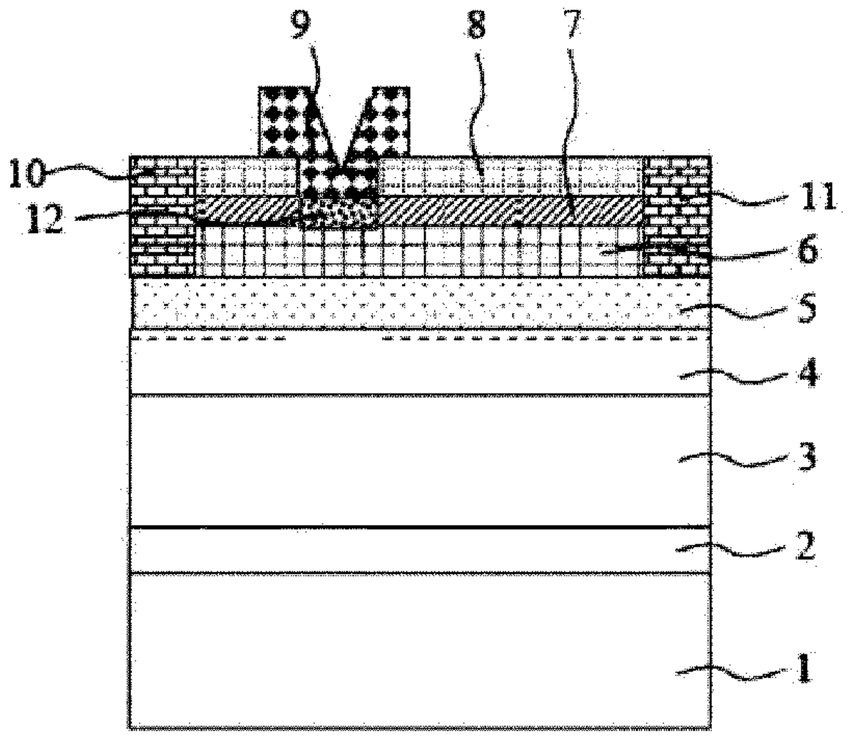

FIG.5f

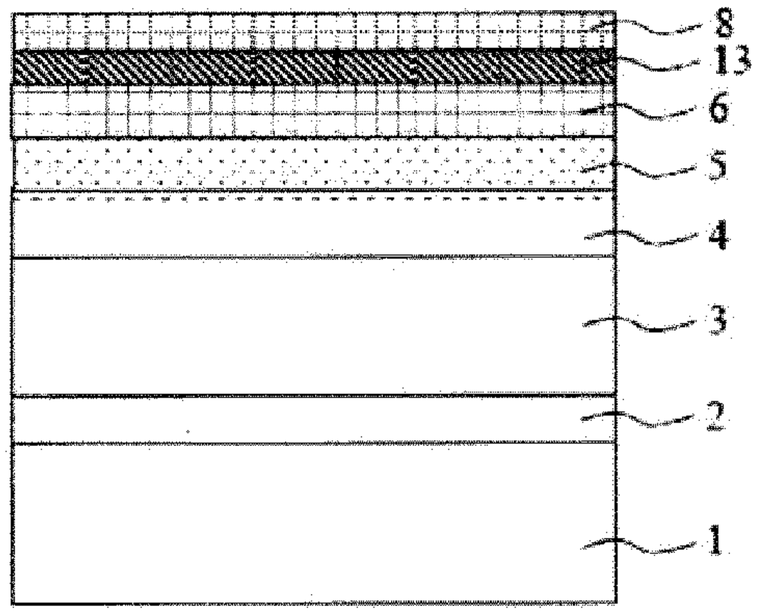

FIG.6a

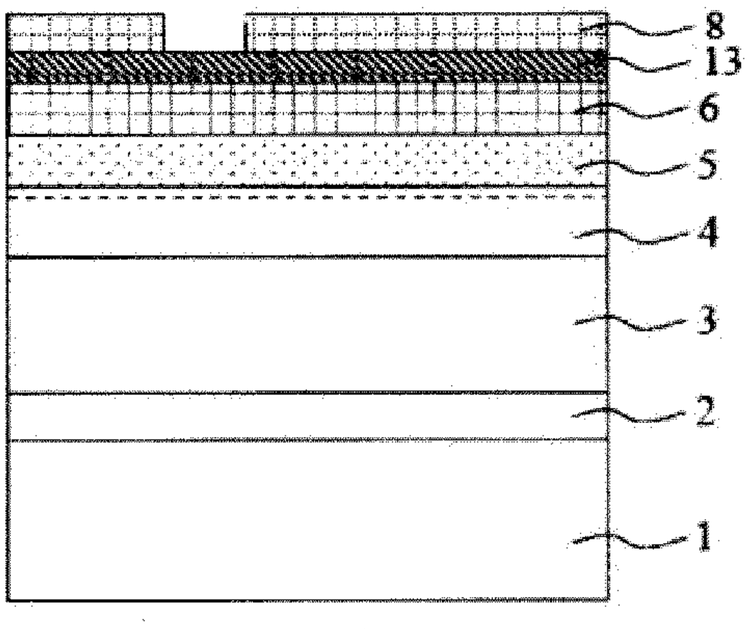

FIG.6b

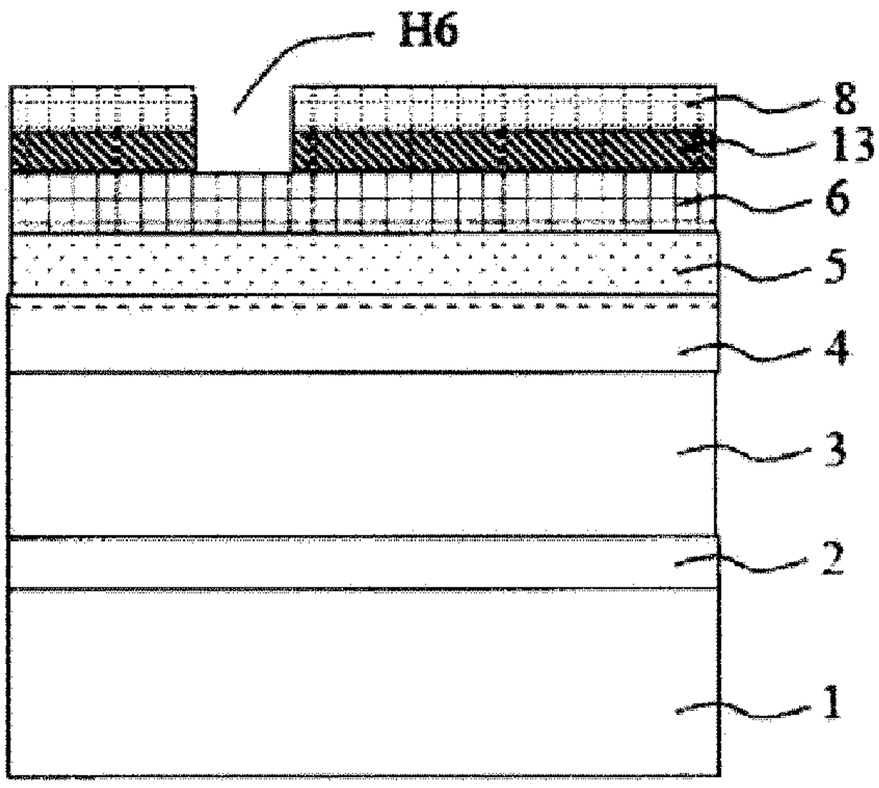

FIG.6c

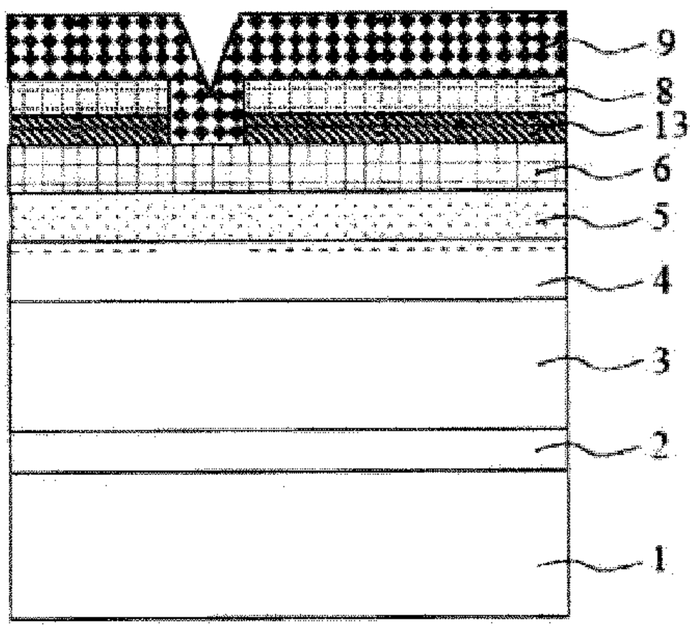

FIG.6d

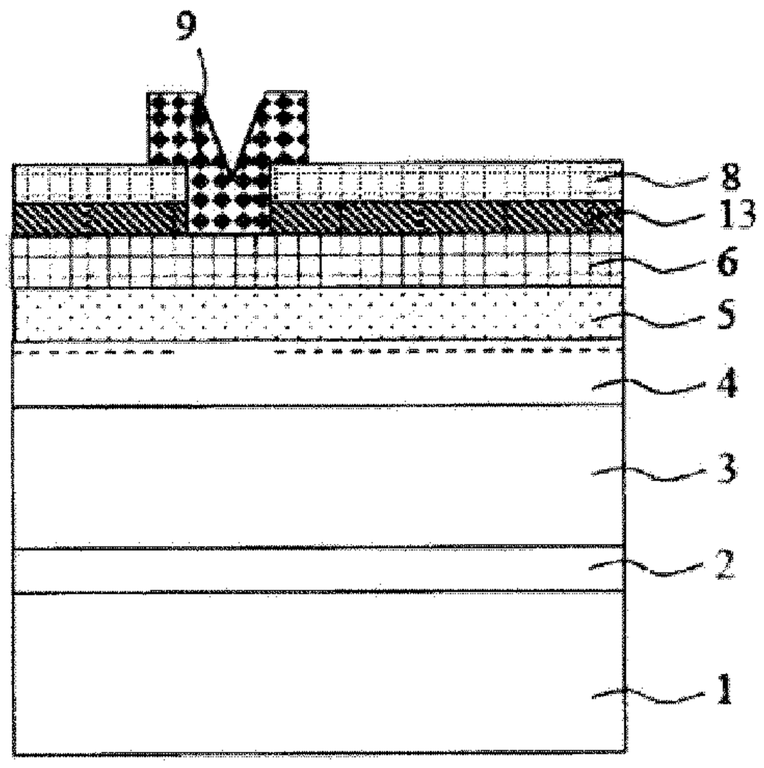

FIG.6e

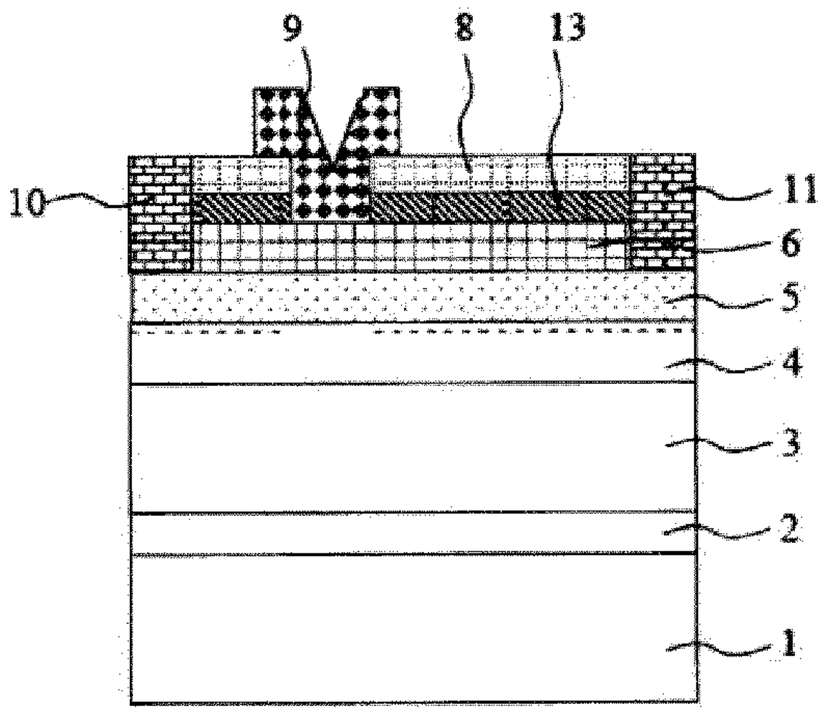

FIG.6f

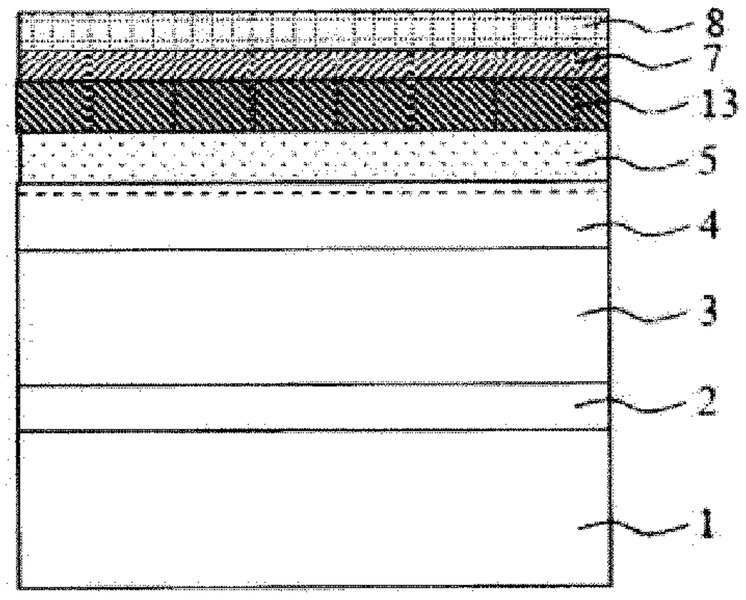

FIG.7a

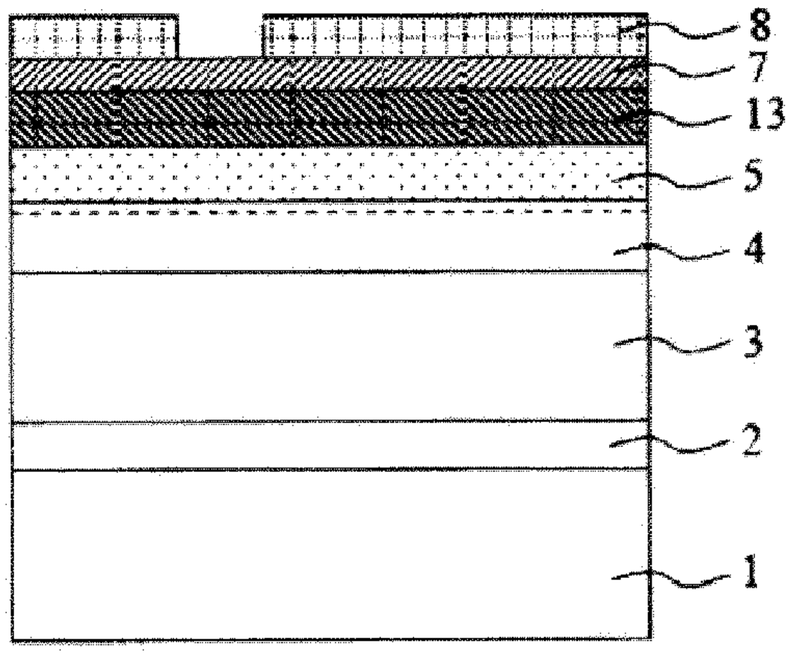

FIG.7b

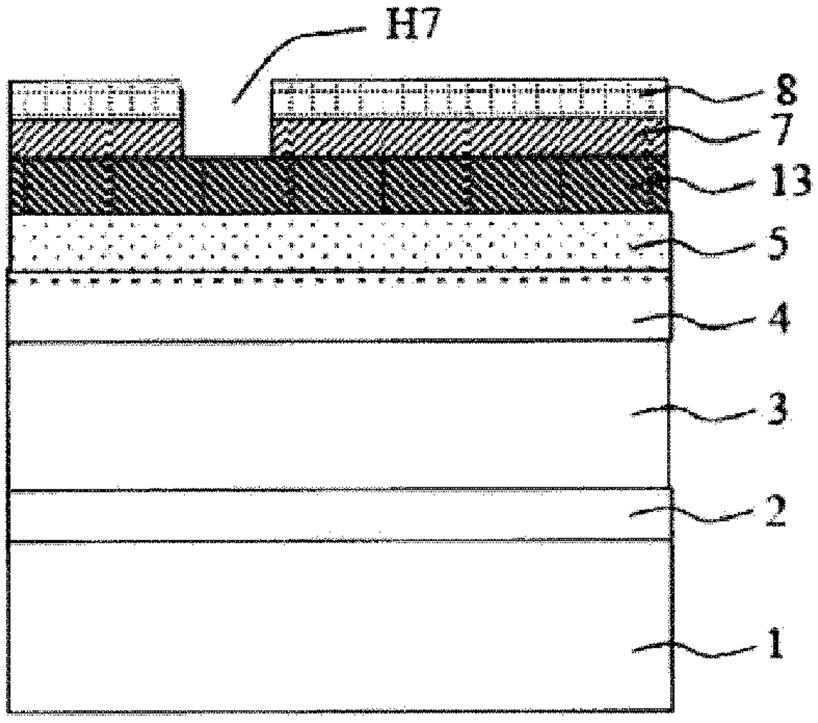

FIG.7c

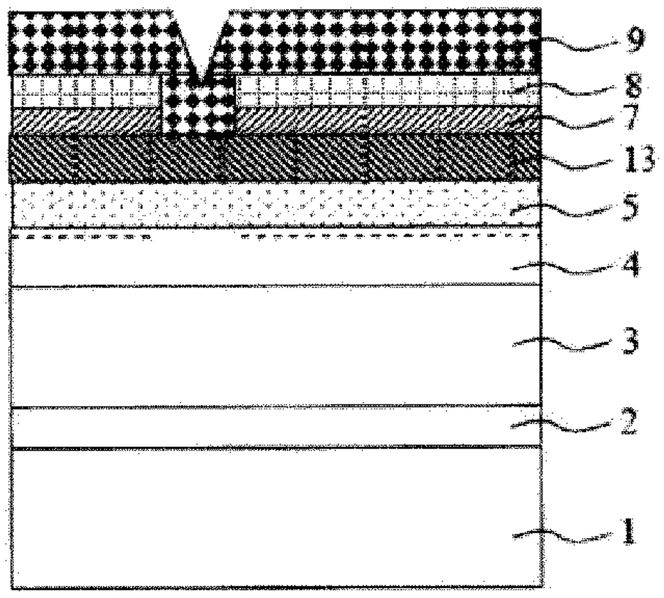

FIG.7d

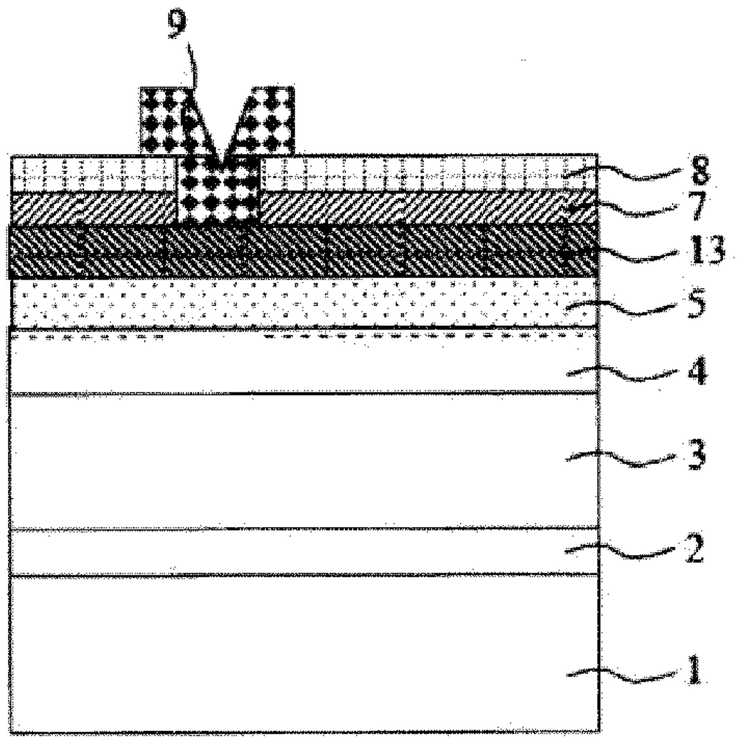

FIG.7e

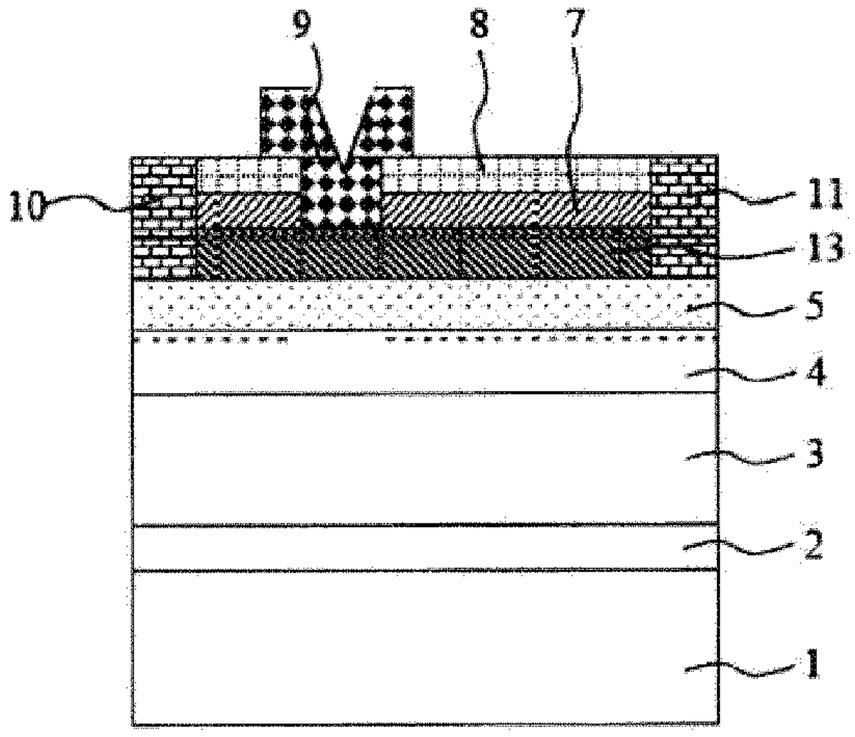

FIG.7f

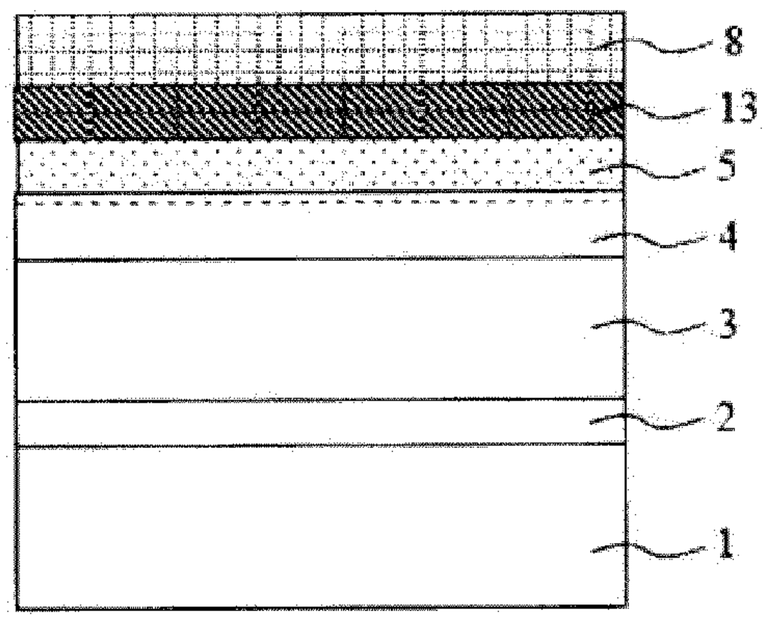

FIG.8a

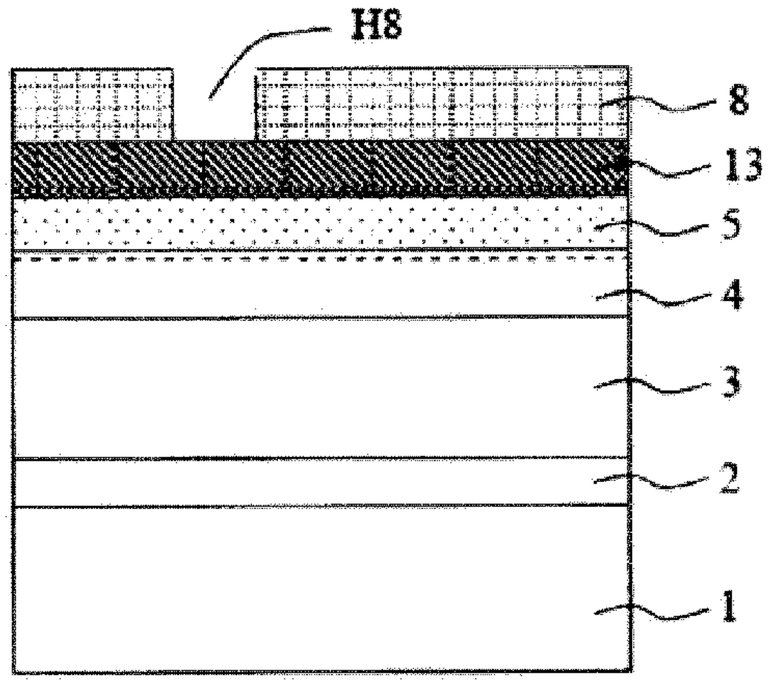

FIG.8b

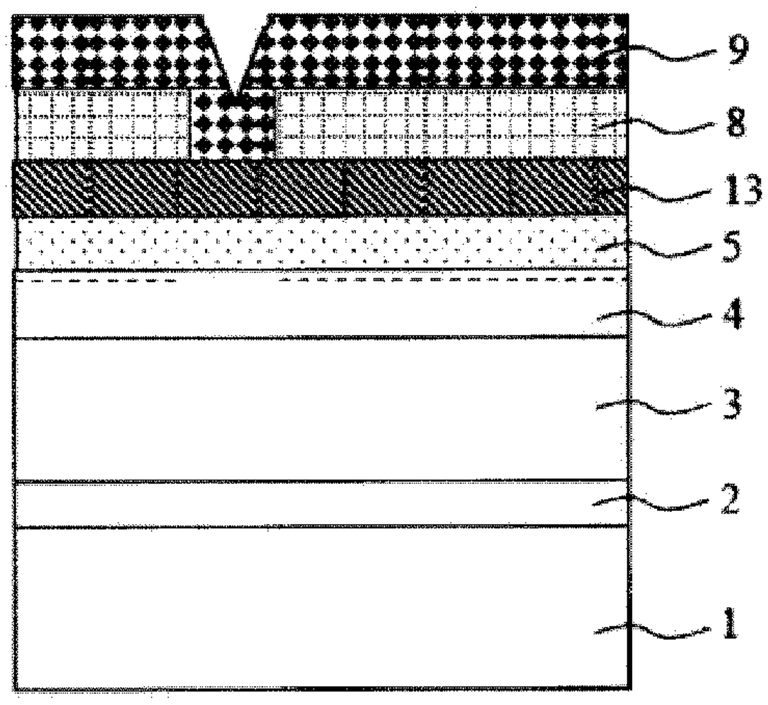

FIG.8c

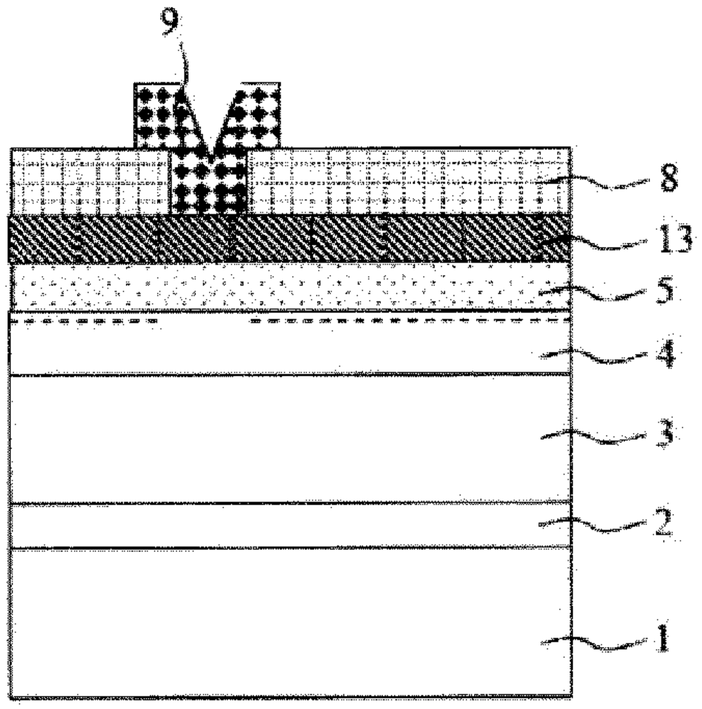

FIG.8d

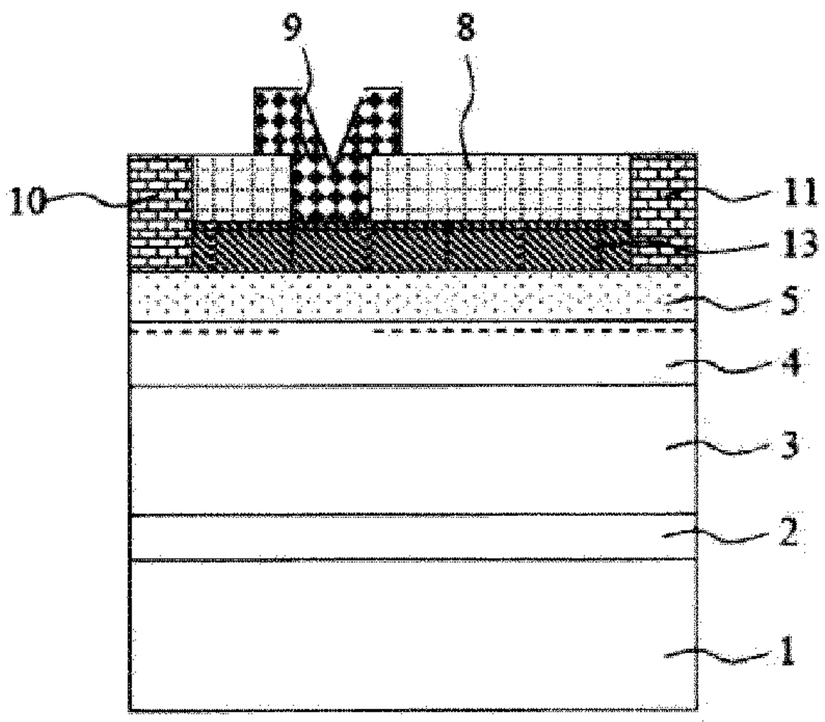

FIG.8e

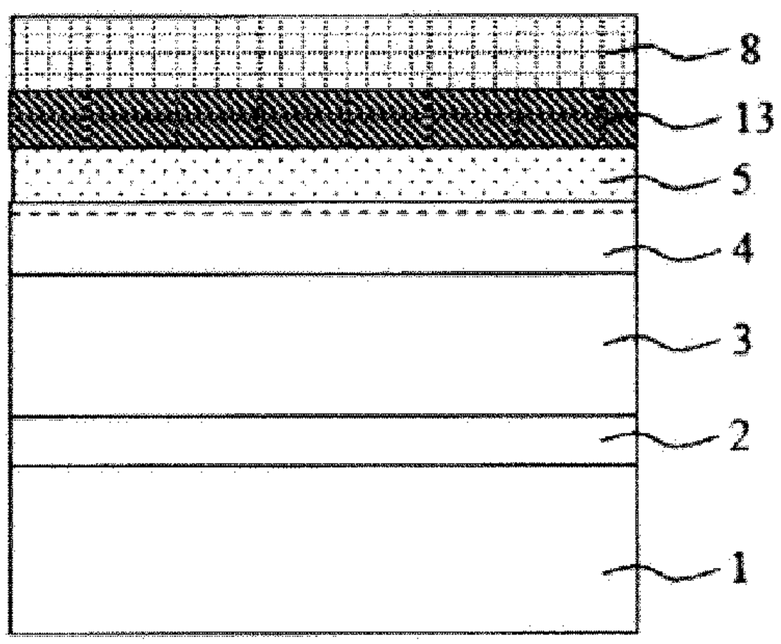

FIG.9a

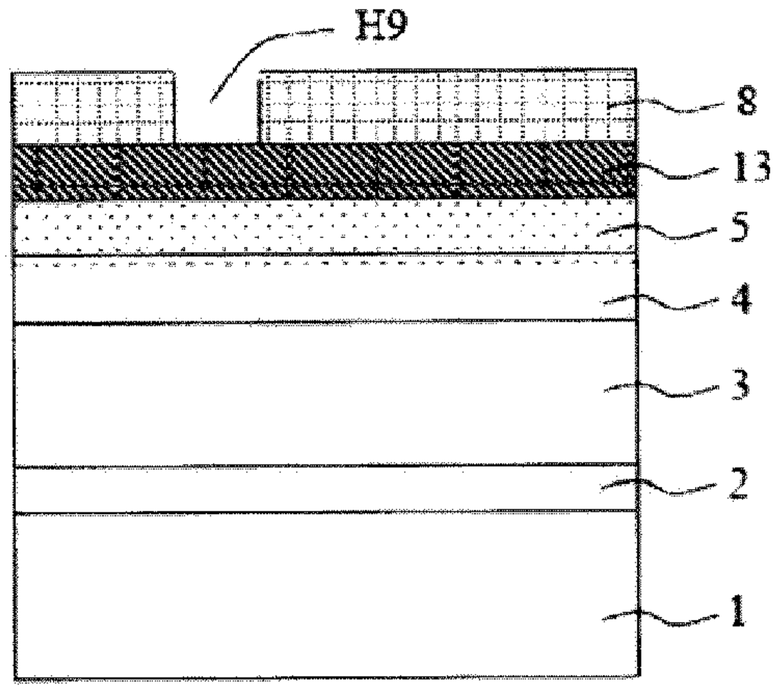

FIG.9b

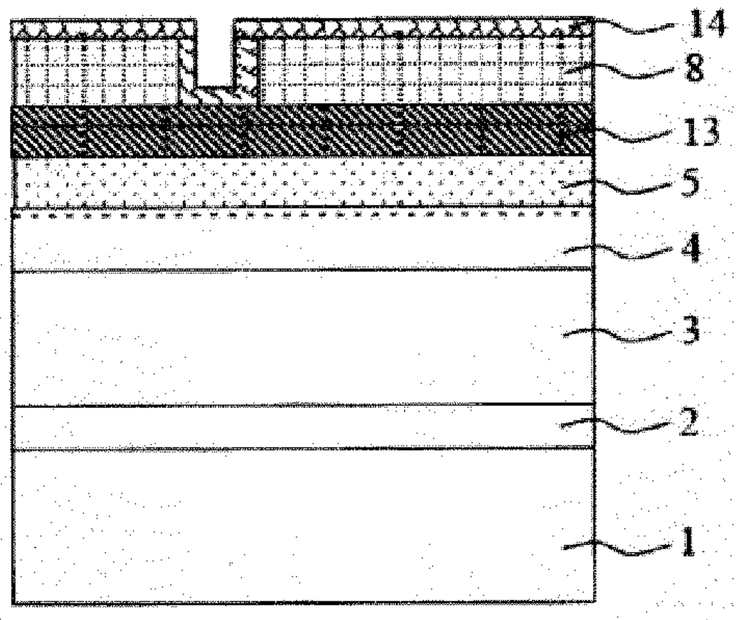

FIG.9c

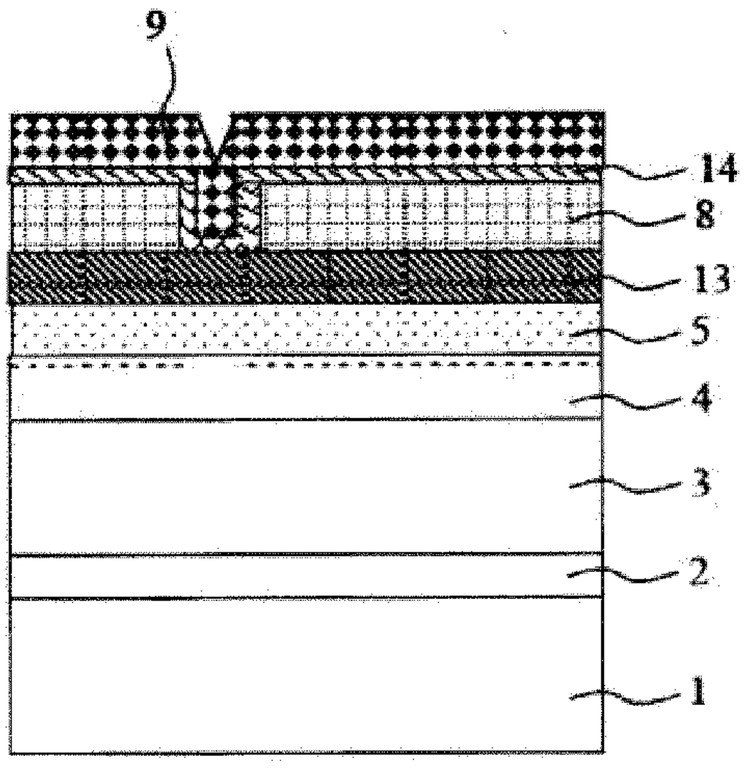

FIG.9d

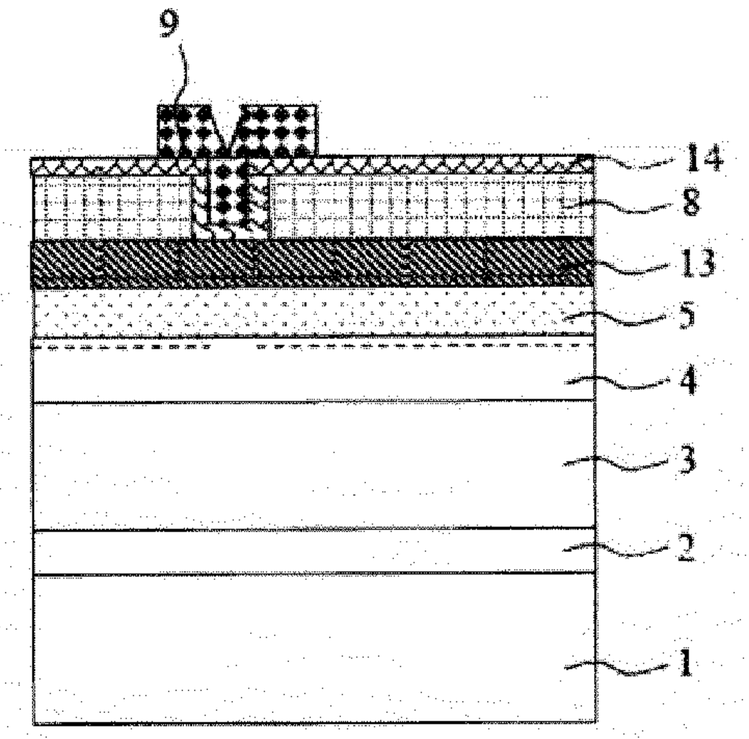

FIG.9e

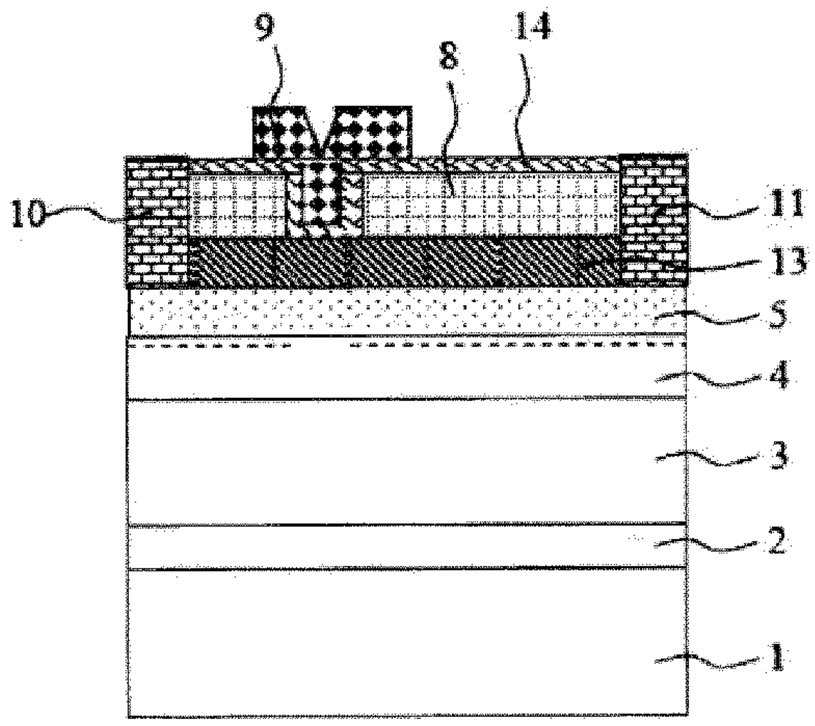

FIG.9f

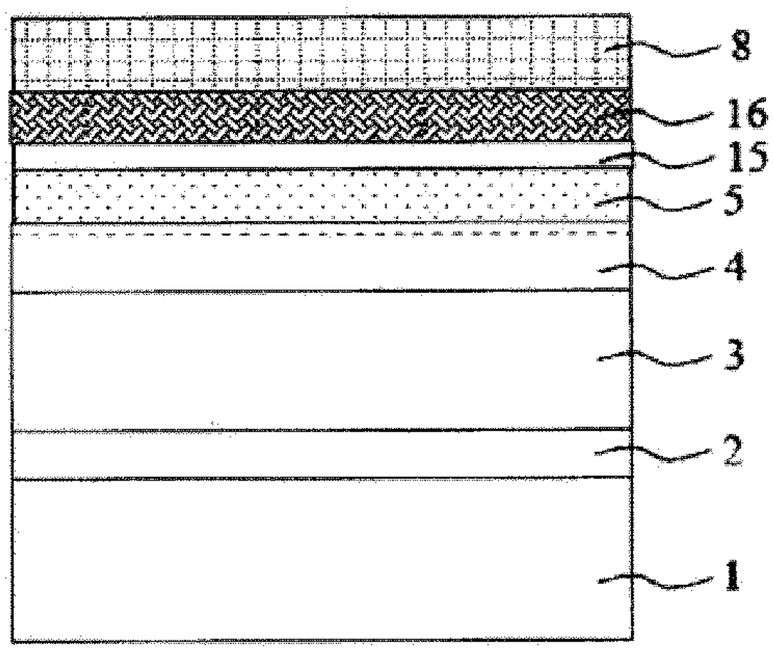

FIG.10a

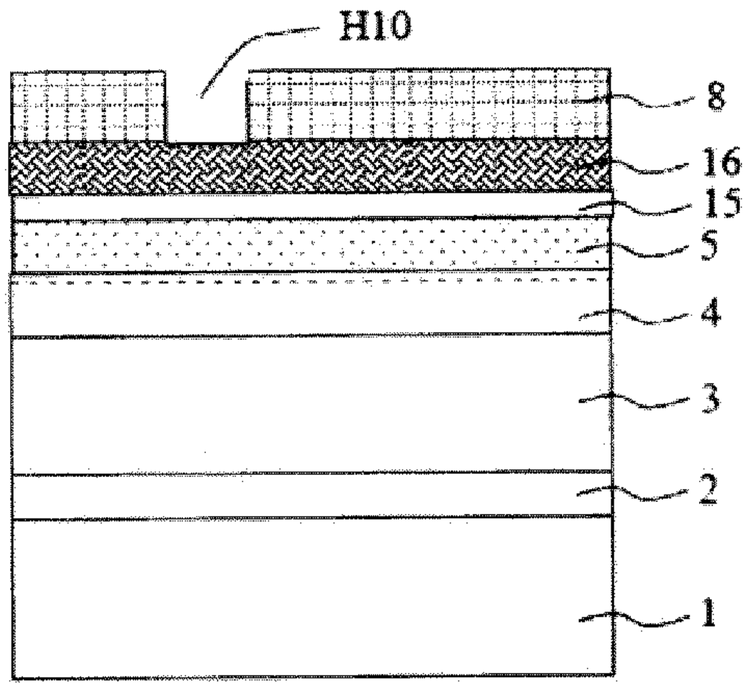

FIG.10b

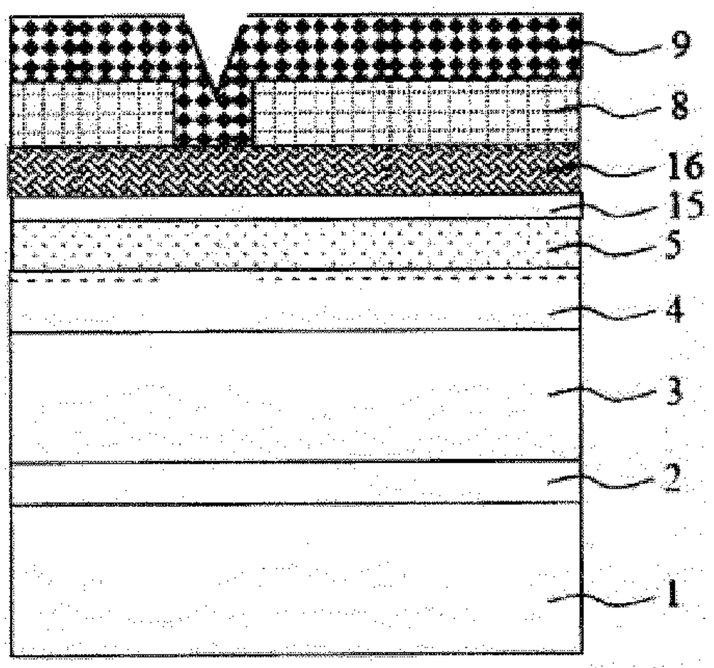

FIG.10c

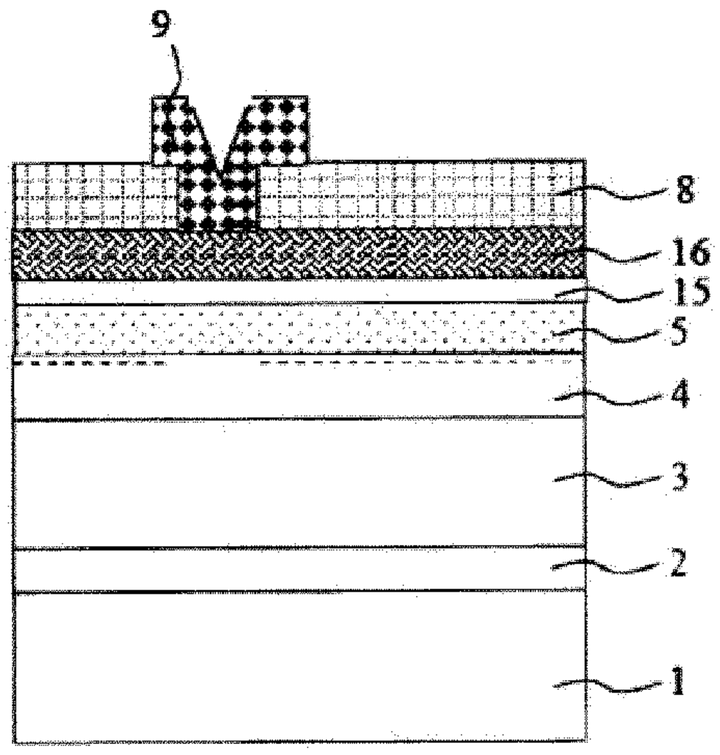

FIG.10d

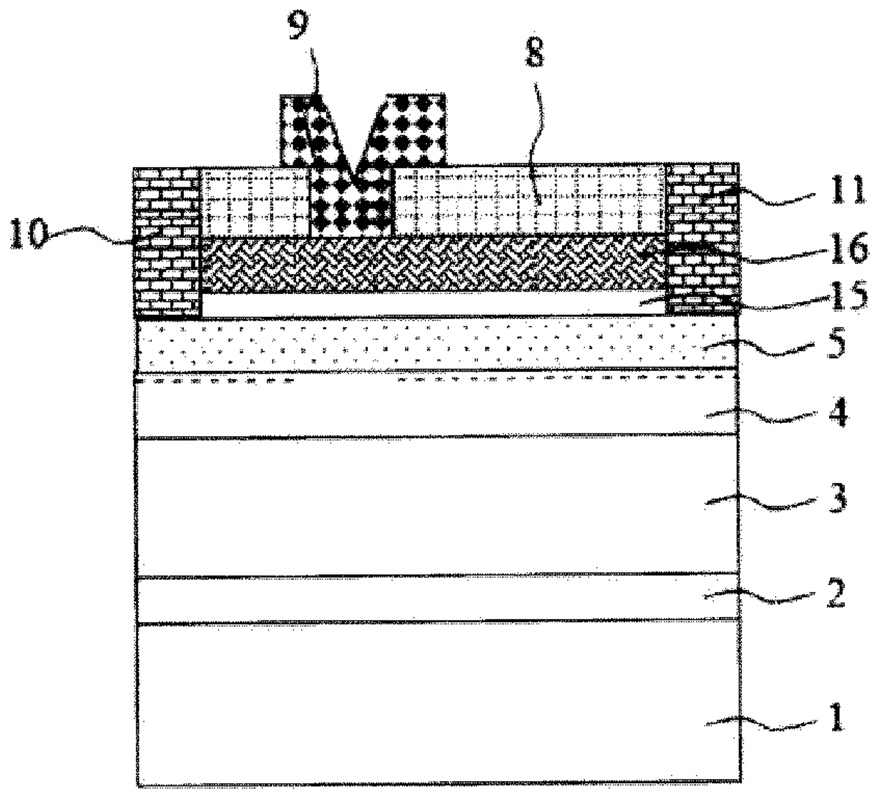

FIG.10e

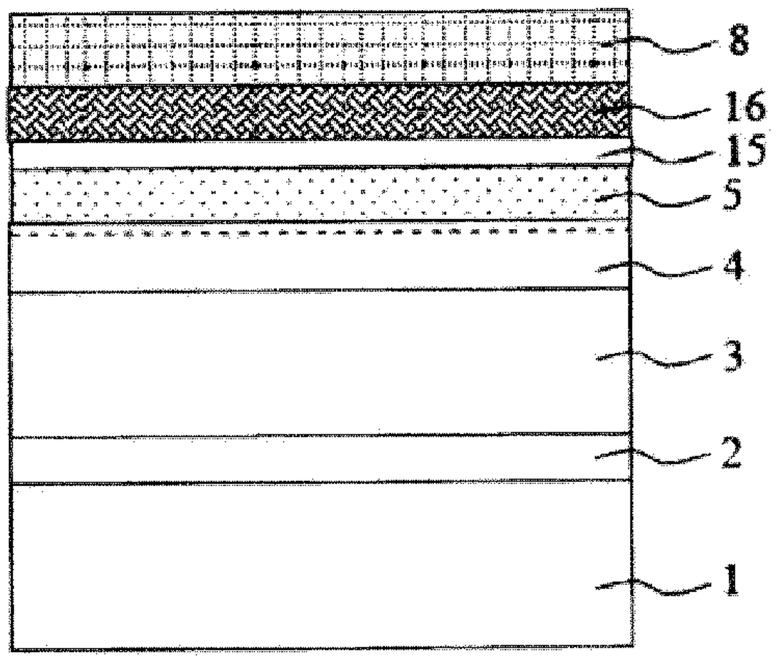

FIG.11a

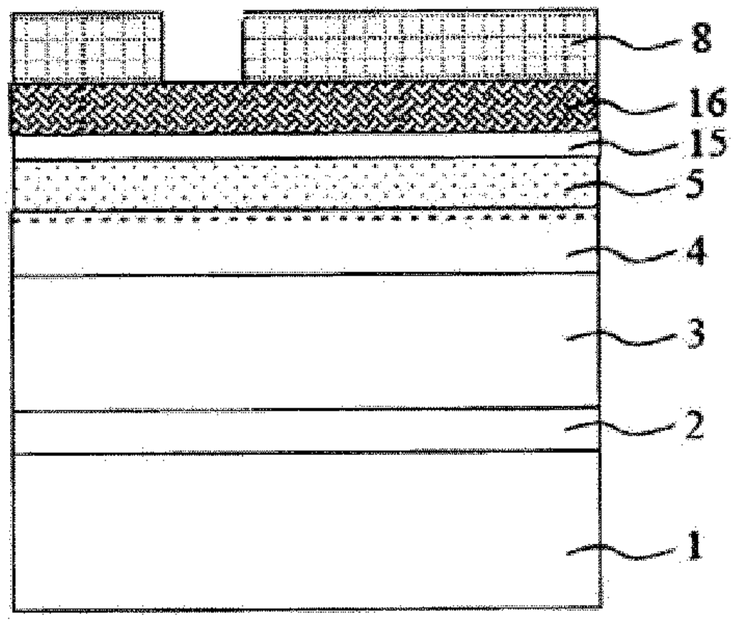

FIG.11b

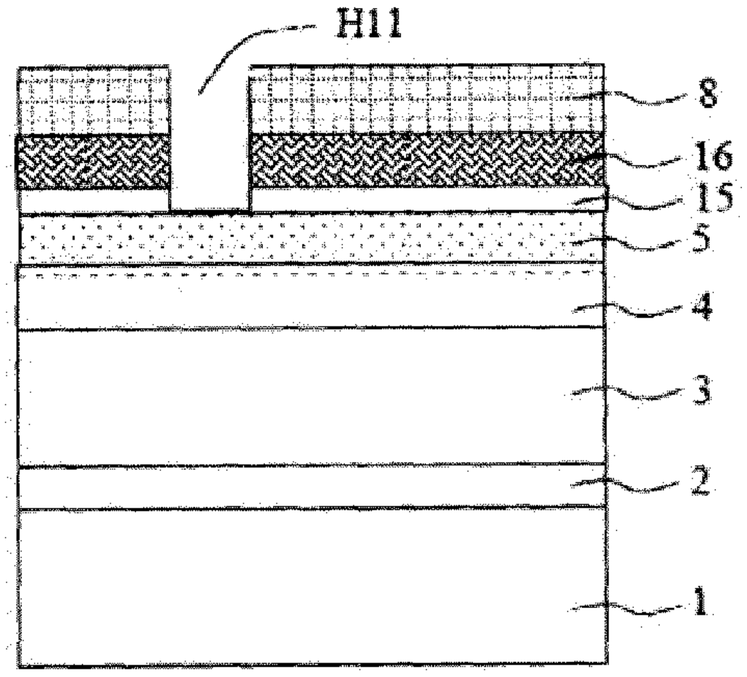

FIG.11c

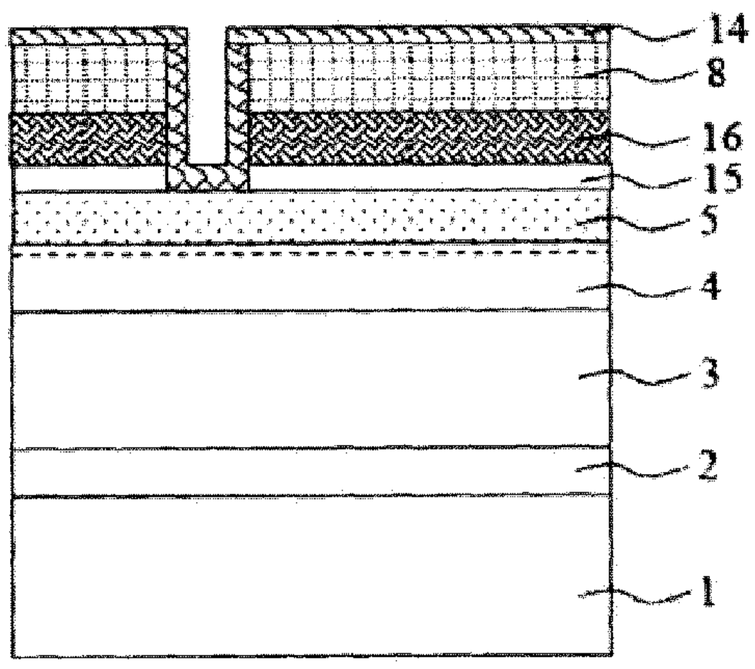

FIG.11d

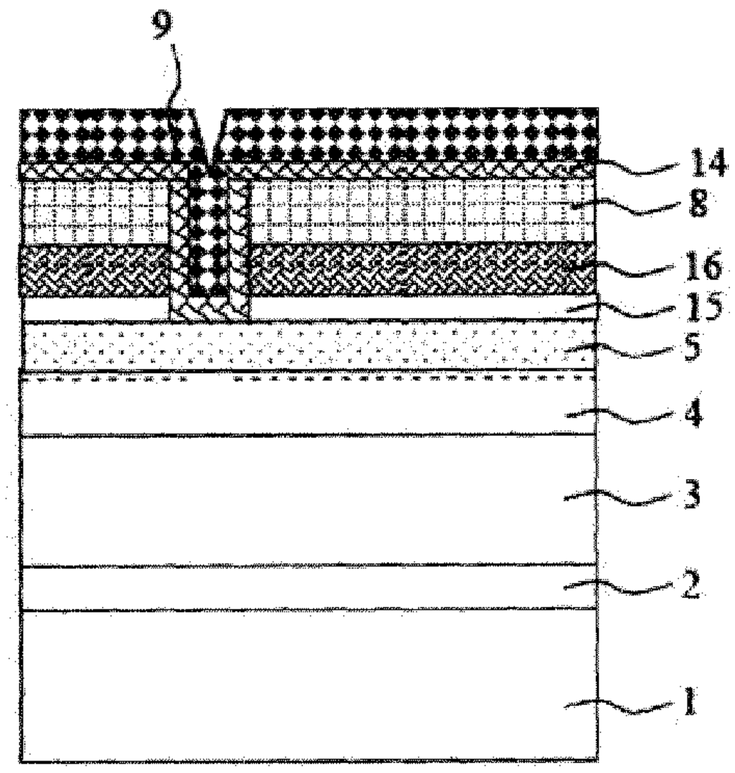

FIG.11e

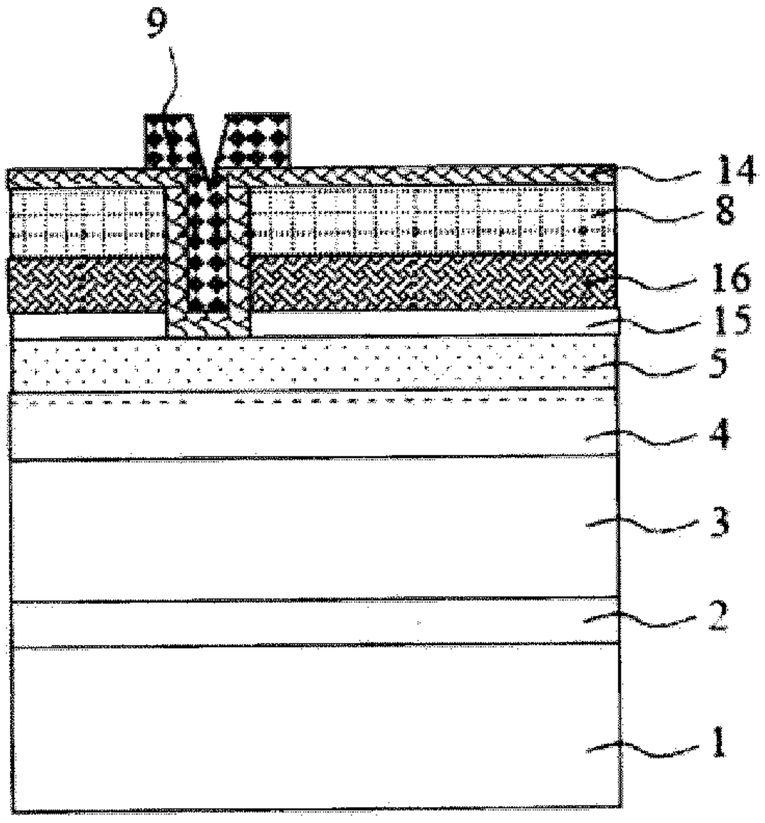

FIG.11f

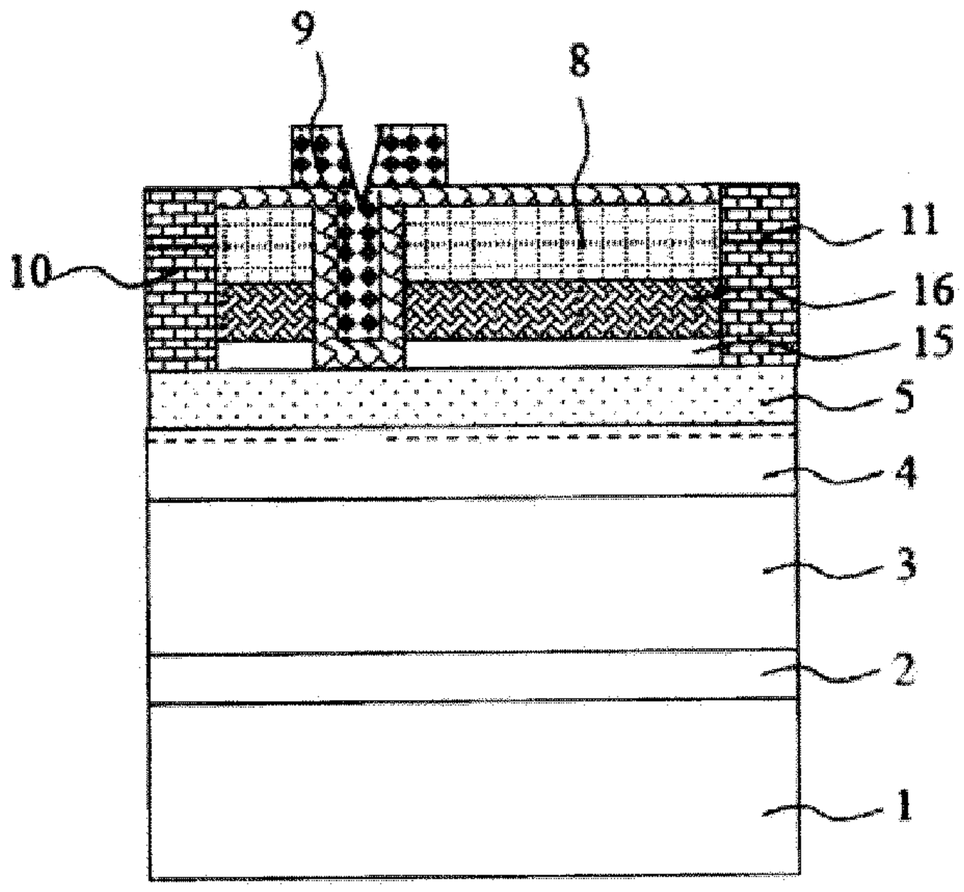

FIG.11g