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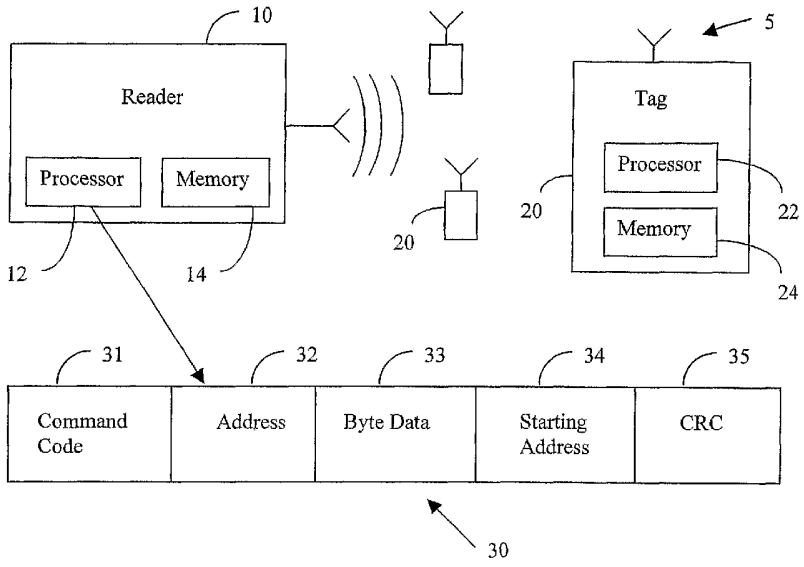
(54) Title: RF TAG SYSTEM WITH SINGLE STEP READ AND WRITE COMMANDS



(57) Abstract: A system has a read command signal that includes an Address field, Byte Data field, and Starting Address field. If the tag data read from the memory address identified by the Address field is the same as the Byte Data, the tag sends a response signal with Page Data read from the memory location identified by the Starting Address field and the tag ID. A write command signal includes an Address field, Byte Data field, Starting Address field, and Page Data field. If the tag data is the same as the Byte Data, the tag writes the data from the Page Data field to the memory location identified by the Starting Address field. Accordingly, data is read from and written to the tags in a single step, and the reader need not wait for the tag to respond with a tag ID before requesting that data be read from or written to that tag.

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RF TAG SYSTEM WITH SINGLE STEP READ AND WRITE COMMANDS

TECHNICAL FIELD

The present invention relates to an RF tag system having commands for reading and writing data. More particularly, the present invention relates to an RF tag system having group commands that reduce the number of steps needed to read data from a tag or write data to the tag.

Background Art

An RF tag system generally has a reader, also referred to as an interrogator or a base station, and tags that communicate with the reader using RF (radio frequency) signals. RF tag systems are shown, for instance, in U.S. Patent Nos. 5,942,987 to Heinrich et al., 5,673,037 to Cesar et al., 5,550,547 to Chan et al., and 5,521,601 to Kandlur et al.

If the reader desires to read data from a specific tag, the reader will transmit a Group Select command addressed to all the tags, or a group of tags, requesting a response. The tags will each respond with its tag identification (ID), which identifies the specific tag to the reader. The reader then transmits a Read command having the tag ID of the desired tag. The specified tag will transmit a response signal, with the requested data. For a tag having a 40Kbps data rate, it takes approximately 3.35ms for the reader to transmit the Group Select command, 2.8ms for the tag to issue a response, 3.15ms to send the Read command, and another 2.8ms for the tag to respond. Accordingly, the total transaction time is about 12.10ms for a tag having a 40 Kbps data rate.

If the reader desires to write data to a specific tag, the reader will transmit a Group Select command addressed to all the tags, or a group of tags, requesting a response. The tags will each respond with its tag ID. The reader then transmits a Write Byte command having the desired tag ID and a first byte of data to be written to the tag. The tag acknowledges that it received a write data command and then writes the data to its memory (usually an EEPROM). The reader then sends a Verify Byte command, which contains the tag ID and the address location of the byte of data that is being verified. The tag responds by reading the byte of data that was written to the memory and sending a Verify Byte Response with that byte of data that was written to the memory. The process repeats for each byte of information to be written to the tag. A typical write process is for eight bytes, which means that the Write Byte - Write Byte Response - Verify Byte - Verify Byte Response cycle is performed a total of eight times.

For a tag having a 40Kbps data rate, it takes 3.35ms for the Group Select command, 2.8ms for the response, 3.35ms for the Write Byte command, 1.4ms for the Write Byte Response, 15ms to write the byte to the tag, 3.15ms for the Verify Byte command, and 1.4ms for the Verify Byte Response. Accordingly, the total transaction time for an 8-byte write operation at a 40Kbps data rate is 200.55ms.

SUMMARY OF THE INVENTION

It is an object of the invention to reduce the amount of time required for reading data from a tag. It is another object of the invention to reduce the amount of time required for writing data to a tag. It is a further object of the invention to provide a single step for reading data from a tag. It is a further object of the invention to provide a single step for writing data to a tag. It is another object of the invention to provide a system for reading data from, and writing data to, a tag that does not require any preceding commands. It is yet another object of the invention to provide a system that can be used for a variable fee toll road which charges a toll fee based upon the entry and exit locations of a particular vehicle.

A system is provided having a read command signal sequence that identifies a group of tags and a memory address from which the designated tags are to return Page Data. The read command signal sequence includes an Address field, Byte Data field, and Starting Address field. The Address field identifies the memory address at which the tag data is to be read and compared to the Byte Data. If the tag data is the same as the Byte Data, the tag responds to the read command signal with tag ID and the Page Data read from the memory location identified by the Starting Address field. If the tag data is not the same, then the tag is not one of the tags designated by the reader to respond to the command, and the tag does not respond.

The system also includes a write command signal sequence that identifies a group of tags and the Page Data to be written to the designated tags. The write command signal sequence includes an Address field, Byte Data field, Starting Address field, and Page Data field. If the tag data at the memory location identified by the Address field is the same as the Byte Data, the tag writes the data from the Page Data field to the memory location identified by the Starting Address field.

Accordingly, the invention provides that the read command signal sequence be sent to the tags for tag ID and data to be read from the designated tags. Thus, the read is accomplished in a single step, and the reader need not wait for the tag to respond with a tag ID before requesting that data be read from that tag. In addition, the invention provides that the write command signal sequence be sent to the tags for data to be written to the designated tags. Thus, the data write is accomplished in a single step, and the reader need not wait for the tag to respond with a tag ID before requesting that the data be written to the tag.

The single step read and write commands reduce the number of signals that need to be transferred between the reader and the tags. As a result, the reader is able to increase throughput. In addition, the time to read data from and write data to the tags is substantially reduced.

These and other objects of the invention, as well as many of the intended advantages thereof, will become more readily apparent when reference is made to the following description, taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram showing the tag system with a command signal sequence used to read Page Data from the tags in accordance with the preferred embodiment of the invention;

Figure 2 is a block diagram showing the command signal sequence used to write Page Data to the tags;

Figure 3 is a flow chart for the operation of reading Page Data from the tags in accordance with the command signal sequence of Fig. 1; and

Figure 4 is a flow chart for the operation of writing Page Data to the tags in accordance with the command signal sequence of Fig. 2.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In describing a preferred embodiment of the invention illustrated in the drawings, specific terminology will be resorted to for the sake of clarity. However, the invention is not intended to be limited to the specific terms so selected, and it is to be understood that each specific term includes all technical equivalents that operate in a similar manner to accomplish a similar purpose.

Turning to the drawings, Fig. 1 shows the tag system 5 having a base station or reader 10 and tags 20. The reader 10 has a processor 12 that interfaces with a memory 14. The processor 12 sends and receives signals to the tags 20 through a reader antenna. The reader 10 may also include a signal generator and receiver that respectively process the signals sent and received by the processor 12. The processor 12 controls the reader 10 and executes the command structure of the present invention. The memory 14 keeps application data, and the tag IDs. The memory 14 can also store the command structure used to communicate with the tags 20.

The tags 20 each include a receiver or processor 22, preferably in the form of an ASIC (application specific integrated circuit) that controls the tag 20 and executes the command structures. The processor 22 receives and sends signals through the tag antenna and controls the processing of those signals. The tags 20 also have a memory 24 that retains the tag ID and Page Data in predetermined memory locations.

As also shown in Fig. 1, the reader 10 transmits a Streamlined Group Select Equal Page Read (SGSEPR) command 30 in accordance with the preferred embodiment of the invention. The SGSEPR command 30 is used to obtain both the tag ID and Page Data from a certain class (group) of tag 20 ASICs in a single command and response transaction.

The first field of the SGSEPR command sequence 30 is the Command Code field 31. The Command Code field 31 identifies the command sequence as being an SGSEPR command 30. The Command Code field is a one-byte value. The next field in the command sequence is the Address field 32. The Address field 32 identifies the memory location in the tag memory 24 that is to be accessed by the tag 20. The next field is the Byte Data field 33, which contains the data that the tag 20 is to compare with the information stored at the memory location identified by the Address field 32. The Starting Address field 34 identifies the memory position of the tag memory 24 that contains the Page Data that is to be returned to the reader 10. The CRC field 35 is a standard cyclic redundancy check field.

Turning next to Fig. 3, the operation of the tag 20 is shown for the SGSEPR command 30 of Fig. 1. The operation is preferably controlled by the tag processor 22. At the first step, step 100, the tag 20 reads the Command Code field 31 of the command sequence 30. The tag 20 identifies the command sequence as being an SGSEPR command 30. At step 102, the tag 20 then reads the Address field 32. The tag 20 preferably stores the Address field 32 in a temporary register location.

At step 104, the tag 20 then reads the Byte Data in the Byte Data field 33, and compares that Byte Data with the data (e.g., a tag group identifier) retrieved from the tag memory location stored at step 102. The tag also reads the Starting Address and CRC field 35. At step 106, if the Byte Data is the same as the tag group identifier data stored in the tag memory 24, the Address is valid (i.e., not a protected address location), and the CRC is accurate, then the tag 20 retrieves the tag ID and the Page Data stored in the tag memory 24 identified by the Starting Address field 34, and returns the tag ID and Page Data to the reader 10, step 108. If the data in the Byte Data field 33 is not the same as the tag group identifier data stored in the tag memory

24, or the Address is not valid, or the CRC is inaccurate, step 106, then the process ends, step 110.

Returning to Fig. 2, a Streamlined Group Select Equal Page Write (SGSEPW) command 40 is shown. The SGSEPW command 40 is generated by the reader 10 and sent to the tag 20 to obtain both the tag ID and to write Page Data to a certain class (group) of tag 20 ASICs in a single command and response transaction. The reader 10 can store the tag ID so that it can be used for other commands that require the tag ID to be present in the command structure.

The first field of the SGSEPW command sequence 40 is the Command Code field 41. The Command Code field 41 identifies the command sequence as being an SGSEPW command 40. The Command Code field 41 is a one-byte value. The next field in the command sequence is the Address field 42. The Address field 42 identifies the memory location in the tag memory 24 that is to be accessed by the tag 20. The next field is the Byte Data field 43, which contains the data that the tag 20 is to compare with the information stored at the memory location identified by the Address field 42. The Starting Address field 44 identifies the memory position of the tag memory 24 that Page Data is to be written to.

Turning next to Fig. 4, the operation of the tag 20 is shown for the SGSEPW command 40 of Fig. 2. The operation is preferably controlled by the tag processor 22. At the first step, step 120, the tag 20 reads the Command Code field 41 of the command sequence 40. The tag 20 identifies the command sequence as being an SGSEPW command 40. At step 122, the tag 20 then reads the Address field 42. The tag 20 preferably stores the Address field 32 in a temporary register location.

At step 124, the tag 20 then reads the Byte Data field 43, and compares that Byte Data with the data (e.g., a tag group identifier) retrieved from the tag memory

location stored at step 122. The tag also reads the Starting Address field 44, the Page Data from the Page Data field 45, and the CRC (not shown, but follows the Page Data field 45). After this, the ASIC will decide to either respond and perform the write, or terminate the transaction and wait for the next command.

Accordingly, if the Byte Data is the same as the group identifier data stored in the tag memory 24, the Address is valid, and the CRC is accurate, step 126, then the tag 20 writes the Page Data into memory 24 starting at the memory location identified by the Starting Address field 44, step 128. If the Byte Data is not the same as the group identifier data stored in the tag memory 24, the Address is invalid, or the CRC is not accurate, step 126, then the Page Data is not written to the tag memory 24 and the process ends, step 130.

Preferably, the tag 20 sends a Group Response to the reader 10 that includes the tag ID, the equivalence of its Page Data and a verification signal status, and then it writes the Page Data to memory 24. The tag 20 verification signal status verifies to the reader 10 whether or not the Page Data was properly written to the tag memory 24. The tag 10 compares the Page Data in the Page Data field 45 to the Page Data in the memory 24 location specified by the Starting Address field 44. If the last write to the tag memory 24 was a good write (that is, there was no error in writing and therefore the verification signal is true), and the Page Data 45 are the same as the Page Data in the memory 24, then the verification response message indicates that the write was a good write and that the data matches.

Otherwise, the tag 20 sends a response message to the reader 10 indicating that the write was not a good write, in which case the reader 10 resends another SGSEPW command 40. An error may result, for instance, where the tag just turned on, so that the initial SGSEPW command signal 40 has not yet resulted in data being written to

the tag. Thus, the write command 40 results in the reader 10 being informed that the write has been successful, or that the write had failed. Usually, it requires two write commands 40 before the tag 20 returns a verification message that the write was successfully performed. The first write command 40 will result in the write of the Page Data, and the second write command 40 will verify that the write was successfully performed.

Accordingly, all tags 20 having the same data in memory 24 as the Byte Data field 33, 43 would respond to the command sequence 30, 40 to either read Page Data from the memory location identified by the Starting Address 34, or to write Page Data 45 to the memory at the Starting Address 44.

The Address field 32, 42 can be utilized to select on any area of memory 24 that the reader 10 desires, but the ASIC will preferably only do comparisons on areas of memory that are not in protected areas. That is, the tag 20 determines whether the specified Starting Address field 34, 44 is a protected area of memory as defined by a Memory Access Map which correlates the data in memory to specific memory addresses, to prevent access to confidential information such as passwords and authorization codes and to prevent information from inadvertently being erased.

The tag 20 can include steps to prevent access to (both reading or writing) protected areas of memory 24, such as by verifying that the Address field 32, 42 and Starting Address field 34, 44 are valid. If either address is invalid, no response will be sent and the state will remain the same. An address is invalid, for instance, if it refers to a memory location that is used to retain confidential or protected information. The tag 20 can also use mutual authentication mode and memory lock bits (i.e., an array of the memory that defines whether or not a memory location is locked) to protect those confidential memory locations.

The SGSEPR and SGSEPW commands 30, 40 result in a shorter time frame to read data from and write data to a tag. The reader need not first obtain the tag ID and perform a specific write to the tag with the obtained ID. In addition, the read and write commands 30, 40 do not require any preceding commands (such as to move the tag into an active state) to read data from and write data to the tag 20. This reduces the time required to process signals at both the reader 10 and the tag 20.

The invention especially results in a greater throughput at the reader 10. For instance, to read data from a tag 20 having a 40Kbps data rate, it takes 1.95ms for the SGSEPR command 30 to be processed and sent by the reader 10, and 4.4ms for the response from the tag 20, for a total transaction time of 6.35ms. To write data to a tag 20 having a 40Kbps data rate, it takes 3.55ms for the SGSEPW command 40 to be processed and sent by the reader 10, 15ms for the data to be written to the tag memory 24, 3ms for the write response, and then another 3.55ms to send another SGSEPW command 40 as a verification that the data was written, and 3ms for the tag to respond with a verification signal. Accordingly, the total transaction time for an 8-byte write operation at a 40Kbps data rate is 20.9ms.

In accordance with the preferred embodiment of the invention, the system 5 is used on a variable fee toll road which charges a toll fee based upon the entry and exit locations of a particular vehicle. Accordingly, the toll fee varies depending on the place that the vehicle enters the toll road and the place that the vehicle exits the toll road. As the vehicle enters the toll road, the SGSEPW command 40 is used to write information, such as a location code, to the tag memory 24. The location code identifies the entry location for that vehicle. The reader at the entry location receives the tag ID from the tag response signal, and can send the tag ID to a host computer (not shown) for tracking and billing purposes.

The SGSEPR command 30 is used to read that same location code from the tag 20 as it exits the toll road. The exit location can then determine the proper toll based on the entry location read from the tag. Of course, other suitable arrangements can be made, such as that the entry location reader and exit location reader each independently send the tag ID and location information to a host computer to calculate the toll and bill the tag account holder.

The location code is written to, and read from, the same memory location, so that the Starting Address 34, 44 is the same for both the SGSEPW command 40 and the SGSEPR command 30. For example, if the Starting Address field 34 is 50, then the tag ID, which is located at 00 to 07, is returned together with the data located at memory location 50 to 57. The Starting Address field defines the page of data that will be returned back to the reader. The tag ID is always returned back with the Page Data.

The foregoing description and drawings should be considered as illustrative only of the principles of the invention. The invention may be configured in a variety of manners and is not intended to be limited by the preferred embodiment. Numerous applications of the invention will readily occur to those skilled in the art. Therefore, it is not desired to limit the invention to the specific examples disclosed or the exact construction and operation shown and described. Rather, all suitable modifications and equivalents may be resorted to, falling within the scope of the invention.

CLAIMS:

1. A radio frequency tag, comprising:

a memory having a first memory location retaining a tag group identifier, a second memory location retaining a tag identification code, and a third memory location retaining page data; and,

a processor for receiving a write signal having an address field identifying the first memory location, a byte data field having byte data, and a page data field having page data, said processor retrieving the tag group identifier from the first memory location of said memory in response to the address field and comparing the tag group identifier with the byte data from the byte data field, wherein said processor writes the page data from the page data field to the third memory location of said memory if the byte data matches the tag group identifier from the first data location.

2. The tag of claim 1, wherein said processor further compares the page data from the page data field to the page data retained at the third memory location and sends a response signal including a verification message confirming whether or not the page data retained at the third memory location matches the page data from the page data field before writing the page data from the page data field to the third memory location.

3. The tag of claim 2, wherein the response signal further includes the tag identification code from the second memory location of said memory.

4. The tag of claim 1, wherein the write signal further includes a starting address field identifying the third memory location, and said processor writes the page data to the third memory location identified by the starting address field.

5. A base station for communicating with radio frequency tags, each tag having a memory with a first memory location retaining a tag group identifier, a second memory location retaining a tag identification code, and a third memory location retaining page data, the base station comprising:

a processor that generates a write signal having an address field identifying the first memory location, a byte data field having byte data that matches the tag group identifier stored in the first memory location of selected ones of the tags, and a page data field having page data; and,

an antenna for transmitting the write signal to a plurality of tags, causing the selected ones of the tags to write the page data from the page data field to the third memory location.

6. The base station of claim 5, said antenna further causing the selected ones of the tags to compare the page data from the page data field to the page data retained at the third memory location and send a response signal including a verification message confirming whether or not the page data retained at the third memory location matches the page data from the page data field before writing the page data from the page data field to the third memory location.

7. The base station of claim 6, wherein the response signal further includes the tag identification code from the second memory location.

8. The base station of claim 5, wherein the write signal further includes a starting address field identifying the third memory location, and said antenna causes the selected ones of the tags to write the page data from the page data field to the third memory location identified by the starting address field.

9. A radio frequency tag, comprising:

a memory having a first memory location retaining a tag group identifier, a second memory location retaining a tag identification code, and a third memory location retaining page data; and,

a processor for receiving a read signal having an address field identifying the first memory location, and a byte data field having byte data, said processor retrieving the tag group identifier from the first memory location of said memory in response to the address field and comparing the tag group identifier with the byte data from the byte data field, wherein said processor reads the page data from the third memory location of said memory if the byte data matches the tag group identifier from the first data location and sends a response signal including the page data read from the third memory location.

10. The tag of claim 9, wherein the response signal further includes the tag identification code from the second memory location of said memory.

11. The tag of claim 9, wherein the read signal further includes a starting address field identifying the third memory location, and said processor reads the page data from the third memory location identified by the starting address field.

12. A base station for communicating with radio frequency tags, each tag having a memory with a first memory location retaining a tag group identifier, a second memory location retaining a tag identification code, and a third memory location retaining page data, the base station comprising:

a processor that generates a read signal having an address field identifying the first memory location, and a byte data field having byte data that matches the tag group identifier stored in the first memory location of selected ones of the tags; and,

an antenna for transmitting the read signal to a plurality of tags, causing the selected ones of the tags to read the page data from the third memory location and send a response including the page data read from the third memory location.

13. The base station of claim 12, wherein the response signal further includes the tag identification code from the second memory location.

14. The base station of claim 12, wherein the read signal further includes a starting address field identifying the third memory location, and said antenna causes the selected ones of the tags to read the page data from the page data field from the third memory location identified by the starting address field.

Figure 1

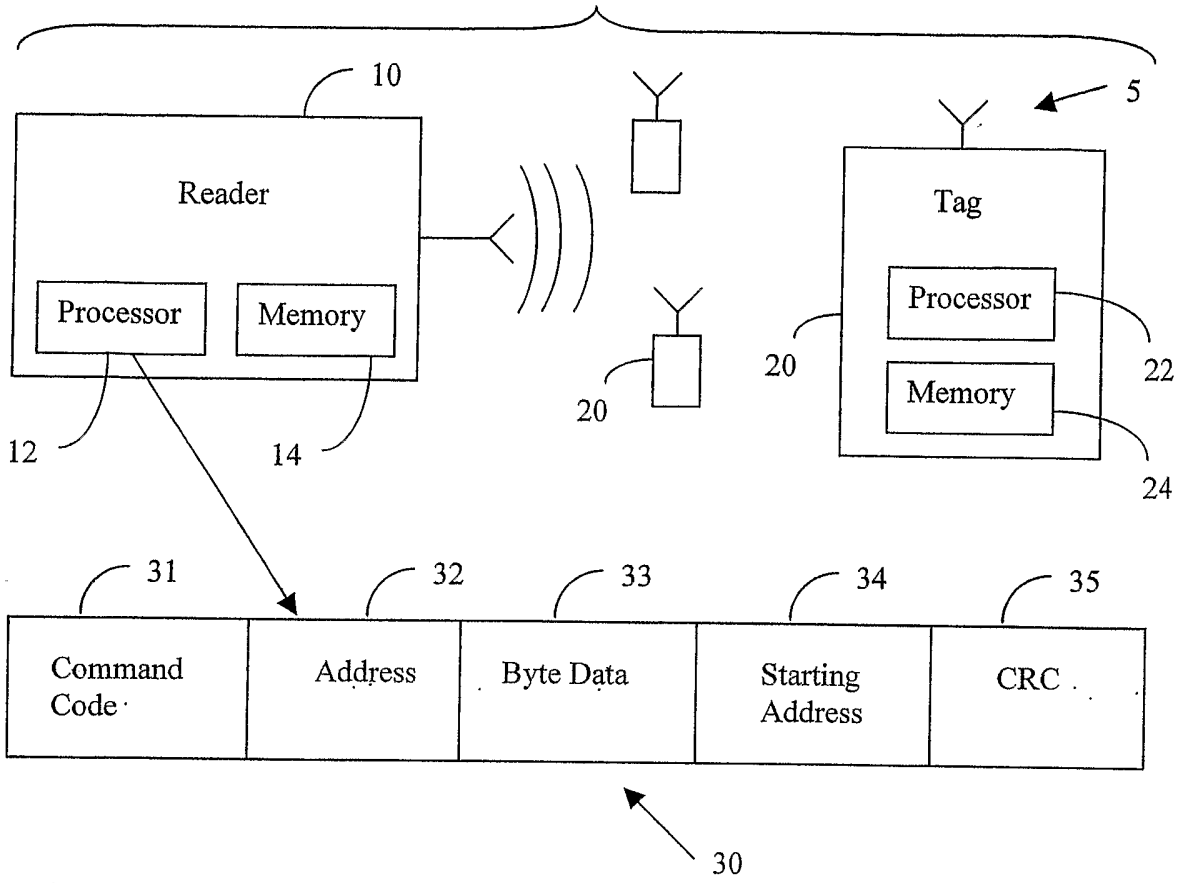

Figure 2

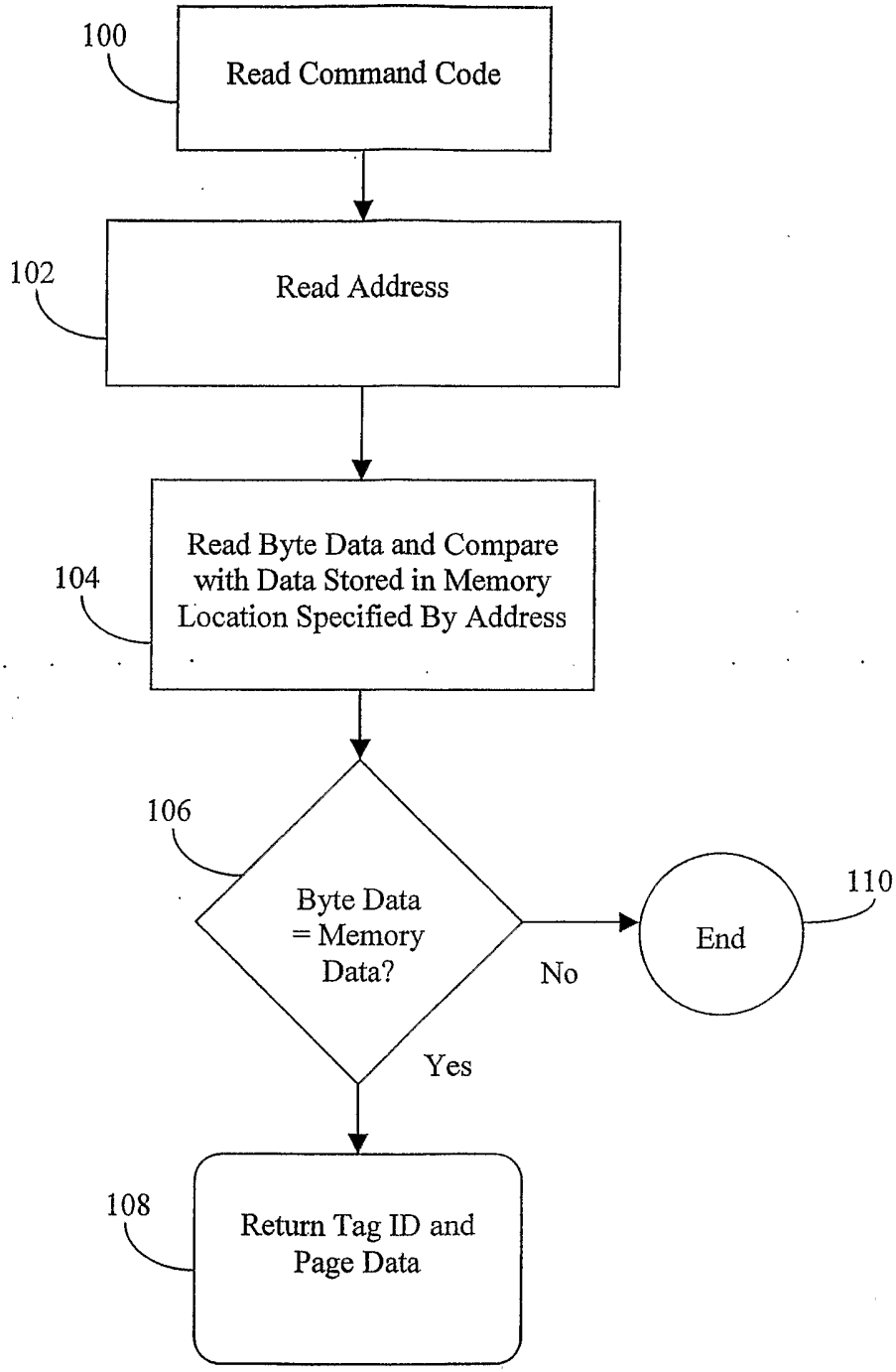
100
Read Command Code
102
Read Address
104
Read Byte Data and Compare with Data Stored in Memory Location Specified By Address
106
Byte Data = Memory Data?
No
110
End
Yes
108
Return Tag ID and Page Data

Figure 3

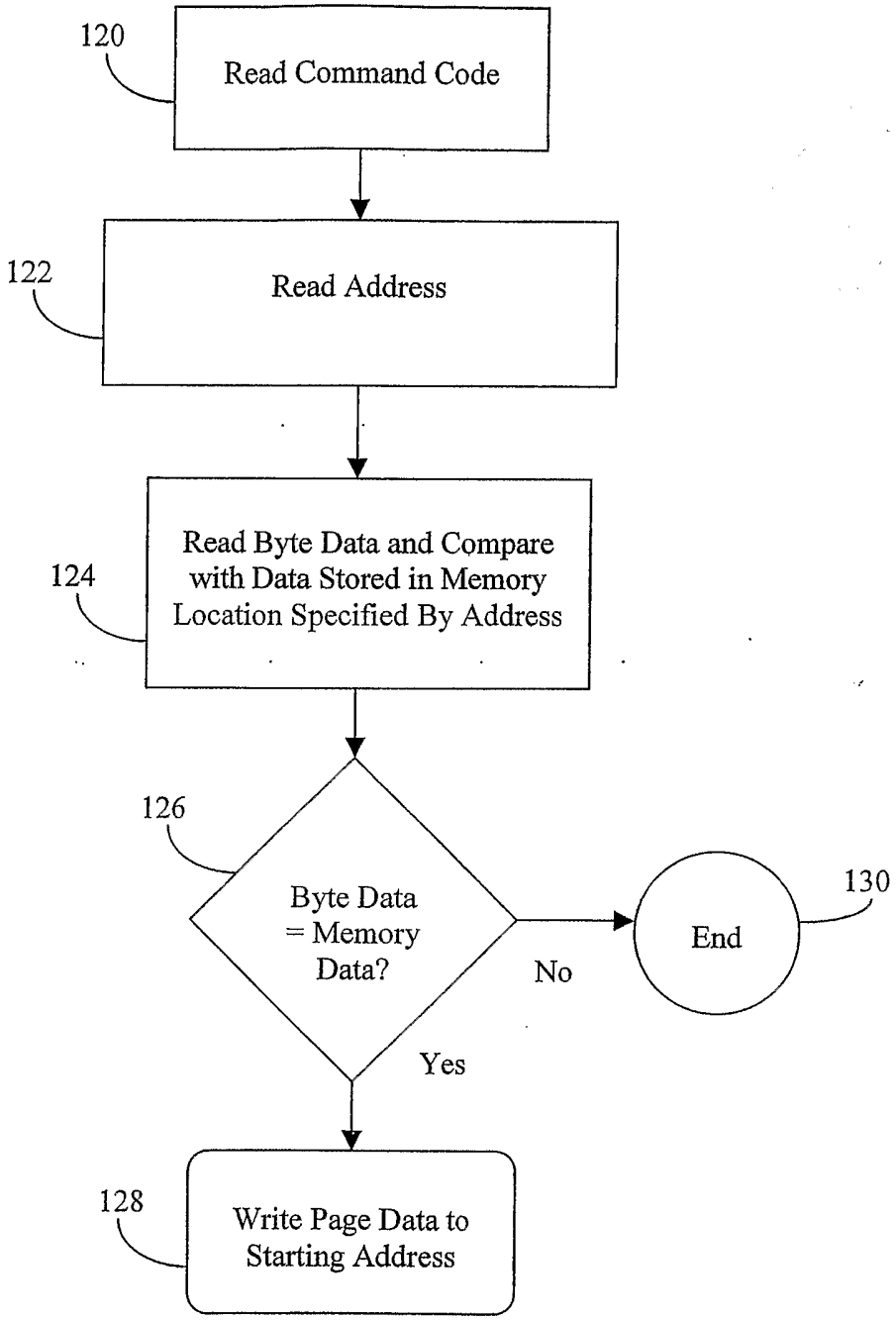
120
Read Command Code
122
Read Address
124
Read Byte Data and Compare with Data Stored in Memory Location Specified By Address
126
Byte Data = Memory Data?
No
130
End
Yes
128
Write Page Data to Starting Address

Figure 4