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3,422,405

DIGITAL COMPUTER HAVING AN INDIRECT FIELD LENGTH OPERATION

Filed March 25, 1966

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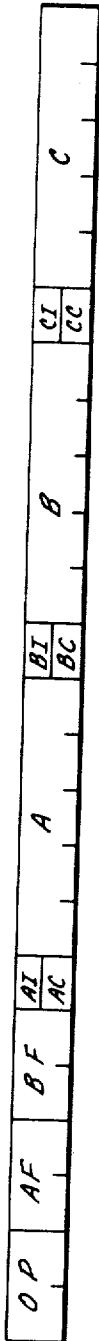


FIG. 1

EIGHT BIT	1	0
FOUR BIT	1	1
TWO BIT	0	1
ONE BIT	1	0

EIGHT BIT
FOUR BIT
TWO BIT
ONE BIT

2₃ 2₄

FIG. 2A

EIGHT BIT	1	1
FOUR BIT	1	0
TWO BIT	1	0
ONE BIT	1	0

EIGHT BIT
FOUR BIT
TWO BIT
ONE BIT

120016 120017

FIG. 2B

EIGHT BIT	1	0
FOUR BIT	0	1
TWO BIT	0	1
ONE BIT	0	0

EIGHT BIT
FOUR BIT
TWO BIT
ONE BIT

120038 120039

FIG. 2C

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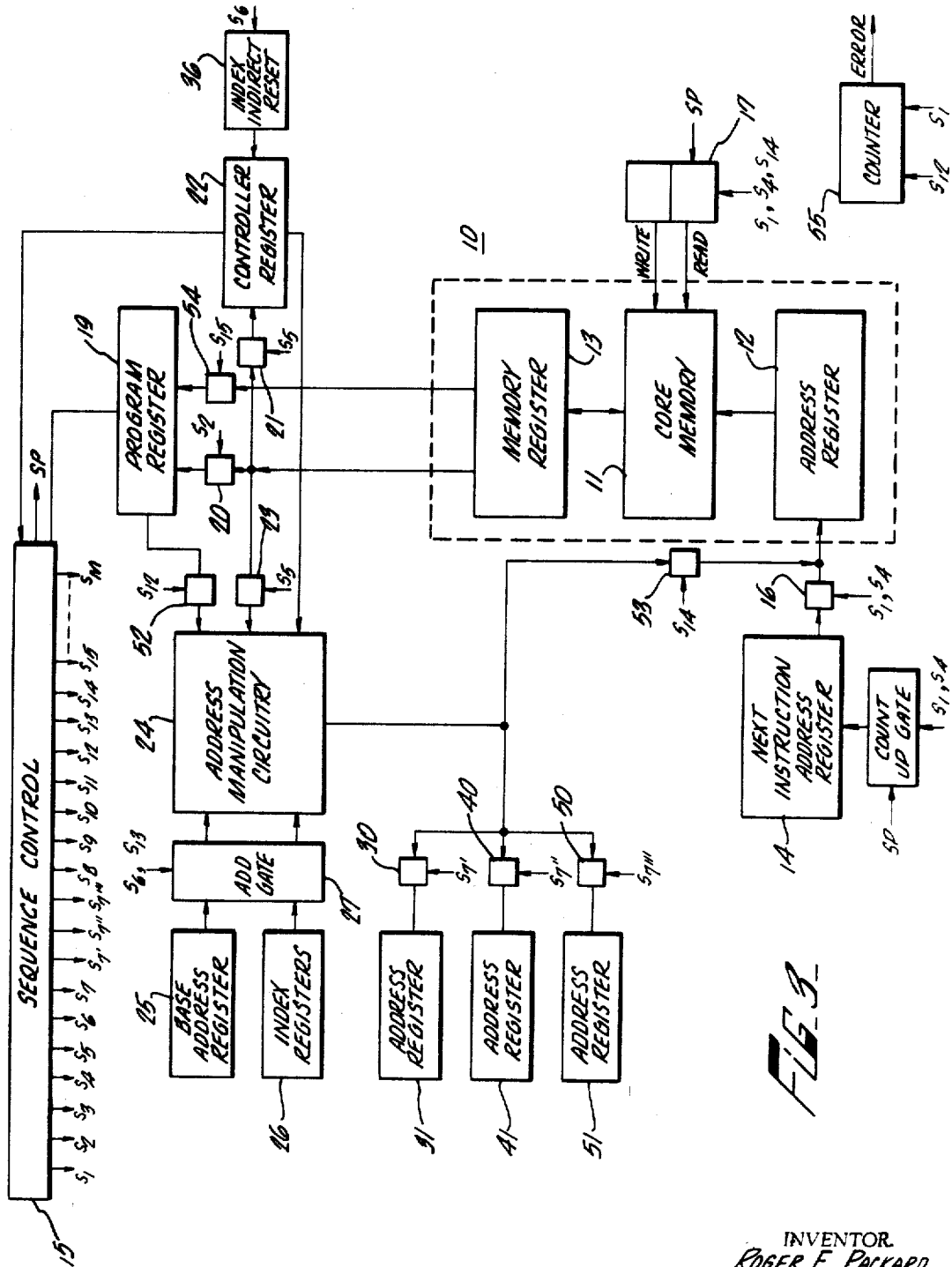
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Sheet 2 of 2



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DIGITAL COMPUTER HAVING AN INDIRECT FIELD LENGTH OPERATION

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Int. Cl. G11b 13/00

9 Claims

ABSTRACT OF THE DISCLOSURE

A digital computer system in which data field lengths specified by program instructions may be altered during the fetch phase of operation without altering the instructions themselves. The length of data specified by an instruction is treated as a variable whenever a particular code is manifested by bits in the field length locations within the instruction. Means are provided to recognize this code and other means, responsive to such recognition, obtain the true length of data from one of several memory locations within the computer. Other bits within the field length locations are utilized to specify the particular memory location.

This invention relates to high speed digital computer systems and, more particularly, to such systems wherein the length of data fields specified by program instructions may be altered during the fetch phase of operation without alteration of the instruction itself.

The operation of an automatic digital computer in carrying out a program of instructions is generally split into two phases which normally alternate: the fetch phase and the execute phase. During the fetch phase of operation, the next instruction to be executed is selected from computer memory and transferred to one or more control registers, while during the execute phase of operation an operation code segment of the instruction is decoded and the particular operation specified by the instruction is executed.

Both the instructions and data operands utilized in the execution of instructions may be stored in the same memory. The computer will ordinarily start with a word stored in some specified location in memory and interpret this word as an instruction. It will subsequently take instruction words from the memory locations in order unless a halt or branch instruction is encountered. Data to be used in executing the instruction will ordinarily be stored in another part of the memory. Flexibility is achieved since either instructions or data can be stored in the same storage registers.

Instructions requiring the performance of operations upon data stored in the memory will normally include operation code digits indicative of the particular operation to be performed, field length digits indicative of the length of one or more data operands on which the operation is to be performed, and address field digits indicative of the addresses in memory where the data operands are located. Additionally, a particular digit within the address field, denoted a controller digit, may be utilized to indicate the format of a data operand. For example, the format may be indicated as being "unsigned numeric," "signed numeric," or "alphanumeric." Use of controller digits to denote the format of data operands is described in the copending application of Lloyd M. Cherry et al., Ser. No. 537,506, filed on even date herewith and assigned to the assignee of the present application.

Consequently, a particular data operand may be specified by digits within an instruction which manifest its address, format and length. It often is advantageous to

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be able to alter particular data operands to which instructions refer without altering the instructions themselves. Such alterations are advantageous, for example, with respect to iterative programs and greatly reduce the number of instructions required in an iterative program.

Index registers may be utilized to alter the address referred to by an instruction without altering the instruction. Similarly, indirect addressing may be utilized to alter the format of a data operand specified by an instruction without altering the instruction in that it fetches a new address having a new controller associated therewith. The use of index registers and indirect addressing are described, for example, in the copending application of Roger Packard and William Buster, Ser. No. 537,572 filed on even date herewith and assigned to the assignee of the present application. It has heretofore been difficult, however, to conveniently alter the length of a data operand specified by an instruction.

The present invention provides an arrangement whereby an instruction is rendered capable of dealing with variable length data operands without alteration of the instruction.

In brief, the advantages of the present invention are realized by means of treating the length of data specified by an instruction as a variable whenever the field length digits of the instruction include a special code. When the special code appears, an indirect field length is indicated and the true length of data is taken from one of several memory locations within the computer, the field length digits then being utilized to specify the particular memory location.

For a complete understanding of the invention reference should be made to the accompanying drawing, in which:

FIG. 1 depicts the format of a typical instruction word which may be utilized in conjunction with the present invention;

FIGS. 2A, 2B, and 2C depict a manner in which the field length digits of the instruction word of FIG. 1 may be utilized to indicate that an indirect field length is being specified and to indicate the location in memory of the true length of data; and

FIG. 3 depicts a schematic block diagram of one embodiment of the present invention utilizing instruction words of the format depicted in FIG. 1.

FIG. 1 depicts the format of a typical instruction word which may be utilized in conjunction with the present invention. It depicts an instruction word which consists of 24 binary coded decimal digits with each decimal digit comprising four binary bits. Each decimal digit is individually addressable in the embodiment shown in FIG. 3 and the instruction is considered to be divided into four six-digit syllables.

The first two digits of the first syllable denote a particular instruction and are referred to as operation code digits. The remaining four digit positions of the first syllable are used as variants. The first two digit positions of the variants are referred to as the AF variant digits and the remaining two digit positions are referred to as the BF variant digits.

The second syllable consists of six decimal digits which make up an A address field, the third syllable consists of six digits which make up a B address field, and the fourth syllable consists of six digits which make up a C address field. The low order five digits of each address field represent a base relative address in core memory. The high order digit of each address field is split. Two bits of the high order digits are designated index bits and denote whether indexing is to be used and if so which of several index registers is to be used. The remaining two bits of the high order digit are designated controller bits and denote whether indirect addressing is to occur, and may also be

used to indicate the nature of data information contained in a data field designated by the particular address field.

In the embodiment of the present invention being described, each digit of an instruction is individually addressable and a syllable of six such digits will ordinarily be read out of memory during a single readout operation. The AF variant digits ordinarily give the length of the data field indicated by the A address and the BF variant digits ordinarily give the length of the data field indicated by the B address. The length of the data field indicated by the C address is ordinarily given by the larger of the AF and BF variant digits or by some combination of the two.

It may be seen that each data operand stored in the memory is characterized by three portions of an instruction word. It is characterized by its address, its controller and its field length, all of which are designated by the instruction. The address designates the beginning location in memory of the data operand, the controller indicates the format of the data operand, and the field length indicates the length of the operand.

During the fetch operation an instruction such as that depicted in FIG. 1 is ordinarily read out of memory a syllable at a time. Certain operations are performed upon these syllables at this time. These operations modify the base relative addresses within the address fields, and produce absolute addresses manifesting the beginning locations in memory of their corresponding data operands. These operations may include indexing whereby the address referred to by an instruction may be altered without altering the instruction itself.

Another operation which may be performed during the fetch operation is that of indirect addressing. By means of indirect addressing both an address and its controller specified by an instruction may be altered without altering the instruction itself. Both indexing and indirect addressing are described, for example, in the copending application of Roger Packard and William Buster, Ser. No. 537,572, filed on even date herewith and assigned to the assignee of this application.

It has heretofore been difficult, however, to conveniently alter the length of a data operand specified by an instruction without altering the instruction. The present invention achieves such alteration in field length by treating the length of data specified in the AF variants or BF variants of an instruction as a variable whenever these variants include a special code. When the special code appears, an indirect field length is indicated and values stored in remaining bit locations of these digits are utilized to indicate a memory location where the actual field length is stored.

FIGS. 2A, 2B, and 2C depict a manner in which the field length digits of the instruction word of FIG. 1 may be utilized to indicate that an indirect field length is being specified and to indicate the location in memory of the true field length.

FIG. 2A depicts the four bits of each of the digits making up the AF variant digits of FIG. 1. These digits are denoted D3 and D4. The bit locations of each digit are denoted the eight-bit, four-bit, two-bit, and one-bit locations. The indication of an indirect field length is manifested by the presence of binary "1's" in both the eight-bit and four-bit locations of digit D3.

FIG. 2A depicts exemplary AF digits wherein binary "1's" do appear in the eight-bit and four-bit locations of digit D3 thereby indicating an indirect field length. The remaining bits of the D3 and D4 digits are then utilized to determine a location in memory where the true field length may be found. In FIG. 2A the remaining bit locations store the decimal value 16. The contents of a base address register will normally be added to the decimal value indicated by the two-bit and one-bit locations of digit D3 and by digit D4 in order to determine an address in memory storing the true field length. Thus, for example, if the base address register had the digital value 120000 to all addresses specified in the instructions of a

particular program, the address at which the true field length may be stored as indicated by FIG. 2A would be the address 120016.

In accordance with the present invention the digital value stored at this address and the next succeeding address are during the fetch operation substituted into that register which normally stores the AF variant digits of the instruction. It is another feature of the present invention that the substituted field length digits may indicate that another indirect field length operation is to be performed.

FIG. 2B depicts exemplary digits stored in memory at addresses 120016 and 120017. These are the digits which are substituted for the digits shown in FIG. 2A in accordance with the particular indirect field length operation indicated by the digits of FIG. 2A. It may be seen that digit D3 of FIG. 2B also indicates that an indirect field length operation is to be performed since the eight-bit location and four-bit location of this digit are both storing a binary "1." The remaining bits indicate a digital value of 38. Consequently, upon the addition of this value to the contents of the base address register, address "120038" results. Thus, the next step in the indirect field length operation called for by the exemplary digits shown in FIG. 2B is to substitute the digits at locations 120038 and 120039 for the AF digits in that register normally storing the AF digits.

FIG. 2C shows the exemplary digits stored at addresses 120038 and 120039. The absence of binary "1's" in both the eight-bit location and four-bit location of the digits stored at address 120038 indicates that these digits store the true field length of a data operand. In FIG. 2C the true field length indicated by these exemplary digits is 86.

FIG. 3 depicts a schematic block diagram of an embodiment of the present invention utilizing instruction words of the format depicted in FIG. 1. In FIG. 3, numeral 10 indicates generally a memory unit which, for example, includes a core memory 11 which is addressed by the contents of an address register 12. In the embodiment shown, six-digit syllables are transferred in and out of core memory 11 through a memory register 13. Program instructions are stored in core memory 11 in sequential locations. The instructions are brought out of memory in response to addresses established in Next Instruction Address register 14 which is counted up following the transfer of each syllable from memory 11 into register 13.

In the embodiment shown, registers 12, 13, and 14 are six-digit registers. Since each digit stored in memory 11 is individually addressable and since six-digit syllables are read out of memory 11 and stored into register 13 during each read operation of the embodiment of the present invention shown in FIG. 3, register 14 will be counted up by "six" following each read operation. The operation of the embodiment shown in FIG. 3 is under the control of a sequence control unit 15. Unit 15 is a central control unit which typically includes a clock pulse source and a sequence control by means of which the sequence control unit is caused to step through a series of sequential steps in which output control lines designated by S_1 through S_m are energized in a controlled sequence. Sequence control unit 15 also includes combinational gating circuitry which in response to signals applied to unit 15 controls the sequence in which the output control lines are energized. Such sequence control units are well known in the computer and data processing art. Initially the sequence control unit 15 is in the S_1 state during which state the first syllable of the first instruction is brought out of memory 11 and inserted into memory register 13. To this end the contents of the register 14 which comprise the address of the initial digit of this syllable are transferred to address register 12 via AND gate 16. Sequence pulses designated SP are generated by sequence control unit 15 at the time the control unit changes from one control state to the next. An SP signal generated at the end of the S_1 state reads the addressed

syllable out of core memory 11 into memory register 13, the SP signal being gated by gate 17 to the read input of core memory 11. At this time, register 14 is counted up by "six" so as to store the address of the first digit of the succeeding syllable stored in memory 11. At the completion of the S₁ state, the sequence control unit 15 advances to the S₂ state.

During the S₂ state, the syllable in memory register 13 is transferred to a six-digit program register 19 by means of AND gate 20. The first syllable of the instruction including the operation code digits, the AF variant digits and the BF variant digits is now stored in register 19. The central control unit next advances to the S₃ state.

During the S₃ state, combinational gating circuitry within sequence control unit 15 may be utilized to detect the presence of particular combinations of bits stored in register 19. One particular combination of bits which may be detected at this time is a combination within the operation code digits which indicates that the instruction is a conditional branch operation. Operations which may follow upon the detection of a conditional branch operation are described in the copending application of R. Packard and W. Buster, referred to hereinbefore.

Another particular combination of bits which may be detected at this time is the combination within the variant digits which indicates that a literal is stored in the instruction. Operations which may follow upon the detection of a literal are described in the copending application of R. Packard, S.N. 537,380, filed on even date herewith and assigned to the assignee of the present application. The central control unit next advances to the S₄ state.

During the S₄ state, the address of the second syllable of the A address field of the instruction word which is now stored in register 14 is transferred via AND gate 16 to address register 12. The subsequent SP signal from control unit 15 causes the second syllable of the instruction to be read out of core memory 11 and stored in memory register 13. Upon the conclusion of state S₄ register 14 is counted up by "six" and the control unit advances to state S₅.

During state S₅, the first digit stored in register 13 is transferred via gate 21 to controller register 22 and the remaining five digits stored in register 13 are transferred via gate 23 to a register within address manipulation circuitry 24. Control unit 15 next advances to state S₆.

At the commencement of state S₆, controller register 22 stores the indexing bits and controller bits of the second syllable of the instruction while circuitry 24 stores the five digits of the address field which designate a relative address. During state S₆ various predetermined manipulations are performed upon this relative address in order to achieve an absolute address indicative of a data operand and upon which operations will be performed during the subsequent execute phase of operation. It is during state S₆ that base address register 25 is used to add a fixed base value to the relative address, and it is during state S₆ that index values from one of a plurality of index registers 26 may be added to the relative address and it is also during state S₆ that indirect addressing may be performed. All of these operations are described, for example, in the copending application of R. Packard and W. Buster referred to hereinbefore.

At the end of state S₆, reset means 36 is used to reset to "0" the bits within the first digit in register 22 which direct that indexing or indirect addressing be performed during state S₆. At the conclusion of state S₆ the control unit 15 advances to state S₇.

During state S₇ circuitry 24 is storing an absolute address indicative of the address of a data operand upon which operations are to be performed during the subsequent execute phase of operation and this absolute address is transferred during state S₇ via gate 30 to a first information address register 31. In the embodiment of the present invention being described, the particular instruction being fetched has three address fields. Sequence

control unit 15 is therefore reset again to state S₄, and during states S₄, S₅, S₆, and S₇, the B address field is read out of memory 11. Manipulations are performed upon the relative address portion of the B address field to obtain an absolute address and this absolute address is transferred via gate 40 to a second information address register 41. The sequence control unit 15 is then again reset to state S₄ and during states S₄, S₅, S₆ and S₇ the C address field is read out of memory 11, manipulations are performed upon the relative address portion of the C address field to obtain an absolute address and this absolute address is transferred via gate 50 to a third information address register 51. The operations performed upon the B address field and the C address field are identical to those just described with respect to the A address field. At the conclusion of the S₇ state, at which time the absolute address obtained by means of manipulations performed upon the relative address portion of the C address field has been stored in third information address register 51, the sequence control unit 15 advances to the S₈ state.

During the S₈ state, combinational gating circuitry within sequence control unit 15 determines whether particular values stored in the AF and BF digit positions of register 19 indicate that indirect field length operations are to be performed. Thus, for example, if the AF digits stored in register 19 are those indicated in FIG. 2A, the combinational gating circuitry of control unit 15 will determine that an indirect field length operation is to be performed. This operation is indicated in the embodiment described by virtue of binary "1's" being stored in the eight-bit location and four-bit location of digit D3 of FIG. 2A. Upon determining that an indirect field length operation is to be performed, sequence control unit 15 advances to state S₁₂.

During state S₁₂, digit D4 of FIG. 2A and the binary values stored in the two-bit and one-bit locations of digit D3 of FIG. 2A are transferred via gate 52 to circuitry 24. Sequence control unit 15 next advances to state S₁₃.

During state S₁₃, the base address value stored in register 25 is added via gate 27 to the digital value just transferred from register 19 to circuitry 24. Thus, if the digital value "16" shown in FIG. 2A and a base address value "120000" are assumed to be added during state S₁₃ the resulting address stored in circuitry 24 is "120016." Control unit 15 next advances to state S₁₄.

During state S₁₄, the address stored in circuitry 24 as a result of the last mentioned manipulations is transferred to register 12 via gate 53. During a subsequent SP signal the digital values stored in address "120016" and in a succeeding address "120017" are read from memory 11 and stored in register 13. Control unit 15 next advances to state S₁₅.

During state S₁₅, the two digital values stored in register 13 are transferred via gate 54 to register 19 and stored in register 19 in the digit positions of the two variant digits which previously had indicated that an indirect field length operation was to be performed. The control unit 15 is now reset to state S₈.

During the succeeding S₈ state, combinational gating circuitry within control unit 15 determines whether the variant digits now stored in register 19 indicate that an indirect field length operation is to be performed. If the newly inserted variant digits in register 19 indicate that a second indirect field length operation is to be performed, this operation is again performed during states S₁₂ through S₁₅, as just described. Thus, for example, if the newly inserted variant digits are those shown in FIG. 2B, a second indirect field length operation is specified and the two digital values stored in memory at addresses "120038" and "120039" will replace the variant digits in register 19 previously inserted therein from addresses "120016" and "120017." Subsequent to the transfer of digits at addresses "120038" and "120039" into the variant digit positions of register 19, sequence control unit 15 is again reset to the S₈ state. If the newly inserted variant digits now stored

in register 19 are assumed to be those indicated in FIG. 2C, the combinational gating circuitry of control unit 15 will determine during state S_8 that no further indirect field length operations are to be performed. At this point the fetch phase of operation is completed and the execution of the particular instruction fetched may commence.

It may be seen that while indirect field length operations may be performed a number of times during a single fetch phase of operation, the total number of such operations during a single fetch is limited. This results since only a limited number of different absolute addresses may be generated during the indirect field length operation. The number of such addresses is limited in the embodiment described to forty. This results since the number of different addresses is determined solely by the values stored in the two-bit location and one-bit location of digit D3 and by the value of digit D4, as shown in FIGS. 2A, 2B, and 2C. Since the number of different digital values which may be assumed by these bits is "40," the maximum number of indirect field length operations which may be performed during a single instruction fetch is also "40," and should it occur that more than forty such indirect field length operations take place, a system error would thereby be indicated. Thus, counting circuit 55 is shown in FIG. 3. Circuit 55 is a conventional counting circuit arranged to generate an error signal upon being counted to "41." The circuit is cleared by the signal generated by control unit 15 during state S_1 and is counted up by "one" each time control unit 15 reaches state S_{12} . Thus, if more than forty indirect field length operations ever take place during a single fetch operation, an error signal generated by circuit 55 will indicate that a system error has occurred.

In other embodiments of the present invention it may be advantageous to use only twenty of the forty different digital values which may be assumed by the two-bit location and one-bit location of digit D3 and by the value of digit D4; for example, the twenty "even" values. Since two digital values stored in adjacent addresses of memory 11 are substituted as new variant digits during an indirect field length operation, it is advantageous from a speed standpoint to read them from the memory simultaneously. In some memory configurations, it is possible to read two addresses simultaneously only when the memory address register stores an even (or odd, as the case may be) valued address. For such configurations the number of different digital values of the two-bit location and one-bit location of digit D3 and by the value of digit D4 are advantageously restricted to twenty.

An alternative or additional error detection means may be provided by determining the maximum length of time which any command may require and by means for providing an error signal whenever the same operation code bits remain in register 19 for more than a predetermined maximum length of time.

Although the embodiment of FIG. 3 has been described in connection with the fetch of a four syllable instruction in which an indirect field length operation has been indicated by particular values stored in the AF variant digits, it is apparent that an indirect field length operation could also be indicated by particular values stored in the BF variant digits. Additionally, the digits indicative of an indirect field length operation may appear in instructions of varying length and format.

What has been described is considered to be only one illustrative embodiment of the present invention. Accordingly, it is to be understood that various and numerous other arrangements may be devised by one skilled in the art without departing from the spirit and scope of the invention.

What is claimed is:

1. A data processing system comprising:

memory means for storing a plurality of binary coded words including a plurality of data words and a plurality of instruction words;

each of the words comprising a plurality of individually addressable digits;

a first register storing the address of a first instruction word stored in the memory;

the first instruction word comprising a plurality of digits including a first plurality of variant digits and a first plurality of address field digits;

means coupled to the memory means and responsive to the contents of the first register for transferring to a second register the first plurality of variant digits;

particular binary values stored in first particular bit locations of the first plurality of variant digits indicating that the first plurality of variant digits indicate an address in memory of the first digit of a

second plurality of variant digits, the second plurality of variant digits manifesting the length of a data word associated with the first plurality of address field digits;

the absence of the particular binary values indicating that the first plurality of variant digits manifest the length of the data word associated with the first plurality of address field digits;

means coupled to the second register for determining the presence of the particular binary values; and

means, responsive to a determination by the last-mentioned means of the presence of the particular binary values, for transferring to the second register the second plurality of variant digits.

2. A data processing system according to claim 1 in which the last-mentioned means comprises:

means coupled to the second register and responsive to a determination of the presence of the particular binary values for transferring particular bits of the first plurality of variant digits to a third register;

a base address register having a predetermined digital value stored therein;

means for adding the contents of the base address register to the contents of the third register thereby producing an absolute address, the absolute address being the address of the first digit of the second plurality of variant digits; and

means including the means coupled to the memory means and utilizing the absolute address for transferring the second plurality of variant digits to the second register.

3. A data processing system according to claim 2 in which the means for transferring particular bits of the first plurality of variant digits transfers to the third register all bits of the first plurality of variant digits other than the bits stored in the first particular bit positions.

4. A data processing system comprising:

memory means for storing a plurality of instruction words, each instruction word comprising operation bits, variant bits and address field bits arranged in a plurality of individually addressable syllables;

a first register storing the address of the first syllable of a first instruction word stored in the memory;

means coupled to the memory means and responsive to the contents of the first register for transferring to a second register the first syllable of the first instruction word, the first syllable including the variant bits of the first instruction word;

a first address field of the first instruction word having particular ones of the variant bits associated therewith; and

means for altering the particular variant bits associated with the first address field comprising:

means coupled to the second register and responsive to a particular value manifested by particular ones of the variant bits associated with the first address field for transferring remaining ones of the variant bits to a third register;

means coupled to the third register for performing predetermined manipulations upon the bits transferred

to the third register thereby obtaining an address of alternative variant bits stored in the memory; and means including the means coupled to the memory means for substituting the alternative variant bits into the second register as new variant bits associated with the first address field.

5. A data processing system comprising:

memory means for storing a plurality of binary coded words including a plurality of data words and a plurality of instruction words, each of the words comprising individually addressable digits; the instruction words including operation code digits, variant digits and address field digits;

a first register storing the address of the first digit of a first instruction word stored in the memory;

means coupled to the memory means and responsive to the contents of the first register for transferring to a second register the variant digits of the first instruction word;

means coupled to the second register and utilizing bits stored in particular first bit positions of the variant digits for determining whether the variant digits represent the field length of a particular data word;

means, responsive to a determination by the last-mentioned means that the variant digits do not represent the field length of the particular data word, for transferring bits stored in particular second bit positions of the variant digits to a third register;

means coupled to the third register for performing predetermined manipulations upon the bits transferred to the third register thereby obtaining an address of alternative variant digits stored in the memory and for storing this address in the first register, the alternative digits being representative of the field length of the particular data word; and

means including the means coupled to the memory means for transferring the alternative variant digits to the second register.

6. A data processing system comprising:

memory means for storing a plurality of binary coded words including a plurality of data words and a plurality of instruction words;

each of the words comprising individually addressable digits, a particular number of such digits constituting a syllable;

a first register storing the address of the first digit of a first instruction word stored in the memory;

the first instruction word comprising first, second, and third syllables;

the first syllable including a plurality of operation code digits, a first plurality of variant digits, and a second plurality of variant digits; the first plurality of variant digits being associated with the second syllable, and the second plurality of variant digits being associated with the third syllable;

means coupled to the memory means and responsive to the contents of the first register for transferring to a second register the first syllable of the first instruction word;

the absence of particular binary values stored in first particular bit locations of the first plurality of variant digits indicating that the first plurality of variant digits manifest the length of a first data word associated with the second syllable;

the presence of the particular binary values indicating that the first plurality of variant digits manifest an address in memory whereat a third plurality of variant digits is stored;

the second plurality of variant digits manifesting the length of a second data word associated with the third syllable;

means coupled to the second register for determining the presence in the first variant digits of the particular binary values stored in the first particular bit locations of the first plurality of variant digits;

means coupled to the second register and responsive to a determination of the presence of the particular binary values for storing in the first register the address of the third plurality of variant digits; and means including the means coupled to the memory means for substituting the third plurality of variant digits for the first plurality of variant digits in the second register.

7. A data processing system comprising:

memory means for storing a plurality of binary coded words including a plurality of data words and a plurality of instruction words;

each of the words comprising a plurality of individually addressable digits;

a first register storing the address of a first instruction word stored in the memory;

the first instruction word comprising a plurality of digits including a first plurality of variant digits and a first plurality of address field digits;

means coupled to the memory means and responsive to the contents of the first register for transferring to a second register the first plurality of variant digits; particular binary values stored in first particular bit locations of the first plurality of variant digits indicating that the first plurality of variant digits represent an address in memory of the first digit of a second plurality of variant digits;

the absence of the particular values indicating that the first plurality of variant digits manifest the length of a data word associated with the first plurality of address field digits;

means coupled to the second register for determining the presence of the particular binary values in the first particular bit locations of the first plurality of variant digits;

means coupled to the second register and responsive to a determination of the presence of the particular binary values for storing in the first register the address of the second plurality of variant digits;

means including the means coupled to the memory means for transferring to the second register the second plurality of variant digits;

particular binary values stored in the first particular bit locations of the second plurality of variant digits indicating that the second plurality of variant digits represent an address in memory of the first digit of a third plurality of variant digits, the third plurality of variant digits manifesting the length of a data word associated with the first plurality of address field digits;

the absence of the particular binary values indicating that the second plurality of variant digits manifest the length of the data word associated with the first plurality of address field digits;

the determining means determining the presence of the particular binary values in the first particular bit locations of the second plurality of variant digits; the means responsive to a determination of the presence of the particular binary values determining the presence of these binary values in the first particular bit locations of the second plurality of variant digits and storing in the first register the address of the third plurality of variant digits; and

the last-mentioned transferring means transferring to the second register the third plurality of variant digits.

8. A data processing system comprising:

memory means for storing a plurality of binary coded words including a plurality of data words and a plurality of instruction words;

each of the words comprising individually addressable digits, a particular number of such digits constituting a syllable;

a first register storing the address of the first digit of a first instruction word stored in the memory;

the first instruction word comprising first, second, and third syllables;
 the first syllable including a plurality of operation code digits, a first plurality of variant digits and a second plurality of variant digits; the first plurality of variant digits being associated with the second syllable and the second plurality of variant digits being associated with the third syllable;
 means for transferring to a second register the first syllable of the first instruction word;
 means for transferring to a third register particular digits of the second syllable of the first instruction word;
 means for performing predetermined manipulations upon the digits stored in the third register;
 means for transferring to a first data address register the digital value resulting from the last mentioned manipulations, the digital value thereby stored in the first data address register being the address of the first digit of a first data word;
 the aforesaid means for transferring to the third register transferring particular digits of the third syllable of the first instruction word to the third register;
 the performing means performing predetermined manipulations upon the digits stored in the third register;
 means for transferring to a second data address register the digital value resulting from the last mentioned manipulations, the digital value thereby stored in the second data address register being the address of the first digit of a second data word;
 particular binary values stored in first particular bit locations of one of the first and second plurality of variant digits determining that the one of these pluralities having such particular binary values stored therein indicates an address in memory of the first digit of a third plurality of variant digits;
 means for determining the presence of the particular binary values; and
 means, responsive to a determination of the presence of the particular binary values, for transferring to the second register the third plurality of variant digits.
 9. A data processing system comprising:
 memory means for storing a plurality of binary coded words including a plurality of data words and a plurality of instruction words;
 each of the words comprising individually addressable digits m , such digits constituting a syllable;
 a first register storing the address of the first digit of a first instruction word stored in the memory; the address consisting of m digits;

the first instruction word comprising first, second, and third syllables;
 the first syllable consisting of n operation code digits, a first group of o variant digits, and a second group of o variant digits; the first group of o variant digits being associated with the second syllable and the second group of o variant digits being associated with the third syllable;
 means for transferring to a second register the first syllable of the first instruction word;
 means for transferring to a third register particular p digits of the second syllable of the first instruction word;
 means for performing predetermined manipulations upon the p digits stored in the third register which produce a m -digit address;
 means for transferring to a first data address register the m -digit address resulting from the last mentioned manipulations, this address being the address of the first digit of a first data word;
 the aforesaid means for transferring to the third register transferring particular p digits of the third syllable of the first instruction word to the third register;
 the performing means performing predetermined manipulations upon the digits stored in the third register, another m -digit address resulting therefrom;
 means for transferring to a second data address register the m -digit address resulting from the last mentioned manipulations, this address being the address of the first digit of a second data word;
 particular binary values stored in particular q bit locations of one of the first and second groups of o variant digits determining that the one of these groups having such particular binary values stored therein indicates an address in memory of the first digit of a third group of o variant digits;
 means for determining the presence of the particular binary values stored in the particular q bit locations; and
 means, responsive to a determination of the presence of the particular binary values, for transferring to the second register the third group of o variant digits.

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