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(54) **Title**: A METHOD OF OPERATING A SPLIT GATE FLASH MEMORY CELL WITH COUPLING GATE

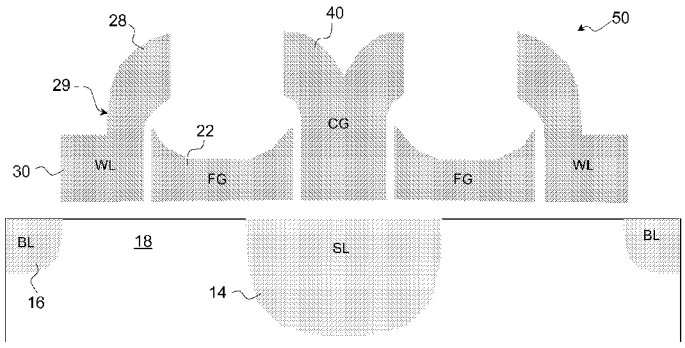

FIGURE 1

(57) **Abstract**: A method of operating a memory cell that comprises first and second regions spaced apart in a substrate with a channel region therebetween, a floating gate disposed over the channel region and the first region, a control gate disposed over the channel region and laterally adjacent to the floating gate with a portion disposed over the floating gate, and a coupling gate disposed over the first region and laterally adjacent to the floating gate. A method of erasing the memory cell includes applying a positive voltage to the control gate and a negative voltage to the coupling gate. A method of reading the memory cell includes applying positive voltages to the control gate, to the coupling gate, and to one of the first and second regions.

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A METHOD OF OPERATING A SPLIT GATE FLASH MEMORY CELL WITH COUPLING GATE

RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 61/485,805, filed May 13, 2011, and which is incorporated herein by reference.

TECHNICAL FIELD

[0002] The present invention relates to a split gate flash memory cell and more particularly to a method of operating a split gate flash memory cell with a coupling gate to enhance the operations of read and erase.

BACKGROUND OF THE INVENTION

[0003] Split gate flash memory cells are well known in the art. One such well known example is disclosed in U.S. Patent 5,029,130 whose disclosure is incorporated herein by reference in its entirety.

[0004] As shown in Figure 1 of U.S. Patent 5,029,130, a split gate flash memory cell 10 comprises a semiconductor substrate 12, with a first conductivity type, such as P. A first region 14 of a second conductivity type, such as N is along the surface of the substrate 12. Spaced apart from the first region 14 is a second region 16 also of the second conductivity type N. Between the first region 14 and the second region 16 is a channel region 18. A floating gate 22 is positioned over a portion of the channel region 18 and over the first region 14 and is capacitively coupled to the first region 14. A control gate 29 has two portions: a first portion 30 is laterally adjacent to the floating gate 22 and is disposed over another portion of the channel region 18, and has little or no overlap with the second region 16. The control gate 29 has a second portion 28 which is connected to the first portion 30 and is disposed over the floating gate 22 (only extends part way over floating gate 22 to reduce capacitive coupling therebetween – i.e. only a weak capacitive coupling therebetween).

[0005] During the read operation, a zero or near zero voltage is applied to the second region 16, with a first positive voltage applied to the first region 14. A second positive voltage is applied to the control gate 29 turning on the portion of the channel region 18 underneath the

control gate 29. In the event the floating gate is programmed, i.e. has stored electron charges, then the positive voltage on the control gate 29 and the positive voltage on the first region 14 are not sufficient to turn on the portion of the channel region 18 underneath the floating gate 22. The low or zero current through the channel region is detected as a first state (e.g. a 1). However, if the floating gate 22 is not programmed (i.e. it lacks stored electron charges), then the positive voltage on the control gate 29 and the positive voltage on the first region 14 are sufficient to cause the floating gate 22 to be capacitively coupled to a more positive voltage, which turns on the portion of the channel region 18 underneath the floating gate 22, thereby turning on the entire channel region 18. The current through the channel region is detected as a second state (e.g. a 0). However, as cell size has shrunk, and dimensions reduced, and the voltages lowered, increasingly it becomes difficult to turn the floating gate 22 on when it is erased. After program-erase cycling, the potential of the floating gate 22 of the erased cell becomes even lower because of electron charge trapping in the tunnel oxide (separating the floating gate 22 and control gate 29) and thus the corresponding decrease of tunneling efficiency. Thus, it is desired to have an additional gate to assist during the read operation, and still be process compatible with the above-described cell.

[0006] U.S. Patents 6,855,980 and 7,315,056 each disclose a flash memory cell with a floating gate, a control gate to one side thereof and an assist gate over the first region to another side of the floating gate. However, these two patents (whose disclosures are incorporated herein by reference in their entirety) do not disclose the method of using that cell to enhance read and erase operations.

[0007] Accordingly, it is one object of the present invention to provide a method of operating a cell during read and erase operations.

SUMMARY OF THE INVENTION

[0008] In the present invention, a method of operating a flash memory cell of the type having a substrate of a first conductivity, with a first region of a second type of conductivity along a surface of the substrate. A second region of the second conductivity type is spaced apart from the first region with a channel region therebetween. A floating gate is disposed over a first portion of the channel region, and over a portion of the first region and is capacitively coupled thereto. A control gate is to one side of the floating gate. The control gate has two portions: a first portion that is disposed over a second portion of the channel region and has little or no

over lap with the second region and is laterally adjacent to the floating gate, and a second portion that is disposed over the floating gate (preferably extending only partially over the floating gate to so there is minimal capacitive coupling therewith). A coupling gate is laterally adjacent to the floating gate to another side thereof and is over the first region, and is capacitively coupled to the floating gate. In the method of the present invention, a read operation is accomplished by applying a first positive voltage to both the control gate and to the coupling gate while a voltage differential is applied between the first region and the second region. In the event the floating gate is not programmed, the first positive voltage causes the channel region underneath the floating gate to be turned on, whereas if the floating gate is programmed, the first positive voltage is insufficient to cause the portion of the channel region underneath the floating gate to be turned on. In an erase operation, the first and second regions are supplied with ground voltage while a negative voltage is applied to the coupling gate and a second positive voltage is applied to the control gate. Because a negative voltage is applied to the coupling gate, and due to the strong capacitive coupling between the coupling gate and its adjacent floating gate, the second positive voltage can be lower than if no negative voltage were applied to the coupling gate. Finally, in a method of programming, a third positive voltage is applied to the first region, while a ground or low positive voltage (lower than Vcc) is applied to the second region. A voltage is applied to the control gate sufficient to turn on the channel region underneath the control gate. Electrons are then accelerated from the second region to the first region and as they near the junction of the floating gate they are abruptly injected onto the floating gate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figure 1 is a cross sectional schematic diagram of a flash memory cell to which the method of the present invention may be used.

DETAILED DESCRIPTION OF THE INVENTION

[0010] Referring to Figure 1, there is shown a schematic diagram of a flash memory cell 50 to which the method of the present invention can be used. Because the flash memory cell 50 is similar to the flash cell 10 disclosed in U.S. Patent 5,029,130, like numbers will be used to designate like parts. The cell 50 is formed in a substrate 12 of a first conductivity, such as P type. The substrate 12 has a surface. Along the surface is a first region 14 of a second

conductivity type, such N. A second region 16 of the second conductivity type N is also along the surface of the substrate 12 and is spaced apart from the first region 14. A channel region 18 is between the first region 14 and the second region 16. A floating gate 22 is disposed over and insulated from a first portion of the channel region 18 and a portion of the first region 14, and is capacitively coupled thereto. A control gate or word line WL 29 is adjacent to the floating gate 22 to one side and is insulated therefrom. The control gate 29 has two portions: first portion 30 and second portion 28. The control gate first portion 30 is laterally adjacent to the floating gate 22, and is also insulated and over a second portion of the channel region 18, and has little or no overlap with the second region 16. The control gate second portion 28 is disposed over a portion of the floating gate 22 and has minimal capacitive coupling with the floating gate 22 by virtue of the relatively small portion of floating gate 22 that is vertically overlapped by control gate second portion 28. Finally, a coupling gate CG 40 is laterally adjacent to another side of the floating gate 22 and is insulated from the floating gate 22. The coupling gate 40 is also disposed over the first region 14 and is insulated therefrom.

[0011] In the operation of the cell 50, the following voltages can be applied. For a read operation:

Control Gate WL 29	Coupling Gate CG 40	Second Region 16	First Region 14
2.5 v, or voltage sufficient to turn on the portion of the channel region 18 underneath the control gate 29	Same as control gate 29	1.0 v	0 v

The positive voltage applied to second region 16 could instead be applied to first region 14.

[0012] The following voltages can be applied for an erase operation.

Control Gate WL 29	Coupling Gate CG 40	Second Region 16	First Region 14
positive voltage (< 10 v)	negative voltage (< 0 v)	0 v	0 v

[0013] The following voltages can be applied for a programming operation.

Control Gate 29	Coupling Gate 40	Second Region 16	First Region 14
Less than Vcc but sufficient to turn on the portion of the channel region 18 underneath the control gate 29	Vcc	5-10 uA, or a ground or low positive voltage (lower than Vcc)	9.0 v

[0014] From the foregoing the following advantages of the method of the present invention can be seen.

[0015] First, during a read operation, because there is increased capacitive coupling between the coupling gate 40 and the floating gate 22, there is greater assurance of read accuracy and increase in signal to noise ratio is obtained. Second during an erase operation, because there is increased capacitive coupling between the coupling gate 40 and the floating gate 22, the tunneling layer between the floating gate 22 and the control gate 29 can be scaled thinner. This would improve the trap up and thereby improving the endurance.

[0016] It is to be understood that the present invention is not limited to the embodiment(s) described above and illustrated herein, but encompasses any and all variations falling within the scope of the appended claims. For example, references to the present invention herein are not intended to limit the scope of any claim or claim term, but instead merely make reference to one or more features that may be covered by one or more of the claims.

[0017] It should be noted that, as used herein, the terms "over" and "on" both inclusively include "directly on" (no intermediate materials, elements or space disposed therebetween) and "indirectly on" (intermediate materials, elements or space disposed therebetween). Likewise, the term "adjacent" includes "directly adjacent" (no intermediate materials, elements or space disposed therebetween) and "indirectly adjacent" (intermediate materials, elements or space

disposed there between), "mounted to" includes "directly mounted to" (no intermediate materials, elements or space disposed there between) and "indirectly mounted to" (intermediate materials, elements or spaced disposed there between), and "electrically coupled" includes "directly electrically coupled to" (no intermediate materials or elements there between that electrically connect the elements together) and "indirectly electrically coupled to" (intermediate materials or elements there between that electrically connect the elements together). For example, forming an element "over a substrate" can include forming the element directly on the substrate with no intermediate materials/elements therebetween, as well as forming the element indirectly on the substrate with one or more intermediate materials/elements therebetween.

What is claimed is:

1. A method of erasing a memory cell that comprises a substrate of a first conductivity type, first and second regions spaced apart in the substrate of a second conductivity type which define a channel region in the substrate therebetween, a floating gate disposed over and insulated from a first portion of the channel region and the first region, a control gate having first and second portions, wherein the control gate first portion is disposed over and insulated from a second portion of the channel region and is disposed laterally adjacent to and insulated from the floating gate, wherein the control gate second portion is disposed over and insulated from the floating gate, and a coupling gate disposed over and insulated from the first region and laterally adjacent to and insulated from the floating gate, the method comprising:

applying a positive voltage to the control gate; and

applying a negative voltage to the coupling gate.

2. The method of claim 1, further comprising:

applying a ground voltage to the first and second regions.

3. The method of claim 1, wherein the positive voltage applied to the control gate is less than 10 volts.

4. A method of reading a memory cell that comprises a substrate of a first conductivity type, first and second regions spaced apart in the substrate of a second conductivity type which define a channel region in the substrate therebetween, a floating gate disposed over and insulated from a first portion of the channel region and the first region, a control gate having first and second portions, wherein the control gate first portion is disposed over and insulated from a second portion of the channel region and is disposed laterally adjacent to and insulated from the floating gate, wherein the control gate second portion is disposed over and insulated from the floating gate, and a coupling gate disposed over and insulated from the first region and laterally adjacent to and insulated from the floating gate, the method comprising:

applying a positive voltage to the control gate;

applying a positive voltage to the coupling gate; and

applying a positive voltage to one of the first and second regions.

5. The method of claim 4, wherein the positive voltage applied to the control gate is equal to the positive voltage applied to the coupling gate.

6. The method of claim 4, further comprising:

applying a ground voltage to the other one of the first and second regions.

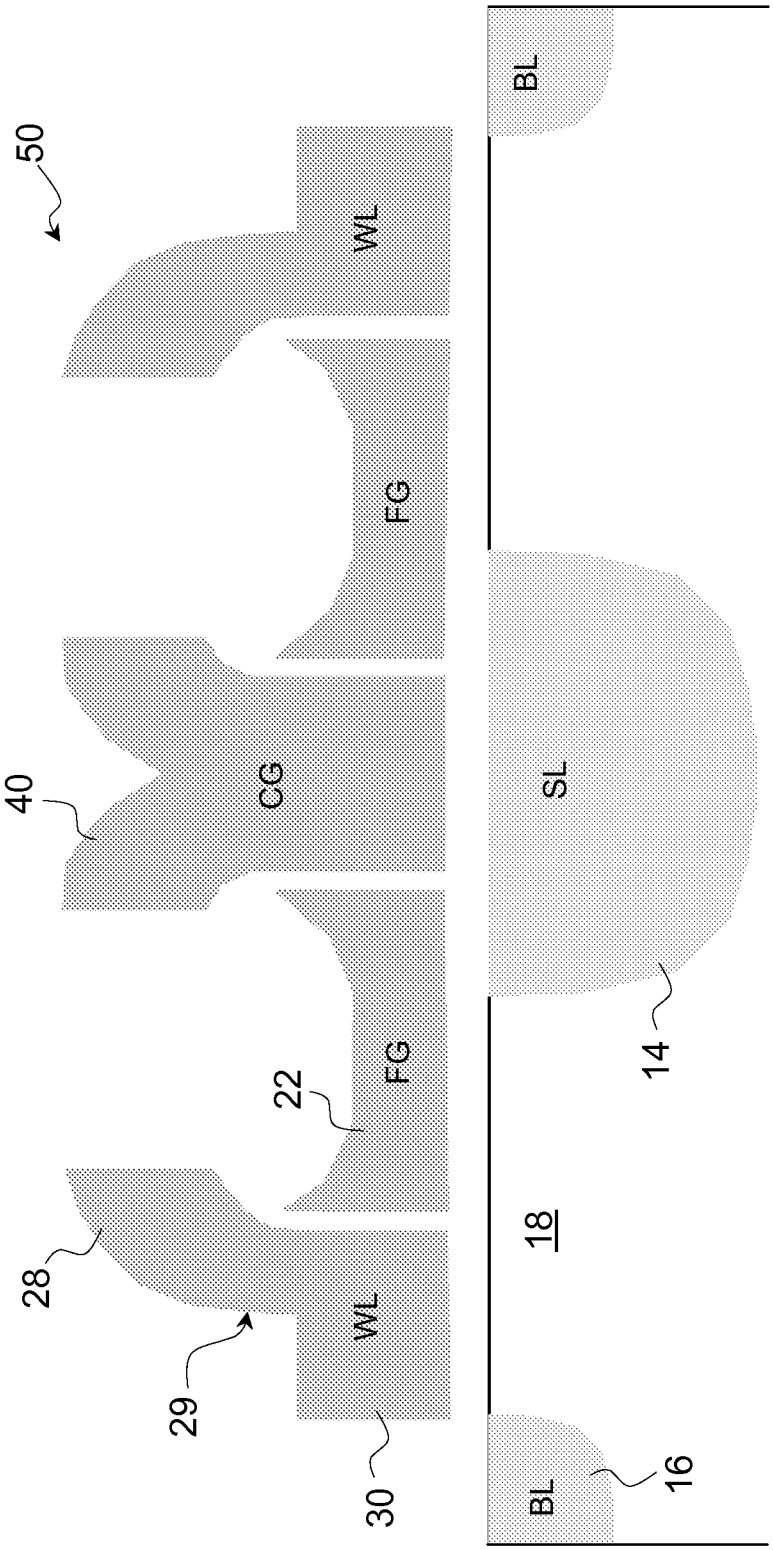

FIGURE 1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 12/36452

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G06F 13/00 (2012.01)
USPC - 711/100
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 711/100

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 711/100-106

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Dialogweb (INSPEC, NTIS, PASCAL, INPADOC, European Patents full test, WIPO/PCT Patents Fulltext, Derwent WPI, French Patents, US Patents Fulltext); Search terms used: voltage, conductivity, flash memory, floating gate, control gate, word line, coupling gate, erase, read

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 6,788,573 B2 (Choi) 07 September 2004 (07.09.2004), Fig. 3D, 4D, col. 10, ln 43-65, col. 13 ln. 5 to col. 14, ln. 44	1, 3 --- 2, 5
X -- Y	US 2009/0141562 A1 (Jeon et al.) 04 June 2009 (04.06.2009), Fig. 7, Table 1, para [0039] - [0047]	4, 6 --- 2, 5

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 June 2012 (15.06.2012)	13 JUL 2012
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

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